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Supplementary information

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ITO-free silicon-integrated perovskite electrochemical cell for light-emission and light-detection

Maria Baeva[1,2,3], Dmitry Gets[2], Artem Polushkin[2], Aleksandr Vorobyov[1], Aleksandr Goltaev[1], Vladimir Neplokh[1,4], Alexey Mozharov[1], Dmitry V. Krasnikov[5], Albert G. Nasibulin[5], Ivan Mukhin[1,4]* and Sergey Makarov[2,6]*

[1]Alferov University, Khlopina 8/3, St. Petersburg 194021, Russia; [2]Department of Physics and Engineering, ITMO University, Lomonosova 9, St. Petersburg 197101, Russia; [3]Institute of Automation and Control Processes (IACP), Far Eastern Branch of Russian Academy of Sciences, Ulitsa Radio 5, Vladivostok 690041, Primorsky Krai, Russia; [4]Peter the Great St. Petersburg Polytechnic University, Polytechnicheskaya 29, St. Petersburg 195251, Russia; [5]Skolkovo Institute of Science and Technology, Nobel 3, Moscow 121205, Russia; [6]Qingdao Innovation and Development Center, Harbin Engineering University, Qingdao 266000, Shandong, China.

*Correspondence: I Mukhin, E-mail: imukhin@yandex.ru; S Makarov, E-mail: s.makarov@metalab.ifmo.ru

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Section 1: Band diagram simulation details

Table S1 | Materials parameters.

	$CsPbBr_3$	Si
Structure properties		
Energy band gap (eV)	2.31	1.12
Electron affinity (eV)	4.17	4.05
Electron effective mass	0.171 m_0	0.36 m_0
Hole effective mass	0.172 m_0	0.81 m_0
Dielectric constant	7.3	11.7
Transport properties		
Electron mobility ($cm^2/(V*s)$)	52	100
Hole mobility ($cm^2/(V*s)$)	11	50
Electron lifetime (ns)	120	30
Hole lifetime (ns)	120	30
Radiative recombination factor (cm^3/s)	5.4×10^{-10}	1.1×10^{-14}

Section 2: Perovskite layer light extraction direction simulation details

Taking that the PeLEC operates in a spontaneous emission regime, we consider an optical point-dipole with a variable over 360° (during calculations) azimuth orientation being placed inside of the perovskite layer as a light emission source. In the SI Fig. S1(a) there is a combined PeLEC's light emission extraction curve versus the point-dipole orientation, where along the substrate surface (viz. at small angles) the maximum extraction efficiency of ~ 13% is achieved. With point-dipole orientation angle increment an abrupt drop in extraction efficiency is observed. According to the emitted light electric field vector modulus map, see SI Fig. S1(b), for smaller angles (< 45°), which make the most contribution to the extraction efficiency, angular distribution similar to isotropic is observed. In such cases, we were able to average the extraction efficiency over the point-dipole orientation angle and determine the mean extraction efficiency, which, when taking into consideration the azimuth angle, constitutes 9.2%. Hence, the experimentally observed data can be explained by the assumption that most of the PeLEC's light emission gets absorbed by the Si substrate.

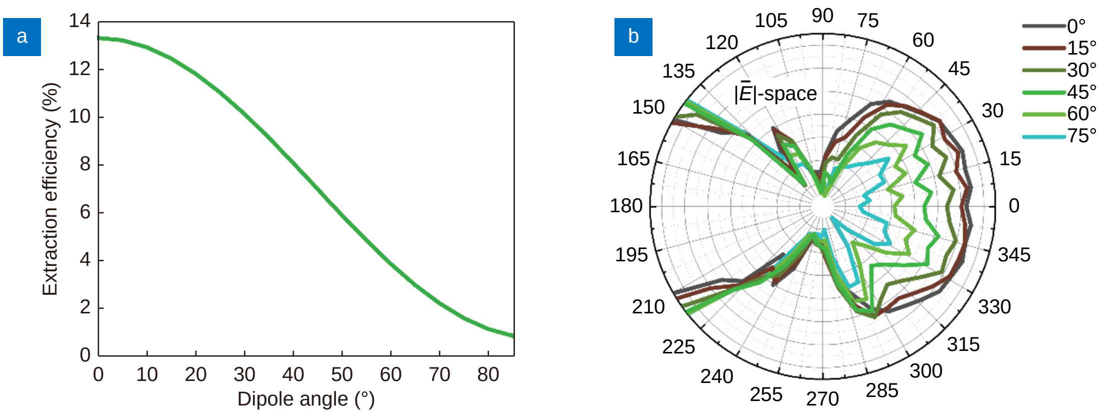

Fig. S1 | (**a**) The PeLEC' emitted light extraction efficiency versus point-dipole orientation angle. (**b**) PeLEC's emitted light electric field vector modulus map at different point-dipole orientations.

Section 3: Laser power density comparison

Table S2 | 450 nm laser incident power density compared to equivalent (eqv.) to one sun power density at 450 nm and to integral (int.) one sun power density.

P (mW)	Power density (mW/cm²)	# of suns (eqv)(counts)	# of suns (int)(counts)
6.38	405.85	18.45	4.06
2.54	161.57	7.34	1.62
1.27	80.98	3.68	0.81
0.25	16.16	0.73	0.16
0.025	1.61	0.07	0.02

Section 4: Avalanche photodiode breakdown voltage fit

$U_{\rm ch}$—avalanche photodiode breakdown voltage—is derived from avalanche photodiode current multiplication equation—$I=\frac{I_0}{1-a*L*\exp(-\left(\frac{|U_{ch}|}{|U|}\right)^m)}$, where I is total current density, I_0 - photocurrent, a - impact ionization coefficient, L - perovskite thickness, $U_{\rm ch}$ - avalanche photodiode breakdown voltage, U - applied to the PeLEC bias. In Fig. S2 we show our experimental data in good agreement with the avalanche photodiode current multiplication equation.

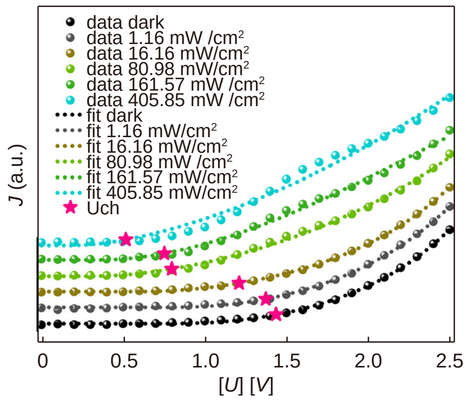

Fig. S2 | PeLEC J-V curve reverse bias branch fit to the avalanche photodiode current multiplication equation.

Section 5: Heat distribution simulation details

We numerically analyzed two perovskite devices: one synthesized on Si substrate 380 μm thick, another—on soda-lime glass 1 mm thick. In a framework of the current thermal problem we considered substrates' and substrate-holder (e.g. iron table) thermal conductivities as well as thermal air convection. The heat source was set to be at the substrate/air interface, which, due to the negligible perovskite layer thickness (compared to the substrate thickness) and Si substrate absorbing the emitted light, corresponds well with the situation in the real experimental system. Defining the heat source power inside of our thermal problem framework, we accounted for experimental data on applied electrical power (139.3 mW for Si; 207 mW for soda-lime glass), low emitted light extraction efficiency (for Si substrate), alongside anticipated IQE value of 60%. We assume that the Si substrate/iron table interface is a perfect contact, where there are no barriers for heat dissipation. That would correspond to attaching the Si substrate backside to the iron table surface with a thin layer of metal conductive glue or easily fusible metal; in reality, the Si substrate was attached to the poorly thermo-conducting material table.

With all of these assumptions, thermal heating power is estimated to be 84 mW and 198 mW for soda-lime glass substrate and Si substrate, respectively. Thus, in our numerical calculations the system on Si substrate emits 2.5 times more heat than the system on soda-lime glass. The numerically simulated maps to compare the two studied systems are given in Fig. S2(a) and S2(b). It can be seen that in the soda-lime substrate case the active region temperature increases by 7 °C compared to the ambient temperature, as for the Si substrate case this temperature increment constitutes only 1 °C.

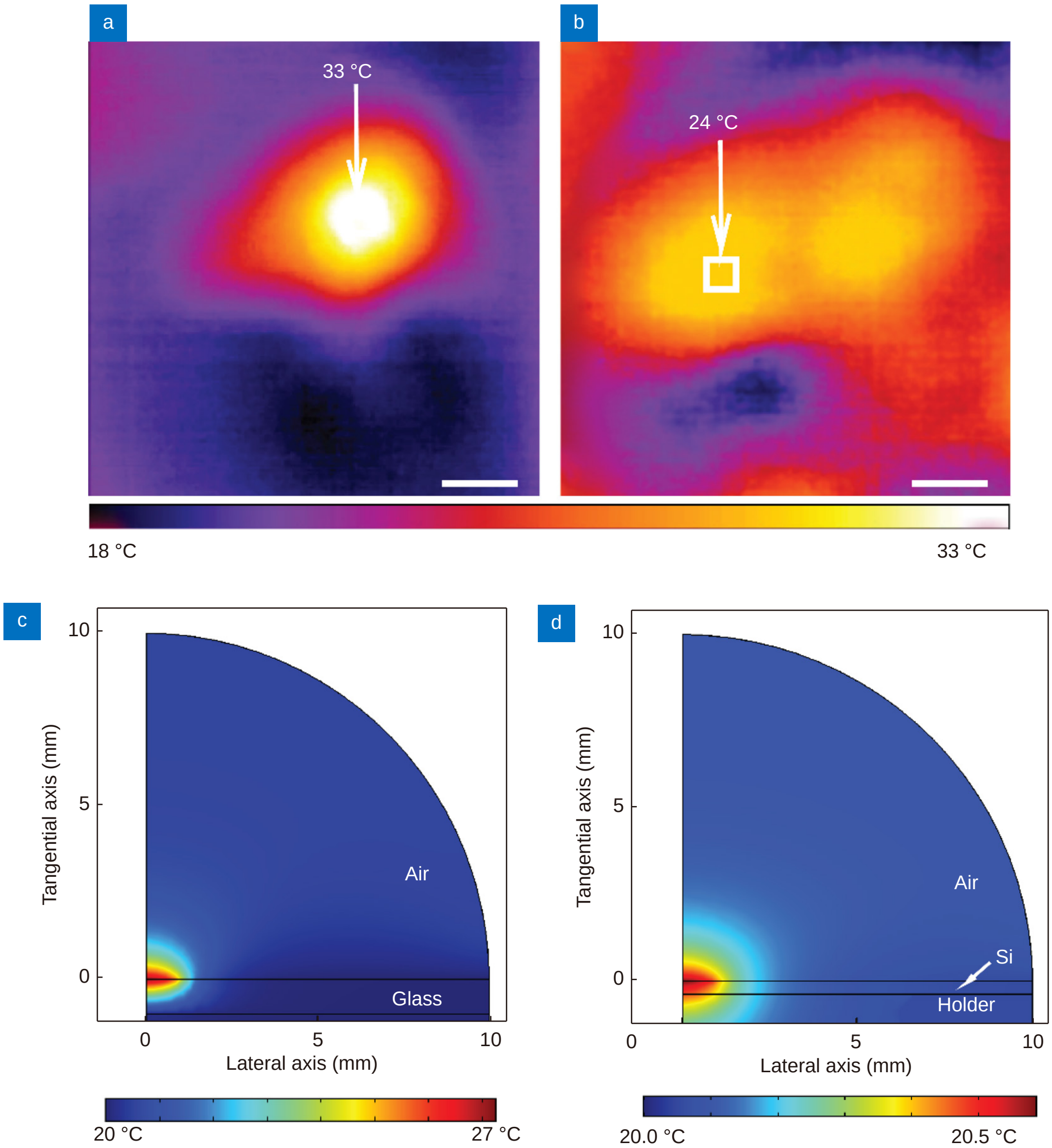

Fig. S3 | IR images of in-operation heat dissipation in PeLEC devices on (**a**) soda-lime glass substrate and (**b**) Si substrate; simulated heat distribution maps for (**c**) soda-lime glass and (**d**) Si substrates. Scale bars in (a) and (b)– 5 mm.

In the ideal case (perfect Si substrate/iron table contact), shown in Fig. S3, when the Si substrate thickness increases from 50 μm to 1000 μm the PeLEC pixel temperature drops, due to the increase in Si substrate thermo-conductivity compared to the iron table. Silicon provides lateral distribution of heat and, as a consequence, heat dissipation from the PeLEC pixel. As a rule, the Si wafers for microelectronics and/or photovoltaics thickness rarely exceeds 1 mm, consideration of thicker silicon wafers is excessive.

Analyzing the data, we conclude that there are several scenarios of how things can go when taking into consideration Si substrate/table interface parameters. In a case when the interface lacks the thermo-conductivity compared to Si, the effect will be similar to the one presented above: Si substrate thickness increase will lead to the PeLEC pixel temperature decrease. When the situation is reversed, there most probably will be a complex relationship between the Si substrate thickness and heat dissipation. However, the technical realization of such a situation is costly (due to the utilization of expensive metals) and will be in demand only in the narrow scope of applications.

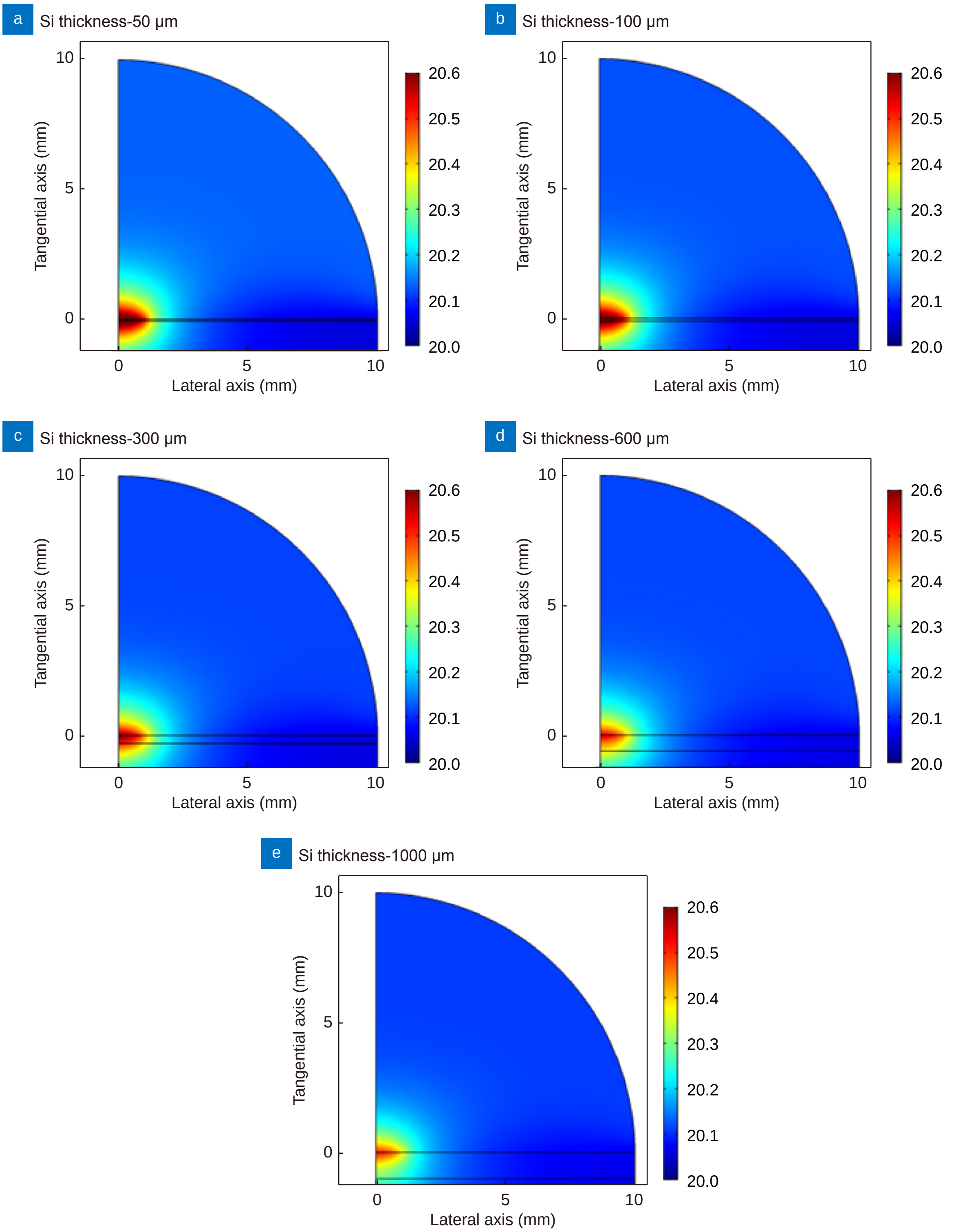

Fig. S4 | Simulated heat distribution maps for Si substrates of the thickness. (**a**) 50 μm. (**b**) 100 μm. (**c**) 300 μm. (**d**) 600 μm. (**e**) 1000 μm.