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An efficient unused integrated circuits detection algorithm for parallel scan architecture

Rekha Sathyanarayana[1], Nataraj Kanathur Ramaswamy[1], Mallikarjunaswamy Srikantaswamy[2], Rekha Kanathur Ramaswamy[3]
[1]Department of Electronics and Communication Engineering, Don Bosco Institute of Technology, Bangalore, India
[2]Department of Electronics and Instrumentation Engineering, JSS Academy of Technical Education, Bangalore, India
[3]Department of Electronics and Communication Engineering, SJB Institute of Technology, Bangalore, India

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ABSTRACT

In recent days, many integrated circuits (ICs) are operated parallelly to increase switching operations in on-chip static random access memory (SRAM) array, due to more complex tasks and parallel operations being executed in many digital systems. Hence, it is important to efficiently identify the long-duration unused ICs in the on-chip SRAM memory array layout and to effectively distribute the task to unused ICs in SRAM memory array. In the present globalization, semiconductor supply chain detection of unused SRAM in large memory arrays is a very difficult task. This also results in reduced lifetime and more power dissipation. To overcome the above-mentioned drawbacks, an efficient unused integrated circuits detection algorithm (ICDA) for parallel scan architecture is proposed to differentiate the '0' and '1' in a larger SRAM memory array. The proposed architecture avoids the unbalancing of '0' and '1' concentrations in the on-chip SRAM memory array and also optimizes the area required for the memory array. As per simulation results, the proposed method is more efficient in terms of reliability, the detection rate in both used and unused ICs and reduction of power dissipation in comparison to conventional methods such as backscattering side-channel analysis (BSCA) and network attached storage (NAS) algorithm.

Corresponding Author:

Mallikarjunaswamy Srikantaswamy
Department of Electronics and Instrumentation Engineering, JSS Academy of Technical Education
Bangalore, Karnataka, India
Email: mallikarjunaswamys@jssateb.ac.in

1. INTRODUCTION

Reusing of integrated circuits (ICs) is considered a biggest threat in electronic systems security and several methods are used detect the used parts. ICs on the printed circuit board (PCB) are considered and it can be introduced to the semiconductor supply chain on a global level. In the boards the obsolete parts are no need to being manufactured and legacy systems is maintained. Due to government budgetary constraints, critical infrastructure is put to the huge part of important infrastructure spare parts supply for steady states [1]. Effect of stress due to temperature on the parts of ICs results in its damage. The electronic waste are handled with care in the condition electrostatic discharges (ESD) protection, and humidity. The Reused parts in the circuits are having the reduced lifetime, low reliability, and degraded in performance [2], [3].

The identification of reused ICs in existing approaches are into the supply chain of electronics system into the classified of several categories. The design-for-anti-counterfeit (DfAC) of first on-chip sensors are proposed to improve the identification of old traditional chips [4], [5]. A major part of vast chips

are already reused by the manufacturer and it is not detected DfAC measures methods. In the literature several conventional methods are recommended [6]–[10]. But these methods are consuming more test time, no automation low detection capability, and critical [11]. The statistical analysis methods are suggested by the researchers for detection of reused parts [12], [13]. However, computation of statistical analysis methods requires huge number of chips. For the detection of reused ICs to be effective, the work proposes effective and novel method using the on-chip static random-access memory (SRAMs) in power-up state. This proposed method effectively detect the chip if it is reused. Each RAM cell is designed using symmetry property in huge memory array. The thermal noise and electrical noise are effectively reduced in the proposed method. The 50% 1s was observed many cells power-up state and 50% of 0 s in SRAM which are unused. But, in the most of older ICs may not embedded with the S-RAMs [14]. A new detection method is proposed in this work to detect reused parts in the logic circuit of the chain. The proposed work is on circuit that contains the flip-flops' power up state (FFs) [15]. The circuit contains only the scanning of parts, for detection and zero extra netlist or information of circuit.

2. BACKGROUND

2.1. Modeling of FF power-up state

A flip-flop is a fundamental building block of digital circuits and is used to store a single binary value (0 or 1). When the circuit is first powered up or reset, the flip-flop can be in an undefined or unpredictable state. Properly handling this power-up state is crucial in digital circuit design to ensure reliable operation. Due to layout's asymmetry of the cell, the D flip-flop (DFF) is not logic 0 or logic 1 unlike the cells of SRAM. This section presents the DFF power-up behavior and impact of variations in manufacturing [16].

2.1.1. FF power-up state

The DFF's typical structure is shown in Figure 1. A clock signal enables the clocked inverters and observe the corresponding output and not enabled state is assumed as a high impedance state [17]. Some flip-flops have an option to specify their initial state through a configuration or initialization signal. This is typically done during the design phase and is not affected by power-up conditions.

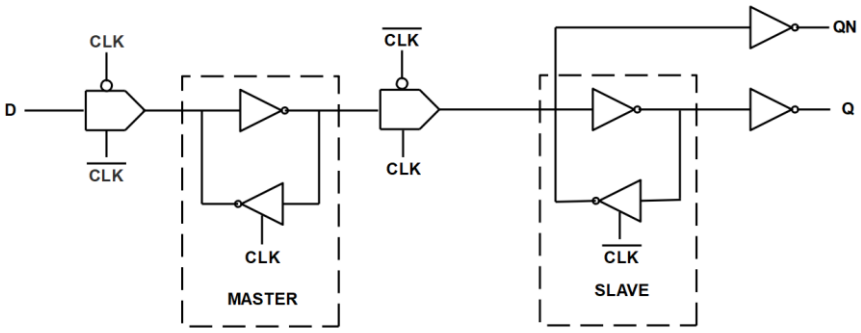


Figure 1. The DFF schematic

The FF's logic state is determined depending on power up sate. The FF's output state is dependent on signal of clock when powered up [18], as seen in Figure 1. The clock signal enables master or slave during its rising or falling edge. From Figure 1, when CLK is high the slave is enabled and CLK is zero master is enabled. Also, correspondingly it produces the output of master or slave in its enabled CLK pulse. By forcing the CLK to the high, the power-up state is captured. In this work we assume the power-up state is captured from slave while CLK is logic 0. Similar analysis can be done for master latch by forcing CLK at logic 1. The DFF of a slave latch simplified schematic. The schematic contains back-to-back connected two inverters. The schematic is a tristate inverter, which is already discussed control by the CLK [19]. The second inverter is designed using the two additional transistors as shown in Figure 2. In the schematic two inverters which are connected back-to-back using the transistors T_1, T_3 and T_2, T_4 and CLK is used to control the transistors T_5 and T_6. The slave latch is need to be isolate from the master by forcing the CLK to be logic 0. Also, CLK=0 is applied consequently for T_5 and T_6 and approximately modelled the channel resistance to the Ron.

Due to the device parameters and transistor sizing the Ron value for p-channel metal-oxide-semiconductor (PMOS) and n-channel metal-oxide-semiconductor (NMOS) transistor is changed [20]. An asymmetry of the layout provides the different values of C_1 and C_2 capacitance values in the schematic. The FF have the asymmetry of several potential sources. Such asymmetry is reduced by cell designers in practice. Noise immunity and bit flip errors are reduced to make the FFs more vulnerable. Therefore, the transistors T_1- T_2, and T_3 -T_4 are identical in the designed layout and latches will have 50% chance to 0 or 1 power-up.

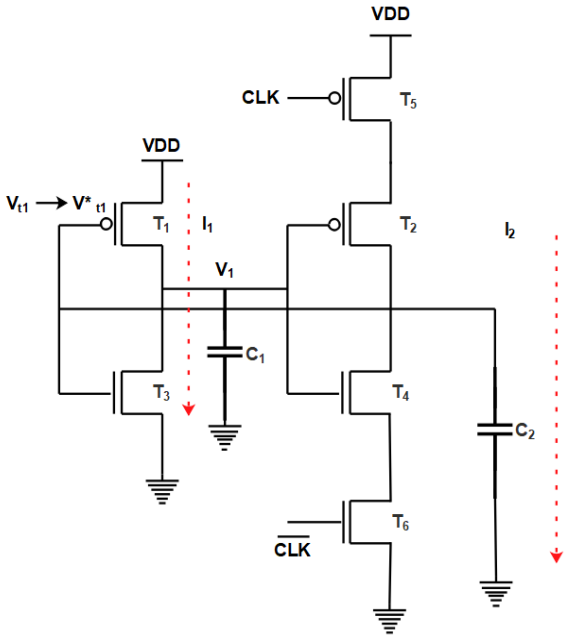


Figure 2. D latch slave schematic simplified diagram

2.1.2. Variation of process Impact and power-up states

The detailed analysis of variation in process and aging effects is presented in Figure 2. The presence resistance Ron and capacitances, C_1, C_2 of differences in node was presented in slave of DFF. The passive components and transistors process variation was further impacted. Here we assumed due to variation in process, Vp_{t1} increases to $Vp*_{t1}$. The FF becomes logical 1 when the when V_2 is greater than V_1. The voltage across C_1 is takes long time to shift to new value due to decreases in I_1 [21]. The simulation results show that metal-oxide-semiconductor (MOS) transistor threshold voltage is considered from 5% of mean value form the standard deviation gaussian distribution. But, as per the previous analysis, the transistor T_1 and T_2 threshold voltage difference must be sufficient make logical 1 [22].

Further, the effects of aging are discussed in which the T_1, T_2 , T_3 and T_4 transistor pairs have assumed to have equal threshold voltages. T_1 transistor will increase the threshold and attains $Vp*_{t1}(>Vp_{t1})$ [23], as a result of NBTI. At the same time T_2 transistor unstressed (OFF) will retain the same value of the threshold voltages. The aging effects makes the power-up to logic 1 when aging exceeds and imbalances the cell in reverse direction. From the simulation results, it can be concluded that when aging happens in logic 0, the DFFs will power up with logic 1.

From Table 1, the simulation results using the H (Hewlett)-Simulation Program with Integrated Circuit Emphasis (HSPICE) is observed. The results show aging effects for 1,000 latches. 90 days of aging considered for the experiment analysis with percentages ranges from 0 to 100%. The predictive technology model (PTM) was used with 32 nm and 20 mV for each transistor threshold voltage. The Synopsys HSPICE was used for simulation [24]. The experiment results of aging patterns with 0% and power up sates with 1%, as seen in Table 1.

Table 1. 90 days usage of start-up value of one-thousand DFFs

Percent of 0's in aging patterns	0	20	40	60	80	100
Percent of 1's in power-up state	4.6	7.6	9.8	12.8	19.8	21.9

2.1.3. Non-uniformed aging

All the flip-flops in sequential circuit will not observe same rate and aging effects post deployment from the bias [25]. The aggregate upon logic state is considered to evaluate the individual flip-flop aging. The node controllability measures are determined from the flip flops logic states. The observed probability is considered to find the probability logic state 0 or 1. The test tools like Sandia Controllability/Observability Analysis Program (SCOAP) testability are commonly incorporated for circuit simulation.

The sequential circuit schematic diagram, as observed in Figure 3. In this analysis the scan of chains is used to directly access flip flop state. Each flip flop state probability is estimated by following steps:

1) Shifted the random pattern into the scan chains (T_c=1)
2) The combinational part response is seen in FFs (T_c = 0)
3) An individual FFs states is recorded; shifted out (T_c= 1)

The above steps are done to select the different random pattern. The probability of each individual FF is determined by applying huge number of random patterns. The probability estimation is described in (1). In the similar way $R_p(0)$ is estimated using (1) by placing 0's in 1's place.

$$R_p(1) = \frac{Number\ of\ \#1s\ in\ Flip\ flop}{Number\ of\ Group\ patter} \quad (1)$$

The continuous functional operation is not accurately duplicated in a single cycle operation. But, because of the statistical behavior inaccuracies are produced in the proposed work. The input probability distribution of $R_p(1)$, as observed in Figure 4 for b_{20} benchmark circuit (ITC'99) including all FFs for demonstrate the asymmetric aging. 2 tails are important for an approximate normal distribution function. In first group, FFs which age with 1 are grouped, and in the second group FFs that will age with maximum 0 are grouped together. Group-1 FFs are belongs to the state 1 during operation. This will increase the power-up over time for the number of logic 0 s. The similar process is done for group 2 for the state 0 during its operation.

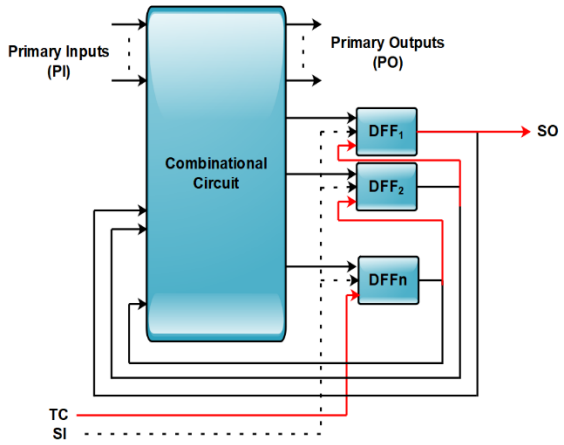


Figure 3. Sequential circuit schematic diagram

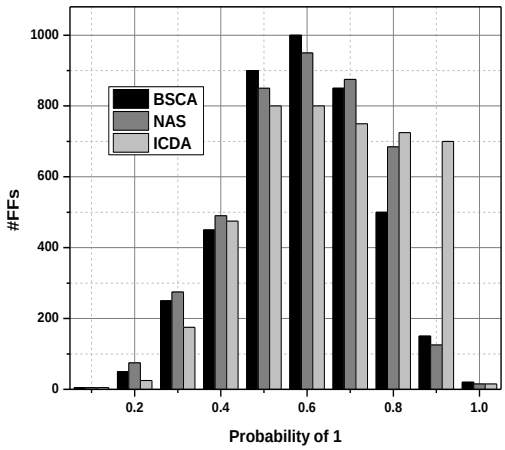


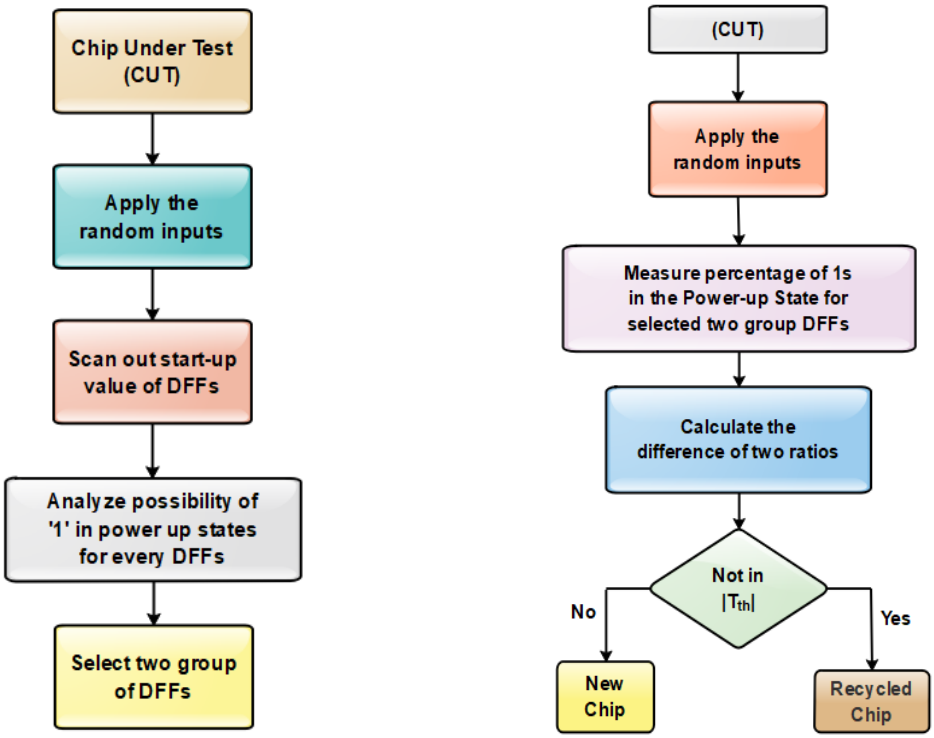
Figure 4. Groups of FFs impacted by aging

3. PROPOSED METHOD

The FFs are scanned for power up states, and are effectively used in this work for efficient detection of reused ICs. But the inherent asymmetry property makes the FF gets skewed by its power-up state. Due to this, two groups of FFs are created for 0 and 1 aging. This section presents procedure to follow to identify reused ICs. The proposed method for detection of reused IC, seen in Figure 5, which is performed in two phases. The initial characterization process was performed in phase 1, observed in Figure 5(a) for the future authentication, the FFs contains of two groups are selected. The detection of ICs or chip whether it is reused or ne is determined in phase 2 as shown in Figure 5(b) the steps followed in the 2 phases are explained:

1) Phase 1. Characterization: The main objective here is to categorize the two groups of FFs aged with 1 and 0. From the chip-under-test (CUT) the control information of FFs are extracted. Further, random input patterns are applied, and corresponding response are recorded. The response of the both the group are produced the similar results with small error which are < 1% in case of large number of FFs are used, as shown in Table 2.

2) Phase 2. Authentication: This phase identifies the reused chip is presented in this phase. This process is simple and straight forward. It is important to calculate all the FFs start-up value for CUT. During the power-up, the clock signal needs to keep logic 0 and this will select the slave latch of the DFFs. When clock signal of DFFs is forced with logic 1 then it will select master of the latch. Based on the phase 1 characterization results construct the 2 FF groups. The logic 1's (in percentage) is calculated for each group and if the difference lies within T_{th}, then chip is defined as new else reused.



(a) (b)

Figure 5. Structure of the proposed ICDA for reused IC detection (a) the characterization of phase 1 and (b) the authentication of phase 2

4. SIMULATION RESULTS AND DISCUSSION

The proposed method is verified for detection of reused ICs by performing the simulation using HSPICE aging for different benchmark circuits [26]. The MOS reliability analysis (MOSRA) was carried out for aging analysis using Synopsys tool [27], [28]. Predictive technology model was used to model the metal-oxide-semiconductor field-effect transistor (MOSFET) in 32 nm low power metal gate. At room temperature of 25 ºC the simulation for aging was carried out with 1 V supply voltage. The Synopsys design compiler (DC) has synthesized the benchmark circuits and synthesized netlist is converted into SPICE netlist using IC Validator. The logic simulation and probabilities are computed using the Synopsis verification conditions (VCs) for the each FFs.

An experiment was conducted for FFs in both groups to obtain the corresponding percentage of 1. For every MOS transistor, threshold voltage is determined by adding the standard deviation σ of 20 mV to implement the process variation. An unaged FFs 100 groups percentage was measured and corresponding distribution is plotted. Also, evaluation FFs having logic 1 for different group sizes and corresponding results of different group distribution of percentage of 1 is observed in Figure 6. The various group size with same threshold value to determination of efficiency of FF as shown in Figure 6(a) determination of threshold (T_{th}) with respect to the group size 100, Figure 6(b) determination of threshold (T_{th}) with respect to the group size 200, Figure 6(c) determination of threshold (T_{th}) with respect to the group size 500 and Figure 6(d) determination of threshold (T_{th}) with respect to the group size 1,000 and for every group power-up state for percentage of 1 is represented in X-axis and corresponding such groups are represented in Y-axis. Figure 6 shows that if there is increase in group size, the standard deviation (σ) decreases. For example, standard deviation (σ) was decreases to 0.751 from 2.663 when group sizes are increases to 1,000 DFFs. For different

standard deviation (σ) σ, 2σ, and 3σ different error rate was observed 68%, 95%, and 99.7%. Another experiment as performed to find our proposed method effectiveness in detection reused ICs using benchmark circuits ITC'99 and ISCAS'85. The selection of groups is depending on group aged with 0 and group aged with 1.

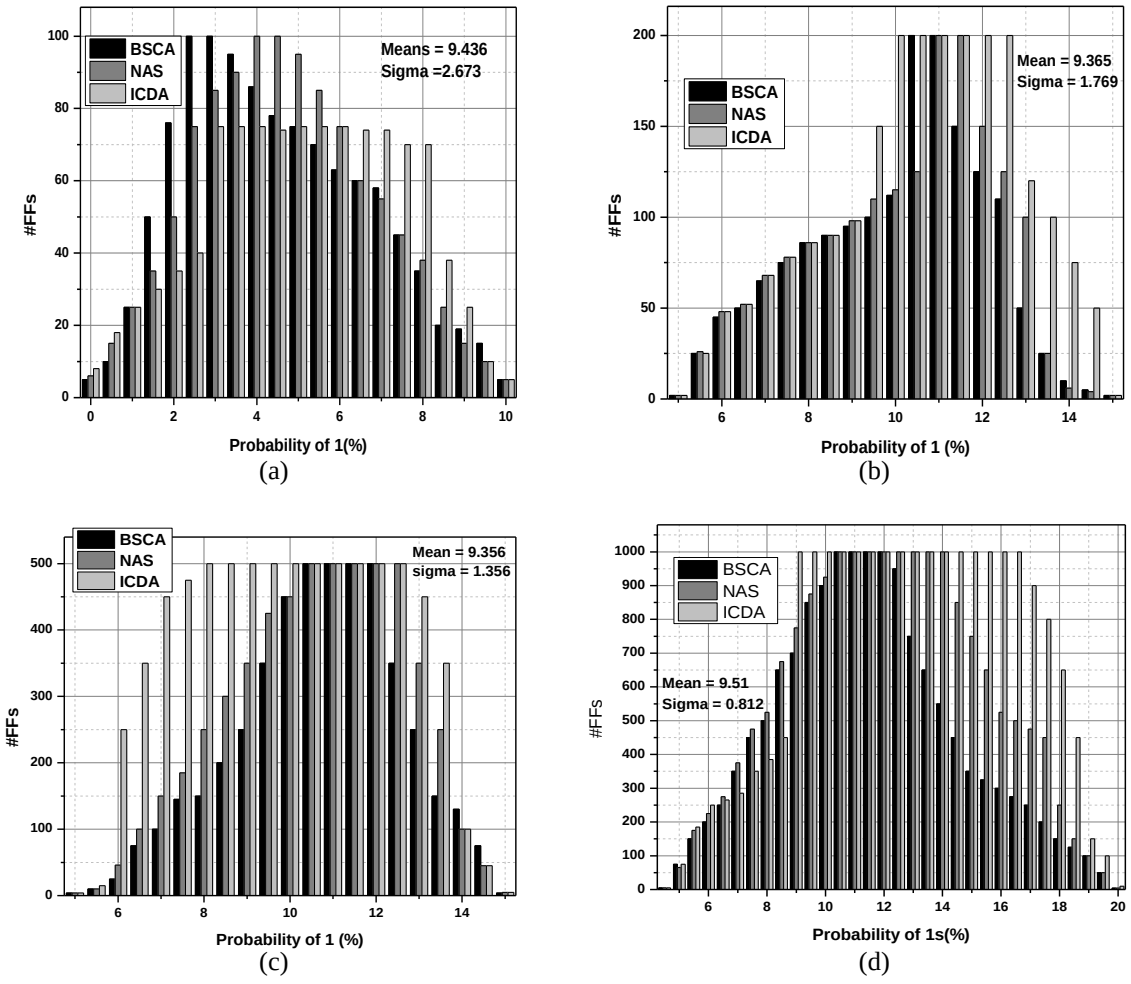


Figure 6. Estimation of threshold for different group sizes (a) hundred group size (b) two hundred group size, (c) five hundred group size, and (d) thousand group size

From Figure 7, it is observed that the inputs of every FF distribution for various circuits. Simulation analysis of DFFs with respect to the various benchmark circuits applied as shown in Figure 7(a) S_{38518}, 7(b) S_{38685}, 7(c) b_{19}, and 7(d) b_{22}. The DFF's input probability being 1 is represented by X-axis and FFs number is represented in Y-axis. For all 4 benchmark circuits the Gaussian distributions was observed. The equal aging (with 0 or 1s) was observed with 2/3 of the FFs and non-uniform aging was observed with the 1/3 of the FFs. The distribution function for different benchmark circuits is seen in Figure 7. The simulation results of the proposed method with aging intervals of three, six and twelve months are shown in Table 2. Over total FFs experience as 1/3 FFs belongs to the non-uniform aging. In the benchmark circuits b_{19} and b_{22} contains the FFs of thousands of numbers. In other type of benchmark circuits such as b_{23}, S_{38518} and S_{38685} do not have thousands FFs to form the group. Therefore only 500 FFs are formed the group. Table 2 first column represents the duration of aging. The column of 2, 3 and 4 represent the size of group and 2 threshold value, respectively. Fifth column of the table represent the group 2 (G2). The table last column represents the 1 difference of percentage for two group after aging. The reused ICs are detected from the last column value which exceeds the threshold value of 2σ. In the analysis it was observed that based on the size of the circuit our proposed solution increases. Figures 8 and 9 shows the analysis of conventional methods with proposed work in terms of life span and reliability respectively by considering the DFFs group size 1,000.

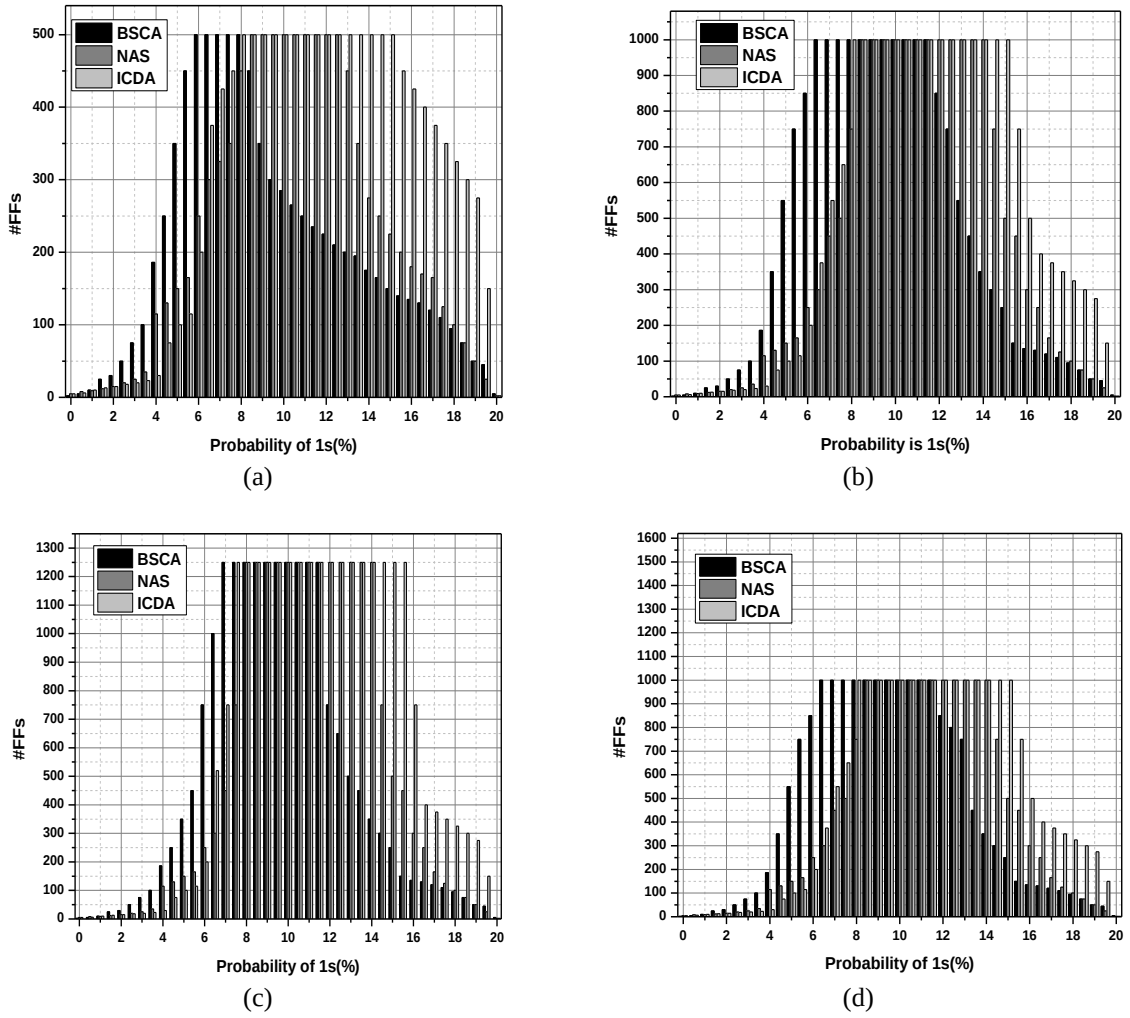


Figure 7. Probability of getting 1 ($R_p(1)$) for different benchmark circuits at input of DFFs for (a) S_{38518}, (b) S_{38685}, (c) b_{19}, and (d) b_{22}

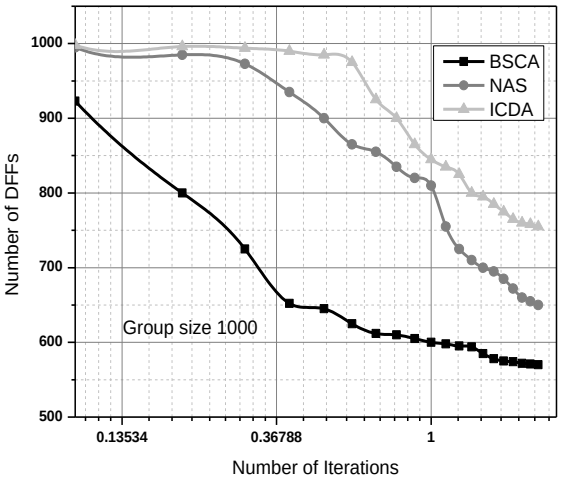


Figure 8. Performance analysis between proposed method with existing methods with respect life span to the group size 1,000

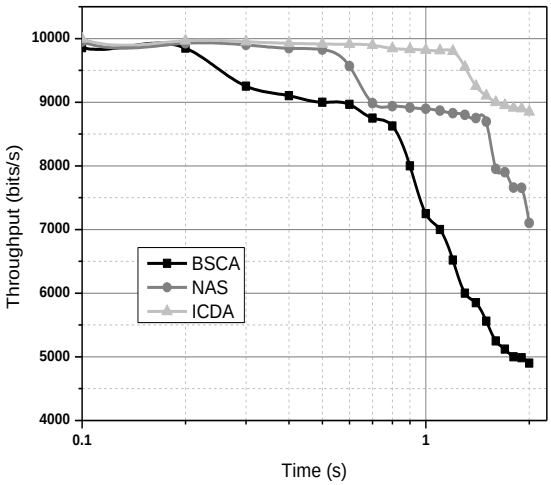


Figure 9. Analysis of conventional methods with proposed work in terms of accuracy

Table 2. Power-up value of FFs for used benchmark circuit

Usage (Months)	Bench Marks	Group Size	2σ Value	%2s For G_1	%2s For G_2	Difference
3	b_{23}	550	2.4	9.98	13.17	3.19
	b_{18}	550	2.4	6.23	12.48	6.25
	b_{19}	1050	1.6	9.16	16.32	7.16
	b_{22}	1050	1.6	8.17	15.72	7.55
	S_{38518}	550	2.4	8.23	14.72	6.49
	S_{38685}	550	2.4	10.46	18.90	8.44
6	b_{23}	550	2.4	9.52	15.98	6.46
	b_{18}	550	2.4	5.92	15.64	9.72
	b_{19}	1050	1.6	7.96	18.07	10.74
	b_{22}	1050	1.6	7.24	17.63	10.39
	S_{38518}	550	2.4	7.96	15.65	7.69
	S_{38685}	550	2.4	10.21	20.98	10.77
12	b_{23}	550	2.4	9.16	16.32	7.16
	b_{18}	550	2.4	5.23	15.75	10.52
	b_{19}	1050	1.6	8.01	18.02	10.01
	b_{22}	1050	1.6	7.32	17.01	9.69
	S_{38518}	550	2.4	7.61	16.02	8.41
	S_{38685}	550	2.4	10.18	20.14	9.96

5. CONCLUSION

The proposed work efficiently detects the unused ICs with the help of scan architecture without taking any additional references. The proposed method enhances the life span of ICs, reliability, accuracy and reduces power dissipation in SRAM memory array. with respect to the life span of 1.25% and 0.98% in comparison to conventional methods Bachelor of Science in Community Development (BSCD) and network-attached storage (NAS) respectively. The proposed work displays improved performance than existing methods with respect to reliability 0.45% and 0.98% as compared to the conventional methods BSCD and NAS. The work proposed has 1.45% and 1.86% as compared to conventional methods BSCD and NAS respectively with respect to probability-distributed 1s and 0s in various group sizes. The proposed method effectively differentiates the IC's nematic bits (NBIT) stress location and allocation of tasks where unused ICs are present. Due to equal distribution of 1s and 0s in entire SRAM memory array, it will support more parallel and switching operations. Future scope: our research is on 64-bit operation, but nowadays more operations are performed on fifth-generation communication and digital operation, hence the proposed method can enhance the scan of the unused ICs in highly integrated very large-scale integration (VLSI Chips and it is capable of operating without any overheads in 128 bits.

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BIOGRAPHIES OF AUTHORS

Rekha Sathyanarayana is currently assistant professor at Don Bosco Institute of Technology, Bangalore. She has around 11 years of teaching experience with industry interactions. He obtained his B.E. degree in electronics and communication enggineering from Visvesvaraya Technological University Belgaum in 2008, M.Tech. degree from Visvesvaraya Technological University Belgaum in 2010. She can be contacted at email: rekha.msn@gmail.com.

Nataraj Kanathur Ramaswamy is currently, Dean and Director at Don Bosco Institute of Technology, Bangalore. He has around 26 years of teaching experience with industry interactions. He has served the VTU at various levels as BOE member, paper setter, and DCS for VTU digital valuation, journal reviewer for IEEE and Springer. He received funds from different funding agencies. He Currently guiding five research scholars in Visvesvaraya Technological University Belgaum. He is a recognized research guide, Ph.D. thesis evaluator of various universities across the country. He can be contacted at email: nataraj.sjbit@gmail.com.

Mallikarjunaswamy Srikantaswamy is currently working as an associate professor in Department of Electronics and Communication Engineering at JSS Academy of Technical Education, Bangalore. He obtained his B.E. degree in telecommunication engineering from Visvesvaraya Technological University Belgaum in 2008, M.Tech. degree from Visvesvaraya Technological University Belgaum in 2010 and was awarded Ph.D. from Jain University in 2015. He has 11+ years of teaching experience. His research work has been published in more than 65 international journals and conferences. He received funds from different funding agencies. Currently guiding five research scholars in Visvesvaraya Technological University Belgaum. He can be contacted at email: mallikarjunaswamys@jssateb.ac.in.

Rekha Kanathur Ramaswamy is currently working as a professor in Department of Electronics and Communication Eng at S.J.B Institute of Technology, Bangalore. He has around 24 years of teaching experience with industry interactions. She has served the VTU at various levels as BOE member, paper setter, and journal reviewer for IEEE and Springer. She received funds from different funding agencies. He currently guiding five research scholars in Visvesvaraya Technological University Belgaum. She is a recognized research guide, Ph.D. thesis evaluator of various universities across the country and an advisory committee member for national, international conferences. She is subject expert for faculty recruitment drives at various institutes. She can be contacted at email: rekha.sjbit@gmail.com.