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Departamento de Electrónica, Sistemas e Informática

Maestría en Diseño Electrónico

REPORTE DE FORMACIÓN COMPLEMENTARIA EN ÁREA DE CONCENTRACIÓN EN DISEÑO ELECTRÓNICO DE ALTA FRECUENCIA

TRABAJO RECEPCIONAL que para obtener el **GRADO** de
MAESTRO EN DISEÑO ELECTRÓNICO

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Content

Introduction

The present reception document describes the most relevant works for the master in electronic design, where there were several interesting subjects from technical and strategical areas but getting as a most important area to me high-frequency studies.

The high-frequency studies helped me comprehend all phenomena that need to be considered when designing high-speed signals for computing servers such as DDR, PCIe, etc.

1. Summary of Realized Projects

The present work describes summarized projects oriented to High-Frequency design covering principal subjects:

- Methods of Simulation of Electronic Circuits and Modeling
- Design of Circuits Based on Optimization
- High-Frequency Electronics Design.

Projects developed in these subjects included the study of via stitching to improve signal integrity quality on high-performance PCBs, the analysis of a parallel coupled band-pass filter for WLAN, and the optimization of a single stub shunt tuning network using space mapping techniques. The knowledge and experience obtained when developing those projects now has become a strong tool, which is been applied to day-to-day work developing high-performance sever boards including Base boards and System boards which drive cutting-edge technology of data processing and transferring.

1.1. Via Stitching to Improve Signal Integrity Quality on High-Performance PCBs

1.1.1 Introduction

Via trough hole transitions are the major contributors to signal degradation in PCB interconnections. As the signal's frequency increases, degradation and reflections increase too. Several design factors can be considered to avoid these undesired effects such as developing PCB Stack-up for the best routing strategy, including ultra-low loss materials, via back drill, etc., but some of these options end up increasing the system's cost. The usage of via stitching is the most common manner to mitigate such degradation effects. However, the contemporaneous Server's PCB real state is too tight to place all desired components as well as routing channels, therefore determining the optimal placement of via stitching is primordial. This analysis aims to understand the effects of via stitching depending on their relative position to the via signal to achieve optimal performance.

1.1.2 Background

Via stitching is used to tie together reference planes on different layers of the PCB, creating a strong vertical connection through the board structure, helping maintain a low impedance and short return loops for via signal.

Simulating and understanding the via stitching effect enables designers to make the best decisions regarding the relative placement of those vias. The present work analyzes the frequency range from 5GHz to 20GHz, starting from 400 mils to 100 mils distance to the via signal.

1.1.3 Solution

Simulation of high-speed signal relies on wavelength, Table I shows the frequencies to analyze and relation with distance for via stitching setup 5GHz, 10 GHz, 15 GHz, and 20 GHz.

1.1. Via Stitching to Improve Signal Integrity Quality on High Performance PCBs

Table I

frequency (GHz)	λ (m)	λ (inches)	λ/8 (inches)
5	0.028612303	1.126466	0.140808
10	0.014306152	0.563233	0.070404
15	0.009537434	0.375489	0.046936
20	0.007153076	0.281617	0.035202

The stack-up considered for this analysis is formed by Top, GND, Power, GND, and Bottom where the thickness of each layer is:

- Top 2mils
- GND 3mils
- Power 3mils
- Bottom 2mils

The analyzed signal net had a 10 mils width, including vias of 10 mils diameter, and pads of 15 mils diameter. When the via signal is crossing the layers, it needs to avoid touching the GND and power layers, therefore they need anti-pads, which creates the areas that are not covered by the conductive material in this design they had a diameter of 20 mils. In Figure 1-1, the initial board to simulate is shown.

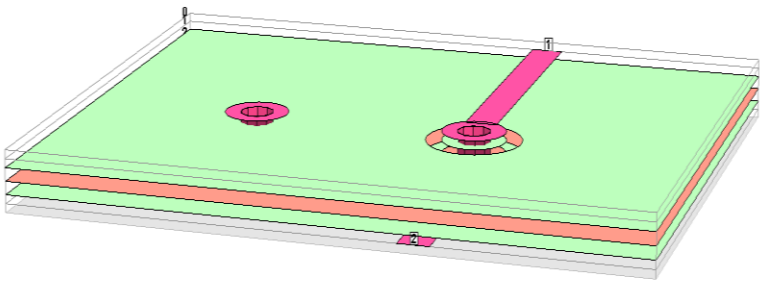


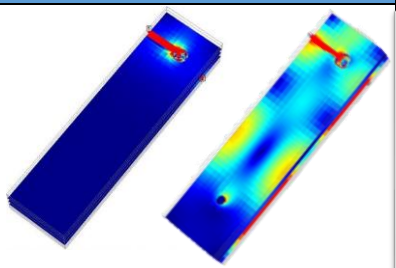
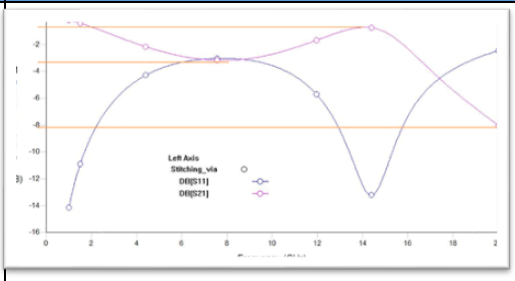
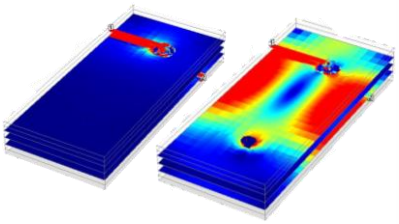
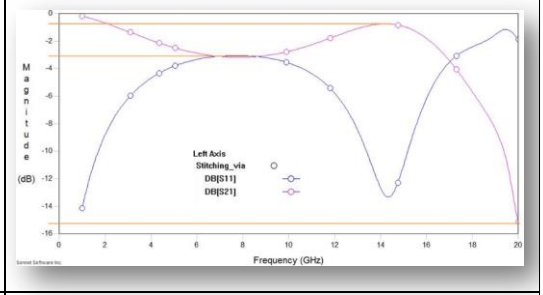
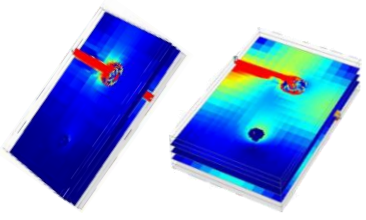
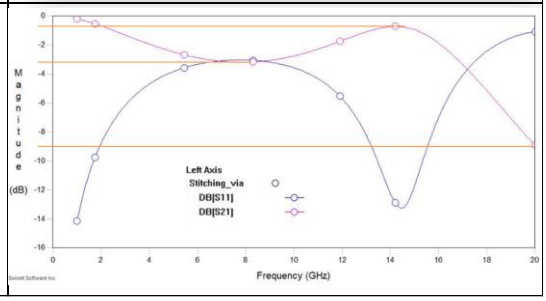
Figure 1-1: Stack-up

1.1. Via Stitching to Improve Signal Integrity Quality on High Performance PCBs

1.1.4 Results

Simulating via stitching placed at different distances away from the transition via signal, the behavior was seen for low frequencies and high frequencies, at low frequencies the transition did not present significant losses nor reflections, or they were minimal, but when the frequency increased the losses and reflections increased too. Now, considering different distance placement of via stitching away from the via signal, it was noticeable losses and reflections were minimized as they were placed nearest to the via signal as in Table II.

Table II

Distance of Stitching via to via signal	PCB Simulation	Simulation Result
400 mils	 5GHz 20GHz	
200 mils	 5GHz 20GHz	
100 mils	 5GHz 20GHz	

1.1. Via Stitching to Improve Signal Integrity Quality on High Performance PCBs

1.1.5 Conclusions

After analyzing the behavior of the via stitching considering as variables just frequency and relative placement from a via signal, they gave a good approach of the best via placement to designers, however, considering just frequency and relative placement is not enough to provide the best solution for specific cases, based on this analysis it was found more variables need to be considered as PCB stack up, specific losses of PCB material, as well as consider specific frequencies design requires.

Also, it was noticeable having the via stitching far away from the via signal did not represent an improvement, due to the weak reference it represents, so in this case designers need to avoid that configuration, because it can consume the real state of CAD design.

Therefore, for a specialized design, it is imperative to carefully analyze all variables present in the design to ensure not only correct placement or distance from the via signal but also consider a correct number of vias stitched as well as the arrangement needed, this will improve not only via signal but also the real state in PCB design. As an example of the via signal in the industry, several frequencies can be found in different High-Speed technologies such as PCIe and DDR which require similar analysis presented in this work to determine the best place of vias stitched, not only to get the better reference effect but also to control other degradation effects.

1.2. Analysis of a Parallel Coupled Band-Pass Filter For WLAN

1.2.1 Introduction

This study presents a band-pass filter operating at a center frequency of 2.4GHz with 54MHz of bandwidth. The design and simulation were based on microwave filters.

The objective of this study was to become familiar with the design methods presented in class and get a certain level of expertise in designing from the analytical perspective to the simulation.

1.2.2 Background

The Band-Pass filter in this work is a 4th-grade Parallel coupled filter which consists of 5 coupled pairs that are placed together to form the 4th-grade filter working at the central frequency of 2.4 GHz and a 240 MHz bandwidth, couple pairs of this filter were formed by Microstrip traces which geometries were calculated considering FR4 PCB material characteristics described in Table III.

Table III

N	Z_{odd}	Z_{even}	Z_0	W	L
1	39.36	70.03	52.5	1.45	17.02
2	39.9	67.98	52.08	1.5	16.98
3	40.98	64.58	51.44	1.59	16.91
4	39.9	67.98	52.08	1.5	16.98
5	39.36	70.03	52.5	1.45	17.02

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

As a result, the filter was configured by five couple pairs which were placed together to conform to the 4th-grade filters, where impedances and geometries are described in Figure 2-1.

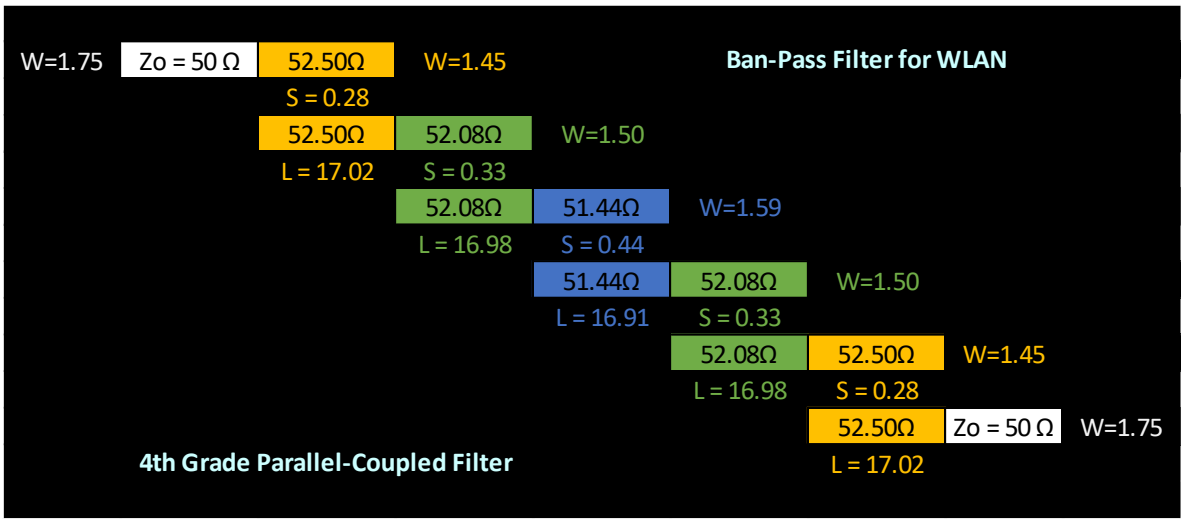


Figure 2-1: 4th Grade Parallel coupled microstrip band filter for 2.4GHz

1.2.3 Solution

Development of this filter was considered a Chebyshev filter, due under the same specifications, the number of poles in Butterworth filters was more elevated than Chebyshev filters and since the number of components required to construct one or the other could be significantly reduced, then, Chebyshev filter was considered the most cost reduced solution becoming as a cost-effective solution for a commercial product. All calculus was done to obtain delta frequency based on the parameter's "g". As a result of scripting in Scilab concentrated topology $\boldsymbol{Z_{odd}}$ and $\boldsymbol{Z_{even}}$ were defined as described in Figure 2-2.

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

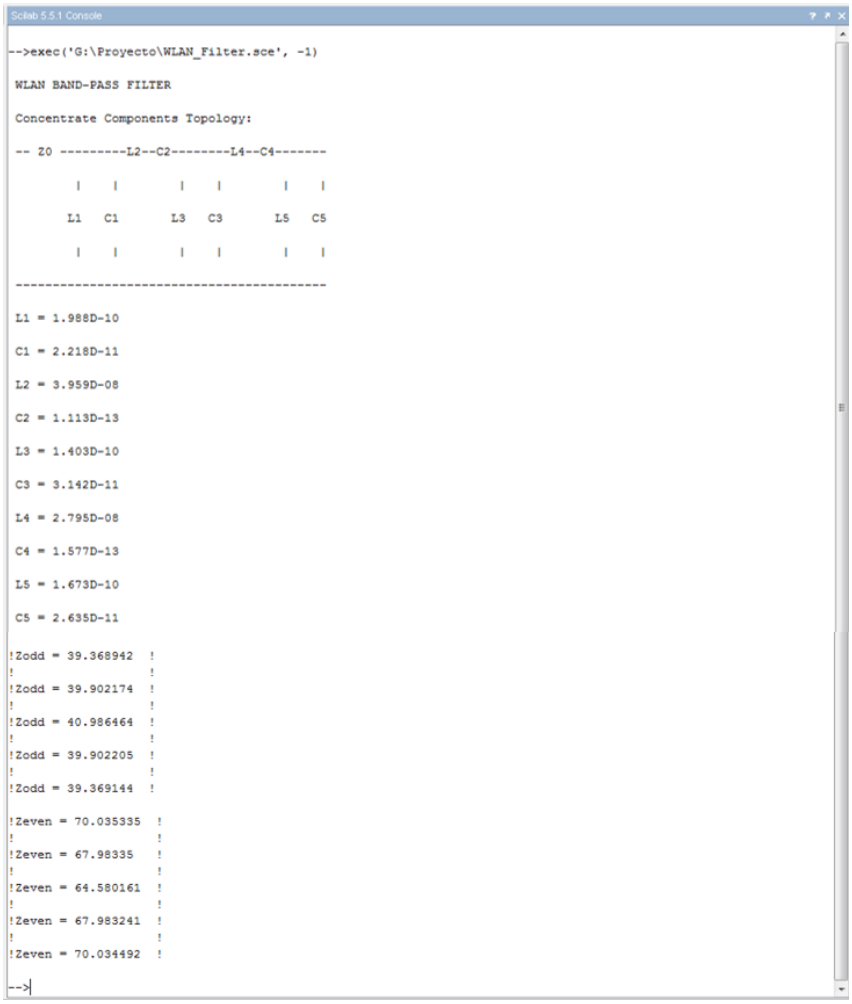


Figure 2-2: Scilab script for concentrated topology.

With values defined by Scilab, a synthesis calculator was used to define the PCB geometries for Microstrip (W (Width), L (Length), and S (Spacing)) as described in Table III. These geometries allowed to simulated Filter in APLAC (Figure 2-3) using lossy traces, which had a degraded performance compared to the simulation in Sonnet (Figure 2-4) for distributed components.

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

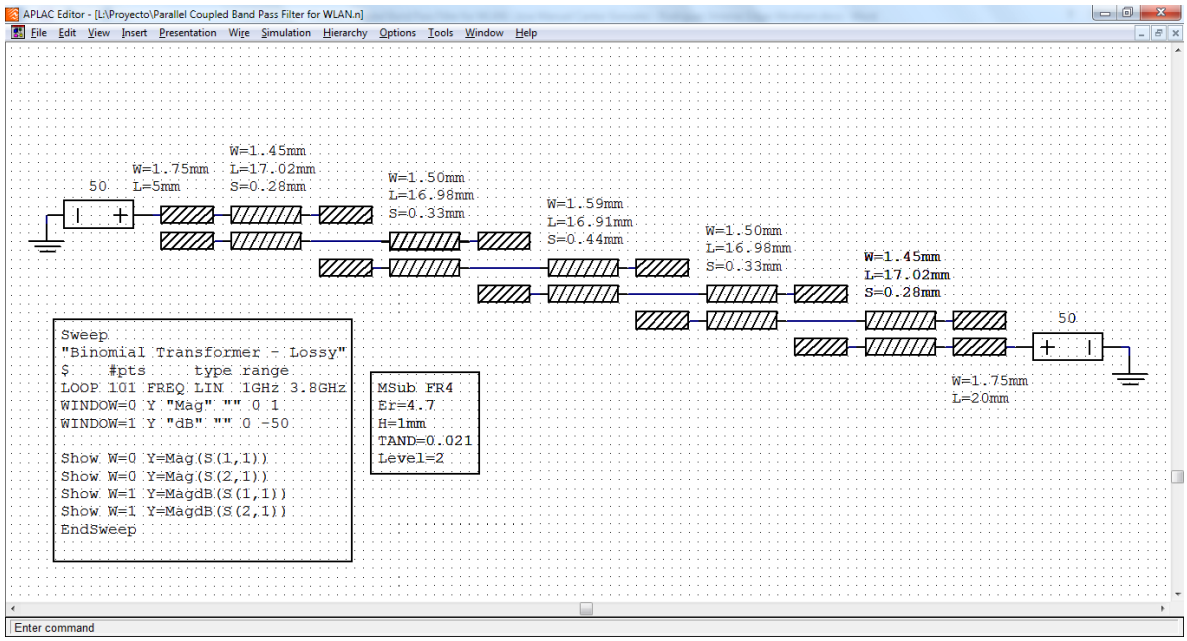


Figure 2-3: 4th Grade Parallel coupled microstrip bandpass filter designed for 2.4GHz with lossy traces.

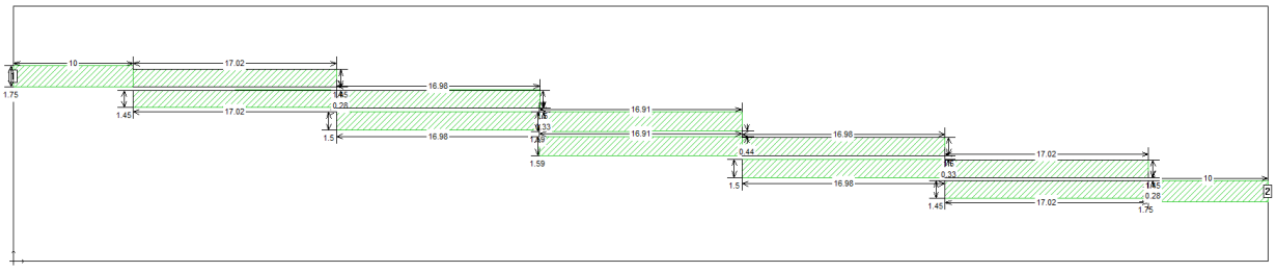


Figure 2-4: 4th Grade Parallel coupled microstrip bandpass filter designed for 2.4GHz with distributed components.

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

1.2.4 Results

From Simulations with APLAC and Sonnet, the filter was correctly tuned when considered as a Lumped or Distributed filter, Additionally, the results show how lossy attributes impacted the filter's performance.

The lumped components simulation response is shown in figure 2-5, where $\boldsymbol{S_{11}}$ shows the filter was correctly tuned to 2.4GHz, and $\boldsymbol{S_{12}}$ displays maximum transmission this circuit allowed around 2.4GHz.

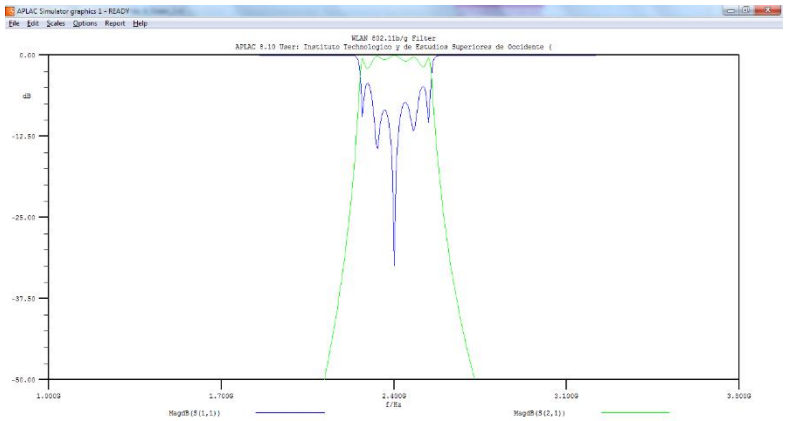


Figure 2-5: APLAC Lumped components response.

The distributed components simulation response is shown in figure 2-6 using APLAC using lossy traces, where $\boldsymbol{S_{11}}$ shows that the filter was correctly tuned to 2.4GHz and $\boldsymbol{S_{21}}$ displays the maximum transmission circuit allowed around 2.4GHz

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

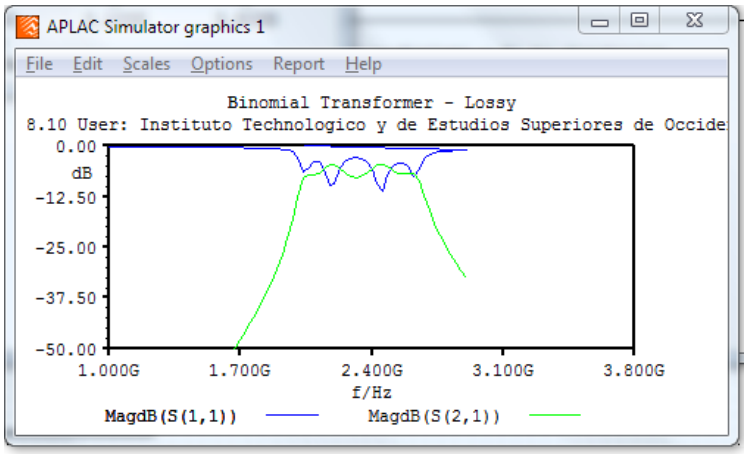
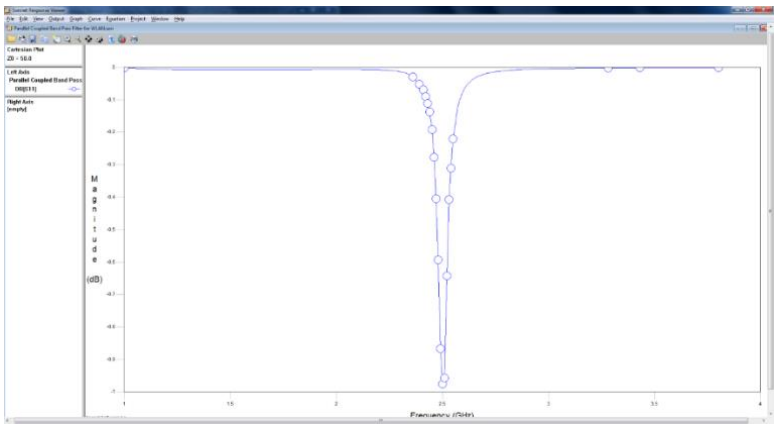


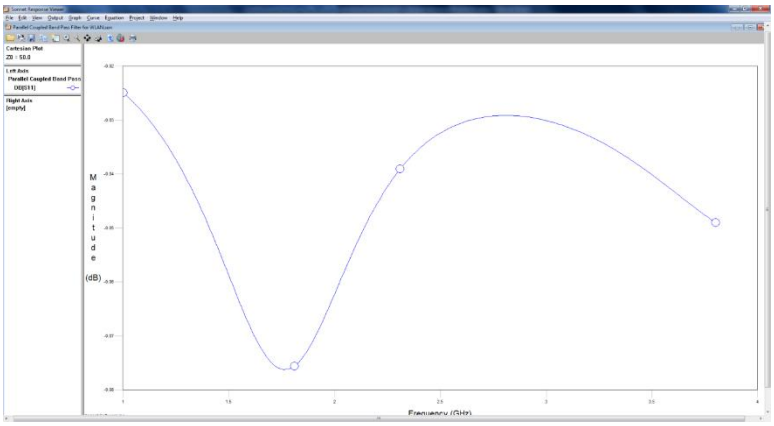
Figure 2-6: APLAC Distributed components response.

The distributed component simulation response is shown in figure 2-7 using SONNET using lossless and lossy traces, where $\boldsymbol{S_{11}}$ shows that the filter was correctly tuned to 2.4GHz for lossless but the central frequency was drastically out of phase for lossy response due to losses added to the circuit.



A) Lossless Response

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping



B) Lossy Response

Figure 2-7: Sonnet Distributed components response.

1.2.5 Conclusions

After analyzing the behavior band pass filter considering two different simulators as well as two different methods, it was found lumped or concentrated method trend to be more exact compared to the distributed component's method, due to several variables, including central frequency and filter grade, which are considered essential factors of the design.

Other important factors or variables to be considered by the designer are the type of PCB material being used as well as the real state available in design due to a distributed filter relying on the real state in PCB.

The designer must consider simulation as a tool to achieve a good solution but, he must also consider the best method and simulation tool for design.

As per my experience in the industry, simulation provides the best solution approach as long as most environmental variables are included, including most of them, speed up design cycles as well as provide high quality to all designs to deliver. However, since not all real-world variables can be included in a simulation, the circuit needs to be validated considering all ecosystem

1.2. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

variables, based on this any of the values in the design can be tuned according to the real-world variables.

1.3. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

1.3.1 Introduction

This work shows the optimization of a single stub shunt tuning network on a transmission line using space mapping (Figure 3-1). This is a simple synthetic problem planned to illustrate the benefits of using a space-mapping approach over other techniques like parameter extraction.

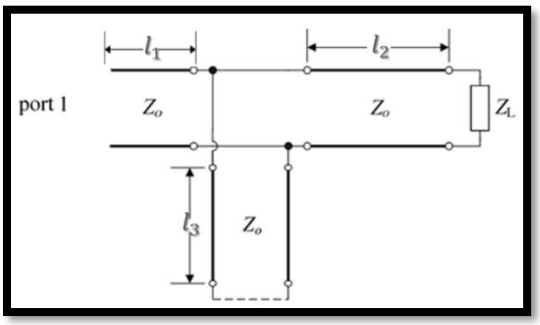


Figure 3-1: Single stub shunt tuning network topology

1.3.2 Background

The transmission line described in Figure 3-1 needed to be matched to 4GHz with a Z_L that consists of 0.8 pf in parallel with 73 ohms, considering a characteristic impedance of 50 ohms and material characteristics H = 0.25 mm, ε_R = 4.12 and tan δ_d = 0.01.

This analysis considered the coarse and the fine models, where the coarse model (Figure 3-2) is considered a lossless transmission line and starts from an optimized point, which meets the design requirements (3-1). Whereas the fine model considered losses of microstrip material (Figure 3-3).

$$x_c = [100mm\ 0.99mm\ 13.11mm] \tag{3-1}$$

1.3. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

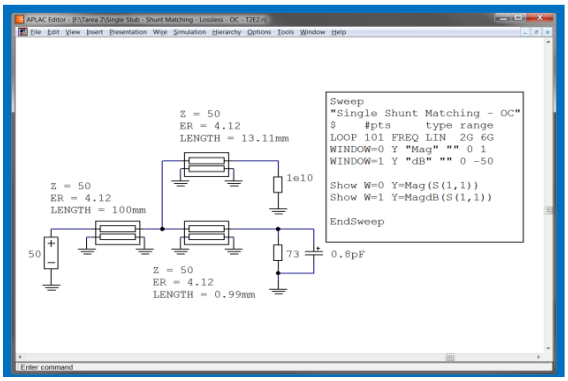


Figure 3-2: Coarse model

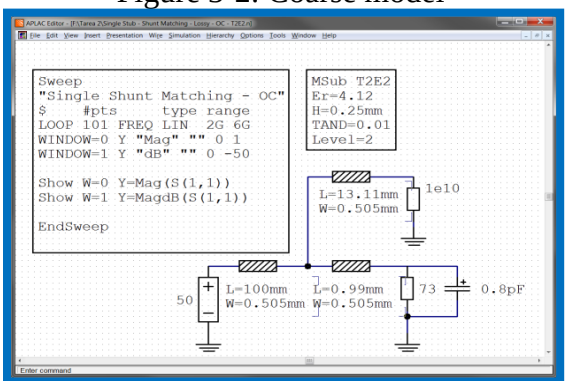


Figure 3-3: Fine model

1.3.3 Solution

Response using the coarse and the fine model is shown in Figure 3-4, the coarse model provided the exact response required at 4GHz (x_c* blue line), whereas the fine model representation deviated from the expected response (x_f red line). The objective of optimizing the fine model with Space mapping was to get an x_f* whose response complies with the 4GHz on spec.

1.3. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

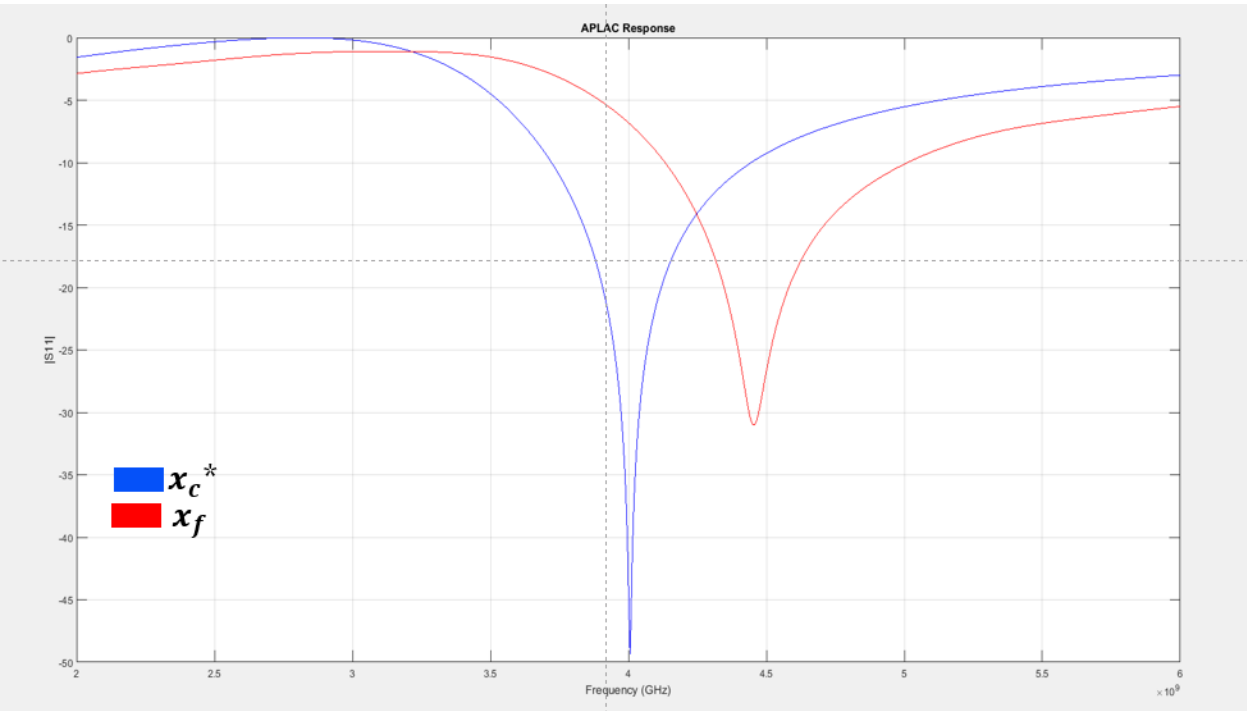


Figure 3-4: Initial design response for coarse and fine models.

Since the base requirement to use space mapping optimization was to have fine and coarse models, once those models were available, the next step was to get x_c to develop Space mapping. The process to calculate x_c* is described as follows:

Calculate the inductive reactance for the capacitor on the load:

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi * 4x10^9 * 0.8x10^{-12}} \approx 49.735\ \Omega \tag{3-2}$$

Then calculate the parallel of the resistor and the capacitor:

$$Z_L = \frac{R_L * (-X_C)}{R_L + (-X_C)} = \frac{73 * (-49.735)}{73 + (-49.735)} \approx 23.143 - 33.968j \tag{3-3}$$

The Smith chart will be used to find a suitable solution, to use the Smith chart, Z_L should be normalized.

Normalizing Z_L:

$$z_L = \frac{Z_L}{Z_o} = \frac{23.143 - 33.968j}{50} \approx 0.46 - 0.68j \tag{3-4}$$

1.3. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

From the Smith chart two points are extracted from the SWR circle that intersects the 1+jb perimeter:

$$y_1 = 1 + 1.25j \tag{3-5}$$

$$y_2 = 1 - 1.25j \tag{3-6}$$

Then, the distance is obtained from the normalized load admittance to both points toward the generator:

$$d_1(to\ y1) = 0.170 - 0.143 = 0.027\ \lambda\ (\mathrm{d_{min}}) \tag{3-7}$$

$$d_2(to\ y2) = 0.330 - 0.143 = 0.187\ \lambda \tag{3-8}$$

$$\ell_{oc} = 0.358\lambda \tag{3-9}$$

To simulate in APLAC the results, it is necessary to transform to millimeters $d_{min},\ \ell_{OC}$:

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3x10^8}{\sqrt{4.12}} \approx 147.8x10^6 \tag{3-10}$$

$$\lambda = \frac{v_p}{f} = \frac{147.8x10^6}{4x10^9} \approx 0.0369m\ \approx 36.9\ mm \tag{3-11}$$

$$d_{min} = 0.027 * \lambda \approx 0.99\ \text{mm} \tag{3-12}$$

$$\ell_{OC} = 0.358 * \lambda = 13.11\ \text{mm} \tag{3-13}$$

1.3.4 Results

After running the **"Broyden-based input space mapping algorithm"** by 22 iterations, the results are shown in (3-5) x_f* (green line), it was evident using optimized values of x_f* (3-14) behaved similarly as x_c* as expected.

$$x_f * = \ [1mm\ 1mm\ 15.0072mm] \tag{3-14}$$

1.3. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

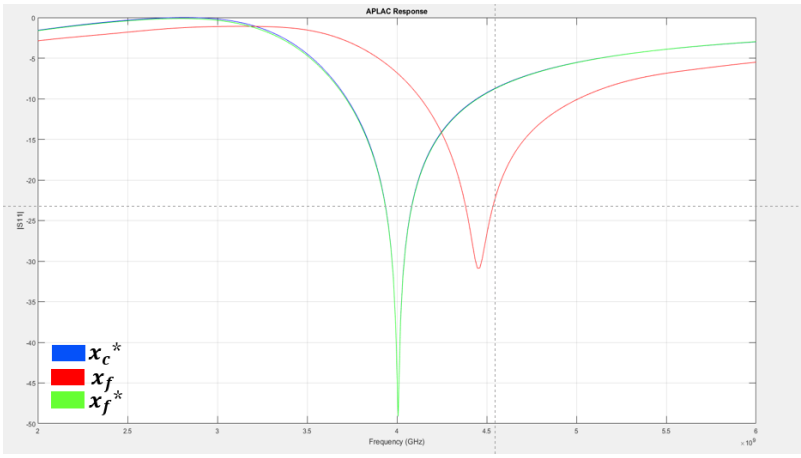


Figure 3-5: Optimized response

1.3.5 Conclusions

After analysis, it was clear some evaluations of the fine model are enough to meet the expected response, avoiding the usage of excessive computing power and time due to commonly heavy simulations that may take days to converge to a valid solution. Almost all the simulations in APLAC were done with the coarse model, which required less time and less computing power than using the fine model.

It was seen during optimization, that the response behavior oscillated and took a lot of iterations, this could be for 2 reasons:

- The length for the input of the shunt tuning network was added as an optimization variable.
- Because normally shunt networks have 2 optimized solutions, but in the end the algorithm converged to 1 of them.

Current optimization analysis of a single stub shunt tuning network applying ASM can be used also in other disciplines such as signal integrity, power distribution, structural design, etc.

2. Conclusions

Since my childhood curiosity to discover everything about electronics has been evident, getting me closer to this science area. It was not a surprise my first studies in electronics started in secondary school driving me to get formal Engineering studies, however the eagerness inside of me to get more knowledge allowed me to start my Master Engineering studies, but by then with a new meaning to me, not only because I like this science's area but also because I wanted to get a bigger purpose in my life to contribute on cutting-edge technologies and provide innovative solutions in the industry but at the same time contributing to the society.

Nowadays, as technology gets complex challenges become more and more complex, so more knowledge is required to provide all the technology solutions modern times require.

There is no doubt the three works presented in this document are the primordial base of my professional development in the industry designing cutting-edge technology server solutions, not only considering analytical design but also considering all business acumen that arises around this segment of the industry at the same time help the ecosystem to find solution environmentally friendly.

Appendix

The appendix includes original final works developed in collaboration between Jose Manuel Cantor Gonzalez and Edgar Abraham Rodriguez Jimenez for the specialization path "**High-Frequency Electronics Design**"

Edgar's grade report can be found at: REPORTE DE FORMACIÓN COMPLEMENTARIA

A. Via Stitching to Improve Signal Integrity Quality on High-Performance PCBs

Simulation Methods for Electronic Circuits
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Abstract

Nowadays the operation frequency of modern systems is increasing exponentially. Therefore, the need for techniques to improve performance plays a key role in reaching desirable operational frequencies. For instance, via-hole transitions are the major contributors to signal degradation in PCB interconnections, due to energy radiation caused by layer transitions. Via Stitching is the most common manner to mitigate such effects. However, the placement of the vias concerning the routing is not quite clearly defined. The objective of this work is to understand how the position (distance) and number of vias stitched to improve signal integrity, allowing to achieve of optimal performance.

Introduction

Vias stitched are recommended to keep the current return path for signals to avoid the reflection caused by the impedance change (or discontinuity) at vias. Considering that these extra vias take up precious space on board, designers often need to know when vias stitched are necessary, and when a design still works without using via stitching.

Simulating and understanding the via stitching effect helps make such decisions. Figure 5 shows the results of via configurations with and without via stitching, and the distance changes from the via signal. Designers can learn in this case that via stitching needs to be placed closer to the via signal; if the budget allows a 0.5dB loss from the via discontinuity, they do not need to use via stitching there.

Some people decide to be on the conservative side and put at least 2 vias stitched around every differential via signal pair that carries signals with data rates over 1Gbps; some do not follow such guidelines at all and include no vias stitched for any multi-Gbps signals. Regarding the locations of via stitching, some designers place vias stitched wherever there is room for them after routing most of the Signals in design; while some pay attention to make sure vias stitched are placed in the vicinity of designated via signals.

With all these different design practices, some boards are overdesigned which results in higher product costs; or some boards have failed SERDES signals.

To avoid design problems and maintain a cost budget, designers need to understand the effects of via stitching. The knowledge and design rules can be obtained by performing 3D analysis combining via signals with via stitching.

In general, vias stitched need to be placed close to the via signal: vias stitched placed far away from the via signal waste board space and will not help provide a continuous return path. In addition, not all SERDES signals need to have via stitching; in many cases, using 2 via stitched for one differential via signal pair is enough.

Theory

In state-of-the-art design circuits, the need for a stack-up with several layers is common, those stack-ups need to have GND reference layers for the high-speed signals. For instance, a good example is a signal routed on Top (Microstrip), the best stack-up configuration for this signal is to have a GND reference plane below it (best known as near reference). But on dense routing this configuration is not always possible, in general, there are signal layers which does not allow a good performance of the high-speed signal because they are not correctly referenced, to avoid those issues the reference planes on the different layer are tied with Vias stitched which are used to tie together larger copper areas on different layers, creating a strong vertical connection

through the board structure, helping maintain a low impedance and short return loops. Figure 1 shows a stack-up example, on red is simulated a high-speed signal route on the Top layer (Microstrip) which has its reference plane (GND) on layer 2, but it needs to change to the Bottom layer (Microstrip) through normal via, to have a good reference both reference layers must be tied together with a via stitching to avoid signal degradation and reflections.

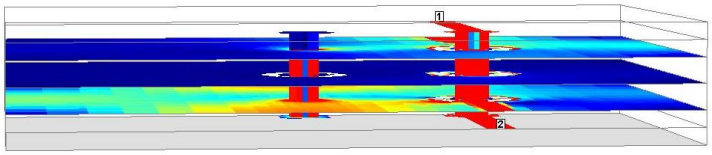


Figure 1

The simulation of high-speed signals is important to know:

- When the via stitching is necessary and when it is not.
- Effect of the distance between via stitching and via signal

A general Rule to arrange via stitching is 1/8 of a wavelength or less your ground to have a plane like solid ground.

$$\lambda = \frac{300}{(F)\sqrt{\varepsilon_R}}$$

λ = wavelength (inches)
F = frequency (MHz)
ε_R = relative permeability (4.4 typical for FR-4)

Table 1 shows the relation between distance and frequency of via stitching setup.

Table 1

frequency (GHz)	λ (m)	λ (inches)	λ/8 (inches)
5	0.028612303	1.126466	0.140808
10	0.014306152	0.563233	0.070404
15	0.009537434	0.375489	0.046936
20	0.007153076	0.281617	0.035202

The stack-up is formed by a different number of layers which are composed of cooper layers split by dielectric materials; the most common dielectric material is FR-4 and cooper as conductor.

The stack-up used was formed by Top, GND, Power, GND, and Bottom, Figure 2

The thicknesses of the layers are:

- Top 2mils
- GND 3mils
- Power 3mils
- Bottom 2mils

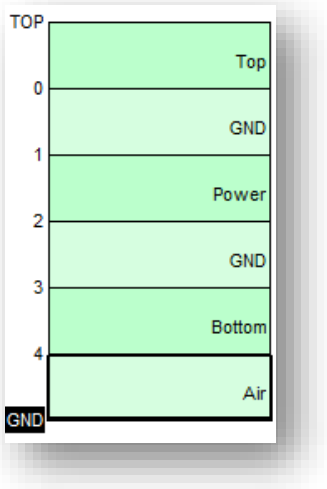


Figure 2

The net for this simulation has 10 mils of width, the vias are 10 mils diameter, and the pads are 15 mils diameter. When the via signal crosses the layers, it needs to avoid touching the GND and power layers, they need anti-pads, which are the areas that are not covered by conductor material in our design whose diameter is 20 mils. In Figure 3 the initial board to simulate is shown.

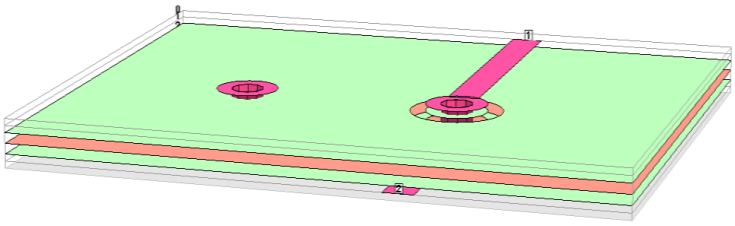
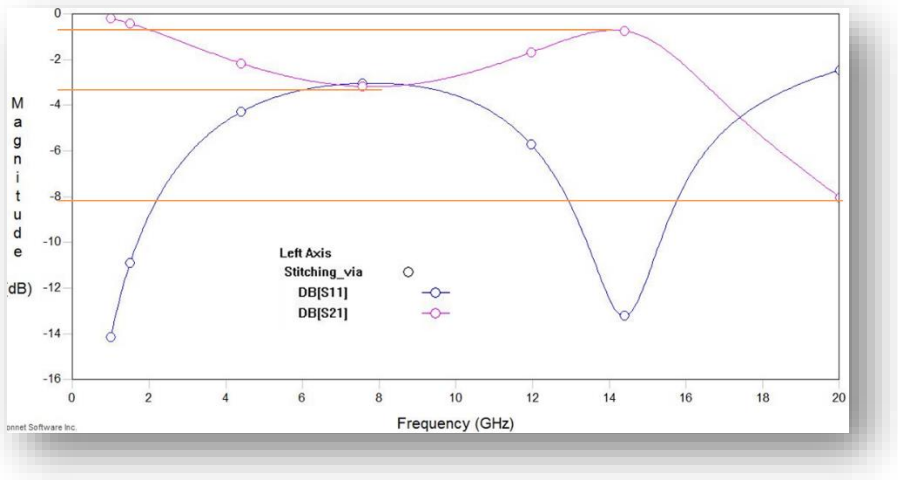


Figure 3

Effects in Generic stack-up with stitching at 400 mils

After simulating the mentioned stack-up with a high-speed signal, the results are that in the low frequencies, the transition presents very low losses and reflections but as the frequency increases the losses and reflections begin to increase, graphic 1 shows the behavior of via stitching 400 mils far away from the via signal.



Graphic 1

Figure 4 shows the current behavior at 5GHz, it is visible that losses are very low.

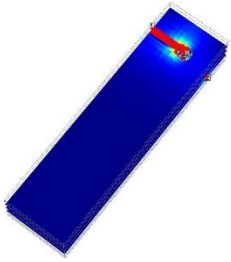


Figure 4

Figure 5 shows the current behavior at 20GHz, it is visible the losses on the reference planes, and how the via stitching sinks a small amount of current and avoids the current going beyond as crosstalk avoiding interference as an induction to other net signals.

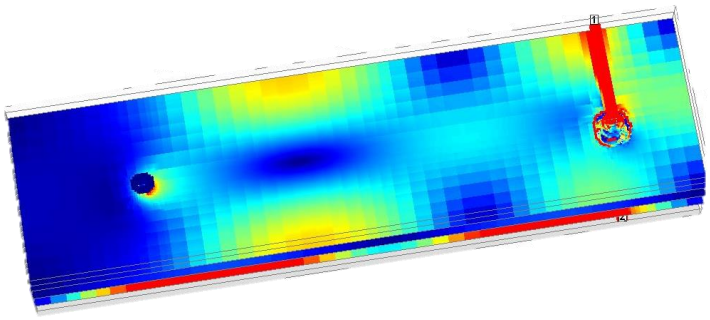
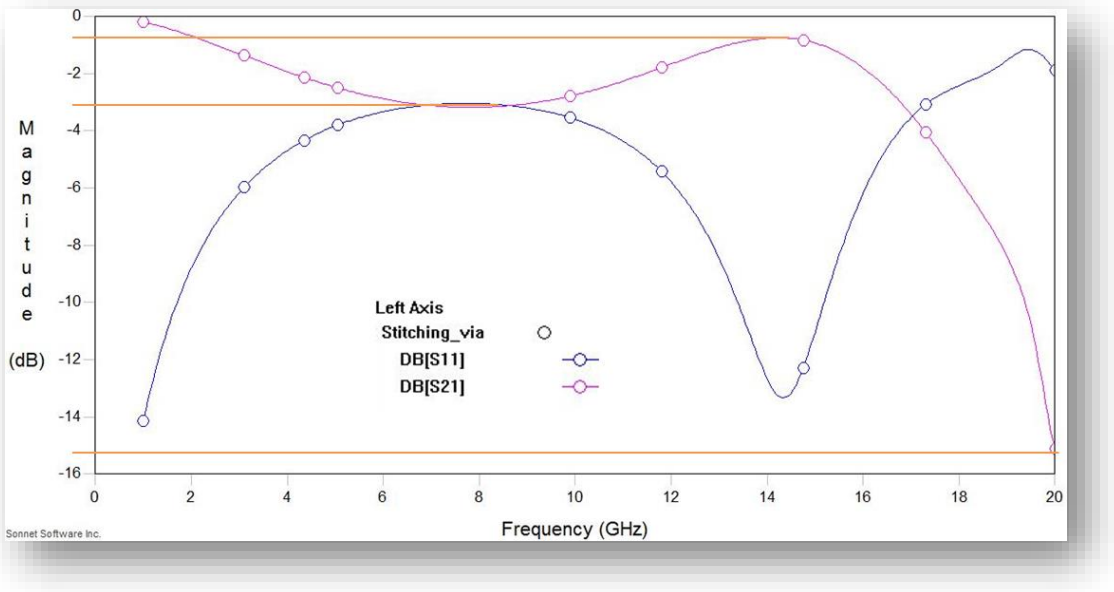


Figure 5

Effects in Generic stack-up with stitching at 200 mils

After simulating the mentioned stack-up with a high-speed signal, the results are that in the low frequencies, the transition presents very low losses and reflections but as the frequency increases the losses and reflections begin to increase too, graphic 2 shows the behavior of via stitching 200 mils far away from the via signal.



Graphic 2

Figure 6 shows the current behavior at 5GHz, it is visible that losses and reflections are very low.

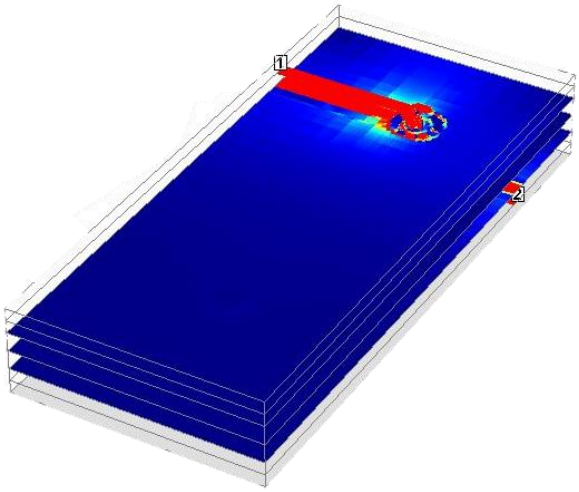


Figure 6

Figure 7 shows the current behavior at 20GHz, it is visible the losses and reflections on the reference planes, and how the via stitching sinks more current compared to the previous distance and avoids the greater amount of current going beyond as crosstalk avoiding interference as induction to other net signals.

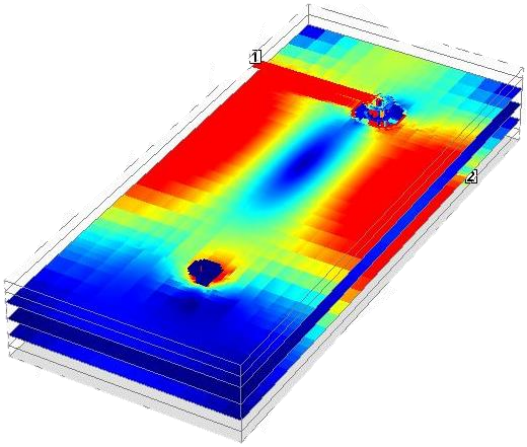
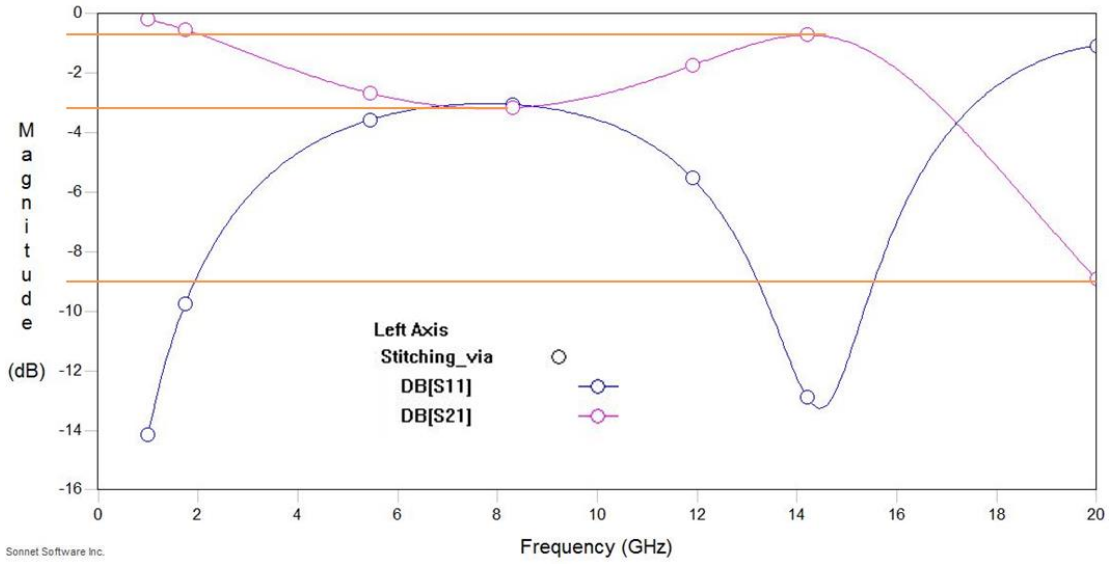


Figure 7

Effects in Generic stack-up with stitching at 100 mils

After simulating the mentioned stack-up with a high-speed signal, the results are that the low frequencies the transition presents very low losses and reflections but as the frequency increases the losses and reflections begin to increase too, the graphic 3 shows the behavior of via stitching 100 mils far away from the via signal.



Graphic 3

Figure 8 shows the current behavior at 5GHz, it is visible that losses and reflections are very low.

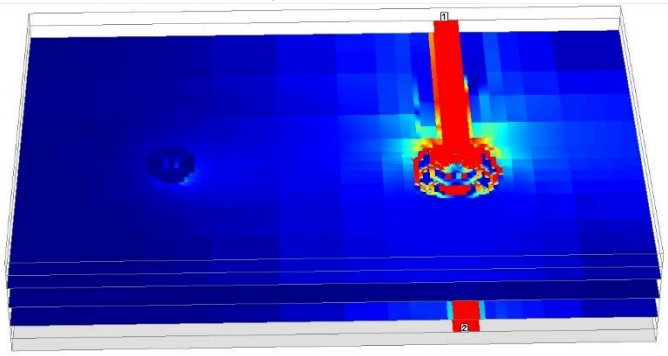


Figure 8

Figure 9 shows the current behavior at 20GHz, it is visible the losses and reflections on the reference planes, and how the via stitching sinks more current compared to the previous distance and avoids more amount of current going beyond as crosstalk avoiding interference as induction to other net signals.

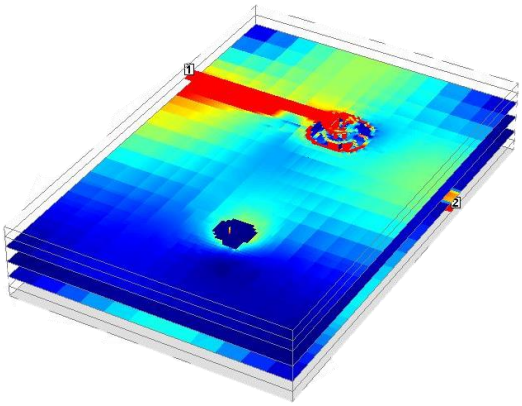


Figure 9

Conclusions

- The most common and most effective distance that can be taken as a thumb rule is to add grounding vias as a starting point at $\lambda/8$ or less, where the transition ground plane will look like solid ground. However best recommendation is to analyze each case because to industry drives different HSIOs (High-Speed Input/Output signals) that require individual analysis to get optimal tradeoff between SI performance and real estate in PCB design, those HSIOs can be DDR, PCIE, UPI, CLKs Etc.
- Via stitching placement should be avoided to be placed far away from the via signal because it will be a waste board space and will not help provide a continuous return path.

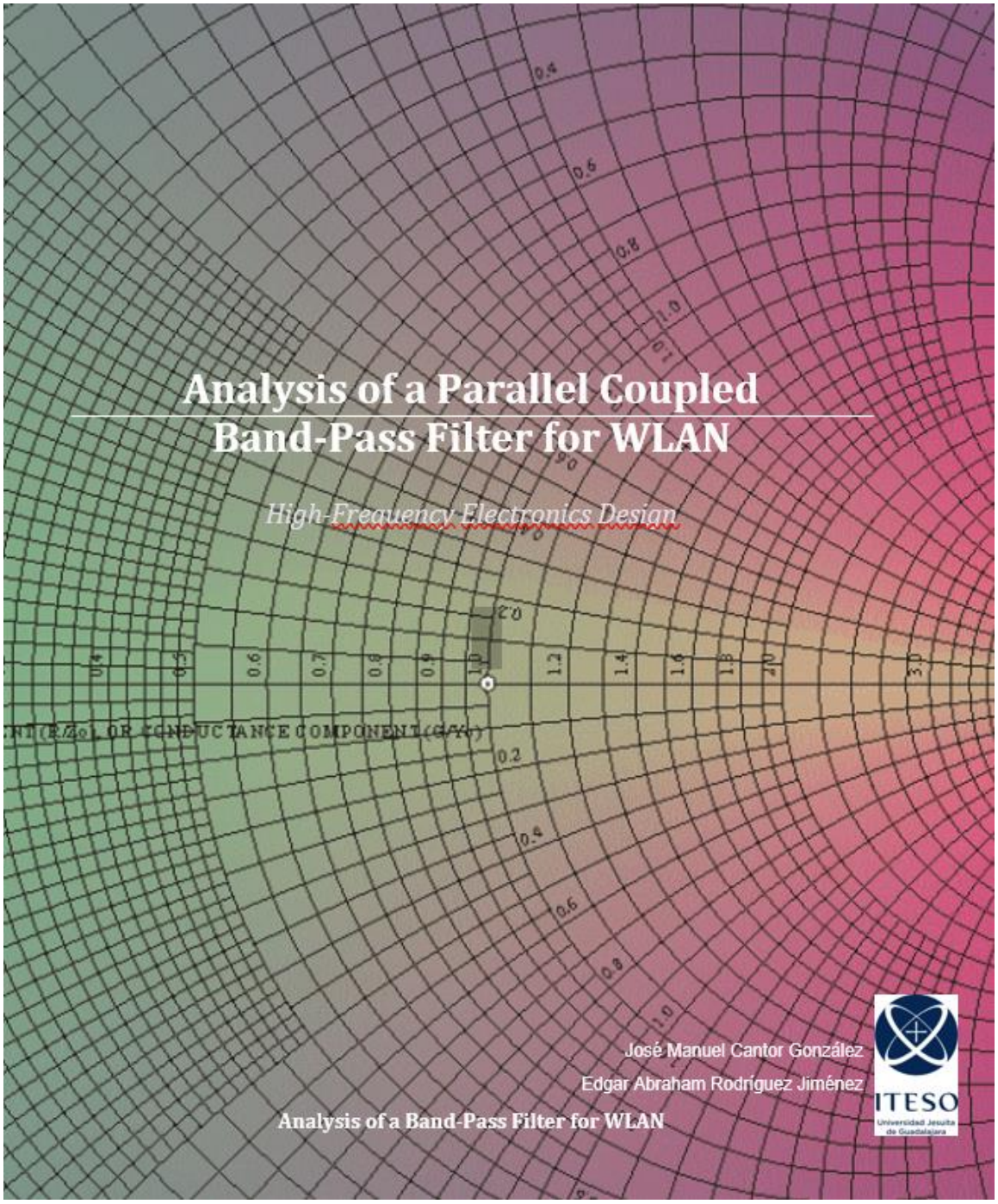
References:

UNDERSTANDING VIA EFFECTS
DR. ZHEN MU, MENTOR GRAPHICS

- Sonnet Software, Inc. " APLAC RF Design Tool". Reference Vol. III. Passive RF Components. Version 8.10.

  APLAC Solutions Corporation. Notas de la clase "Simulation Methods for Electronic Circuits (graduate course)". High-frequency circuit simulation, Full-wave EM simulation.

B. Analysis of a Parallel Coupled Band-Pass Filter For WLAN


Analysis of a Parallel Coupled
Band-Pass Filter for WLAN
High-Frequency Electronics Design
José Manuel Cantor González
Edgar Abraham Rodríguez Jiménez
Analysis of a Band-Pass Filter for WLAN
ITESO
Universidad Jesuita de Guadalajara

Introduction

Nowadays the operation frequency of modern systems is increasing exponentially. Therefore, the technologies used in the day-to-day require more complex systems which they turn challenge the design techniques to create in series manufacturable systems, balancing their performance and cost. One of the most exploited wireless technologies is the WLAN (Wireless Local Area Network), connecting to the internet, millions of people around the world every day. Computers, tablets, smartphones, televisions, and even refrigerators are connected to the net providing a modern lifestyle. Key parts of these complex systems are the filters designed to either transmit or receive data through the endpoints, particularly to the known operation frequency of 2.4 GHz that covers the popular standard 802.11.

This study presents a band-pass filter operating at a center frequency of 2.4GHz with 54MHz of bandwidth. It will be designed and simulated only. Since the micro-strip filters are considered one of the important components of a Local Area Network, many different designs can be found in both academic studies and the industry, however, our objective is to get familiar with the design methods presented in class and get a certain level of expertise designing from the analytical perspective to the simulation (unfortunately there is no chance to fabricate the design and correlate data). Optimization processes are out of the scope of the work.

Theoretical Analysis

From the basic design parameters mentioned previously, we can list the following:

- Filter Type = Band-Pass
- f_c = 2.4 GHz
- BW = 240 MHz
- f_1 = 2.28 GHz
- f_2 = 2.52 GHz
- 0.5 dB Ripple
- FR4
- ε_R=4.7
- Loss Tangent=0.021
- H=1mm
- T=0.01mm

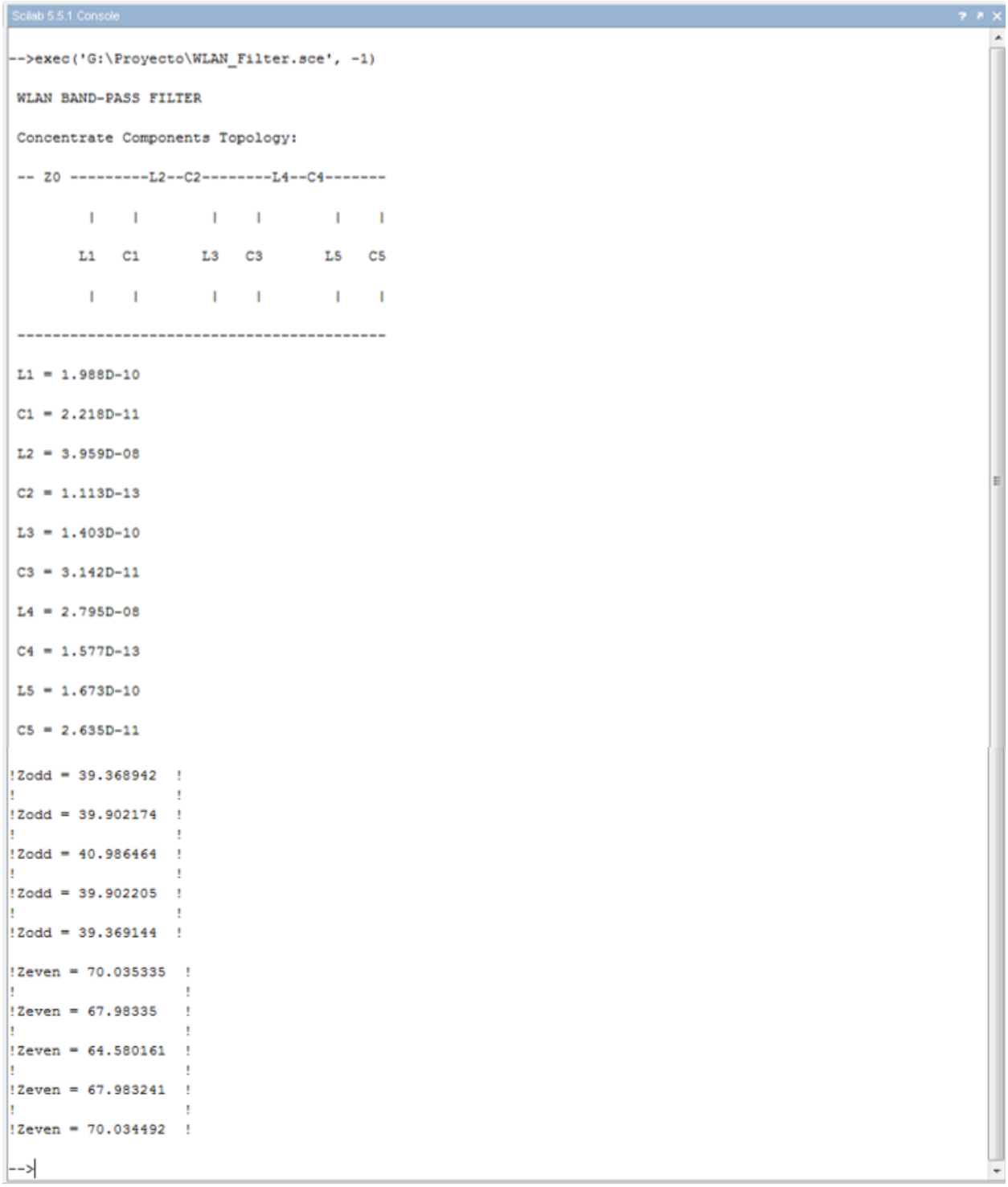
It is known that under the same specifications, the number of poles in Butterworth filters is more elevated than in Chebyshev filters, this means that the order of the filters is more elevated. This fact led us to select the Chebyshev type for practical implementation reasons since the number

of components required to construct one or the other will be reduced significantly. Therefore, the Filter design will start with the calculations by obtaining the frequency delta, and based on the "g" parameters, which are obtained from the plotting of the normalized frequency versus attenuation we can calculate the value of the concentrated parts. To do all calculations, we will use the following Scilab script that helps with all the processing. Note that the targeted outcome is a 4th-grade filter.

```
// ************************************************************************//
// Parallel Coupled Filter for WLAN - High-Frequency Electronic Design     //
// Ing. José Manuel Cantor González                                        //
//                                                          December 2014  //
// ************************************************************************//

// Defining Project Requirements:

fc =2.4e9;   // Central Frequency
f1 =fc-120e6; // Low Frequency
f2 =fc+120e6; // High Frequency
Zo =50;      // Characteristic Impedance
N  = 4;      // Filter Grade

// FR4 physical characteristics and PCB parameters definitions:

Er = 4.7;    // Relative permutability
lt = 0.021   // Loss Tangent
H  = 0.001;  // Dielectric thickness specified in meters
T  = 0.00001; // Trace thickness specified in meters

// First Set of calculations:

D   = (f2-f1)/fc;
iat = (f2/fc)-1;
Wo  = sqrt((2*%pi*f1)*(2*%pi*f2));
Vp  = 3e8/sqrt(Er);

// Defining column vectors to store values/results

J_N  = zeros(5,1);
ZO_N = zeros(5,1);
ZE_N = zeros(5,1);

// For a 4th order Chebyshev Filter, the g parameters are:

g0 = 1;
g1 = 1.6703;
g2 = 1.1926;
g3 = 2.3661;
g4 = 0.8419;
g5 = 1.9841;




// Transforming the low pass filter to bandpass filter //

//  Parallel Components
```

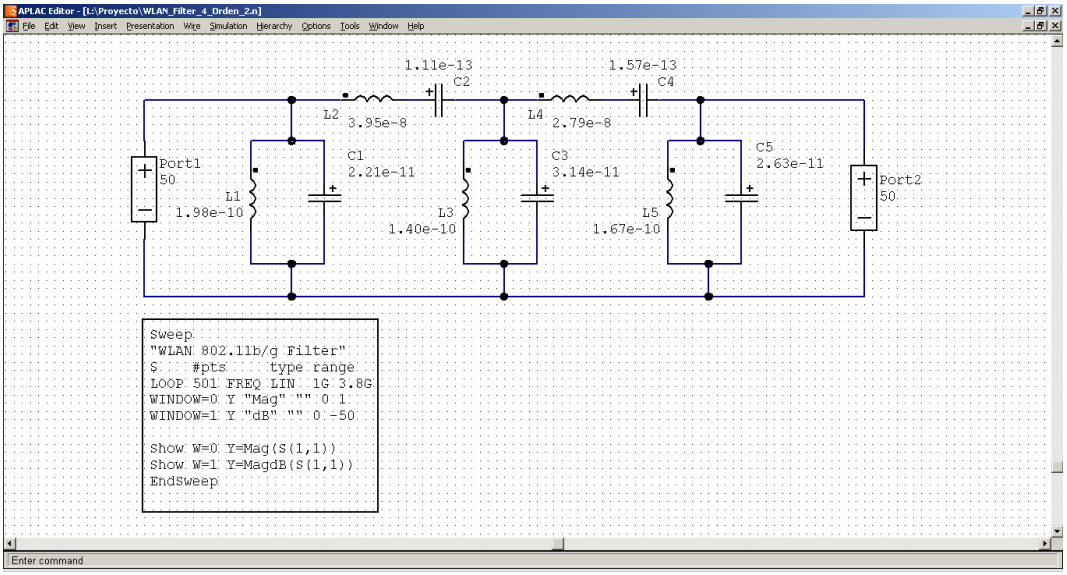
```
L1=(Zo*D)/(Wo*g1);
C1=g1/(Zo*Wo*D);

L3=(Zo*D)/(Wo*g3);
C3=g3/(Zo*Wo*D);

L5=(Zo*D)/(Wo*g5);
C5=g5/(Zo*Wo*D);

// Serial Components

L2=(Zo*g2)/(Wo*D);
C2=D/(Zo*Wo*g2);

L4=(Zo*g4)/(Wo*D);
C4=D/(Zo*Wo*g4);


// Odd and Even Z characteristics calculations:

J_N(1,:) = (1/Zo)*sqrt((%pi*D)/(2*g0*g1));
J_N(2,:) = (1/Zo)*sqrt((%pi*D)/(2*g1*g2));
J_N(3,:) = (1/Zo)*sqrt((%pi*D)/(2*g2*g3));
J_N(4,:) = (1/Zo)*sqrt((%pi*D)/(2*g3*g4));
J_N(5,:) = (1/Zo)*sqrt((%pi*D)/(2*g4*g5));

ZO_N(1,:) = Zo*(1-(Zo*J_N(1))+((Zo*J_N(1))^2));
ZO_N(2,:) = Zo*(1-(Zo*J_N(2))+((Zo*J_N(2))^2));
ZO_N(3,:) = Zo*(1-(Zo*J_N(3))+((Zo*J_N(3))^2));
ZO_N(4,:) = Zo*(1-(Zo*J_N(4))+((Zo*J_N(4))^2));
ZO_N(5,:) = Zo*(1-(Zo*J_N(5))+((Zo*J_N(5))^2));

ZE_N(1,:) = Zo*(1+(Zo*J_N(1))+((Zo*J_N(1))^2));
ZE_N(2,:) = Zo*(1+(Zo*J_N(2))+((Zo*J_N(2))^2));
ZE_N(3,:) = Zo*(1+(Zo*J_N(3))+((Zo*J_N(3))^2));
ZE_N(4,:) = Zo*(1+(Zo*J_N(4))+((Zo*J_N(4))^2));
ZE_N(5,:) = Zo*(1+(Zo*J_N(5))+((Zo*J_N(5))^2));

// Displaying Results

// Concentrate Components Topology:

   disp("WLAN BAND-PASS FILTER");

   disp("L1 = "+string(L1));
   disp("C1 = "+string(C1));

   disp("L2 = "+string(L2));
   disp("C2 = "+string(C2));

   disp("L3 = "+string(L3));
   disp("C3 = "+string(C3));

   disp("L4 = "+string(L4));
   disp("C4 = "+string(C4));

   disp("L5 = "+string(L5));
   disp("C5 = "+string(C5));

   disp("Zodd = "+string(ZO_N));

   disp("Zeven = "+string(ZE_N));
```

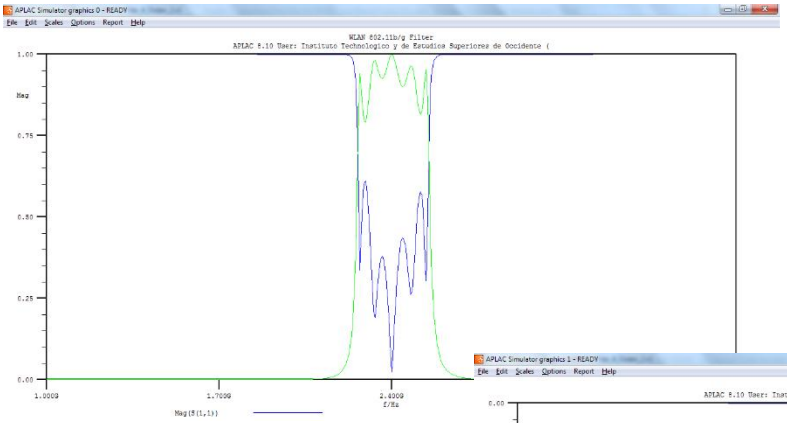
Found results are shown below:



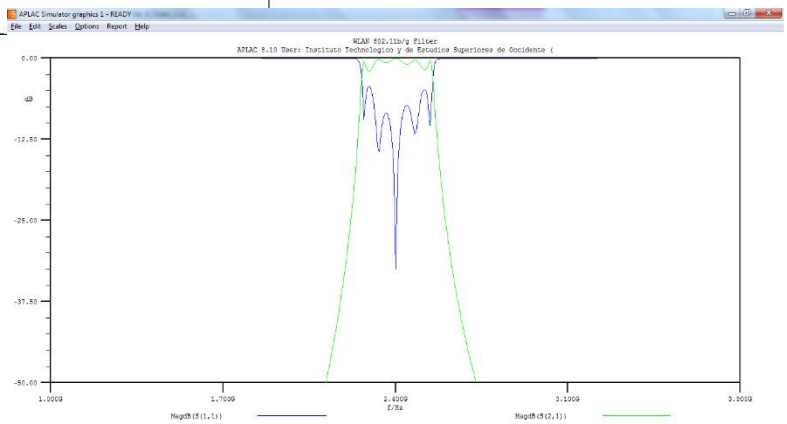
Up to this point, we can start simulating the circuit made of concentrate devices only. This will demonstrate that the filter is well calculated according to specifications. The simulation will comprehend from 1GHz to 3.8GHz, plotting S_{11} for dB and magnitude.

APLAC simulations with concentrated components:





Mag



dB

Now it is time to define the geometry to be used by this filter. Since Richardson's and Kouda´s transformations do not work as desired due to the low impedance traces needed, another option has been foreseen: The Parallel-Coupled filter. To properly define the shapes and spaces, it was necessary to calculate the Zodd and Zeven and then consider the results, and the characteristic impedance of each coupled trace (Calculus found in the script shown before).

Once this point was reached, it was mandatory to think about what material was expected to be used for the filter, depending on the material parameters itself or even on availability and price. For this study, it was decided to use the popular FR-4 with the following physical parameters:

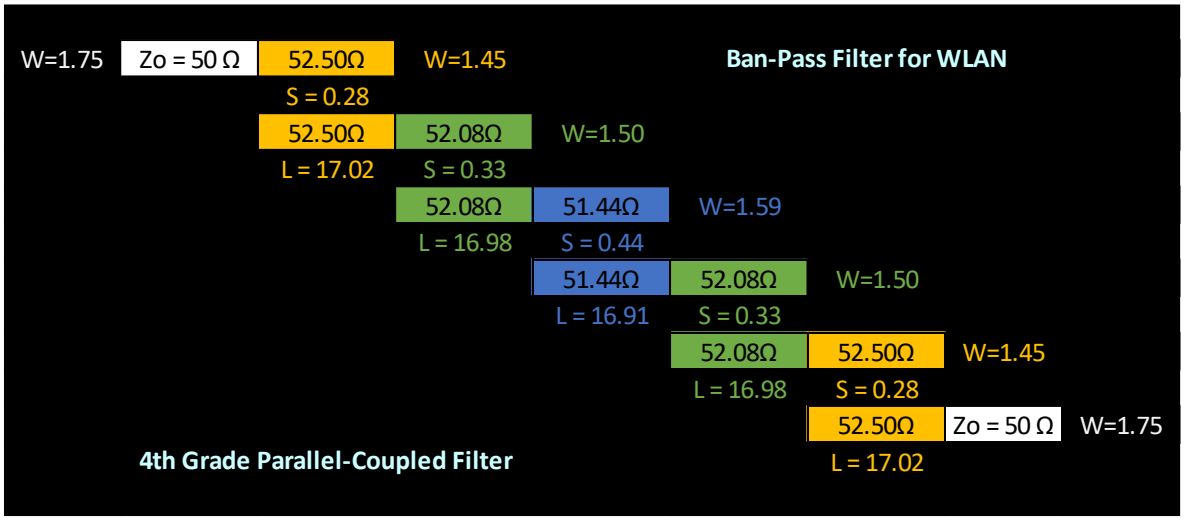
Rigid FR4 standard PCBs – electrical characteristics

Characteristic	Unit	Value/property/content
Dielectric coefficient (εr)	-	4,7
tan δ	-	0,021
Volume resistant	Ωcm	3,0 x 10e13
Electric strength	kV/mm	30
Surface resistant	Ω	2,0 x 10e13
CTI	V	>175

With all the data up to this point, a synthesis calculator was used to define the W (Width), L (Length), and S (Spacing) that will provide the desired response. The table below summarizes the parameters:

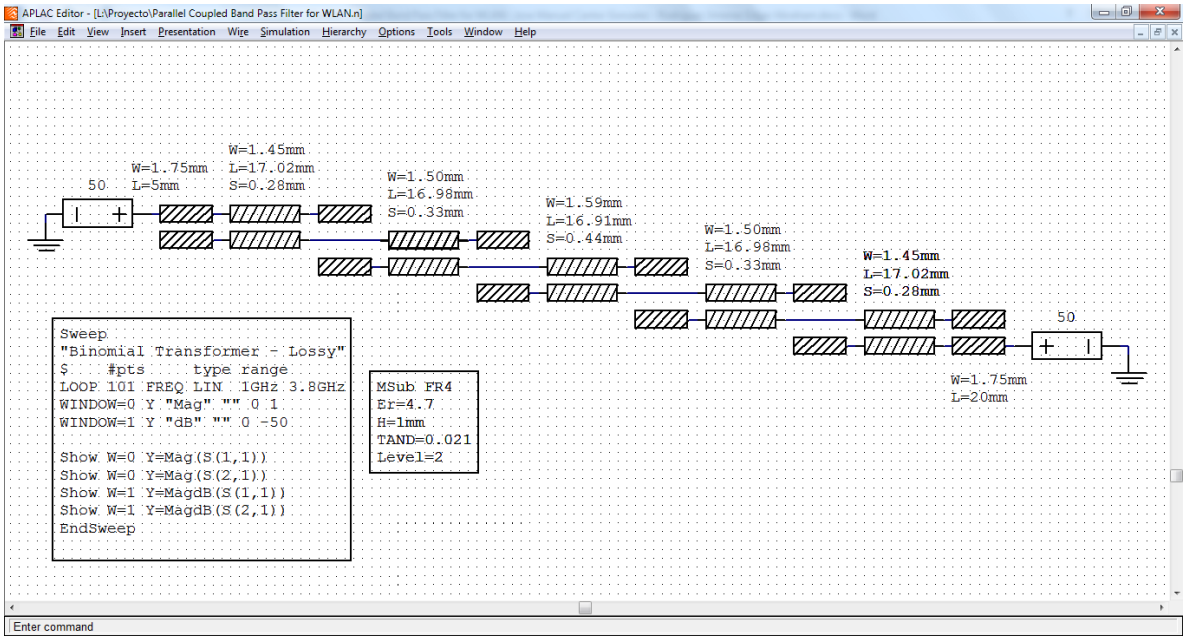
N	Z_{odd}	Z_{even}	Z_0	W	L
1	39.36	70.03	52.5	1.45	17.02
2	39.9	67.98	52.08	1.5	16.98
3	40.98	64.58	51.44	1.59	16.91
4	39.9	67.98	52.08	1.5	16.98
5	39.36	70.03	52.5	1.45	17.02

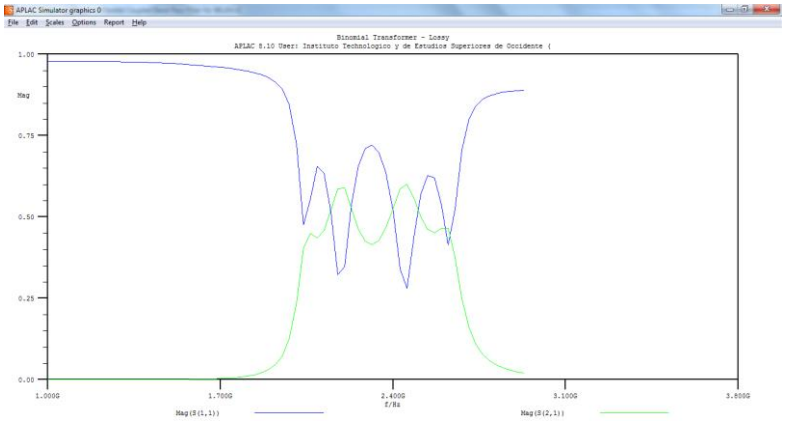
Finally, the final topology outcome consists of 5 coupled pairs that placed together form a 4th-grade filter working at the central frequency of 2.4 GHz and a 240 MHz bandwidth:



APLAC implementation is demonstrated below using lossy traces, which in reality has a depredated performance compared to the concentrated simulation.

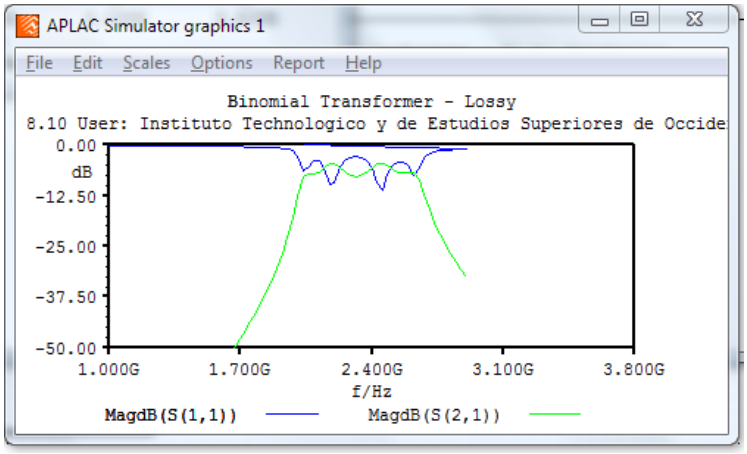
APLAC simulations with concentrated components:



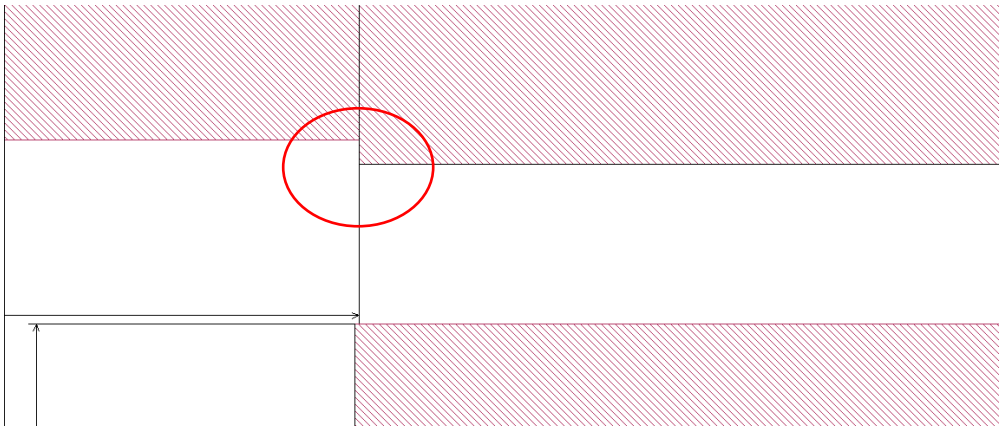


Mag

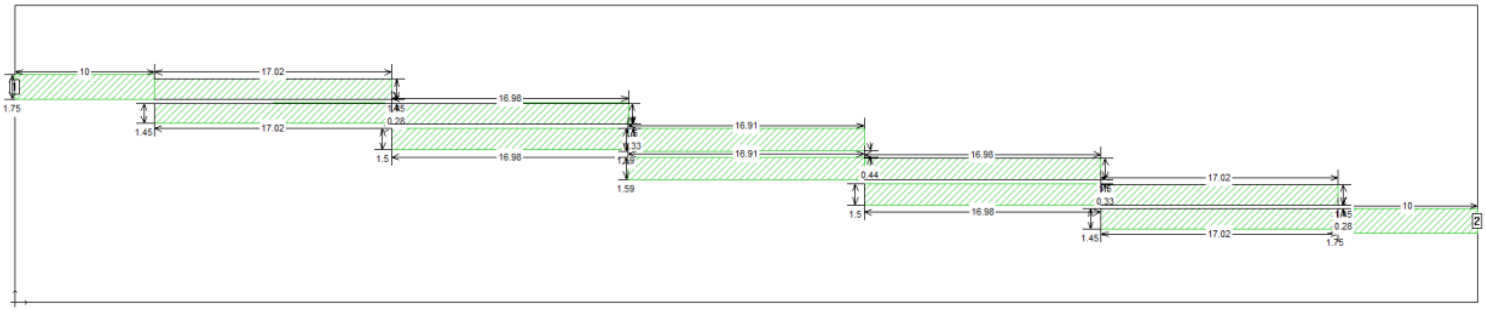
dB

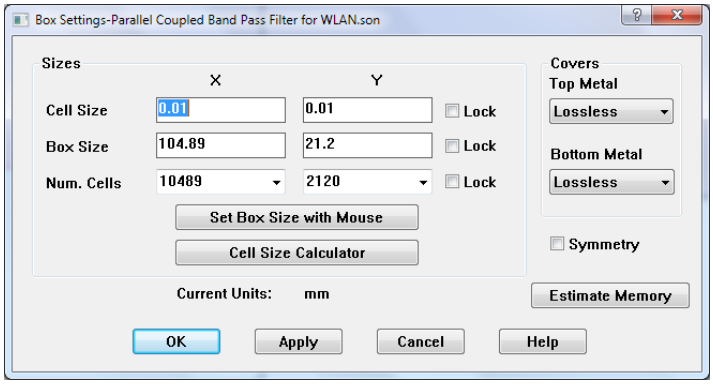


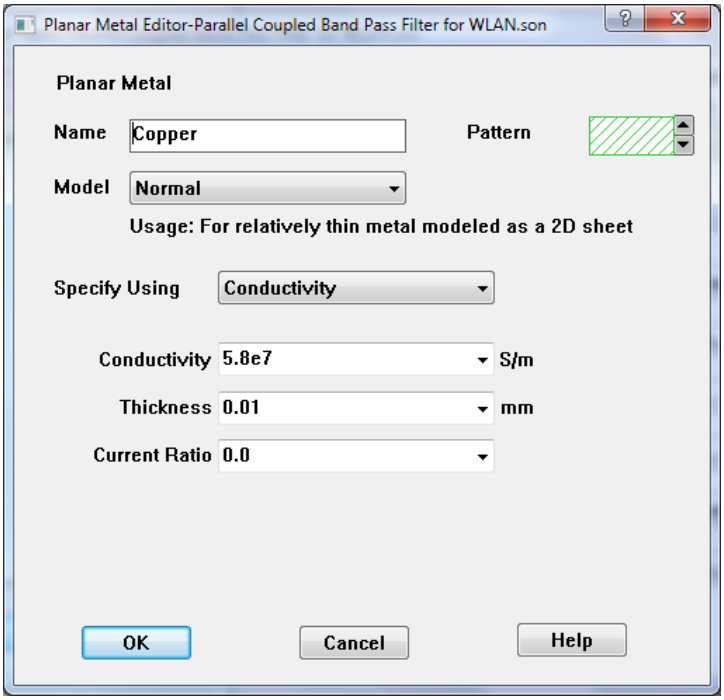
Additionally, Sonnet simulations were performed to compare against APLAC, to appreciate the effects of the details that APLAC cannot consider as the mismatch in the borders of the joins.

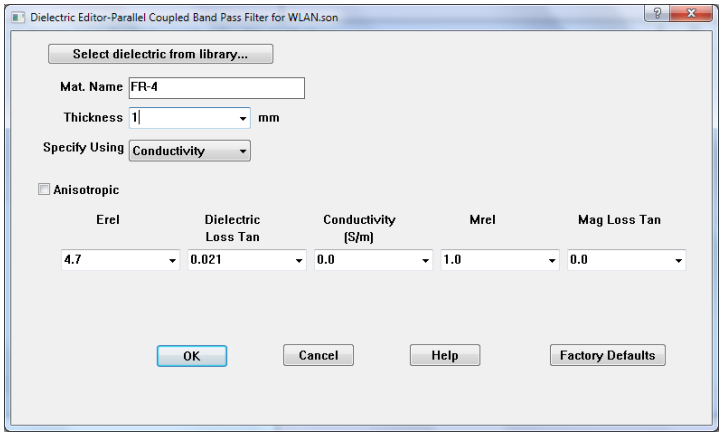


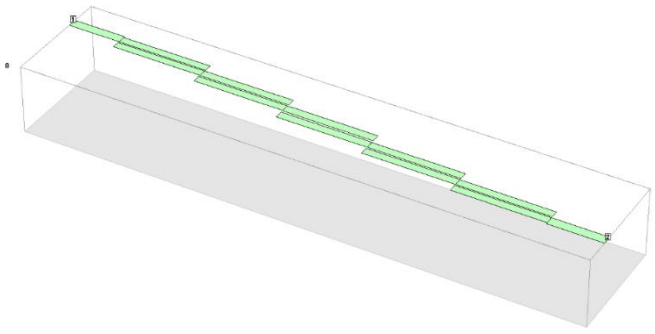
Sonnet simulations with distributed components:



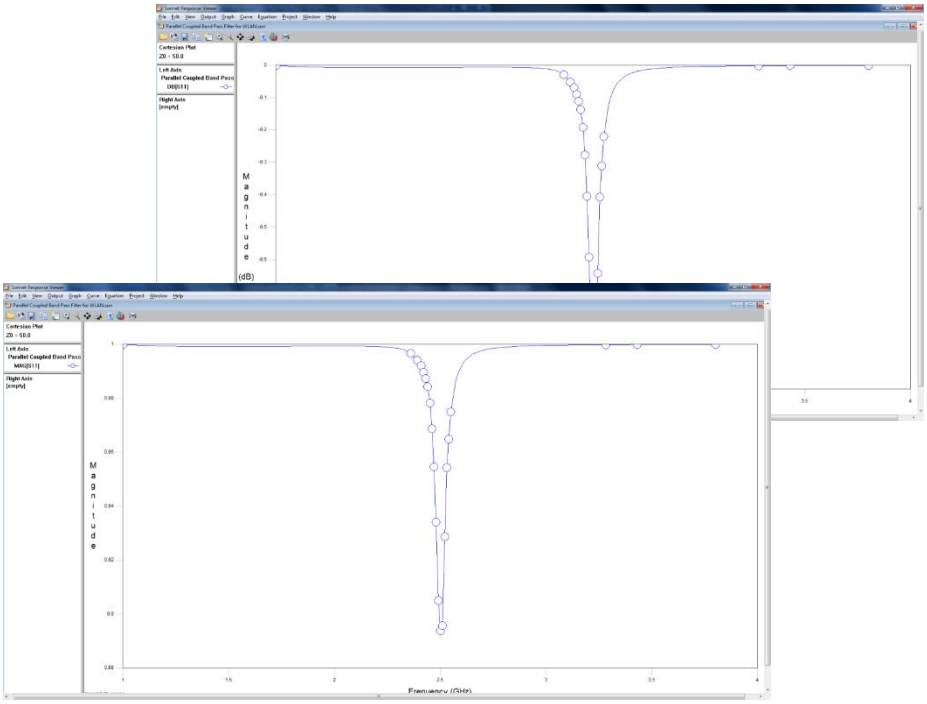




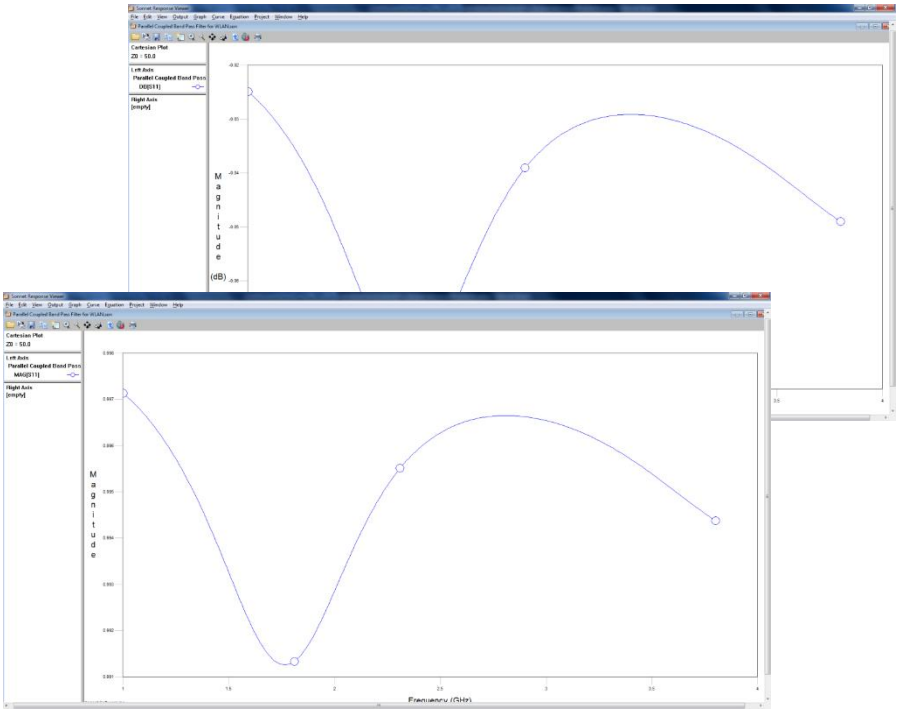




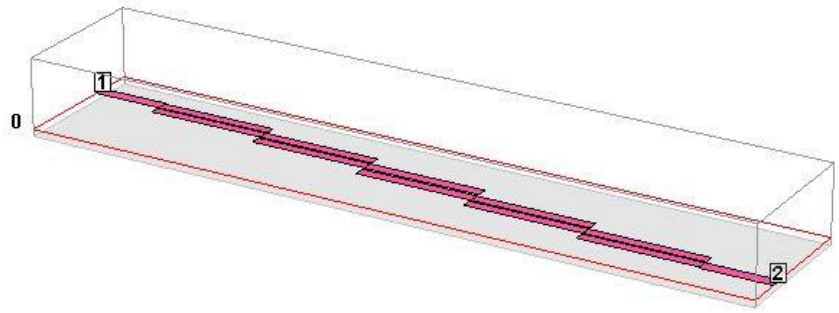
Lossless:

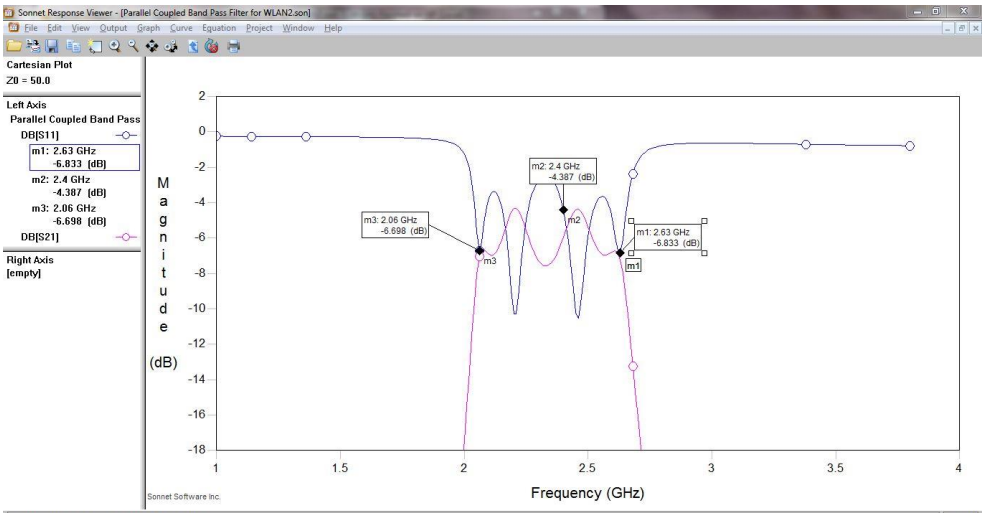


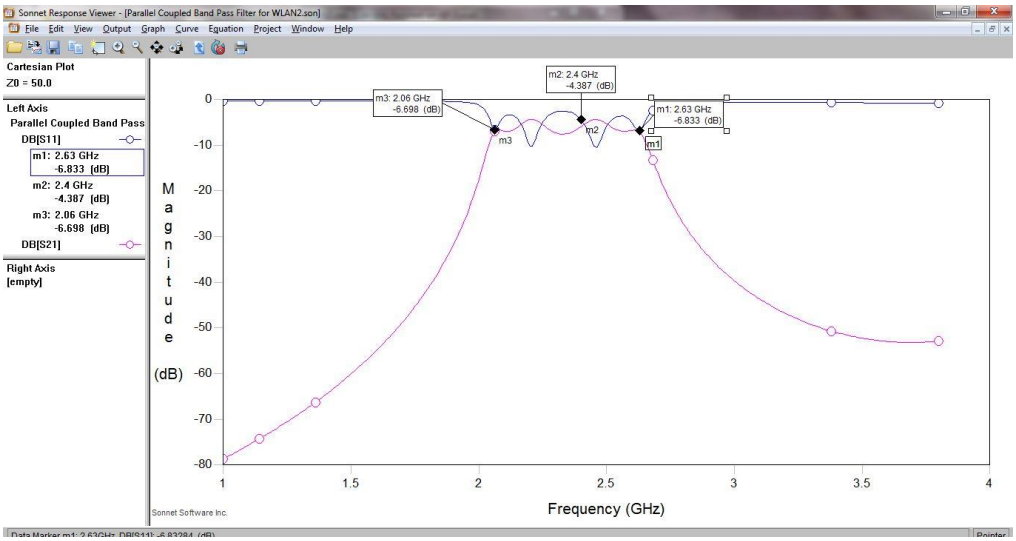
Lossy:



Sonnet simulations with distributed components with air:







Conclusions:

In conclusion the experience, we got during this work, we can summarize three main points that we consider as the "key" to a good design:

- Central frequency, bandwidth, and the grade of the resulting filter are essential factors in the design. It may be obvious, but it is not when defining the geometry that better suits your design. Mathematically, most of the time it is possible to find solutions but not always this solution is practical. Depending on the application, and the frequencies defined the topology may be different, furthermore, variables such as the material, space (real estate), and more are considered for practical and real applications.

- Simulation results and their interpretation. We must never forget that a simulation is just a tool that helps to create a workable design, but it is not a matter of "design and build". You need to always question your simulation tools and methods and make sure you understand how they work to make accurate decisions not only on the design itself but also on the tools and methodologies. From our point of view, the time spent during simulations is the part that makes the design successful or not.

- Choose wisely, not always the first approach it is the right way to go. Open your mind, eyes, and as many books and papers as possible. They will make you learn and understand better. And of course, share your results!

The optimization process will improve filter performance. But for this course, it is out of scope and so for the analysis.

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- D. M. Pozar, Microwave Engineering, Wiley, 2005.

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C. Optimization of a Single-Stub Shunt Tuning Network through Space Mapping

Optimization-Based Modeling and Design of Electronic Circuits

Edgar Rodriguez - Jose Manuel Cantor

01/05/2017

ITESO

Introduction

During the development of state-of-the-art technologies, high-speed signals require special treatment due to their constant speed increase. Matching loads is one parameter to take care of, using microstrip configurations is a good option for matching loads for high-speed signals.

This work shows the optimization of a single stub shunt tuning network on a transmission line using space mapping (Figure 1). This is a simple synthetic problem that will be used to illustrate the benefits of using a space-mapping approach over other techniques like parameter extraction.

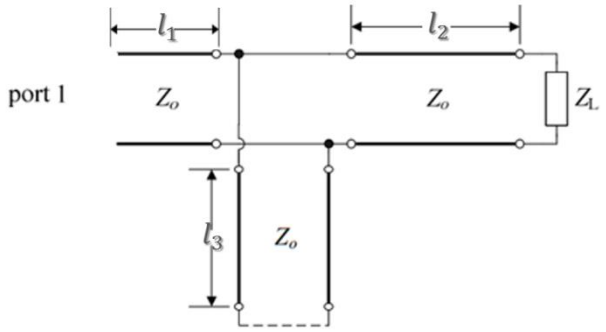

Figure 1

Optimization Problem:

The transmission line described in Figure 1, needs to be matched to load impedance Z_L which consists of 0.8 pf in parallel with 73 ohms, considering a characteristic impedance of 50 ohms and operation frequency of 4GHz.

Design parameters:

H = 0.25 mm, ε_R = 4.12 and tan δ_d = 0.01.

The coarse model will not consider losses on the transmission line and will start from an optimized point, that satisfies the requirements of the design (Figure 2).

$$x_c = \ [100mm\ 0.99mm\ 13.11mm]$$

Note: Optimized values extraction of x_c are explained on complementary information.

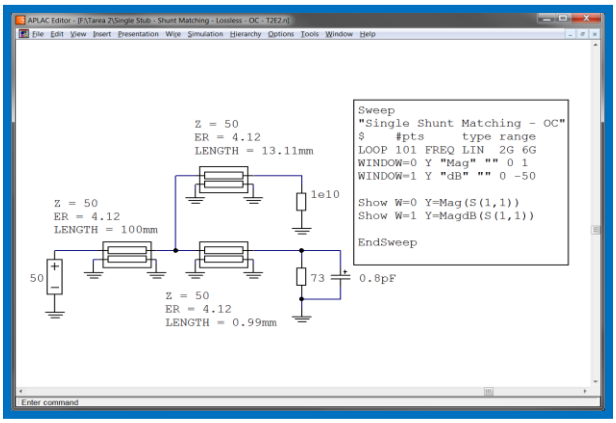

Figure 2

Whereas the fine model will take into consideration the losses of the material (Figure 3)

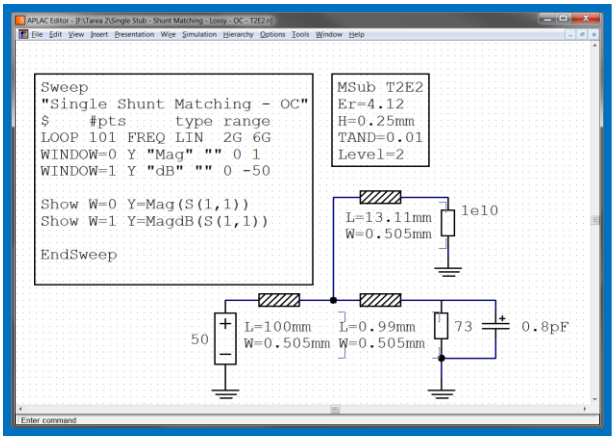

Figure 3

Initial Response using the coarse model and fine model is shown in Figure 4, in blue is the coarse model which provides the exact response required at 4GHz, whereas in red is the response of the fine model is deviated from the expected response. The objective of optimizing the fine model with Space mapping is to get an x_f* which response complies with the 4GHz on spec.

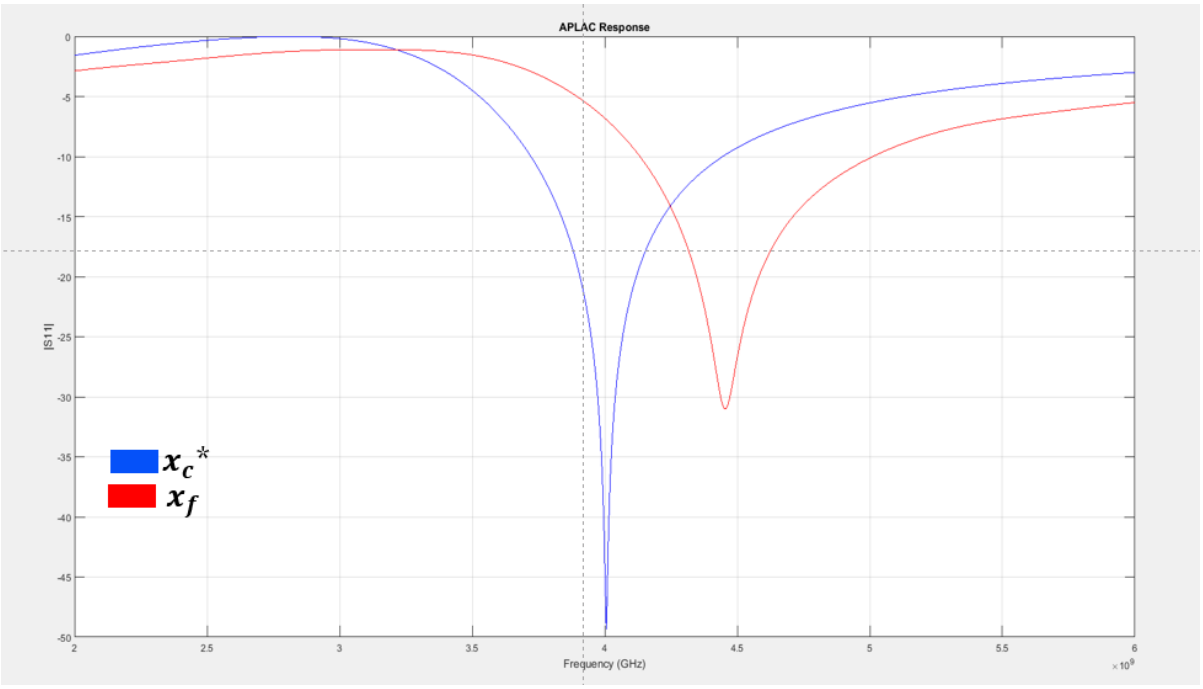

Figure 4

The basic requirements to use Space mapping optimization are having a fine model and a coarse model, once those models are available, x_c optimized needs to be gotten as the first step to develop Space mapping.

Current work was optimized using the **"Broyden-based input space mapping algorithm"**, which requires as input the x_c optimized, and gets the parameter extraction on coarse model in a cycling routing, once parameter extraction is gotten results of new x_f is evaluated on fine model, to look for the parameters that Fine model needs to get a response of 4Ghz as the

coarse model. Figure 5 depicts the flow diagram of the **"Broyden-based input space mapping algorithm"**

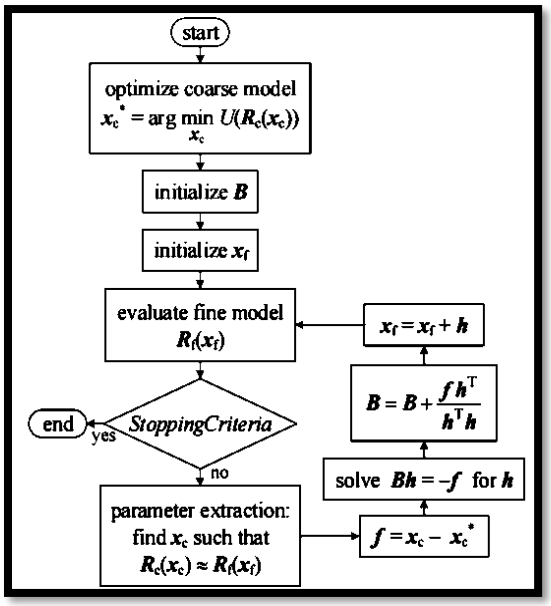

Figure 5

After running the **"Broyden-based input space mapping algorithm"**, the gotten results are:

- x_f* In green, behaves the same as x_c* as expected.
- The lengths needed by the fine model to comply with the specs are:

$$x_f* = [1mm\ 1mm\ 15.0072mm]$$

The number of iterations to find out the x_f* was 22. Figure 6 shows the comparison among x_c*, x_f and x_f*.

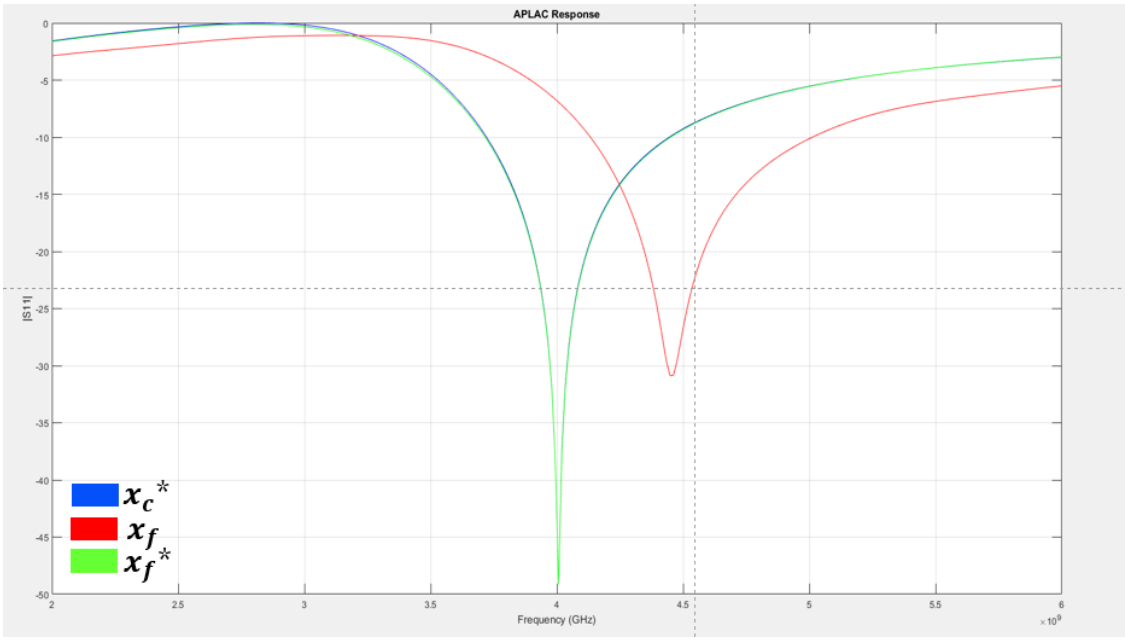

Figure 6

Conclusions:

- Just some evaluations of the fine model are needed, this avoids the usage of computing power in excess. Almost all the simulations in APLAC are done with a coarse model, which requires less time and less computing power than using the fine model.

- During optimization, the response behavior oscillated and took a lot of iterations, this could be for 2 reasons:

    1. Length for input of the shunt tuning network was added as an optimization variable, but it could be ignored.

    2. Because normally shunt networks have 2 optimized solutions, but in the end the algorithm converged to 1 of them.

- A different response is expected if the model is simulated on an electromagnetic simulator as a Sonnet.

References:

- Space mapping techniques Notes. Dr. José Ernesto Rayas Sánchez
- D. M. Pozar, Microwave Engineering, Wile
- Matlab Help

Complementary Information

The process to calculate x_c* is as follows:

Calculate the inductive reactance for the capacitor on the load:

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi * 4x10^9 * 0.8x10^{-12}} \approx 49.735\ \Omega$$

And then calculate the parallel of the resistor and the capacitor:

$$Z_L = \frac{R_L * (-X_C)}{R_L + (-X_{C)}} = \frac{73 * (-49.735)}{73 + (-49.735)} \approx 23.143 - 33.968j$$

The Smith chart will be used to find a suitable solution (Figure A1), but before Z_L should be normalized.

Normalizing Z_L:

$$z_L = \frac{Z_L}{\mathrm{Z_o}} = \frac{23.143 - 33.968j}{50} \approx 0.46 - 0.68j$$

From the Smith chart (Figure A1) it is observed that two points of the SWR circle intersect the 1+jb perimeter:

$$y_1 = 1 + 1.25j$$

$$y_2 = 1 - 1.25j$$

Smith Chart

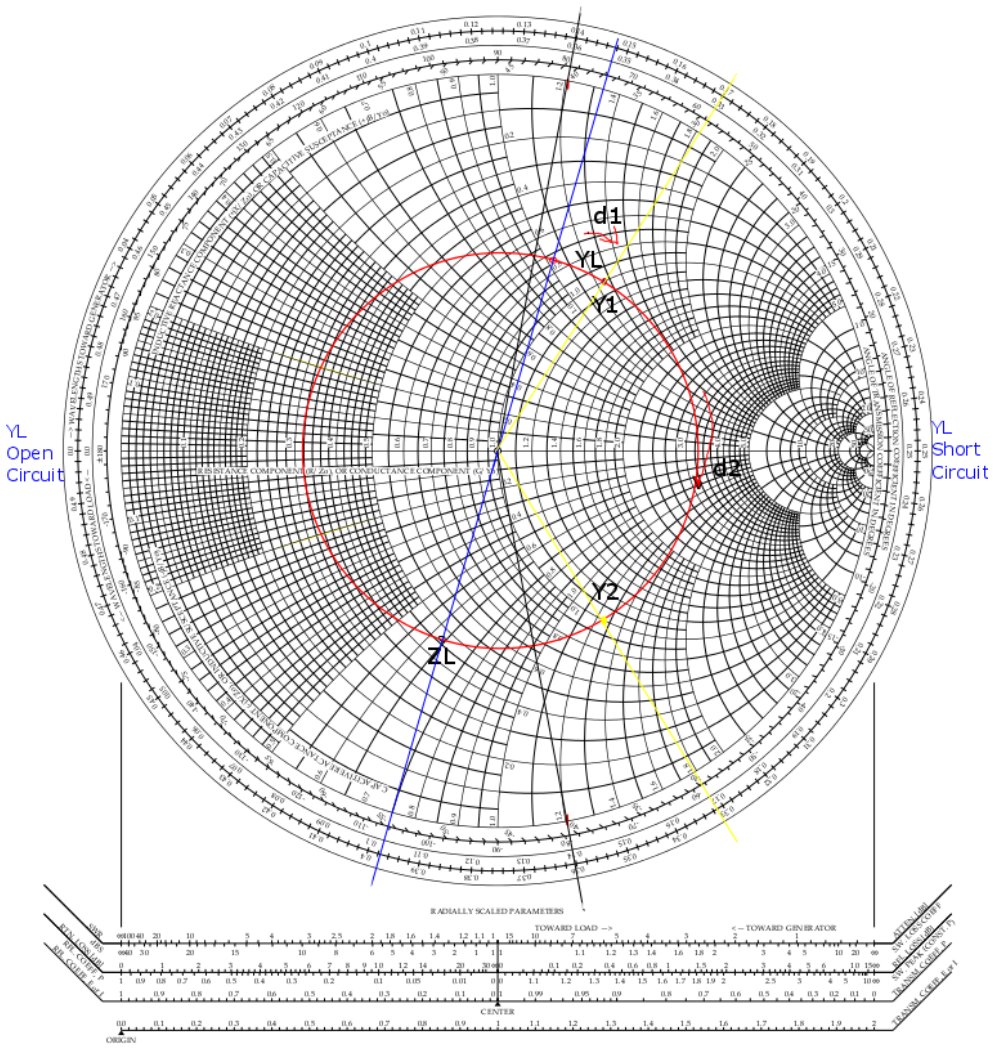

Figure A1

Then, distance is obtained from the normalized load admittance to both points toward the generator:

$$d_1(to\ y1) = 0.170 - 0.143 = 0.027\ \lambda\ (\mathrm{d_{min}})$$

$$d_2(to\ y2) = 0.330 - 0.143 = 0.187\ \lambda$$

In this case, the solution belongs to the left (side value of the Smith chart to the point marked as L1, resulting in:

$$\ell_{oc} = 0.358\lambda$$

To simulate in APLAC the results, it is necessary to transform to millimeters d_{min}, ℓ_{OC} :

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3x10^8}{\sqrt{4.12}} \approx 147.8x10^6 \qquad \lambda = \frac{v_p}{f} = \frac{147.8x10^6}{4x10^9} \approx 0.0369m \approx 36.9\, mm$$

$$d_{min} = 0.027 * \lambda \approx 0.99 \text{ mm}$$
$$\ell_{OC} = 0.358 * \lambda = 13.11 \text{ mm}$$