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DEVELOPMENT OF NANOIMPRINT LITHOGRAPHY PROCESSES FOR STATE-OF-THE-ART LIGHT MANAGEMENT STRATEGIES TO BE INTEGRATED IN CIGS SOLAR CELLS

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Development of Nanoimprint Lithography processes for state-of-the-art light management strategies to be integrated in CIGS solar cells

Para os meus pais e Inês

ACKNOWLEDGMENTS

"For the things we have to learn before we can do them, we learn by doing them." (Aristotle)

ABSTRACT

The growing energy demand requires a strong portfolio of sustainable energy sources, such as photovoltaics. Notwithstanding, it is imperative to minimize critical raw materials consumption for the implementation of these renewable solutions. In this regard, record-efficiency thin-film solar cells based on $Cu(In,Ga)Se_2$ (CIGS) are moving from a micrometre absorber to the nanometre range – ultrathin. However, incomplete light absorption arising from this thickness reduction calls for light management solutions which, conversely, demand a cost-effective and high resolution nanofabrication alternative to develop the sub-wavelength structures. This work presents and discusses nanofabrication procedures for light management solutions compatible with ultrathin CIGS technology, via nanoimprint lithography (NIL). Front and rear strategies were considered, through a broadband anti-reflective moth-eye (ME) structure and two photonic crystal schemes, respectively. A gold nanoparticles etch mask was tailored via a 3-cycle thermal dewetting, followed by an optimized reactive ion-etching (RIE) to fabricate a ME NIL master stamp. Two intermediate polymer stamps were used for the ME replication, with anti-sticking layer studies in each procedure, to ensure good demoulding and high pattern transfer fidelity. Two rear scattering architectures based on dielectric SiO_2 photonic crystals were optimized via optical simulations – hemisphere and pillar arrays. A process-flow encompassing an isotropic etch to fabricate the master stamp, an inversion NIL step, and an anisotropic etch were developed for the hemispheres architecture. Two RIE approaches with selectivity close to one were employed for the final etch step to produce proof-of-concept hemisphere-like structures. For the pillars array, a master stamp with the simulated dimensions was fabricated through a process comprising electron-beam lithography, NIL, RIE, and chemical vapour deposition. The photonic crystals enabled a significant diffuse reflectance increase compared to a Bare Si sample, showing the scattering potential of all developed structures.

Keywords: nanoimprint lithography, light management, moth eye, photonic crystals, sub-wavelength structures

RESUMO

A demanda energética requer um portfolio sólido de fontes de energia sustentáveis, como a fotovoltaica. Contudo, é imperativo minimizar o consumo de matérias-primas críticas nas soluções renováveis. Neste sentido, a transição de uma camada absorvente micrométrica para nanométrica (ultrafino) tem vindo a ocorrer em células solares de $Cu(In,Ga)Se_2$ (CIGS). Porém, a absorção incompleta de luz decorrente desta redução de espessura, requer a implementação de esquemas de manipulação de luz. Todavia, o desenvolvimento de estruturas com dimensão menor que o comprimento de onda da luz necessita de um processo de nanofabricação que garanta resolução e baixo-custo. Este trabalho apresenta e discute diferentes procedimentos de nanofabricação via litografia por nanoimpressão (NIL), para a integração de esquemas de manipulação de luz na tecnologia CIGS. Duas estratégias, para a superfície frontal – através da estrutura anti-refletora "moth-eye" (ME), e para o contacto posterior – através de dois esquemas de cristais fotónicos, foram estudadas. Desenvolveu-se uma máscara de nanopartículas de ouro via 3-ciclos de "thermal dewetting", seguido de erosão reativa iónica (RIE) para um molde ME para NIL. Usaram-se dois moldes poliméricos intermédios para replicar a ME, com estudos da camada antiaderente para assegurar um bom desmolde e fidelidade no padrão transferido. Otimizaram-se duas arquiteturas para dispersão de luz baseadas em cristais fotónicos de SiO_2 através de simulações óticas – matrizes de hemisférios e pilares. Para os hemisférios desenvolveu-se um procedimento que engloba erosão isotrópica para o molde, NIL para inversão e erosão anisotrópica. Finalmente, duas opções de RIE com seletividade ~1 foram usadas para produzir provas-de-conceito de estruturas hemisféricas. Para a matriz de pilares, fabricou-se um molde com as dimensões simuladas via litografia de feixe de eletrões, NIL, RIE e deposição química de vapor. Os cristais fotónicos exibiram um aumento significativo da refletância difusa comparativamente ao Si, demonstrando o potencial para uma eficiente dispersão de luz.

Palavras-chave: litografia por nanoimpressão, manipulação de luz, moth eye, cristais fotónicos, estruturas com dimensão menor que o comprimento de onda da luz

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ACRONYMS

AFM	Atomic Force Microscopy
APS	Advanced Plasma System
AR	Anti-Reflectance
ARC	Anti-Reflective coating
ASL	Anti-Sticking Layer
AuNPs	Gold Nanoparticles
AZO	Al-doped ZnO
BIPV	Building Integrated Photovoltaics
c-Si	Monocrystalline Si
CIGS	$Cu(In,Ga)Se_2$
EBL	Electron-Beam Lithography
EMT	Effective Medium Theory
F13-TCS	1H,1H,2H,2H,-perfluorooctyl-trichlorosilane
FDTD	Finite-Difference Time-Domain
HF	High Frequency (13.56 MHz)
HMDS	HexaMethylDiSilazane
HS	Hemispheres
IBC	Interdigitated Back Contact
ICP	Inductive Coupled Plasma
IQE	Internal Quantum Efficiency
ME	Moth-Eye
NIL	NanoImprint Lithography
NPs	NanoParticles
PECVD	Plasma Enhanced Chemical Vapour Deposition
PL	Pillars
PML	Perfectly Matched Layer
PV	Photovoltaics
RIE	Reactive Ion Etching
RR	Residual Resist
SAM	Self-Assembled Monolayer

SEM	Scanning Electron Microscopy
SLG	Soda-Lime Glass
STU®-NIL	Simultaneous Thermal and Ultraviolet Nanoimprint Lithography
T-NIL	Thermal Nanoimprint Lithography
TCO	Transparent Conductive Oxide
UV-NIL	Ultraviolet Nanoimprint Lithography
WCA	Water Contact Angle

Symbol	Name	Unit
a_1	ASL-1 thickness	m
a_2	ASL-2 thickness	m
ABS	Total light absorbance	%
a_{HS}	Hemispheres nearest neighbour distance	m
a_{PL}	Pillars nearest neighbour distance	m
c	Speed of light	$m.s^{-1}$
$|E|^2$	Electric field intensity	$V^2.m^{-2}$
h	Planck's constant	$m^2.kg.s^{-1}$
h_{PL}	Pillars height	m
$I_{AM1.5}$	AM1.5 solar irradiance spectrum	$W.m^{-2}$
J_{SC}	Short circuit current density	$A.m^{-2}$
n	Refractive index	-
P_{ABS}	Power absorbed per unit volume	$W.m^{-3}$
p_{ABS}	Normalized power absorbed per unit volume by the source power	-
q	Elementary charge	C
r	Hole radius	m
r_{HS}	Hemisphere radius	m
r_{OX}	Etch rate of SiO_2	$m.s^{-1}$
r_{PL}	Pillars radius	m
r_R	Etch rate of resist	$m.s^{-1}$
S	Selectivity of the etch process	-
T_0	Thermal dewetting temperature	K
t_0	Thermal dewetting time period	s
V	Volume	m^3
Z	Etched depth	m
z_0	Initial Au thin-film thickness	m
ε''	Imaginary part of the dielectric permittivity	$F.m^{-1}$
λ	Wavelength	m
ω	Angular frequency	$rad.s^{-1}$

For a very long time, humankind has preferred fossil fuels as its main source to meet the increasing global energy demand. The negative environmental effects are well-known, and thus replacement with renewable sources is urgent to ensure a sustainable future. Additionally, the recent military conflict in Ukraine further accentuates the need for the expansion and decentralisation of the renewable energy sector, as many European countries seek independence from Russian natural gas imports.[1,2]

Solar energy is a strong contender, given the possibility to exploit a virtually infinite energy source. Currently, several photovoltaics (PV) technologies are available, and thin-film solar cells are highlighted as an economical and more sustainable alternative to their competitors since material usage is minimized, while power conversion efficiency values up to 23 % are achieved. This material reduction also opens the path toward implementation on flexible substrates, enabling roll-to-roll production, as well as building integrated PV (BIPV), and further reducing production costs.[3,4] In this category, $Cu(In,Ga)Se_2$ (CIGS) solar cells present great potential, thanks to their direct bandgap, and consequently, high absorption coefficient value, rendering them a solid efficiency within the thin-film solar cells technology.[5,6] Nevertheless, the scarcity of the elements that compose the absorber raises sustainability concerns and limits the competitive position of this technology. Thus, there is a trend toward ultrathin CIGS devices, with a further absorber thickness reduction to a sub-micrometre scale, as a strategy to minimize material consumption and, thus, cost, as well as allowing for more unusual aesthetics (colour, shapes, …) , compatible with a decentralised energy fostering concept. This, however, poses new challenges, as ultrathin CIGS devices have yet to surpass thin-film power conversion efficiency values due to incomplete light absorption and interface recombination losses. Notwithstanding, optical losses can be tackled by implementing light management strategies, as these have successfully improved the performance of other PV technologies.[7] This is rather challenging in CIGS, particularly for the rear interface since the chosen materials must be compatible with the harsh absorber deposition conditions.[4,7] Moreover, the mandatory high resolution of the nanofabrication procedures, needed to achieve the required architectural dimensions for efficient light management (anti-reflection, scattering, …), comes at a cost. Those may lead to a significant reduction in the throughput, while increasing the production cost. Thus, a high resolution nanofabrication solution that ensures scalability is key for the spread of ultrathin technology in the PV market. The main goal of the present work is to develop nanofabrication process-flow(s), for front and rear light management solutions compatible with the ultrathin CIGS solar cell technology. In this regard, the nanofabrication processes relied mostly on nanoimprint lithography (NIL), and the development of master stamps for light management schemes, that will allow for a fast and high resolution replication of the nanopatterns. Thus, a front anti-reflection architecture – moth-eye, and two rear scattering architectures based on photonic crystals – hemispheres and pillars, are aimed to be settled as optimized schemes to be produced by a simple replication method.

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1.1 CIGS solar cells

Among the several PV technologies available today, it is notable that thin-film solar cells are an alternative that allows for the expansion of PV to various applications, such as BIPV, thanks to its adaptability to flexible substrates. Herein, CIGS thin-film solar cells, with an absorber thickness around 1.5-3 µm, present a record power conversion efficiency value of 23.35 %,[8] owing to their direct bandgap nature, allowing for a high absorption coefficient value, and improved absorber electronic properties via alkaline post-deposition treatments.[5,6] Despite its solid record efficiency value, when CIGS is compared with the monocrystalline Si (c-Si) champion cell, the gap in cell structure complexity is striking. For instance, the record c-Si cell owes its power conversion efficiency of 26.6 % to optical and electronic optimizations, namely, front anti-reflectance (AR) texturization, interdigitated back contacts (IBCs), and passivation layers to boost electrical performance.[9] In contrast, the CIGS champion cell lacks any passivation, or light management strategies beyond the typically used MgF_2 anti-reflective coating (ARC).[8]

The conventional thin-film CIGS solar cell is fabricated in substrate configuration, as illustrated in Fig. 1.1, and is based on a p-n heterojunction formed by the p-type CIGS absorber layer and an n-type buffer layer, typically CdS. CIGS solar cells can be produced on hard or flexible substrates, which are covered by the rear electrical contact. Generally, soda-lime glass (SLG) is used as substrate, and Mo is the standard choice for the back contact since it provides good electrical conductivity, good adhesion, and forms a quasi-ohmic contact with the absorber layer – $MoSe_2$. Following, the absorber layer, CIGS, can be deposited by vacuum processes, such as co-evaporation or selenization of vacuum deposited metallic precursors, or even non-vacuum processes.[6] The deposition of CdS, then forms the n side of the heterojunction via chemical bath deposition and the structure is complete with the i-ZnO/ZnO:Al (AZO) window layer.[6,10] The strategy to elevate the CIGS technology to a more dominant position in the PV market relies essentially on two key points: reduce production costs and enhance cell efficiency.[7]
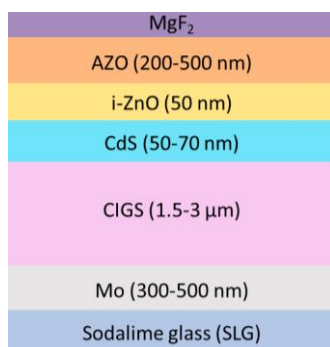
Fig. 1.1 – Schematic representation of a typical thin-film CIGS solar cell. Not to scale.

1.2 Ultrathin CIGS and the demand for light management

Minimizing production costs could be achieved through a reduction in the volume of the raw materials used, especially the scarce elements present in the absorber layer (In and Ga). The shift towards ultrathin absorber layers (sub-micrometre) is a growing trend in CIGS technology, aiming to reduce production costs

with the promise of efficiency.[4,7] However, this thickness reduction incurs an aggravated optical loss, leading to underperformance when compared to the standard thin CIGS solar cells, as demonstrated in Fig. 1.2. Optically, ultrathin CIGS suffer from incomplete light absorption, because the absorber thickness is lower than the required depth to absorb all incident light in a single pass, resulting in a decrease of the short circuit current density (J_{SC}) value.[4,7,11] In addition to the incomplete light absorption, both ultrathin and thin CIGS solar cells are subject to optical losses arising from shading by metallic grids, reflection at the top surface, and parasitic absorption in the buffer and window layers.[4,6] The efficiency gap between ultrathin and thin-film CIGS solar cells can only be diminished through additional optimizations of the cell structure. From an optical point of view, that implies the incorporation of light management schemes which maximize the amount of absorbed light, these have been introduced in other PV technologies.[12–15] Approaches such as, replacing the classic MgF_2 ARC with a broadband AR scheme, and enhancing light reflection and scattering at the rear contact interface are promising strategies to boost ultrathin CIGS performance.[6] Notwithstanding, it is rather challenging to incorporate light management architectures in CIGS, due to fabrication constraints. For instance, the absorber layer is typically deposited at temperatures ranging from 400 to 600 °C, so rear light management architectures must withstand these high temperatures.[4] On the other hand, the buffer layer can suffer degradation or even diffuse to the CIGS if the cell is exposed to temperatures above 200 °C,[4] establishing a maximum process temperature for the development of front light management architectures. Thus, in general, materials and processes employed in the fabrication of light management schemes must respect these limitations, so as not to degrade cell performance. The following Sections will briefly overview light management strategies for the front and rear interface that might be integrated into ultrathin CIGS solar cells, to enhance their optical performance.
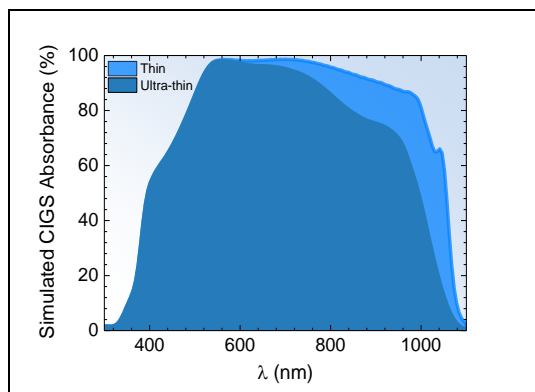
Fig. 1.2 – Simulated CIGS absorbance of thin (2000 nm) and ultrathin (500 nm) solar cell devices, adapted from[7].

1.3   Front light management

At the front side of a CIGS solar cell, one of the optical losses to counter is reflection at the top surface. Currently, the most common solution is the use of a thin MgF_2 ARC, which produces the AR effect through destructive interference between the reflected rays. However, this method is only effective over a narrow wavelength range and close-to-normal incidence angles. Enabling broadband and angle-independent AR is of utmost interest, to enhance light absorption in CIGS especially in applications where an optimal performance is required for diffuse light conditions, such as BIPV without tracking systems.[7] An architecture that satisfies these requirements is micro-scale texturization, as used in c-Si.[9] However, micro-scale features promote scattering, leading to parasitic absorption in the front layers of the CIGS solar cell. On the other hand, some natural structures also exhibit a broadband and omnidirectional AR effect, although without scattering.[16,17] Commonly referred to as moth-eye (ME), this structure is composed of closely packed tapered nanopillars, and the AR results from a gradual refractive index (n) variation,[18] which in turn is explained through the effective medium

theory (EMT). This homogenization theory states that if the period of the features on a texturized surface is much smaller than the incident wavelength value, the wavefront interacts with the structure as a homogenous surface, meaning the nanopillars/air interface is perceived as one material.[19] As such, the resulting n depends on the volume fractions of air and the material, which vary due to the tapered profile of the ME nanopillars, producing the n-grading effect, and reducing reflection drastically.[20] This dense nanostructure architecture has been artificially replicated as arrays of cones, hemispheres, nanopillars, or pyramids in solar cell devices,[21–25] through various techniques, such as electron-beam,[26] colloidal,[27] or interference lithography[24]. Typically, the ME architecture is applied at the solar cell encapsulant layers, such as glass or polymers.[28,29] However, the fabrication of such architecture is expensive, as it is hard to achieve this dense array of nanostructures with a high aspect ratio over large areas. Thus, one of the challenges of this Thesis is to bring a state-of-the-art solution to achieve a low-cost scalable ME scheme.

1.4 Rear light management

At the rear side, light management solutions aim to enhance light scattering and/or reflectivity at the back contact interface, to enhance the optical path length in the absorber. Initial solutions proposed the replacement of the poorly reflective Mo by other metals, such as Au, Ag, Al, or Cu[7]. Yet, this substitution requires adjustments to the absorber deposition processes, because under the typical high processing temperatures these metals may diffuse into the CIGS layer and, as a result, hinder cell performance.[4,7] Alternatively, it has been proposed replacing Mo by a Ag mirror covered by a transparent conductive oxide (TCO).[30–32] While the TCO would prevent Ag diffusion, its lower thermal stability also imposes limitations to the CIGS deposition processes.[31,32] Furthermore, regardless of successfully implementing a perfectly reflective layer at the rear interface, it has been demonstrated that the resulting doubled optical path length is not sufficient to counter the optical losses in the NIR wavelength region – light scattering is required.[7,11] As such, the incorporation of nanoparticles (NPs) at the Mo/CIGS interface is a viable solution, as the optical path length can be enhanced through scattering.[4] Despite their strong light interaction, metallic NPs are not compatible with CIGS technology due to diffusion to the absorber and present parasitic absorption. In contrast, dielectric NPs are absorption-free, thermally and chemically stable, and can also deliver resonant modes as metallic NPs, albeit having to be larger in size.[4,7] This approach has been implemented in other PV technologies previously and has been experimentally executed in CIGS.[33,34] When dielectric nanostructures are tailored into periodic arrays, distinct modes with precise geometrical resonance conditions arise, as a result of the single nanostructures collective response. Thus, the performance of the dielectric resonators can be further optimized when single nanostructures are displayed into periodic arrays – photonic crystals. The interaction between the incident light and these metasurfaces depends on the dielectric material, nanostructure shape, feature dimension, and periodic scheme.[35] So far, a large number of lithography procedures are available to design metasurfaces based on pillars, hemispheres, disks, pyramids, among others.[35] The portfolio of state-of-the-art metasurfaces for energy applications, such as those for broadband light scattering, is well reported by Cortés *et al.*[35], where the challenges to incorporate sub-wavelength periodic structures in market solutions are highlighted. The ideal nanofabrication process should gather high resolution, as well as high throughput allowing for upscaling. Thus, during this work different considerations were taken when choosing the nanofabrication process-flow(s) to develop efficient scattering schemes, and to overcome the trade-off between high resolution and scalability.

1.5 Nanoimprint lithography: high resolution and scalability

Lithography is the core process in the development of sub-wavelength structures, with a multitude of procedures currently available. Notwithstanding, the integration of efficient and cost-effective light management schemes in optoelectronic devices, such as solar cells, requires high resolution and must meet scalability targets[35]. For instance, while electron-beam lithography (EBL) provides state-of-the-art resolution, it is outweighed by the high throughput of photolithography. Therefore, a procedure that satisfies both, high resolution and high throughput, is necessary to render the production of light management schemes a worthwhile solution in PV.

NIL has emerged as a low-cost procedure for the development and production of high resolution nanostructures that also provides the demanded scalability. Succinctly, a master stamp is pressed into a resist layer, and through 3D material displacement and an ensuing curing step, the resist acquires the reverse pattern of the stamp, with nanoscale resolution.[36,37] After imprinting, reactive ion etching (RIE) is performed to remove the residual resist (RR) and expose the substrate, while maintaining the thicker regions of the resist, to enable subsequent etching to fabricate the final structures.[36] NIL resists can undergo thermal (T-NIL), UV- (UV-NIL) curing, or a combination of both through simultaneous thermal and UV curing (STU®-NIL).[36,38] One of the limitations of NIL procedures is that the master stamp is prone to damage and contamination due to being in direct contact with the substrate, and since the stamp's feature size determines the resolution of the imprinted pattern, it is critical to preserve its quality.[36] Notably, the STU-IPS® procedure proposed by Obducat AB[38,39] maximizes stamp preservation by using an intermediate polymer stamp, IPS®. In this two-step approach, IPS® is first patterned with the master stamp by UV-NIL and is then used to pattern the resist surface through STU®-NIL, at a constant imprint temperature. In this way, direct contact of the master stamp with the replicas is supressed, enhancing its lifetime. Furthermore, using soft intermediate polymers such as IPS® or even Ormostamp® has the advantage of higher mechanical flexibility, low-cost, and high resolution.[36,39] Regardless, in any NIL variant the demoulding step is critical for the pattern quality – upon release, the resist must remain attached to the substrate and separated from the stamp. Since the nanoscale features increase adhesion forces between stamp and resist, it is crucial to confer anti-adhesive properties to this interface.[37,39] Thus, demoulding can be facilitated by incorporating release agents in the resist formulation[37] or by coating the stamps with low surface-energy layers, such as a self-assembled monolayer (SAM) of fluorinated silanes[36,40] or a Teflon-like film fabricated from C_4F_8-based plasma.[41] Notwithstanding, as the nanostructures scale is decreased and/or the schemes complexity increases, the thickness of these anti-sticking layers (ASLs) may impose limitations on the resolution, as it can hinder the pattern transfer of closely packed structures.

Along these lines, the main goal of this Thesis is to develop nanofabrication process-flow(s) for front and rear light management schemes, based on NIL, to be integrated into the scalable production of CIGS ultrathin solar cells. Hereof, after the development and production of the NIL master stamp, along with the validation of the patterns replication, the process will rely on a simple replication/stamping procedure, enabling an industrial context to the developed process-flow(s). For front light management, a ME master stamp was developed through RIE using a gold nanoparticles mask fabricated by thermal dewetting, followed by NIL replication tests with varying parameters. For the rear interface, photonic crystals solutions were employed, starting with optimization of the periodic array's geometry and dimensions through optical simulations in the Lumerical software, contemplating nanofabrication constraints. Afterwards, proof-of-concept hemispheres procedures and a pillars master stamp were developed. Overall, this work shows and discusses the challenges associated with the fabrication of sub-wavelength structures, and presents different high resolution and scalable process-flow(s), as high throughput solutions for the integration of efficient light management architectures in solar cells, considering front and rear approaches.

MATERIALS AND METHODS

2.1 Moth-eye structure for front light management

2.1.1 Stamp fabrication

A ME structure was developed through an anisotropic etch of a Si substrate, using a mask of gold nanoparticles (AuNPs).

To launch the development of the ME structure, preliminary etch tests were run to select the most suitable technique. Two homemade AuNPs colloidal suspensions with a nominal diameter of 100 and 140 nm were drop-casted on Si substrates following the procedure in[42]. Samples were split into two etching procedures: alkaline etch with KOH 30 % at 65 °C for 40 s and RIE in SPTS Pegasus with simultaneous SF_6 and C_4F_8 plasma for 20 up to 40 s, henceforth designated ME-PEG. The RIE was the chosen etch procedure to develop the ME structure.

Moving forward, the AuNPs mask was fabricated on a Si substrate using sequential cycles of thermal dewetting and sputtering, based on the procedure proposed by Ray *et al*[43]. A 3-cycle process was used, as schematically represented in Fig. 2.1. Thus, to obtain the AuNPs, a thin Au film with an initial thickness value of z_0 was sputtered (Kenosistec UHV PVD) onto a 5×5 cm Si substrate, which was then annealed at atmospheric pressure in a Termolab Chamber Furnace Type MLM oven at T_0 temperature during a t_0 period. Subsequently, to grow the AuNPs, a thin-film with the same z_0 was sputtered onto the sample and annealed under the same conditions. An additional growth cycle was carried out, to obtain AuNPs with the desired diameter value and surface coverage, resulting in a total of 3-cycles dewetting. Optimizing the AuNPs mask required several tests via z_0, T_0, and t_0 variations to obtain the AuNPs diameter values and surface coverage that meet and gather the targeted AR properties and the nanofabrication limits.
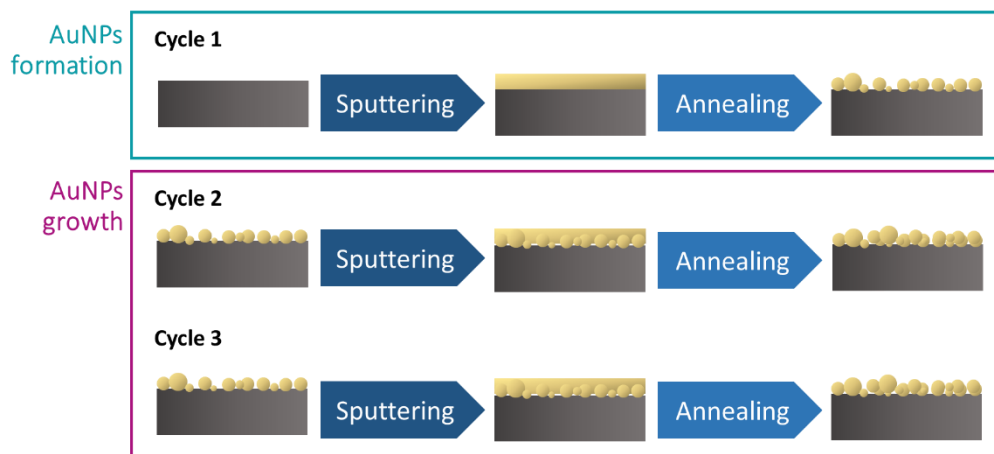
Fig. 2.1 – Schematic representation of the 3-cycles dewetting AuNPs mask fabrication process-flow.

Following, the AuNPs mask underwent ME-PEG to produce the nanopillar ME structure, then AuNPs were removed with a mixture of concentrated hydrochloric acid and nitric acid (HCl:HNO₃) on a 3:1 ratio (aqua regia). The overall process-flow used for the development of the ME master stamp is presented in Fig. 2.2.

Fig. 2.2 – Schematic representation of the ME master stamp process-flow.

2.1.2 Pattern transfer

After the ME stamp fabrication, pattern transfer tests were carried out to optimize the NIL process, aiming to replicate the ME texture. Two NIL procedures were developed using two materials as an intermediate polymer stamp, IPS® and Ormostamp® – coated glass (referred to as OStamp). The schematic for the process-flow is presented in Fig. 2.3. While the patterning of either polymer follow distinct paths, there are key common points in both procedures: an ASL is deposited first on the ME stamp – ASL-1, with thickness a_1, and then on the patterned IPS® or OStamp – ASL-2, with thickness a_2. Following the first UV-NIL imprint, the patterned polymer was used to imprint the ME structure on the resist, through an STU®-NIL step. Thus, there are two demoulding steps, the first one after the intermediate polymer stamp imprint, and the second following the resist imprint. Each procedure is described in detail over the next Sections.
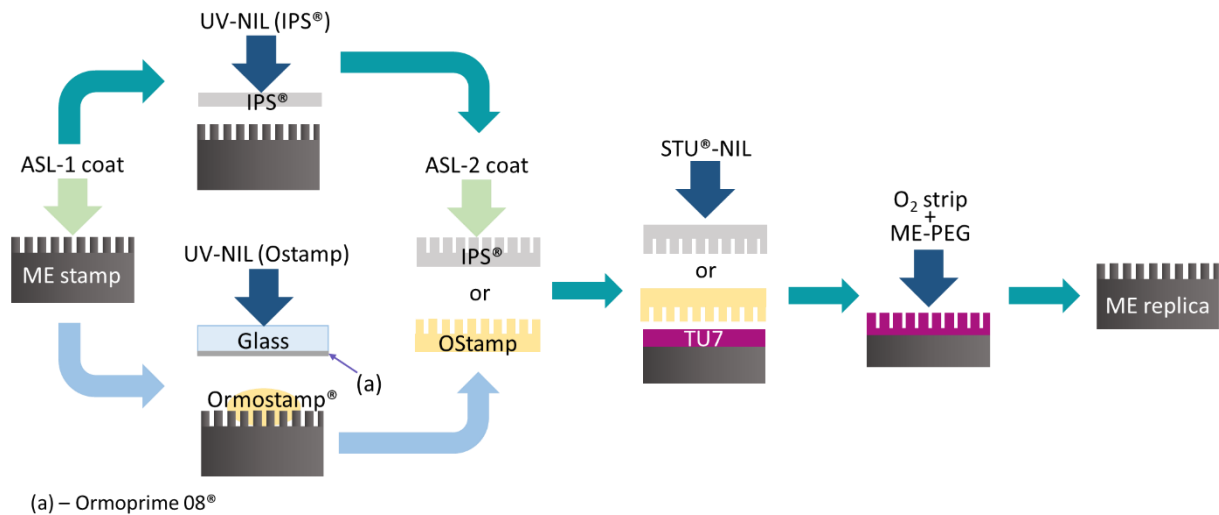
Fig. 2.3 – Schematic representation of the studied NIL process-flow.

2.1.2.1 IPS-NIL

After the deposition of a Teflon-like ASL-1[1]* on the ME stamp, the ME structure is imprinted onto the IPS®, at 22 °C, starting by setting the pressure to 15 bar for 60 s and then exposing it under UV illumination for 240 s – UV-NIL (IPS). The same Teflon-like polymer was used as ASL-2[1]*. Optimization tests were conducted with different combinations of a_1 and a_2 values for the thickness of the ASL-1 and ASL-2, respectively.

2.1.2.2 Ostamp-NIL

To prepare the Ostamp, a 5×5 cm glass substrate was first cleaned to prepare for Ormoprime® 08 spin coating in Suss MicroTec Gamma Photoresist Cluster, with a 300 s bake at 150 °C. This step is critical to ensure good adhesion of the Ormostamp® to the glass. Following, a droplet of 175 μl of Ormostamp® was deposited on the ME stamp, previously coated with a_1 nm of ASL-1[1]*. Then, the glass was carefully dropped onto the stamp, and UV-NIL (OStamp) was carried out. First, the pressure was raised to 10 bar for 600 s,

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[1]* ASL was deposited using C_4F_8 plasma in a STPS Pegasus.

followed by UV exposure for 35 s, under the same pressure – UV-NIL (OStamp). Finally, the stamp and glass stack underwent hard-baking and were separated with a blade. Afterwards, OStamp was coated with a2 nm of a Teflon-like ASL-2[1*].

Several tests were carried out with different combinations of parameters: the glass surface was prepared by 1a) acetone ultrasound bath followed by dehydration[2*] or 1b) O_2 plasma ashing[3*] for 15 min. The adhesion agent, Ormoprime® 08 was spin-coated at 2a) 2000 rpm and 2b) 4000 rpm. Demoulding was performed at different stages of the hard-bake: 3a) upon reaching 80 °C, 3b) upon reaching 130 °C, and 3c) after 30 min at 130 °C of hard-bake; different ASLs were used for the stamp: 4a) 70 nm of Teflon-like coat, 4b) 1H,1H,2H,2H-perfluorooctyl-trichlorosilane (F13-TCS) SAM deposited by vapour-phase for 1 h,[44] 4c) 5 nm of SiO_2[4*] followed by deposition of 28 nm of Teflon-like ASL-1 layer[1*].

2.1.2.3 ME replica fabrication

The Si substrate of the replica sample first underwent a dehydration[2*] process, followed by spin-coating of 300 nm of TU7[5*]. Then, using OStamp as an intermediate stamp, the resist was patterned by STU®-NIL, first raising the temperature to 65 °C for 10 s and next applying 15 bar pressure for 100 s. Finally, UV exposure was done for 180 s. Afterwards, the RR layer was removed with an O_2 strip[6*]. Next, the sample was etched with the ME-PEG process for 60 s and the remaining resist was removed by O_2 plasma ashing[3*] for 8 min.

2.2 Photonic Crystals for rear light management

2.2.1 Optical simulations

Two photonic crystal architectures were studied: SiO_2 hemispheres (HS) and pillars (PL), in a periodic square array configuration, to integrate at the Mo/CIGS interface in an ultrathin solar cell. Additionally, a conventional ultrathin CIGS solar cell was simulated for comparison purposes. Within this framework, optical simulations were employed to overcome the complexity of the CIGS solar cell system, and to study the photonic crystal architectures, considering HS and PL, that will allow for an optical gain, and then guide through the aimed features of the developed metasurfaces. The geometric dimensions were optimized through optical simulations with the finite-difference time-domain (FDTD) solutions package of the Lumerical software. This method retrieves direct-time and space solutions to Maxwell's equations in complex geometries, which enables the determination of frequency-dependent electromagnetic fields.[45] For each architecture, the FDTD simulated region was defined around one unit cell of the periodic array (Fig. 2.4), with anti-symmetric and symmetric boundary conditions in the X and Y directions to reduce simulation time and memory requirements. In the Z direction, perfectly matched layer (PML) boundary conditions were employed. A broadband plane wave source with a wavelength range of 300-1100 nm was used to simulate the solar illumination, in normal incidence. The simulated cell stack had the following configuration: Mo (350 nm)/ $MoSe_2$ (5 nm)/ (SiO_2 HS or PL)/ CIGS (500 nm)/ CdS (50 nm)/ i-ZnO (50 nm)/ AZO (300 nm), with respective complex refractive indexes taken from elsewhere: Mo from [46], $MoSe_2$ from [47], SiO_2 from in-house spectroscopic ellipsometry measurements, CIGS from [48] and CdS, ZnO and AZO and from [49]. Given the incorporation of the nanostructures, the thickness of the CIGS layer was adjusted by volume compensation. Parameter sweeps determined the optimal

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[2*] Dehydration in a Vapour Prime Oven YES-310TA at 150 °C.

[3*] O_2 plasma ashing with 600 sccm flow of O_2 and 50 sccm flow of Ar - PVA Tepla Plasma Asher.

[4*] SiO_2 deposited by plasma-enhanced chemical vapour deposition (PECVD) using an MPX CVD SPTS system at 13.56 MHz, 300 °C with SiH_4 and N_2O chemistry.

[5*] TU7 at 3000 rpm and baked at 90 °C for 60 s - Suss MicroTec Gamma Photoresist Cluster.

[6*] O_2 strip for 12 s, with an O_2 flow of 115 sccm at 13.56 MHz in SPTS Pegasus.

dimensions for each architecture prior to fabrication: radius (r_{HS}) and nearest neighbour distance (a_{HS}) for the HS architecture, and radius (r_{PL}), height (h_{PL}), and nearest neighbour distance (a_{PL}) for the PL array. Moreover, for high accuracy simulations the smallest mesh size was used, with respect to memory and time requirements, as well as override mesh regions over critical interfaces.
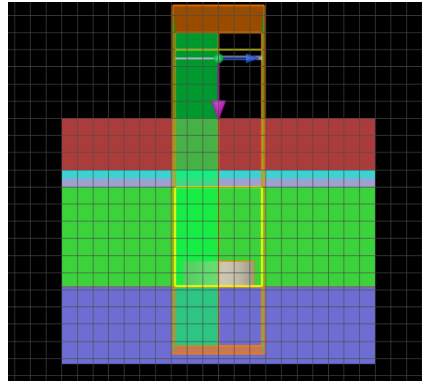
Fig. 2.4 – Simulation setup for the PL architecture.

2.2.2 Hemisphere array fabrication

To fabricate the SiO_2 HS array the process-flow displayed in Fig. 2.5 was proposed. First, using an in-house Si master stamp, a hexagonal 200 nm hole radius array is imprinted on 200 nm mr-NIL 6000 2E[7*] over Si through the UV-NIL (IPS) and STU®-NIL steps described previously. After O_2 strip[6*] of the RR, hemispheric cavities are formed with an isotropic etch, followed by OStamp fabrication to create a stamp with the reverse structure, the HS array. Finally, on the test sample, coated with SiO_2[4*], the 450 nm TU7[8*] resist is patterned by UV-NIL (IPS) followed by STU®-NIL, and the pattern is transferred after an optimized anisotropic etch. To carry out this complex nanofabrication procedure, several steps required optimization: the isotropic etch, the HS OStamp fabrication, and the final anisotropic etch.
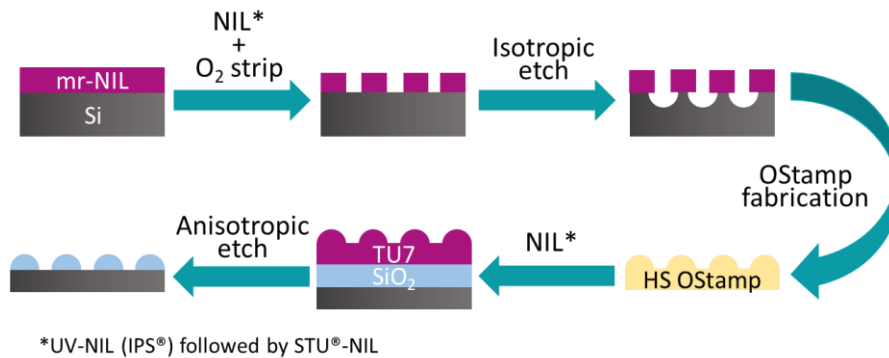
Fig. 2.5 – Schematic representation of the SiO_2 HS array process-flow via NIL.

2.2.2.1 Isotropic etch optimization

Similarly to Section 2.1, the process begins with the NIL stamp fabrication. For the etch mask, 5×5 cm Si substrates were dehydrated[2*], coated with 200 nm of mr-NIL 6000 2E[7*]. The resist was patterned with an in-house Si stamp with a hexagonal hole array with 200 nm radius and 2 μm pitch, following UV-NIL (IPS) and STU®-NIL, using a 70 nm Teflon-like coat for ASL-1 and -2. RR was striped with O_2 plasma[6*] for 12 s. Next,

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[7]* mr-NIL 6000 2E at 3000 rpm and baked at 90 °C for 60 s - Suss MicroTec Gamma Photoresist Cluster.

[8]* TU7 at 1500 rpm and baked at 90 °C for 60 s - Suss MicroTec Gamma Phooresist Cluster.

to produce the hemispheric cavities in Si, an isotropic etch with SF_6 plasma was optimized in SPTS Pegasus, varying the SF_6 flow and the 13.56 MHz (high frequency – HF) coil power.

2.2.2.2 Hemispheric cavity inversion

As an initial test, the hemispheric cavities were reversed into an OStamp following the procedure described in Section 2.1.2.2 with the following parameters: glass surface was cleaned with O_2 plasma[3*] for 15 min. Ormoprime® 08 was spin-coated at 4000 rpm; demoulding was performed at 80 °C. The resulting OStamp, now patterned with HS, was then used as the stamp for the following UV-NIL (IPS) and STU®-NIL steps to pattern the inversion test sample with the HS array, using a 70 nm Teflon-like layer as ASL-1 and -2.

The inversion test was performed on a Si substrate sample coated with 400 nm of SiO_2[4*]. This test sample was dehydrated at 150 °C in a hexamethyldisilazane (HMDS) rich atmosphere (Vapour Prime Oven YES-310TA) and then coated with 430 nm of mr-NIL 6001.0E_XP[9*].

2.2.2.3 Anisotropic etch for the development of SiO_2 hemispheres

Upon the successful imprint of the HS on the resist, optimization proceeded with the development of a single anisotropic etch step to transfer the texture to the SiO_2[4*] layer below. The goal was to find an etch procedure with the same etch rate for the resist and the oxide.[50] First, the etch rate of several in-house procedures was assessed. For this, several Si samples were coated with 500 nm of SiO_2[4*] and either coated with 430 nm of mr-NIL 6001.0E_XP[9*] or 450 nm of TU7[8*]. The resist thickness was measured before and after each etch process.

Following etch rate assessment, two procedures were selected: HS-PEG, a RIE process with 280 sscm of C_4F_8 and 120 sscm of SF_6 based plasma, and HS-ICP, an inductive coupled plasma (ICP) procedure with a 30 sscm CF_4 based plasma (SPTS ICP). In the end, proof-of-concept samples were fabricated using both processes with optimized etch times for the TU7 resist.

2.2.3 Nanopillar array fabrication

2.2.3.1 E-beam lithography for master fabrication

The fabrication begins with EBL to pattern the resist with the sub-micrometric pitch structure. A Si substrate was coated with 150 nm of SiO_2[4*] and primed in an HMDS-rich atmosphere. Then, it was coated with 200 nm of ARN 7520.18 diluted in AR 300-12 in 1:1 ratio at 2750 rpm and baked at 85 °C for 60 s. Following a calibration procedure to find an appropriate electron-beam dose for the desired architecture, an EBL exposure was done with an 11565 µC/cm^2 dose (Vistec EBPG 5200 ES) to create a square array of circles with 550 nm pitch and nominal 200 nm diameter. Afterwards, a post-exposure bake was done at 85 °C for 120 s, followed by development in TMAH for 60 s. Finally, all the exposed oxide was etched by RIE in SPTS Advanced Plasma System (APS) with H_2 and C_4F_8 based plasma at 13.56 MHz, and the resist was stripped[6*] in Plasma Asher. The resulting sample, PL master, was used for the subsequent tests.

2.2.3.2 Stamp fabrication

Following, PL master was replicated to prevent repeating the time-consuming EBL over the ensuing optimization steps. Thus, the goal was to fabricate the PL stamp, with the optimized simulated dimensions: $r_{PL} = 225$ nm, $h_{PL} = 150$ nm and $a_{PL} = 100$ nm. This was achieved through UV-NIL (IPS) followed by STU®-NIL, using a Teflon-like ASL with $a_1 = a_2 = 70$ nm. After NIL, the RR stripping, and the oxide etch step were tuned

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[9*] mr-NIL 6001.0E_XP diluted in ma-T 1045 in a 1:1 ratio at 2000 rpm and baked at 90 °C for 60 s - Suss MicroTec Gamma Photoresist Cluster.

by testing a series of etching procedures combinations. For RR removal, the O_2 strip and the HS-ICP process were tested. The SiO_2 etch was performed in APS. PL stamp is complete after PECVD of SiO_2[4]* to increase the pillars size to the desired radius. The process-flow is presented in Fig. 2.6.

*UV-NIL (IPS®) followed by STU®-NIL
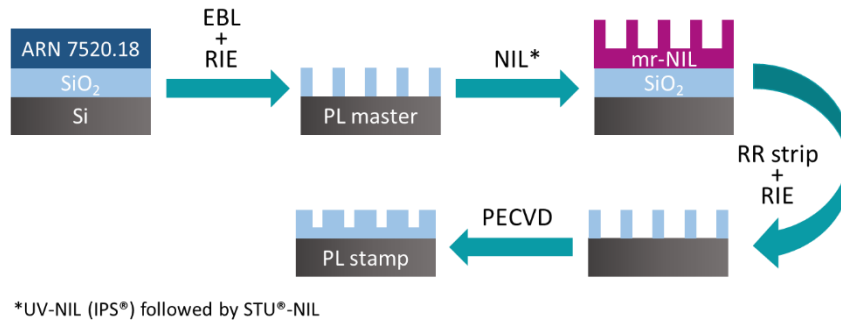
Fig. 2.6 - Schematic representation of the SiO_2 PL array process-flow via NIL.

2.3 Characterization

The presented work is settled in developing different nanofabrication process-flow(s). In this regard, the use of different characterization techniques will allow for an accurate evaluation of the different stages of the process, and proceed through the next steps. Thus, the characterization techniques can be split into: a) evaluation and validation of the nanofabrication architectures and b) evaluation and discussion of the optical properties: a.1) Scanning Electron Microscopy (SEM) imaging was done on NovaNanoSEM650, to assess results over various stages of the processes, and some features were measured with software ImageJ; a.2) atomic force microscopy (AFM) characterization was done in Bruker Dimension Icon Atomic Force Microscope, on tapping mode at 0.5 Hz to evaluate the fabricated features; a.3) the different resists thickness values were scrutinized via an OPM Nanocalc Interferometer; b.1) total and diffuse reflectance spectra from 300-1100 nm were measured in a Perkin-Elmer Lambda 950 UV-VIS-NIR spectrophotometer with an integrating sphere; and finally, water contact angle (WCA) measurements on the ME architectures were performed using a Krüss DSA 100 to evaluate the hydrophobicity of the surfaces.

A summary of the work conducted during this Thesis is displayed in Fig. 2.7.
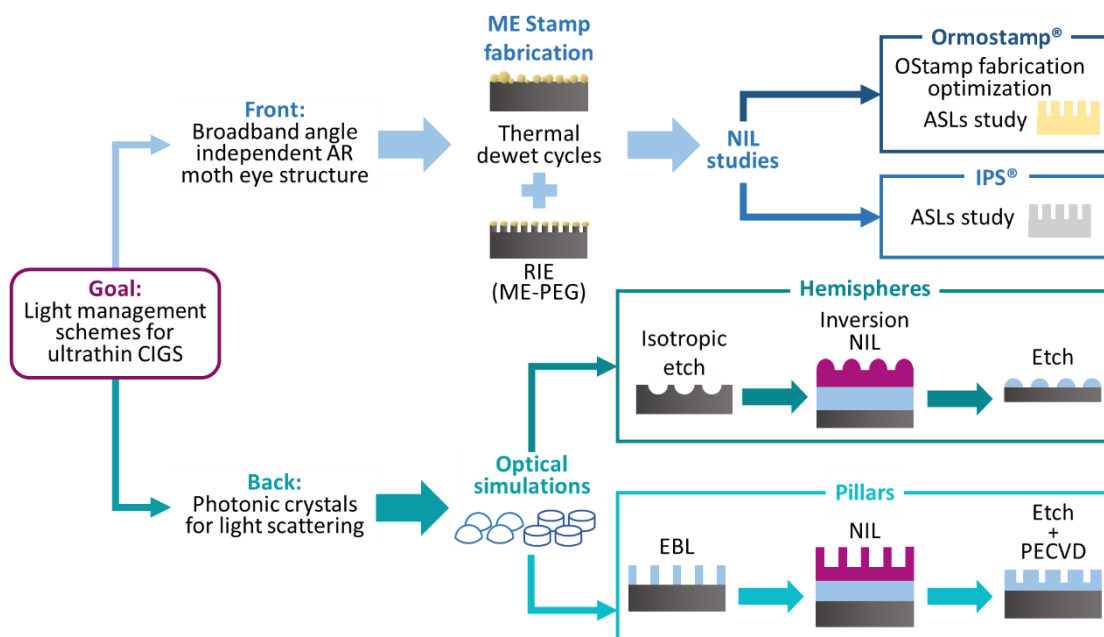
Fig. 2.7 - Schematic representation of the work developed throughout this Thesis.

RESULTS AND DISCUSSION

3.1 Moth-eye structure for front light management

3.1.1 Stamp fabrication

A master stamp for the ME structure was produced by an anisotropic etch of a Si substrate, covered by a mask of AuNPs. In the next Sections, all the developments and overall process-flow(s) to produce the afore-mentioned ME master stamp are presented and discussed.

3.1.1.1 Preliminary anisotropic etching tests

Cross-section SEM images of etched colloidal AuNPs masks are presented in Fig. 3.1. The alkaline based etch (KOH) produced pyramidal nanostructures underneath the NPs, as shown in Fig. 3.1a)-b), demonstrating good selectivity with the etch mask. It has been well reported, in alkaline etchants, that the etch rate of the (111) Si plane is significantly lower than for other planes[51]. This effect has been associated to a higher activation energy to remove a Si atom from the (111) plane, in comparison to the (100) or (110), leading to pyramidal structures. However, the obtained nanostructure height varies throughout the sample, with higher structures in regions with AuNPs aggregates. In contrast, the ME-PEG process produced higher and vertical nanopillars with ~790 nm, with high uniformity throughout the sample (Fig. 3.1c)-d)), in comparison to the nanostructures produced by the KOH etch. The observed vertical profile may be associated with the combined action of the used gas precursors. When the C_4F_8 precursor gas is dissociated it leads to a passivation of the etching area. Then, due to the highly directional ion bombardment, the passivation layer is removed from the bottom of the exposed surface, while the sidewalls passivation is kept. Therefore, the fluorine ions from SF_6 will etch the exposed surface leading to a vertical profile. Furthermore, as shown in Fig. 3.1c) the 100 nm AuNPs were almost completely consumed, while, in Fig. 3.1d) it can be seen that the 140 nm AuNPs were partially etched, thus establishing a threshold on the AuNPs diameter of approximately 100 nm for the etch to be used in the ME master stamp process. In addition, while the sloped structure obtained through KOH etch is more desirable to mimic the ME structure since it promotes a gradual increase in the n value,[16,20] the ME-PEG process assures a good nanopillar height uniformity, mandatory for a controllable nanofabrication process. Thus, the latter procedure was the chosen to move forward with ME development.
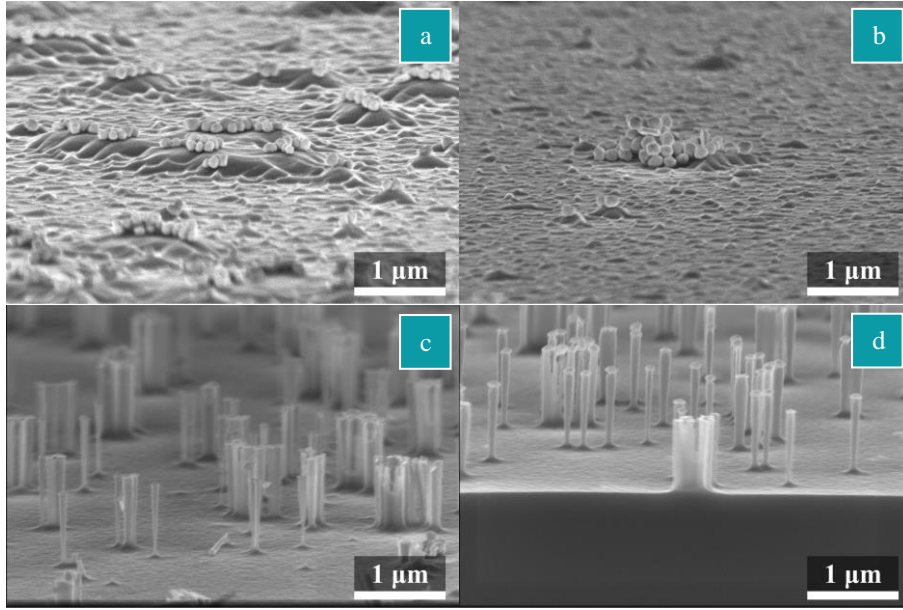
Fig. 3.1 – Si nanostructures produced by 40 s of etching tests in different-sized colloidal AuNPs masks. KOH etch in a) 100 nm and b) 140 nm AuNPs mask; ME-PEG in c) 100 nm and d) 140 nm AuNPs mask.

3.1.1.2   Thermal dewetting AuNPs mask optimization

A thermal dewetting procedure was optimized through several runs with varying z_0, T_0, and t_0 values to produce AuNPs with surface coverage and diameter that meet the requirements to exhibit the broadband AR effect, as well as the minimum diameter to perform the masking effect for the ME-PEG process. Briefly, the used scalable thermal dewetting procedure relies on a solid-state mechanism, as it occurs at a T_0 well below the metal melting temperature (1064 ℃ for Au[52]). Thermal dewetting promotes the appearance of voids throughout the film, which grow with time. As the film retracts, there is a point when the voids' edges come into proximity and merge, forming the NPs.[43,53] The first batch of AuNPs was fabricated from films with z_0 = 3, 5, 8, and 10 nm, and annealed with the T_0 and t_0 combinations listed in Table 3.1.

Table 3.1 – Thermal anneal T_0 and t_0 combinations studied for z_0 = 3, 5, 8, and 10 nm Au thin-films.

Run	T_0 (°C)	t_0 (min)
I	500	120
II		30
III	800	120
IV		30

For clarity, samples are designated by their z_0, thermal dewetting run, and the number of sputtering and anneal cycles as follows: z_0.run.#ofdewets. For instance, 3.III.2 refers to AuNPs fabricated from a 3 nm z_0 at 800 ℃ for 120 min by 2-cycle dewets.

As a representative, and to evaluate the 1-cycle dewet process, AuNPs SEM top-view images of samples 8.I.1, 8.II.1, 8.III.1, and 8.IV.1 are displayed in Fig. 3.2a)-d), respectively. It is visible by comparing Fig. 3.2a-b) showing AuNPs obtained at 500 ℃ and Fig. 3.2c-d) at 800 ℃, that annealing at higher T_0 drives more circular NPs, considering the same t_0. Additionally, a longer t_0 (Fig. 3.2c)-d)) also contributes positively to the NPs circularity. The obtained circularity trends for T_0 and t_0 are compatible with an enhanced Au surface diffusion, promoted by each parameter. Indeed, the aforementioned dependences were observed for the remaining z_0 Au films (Fig. A.1.1). Furthermore, the SEM analysis of all 1-cycle dewet samples (Fig. 3.2 and Fig. A.1.1) demonstrated that, as expected, with increasing z_0 the NPs diameter increases and the surface coverage decreases, as summarised in Fig. 3.2e)-f).[52]
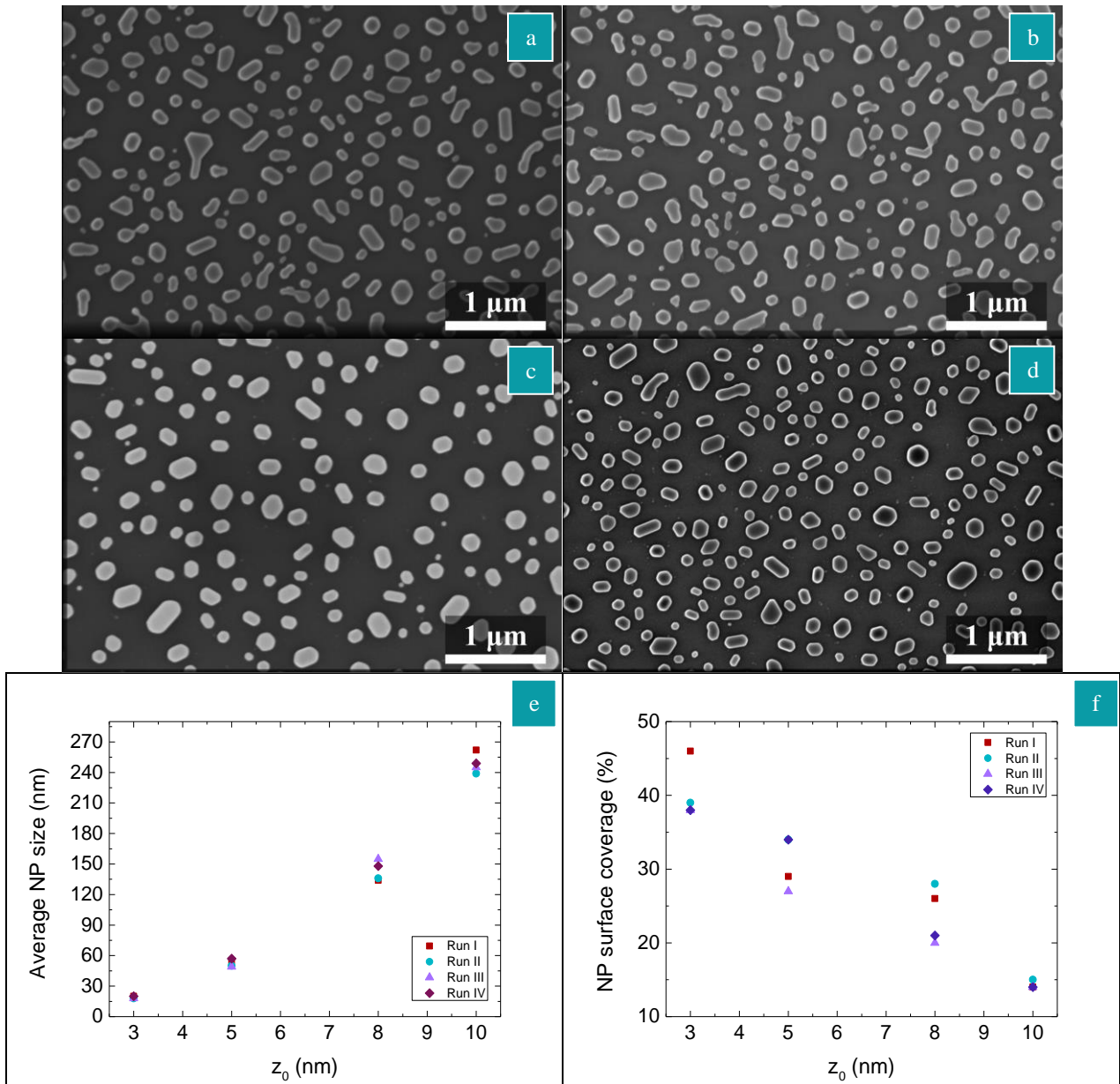
Fig. 3.2 – AuNPs resulting from 8 nm Au films by thermal 1-cycle dewet for each run: a) 8.I.1, b) 8.II.1, c) 8.III.1, and d) 8.IV.1; e) average NPs diameter and f) surface coverage plots taken from SEM top-view images through ImageJ.

Running in parallel to the dewetting process optimization, etching tests were continuously conducted. Thus, several not optimized AuNPs masks were used for etching tests. In fact, those tests provided key details for the establishment of the masks aiming properties, considering nanofabrication constraints. To use NPs with a minimum diameter value of around 100 nm, the smaller z_0 series (3 and 5 nm) were not considered (Fig. 3.2e)). As such, the 8.I.1 sample, with an average NPs diameter of 136 nm was etched with 40 s ME-PEG. The same masking effect observed for the ME-PEG discussed in Section 3.1.1.1 was reproduced (Fig. 3.3a)). Notwithstanding, relative total reflectance spectra presented in Fig. 3.3b) shows only a small AR effect in the 8.I.1 sample, when compared with a Bare Si substrate, due to the low AuNPs surface coverage of 26 % (Fig. 3.2f)). Given the average NPs inter-distance relation with z_0,[52] it is inferred that AuNPs fabricated from a smaller z_0, would produce a larger AR effect since the average NPs inter-distance would shift to dimensions smaller than the incident wavelength range. Consequently, to withstand the etch step and to obtain an effective improvement in the AR properties, the NPs produced from the 3 and 5 nm underwent a growth process adapted from [43].
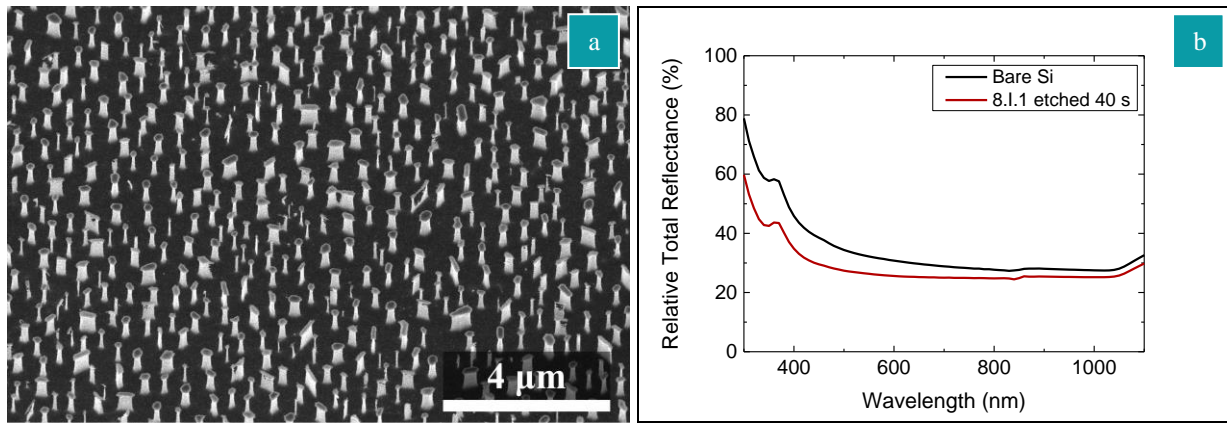
Fig. 3.3 – Etched 8.I.1 sample a) SEM top-view tilted at 30º image and b) UV-Vis relative total reflectance spectrum compared with a Bare Si sample.

In the 1-cycle dewet, as discussed above, the NPs are formed, and their diameter and average inter-distance are determined by z_0. Over the following cycles, the initial NPs act like a seed layer and grow radially. [43] Two growth dewetting cycles were run on the 3 and 5 nm z_0 samples, resulting in a total of 3-cycle dewetting. The SEM images in Fig. 3.4a)-c) depict the AuNPs formed from a film with $z_0 = 3$ nm over 1-, 2-, and 3-cycle dewet, respectively (3.I.1, 3.I.2, and 3.I.3), while in Fig. 3.4d)-f), the corresponding dewet cycles for a $z_0 = 5$ nm (5.I.1, 5.I.2, and 5.I.3) are shown. Radial growth of the NPs occurred over the 2- and 3-cycle, with an increase of surface coverage of 14 % for a 3 nm z_0 and 31 % for a 5 nm z_0, and growth of, on average, 16 nm and 24 nm of the initial average NP diameter, for $z_0 = 3$ and 5 nm, respectively.
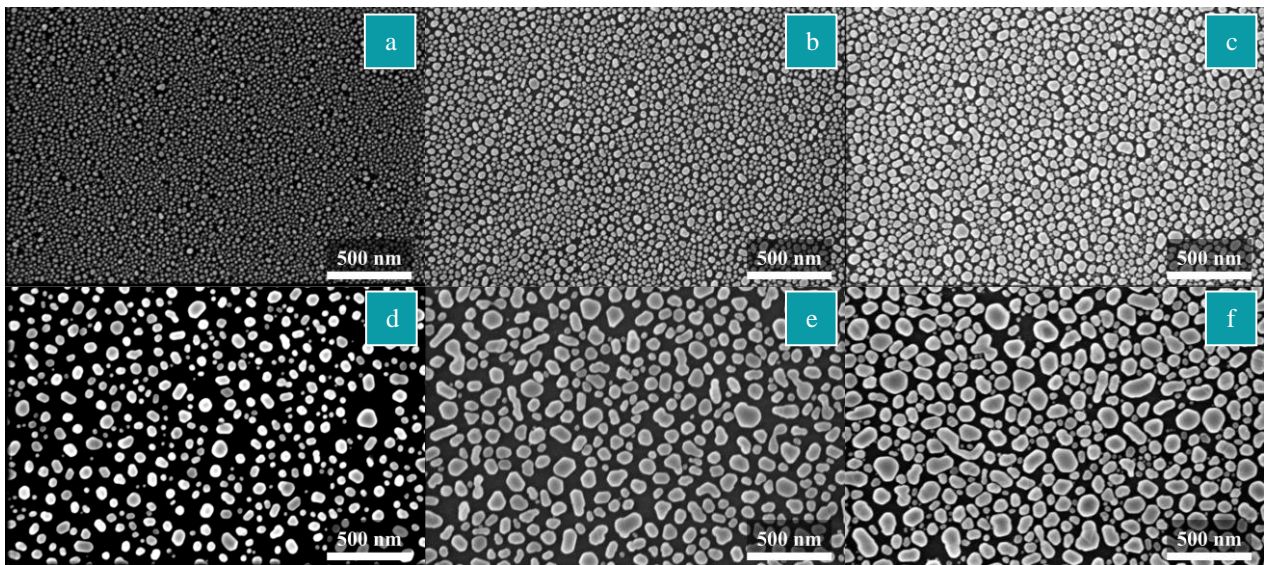
Fig. 3.4 – AuNPs resulting from $z_0 = 3$ and 5 nm and annealed at 500 °C for 120 min after 1-, 2- and 3-cycles dewet: samples a) 3. I.1, b) 3.I.2, c) 3.I.3, d) 5.I.1, e) 5.I.2, and f) 5.I.3.

Results revealed that even after 3 dewetting cycles, the largest AuNPs did not reach the 100 nm diameter threshold (Fig. A.1.2). Nonetheless, the 5.I.3 sample, with an average NPs diameter of 75 nm, was etched by ME-PEG to assess the masking effect (Fig. 3.5), and as expected most of the AuNPs were etched during the process and there was no formation of nanopillars with enough height.
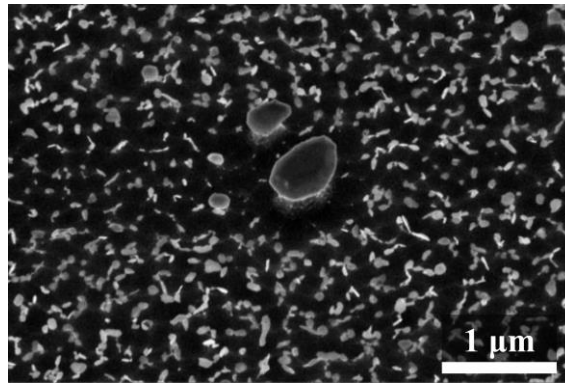
Fig. 3.5 – Sample 5.I.3 after ME-PEG etch of 40 s.

Considering that the NPs of 8.I.1 did not reach a surface coverage value that allowed for an efficient AR effect, and the 5.I.3 NPs were too small to act as the etch mask, it was concluded that the AuNPs that should meet both requirements are produced from a film with a z_0 between 5 and 8 nm. Thus, a second batch of AuNPs was fabricated from a 3-cycle dewet at 800 °C for 120 min (run III), with z_0 = 5.5, 6, 6.5, 7, and 7.5 nm. SEM top-view images of the final AuNPs are shown in Fig. 3.6a-c) for 5.5.III.3, 6.5.III.3, and 7.5.III.3, respectively. The results follow the same trend previously discussed, with an increase on the NPs diameter for thicker z_0.
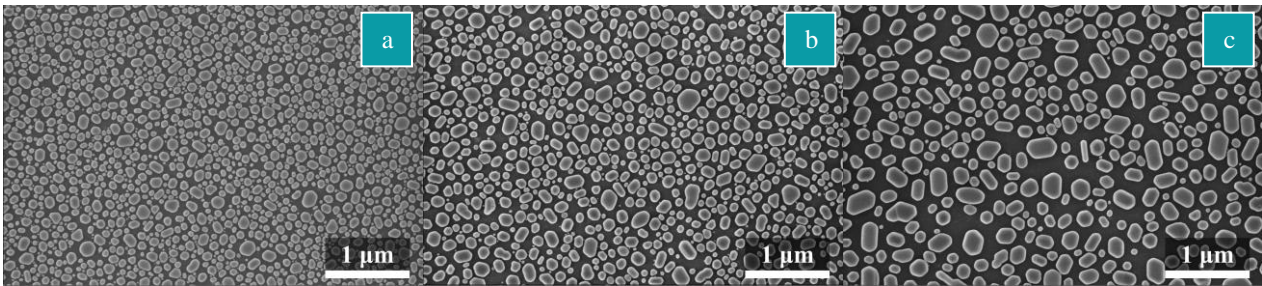

Fig. 3.6 – SEM top-view images of samples a) 5.5.III.3, b) 6.5.III.3, and c) 7.5.III.3

The evolution of the NPs diameters and samples surface coverage throughout the 3-cycle thermal annealing processes are summarised in Fig. 3.7a) and b), respectively. After the 3-cycle process, the samples displayed AuNPs with an average diameter between 83 and 156 nm, as well as surface coverage above ~50 %. These results show that all the produced 3-cycle dewet samples on the aforementioned batch (z_0 = 5.5, 6, 6.5, 7, and 7.5), present the NPs diameter and surface coverage values that may withstand the nanofabrication constrains, and allow for an efficient AR effect, since the NPs average inter-distance value is smaller than the wavelength of the incident light, as required for the textured surface to behave as a homogenized planar version.[19] Despite sample 5.5.III.3 NPs diameter being 83 nm, which is lower than the 100 nm limit established in the preliminary etch tests and considering the poor results of the 75 nm NPs from sample 5.I.3 (Fig. 3.5), it is noteworthy that the 100 nm colloidal NPs mask produced 790 nm nanopillars (Fig. 3.1c)). Thus, the 5.5.III.3 sample was considered as a ME master stamp. Indeed, the nano-scale broadband and omnidirectional AR architectures implemented in CIGS solar cell devices typically have a height below 400 nm. However, the AR enhancement is favoured by the height factor and pyramidal-like slope, as they allow for a progressive increase of the n value.[7] Herein, the aimed ME replica should meet a nanopillars architecture height of 550-600 nm. Furthermore, the ME stamp nanopillars' height does not need to meet the final ME structure height, as these parameters must be controlled on the replication process and tailored accordingly.
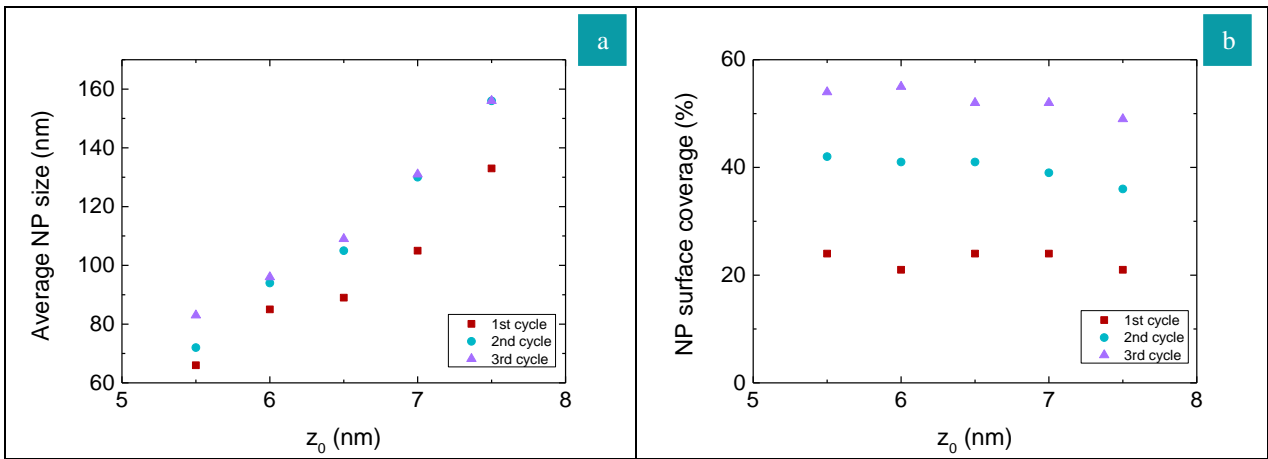
Fig. 3.7 – Dependence of the a) average NPs diameter and b) surface coverage on z_0 for the 3-cycle dewet taken from SEM top-view images through ImageJ.

3.1.1.3 ME-PEG etch rate calibration

Before proceeding with the NIL optimization, an etch rate calibration was performed on samples that underwent a 3-cycle dewet from z_0 series 5.5, 6.5, and 7.5 nm. For each series, several samples were etched by ME-PEG from 30 to 60 s, in 5 s increment. Fig. 3.8a)-c) show the progress of the etched nanopillars profile through cross-section SEM images for sample 7.5.III.3, after those underwent a ME-PEG of 30, 40, and 60 s, respectively. As expected from the results of the preliminary etching tests, nanopillars were etched underneath each NP. Herein, the nanopillars went from 25 nm height up to 606 nm. Moreover, as the etch time increases, the nanopillars acquire a sloped profile, which is beneficial for the AR properties, since it produces the n-grading effect.[7,19] Cross-section SEM images of the 40 s etched 5.5.III.3, 6.5.III.3, and 7.5.III.3 samples are shown in Fig. 3.8d)-f), respectively. The width value of the nanopillars follows the NPs diameters and for 40 s etch time pyramidal-like slopes are achieved for the 5.5.III.3 and 6.5.III.3 samples, but only appear for the 7.5 nm sample for etch times higher than 40 s. Thus, as the NP diameter increases, a higher etch time is needed to obtain a pyramidal-like slope. Nevertheless, the three samples after a 40 s etch present nanopillar profiles that allow proceeding in the ME stamp production.
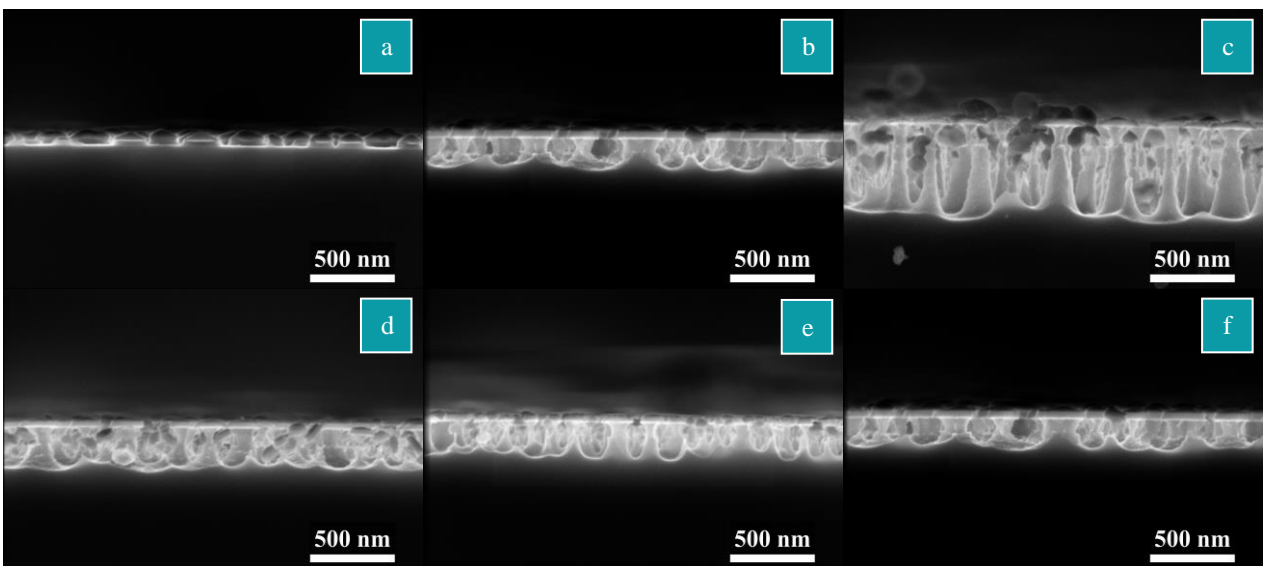

Fig. 3.8 – Nanopillars fabricated through ME-PEG from various z_0 series: 7.5.III.3 samples etched for a) 30, b) 40, and c) 60 s; d) 5.5.III.3, e) 6.5.III.3, and f) 7.5.III.3 etched for 40 s. Before aqua regia etch.

Fig. 3.9a) shows average etched depth dependence on the etch time. While at 30 s only under 30 nm of Si were etched, there is a steep etch depth increase by just a 5 s raise. As the etch time increases, differences between the samples etch rate values are more clearly shown. The 5.5.III.3 sample, presenting the smallest NPs and highest surface coverage, tends to a smaller etch rate than the other samples.

The ME stamps will be etched through 40 s leading to ~200 nm nanopillars height, then for the ME replicated pattern, an approximately 550-600 nm nanopillars height is aimed, to obtain an efficient ME effect,[7,20] which matches a 60 s etch time. Thus, to evaluate the optical properties of the ME stamp and to preview the ME replica ones, the relative total reflectance spectra of the samples etched for 40 and 60 s are shown in Fig. 3.9b). Independently of the etch time and z_0, there is a broadband spectrum decrease in comparison to the Bare Si. Nevertheless, the AR improvement is higher for the 550-600 nm nanopillars, which should be the ME replica height, with respect to the 200 nm ones. Hence, efficient ME schemes were successfully produced by a ME-PEG etch of a high surface coverage AuNPs mask developed by a 3-cycle thermal dewetting, for all z_0 samples.
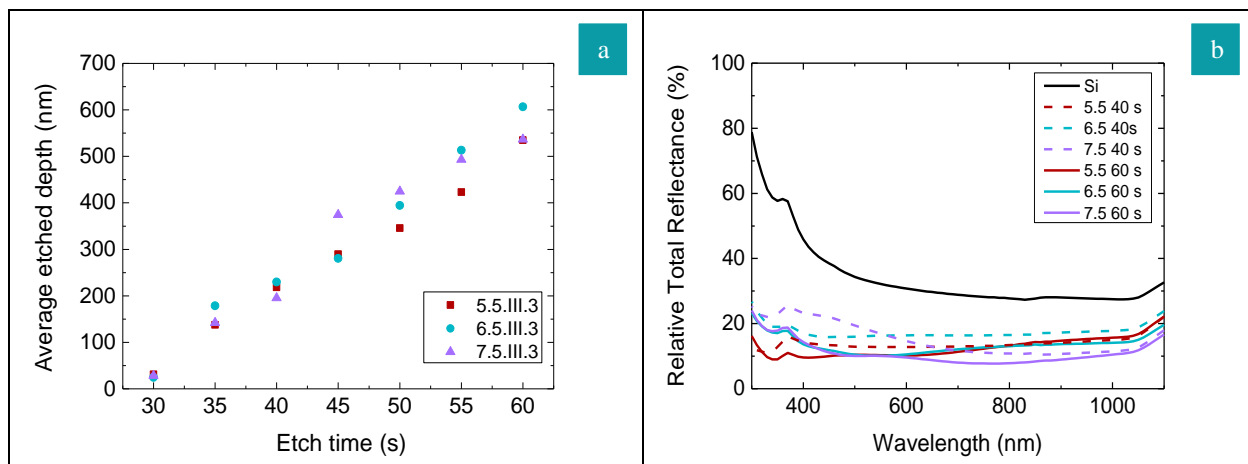
Fig. 3.9 – a) Etch rate assessment curves of samples 5.5.III.3, 6.5.III.3 and 7.5.III.3; and b) respective relative total reflectance spectra of samples etched for 40 and 60 s.

In addition to the broadband and omnidirectional AR, solar modules also benefit from a self-cleaning behaviour, as those are subject to different environment conditions. In this regard, WCA measurements were performed in a Bare Si sample and in the developed ME structure, sample 5.5.III.3 etched for 60 s, as shown in Fig. 3.10a)-c), respectively. The ME structure enabled an increase of the WCA from 30° (Bare Si) to 130°. Firstly, it is noteworthy that the surface changes from a hydrophilic to a hydrophobic behaviour through the integration of the ME scheme. In addition, the contact angle measured for the ME surface approaches a super hydrophobic behaviour, required for self-cleaning surfaces.
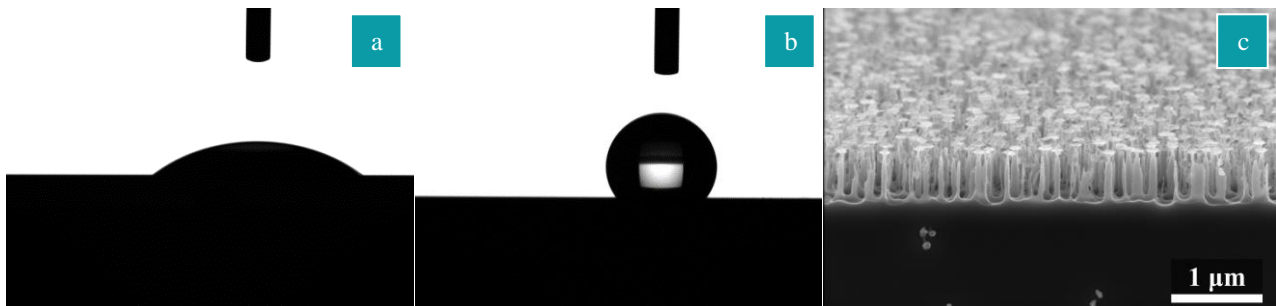
Fig. 3.10 - Water contact angle comparison between a) a Bare Si sample and b) sample 5.5.III.3 etched for 60 s; and c) SEM cross-section tilted at 10° of the 5.5.III.3 etched for 60 s.

Upon completing the etch calibration for the AuNPs masks, the stamps were fabricated, and will be referred to by the z_0 of their mask. As such, for the pattern transfer tests, 5.5, 6.5, and 7.5 nm stamps with a 200 nm nanopillar height were fabricated, and used in the tests interchangeably, as it was observed previously that their optical behaviour is mostly the same. As a representative ME stamp, the top-view and cross-section SEM images of a 7.5 nm ME stamp are presented in Fig. 3.11a)-b), respectively.
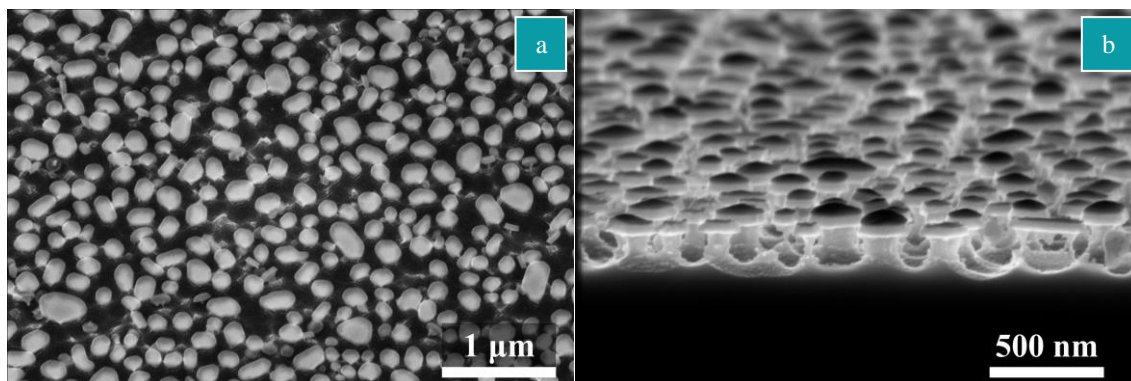

Fig. 3.11 – SEM a) top-view tilted at 30º and b) cross-section tilted at 10º images of a 7.5 nm ME stamp with a 200 nm average nanopillar height. Before aqua regia etch.

3.1.2 Pattern transfer

From the developed ME stamps, different tests were conducted to replicate the ME pattern. Two NIL approaches, running in parallel, were tested and optimized: the IPS-NIL and the OStamp fabrication, both followed by STU®-NIL. The process-flows and the obtained results are presented and discussed in regard to an aimed ME architecture with a final 550-600 nm nanopillars height.

3.1.2.1 IPS-NIL

To transfer the ME texture to a replica sample, IPS-NIL followed by STU®-NIL was first attempted. Three tests were run with varying combinations of the Teflon-like ASL with thicknesses a_1 and a_2 (see Fig. 2.3), as shown in Table 3.2. The test nomenclature refers to the ASL deposition time of the Teflon-like layer thickness.

Table 3.2 – Teflon-like ASL thickness values used in the IPS-NIL tests.

Test name	a_1 (nm)	a_2 (nm)
10s-10s	70	70
10s-1s	70	7
1s-1s	7	7

In Fig. 3.12, from a)-d) it is shown through SEM images, of the 7.5 nm ME stamp, the patterned IPS®, and then the patterned resist, the progress over the replication process, while the results for the 5.5 and 6.5 nm ME are shown in Fig. A.2.1 and Fig. A.2.2, respectively. Comparing the 7.5 ME stamp in Fig. 3.12a) with the patterned IPS® in Fig. 3.12b), the reverse structure of the stamp is visible on the polymer surface. However, the top of the nanopillars appears larger. The resulting patterned resist (Fig. 3.12c)-d)) presents texturization and a few nanostructures resembling the top-view of the stamp nanopillars, yet they are sparser and fewer. In Fig. 3.12d) the cross-section view of the patterned resist confirms the presence of tapered structures. Following these results, a 7.5 nm ME stamp with the 70 nm Teflon-like ASL-1 coat (a_1) was analysed in SEM (Fig. A.2.3), showing that the ASL fills the inter-pillar spacing. These results indicate that the ASL may be too thick for the ME structure and, as a result, affect the transferred pattern. As such, the 10s-1s and 1s-1s tests were carried out, motivated by positive results of an ASL thickness optimization study done in parallel.[54]
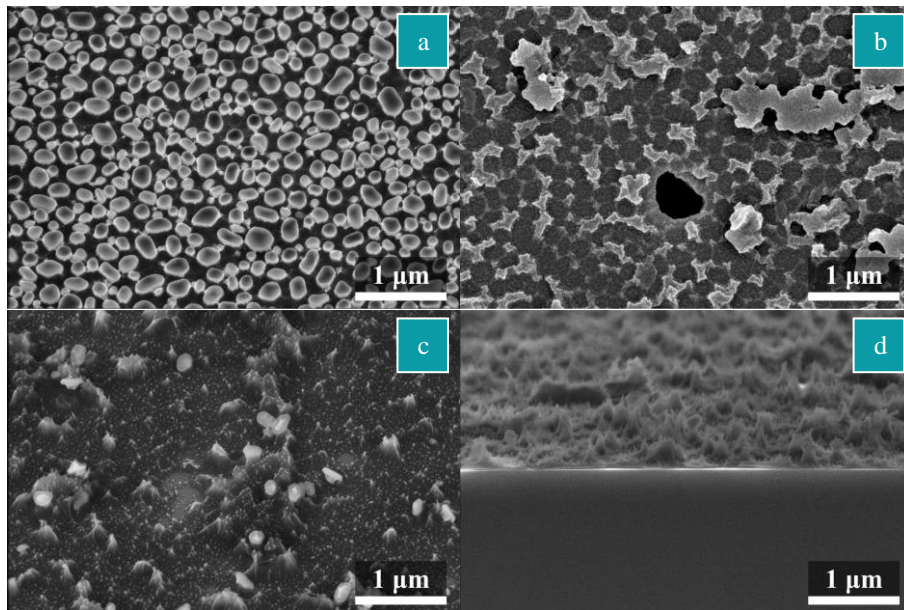
Fig. 3.12 – SEM images of the 7.5 nm a) ME stamp tilted at 30º, b) patterned IPS®; patterned resist c) top-view tilted at 30º, and d) cross-section tilted at 10º for the 10s-10s test.

The main concern when using a thinner ASL is that demoulding can be compromised and can even result in the resist attaching to the IPS® surface and peeling-off the substrate.[40] The first demould, i.e., of the IPS® from the stamp, occurred normally for 10s-1s test. SEM images of the 5.5 nm ME stamp and the patterned resist for this test are depicted in Fig. 3.13a)-b). There is a clear presence of pillar-like structures in the patterned resist; however, with a small or inexistent inter-distance between nanopillars. Once again, the a_1 10 s deposition used for the ASL-1 was too thick and covers the voids between the nanopillars. Nonetheless, the main goal of this intermediate test was to achieve a successful demoulding with a smaller a_2, which in the end posed no issue. Thus, a smaller a_1 was used in the 1s-1s test. For this test, the adhesion of the IPS structure increased, hampering the demoulding process. Clearly, the 7 nm polymer layer is too thin to confer the typical anti-sticking properties to the ME stamp, which should enable a smooth demoulding with no application of mechanical strength to separate the stack, to minimize pattern defect density.[40] SEM images of the 6.5 nm stamp and patterned resist for the 1s-1s test are shown in Fig. 3.13c)-d), respectively. Only a few nanopillars were imprinted in the resist surface, which can result from the deficient first demoulding. Nonetheless, the nanopillars were transferred to the resist layer with high fidelity. Overall, in order to successfully transfer the ME architecture through the IPS-NIL procedure, the ASL thickness should be between 7 and 70 nm to achieve an optimum balance between resolution and stamp demoulding.
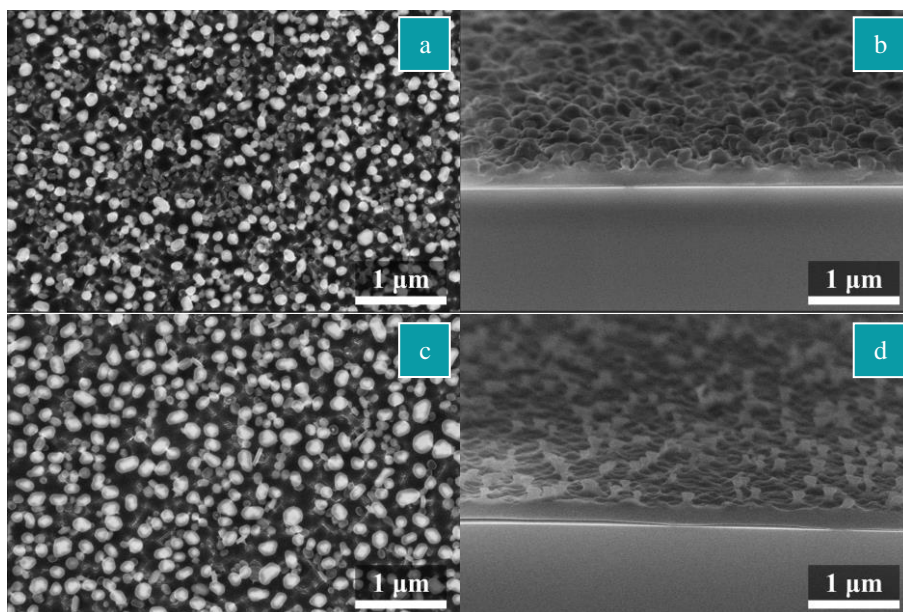
Fig. 3.13 – SEM images of the 5.5 nm a) top-view ME stamp b) cross-section tilted at 10º of patterned resist for the 10s-1s test; and the 6.5 nm c) top-view ME stamp d) cross-section tilted at 10º of patterned resist for the 1s-1s test.

3.1.2.2   OStamp fabrication

The OStamp patterning process was optimized iteratively through various tests, varying several parameters, such as the glass surface preparation, Ormoprime® 08 spin-coating rotation speed, hard-bake duration, demoulding temperature, and the ASL used on the stamp (Section 2.1.2.2).

On the first runs, the glass surface was cleaned in an acetone ultrasound bath and dehydrated in the vapour prime oven before the Ormoprime® 08 spin-coating, at 2000 rpm. With this procedure, demoulding was carried out in two different periods – once the stack reached 130 °C and after a 30 min bake at this temperature. Both tests resulted in failure, because upon detaching the OStamp from the ME stamp, a large portion of cured Ormostamp® remained attached to the ME stamp surface (Fig. 3.14a)). Consequently, only a few small areas of the polymer remained on the OStamp (Fig. 3.14b)). Notwithstanding, upon replication, Fig. 3.14c) shows a SEM cross-section image of the ME replica in the patterned resist, which confirms the presence of nanopillars in these small areas.
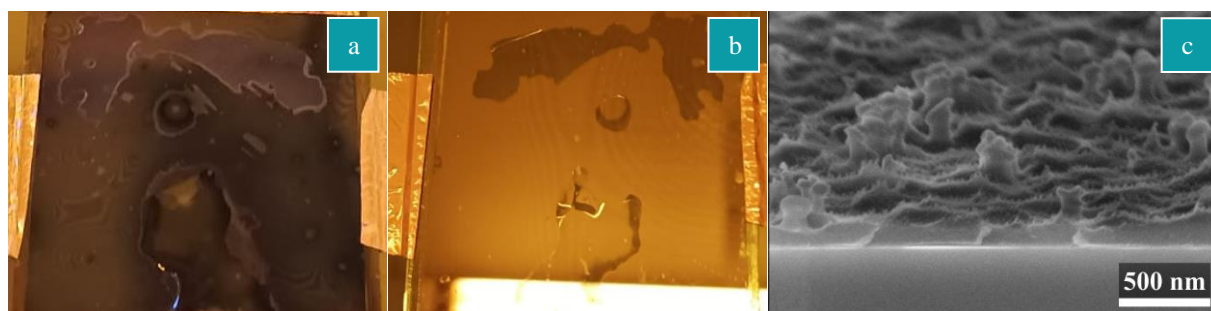

Fig. 3.14 – Detached Ormostamp® on the 5.5 nm a) ME stamp and b) OStamp; and c) cross-section tilted at 10º of the patterned resist.

The obtained poor demoulding in the previous test, indicated that the Ormostamp® adhesion to the glass substrate was defective. Therefore, the ensuing procedure, hereafter referred to as OST, was adjusted as follows: the glass surface received 15 min O_2 plasma treatment and the Ormoprime® 08 spin-coat was done at 4000 rpm. For the hard bake, at around 80 °C, the stack showed visual signs of natural detachment, and manual separation with a blade was successfully achieved shortly after, with no Ormostamp® detachment. This procedure was repeated once and produced the same outcome. In Fig. 3.15a-c), SEM images of the 5.5 nm ME

stamp (before and after ASL coat) and the resist after the imprint are presented, respectively. Despite the improved demoulding step, SEM analysis demonstrated the same issue as for the IPS® tests – the 70 nm Teflon-like ASL-1 fully covered most of the inter-pillar spacing (Fig. 3.15b)). Consequently, the replicated structure was changed, and, in the end, the ME texture was not transferred to the resist layer (Fig. 3.15c)).
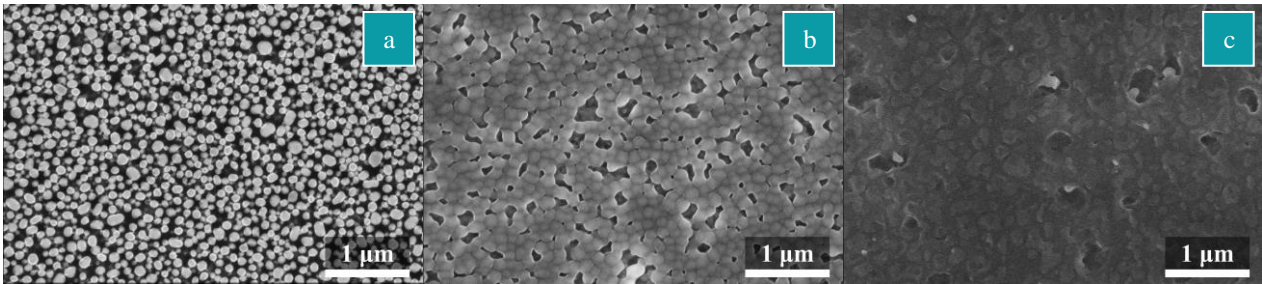

Fig. 3.15 – SEM images of the 5.5 nm ME stamp used to test OST a) before and b) after 70 nm Teflon-like ASL-1 coat; c) top-view of patterned resist.

Despite the good demoulding, the poor ME replication motivated new adhesion tests with alternative ASLs, aiming to reduce their thickness as much as possible. For the first approach a SAM of F13-TCS deposited by vapour-phase for 1h, was used. While demoulding was attempted at either upon reaching 130 °C or after baking for 30 min at that temperature, all runs resulted in Ormostamp® detachment. Alternatively, the stamp was coated with 5 nm of SiO_2 and 28 nm of the Teflon-like ASL, aiming to facilitate the demoulding in compensation for a thinner ASL-1[40] This thickness was chosen based on the analysis of the effect on the original pattern upon the deposition of varying thicknesses of the Teflon-like ASL layer (Fig. A.2.4). Demoulding was done upon reaching 130 °C. Fig. 3.16a) presents the SEM image of the 7.5 nm ME stamp with 5 nm SiO_2 + 28 nm of Teflon-like ASL-1 coat, while in Fig. 3.16b)-c) the ME replica textured surface after undergoing ME-PEG for 60 s, prior to removing the RR is shown. Clearly, additional optimization of the RR removal is needed, as it can be observed in Fig. 3.16c) that some areas remained unexposed and, consequently, the underlying Si was not etched. Regardless, two points must be considered: the patterned resist displayed the typical ME nanopillars, and texturization of the Si was achieved. Thus, with longer O_2 strip and ME-PEG process times, the Si texturization might meet the ME stamp structure. Nonetheless, due to time and logistic constraints, no further tests were run for this Section.
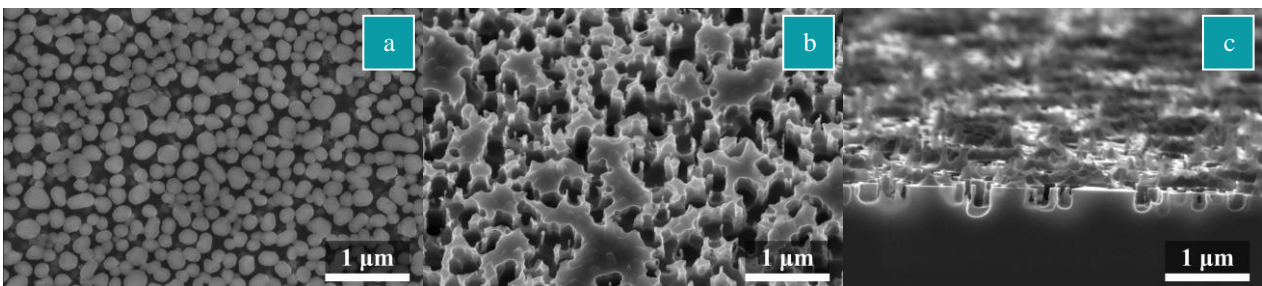

Fig. 3.16 – SEM images of the 7.5 nm a) ME stamp coated with 5 nm SiO_2 + 28 nm of Teflon-like ASL; of the ME replica etch for 60 s, b) top-view tilted at 30° and c) cross-section tilted at 10º.

Overall, employing NIL using an OStamp as the intermediate stamp to replicate the ME structure posed several challenges. Firstly, the sub-wavelength inter-pillar distance value raised a major limitation on the optimum ASL thickness a_1 value. On one hand, the 70 nm Teflon-like ASL-1 coat was too thick and changed the pattern transferred to the resist. On the other hand, no success was found when switching to F13-TCS, which is the ASL suggested by the supplier. Perchance, different results might be obtained if the silane deposition is carried out for a longer period.[44] Notwithstanding, with the adjustments of the parameters that define the OST procedure, the process was carried out with no Ormostamp® detachment. Notably, with the 70 nm

Teflon-like ASL-1, the release step occurred on its own before reaching a 130 °C temperature and showed good reproducibility, indicating that this procedure can be applied in the replication of structures where the spacing of the nanostructures is large enough to be compatible with this a_1 value. Moreover, the optimized SiO_2 + Teflon-like ASL-1 also allowed for a successful demoulding. However, the pattern transfer fidelity may still be optimized as the final surface contained areas where Si remained unetched. Nevertheless, these limitations arise from the short inter-pillar distance of the fabricated ME stamp. As a nanofabrication balance, a ME with a longer inter-distance could minimize the aforementioned challenges, as long as the AR requirements are still met. For future improvements, it is suggested that a mask with AuNPs fabricated from 2-cycle dewets is used to produce the ME stamp, as despite presenting a lower surface coverage, it still provides the small inter-pillar distance required for omnidirectional and broadband AR. For this, a different etch rate assessment would be necessary. Furthermore, additional adjustments to the subsequent steps, the RR O_2 strip, and the ME-PEG etch are required to reach the end goal of replicating the ME.

3.2 Photonic Crystals for rear light management

3.2.1 FDTD simulations

The FDTD method allows for the calculation of the total light absorbed by a given cell layer and, subsequently, the photogenerated current. First, the power absorbed per unit of volume, P_{ABS}, is determined by:

$$P_{ABS} = \frac{1}{2} \omega \, \varepsilon'' |E(\lambda)|^2 \tag{1}$$

where λ is the wavelength, ω is the angular frequency, ε'' is the imaginary part of the dielectric permittivity, and $|E|^2$ is the electric field intensity. Following, the total light absorbance, $ABS(\lambda)$, is calculated by the integration of the normalized P_{ABS} by the source power, p_{ABS}, over a specific volume V:

$$ABS(\lambda) = \int p_{ABS}(\lambda, V) dV \tag{2}$$

Following, the J_{SC} can be determined as follows:

$$J_{SC} = q \int \frac{\lambda}{hc} ABS(\lambda) I_{AM1.5}(\lambda) d\lambda \tag{3}$$

where q is the elementary charge, h is the Planck constant, c is the speed of light in vacuum, and $I_{AM1.5}(\lambda)$ is the AM1.5 solar irradiance spectrum. Herein, the internal quantum efficiency (IQE) is assumed to be 1, implying that every absorbed photon generates one electron-hole pair that is collected. As such, only the cell's optical performance is considered, and J_{SC} will be the maximum current density value.[11] Thus, in the subsequent optimization, J_{SC} is considered the figure of merit.

Parameter sweeps were run for the two studied photonic crystal architectures to determine their optimal dimensions, i.e., that produce the highest J_{SC} value, while considering nanofabrication constraints (a_{HS} (a_{PL}) $\geq$ 100 nm). Additionally, an ultrathin CIGS reference cell, without photonic crystals, was also simulated, to determine its J_{SC} that will be named J_{ref}. In Fig. 3.17a)-b), the ΔJ_{SC} variation, defined as $J_{SC} - J_{ref}$, is presented for both HS and PL, respectively. The incorporation of both photonic crystal architectures contributed to an optical gain observed through the ΔJ_{SC} value, with a more pronounced J_{SC} increase for geometries with smaller nearest neighbour distance and radius values. The HS array exhibited the highest ΔJ_{SC} value for r_{HS} = 250 nm and a_{HS} = 100 nm. On the other hand, the PL array performed best for r_{PL} = 225 nm, h_{PL} = 150 nm and

a_{PL} = 100 nm. Note that previous SiO₂ metasurfaces for light scattering in ultrathin CIGS solar cells, were also studied and similar architectural dimensions were obtained via optical simulations.[33,34]
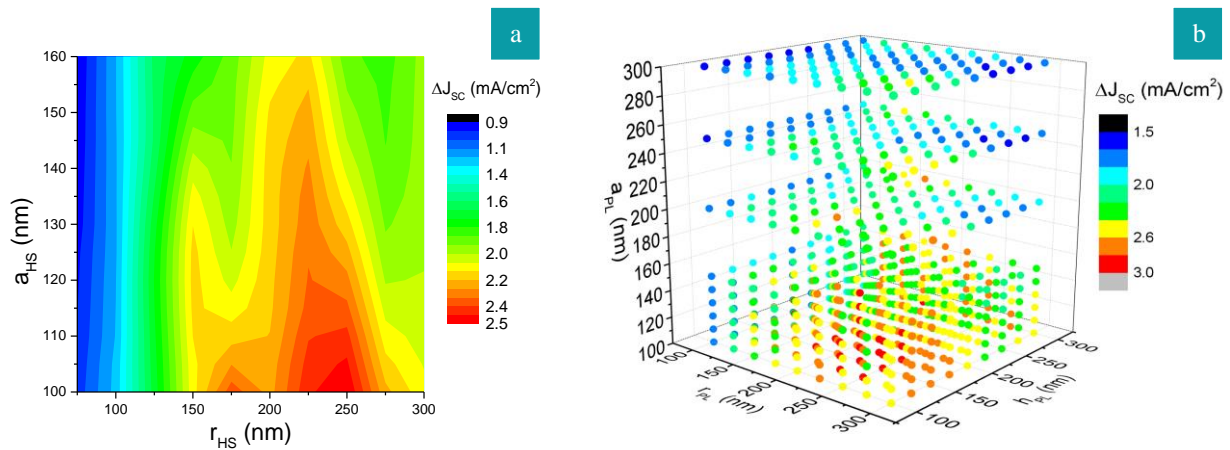

Fig. 3.17 – Resulting simulated ΔJ_{SC} parameter sweep maps as a function of a) r_{HS} and a_{HS} for the HS architecture and b) as a function of r_{PL}, h_{PL}, and a_{PL} for the PL array.

The simulated CIGS absorbance spectrum of a reference and the two solar cells with integrated optimized HS and PL, are presented in Fig. 3.18. There is a visible enhancement in the absorbance spectrum, for wavelength values higher than 600 nm, for the two solar cells architecture with photonic crystals over the reference one. An important remark lies in the spectral region where the enhancement occurs, which meets the wavelength range where ultrathin solar cells present their optical losses regarding the thin technology (Fig. 1.2). Nonetheless, interference fringes are observed in all spectra as a result of interaction between incident and rear reflected light. A similar J_{SC} value was obtained with 28.8 and 28.9 mA/cm² for the HS and PL, respectively. The obtained improvements are attributed to scattering resonant effects from the dielectric periodic array. From an optical gain point of view, both architectures' performance is similar. However, when other solar cell figures of merit are taken into account, an important consideration is the height value of the nanostructure, as high height values will be detrimental for the open circuit voltage and fill factor[42]. Thus, the PL with its 150 nm height could contribute for a better overall solar cell performance.
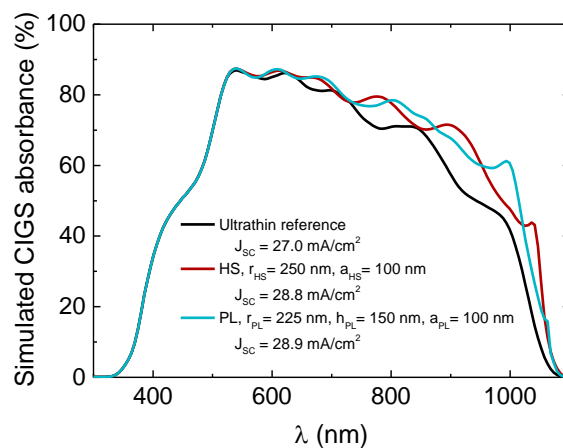

Fig. 3.18 – Simulated CIGS absorbance spectrum for an ultrathin CIGS conventional solar cell, and with integrated optimized HS and PL architectures.

3.2.2   Hemisphere array fabrication

Following the procedure presented in Section 2.2.2 the goal was to produce a HS array. Thus, a proof-of-concept for the nanofabrication of a SiO_2 HS photonic crystals is presented. For that purpose, a process-flow based on a previously fabricated point contact stamp in hexagonal array configuration was implemented. In the following Sections, the tests and established processes are presented and discussed.

3.2.2.1   Isotropic etch optimization

From the HS process-flow in Fig. 2.5, a point contact stamp with 200 nm hole radius and 2 µm pitch was used to pattern a mr-NIL resist layer on top of a Si sample. Then, an isotropic RIE process using SF_6 as precursor gas was optimized varying the parameters according to Table 3.3, with the goal of obtaining hemispheric cavities and a low etch rate for precise size control. All five samples were etched for 20 s, under 2.5 mTorr pressure, at 20 °C. Hole radius values were measured through SEM images with ImageJ software and isotropy was estimated through the ratio between the hole radius (r) and the etched depth (Z). Considering all samples were etched for the same time interval, there is a clear tendency for a lower etch rate with decreasing SF_6 flow. On the other hand, decreasing the HF coil power leads to a worse isotropy. Sample Iso_3 was considered the best result, as it exhibited an isotropy of 1.00 and the smallest resulting dimensions, hence, lowest etch rate. Thus, this sample was selected to move forward with the cavity inversion tests.

Table 3.3 – Dimension of the 20 s etched cavities according to the etch parameters variation and respective isotropy.

Sample	SF_6 (sscm)	HF Coil (W)	Avg r (nm)	Avg Z (nm)	Isotropy
Iso_0	100	1000	546	510	1.06
Iso_1	75	1000	431	458	0.95
Iso_2	50	1000	411	456	0.90
Iso_3	25	1000	363	362	1.00
Iso_4	100	750	445	550	0.81
Iso_5	100	500	489	334	1.47

In Fig. 3.19a)-b), the top-view and cross-section SEM images of sample Iso_3 are presented, respectively. Despite the ideal isotropy, the resulting dimensions of r = 363 nm and Z = 362 nm are much larger than the intended 250 nm for both. Here, two points must be considered: firstly, preliminary etch tests determined that the isotropic etch cannot be performed for less than 20 s, since the plasma is still unstable, irregular cavities are produced (Fig. A.3.1). Thus, the 20 s etch time determines the lower threshold for the stamp's dimensions. Secondly, the stamp used to obtain the holes array for these tests did not present the suitable dimensions to attain the optimized HS geometry – while the simulated HS has a r_{HS} of 250 nm with a 600 nm pitch in a square configuration, the initial stamp presented a hole radius of 200 nm and a 2 µm pitch in a hexagonal configuration. To achieve the optimized dimensions, a different stamp with a smaller pitch and hole radius must be fabricated through EBL in a square arrangement, and it is expected that smaller holes would facilitate the fabrication of the aimed hemispheric cavities. In this regard, as isotropy and lower etch rate for process control were successfully attained, the Iso_3 master stamp was implanted in a process-flow to move forward to develop a HS proof-of-concept architecture.
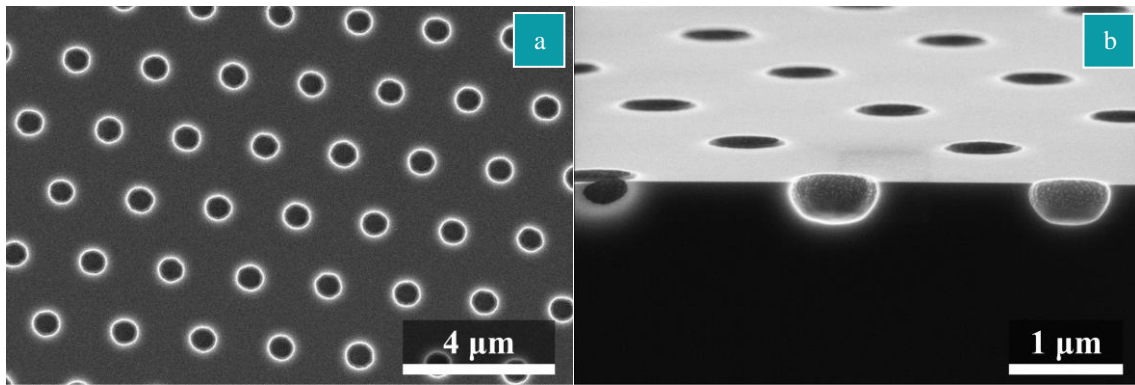
Fig. 3.19 – SEM a) top-view and b) cross-section tilted at 10º images of the hemispheric cavities fabricated on the Iso_3 master stamp.

3.2.2.2 Hemispheric cavity inversion test

The inversion test aimed to imprint on resist the reverse structure of the cavities – the HS. The employed OST method proved to be very effective on this structure, as upon the OStamp fabrication, the stack separated on its own upon reaching 80 °C, requiring little to no pressure to demould it. Ultimately, for architectures with dimensions that are not affected by the 70 nm Teflon-like ASL-1, this procedure has a very high success rate. The SEM top-view and cross-section images of the mr-NIL 6001 resist surface patterned with the HS OStamp is displayed in Fig. 3.20a)-b), showing a very uniform array of HS indicating the success of the inversion test.
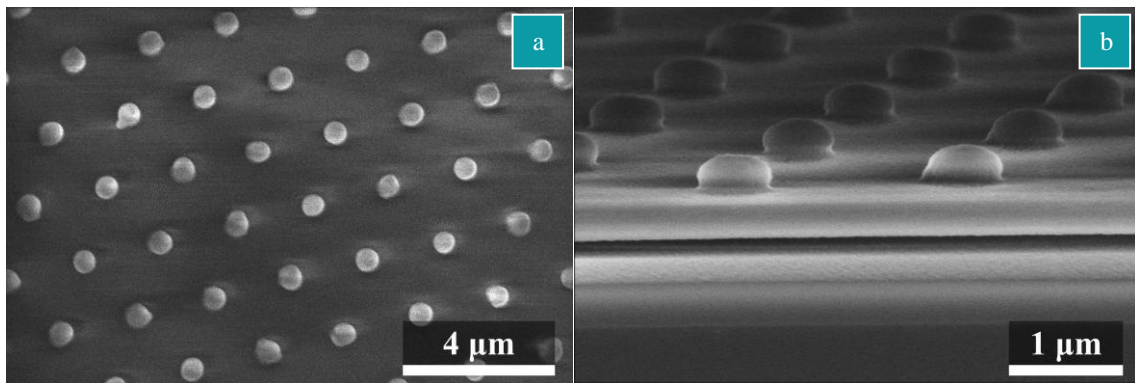
Fig. 3.20 – SEM a) top-view and b) cross-section tilted at 10º images of the HS array on resist after the inversion NIL procedure.

3.2.2.3 Anisotropic etch for SiO$_2$ hemispheres formation

In the previous Section, 3D structures were successfully imprinted on the resist surface. The next step aims to enable a reliable pattern transfer from the resist to the SiO$_2$. Several in-house etch procedures were tested and their respective selectivity (S), which is defined as the ratio between the etch rates of the SiO$_2$ (r_{Ox}) and resist (r_R), i.e. $S = r_{Ox}/r_R$, was assessed through measurements of the resist and SiO$_2$ layers thickness values before and after the etch procedure. The resulting S values of the tested etches considering two resist layers – mr-NIL 6001 and TU7, are plotted in Fig. 3.21, and further details are presented in (Table A.3.2). Of the four tests, APS-1 and APS-2 etch were performed in SPTS APS, HS-PEG in SPTS Pegasus, and HS-ICP in SPTS ICP. APS-1 and APS-2 displayed the highest S, since they are commonly employed for anisotropic etch of SiO$_2$, therefore presenting a high r_{Ox}. Thus, both processes, were rendered unsuitable to proceed. In contrast, the S of HS-ICP was 1.85 for mr-NIL 6001 and 1.34 for TU7, whereas for HS-PEG it was ~0.50 for both resists. While S = 1 was not achieved with the tested processes, both HS-ICP and HS-PEG were selected to continue with the fabrication of the proof-of-concept samples and to study the effect of S>1 and S<1, as these

may also be suitable for light management applications. Furthermore, TU7 was the selected resist layer given that it presented the S closest to 1 for HS-ICP.
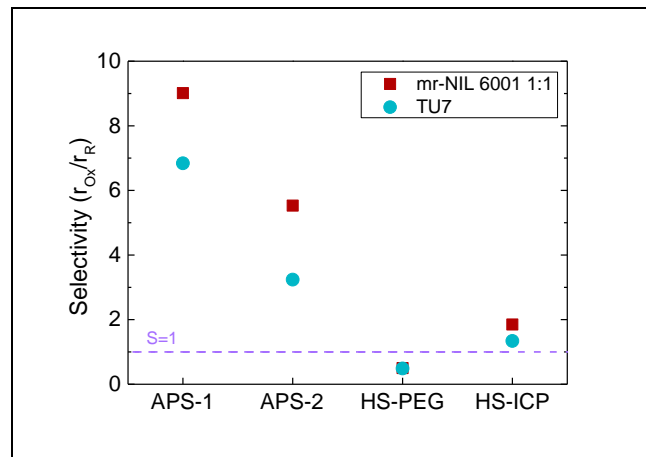

Fig. 3.21 – SiO$_2$/resist selectivity of the different tested etch procedures.

Over subsequent tests, several samples patterned with the method described in 2.2.2.2 were etched by either HS-ICP or HS-PEG, to assess each SiO$_2$ HS features' profile. All samples consisted in a Si substrate with a 400 nm SiO$_2$ film, coated by 450 nm of TU7. Representative SEM images of the resulting nanostructures via HS-ICP (S>1) and HS-PEG (S<1) are presented in Fig. 3.22a)-b), respectively. Using HS-ICP, conical structures were formed after etching for 7 min 30 s, and AFM measurements (Fig. A.3.3a)) confirmed that the cones in Fig. 3.22a) had an average base radius of 397 nm and average height of 345 nm. In contrast, HS-PEG etch for 12 min resulted in flat ellipsoids, with an average base radius of 467 nm and average height of 139 nm (Fig. A.3.3b)). From the two procedures, HS-ICP produced structures with an aspect ratio closer to 1 when compared to the HS-PEG ellipsoids. This is expected due to the contrasting etch rates: for HS-ICP, $r_{Ox}>r_R$, while for HS-PEG, r_{Ox} is half of r_R.
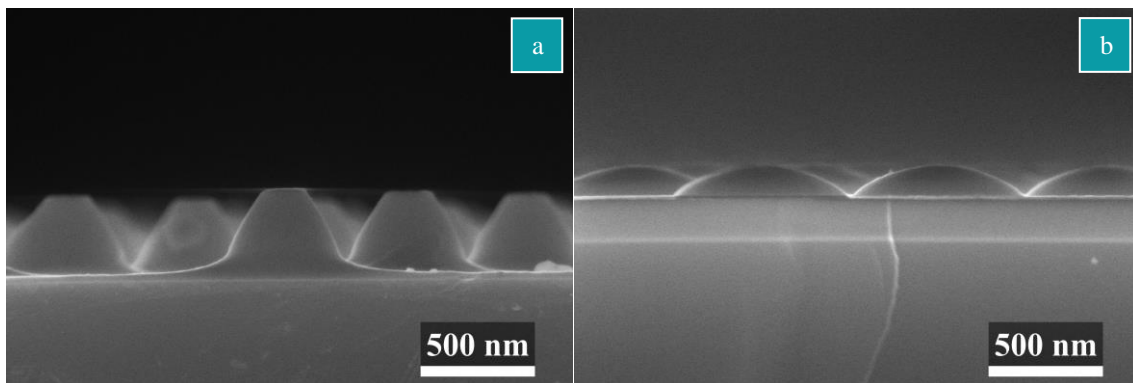
Fig. 3.22 – SEM cross-section image of nanostructures fabricated through a) HS-ICP etch for 7 min 30 s and b) HS-PEG etch for 12 min.

Ultimately, HS-ICP and HS-PEG etched distinct profiles, and either procedure can be employed to fabricate the HS architecture. To conclude, the final structure to be integrated in an ultrathin CIGS device can be made by first fabricating the HS cavities stamp with the optimized dimensions, i.e., with a square array arrangement and 250 nm radius cavities. In this regard, prior to the isotropic etch, the resist must be patterned through EBL with hole dimensions that allow the formation of cavities with the goal radius. Following, the resist on a SLG/Mo/SiO$_2$ stack would be patterned with the HS array and undergo the etch described in this Section. Given that HS-ICP presented the aspect-ratio closer to 1 compared to HS-PEG, it is recommended to select this procedure, as these nanostructures are closer to a HS configuration.

3.2.3 Pillar array fabrication

3.2.3.1 EBL master fabrication

The PL master fabrication started with an EBL process with a negative resist to produce SiO_2 pillars with a radius of 225 nm and a pitch of 550 nm. A preliminary dose calibration revealed that larger doses enabled the desired dimensions, however the resulting pillars exhibited rough edges (Fig. A.4.1). In contrast lower doses produced round pillars, as desired, albeit with smaller dimensions. Thus, only pillars with a radius up to around 100 nm could be produced using an 11565 $\mu C/cm^2$ dose, and SiO_2 deposition would be required to increase the pillars' diameter. In Fig. 3.23 the resulting pillars are presented before and after the deposition of 125 nm of SiO_2 for a) and b), respectively.
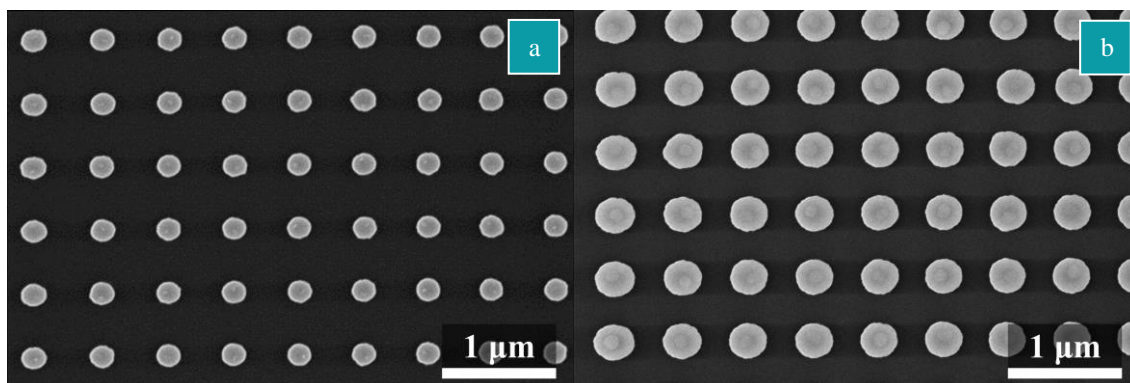
Fig. 3.23 – SEM top-view images of SiO_2 pillars a) after EBL and b) after 125 nm SiO_2 deposition.

Since the subsequent steps to fabricate the PL architecture required optimization, replicas of PL master were developed to prevent repeating the time-consuming EBL procedure. Alas, this step imposed its own challenges, as will be discussed next.

3.2.3.2 Pillar array stamp fabrication

Upon completing the PL master (Fig. 3.24a)), the structure had to be replicated through NIL. In Fig. 3.24, the resulting nanostructures fabricated over the initial NIL runs are presented. All SEM images depict the samples' surface after the resist removal in Plasma Asher. First, after the resist imprint, a 12 s O_2 strip was performed to remove the RR, followed by oxide etch in SPTS APS for 40 s (APS-1). As depicted in Fig. 3.24a), this procedure resulted in very short nanostructures, with no resemblance to pillars. Control SEM observations throughout the process-flow confirmed that after the NIL imprint the resist exhibited the PL structure, indicating that the fault lies in the subsequent etch stages of fabrication (Fig. A.4.2). As such, a first optimization was attempted, varying the O_2 strip and APS etch times, and the PL master was successfully replicated by combining 5 s O_2 strip with a 90 s APS etch (Fig. 3.24b)). Notwithstanding, it was later confirmed that the process is not reproducible, likely due to O_2 plasma instability associated with the short etch time. Alternatively, the RR removal and oxide etch steps were replaced by a single etch process, using 160 nm of resist instead. This was tested using APS-1 (Fig. 3.24c)) and the HS-ICP etch (Fig. 3.24d)). Using APS-1 as a single etch step failed to produce the desired structures. Most likely, the low resist etch rate combined with the prolonged 120 s time interval resulted in damage to the resist surface and, as a result, ineffective oxide etch. On the other hand, through HS-ICP short pillars were fabricated. Extending the process time resulted in spiked pillar tops (Fig. A.4.3), similarly to the results with HS-ICP structures (Fig. 3.22a)).
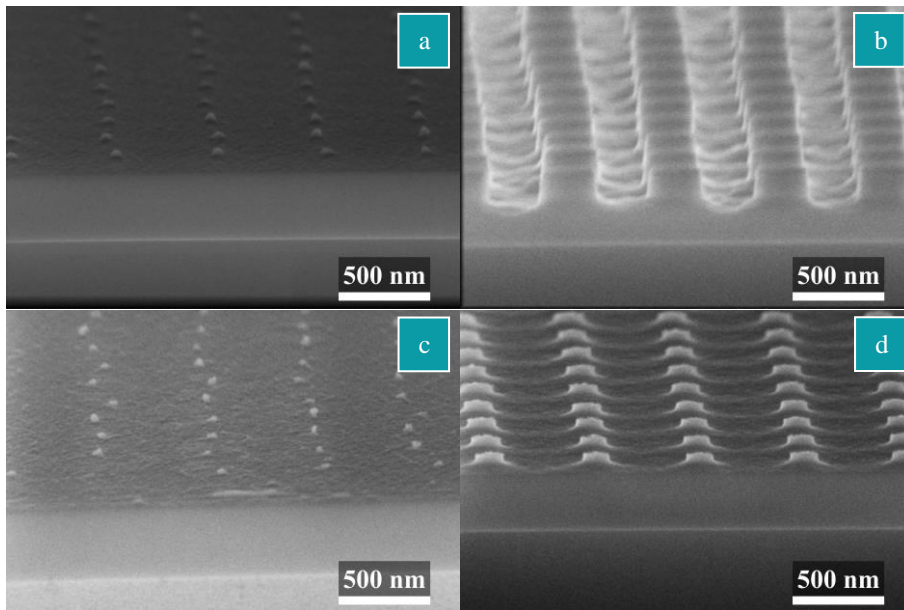
Fig. 3.24 – SEM cross-section images tilted at 10º of the resulting nanostructures from the tested etch combinations: a) 12 s O_2 strip + 40 s APS oxide etch, b) 5 s O_2 strip + 90 s APS, c) 120 s of APS etch, and d) 165 s of HS-ICP.

Following previous test results, the HS-ICP for 75 s was employed for the RR removal and the 400 nm SiO_2 was etched by APS-1 for 40 s, which proved successful. Subsequently, this procedure was repeated, using an 150 nm SiO_2 to fabricate the final PL master stamp. In Fig. 3.25a)-b) SEM top-view and cross-section of the PL master stamp, respectively, show that the procedure was a success, as the PLs are straight with a smooth surface, and all the oxide below was etched. Furthermore, after PECVD of 270 nm of SiO_2, r_{PL} increased to 220 nm (Fig. 3.25c), albeit a curvature in the SiO_2 film in the inter-pillar spacing (Fig. 3.25d)) is visible.
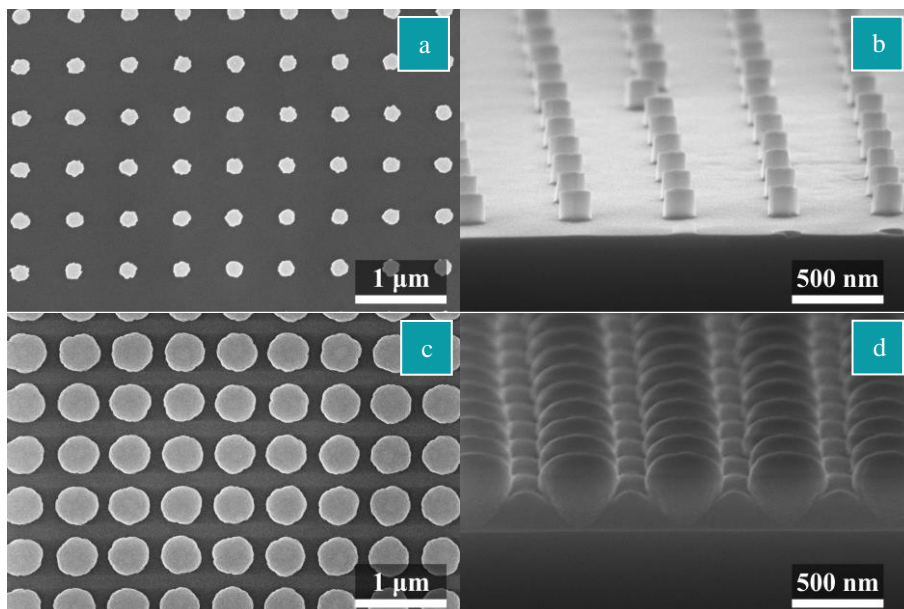
Fig. 3.25 – SEM images of the PL master stamp formed by RR removal with 75 s of HS-ICP and 40 s SiO_2 etch with APS-1: a) top-view and b) cross-section tilted at 10º, and after 270 nm of SiO_2 deposition: c) top-view and d) cross-section tilted at 10º.

At last, the fabrication of a PL square array NIL stamp was complete. The next step would be to replicate this new stamp with NIL and conduct additional ASL thickness optimization studies, given that, as demonstrated in Section 3.1.2, its thickness could hinder the pattern transfer of the ~100 nm spaced pillars. Lastly, to form the PL photonic crystal for light management in CIGS devices, the PL master stamp would be used to

pattern a 150 nm SiO$_2$ film on a SLG/Mo stack, which could then undergo the subsequent solar cell fabrication steps.

3.2.4 Photonic Crystals – optical behaviour

Fig. 3.26 shows the diffuse reflectance spectra of a Bare Si sample and the developed photonic crystal architectures. Clearly, the HS structure arrays lead to a broadband diffuse reflectance enhancement in comparison to the Bare Si sample, while the PL master stamp scheme shows a more localized increase for wavelength values lower than 600 nm. An important remark is that these measurements were performed in air, and when integrated in CIGS solar cells a redshift of the spectra peaks is expected. The metasurfaces' resonant modes are dependent on several factors such as, photonic crystal material, geometry, features' dimensions, pitch, dielectric medium, and substrate.[35,55] In all spectra, a peak at approximately 370 nm is observed. The Si total reflectance spectrum typically presents a peak in this region.[56] Thus, the peaks at 370 nm might be attributed to the Si substrate common to all samples. Nonetheless, the HS-ICP sample seems to present a resonant behaviour around the same region which might overlap with the Si peak. If a resonant mode is considered in the region near 370 nm for the HS-ICP sample, the peak broadening and intensity drop observed for the HS-PEG sample is well explained, since the HS-ICP sample presents a much higher aspect ratio than the HS-PEG one.[55] The redshift observed for the HS-PEG sample with respect to the HS-ICP, might be associated to the larger diameter value for the HS-PEG structures.[55]

The PL master stamp showed a well-defined peak around 510 nm and a sharp diffuse reflectance increase towards 300 nm. A well-defined peak allows for a precise control of the light-matter interaction over a specific spectral range, which in the case of study, i.e. ultrathin CIGS solar cells, will allow for an optimum scattering performance in the wavelength region with higher incomplete absorption losses. The overall diffuse reflectance results show that to obtain a well-defined resonant behaviour the photonic crystal structure dimensions must meet the optical simulation predicted values, which 1) validates the simulation's accuracy, and 2) demonstrate that despite not being perfect HS, the proof-of-concept structures presented can also show very well defined resonances as the dimensions move towards the ones predicted, since for larger structures a clear broadening and dampening was observed for the HS-PEG. Thus, the optical results show that three efficient scattering schemes concepts are presented in this Thesis.
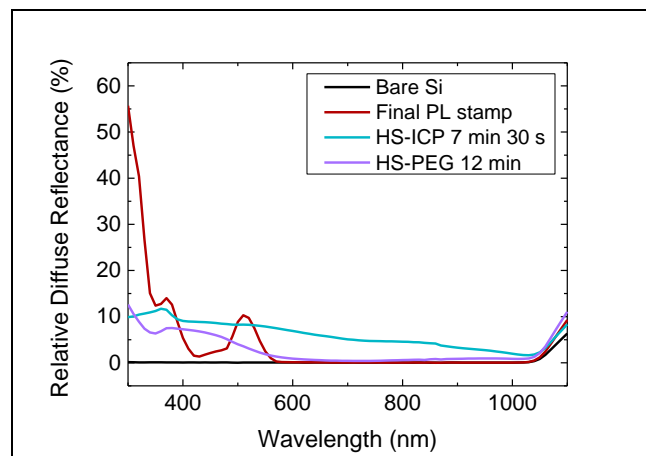
Fig. 3.26 – Relative diffuse reflectance spectra of the developed photonic crystal architectures: final PL stamp and HS schemes formed by HS-ICP and HS-PEG.

4.

CONCLUSIONS

The present work aimed to develop nanofabrication procedures for light management solutions compatible with CIGS technology, using mainly NIL as a high resolution and cost-effective nanofabrication process.

For front AR, a ME NIL stamp was developed. First, a AuNPs etch mask was tuned through a thermal dewetting method, demonstrating that longer anneal duration and higher temperature leads to rounder AuNPs, whereas a higher initial film thickness allows for larger and sparser AuNPs. Then, a RIE calibration for initial Au thin-films with 5.5, 6.5, and 7.5 nm, was optimized, and all samples showed a broadband AR. Additionally, the developed ME structures demonstrated a high WCA, close to a superhydrophobic behaviour, compatible with self-cleaning. Thus, an efficient broadband AR ME stamp was fabricated. Following, ME stamps were used for NIL studies with two intermediate stamps: IPS® and Ormostamp®. IPS-NIL was tested by implementing different combinations of a_1 and a_2 Teflon-like ASL thickness, and it was found that an a_1 of 70 nm hinders pattern transfer, as it covers the inter-pillar spacing. However, using $a_1 = 7$ nm compromises the first demould step. As for OStamp-NIL process-flow, several stages were adjusted to ensure an efficient stack release. The combination of parameters called OST, later employed for HS fabrication, displayed the best results, with a natural stack release at ~80 °C but being more suitable for larger inter-distance structures as it uses a 70 nm ASL. Alternative thinner ASLs were studied and a combination of a 5 nm SiO_2 with a 28 nm ASL displayed the best results. Nonetheless, for a ME replica, additional RR O_2 strip and ME-PEG etch optimization is required. The Ormostamp® detachment and ASL thickness limitation challenges arise from the closely packed ME structure. For future improvement, a ME stamp with a larger inter-distance is proposed. It is suggested to perform 2-cycle dewets for the AuNPs mask using a z_0 that fulfils a sufficiently high AuNPs diameter and surface coverage, to withstand the RIE and achieve a broadband AR, respectively. After a ME replication, the next step is to execute it on a glass surface, which will require optimized etch procedures.

For rear scattering enhancement, two SiO_2 photonic crystal architectures to integrate at the Mo/CIGS interface, HS and PL, were studied through optical simulations. Optimal dimensions of $r_{HS} = 250$ nm and $a_{HS} = 100$ nm for HS, and $r_{PL} = 225$ nm, $h_{PL} = 150$ nm, and $a_{PL} = 100$ nm for PL led to J_{SC} values of 28.8 and 28.9 mA/cm^2, respectively. For HS, a cavities Si stamp was fabricated with a tuned isotropic etch to pattern the resist through inversion NIL, followed by an anisotropic etch step to transfer the pattern to the underlying SiO_2 layer. Two etch procedures, HS-ICP (S = 1.34) and HS-PEG (S = 0.49) were employed with TU7 resist. HS-ICP formed cones with an aspect ratio close to 1, thus considered the best option. While the proof-of-concept samples did not display the optimized dimensions, these can be achieved by combining these optimized steps with a hole mask with a smaller radius, pitch, and in a square configuration, fabricated with EBL. For PL, a stamp with the optimized dimensions was fabricated through replication of an EBL master via NIL, RR strip with HS-ICP, etch in APS, and PECVD of SiO_2. Before transferring either HS or PL to a SLG/Mo stack for integration in CIGS, additional ASL thickness studies should be done due to their 100 nm spacing. The developed photonic crystal architectures enabled a significant diffuse reflectance increase with respect to a Bare Si sample, showing an efficient light scattering for all developed structures.

In summary, master stamps with sub-wavelength dimensions were successfully created. Different process-flow(s) were suggested and optimized. Throughout the presented work, several barriers and drawbacks were detected and overcome, while there are still stages to be improved. Notwithstanding, this Thesis places itself at the forefront for the integration of low-cost and efficient light management in the PV market.

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A.1 AuNPs obtained via thermal dewetting - optimization process

SEM images of the 1-cycle dewet AuNPs obtained through $z_0 = 3$, 5, and 10 nm for runs I, II, III, and IV (Table 3.1) are presented in Fig. A.1.1. AuNPs average diameter values and surface coverage for $z_0 = 3$ and 5 nm annealed at 500 °C for 120 min (run I) after 1-, 2- and 3-cycles dewet are plotted in Fig. A.1.2 a) and b), respectively.
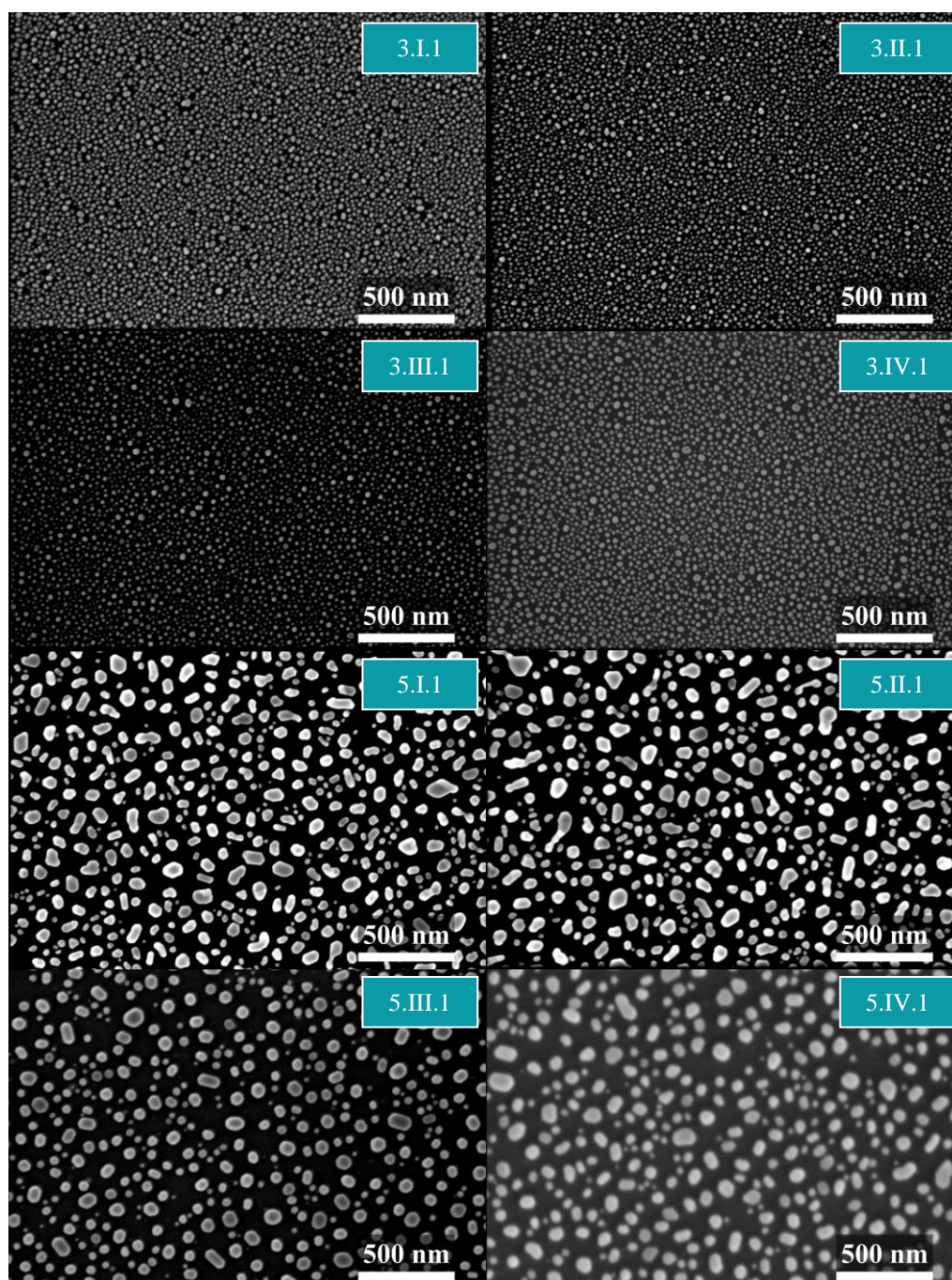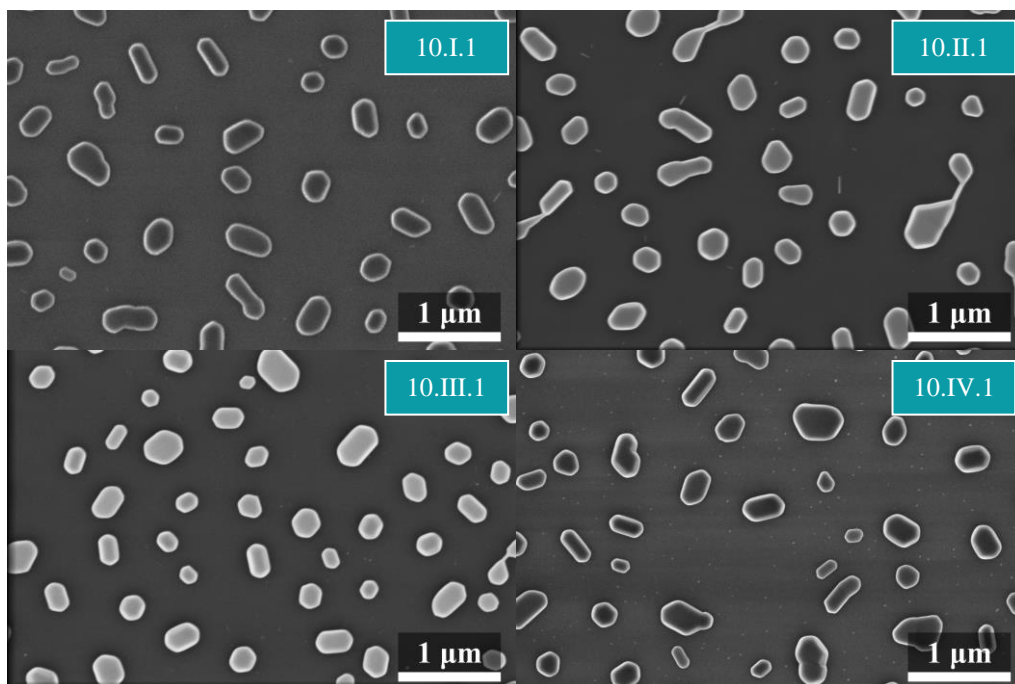
Fig. A.1.1 – SEM top-view images of AuNPs resulting from 3, 5, and 10 nm Au films by 1-cycle dewet for each run: 3.I.1, 3.II.1, 3.III.1, 3.IV.1, 5.I.1, 5.II.1, 5.III.1, 5.IV.1, 10.I.1, 10.II.1, 10.III.1, and 10.IV.1.
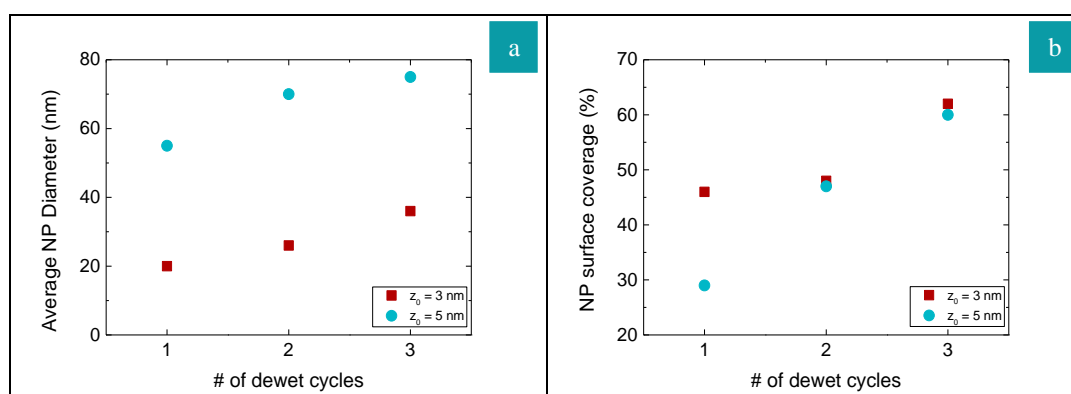
Fig. A.1.2 – Average NPs a) diameter and b) surface coverage plots – taken from SEM top-view images through ImageJ, for 3.I.1, 3.I.2, 3.I.3, 5.I.1, 5.I.2, and 5.I.3 samples.

A.2 ME Pattern transfer

In Fig. A.2.1 and Fig. A.2.2, from a)-d) it is shown through SEM images, of the ME stamps, the patterned IPS®, and then the patterned resist, the progress over the replication process, for the 5.5 and 6.5 nm AuNPs mask, respectively. Fig. A.2.3 shows a top-view SEM image of the 7.5 nm ME stamp with a Teflon-like ASL-1 with a 70 nm thickness for the IPS 10s-10s process. The Teflon-like ASL-1 thickness optimization for the Ostamp patterning process is shown in Fig. A.2.4 a)-d) for a_1 of 14, 28, 42 and 56 nm, respectively, which corresponds to 2, 4, 6, and 8 s of deposition.
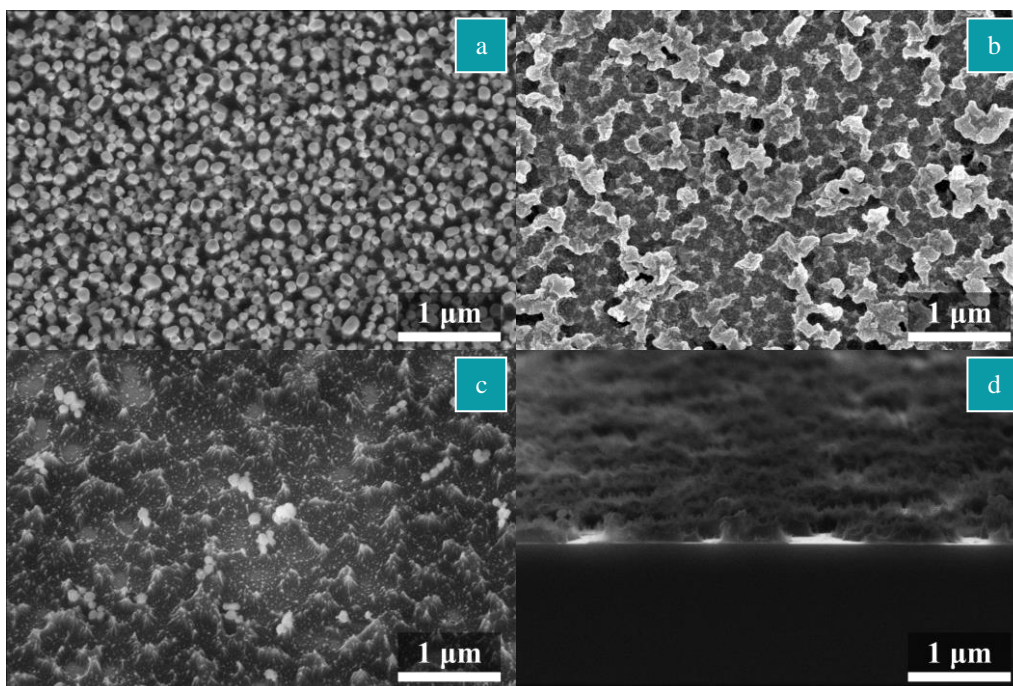
Fig. A.2.1 – SEM images of the 5.5 nm a) ME stamp tilted at 30º, b) patterned IPS®; pattern resist c) top-view tilted at 30º, and d) cross-section tilted at 10º for the 10s-10s test.
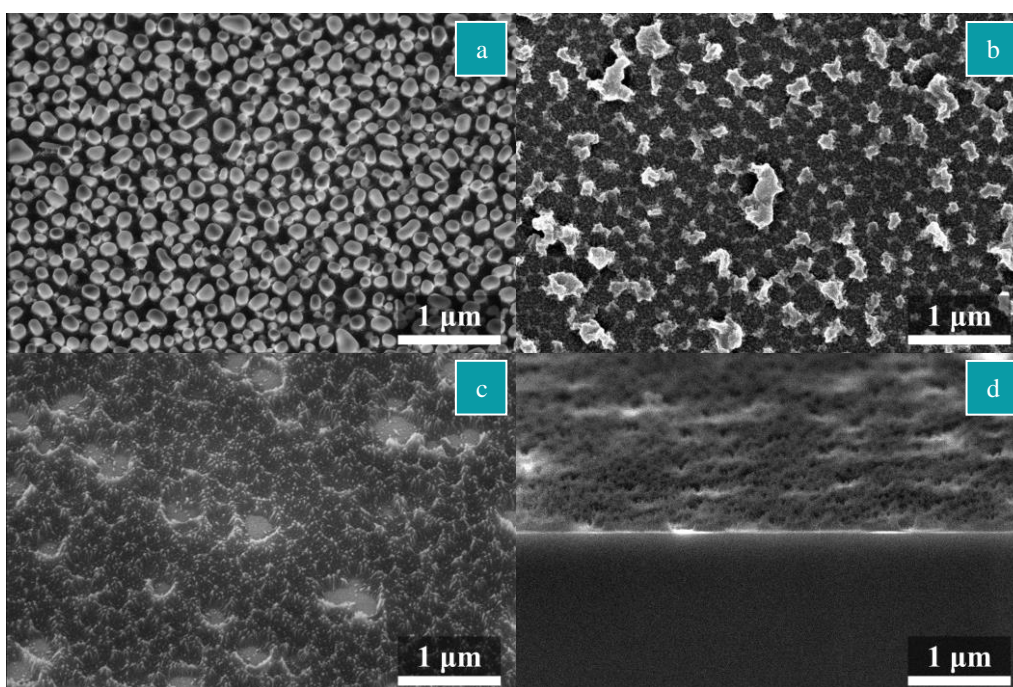
Fig. A.2.2 – SEM images of the 6.5 nm a) ME stamp tilted at 30º, b) patterned IPS®; pattern resist c) top-view tilted at 30º, and d) cross-section tilted at 10º for the 10s-10s test.
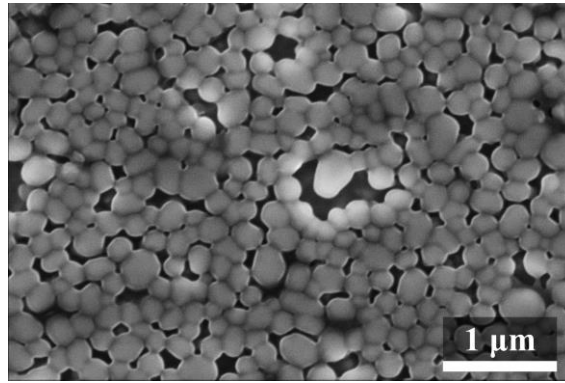
Fig. A.2.3 – SEM top-view image of the 7.5 nm ME stamp with 70 nm a_1 for the IPS 10s-10s test.
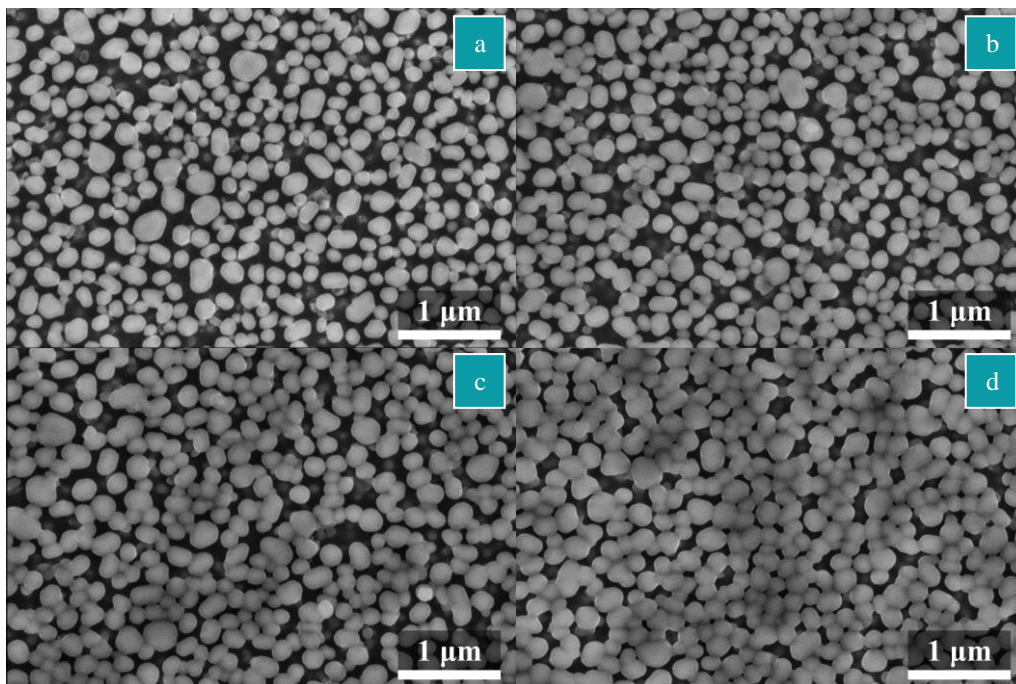
Fig. A.2.4 – SEM top-view images of the 7.5 nm ME stamps with a_1 of a) 14, b) 28, c) 42, and d) 56 nm.

A.3 HS array optimization

In Fig. A.3.1 the top-view and cross-section SEM images of a sample etched with a 9 s isotropic etch are presented, respectively. In Table A.3.2, the etch processes' parameters for the anisotropic HS etch optimization are presented. Fig. A.3.3 a)-b) shows AFM 3D profiles of the obtained HS metasurfaces for S>1 and S<1, respectively.
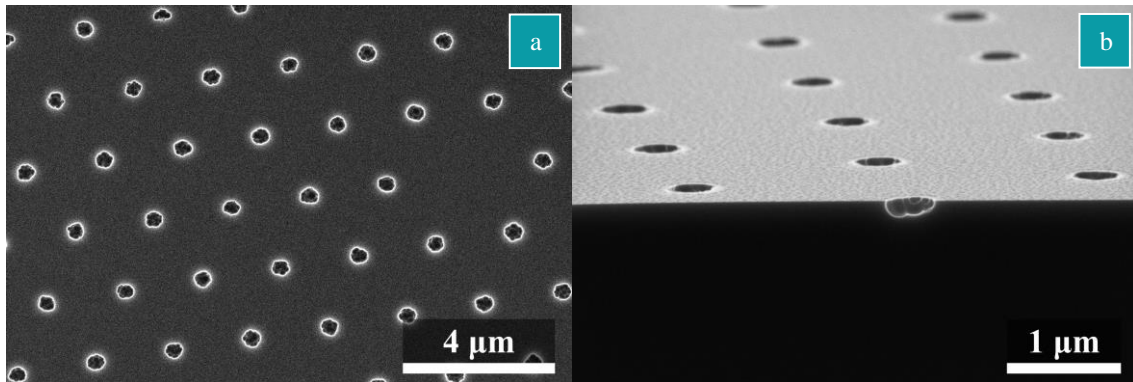
Fig. A.3.1 – SEM a) top-view and b) cross-section tilted at 10º images of the hemispheric cavities formed after a 9 s isotropic etch.

Table A.3.2 – Parameters of the tested etch procedures and respective Resist/SiO$_2$ selectivity.

Recipe	Pressure (mTorr)	Gases (sccm)				Power (W)		S (r_{Ox}/r_R)	
		SF$_6$	C$_4$F$_8$	H$_2$	CF$_4$	HF Coil	HF Platen	mr-NIL	TU7
HS-PEG	15	120	280			2000	45	0.50	0.49
APS-1	5		50	30		2000	700	9.01	6.84
APS-2	5		50			2000	700	5.53	3.24
HS-ICP	5				30	1300	50	1.85	1.34
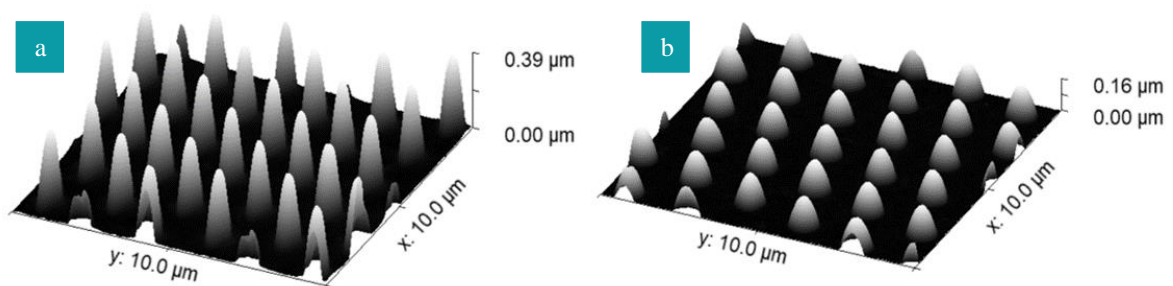
Fig. A.3.3 – AFM 3D profile of the HS metasurfaces for a) S>1 and b) S<1.

A.4 PL master stamp development

In Fig. A.4.1 a SEM image of the resulting PLs from an EBL exposure with a dose of 16009 µC/cm^2 is presented. Fig. A.4.2 shows a cross-section SEM image of the patterned resist with the PL array after the NIL process. In Fig. A.4.3, a cross-section SEM image of the resulting PL array from a HS-ICP etch during 195 s is shown.
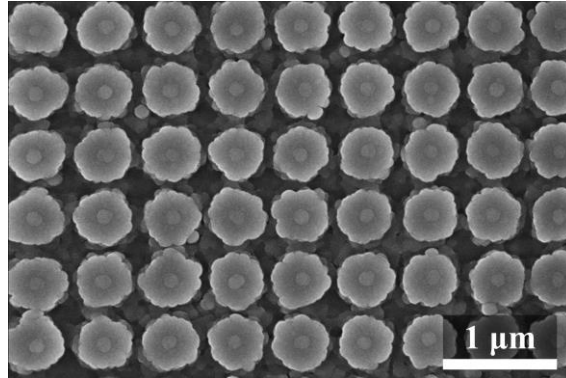
Fig. A.4.1 – SEM top-view images of SiO$_2$ pillars obtained through an EBL exposure with a dose of 16009 µC/cm^2.
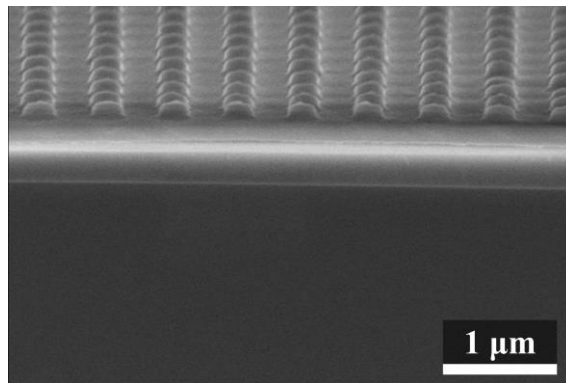
Fig. A.4.2 – SEM cross-section tilted at 10º image of the patterned resist layer after the NIL.
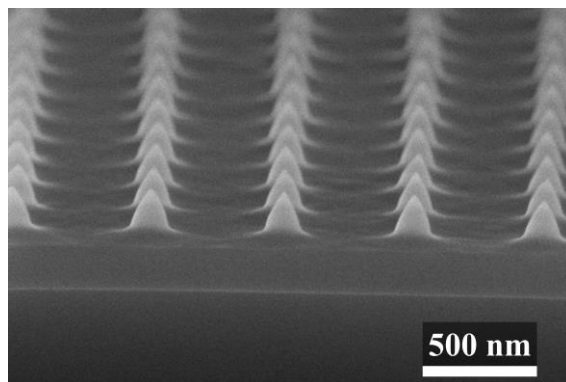
Fig. A.4.3 – SEM cross-section tilted at 10º image of the resulting nanostructures from a 195 s of HS-ICP etch.

A.5 Dissemination

Articles in Peer-reviewed Journal

T. S. Lopes, M. Monteiro, A. Violas, M. A. Curado, B. R. Ferreira, **R. F. Alexandre**, A. J. N. Oliveira, E. J. Ribeiro, J. P. Teixeira, G. Brammertz, P. A. Fernandes, B. Vermang, P. M. P. Salomé, "*C_4F_8 based anti-sticking layer for nanoimprint processes*" to be submitted to MicroEletronics Engineering.

Oral Presentation at Conferences and Workshops

A. J. N. Oliveira, J. P. Teixeira, T. S. Lopes, **R. F. Alexandre**, D. Ramos, J. R. S. Barbosa, K. Oliveira, P. A. Fernandes, P. M. P. Salomé, "*The Challenges and Developments in Light Management for CIGS Solar Cells*", E-MRS 2022 Spring Meeting, symposium K: Thin Film Chalcogenide Photovoltaic Materials

Poster Presentation at Conferences and Workshop
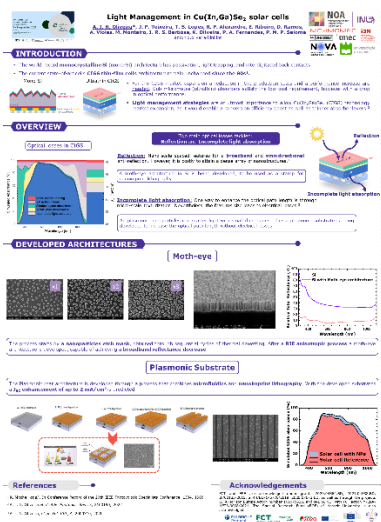
A. J. N. Oliveira, J. P. Teixeira, T. S. Lopes, **R. F. Alexandre**, E. Ribeiro, D. Ramos, A. Violas, M. Monteiro, J. R. S. Barbosa, K. Oliveira, P. A. Fernandes, P. M. P. Salomé, "*Light Management in Cu(In,Ga)Se$_2$ solar cells*" Summer School of Materials for Energy Transition 2022- **Best Poster for critical materials reduction**
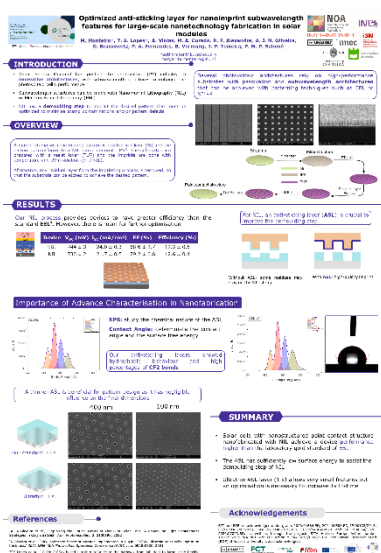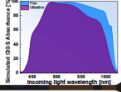
M. Monteiro, T. S. Lopes, A. Violas, M. A. Curado, **R. F. Alexandre**, A. J. N. Oliveira, G. Brammertz, P. A. Fernandes, B. Vermang, J. P. Teixeira, P. M. P. Salomé, "*Optimized anti-sticking layer for nanoimprint subwavelength features for large-scale nanotechnology fabrication in solar modules*" Summer School of Materials for Energy Transition 2022

E. J. Ribeiro#, **R. F. Alexandre#**, A. J. N. Oliveira, T. S. Lopes, A. Violas, J. P. Teixeira, P. A. Fernandes, P. M. P. Salomé, *"Low-cost nanofabrication for light management architectures in ultrathin solar cells"*, UT Austin Portugal Annual Conference 2022, Nanotechnologies program **#Authors contributed equally**

A. J. N. Oliveira, D. Ramos, **R. F. Alexandre**, E. J. Ribeiro, T. S. Lopes, A. Violas, J. P. Teixeira, P. A. Fernandes, P. M. P. Salomé, *"Plasmonic rear architecture as an efficient light management strategy for ultrathin solar cells"* UT Austin Portugal Annual Conference 2022, Nanotechnologies program
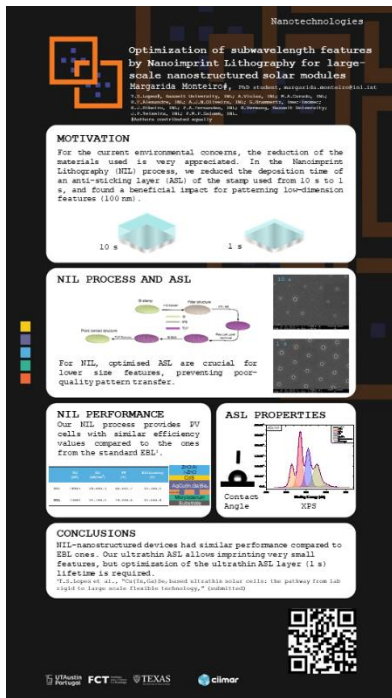
M. Monteiro, T. S. Lopes, A. Violas, M. A. Curado, **R. F. Alexandre**, A. J. N. Oliveira, G. Brammertz, E. J. Ribeiro, P. A. Fernandes, B. Vermang, J. P. Teixeira, P. M. P. Salomé, *"Optimization of subwavelength features by Nanoimprint Lithography for large-scale nanostructured solar modules"* UT Austin Portugal Annual Conference 2022, Nanotechnologies program

Outreach

A. J. N. Oliveira, **R. F. Alexandre**, A. Violas, T. S. Lopes, J. P. Teixeira, P. A. Fernandes, P. M. P. Salomé. *"Light Wars"*, INL Research Symposium 2022, Video
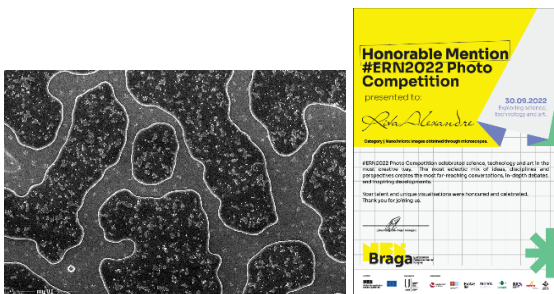
R. F. Alexandre, European Researchers' Night 2022 Braga #ERN2022 Photo Competition – **Honourable Mention**

NOVA SCHOOL OF
SCIENCE & TECHNOLOGY

Development of nanoimprint lithography processes for state-of-the-art
light management strategies to be integrated in cigs solar cells

RITA FRIJA ALEXANDRE

2022