NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

DANIEL NETO SEBASTIÃO

BSc in electrical and computer engineering

AN 18GHz WIDE-BAND BUFFER

MASTER IN ELECTRICAL AND COMPUTER ENGINEERING

NOVA University Lisbon
September, 2022

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DANIEL NETO SEBASTIÃO

BSc in electrical and computer engineering

Adviser: João Carlos da Palma Goes
Full Professor, NOVA University Lisbon

Co-adviser: Bob Verbruggen
PMTS Silicon Design Engineer, Advanced Micro Devices, Inc. (AMD)

Examination Committee

Chair: Pedro Miguel Figueiredo Amaral
Assistant Professor, NOVA University Lisbon

Rapporteur: Fábio Moreira de Passos
Researcher, Instituto de Telecomunicações do Instituto Superior Técnico

Member: João Carlos da Palma Goes
Full Professor, NOVA University Lisbon

MASTER IN ELECTRICAL AND COMPUTER ENGINEERING
SPECIALIZATION IN MICROELECTRONICS, TELECOMMUNICATIONS, AND ELECTRICAL POWER ENGINEERING

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This document was created with the (pdf/Xe/Lua)LaTeX processor and the NOVAthesis template (v6.9.14) [1].

To my lovely parents (Jorge and Maria)
To my lovely brother (Filipe)
And last, but not least, to my lovely girlfriend (Inês)

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"The most beautiful experience we can have is the mysterious. It is the fundamental emotion which stands at the cradle of true art and true science. Whoever does not know it and can no longer wonder, no longer marvel, is as good as dead, and his eyes are dimmed." (Albert Einstein, 1879-1955)

Abstract

Recent developments in wireless communication and systems, such as sixth-generation (6G), radar and instrumentation have led to massive use of high-frequency carriers. As a result, there is a high demand for Analog-to-Digital Converters (ADCs) in direct-conversion architectures with high bandwidth, high-resolution, and with the highest possible power efficiency and spectral purity.

A potential performance enhancement of an ADC can be realized by adding a voltage Input Buffer (IB). To increase the IB bandwidth and decrease the distortion from the nonlinear sampling circuit, a low output impedance is required. Therefore, to achieve low output impedance, it is necessary to dissipate power that is often equal to or greater than the power dissipated in the rest of the ADC blocks combined, since the output impedance is inversely proportional to the bias current. Consequently, input buffers are one of the most "power-hungry" building blocks of any direct receiver chain.

In recent years, due to the high ADC resolution and quantization range, the existing approaches use IBs with supply voltages above the nominal rails, for instance, 2.5 or 4.0 V, to increase the linearity and to not limit the ADC output swing. However, it inherently creates reliability and robustness issues.

This work investigates several different input buffers implemented in 7 nm FinFET technology with 1.8V of supply voltage in which a one pico farad of sampling capacitance is driven. The study starts by exploring four single-stage topologies in thick gate devices with and without linearity techniques, for example, the drain-source voltage "bootstrap" technique. Moreover, two bandwidth extension techniques are introduced, for instance, the Bridge T-coil with Series Peaking and the Distributed Approach. Lastly, two-stage IB architectures with thick oxide devices together with thin oxide devices are implemented.

Finally, the new solutions presented meet the requirements by exhibiting more than 18 GHz of bandwidth with a linearity (IIP3) higher than 16.3 dBm, and a DC power consumption lower than 178.2 mW without compromising reliability and robustness issues.

Keywords: 6G, ADC, Direct-conversion, Input Buffer, 7 nm FinFET, Wide-Band, High linearity, Power efficiency, Reliability.

Resumo

Os mais recentes desenvolvimentos nos sistemas de comunicação sem fios, como a sexta geração (6G) de redes móveis, levaram ao uso massivo de portadoras de alta frequência. Com efeito, é crescente a demanda por conversores analógico-digital (*ADCs*) nas arquiteturas de conversão direta, com elevada largura de banda, de alta resolução, com um baixo consumo de energia e com uma elevada linearidade.

Uma potencial melhoria no desempenho do *ADC* pode ser alcançada através de um *input buffer (IB)*. Para aumentar a largura de banda do *IB* e diminuir a distorção causada pelo circuito de amostragem é necessária uma baixa impedância de saída. Sendo a impedância de saída inversamente proporcional à corrente de polarização, para alcançar uma impedância de saída baixa é essencial dissipar potência que muitas das vezes é igual ou superior à soma da potência consumida no resto dos blocos do *ADC*. Consequentemente, o *input buffer* é um dos blocos da cadeia recetora que mais energia consume.

Nos últimos anos, devido à elevada resolução do *ADC*, as abordagens existentes usam *input buffers* com tensões de alimentação superiores à tensão nominal de alimentação, por exemplo, 2.5 ou 4.0 V, de forma a aumentar a linearidade e não limitar a tensão saída do *ADC*. Porém, inerentemente surgem questões de fiabilidade e robustez.

Neste contexto, o escopo do presente trabalho é investigar diversos *input buffers* implementados em tecnologia 7 nm *FinFET* com 1.8V de tensão de alimentação e com uma capacidade de carga de um pico farad. O estudo começa por explorar quatro topologias de *input buffer* com dispositivos de grandes dimensões, com e sem técnicas de linearidade, nomeadamente, a técnica que força a tensão dreno-fonte a ser constante. Ademais, são introduzidas duas técnicas que aumentam a largura de banda, *The Bridge T-coi*l com *Series Peaking* e a *Distributed Approach*. Finalmente, são implementadas arquiteturas de *input buffer* com dois andares em dispositivos de pequenas e grandes dimensões.

Por último, são apresentadas novas soluções que cumprem inteiramente as especificações, uma vez que exibem uma largura de banda maior que 18 GHz com uma linearidade (IIP3) superior 16.3 dBm e um consumo de potência inferior a 178.2 mW, sem comprometer a fiabilidade e a robustez dos dispositivos.

Palavras-chave: 6G, *ADC*, Conversão direta, *Input buffer*, 7 nm *FinFET*, Largura de banda, Linearidade, Potência, Fiabilidade.

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Acronyms

6G Sixth-Generation *(p. viii)*

AC Alternating Current *(p. 3)*
ADC Analog-to-Digital Converter *(p. 1)*

BSF Basic Source Follower *(pp. 6, 87)*
BW Bandwidth *(p. 1)*

CMFB Common-Mode Feedback *(p. 36)*
CMRR Common-Mode Rejection Ratio *(p. 23)*
CSF Cascade Source Follower *(p. 19)*

DC Direct Current *(p. 3)*

ESD Electrostatic Discharge *(pp. 4, 87)*

FinFET Fin Field-Effect Transistor *(p. 4)*
FSF Flipped Source Follower *(p. 20)*

HD3 3^{rd} Harmonic Distortion *(p. 33)*

IB Input Buffer *(p. 1)*
IIP2 Input second Intercept Point *(p. 23)*
IIP3 Input third Intercept Point *(p. 33)*
IM Inter Modulation *(p. 34)*
IM3 3^{rd} order Inter-Modulation *(p. 33)*

KCL Kirchhoff's Current Law *(p. 6)*

LNA Low Noise Amplifier *(p. 1)*

MOS Metal Oxide Semiconductor *(p. 6)*

RX Receiver *(p. 1)*

S/H Sample-and-Hold *(p. 1)*
SF Source Follower *(p. 6)*
SFDR Spurious-Free Dynamic Range *(p. 4)*
SNR Signal-to-Noise Ratio *(p. 23)*
SSF Super Source Follower *(p. 21)*

TF Transfer Function *(p. 7)*
THA Track-and-Hold Amplifier *(p. 4)*
TSMC Taiwan Semiconductor Manufacturing Company *(p. 31)*

Symbols

A_{DC}	DC gain *(p. 8)*
A_{in}	Input amplitude *(p. 33)*
C_0	Oxide capacitance per unit transistor width *(p. 6)*
C_{load}	Sampling capacitance *(p. 2)*
C_{db}	Drain-to-body intrinsic capacitance *(p. 9)*
C_g	Gate intrinsic capacitance *(p. 6)*
C_{gb}	Gate-to-body intrinsic capacitance *(p. 6)*
C_{gd}	Gate-to-drain intrinsic capacitance *(p. 6)*
C_{gs}	Gate-to-source intrinsic capacitance *(p. 6)*
C_{in}	Total input capacitance *(p. 30)*
C_{ox}	Gate oxide capacitance *(p. 6)*
C_{sb}	Source-to-body intrinsic capacitance *(p. 9)*
u_n	Electron mobility *(p. 15)*
f	Frequency *(p. 12)*
f_{-3dB}	Half power point *(p. 3)*
Φ_F	Fermi potential *(p. 14)*
g_{ds}	Output small-signal conductance *(p. 17)*
g_m	Gate small-signal transconductance *(p. 2)*
g_{mb}	Body small-signal transconductance *(p. 8)*
I_D	Drain current *(p. 11)*
$IIP3_{min}$	Minimum value of IIP3 within the band *(p. 3)*
$IM3_{LOW}$	Low frequency IM3 *(p. 42)*
L	Transistor length *(p. 6)*

L'	Effective channel length *(p. 15)*
λ	Body effect coefficient *(p. 15)*
ΔV_{out}	Output swing *(p. 11)*
P_{DC}	DC power *(p. 12)*
P_{in}	Input power *(p. 41)*
R_{out}	Output resistance *(p. 2)*
R_{ds}	Transistor output resistance *(p. 8)*
s	Laplace variable *(p. 9)*
$S_{11_{dd}}$	Differential input port voltage reflection coefficient *(p. 3)*
V_{DD}	Voltage supply *(p. 6)*
V_{ds}	Drain-Source voltage *(p. 6)*
$V_{DS,sat}$	Minimum voltage required to keep the transistor in saturation *(p. 17)*
V_{gs}	Gate-Source voltage *(p. 6)*
V_{in}	Input signal *(p. 6)*
$\overline{V_{n,in}^2}$	Input-referred noise *(p. 17)*
V_{out}	Output signal *(p. 6)*
$V_{out_{CM}}$	Output common-mode voltage *(p. 52)*
$V_{out_{pp}}$	Differential output voltage peak-to-peak *(p. 41)*
V_{sb}	Source-Bulk voltage *(p. 8)*
V_{TH}	Threshold voltage *(p. 6)*
W	Transistor width *(p. 6)*
ω	Angular frequency *(p. 10)*
Z_{in}	Input impedance *(p. 11)*
Z_L	Load impedance *(p. 11)*
Z_{out}	Output impedance *(p. 11)*
Z_s	Source impedance *(p. 11)*

1 Introduction

Rapid advances in wireless communication as sixth-generation (6G) have led to massive use of high-frequency carriers. As a result, more carriers, higher data rates, wider cellular coverage, and a simpler system design are required for the emerging technology compared to the state of the art [2]. For these reasons, there is a high demand for Analog-to-Digital Converters (ADCs) with high-resolution, high Bandwidth (BW), and with the highest possible power efficiency and spectral purity [3].

ADCs are the interface between two worlds: analog and digital. The analog domain corresponds to the environment as a variation in any physical quantity, such as temperature or speed can be expressed as an analogue signal (continuous in time). Nevertheless, performing computations and data processing for majority of information is more efficient in digital domain. Thus ADC is required.

The recent development in direct-conversion ADC architectures has resulted in lower complexity, power and cost with respect to traditional receiver architectures as Heterodyne Receiver (see Figure 1.1) [4]. In addition, the replacement of traditional receiver architectures (narrowband architectures) with direct conversion architectures eliminated the need for linear amplifiers [5], analog mixers, and complex filters. Moreover, realization and simplification of several operations in the digital domain are acquired, thus the performance of the whole receiver chain is increased [2, 3].

Although the direct conversion receiver does not need the analog mixers, it does require high sampling frequencies (fs) since the ADC is closer to the antenna (see Figure 1.1), consequently, increasing the ADC power consumption.

A potential performance enhancement of the receiver can be realized with a voltage Input Buffer (IB). There are several benefits IB could provide to the Receiver (RX) Chain performance. First of all, the Sample-and-Hold (S/H) circuit and the Low Noise Amplifier (LNA) cannot be linked directly without significantly rising the power dissipation and degrading the ADC drive. Secondly, the high input resistance and low output resistance [6] allow the absence of resistive input-matching because, from the S/H circuit point of view, the ideal Input Buffer works as a wire (a constant impedance [7], more precisely an impedance with low variations [3]). Therefore, the S/H circuit can sense a perfect replica

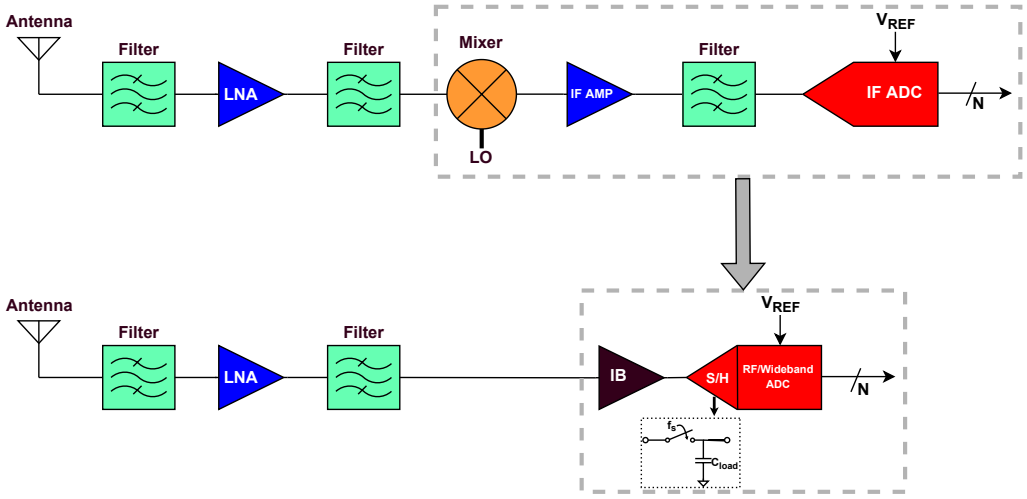


Figure 1.1: Traditional Heterodyne Receiver vs Direct RF Receiver

of the input signal, thus isolating the input signal from any load injection or any kickback noise coming from the sampling capacitance (C_{load}) [2, 8, 9].

On the other hand, to increase the bandwidth and decrease the distortion from the nonlinear sampling circuit [9], a low output impedance is required [2]. To achieve a low output impedance, it is necessary to dissipate power that is often equal to or greater than the power dissipated in the rest of the ADC blocks combined [3, 6, 7] since the output impedance is inversely proportional to the bias current ($R_{out} \approx \frac{1}{g_m}$). As a result, the Input Buffers are one of the most "power-hungry" building blocks of any Direct RX Chain.

In recent years, due to the high ADC resolution and quantization range, an IB with a high output swing is required [7]. Therefore, the existing approaches use IB with supply voltages above the nominal rails, for instance, 2.5 or 4.0 V, to not limit the ADC output swing. However, it inherently creates reliability and robustness issues [3].

It is worth mentioning that, the replacement of the IB with a voltage amplifier is hardly possible, in the sense that the voltage amplifier has a low input bandwidth.

Based on the aforementioned explanations, the ideal Input Buffer has the following specifications:

- DC gain approximately equal to one.
- Low power consumption.
- Low input-referred noise.
- Low output impedance.
- High input impedance.
- High output swing.
- High bandwidth.
- High linearity.

1.1 Thesis Objectives and Original Contributions

Based on the discussion above, the aim of this thesis is therefore to implement a 18 GHz wide-band buffer with its specifications as close as possible to an ideal input buffer while

obtaining highest possible bandwidth and spectral purity. Furthermore, it should improve the power efficiency of the entire RX chain compared with the state of the art.

First goal of this dissertation is to explore, simulate and compare different input voltage buffer topologies described in the literature. Second objective is to understand various design parameters such as bias currents, transistors widths, and trade-offs present in IBs. Finally, the design exploration performed results in a design of IBs with the following specifications:

Table 1.1: Input Buffer Specifications

Output common-mode voltage	0.7/0.9 V
Bandwidth (f_{-3dB})	> 18 GHz
Input return loss ($S_{11_{dd}}$)	-10 dB up to 18 GHz
DC gain	$\approx -6dB$
$IIP3_{min}$	$\approx$ 23 dBm
Input-referred noise	$\approx$ 200 μV_{rms}

It should be pointed out that the DC gain should be approximately equal to -6 dB with an AC magnitude of 0.5V.

Moreover, with the discovered solutions, a manuscript with the title "Design of an 18 GHz Wide-Band Input Buffer" (see Annexes) will be submitted for publication to the IEEE International Symposium on Circuits and Systems, ISCAS'23 (to be hosted in Monterey, California, USA, in June 2023), on the 24th of October.

1.2 Thesis Outline

This dissertation is organized as follows:

In chapter 2 is presented the results from the best state-of-art papers.

In chapter 3 the main features of various state-of-the-art Source Follower topologies are described. Furthermore, a theoretical analysis is provided in terms of gain, noise, bandwidth, and AC transfer function.

In chapter 4, after reviewing the design trade-offs and selecting the best configurations for this project, the test bench used for evaluation of different topologies and simulation constraints are presented.

In chapter 5 two bandwidth extension techniques are introduced, which lead to increase in bandwidth and improve the return loss.

In chapter 6 two-stage architectures are discussed, where input buffers are presented to increase bandwidth at the cost of noise, area, and linearity.

In chapter 7, the dissertation is concluded, and sensible recommendations are presented for future developments.

2

State-of-the-Art

This chapter introduces the best state-of-art papers and is divided into two sections. The first section describes ultra-wideband input stages, and the second section presents linearity enhancements in input networks.

2.1 Ultra-wideband Input Stages

2.1.1 Hybrid Push-pull Amplifier-Buffer (A. Ramkaj, IEEE VLSI, 2022)

The paper in [10] describes a 30GHz direct receiver analog front end in 16 nm FinFET technology. The project consists of a distributed ESD protection with a variable attenuation filter and a two-path hybrid push-pull amplifier and buffer. This article achieves our specs, 18GHz, and 23 dBm-IIP3, in terms of bandwidth and linearity for a 300fF sampling capacitance. In terms $S_{11_{dd}}$ does not meet our requirements, for instance, $S_{11_{dd}}$ lower that -10dB up to 18 GHz.

2.1.2 T&H Push-pull Buffer (A.M.A. Ali, ISSCC, 2020)

The paper in [11] presents a track and hold (T&H) Push-pull buffer in 16 nm FinFET and achieves 18 GHz and an 1-tone SFDR of 61 dBc at 4 GHz. It uses one Push-pull with "drain bootstrap" for the input buffer and a basic push-pull for the output buffer. The output buffer provides a low output impedance to drive the sampling capacitance and isolates the THA sampling switches from any charge injection. This work meets our spec of 18GHz.

2.2 Linearity Enhancements

2.2.1 AC-Coupled Flipped Source Follower (Z. Huang, IEEE TCS, 2022)

Output Current Linearization

In [12] a flipped source follower is implemented with the replica capacitance approach, discussed in section 3.8. This project has 6GHz bandwidth and 1-tone SFDR of 74 dB

at 300MHz. It improves the linearity by using the replica capacitance and the drain bootstrapping, but the bandwidth does not meet our spec.

2.2.2 Push-pull Buffer (S. Devarajan, JSSC, 2017) and RC Assisted Buffer (M. Straayer, ISSCC, 2016)

Channel Length Modulation Linearization

The articles [4, 13] describe a push-pull based topology that uses the "bootstrapping" technique, stated in section 3.9, to minimize the channel length modulation. These projects [4, 13] have a bandwidth of 7.4 and 4 GHz, respectively.

The implementations do not achieve 18 GHz bandwidth but show quality linearity measures.

2.3 Conclusion

The following table shows the results achieved by the best input stages in the state-of-art, the table only have bandwidth, linearity and DC power because this thesis is manly focused in input networks for high-speed applications with high linearity and low power consumption.

Table 2.1: Results state-of-the-art

Specification	**[10] Ramkaj**		**[11] Ali**		**[4] Devarajan**	**[12] Huang**		**[13] Straayer**
Technology	16 nm FinFET		16 nm FinFET		28 nm CMOS	28 nm CMOS		65 nm CMOS
Topology	Hybrid Push-pull		T&H Push-pull		Push-pull	Flipped SF		Dual Push-pull
Bandwidth [GHz]	30		18		7.4	6.0		4.0
Input Freq. [GHz]	5.0	10.0	4.0	8.0	4.0	1.8	4.0	1.8
1-tone SFDR [dBc]	67.9	64.3	61.0	55.0	66.0	65.0	69.0	66.3
Power [mW]	210.0		220.0		400.0	137.0		207.0

In literature, it is commonly used source follower typology's to drive ADCs. Therefore, source follower-based buffers will be investigated in the next chapter.

3

Source Follower Topologies

With state of the art topologies discussed, the analysis of each SF based buffer has to be performed in terms of gain, noise, bandwidth, and AC transfer function. The Basic Source Follower (BSF), section 3.1, provides a detailed analysis using the small-signal model. As the small signal analysis of other topologies is similar to the BSF, only a summary of the analysis is provided for the other architectures. Moreover, Matlab software is used for Kirchhoff's Current Law (KCL) equations since some designs are too difficult to analyze by hand.

It is worth mentioning that all the MOS transistors from the different topologies are working in the saturation region ($V_{ds} > V_{gs} - V_{TH}$ and $V_{gs} > V_{TH}$), since one of the aims of this project is high-speed applications. Because of this, except in the BSF, only the C_{gs} capacitance from the devices is considered (see Table 3.1).

Table 3.1: Capacitance of MOS transistor for different operation regions [14]

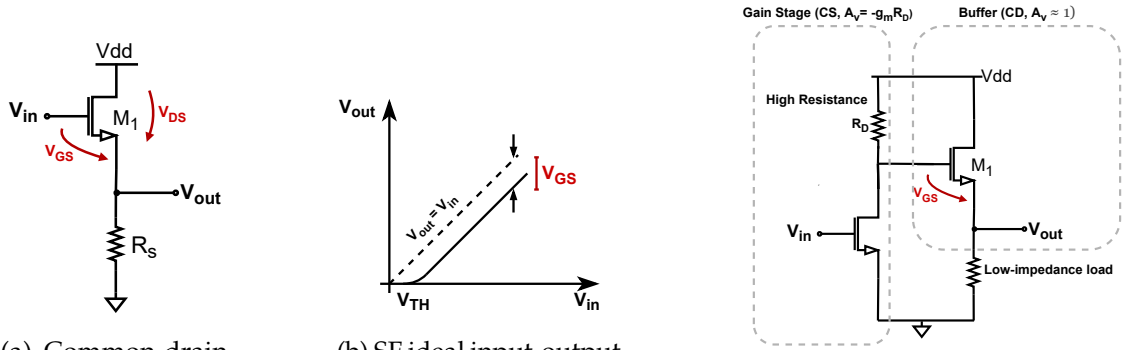
Operation Region	C_{gb}	C_{gs}	C_{gd}	C_g
Cutoff	WLC_{ox}	0	0	$WLC_{ox} + 2WC_0$
Resistive\Triode	0	$WLC_{ox}/2$	$WLC_{ox}/2$	$WLC_{ox} + 2WC_0$
Saturation	0	$(2/3)WLC_{ox}$	0	$(2/3)WLC_{ox} + 2WC_0$

3.1 Basic Source Follower

The simplest realizable Input Buffer in Complementary Metal Oxide Semiconductor (CMOS) technology is a transistor in common drain configuration (Figure 3.1a), also known as Source Follower (SF).

As depicted in Figure 3.1a, the input signal (V_{in}) is applied at the gate, having a high input impedance and the output signal (V_{out}) appears at the source, with a low output impedance. The voltage supply (V_{DD}) is injected into the drain.

The source follower senses an almost perfect replica of the input signal at the source. In other words, the source potential "follows" the gate voltage, despite vertical translation equal to minus V_{GS}. The level shift V_{GS} (see Figure 3.1b) reduces the input swing [15].



(a) Common-drain with a resistive load

(b) SF ideal input-output characteristic

(c) SF role

Figure 3.1: Source Follower

The gate receives the input signal, providing a low input current [16] since the resistance seen from the gate is approximately infinite, helping the source follower to be closer to the ideal case of input resistance being infinity.

A typical application of SF is to interconnect a gain stage with high output impedance (R_D) to drive the low-impedance load (see Figure 3.1c). In this case, an SF must be placed in between the gain stage and the load to ensure that the gain stage's high output impedance is not connected in parallel with the load's low impedance. Thus, it is ensured that the overall gain is not degraded [15].

3.1.1 DC Transfer Function

An analytical low-frequency Transfer Function (TF) can be derived from the small signal investigation (Figure 3.2). If "body effect" and the "channel-length modulation" are considered, the DC TF can be determined. One must emphasize that the MOS transistor itself is non-linear and is only considered linear around the DC operating point with low-amplitude signals, hence the name small-signal model.

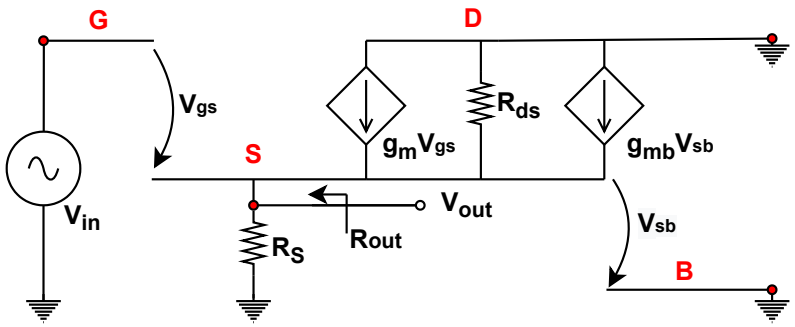


Figure 3.2: SF DC small-signal model

The algebraic sum of all currents entering and exiting a node must be equal to zero. This law is named Kirchhoff's law of currents and is utilized to derive the following

equations.

$$V_{gs} = V_{\text{in}} - V_{out} \qquad V_{sb} = V_{out} \tag{3.1}$$

The DC gain (A_{DC}) is equal to,

$$A_{DC} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{gm}{gm + g_{mb} + \frac{1}{Rds} + \frac{1}{Rs}} \tag{3.2}$$

where g_m is the transconductance of the transistor and R_{ds} its output resistance.

Another way to derive the DC transfer function of the circuit is through the equation Equation 3.3. Where G_m is the SF transconductance and R_{out} is the output resistance.

$$A_{DC} = \frac{V_{out}}{V_{in}} = G_m \times R_{out} \tag{3.3}$$

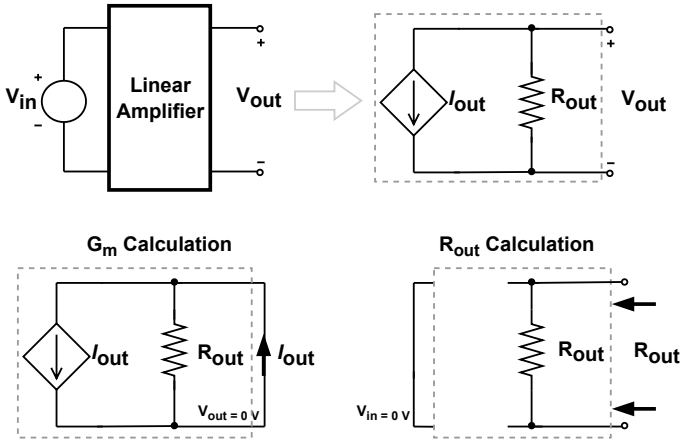
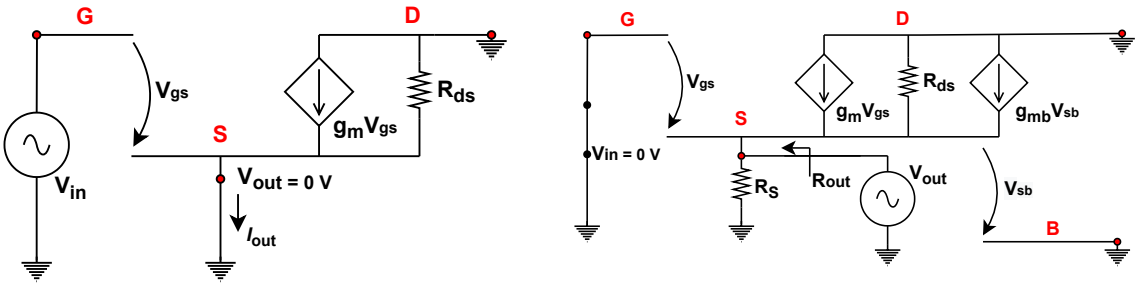


Figure 3.3: Norton equivalent of a linear circuit and $G_m R_{out}$ calculation



(a) G_m calculation

(b) R_{out} calculation

Figure 3.4: Gain calculation

By inspection of Figure 3.4 and use of KCL at the output node it can be proved that G_m and R_{out} are equal to Equation 3.5.

$$G_m = \left(\frac{i_{out}}{V_{\text{in}}}\right)_{V_{out}=0} \qquad R_{out} = \left(\frac{V_{out}}{i_{\text{out}}}\right)_{V_{in}=0} \tag{3.4}$$

$$G_m = \frac{i_{\text{out}}}{V_{\text{in}}} = g_m \qquad R_{\text{out}} = \frac{1}{g_m + g_{mb} + \frac{1}{R_S//R_{ds}}} \tag{3.5}$$

Finally, the DC voltage gain is equal to:

$$A_{DC}(s=0) = G_m \times R_{\text{out}} = \frac{g_m}{g_m + g_{mb} + \frac{1}{R_S//R_{ds}}} \tag{3.6}$$

The difference between the numerator and denominator in the DC gain equation, Equation 3.6, is $g_{mb} + \frac{1}{R_S//R_{ds}}$. This difference is called follow-up error (FE), in other words the error that diverges the SF from a unity gain buffer. It has to be noted that A_{DC} is only equal to one in the ideal scenario, without second-order effects, such as channel-length modulation and body effect. Nonetheless, if $g_m \gg FE$ is reasonable to assume that the DC gain is approximately one.

$$A_{DC} \approx 1 \tag{3.7}$$

3.1.2 AC Transfer Function

The DC transfer function does not account for the NMOS transistor intrinsic capacitances, such as C_g, C_{gs}, C_{gd}, C_{db}, C_{sb}, and C_{gb}. These capacitances are critical because they determine the bandwidth of the circuit.

A MOS transistor with a high channel length means large intrinsic capacitance (see Table 3.1), which translates to low bandwidth. Although, it also means higher gain since there is a trade-off between gain and bandwidth.

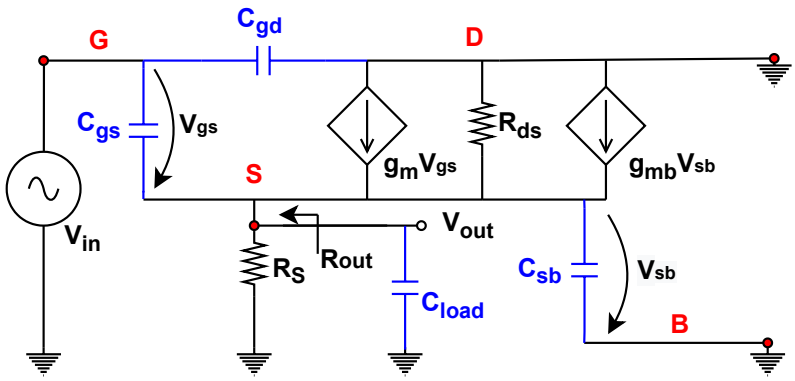


Figure 3.5: SF AC small-signal model

From the Figure 3.5 its possible to extract an approximated expression of the AC transfer function. Applying KCL at the output node, the following equation relating V_{out} and V_{in} is obtained.

$$V_{\text{out}}\, sC_{sb} + \frac{V_{\text{out}}}{R_S//R_{ds}} - g_m V_{gs} + g_{mb} V_{sb} - V_{gs} sC_{gs} = 0 \tag{3.8}$$

By rearranging Equation 3.8 and replacing V_{gs} for $V_{\text{in}} - V_{out}$, this equation can be written as Equation 3.9.

$$TF(s = j\omega) = \frac{g_m + sC_{gs}}{g_m + g_{mb} + \frac{1}{R_S//R_{ds}} + s\left(C_{gs} + C_{sb}\right)} \tag{3.9}$$

Equation 3.9 describes the existence of one pole and one zero in the SF. Where the pole and zero is equal to, ω_p and ω_z, respectively.

$$\omega_p = -\frac{g_m + g_{mb} + \frac{1}{R_s//R_{ds}}}{C_{gs} + C_{sb}} \qquad \omega_z = -\frac{g_m}{C_{gs}} \tag{3.10}$$

It is worth mentioning that the input resistance is considered infinite, and the gate capacitance C_g is ignored. Because of this, there is only an output pole and no input pole. Moreover, in practical situations, the SF is connected to a sampling capacitance (C_{load}), meaning that ω_p could not be precise. To make the approximation more accurate, and if $C_{load} \gg C_{gs} + C_{sb}$, the equation can be altered as follows:

$$\omega_p \approx -\frac{g_m + g_{mb}}{C_{load}} \tag{3.11}$$

In terms of stability, the zero and the pole are always stable. To be precise, they are located on the left half-plane in root-locus.

The key observation here is the necessity to increase g_m or decrease C_{gs}, C_{load} to extend the bandwidth, technically shifting the output pole to higher frequencies. There are three ways of doing this, reducing L to lower C_{gs} or escalating I_D or W to increase g_m. Although, the most sensible way is to "burn current" and reduce L instead of increasing W, which inherently creates parasitic capacitance issues [17].

3.1.2.1 AC transfer function with a complex source impedance

As stated previously, for the AC TF to be precise a complex source impedance and a gate to ground capacitance (C_g) have to be considered.

The small signal model can be drawn as shown in Figure 3.6.

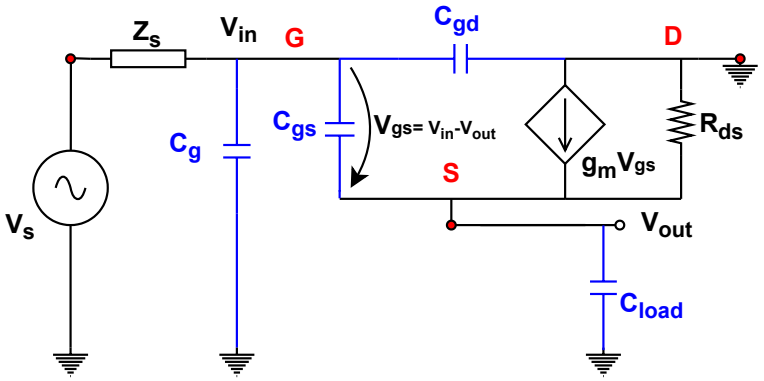


Figure 3.6: SF AC small-signal model with a source impedance

Ignoring the body effect and consider R_s infinite, the transfer function of the SF can be described as:

$$\frac{V_{out}}{V_s}(s) \approx \frac{1}{\left(1+s(C_g+C_{gd})Z_s\right)} \times \frac{1}{\left(1+\frac{\frac{Z_s}{1+s(C_g+C_{gd})Z_s}+\frac{1}{sC_{gs}}}{\left(1+g_m\frac{1}{sC_{gs}}\right)Z_L}\right)} \tag{3.12}$$

where Z_s is the source impedance, and Z_L is the load impedance.
The input and output pole are approximately equal to,

$$\omega_{p_{out}} \approx -\frac{g_m}{C_{load}} \qquad \omega_{p_{in}} \approx -\frac{1}{\Re(Z_s)\cdot(C_g+C_{gd})} \tag{3.13}$$

As discussed in subsection 3.1.1 it is impossible to have a unity transfer function, but it's crucial to get as close as possible to improve linearity.

Equation 3.12 indicates that, to have a TF approximately equal to one, the following has to happen

$$s(C_g+C_{gd})Z_s \to 0 \quad \cap \quad (1+g_m\frac{1}{sC_{gs}}Z_L) \to +\infty \tag{3.14}$$

Meaning that the MOS intrinsic capacitances (C_g,C_{gd}, and C_{gs}) have to be lower as possible and g_m, Z_L have to be large. This can be done by increasing the current and decreasing the load capacitance. In the (former or latter) case also the cut-off frequency is increased (see Equation 3.13).

An input buffer provides a high input impedance for a better isolation (reverse gain) and low output impedance to drive the sampling capacitance. The input impedance and the output impedance are:

$$\begin{aligned}\frac{1}{Z_{\text{in}}} &\approx s(C_g+C_{gd}) + \frac{1}{\frac{1}{sC_{gs}}+Z_L+g_m\cdot\frac{1}{sC_{gs}}\cdot Z_L}\\ \frac{1}{Z_{\text{out}}} &\approx \frac{1}{\frac{1}{g_m}+\frac{Z_s}{g_m\cdot\frac{1}{sC_{gs}}}}\end{aligned} \tag{3.15}$$

To increase Z_{in} and decrease Z_{out}, have to:

- Increase g_m.
- Decrease C_{gs}.
- Decrease C_{load}.
- Decrease Z_s.
- Decrease $C_g + C_{gd}$

3.1.3 Output Swing and DC Power Consumption

The output swing (ΔV_{out}) refers to the range of values the output signal can take under specified conditions. For instance, all the transistors in the circuit stay in saturation. The source follower with a resistive load has an output swing equal to,

$$\Delta V_{out} = V_{DD} - V_{DS,SAT_1} - I_D R_s \tag{3.16}$$

where V_{DS,SAT_1} is the minimum required voltage to keep M1 in saturation.

The source follower DC power consumption is equal to,

$$P_{DC} = I_D \times V_{DD} \tag{3.17}$$

One way to improve the source follower linearity is to increase the output swing by increasing V_{DD}. However, that degrades the DC power consumption [11].

3.1.4 Noise and DC Power Consumption

Noise versus DC power consumption (P_{DC}) represents a well know trade-off in analogue design. For this analysis the superposition theorem is used that holds for uncorrelated noise sources.

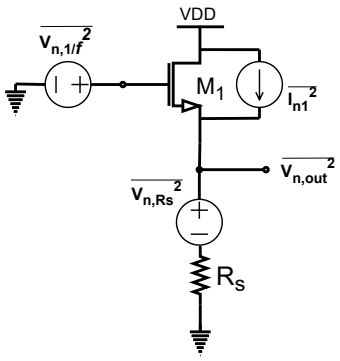


Figure 3.7: SF Noise

Parametrizing the transistor M1 with multiple fingers allows us to neglect the gate resistance noise. Considering the channel thermal noise, $\overline{I_{n1}^2}$, and the flicker noise $\overline{V_{n,\frac{1}{f}}^2}$, Equation 3.18.

$$\overline{I_{n1}^2} = 4kT\gamma g_m \qquad \overline{V_{n,1/f}^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{3.18}$$

The SF input-referred noise (gain independent) is approximately equal to:

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_{DC}^2} = \frac{4KT\gamma}{g_m} + \frac{K}{C_{ox}WL} + 4KTR_s \quad \frac{V^2}{Hz} \tag{3.19}$$

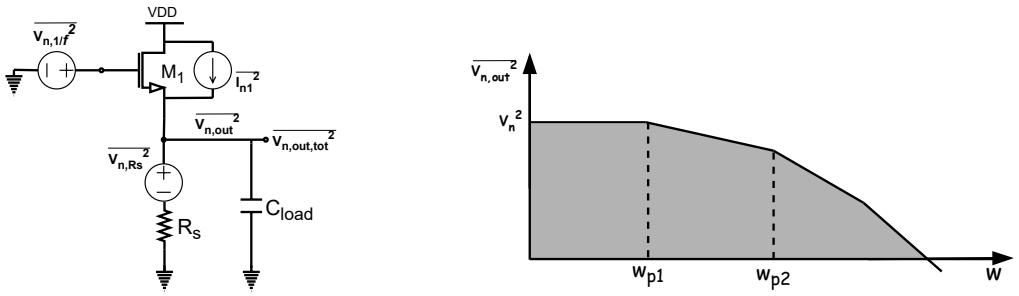
As detailed in Equation 3.19, increasing the drain current can lower the noise. On the other hand, P_{DC} is roughly $V_{DD} \times I_D$, which means that increasing the drain current leads to higher power consumption.

3.1.5 Noise and Bandwidth

In section above, the input-referred noise is analyzed without consideration of the output capacitive load C_{load}. This assumption neglects some key aspects, such as the bandwidth and noise dependence on C_{load}. Considering C_{load} is essential, otherwise the bandwidth

is not limited due to a pole absence. In such a case the integrated noise is infinite as the magnitude of the noise sources does not fluctuate across frequencies.

The total noise corruption results from all the components that fall in band of interest, meaning that decreasing the bandwidth will reduce the noise. For a multipole system with noise spectrum as in Figure 3.8b, the total output noise can be estimated by calculating the total area below the output noise spectral density.



(a) Noise calculation (b) Output noise spectrum

Figure 3.8: Noise Bandwidth

$$\overline{V_{n,\text{out,tot}}^2} = \int_0^\infty \overline{V_{n,\text{out}}^2} \quad df \tag{3.20}$$

From signal theory, if a signal with spectrum S_x is applied to a linear time invariant system (LTIS) with transfer function H(s), the output spectrum S_Y is equal to:

$$S_Y(f) = S_x(f)|H(f)|^2 \tag{3.21}$$

Consider $R_s \gg \frac{1}{g_m}$ and the output pole approximately $\omega_p \approx -\frac{g_m}{C_{load}}$. The total integrated noise can be calculated as:

$$\begin{aligned}
\overline{V_{n,\text{out,tot}}^2} &\approx \int_0^\infty \overline{V_{n,out}^2}|H(f)|^2 df = \int_0^\infty \overline{V_{n,out}^2}\left|\frac{g_m}{g_m + j\omega C_{load}}\right|^2 df \\
&= \int_0^\infty \overline{V_{n,out}^2}\frac{g_m^2}{g_m^2 + \omega^2 C_{load}^2} df = \overline{V_{n,out}^2}\int_0^{+\infty} \frac{1}{1 + \left(2\pi f/\omega_p\right)^2} df \\
&= \overline{V_{n,out}^2}\cdot\frac{\omega_p}{2\pi}\cdot\lim_{f\to+\infty}\text{atan} f = \overline{V_{n,out}^2}\cdot\frac{\omega_p}{2\pi}\cdot\frac{\pi}{2} = \frac{1}{4}\overline{V_{n,out}^2}\cdot\frac{g_m}{C_{load}}
\end{aligned} \tag{3.22}$$

It is worth mentioning that, in this analysis the output pole is considered the circuit's dominant pole (w_{p1}).

According to Equation 3.22, the total noise can be reduced by using a higher capacitive load. However, this will reduce the bandwidth by generating a lower output pole.

3.1.6 SF Non-Linearity

Unfortunately, the great benefits of using an SF come with drawbacks, such as body effect, channel length modulation, and output current variation.

3.1.6.1 Body Effect

The V_{GS} dependence on drain current and the threshold voltage (V_{TH}) is a crucial aspect in analog circuit design due to the causal relationship between V_{GS} and body effect [18]. If V_{in} starts to vary, the potential difference between the source and the bulk (V_{sb}) starts to fluctuate. Thus the higher V_{sb} is, the higher the V_{TH} and V_{GS} are, Equation 3.23 and Equation 3.24, consequently reducing the output voltage for the same V_{in}, Figure 3.9.

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L'}}} + V_{TH} \tag{3.23}$$

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F + V_{sb}} - \sqrt{|2\Phi_F|} \right) \tag{3.24}$$

It is worth mentioning that the previous equations are valid when the transistor is operating in strong inversion and in saturation zone.

Additionally, there is a variation of depletion region charge with V_{sb}. If V_{sb} increases the charge carrier concentration in the channel increases, leading to an increasing V_{TH}.

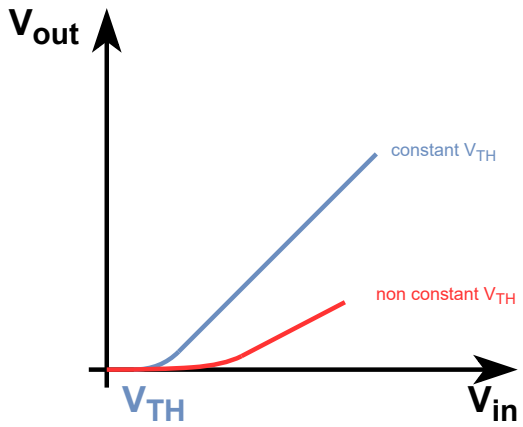


Figure 3.9: SF real input-output characteristic

As discussed earlier, it is possible to conclude that the SF with body effect leads to a nonlinear device, causing distortion in the output [16, 18]. This distortion is dictated by the dominant second harmonic [19]. However, when using a differential topology, the second harmonic can be eliminated leading to a third order dependency [16]. There are two ways to minimize body effect. The first one is to attach both source and bulk terminals to one another, forcing V_{TH} to be constant. Although, V_{TH} is almost constant, the dependence of V_{GS} in the drain current (I_D) means that increasing the DC input level increases V_{GS} and I_D. But not in the same proportion, thereby incurring non-linearity [15]. In addition, if the connection between the source and drain introduces considerable parasitic capacitances on the output, the linearity is degraded even further [20].

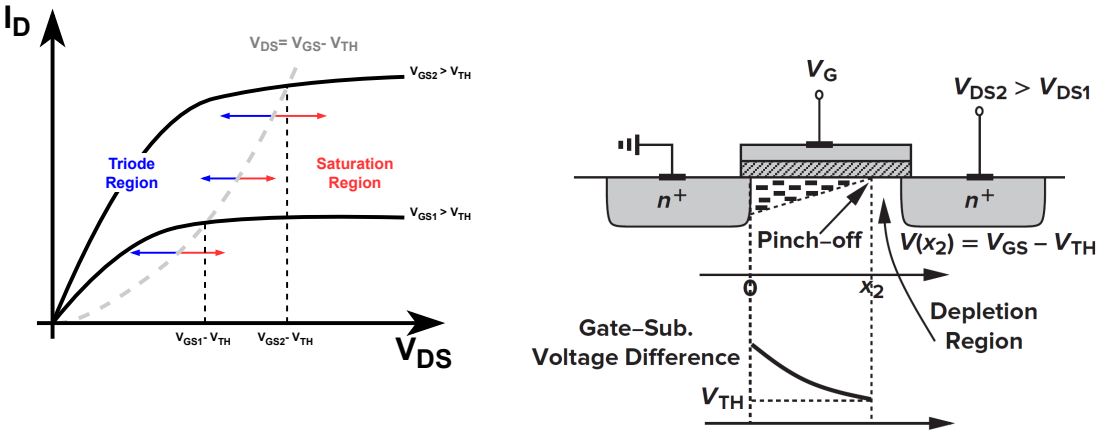
Another way to suppress body effect is by replacing the load resistance with a current source, which makes the DC input signal more independent from I_D (see subsection 3.1.7).

To sum up, the proper approach to deal with body effect is to bias the transistor using current instead of voltage and linking both source and bulk terminals. A current biased circuit is less sensitive to PVT (Process Spread, supply Voltage, Temperature), which heavily affects the values of V_{TH}, u_n, and C_{ox}. Moreover, attaching the source to the bulk means that V_{TH} is relatively constant.

3.1.6.2 Channel-Length Modulation

Another crucial aspect of non-linearity, perhaps the most predominant factor of non-linearity in short-channel devices, is the variation of the effective channel length (L') with the drain-source voltage (V_{DS}), called "channel-length modulation".

To understand this phenomenon, we need to understand the "pinch-off behavior". When V_{DS} exceeds the overdrive voltage ($V_{ov} = V_{GS} - V_{TH}$), the dashed grey line in Figure 3.10a , the drain current does not follow the parabolic behavior but starts to become almost constant. At this point the transistor begins to operate in the saturation region, the inversion layer stops, and the channel enters "pinch-off" [15], meaning that L' will be different from the actual device length L, Figure 3.10b.



(a) Output characteristic

(b) Pinch-off behavior [15]

Figure 3.10: Channel-Length Modulation phenomenon

Mathematically it is possible to demonstrate the pinch-off phenomenon using the "square-law" formula (Equation 3.25) and the effective length formula (Equation 3.26).

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2 \tag{3.25}$$

$$L' = L - \Delta L = L\left(1 - \frac{\Delta L}{L}\right) \cong L(1 - \lambda V_{DS}) \cong \frac{L}{1 + \lambda V_{DS}} \tag{3.26}$$

As a result, the "square-law" formula with V_{DS} explicit is as follows:

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.27}$$

From Equation 3.27 it is clear that the drain current is a function of V_{DS}. Unfortunately, when the input signal changes the potential V_{DS} also changes, thereby implying non-linearity.

Finally, there are several ways to minimize channel length modulation. The first one is to design the transistor in the triode region, where there is no channel-length modulation. The second one is to parameterize the channel length with a high value ($\frac{\Delta L}{L} \approx 0$). However, neither of the two solutions works for high-speed applications.

The third way is to "bootstrap" the potential V_{DS}, in other words, forcing V_{DS} to be relatively constant. This approach is studied and simulated in chapter 4.

3.1.6.3 Output Current Variation

Previously we have seen the SF intrinsic non-idealities, but these are not the only sources of non-linearity. Another factor that influences the linearity is the buffer interaction with its load Z_L and its driver Z_s.

As displayed in Figure 3.11 the current in the channel ($I + i_L$) is the sum of a DC component I and an AC component i_L. The I is the DC bias current and i_L is the current flowing in the load capacitance (C_{load}).

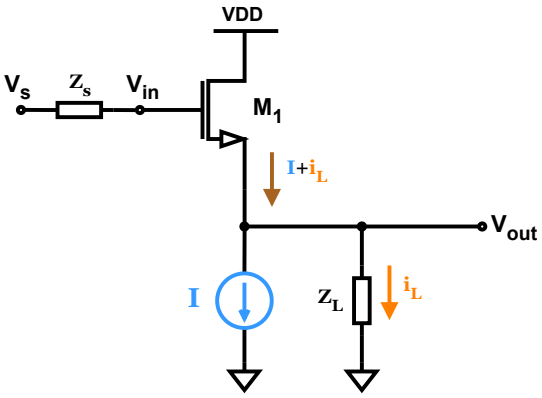


Figure 3.11: SF with complex impedances

Mathematically the load current is equal to

$$i_L = \frac{V_{out}}{Z_L} \cong V_{out} \cdot \omega_{in} \cdot C_{load} \tag{3.28}$$

As detailed in Equation 3.28, a variation in V_{out} and/or in the input frequency will produce a variation in the g_m, meaning that $g_m = \sqrt{\frac{2\mu_n C_{ox} W(I+i_L)}{L}}$ is amplitude and frequency dependent. Therefore, the overall circuit distortion is going to be increased [20].

One approach of reducing output current variations is to substantially increase the bias current I compared with i_L. As a result, the channel current will be less sensitive to a variation of i_L [21].

However, short-channel devices do not have a strong suppression ability to the non-linearity because their intrinsic gain is no more than 40 dB [8]. Furthermore, section 3.8 will introduce another way to mitigate this problem.

3.1.7 Source Follower with a Current Source

As discussed in 3.1.6.1, one way to alleviate the dependence of I_D on the DC input level is to replace the resistor R_S with a constant current source, as shown in Figure 3.12. Additionally, the bulk and source terminals are connected to eliminate the body effect.

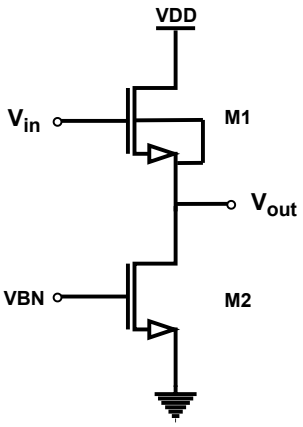


Figure 3.12: SF with a current source

The transfer function of this topology can be described as

$$TF(s = j\omega) = \frac{g_{m1} + sC_{gs1}}{g_{m1} + \frac{1}{R_{ds1}//R_{ds2}} + s\left(C_{gs1} + C_{db2}\right)} \tag{3.29}$$

Equation 3.29 demonstrates the DC gain, the zero, and the output pole. The theoretical equations for all the involved quantities are displayed in Table 3.2.

Table 3.2: SF with current source theoretical analysis

A_{DC}	R_{out}	ω_Z	ω_p	$\overline{V_{n,in}^2}$	ΔV_{out}
$\frac{1}{g_{m1}}$	$\frac{g_{m1}}{g_{m1}+\frac{1}{R_{ds1}//R_{ds2}}}$	$-\frac{g_{m1}}{C_{gs1}}$	$-\frac{g_{m1}+g_{ds1}+g_{ds2}}{C_{gs1}+C_{db2}}$	$4KT\gamma\left(\frac{1}{g_{m1}}+\frac{g_{m2}}{g_{m1}^2}\right)$	$V_{DD}-2V_{DS,sat}$

Table 3.2 illustrates the output resistance from SF with current source configuration, which is equal to $\frac{1}{g_{m1}}$ instead of $\frac{1}{g_{m1}+g_{mb1}}$. As discussed in previous sections, connecting the bulk and source terminals can improve the linearity. Nevertheless, the output resistance is increased [15], which heavily affects the bandwidth.

Unfortunately, the output resistance from this topology is too high for an input buffer [18]. To overcome the limitations due to the resistance, large bias current and W dimensions can be used. As a result, area and power consumption will increase drastically [18, 22].

From Table 3.2 it can be seen that noise can be minimized by using a large g_m for transistors processing the signal (M1) and a lower g_m for transistors acting as current sources (M2).

3.2 Cascode Source Follower

The cascode SF in Figure 3.13 shows higher linearity than the Basic SF by fixing V_{GS} of M3 through the current source created by the transistors M4 and M5. In addition, the variation of V_{sb2} with the input signal is minimized [23, 24], see Equation 3.30.

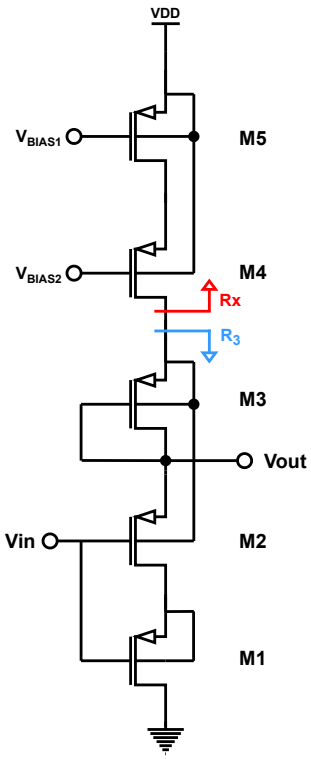


Figure 3.13: Cascode SF

Trying to keep V_{sb_2} fixed is not the only thing that improves the linearity. The potential V_{DS2} is approximately constant, meaning that a variation in the output signal will be absorbed by the potential V_{DS1} [23]. In other words, M1 improves the linearity by "bootstrapping" V_{DS2}.

$$R_3 = \frac{1}{g_{m3} + g_{ds3}} \qquad R_x = R_{ds4} + R_{ds5} + g_{m4} \cdot R_{ds4}$$
$$V_{sb_2} \approx \lim_{R_x \to \infty} \frac{R_3}{R_3 + R_x} \approx 0 \tag{3.30}$$

The transfer function can be expressed as

$$FT(s = j\omega) \approx \frac{s^2 \cdot C_{gs1} \cdot C_{gs2} + s \cdot \left(C_{gs1} \cdot g_{m2} + C_{gs2} \cdot g_{m1}\right) + g_{m2} \cdot (g_{m1} + g_{ds1})}{s^2 \cdot C_{gs1} \cdot C_{gs2} + s \cdot \left[C_{gs1} \cdot g_{m2} + C_{gs2} \cdot g_{m1}\right] + (g_{m1} + g_{ds1}) \cdot g_{m2}} \tag{3.31}$$

where the DC gain is equal to

$$A_{DC}(s=0) \approx \frac{g_{m2} \cdot (g_{m1} + g_{ds1}) + g_{ds2} \cdot g_{m1}}{(g_{m1} + g_{ds1}) \cdot g_{m2} + g_{ds2} \cdot g_{m1}} \tag{3.32}$$

The output resistance, the output pole, and the output swing are approximately equal to

$$R_{\text{out}} \approx \frac{1}{g_{m2}} \quad \omega_{pout} \approx -\frac{g_{m2}}{C_{load}} \quad \Delta V_{out} \approx V_{DD} - 5 \cdot V_{DS,SAT} \tag{3.33}$$

As a final point, this topology has a large input capacitance that reduces the bandwidth, a high number of MOS transistors contributing to noise, and a low output swing [25].

3.3 Cascade Source Follower

The Cascade Source Follower (CSF) is a two-stage configuration (see Figure 3.14), where each stage is a Basic SF. A two-stage configuration can increase the linearity by improving the isolation [26].

As stated in section 3.1, the Basic SF has a DC level-shift equal to V_{GS} that reduces the input swing. The cascade SF topology uses two complementary SF to reduce the DC output offset that is equal to $V_{SG_{p2}} - V_{GS_{n1}}$ [27]. However, this approximately doubles the area and increases noise.

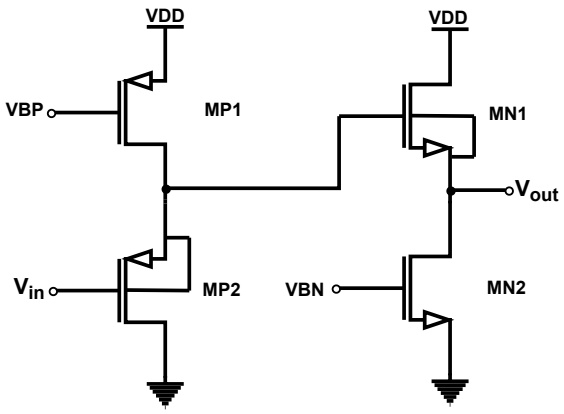


Figure 3.14: Cascade SF

Taking into account the channel length modulation and eliminating the body effect, the transfer function is as follows:

$$TF \approx \frac{s^2 C_{gsn1} C_{gsp2} + s\left(C_{gsn1} g_{mp2} + C_{gsp2} g_{mn1}\right) + g_{mp2} g_{mn1}}{s^2 C_{gsn1} C_{gsp2} + s\left[C_{gsn1} g_{mp2} + C_{gsp2} g_{mn1}\right] + \left(g_{mp2} + g_{dsp}\right) g_{mn1} + g_{mp2} g_{dsn}} \tag{3.34}$$

where the DC gain is equal to

$$A_{DC}(s=0) \approx \frac{g_{mp_2} \cdot g_{mn1}}{g_{mp_2} \cdot g_{mn1} + g_{mp_2} \cdot g_{dsn} + g_{dsp} \cdot (g_{mn1} + g_{dsn})} \tag{3.35}$$

Note: $g_{dsn} = g_{dsn1} + g_{dsn2}$ and $g_{dsp} = g_{dsp1} + g_{dsp2}$.

The output resistance, the output pole, and the output swing are approximately equal to

$$R_{\text{out}} \approx \frac{1}{g_{mn1}} \quad \omega_{pout} \approx -\frac{g_{mn1}}{C_{load}} \quad \Delta V_{out} \approx V_{DD} - 2 \cdot V_{DS,SAT} \tag{3.36}$$

The offset is zero only if MP1 and MP2 are considered to be ideal current sources, forcing the potential difference between the gate and the source to be constant and independent of the input signal. Moreover, for zero offset to hold no mismatch or variation in the components can be present. It seems impossible in practice because there will always be variations in PVT [27].

3.4 Flipped Source Follower

The name Flipped Source Follower (FSF) comes from the fact that the drain of transistor M1 is connected to a "flipped" DC current (I_{BIAS}) instead of V_{DD} like the Basic SF, as displayed in Figure 3.15 [28].

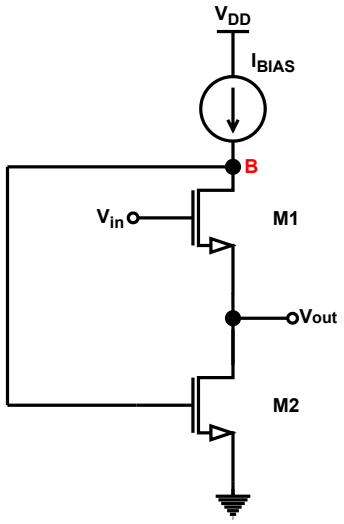


Figure 3.15: Flipped Voltage Follower

FSF provides two improvements comparing to the previous architecture as a negative voltage feedback loop is formed by the drain of M1 and the gate of M2. Firstly, the linearity is improved since the feedback loop sets the drain current approximately constant and independent of the input signal. Secondly, there is a reduction in output resistance [29–32]. On the other hand, the loop causes a low output swing and low frequency pole [12].

The TF is equal to

$$TF(s) \approx \frac{s^2 \cdot C_{gs1} \cdot C_{gs2} + s \cdot \left(C_{gs2} \cdot g_{m1}\right) + g_{m1} \cdot g_{m2}}{s^2 \cdot C_{gsn1} \cdot C_{gsp2} + s \cdot \ C_{gs2} \cdot (g_{m1} + g_{mb1}) + g_{m2} \cdot (g_{m1} + g_{mb1}) + g_{ds1} \cdot g_{m2}} \tag{3.37}$$

where the DC gain is equal to

$$A_{DC} \approx \frac{g_{m1} \cdot g_{m2}}{g_{m2} \cdot (g_{m1} + g_{mb1}) + g_{ds1} \cdot (g_{m2} + g_{ds2})} \tag{3.38}$$

Once more, if the channel length modulation and the body effect are neglected, the DC gain is one [33].

The output pole and the output swing are approximately equal to

$$\omega_{\text{out}} \approx \frac{1}{R_{\text{out}} \cdot C_{\text{out}}} = \frac{1}{\frac{1}{(g_{m1}+g_{mb1})\cdot g_{m2}\cdot R_{ds1}} \cdot C_{load}} \qquad \Delta V_{out} \approx V_{DD} - 3V_{DS,sat} \tag{3.39}$$

It must be emphasized that the feedback loop creates a new pole in node B, the pole can be expressed as

$$\omega_{\text{B}} \approx \frac{1}{R_{\text{ds1}}//R_{\text{BIAS}} \cdot \left(C_{\text{gs2}} + C_{\text{BIAS}}\right)} \tag{3.40}$$

where R_{BIAS} and C_{BIAS} are resistance and capacitance from the bias current, for example, a MOS transistor. The bias component values cause a reduction of bandwidth by introducing a low-frequency pole.

3.5 Super Source Follower

In the context of conventional SF topologies for low-speed applications, the Super Source Follower (SSF) is the best architecture [22]. It has a higher output swing than FSF [31] while maintaining high linearity and low output resistance.

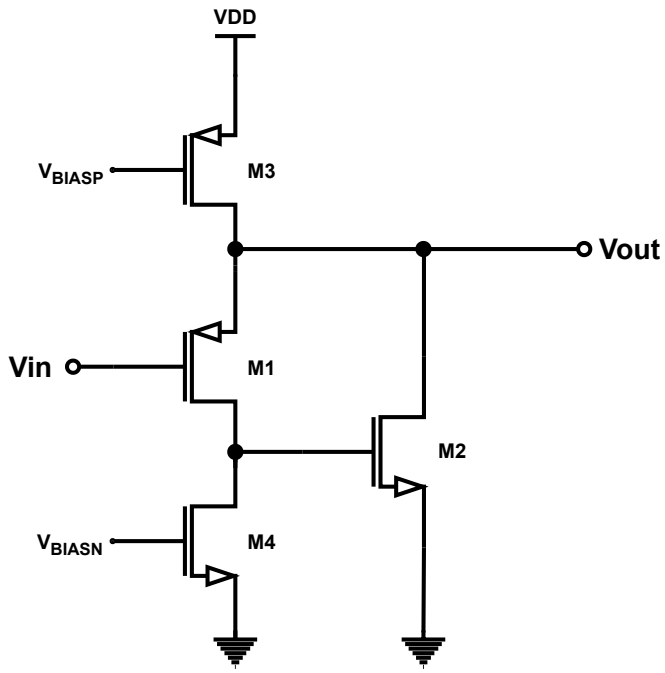


Figure 3.16: Super Source Follower

Considering transistors M3 and M4 ideal current sources, the TF of the buffer can be given by:

$$TF(s) \approx \frac{s^2 \cdot C_{gs1} \cdot C_{gs2} + s \cdot \left(C_{gs2} \cdot g_{m1} + C_{gs1} \cdot g_{ds1}\right) + g_{m2} \cdot g_{m1}}{s^2 \cdot C_{gs1} \cdot C_{gs2} + s \cdot C_{gs2} \cdot (g_{mb1} + g_{m1}) + g_{ds1} \cdot g_{m2} + g_{m2} \cdot (g_{mn1} + g_{mb1})} \tag{3.41}$$

The DC gain is

$$A_{DC} \approx \frac{g_{m1} \cdot g_{m2}}{g_{m2} \cdot (g_{m1} + g_{mb1}) + g_{ds1} \cdot (g_{m2} + g_{ds2})} \tag{3.42}$$

The output pole and the output swing are equal to

$$\omega_{\text{out}} \approx \frac{1}{R_{\text{out}} \cdot C_{\text{out}}} = \frac{1}{\frac{1}{(g_{m1}+g_{mb1}) \cdot g_{m2} \cdot R_{ds1}} \cdot C_{load}} \qquad \Delta V_{out} \approx V_{DD} - 2V_{DS,sat} \tag{3.43}$$

The negative voltage feedback through M2 improves the linearity and reduces the output resistance but may not be stable in all cases [34]. In addition, like FSF topology, the SSF introduces a low-frequency pole located at the gate of M2.

In literature, approaches related to the SSF are given, for instance, the class AB SSF in [35] and the modified SSF in [18]. The first paper uses an intermediate stage, and the second uses the QFG (Quasi-Floating Gate) technique to reduce the output resistance.

3.6 Source Follower with Current Feedback

The basic source follower with current feedback is shown in Figure 3.17. The feedback loop maximizes the linearity of M2 by using a cascode current mirror. The cascode current mirror absorbs any signal-dependent increase in current drawn by M2 [36]. Thus, if V_{in} increases, I_{REF} will decrease due to the decrease in voltage V_{SG} of M3. Consequently the current I_{out} will drop because I_{out} is replica of I_{REF}, apart from a scaling factor (see Equation 3.44), thus increasing the output voltage (V_{out}).

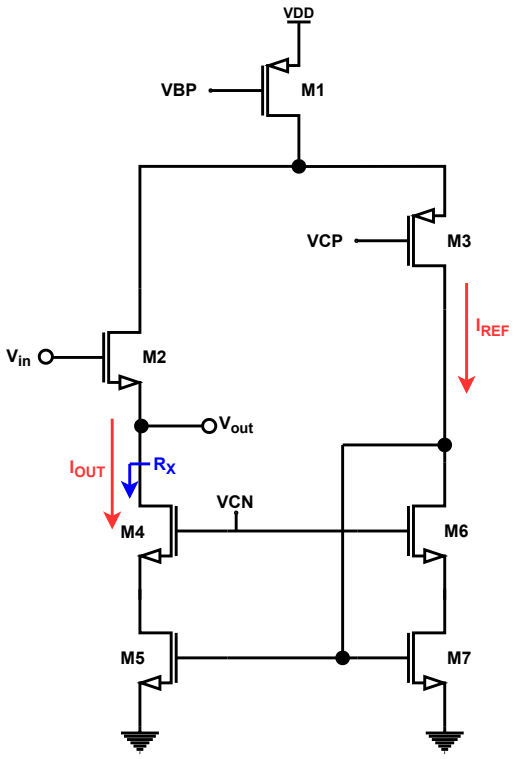


Figure 3.17: Source Follower with Current Feedback

$$I_{out} \approx \frac{\left(\frac{W}{L}\right)_{M4}}{\left(\frac{W}{L}\right)_{M6}} \times \frac{\left(\frac{W}{L}\right)_{M5}}{\left(\frac{W}{L}\right)_{M7}} \times I_{REF} \tag{3.44}$$

As discussed in the previous sections, a voltage feedback loop can increase the linearity but could also introduce stability problems and create low-frequency poles. On the other hand, a current feedback loop can improve the linearity without introducing low-frequency poles as the voltage loop. However, the current loop also generates issues with stability as the voltage loop.

The DC gain is the same as the SF gain

$$A_{DC} \approx \frac{g_{m2}}{g_{m2} + g_{mb2} + g_{ds2}} \tag{3.45}$$

The output resistance, the output pole, and the output swing are approximately equal to

$$R_{\text{out}} \approx \frac{1}{g_{m2}} \quad \omega_{pout} \approx -\frac{g_{m2}}{C_{load}} \quad \Delta V_{out} \approx V_{DD} - 4 \cdot V_{DS,SAT} \tag{3.46}$$

One can notice that a trade-off between noise and speed is present in the equations [36]. The output current has to increase substantially to increase bandwidth. In other words, the mirror ratio between M4/M5 and M6/M7 has to be huge. However, to escalate the mirror ratio, the MOS 4 and 5 have to be large devices, thus increasing the noise. Additionally, if I_{out} is much larger than I_{REF}, the current feedback sensitivity will decrease, as a consequence, degrading the linearity.

3.7 Differential Source Follower

This section describes two of the conventional SF architectures in differential mode, the differential Source Follower and the differential Super Source Follower.

In most cases, it is preferable to use a differential operation than a single-ended operation.

The advantages are:

- Double input swing.
- Higher CMRR.
- Higher linearity, high IIP2.
- Lower NF (Noise Figure).
- Immunity to interferers (cross-talk).

The disadvantages are:

- Double area.
- Double power consumption, with the same SNR as single-ended.

3.7.1 Differential Source Follower with Cross-couple Pair

The main advantage of Differential Source Follower (DSF) over SF is the cancellation of the even harmonics. Nonetheless, most circuit parts have to be duplicated, leading to area and power consumption increase [37]. Moreover, a differential structure can reduce noise and miss-match errors [38].

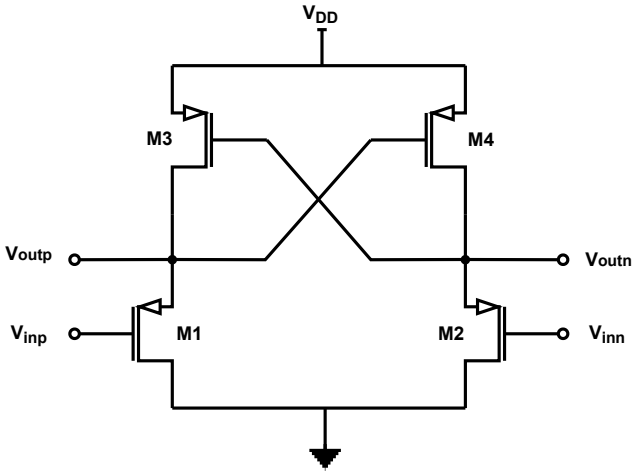


Figure 3.18: Differential Source Follower with cross-couple pair

If any miss-match between M1, M2, and M3, M4 is considered, the DC gain is equal to

$$A_{DC} \approx \frac{g_{m1,2}}{g_{m1,2} + g_{mb1,2} + g_{ds1,2} + g_{ds3,4}} \tag{3.47}$$

On the other hand, if there is some miss-match between the transistors, the common mode rejection ratio is approximately:

$$CMRR \approx \frac{1}{2} \cdot \frac{g_{m1} + g_{m2}}{g_{m1} \cdot (g_{m2} + g_{mb2} + g_{ds2}) - g_{m2} \cdot (g_{m1} + g_{mb1} + g_{ds1})} \tag{3.48}$$

The ideal case is when there is no miss-match in components, meaning that the CMRR is infinite.

The output resistance, the output pole, and the output swing are approximately equal to

$$R_{\text{out}} \approx \frac{1}{g_{m1,2}} \quad \omega_{pout} \approx -\frac{g_{m1,2}}{C_{load}} \quad \Delta V_{out} \approx V_{DD} - 2 \cdot V_{DS,SAT} \tag{3.49}$$

It is important to recall that although this architecture improves linearity, its output resistance is still too high.

3.7.2 Differential Super-source Follower with Cross-couple Pair

The differential SSF combined with the cross-coupled pair proposed in [38] is presented in Figure 3.19. Its main advantage over the SSF is DC gain higher than one, and output resistance lower than $\frac{1}{g_m}$ since there is the feedback loop through M2. However, increasing the area causes limitations in bandwidth [38].

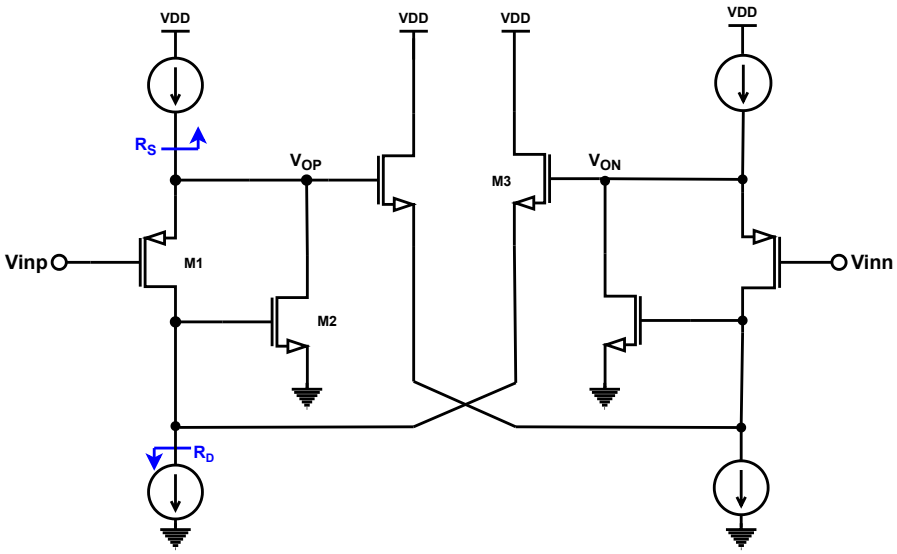


Figure 3.19: Differential Super Source Follower with cross-couple pair

The DC gain is

$$A_{DC} \approx \frac{g_{m1}R_S\left(1+g_{m2}R_D\right)}{1+\left[g_{m1}+g_{m2}R_D\left(g_{m1}-g_{m3}\right)\right]R_S} \tag{3.50}$$

The output pole and the output swing are equal to

$$R_{\text{out}} \approx R_S \left\| \frac{1}{g_{m1}\left(1+g_{m2}R_D\right)} \right\| \frac{-1}{g_{m3}\left(g_{m2}R_D\right)} \qquad \Delta V_{out} \approx V_{DD} - 2V_{DS,sat} \tag{3.51}$$

3.8 Replica Capacitance Assisted Buffer

As discussed in subsubsection 3.1.6.3, the buffer interaction with its load Z_L and its driver Z_s is one of the main sources of non-linearity. The output current variation due to the frequency variation is the dominant non-linearity at higher frequencies [6]. In other words, g_m is frequency dependent [39].

One approach to alleviate this problem is to increase the load impedance or/and the transconductance, leading to higher power dissipation [9, 39]. Another way is to implement the replica capacitance assisted buffer, as shown in Figure 3.20.

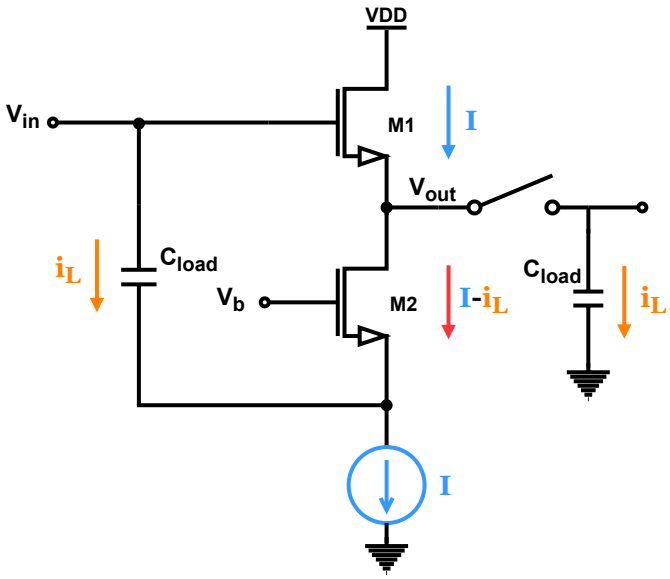


Figure 3.20: Replica capacitance assisted buffer

This approach improves the linearity without a massive increase in bias current [2].

The replica capacitance buffer adjusts the drain current equal to the bias current (I) by introducing a "replica" C_{load} in the input node. The input capacitance C_{load} will compensate the AC current going to the load, thus decreasing the current variations in the SF device M1 [7, 39].

The gain DC is the same as the SF gain

$$A_{DC} \approx \frac{g_{m1}}{g_{m1} + g_{mb1} + g_{ds1}} \tag{3.52}$$

The output resistance, the output pole, and the output swing are approximately equal to

$$R_{\text{out}} \approx \frac{1}{g_{m1}} \quad \omega_{pout} \approx -\frac{g_{m1}}{C_{load}} \quad \Delta V_{out} \approx V_{DD} - 3 \cdot V_{DS,SAT} \tag{3.53}$$

Although the replicated capacitance increases, it also decreases input impedance [2] degrading the isolation (reverse gain) and introducing a low-frequency input pole. Furthermore, a higher input capacitance can lead to a challenging "drive" from the previous stage.

3.9 Capacitance Level-shifter Assisted Buffer

As mentioned in the previous section, the output current variation is the dominant source of non-linearity at higher frequencies while at low frequencies the channel length modulation is the dominant non-linearity [6, 9, 39].

The Capacitance level-shifter assisted buffer shown in Figure 3.21 tries to improve the linearity in all spectrum by implementing the "replica capacitance" and the V_{DS1} "bootstrapping". In other words, this topology forces the drain voltage of M1 to follow the

input by "bootstrapping" A_{in} to A_2 using a switch-capacitor level-shifting circuit, formed by C_1, C_2 and the source follower M3.

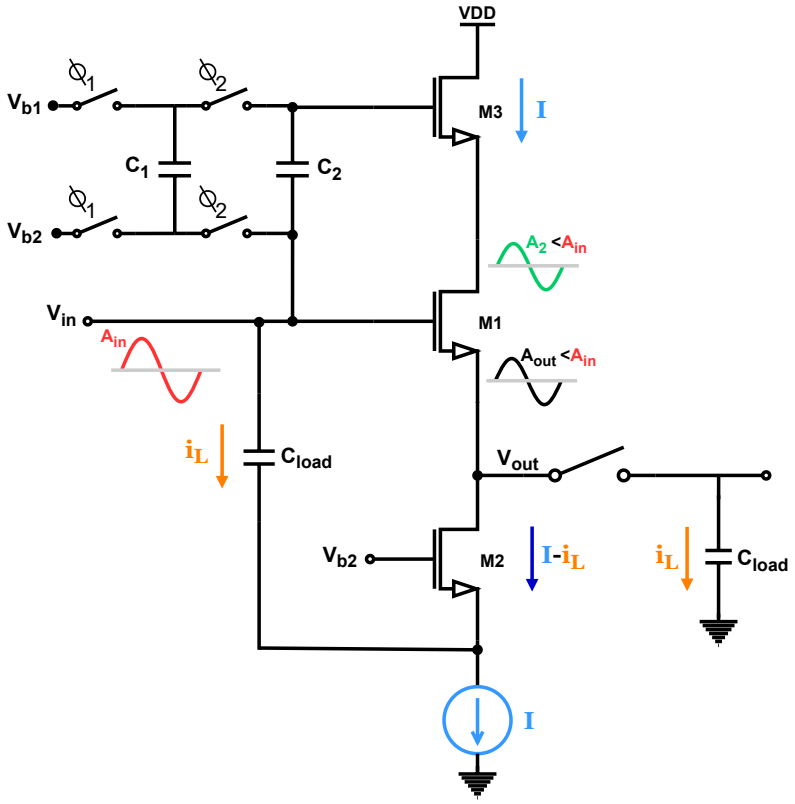


Figure 3.21: Capacitance level-shifter assisted buffer

It has to be noted that the channel length modulation is only eliminated if $A_{in} = A_2 = A_{out}$, meaning that the SF M3 DC gain is one and there is no signal attenuation due to C_2, in practice impossible to achieve.

The DC gain and the output resistance are the same as the replica capacitance assisted buffer, but the output swing is lower and is equal to

$$\Delta V_{out} \approx V_{DD} - 4 \cdot V_{DS,SAT} \tag{3.54}$$

Moreover, the V_{DS1} "bootstrapping" is done using a nonlinear circuit, for example, a switch controlled by Φ_1 and Φ_2, generating an undesirable spur in the output spectrum [2].

3.10 RC Assisted Buffer

The RC assisted buffer has the same goal as the switch-capacitor level-shifting circuit in the "Capacitance level-shifter assisted buffer". As displayed in Figure 3.22, the capacitance Cap couples the AC signal to M3 and the series resistor supports the DC bias of M3. Replacing the switch-capacitor with a RC circuit improves the linearity by eliminating an undesired spur in the output spectrum [7].

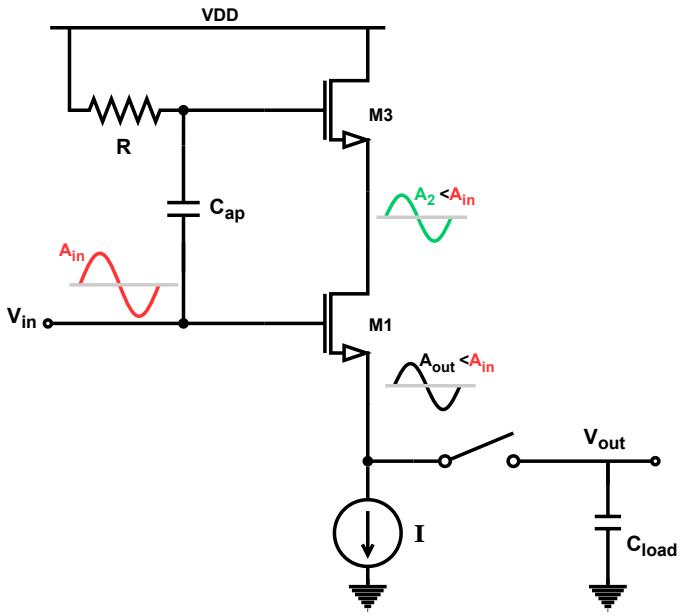


Figure 3.22: RC assisted buffer

The DC gain and the output resistance are the same as the Capacitance level-shifter assisted buffer, but the output swing is higher and is equal to

$$\Delta V_{out} \approx V_{DD} - 3 \cdot V_{DS,SAT} \tag{3.55}$$

However, this topology does not attempt to minimize the output current variation by decreasing input bandwidth and output swing. It tries to reduce the channel length modulation by using the capacitance Cap, which inherently reduces the input bandwidth [40]. In addition, the cascode transistor M3 can improve the Power-Supply Rejection Ratio (PSRR) by increasing the resistance seen from the supply terminal.

The key trade-off here is linearity versus bandwidth created by the RC circuit, this trade-off will be studied and simulated in chapter 4.

3.11 Push-pull

Nowadays, a widely used architecture is the Push-pull source follower [5, 11, 41], as shown in Figure 3.23. The Push-pull is just a RC assisted buffer with a complementary branch.

The circuit operates by pushing the current through NMOS devices to the load when input rises and pulling the current through PMOS devices when signal falls. Because of this behavior, this topology is called a "Push-pull".

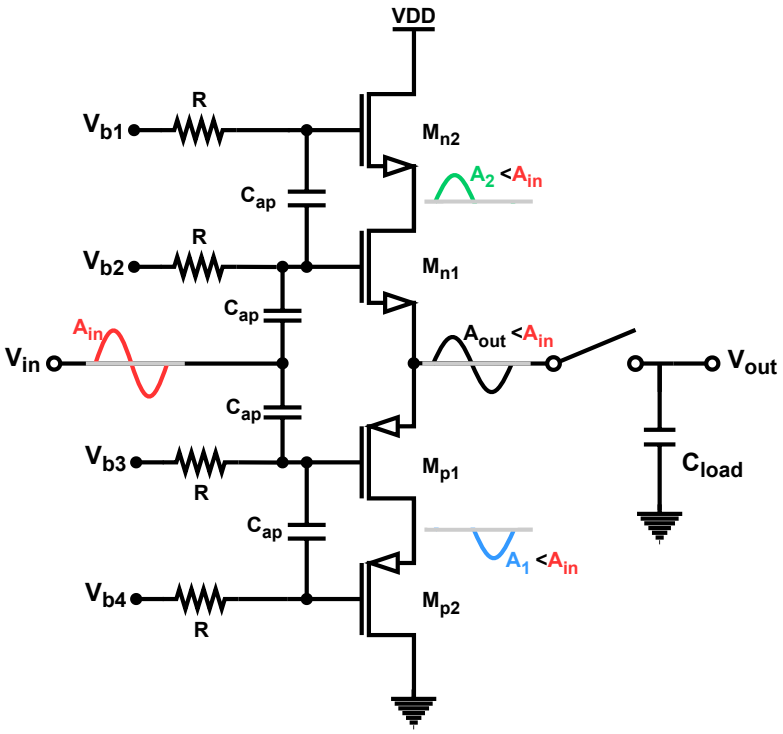


Figure 3.23: Push-pull

The complementary branch improves the DC power consumption [6] by reducing the output resistance [7]. On the other hand, to couple the AC signal to M_{n1} and M_{p1}, two additional $Caps$ are needed leading to a bandwidth reduction. Consequently, there is a trade-off between gain and bandwidth.

The DC gain is zero, and the output resistance, the output pole, and the output swing are approximately equal to

$$R_{\text{out}} \approx \frac{1}{2 \cdot g_{m1}} \quad \omega_{pout} \approx -\frac{2 \cdot g_{m1}}{C_{load}} \quad \Delta V_{out} \approx V_{DD} - 4 \cdot V_{DS,SAT} \tag{3.56}$$

As detailed in Equation 3.56, term two (highlighted in red) allows us to decrease the output resistance and shift the output pole to higher frequencies without a colossal increase in current, compared with configurations where the output resistance is approximately $\frac{1}{g_m}$.

3.12 Conclusion

With SF-based topologies analyzed it can be argued that for high bandwidth, it is better to use small intrinsic capacitances, for instance, small-scale transistors ($L = L_{min}$) and a lower number of MOS. A low output resistance is required to decrease power dissipation and increase bandwidth. Lastly, to improve linearity is helpful to have a high output swing and a linearization technique.

Table 3.3 has a summary of SF topologies (not all) in terms of output resistance, transistors number, input capacitance C_{in}, output swing, and the linearization technique used.

Table 3.3: SF topologies summary

Topology	**SF**	**CSF**	**FSF**	**SSF**	**SF Current loop**	**Replica capacitance**	**RC assisted**	**Push-Pull**
MOS Number	2	4	3	4	7	3	3	4
Rout	$\frac{1}{gm}$		$\frac{1}{gm \cdot gm \cdot R_{ds}}$		$\frac{1}{gm}$			$\frac{1}{2 \cdot gm}$
Cin	Low		Medium	High	Low	High	High	Very High
Output Swing	$-2V_{DSAT}$		$-3V_{DSAT}$	$-2V_{DSAT}$	$-4V_{DSAT}$	$-3V_{DSAT}$		$-4V_{DSAT}$
Linearity technique	None		Voltage feedback		Current feedback	Replica capacitance	V_{DS} "bootstrap"	

As detailed in Table 3.3 is possible to see that the FSF and the SSF have the lowest output resistance but they use voltage feedback that could introduce stability problems and low-frequency poles. The current feedback technique does not introduce low frequency poles but a loop gain is small at radio frequency, meaning that the current loop has almost no effect at high frequencies.

The Replica capacitance and the RC assisted buffer have a high input capacitance that lowers the input bandwidth. Nonetheless, both configurations have a linearization technique that could work in high frequencies.

The replica capacitance value is fixed by the sampling capacitance, which does not give much design freedom. In contrast, the capacitance Cap from the RC assisted and the Push-pull buffer can be a design parameter. In addiction, the Push-pull is the buffer with the lowest output resistance after FSF and the SSF.

Finally, the basic SF is the buffer with the lowest input capacitance but without any linearization technique.

4

Best Candidates Study and Simulation

In this chapter the simulation results of the previously discussed topologies (Basic SF, the RC assisted buffer, the Basic push-pull, and the Push-pull) are provided. The topologies are evaluated and compared on their DC power consumption, linearity, DC gain, noise, while also investigating the maximum achievable bandwidth.

It is important to note that the reported results are pre-layout/schematic and not post-layout results. The simulator used is Spectre Circuit Simulator from Cadence and the software Matlab.

4.1 Simulation Constraints and Performance Metrics

In order to have fair comparisons between topologies, simulations are performed with the following constraints:

Table 4.1: Constraints

Technology	TSMC 7nm FinFET (Thick gate devices)
Channel length	L_{min} = 72 nm
Number fingers	10
Number fins	4
Sampling capacitance	1 pF
Voltage supply	1.8 V
Flying capacitance parasitics	0.1· Cap
ESD protection	Standart TMSI
Input amplitude in transient analysis	0.25 V
AC magnitude in AC analysis	0.5 V
Carrier frequency	100 MHz up to 25GHz
Two tone spacing	19.53 MHz

It must be emphasized that because of ESD protection and reliability concerns, for instance, no need for secondary protection, the thick oxide devices are primarily used in the design ("nch_18ud12_dnw_mac" and "pch_18ud12_mac") instead of thin oxide devices.

Although, the use of thin gate devices improves the bandwidth (L_{min} = 8 nm), the output swing (smaller V_{th}), and the power consumption, creates reliability and robustness issues.

4.1.1 Simulation Test Bench

The used simulation test bench is represented in Figure 4.1. The test bench implements a differential operation with 50 Ω resistance and a standard TMSI protection. The protection consists of diodes meant for static electricity (ESD) countermeasures. Diodes absorbs the above rails voltage coming from external terminals, thus protecting the devices. Moreover, they are ideal for consuming and suppressing static electricity or short-pulse voltage.

Every simulated transistor has 10 fingers, 4 fins, 72 nm length, and every topology drives 1 pF sampling capacitance.

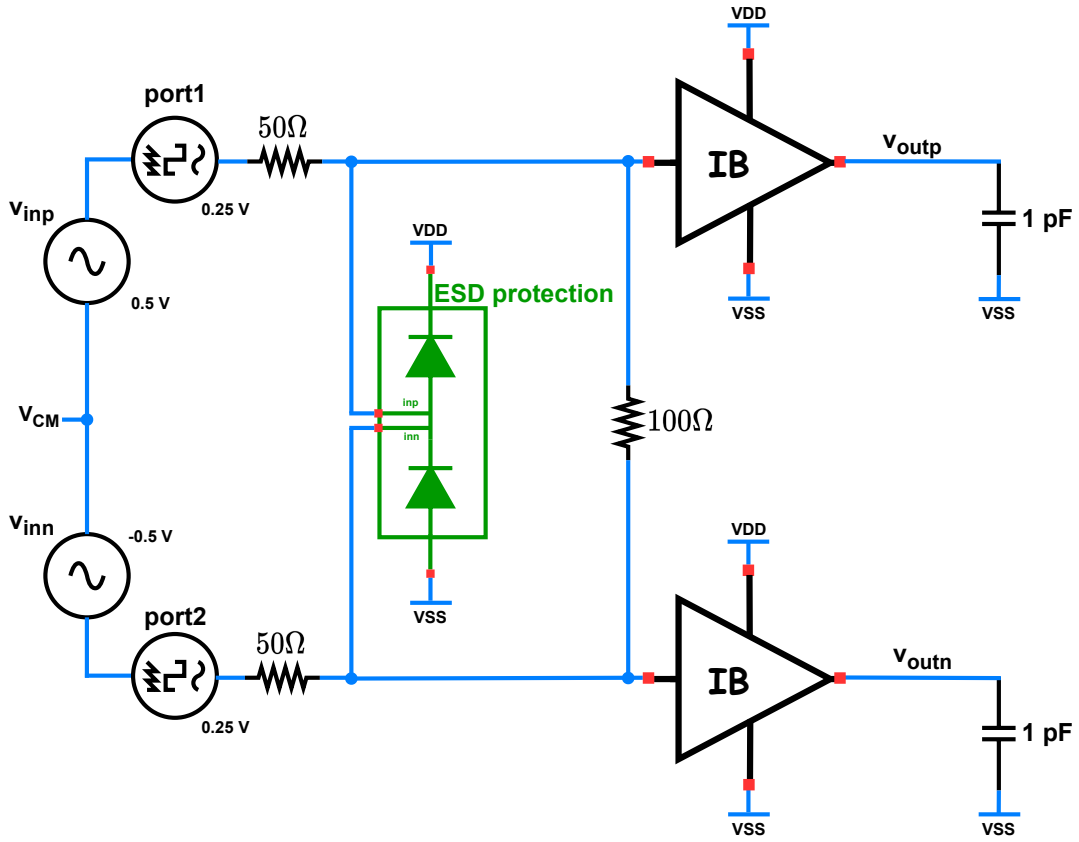


Figure 4.1: Simulation test bench

4.1.2 Performance Metrics

The performance metrics are DC gain, DC power, the third order input intercept point (IIP3), the fractional third harmonic distortion (HD3) and the input-referred noise.

To obtain the DC gain, the output common mode voltage, and the DC power consumption a DC simulation is performed. The DC simulation allows to verify and tune the DC operation point and see if every transistor is in saturation. Noise analysis determines the

input-referred noise, and through an AC simulation (small-signal analysis) the bandwidth is calculated. The DC gain is observed at 100 MHz, and the bandwidth is the frequency where the DC gain drops 3 dB compared to the gain (half of the power).

A transient simulation can provide measures of linearity, but this analysis is complex, and because of that, the section below briefly describes the theory behind HD3 and IM3. Additionally, explains how to estimate IIP3 from IM3.

4.1.3 Harmonic Distortion

A system that is nonlinear and depends on the past values of its input/output is called nonlinear time-variant system, for instance, a MOSFET. Such a system introduce distortion, which means if excited with a sinusoidal signal, the output spectrum will manifest frequency components that are integer multiples ("harmonics") of the input frequency. The existence of harmonics can be proven using the Taylor expansion; to simplify the analysis a memoryless (time-invariant) system is considered.

If the input signal is a single tone equal to $x(t) = A_{in} \cos \omega_1 t$, the output characteristic can be approximated by:

$$\begin{aligned} y(t) &= \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots \\ &\approx \alpha_1 A_{in} \cos \omega_1 t + \alpha_2 {A_{in}}^2 \cos^2 \omega_1 t + \alpha_3 {A_{in}}^3 \cos^3 \omega_1 t \\ &\approx \frac{\alpha_2 {A_{in}}^2}{2} + \left(\alpha_1 A_{in} + \frac{3\alpha_3 {A_{in}}^3}{4}\right) \cos \omega_1 t + \frac{\alpha_2 {A_{in}}^2}{2} \cos 2\omega_1 t + \frac{\alpha_3 {A_{in}}^3}{4} \cos 3\omega_1 t \end{aligned} \tag{4.1}$$

where the first term is the DC component, the second term is the fundamental frequency (f_1), the third term is the second harmonic ($2 \cdot f_1$), and the last term is third harmonic ($3 \cdot f_1$). These components in the frequency domain are shown in Figure 4.2.

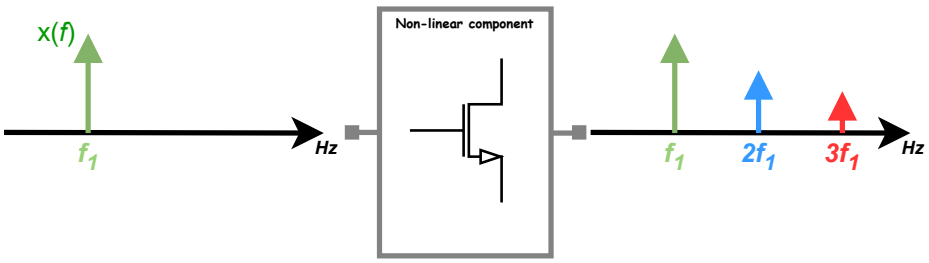


Figure 4.2: Harmonic distortion

To decrease distortion, the power of each harmonic should be minimized. One way to measure the level of distortion due to harmonic components is the metric HD3, which relates the power level of the third harmonic to the fundamental.

HD3 is defined as

$$HD3 = \frac{\text{third harmonic}}{\text{fundamental}} = \frac{1}{4}\left|\frac{\alpha_3}{\alpha_1}\right| {A_{in}}^2 \tag{4.2}$$

Equation 4.2 demonstrates that HD3 is amplitude-dependent.

As detailed in Figure 4.2, the output spectrum exhibits more harmonics than the third harmonic. Nonetheless, in this project "differential" approach is used, consequently the second harmonic is almost eliminated. As a result, only HD3 is reported and not HD2.

4.1.4 Intermodulation Distortion

The previous section discussed the distortion due to a single tone at the input port. Another scenario of interest is when more than one tone appears at the input port.

For example, if two interferers (f_2 and f_3) arrive at the antenna accompanied by a desired signal (f_1), the output spectrum will exhibit harmonics and intermodulation (IM) products. As mentioned above, harmonic components are mainly generated by the system. However, the IM products, for instance, the third-order IM products that are equal to ($2 \cdot f_2 - f_3$ and $2 \cdot f_3 - f_2$), result from mixing/multiplication between the two interferers. Therefore, mixing components can be a problem when the resulting frequency falls into the desired channel (f_1) and corrupts the signal, meaning that $2 \cdot f_2 - f_3$ or $2 \cdot f_3 - f_2$ is equal to f_1. This is the worst-case scenario and is detailed in Figure 4.3.

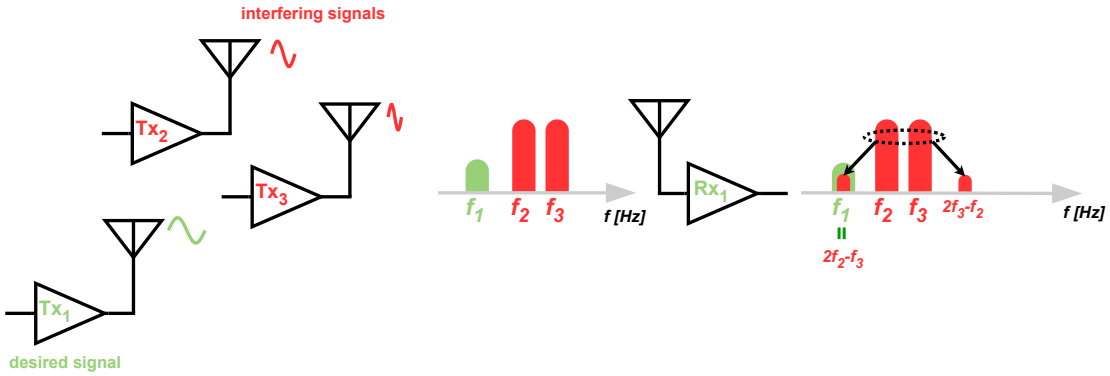


Figure 4.3: Corruption due to third-order intermodulation.

Figure 4.3 shows three users (TX_1, TX_2, and TX_3) that are in the receiver (RX_1) range, and all of them are trying to communicate. Channel f_1 is the wanted signal, and channels f_2 and f_3 are blockers. Due to path loss, the desired signal from TX_1 arrives at the receiver with less power compared to the two interfering signals from TX_2 and TX_3. The "mixing" between the interfering channels f_2 and f_3 creates a component in the same frequency of channel f_1, equal to $f_1 = 2 \cdot f_2 - f_3$, that corrupts the desired signal. Moreover, the level of corruption depends on the power level of this third-order IM product.

One performance metric to measure the level of corruption is third-order IM distortion product (IM3). IM3 is calculated by performing a two-tone test, which is performed by exciting the nonlinear system with two tones of equal amplitude and measuring the difference between the power of a single tone and the third-order IM product.

Mathematically it is possible to demonstrate that if two signals with frequencies f_1 and f_2 are applied to a non-linear system the output spectrum will exhibit two components equal to ($2 \cdot f_2 - f_3$ and $2 \cdot f_3 - f_2$).

For example, $x(t) = A_{in}\cos(\omega_1 t) + A_{in}\cos(\omega_2 t)$ is applied into a circuit, using the Taylor expansion the output characteristic will be equal to

$$\begin{aligned} y(t) =& \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots \\ \approx& \overbrace{\alpha_2 A_{in}^2}^{DC} + \overbrace{\left(\alpha_1 A_{in} + \frac{9}{4}\alpha_3 A_{in}^3\right)\cos\omega_{1,2}t}^{\text{Fundamental}} + \overbrace{\frac{1}{2}\alpha_2 A_{in}^2 \cos 2\omega_{1,2}t}^{2^{\text{nd}}-\text{Harmonic}} + \overbrace{\frac{1}{4}\alpha_3 A_{in}^3 \cos 3\omega_{1,2}t}^{3^{\text{rd}}-\text{Harmonic}} \\ &+ \underbrace{\alpha_2 A_{in}^2 \cos(\omega_2 \pm \omega_1)}_{2^{\text{nd}}\text{-order IMD}} + \underbrace{\frac{3}{4\alpha_3 A_{in}^3 \cos(2\omega_{1,2} \pm \omega_{2,1})}}_{3^{\text{rd}}\text{-orderIMD}} + \dots \end{aligned} \tag{4.3}$$

Note: $\cos\omega_1 \cdot \cos\omega_2 = \frac{\cos(\omega_1+\omega_2)+\cos(\omega_1-\omega_2)}{2}$

The output characteristic in the frequency domain is displayed in Figure 4.4. As shown in the figure, the linearity metric IM3 is the difference between the third-order IM product power and the desired signal power (green tone).

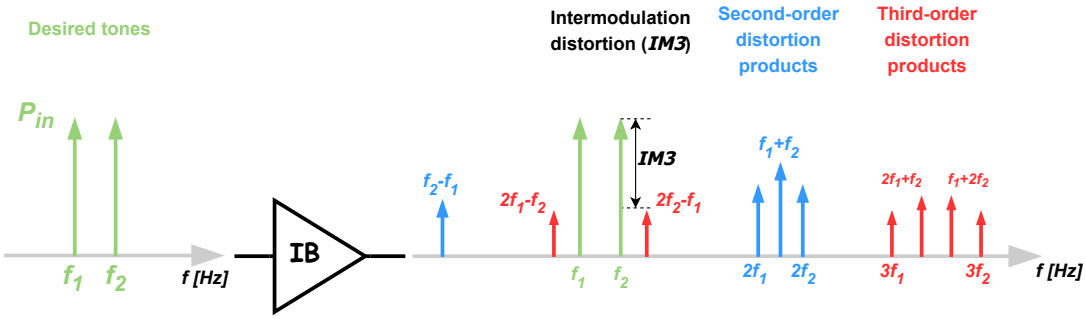


Figure 4.4: Output spectrum in the two-tone test

Even thought two-tone test provides information on several frequency components, only the 3rd order IM product is of interest as it falls into the band. In order words, the other tones can be filtered using a band pass filter.

However, IM3 is hard to specify because it is only a relevant measure when the value P_{in} is given. Luckily, there is the "input third intercept point" (IIP3), which is a measure that is frequency-dependent but amplitude-independent. The IIP3 is the input power level where the third-order IM product power is equal to the fundamental tone power.

IIP3 is obtained from simulations, where the input power is swept until a determination of a point where fundamental tones and 3^{rd} order IM are equal. For eased analysis, the input power is plotted on a log-log scale as then the exponential functions obtained from Taylor expansion appear as straight lines (see Figure 4.5).

The extrapolation of equal amplitudes is only valid for not too high power levels, and not too low power levels because for high values the circuit starts to have gain compression, and for low values, the IM components become comparable with the noise floor leading to inaccurate results.

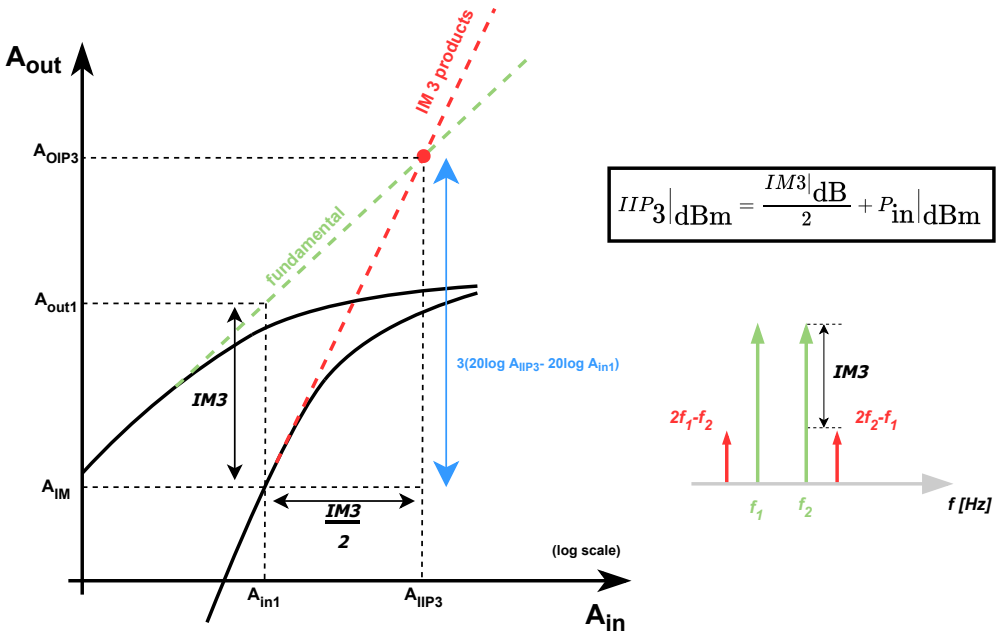


Figure 4.5: Shortcut technique to calculate IIP3 from IM3

Nevertheless, a shortcut technique for IIP3 estimation is usually preferred in order to simplify calculations. As shown in Figure 4.5, the third-order IM products have a slope of magnitude times 3 and the fundamental a slope of single magnitude, meaning that the difference between the two plots is two. With some geometric manipulations it can be shown that

$$IIP_3|_{\text{dBm}} \approx \frac{IM3|_{\text{dB}}}{2} + P_{\text{in}}|_{\text{dBm}} \tag{4.4}$$

Equation 4.4 is the shortcut technique that estimates IIP3 without any extrapolation.

The linearity metric Spurious Free Dynamic Range (SFDR) is more commonly used in ADC metrics than IIP3. Nevertheless, its only possible to calculate SFDR when the receiver sensitivity is know.

4.2 Basic Source Follower

The Basic Source Follower is biased with a simple current mirror and with an ideal amplifier that implements the Common-Mode Feedback (CMFB) to set the DC output voltage at 0.7 V (V_{CM}), as shown in Figure 4.6.

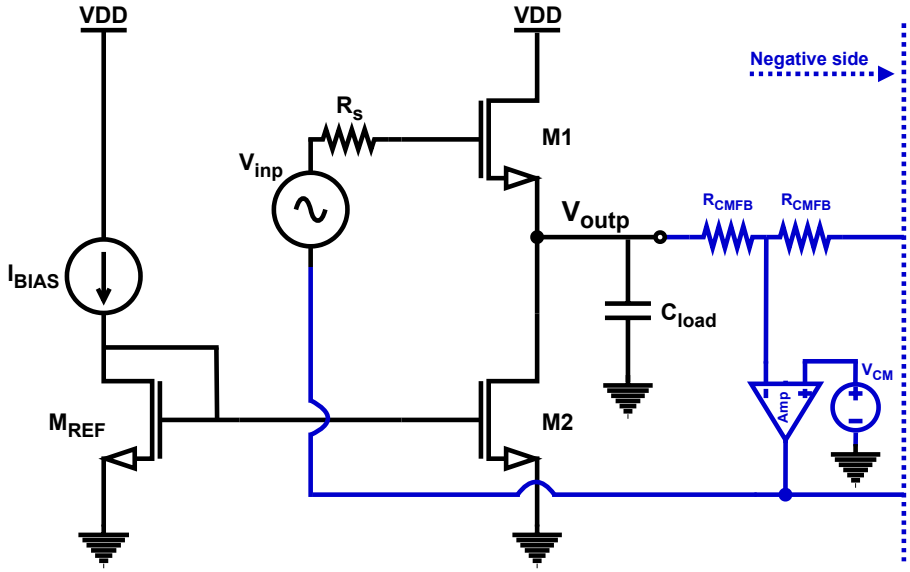


Figure 4.6: Basic SF bias with a current mirror

The R_{CMFB} resistances are enormous for the current in that branch to be almost zero, which means that only the voltage is sensed at that node. Therefore, CMFB circuit senses the output voltage and compares that voltage with a reference, in this scenario 0.7 V, and feeds the result back to the circuit. As a result, CMFB enables the topology to change the current to fix the desired output voltage.

Theoretical analysis for the Basic SF is presented in Table 4.2.

Table 4.2: BSF theoretical analysis

DC gain	$\frac{g_m}{g_m+g_{mb}+g_{ds}}$
Rout	$\frac{1}{g_m+g_{mb}+g_{ds}}$
Zero	$\frac{g_m}{C_{gs1}}$
Output Pole	$\frac{g_m+g_{mb}+g_{ds}}{C_{load}+C_{sb}}$
Input Pole	$\frac{1}{Rs\left[C_{gd}+\frac{C_{gs}(g_{mb}+g_{ds})}{g_m+g_{mb}+g_{ds}}\right]}$
Input referred noise	$4kT\gamma\left(\frac{1}{g_{m1}}+\frac{g_{m2}}{g_{m1}^2}\right)$

BSF does not have many degrees of freedom, only the source follower width (W) and DC current. The SF DC current is a replica of the bias current (I_{BIAS}); I_{BIAS} is equal to 1 mA and M_{REF} multiplier is equal to 3.

4.2.1 Design Strategy and Sizes

As there are not many degrees of freedom, the strategy implemented, was to vary M1 and M2 multipliers. The results from sweeping the width and the DC current in simulation to achieve the maximum bandwidth are plotted in Figure 4.7.

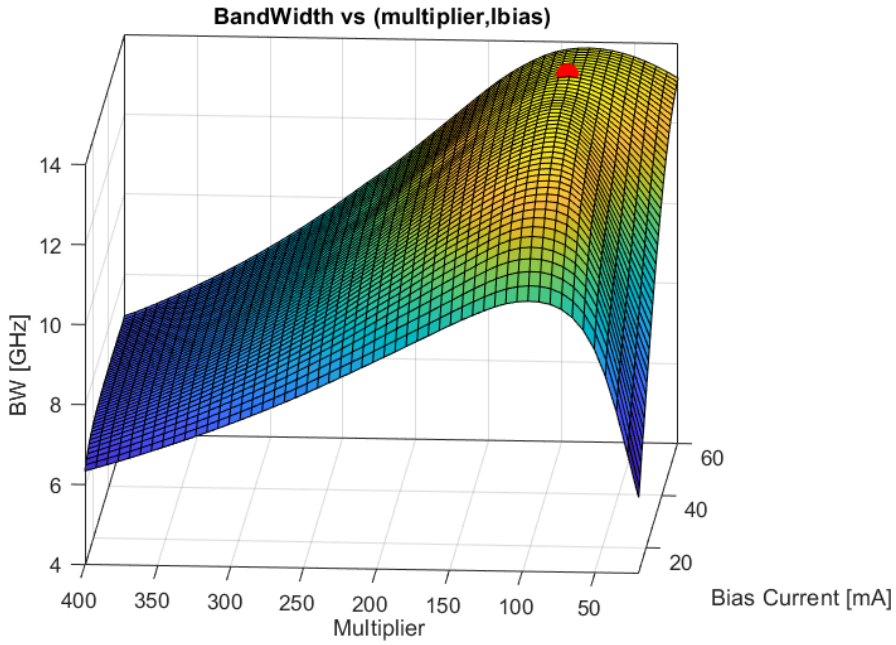


Figure 4.7: SF Maximum Bandwidth

The results show that for maximum bandwidth with an input common mode less than 1.5 V and an output common mode approximately 0.7 V, the SF multiplier (M1) is equal to 90 and the M2 multiplier is equal to 147. This results in a DC current equal to 49 mA (see Equation 4.5).

$$I_{SF} \approx \frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M_{REF}}} \times I_{BIAS} = \frac{147}{3} \times 1mA \tag{4.5}$$

In order to properly analyze the plot from Figure 4.7, one has to remember that there are 2 crucial poles in the circuit: input and output poles. The dominant pole is the one located at lower frequencies - it dictates where the DC gain roll-off begins. Therefore, to maximize the bandwidth the dominant pole has to be at the highest frequency, as shown in Figure 4.8.

Its possible to increase the input and output pole frequency by increasing the transconductance - escalate I_{Bias} or increasing the M1 width. The most reasonable solution is to increase the bias current rather than the width to avoid parasitic capacitance issues - such scaling is also performed in Figure 4.7.

The Figure 4.8 depicts first order bandwidth approximation as zeros and complex poles are neglected, meaning that no overshoot at higher frequencies is present. The equations included in the graph are acquired by Equation 4.6 with RC being time constant.

$$\omega_h \approx -\sum_{i=1}^{n} p_i = \sum_{i=1}^{n} \frac{1}{\tau_i} = \frac{1}{\sum_{i=1}^{n} \frac{1}{RC_i}} \tag{4.6}$$

The key observation here is that the optimum design is reached when the poles coincide at the same frequency. As the input pole is dominating, it is not necessary to

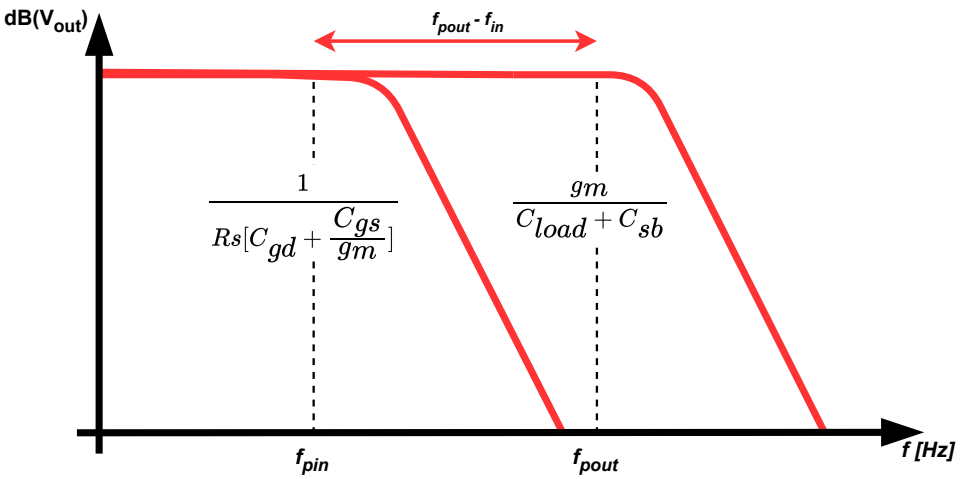


Figure 4.8: Effect of the poles in circuit bandwidth

choose a large bias current to shift the output pole to higher frequencies when the input pole is already dictating the circuit bandwidth, $\omega_{in} \approx \frac{1}{[\frac{C_{gs}}{g_m} + C_{gd}] \cdot Rs}$.

4.2.2 DC Analysis

To obtain a certain DC behavior of the circuit, proper biasing has to be performed, thus the operating point has to be investigated. The DC operating point is displayed in Figure 4.9, all transistors are in saturation, and the output common mode is approximately 0.7 V.

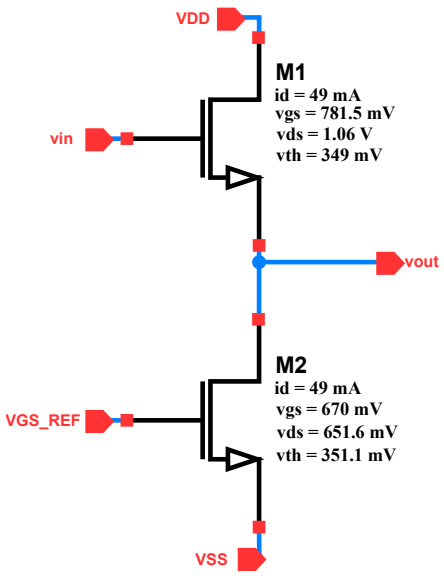


Figure 4.9: BSF DC operating point

It is a fact that this topology consumes a tremendous value of current, 49 mA. Nonetheless, it is a price to pay to obtain high frequencies.

4.2.3 AC Analysis

The AC analysis does not account for any distortion as only small signals are considered. It is a frequency-domain analysis where the derivatives are computed.

The Bode diagram from the BSF is provided in Figure 4.10. The DC gain is flat at low frequencies, and the bandwidth is approximately 13.85 GHz. At this frequency, the DC gain drops 3 dB compared to the initial value.

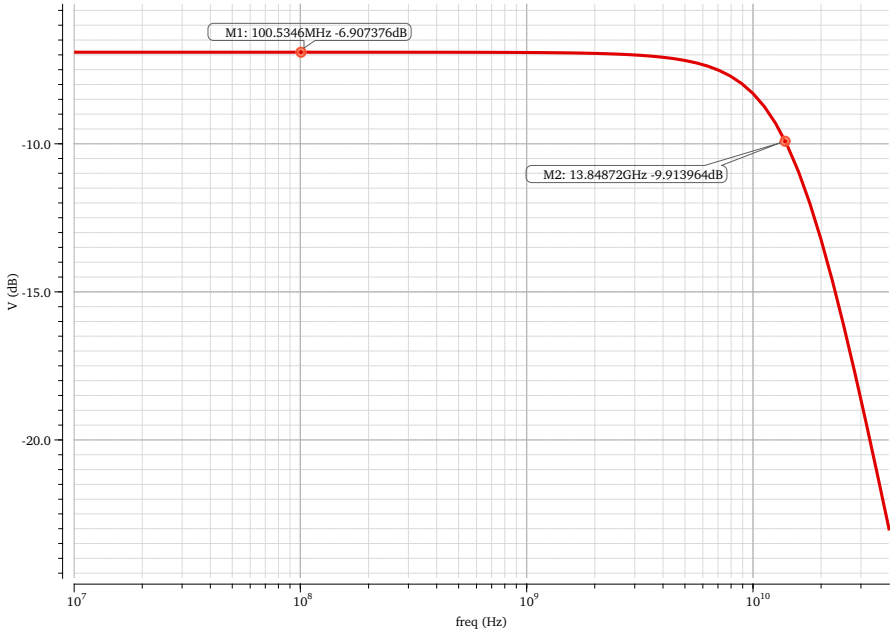


Figure 4.10: BSF frequency response

4.2.4 Noise Analysis

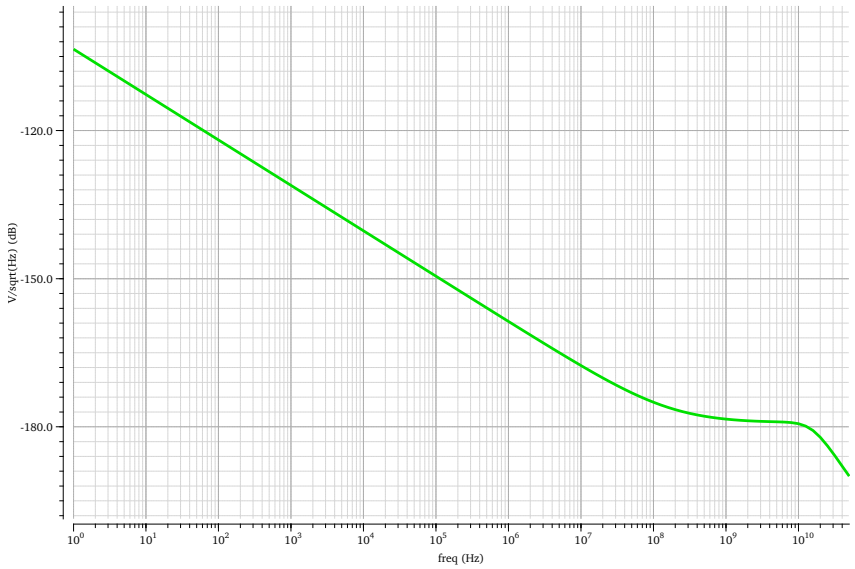


Figure 4.11: BSF Integrated noise

The noise analysis computes integrated root-mean-square of the total noise over the bandwidth of interest (100MHz to 50 GHz).

For the BSF the integrated noise is 172 μVrms (see Figure 4.11), meaning that the requirements set for the project are met.

4.2.5 Transient Analysis

IM3 is calculated for different frequencies, but only one frequency is described in detail for each topology. This frequency is 2.744 GHz, that is accompanied by a second tone with equal amplitude at 2.764 GHz. As a result, the two-tone spacing is approximately 20 MHz.

Figure 4.12 shows that the IM3 value for 2.744 GHz input frequency with a input amplitude of 0.25 V is 59.94 dB.

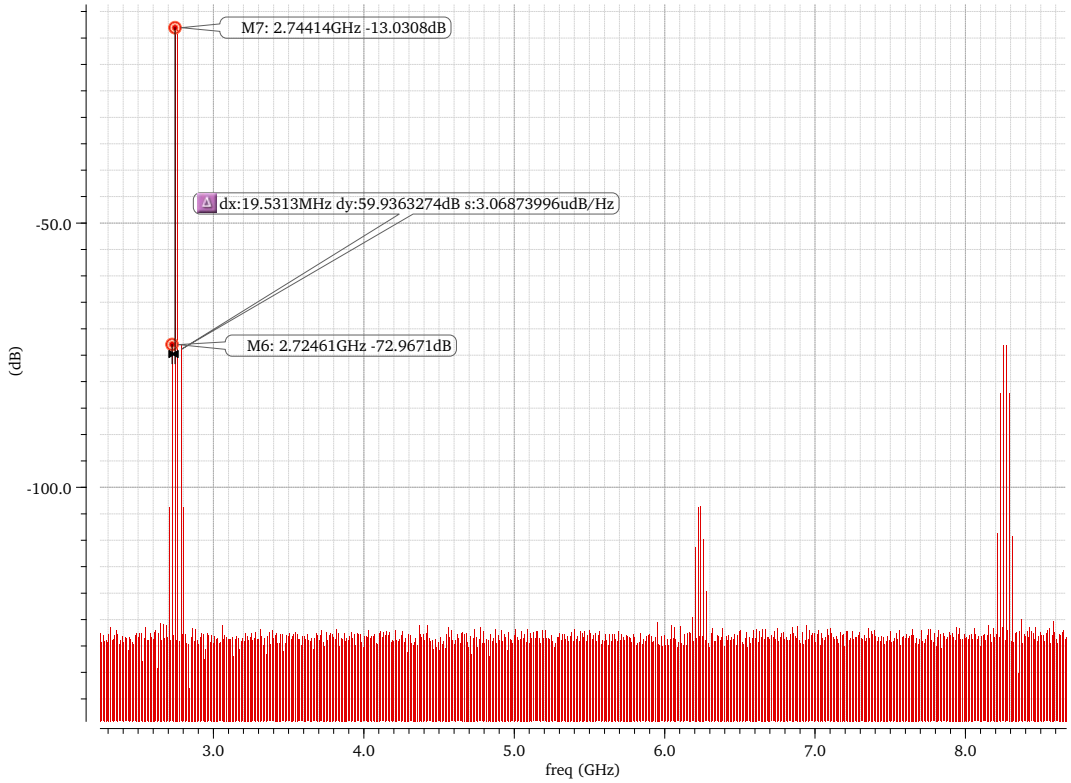


Figure 4.12: BSF two-tone test spectrum

As discussed in subsection 4.1.4, IIP3 is usually estimated from IM3. By applying Equation 4.7, IIP3 is approximately 27.93 dBm.

$$IIP_3|_{\text{dBm}} \approx \frac{IM3|_{\text{dB}}}{2} + P_{in}|_{\text{dBm}} = \frac{59.94}{2} + 10\log_{10}\frac{0.25^2}{2 \cdot 50 \cdot 10^{-3}} = 27.93 \quad \text{dBm} \tag{4.7}$$

In the time domain, the output voltage is represented in Figure 4.13, where the differential output voltage peak-to-peak ($V_{out_{pp}}$) is approximately 890 mV. Moreover, as detailed in Table 4.1, $V_{out_{pp}}$ is calculated with an AC magnitude of 0.5V and HD3 with an input amplitude (Ain) of 0.25V.

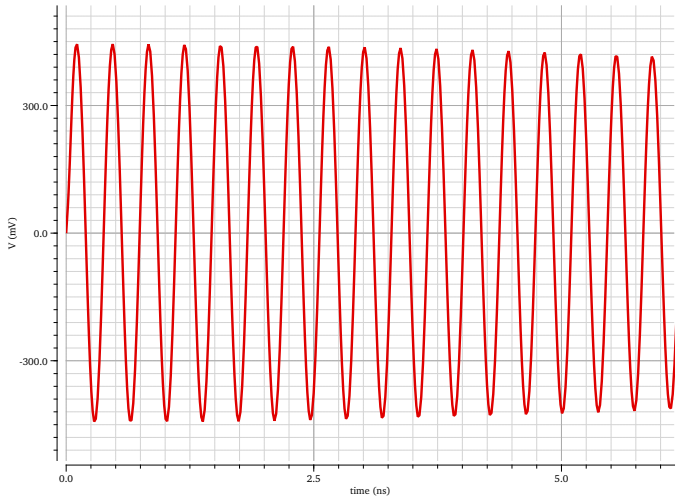


Figure 4.13: BSF two-tone test time domain

Usually, the linearity drops as the frequency increases; Figure 4.14 with the SF linearity results follows this trend. As stated previously, the higher the IIP3 value, the better the linearity is. For the BSF the worst case of linearity is 25.13 dBm from the ones that fall in the band of interest.

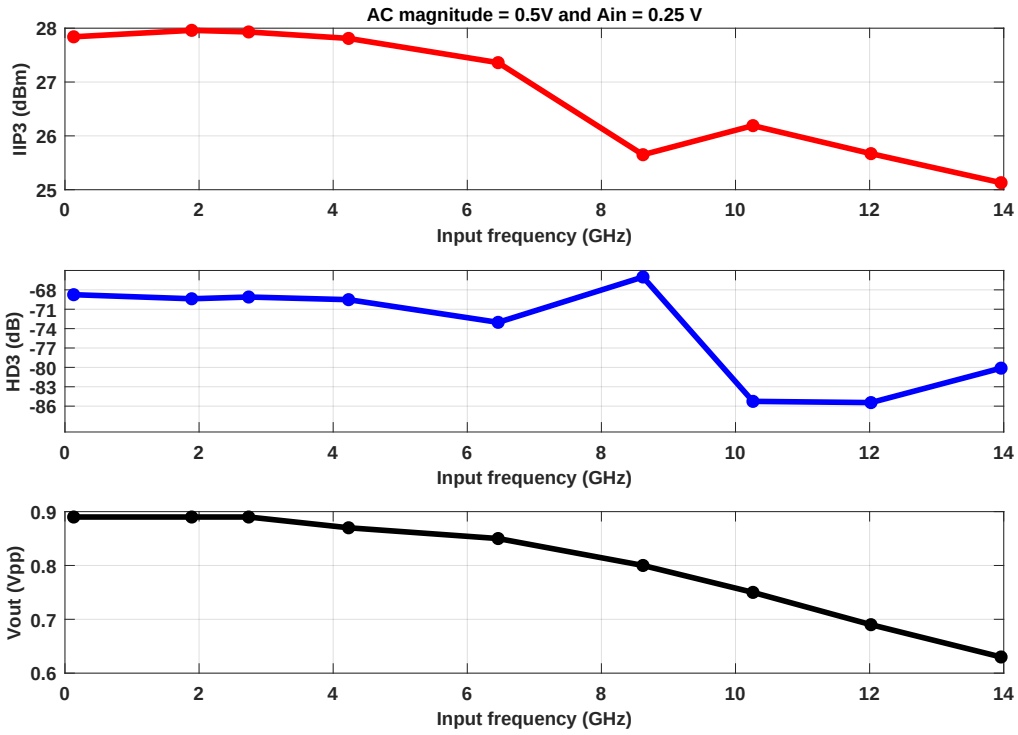


Figure 4.14: BSF linearity results

It's worth noting that $IM3_{LOW}$ measures the third order IM products at $(2 \cdot f_1 - f_2)$. Although, there is another third-order IM product at $(2 \cdot f_2 - f_1)$, the value of the terms is usually the same. Therefore, only the "LOW" frequency product is reported in the Figure 4.14.

4.2.6 Basic Source Follower Results

With the simulations performed, all the results are summarised in Table 4.3.

Table 4.3: BSF results

	BSF	Specification
Output common-mode (V)	0.69	0.70
Bandwidth (GHz)	13.85	18
Noise (μV_{rms})	172.3	200
DC gain (dB)	- 6.91	≈ - 6
IIP3$_{min}$ (dBm)	25.13	≈ 23
Input common-mode (V)	1.49	< 1.5
DC power (mW)	2 × 90	-
Current (mA)	49	-

The results show that the BSF meets the linearity and noise requirements but does not meet the bandwidth requirement. In addition, the term two in the DC power results from using a differential structure.

4.3 RC Assisted Buffer

Like the BSF, the RC assisted buffer is biased with a simple current mirror and with an ideal amplifier that implements the common-mode feedback (CMFB) to set the DC output voltage at 0.7 V (V_{CM}), as shown in Figure 4.15.

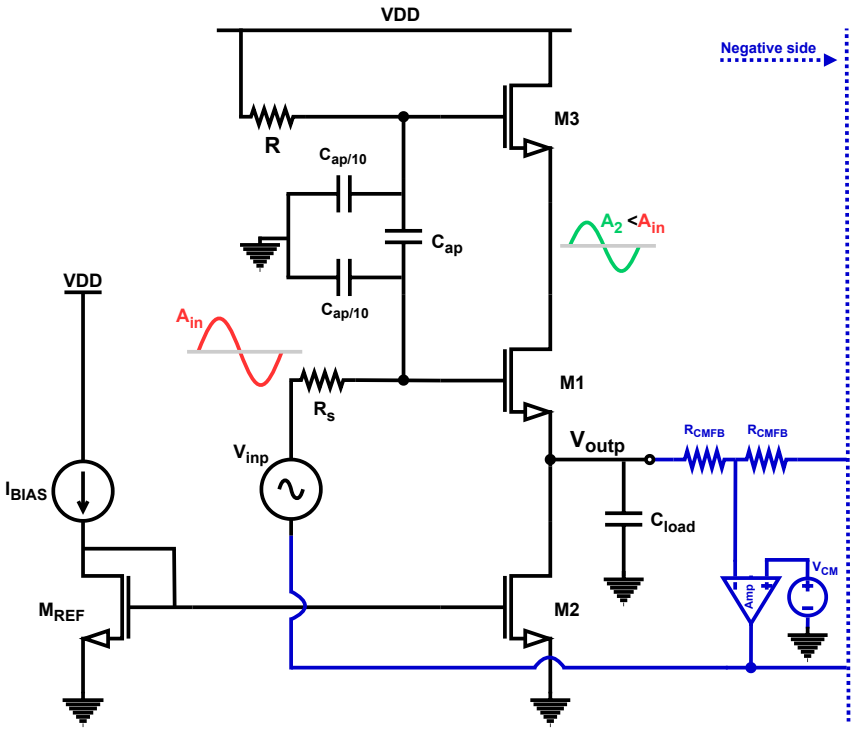


Figure 4.15: RC assisted buffer bias with a current mirror

As discussed in section 3.10, to improve the linearity by reducing the channel length modulation, the SF M1 drain is "bootstrapped" using the RC circuit and the SF M3.

To ensure that the simulation represents the real life conditions more accurately, the capacitance $Caps$ has two flying cap parasitic to ground equal to 0.1·Cap.

A simplified theoretical analysis is displayed in Table 4.4, where $C_{p_{M3}}$ is a fictitious capacitance representing the transistor M3 equivalent capacitance.

Table 4.4: RC SF theoretical analysis

DC gain	$\frac{g_{m1}}{g_{m1}+g_{mb1}+g_{ds1}}$
Rout	$\frac{1}{g_{m1}}$
Output Pole	$\frac{g_{m1}}{C_{load}}$
Input Pole	$\frac{1}{Rs\left[C_{ap}+C_{gs1}+C_{p_{M3}}\right]}$
Input referred noise	$4kT\gamma\left(\frac{1}{g_{m1}}+\frac{g_{m2}}{g_{m1}^2}\right)$

In this design, the degrees of freedom are the DC current (M2 multiplier), SF M1 and M3 multiplier, the resistance R value, and the capacitance Cap value.

4.3.1 Design Strategy and Sizes

The main trade-off in this architecture exists between linearity and bandwidth created by the capacitance Cap and the M3 multiplier. By forcing V_{DS1} to be almost constant to improve the linearity, V_x has to be approximately equal to V_{in} (see Figure 4.16). However, if $V_x \approx V_{in}$, the capacitance Cap have to be huge for $\left|\frac{1}{1+\frac{C_{p_{M3}}}{C_{ap}}}\right| = 1$. Consequently, a high Cap will translate into a low input pole which degrades the bandwidth.

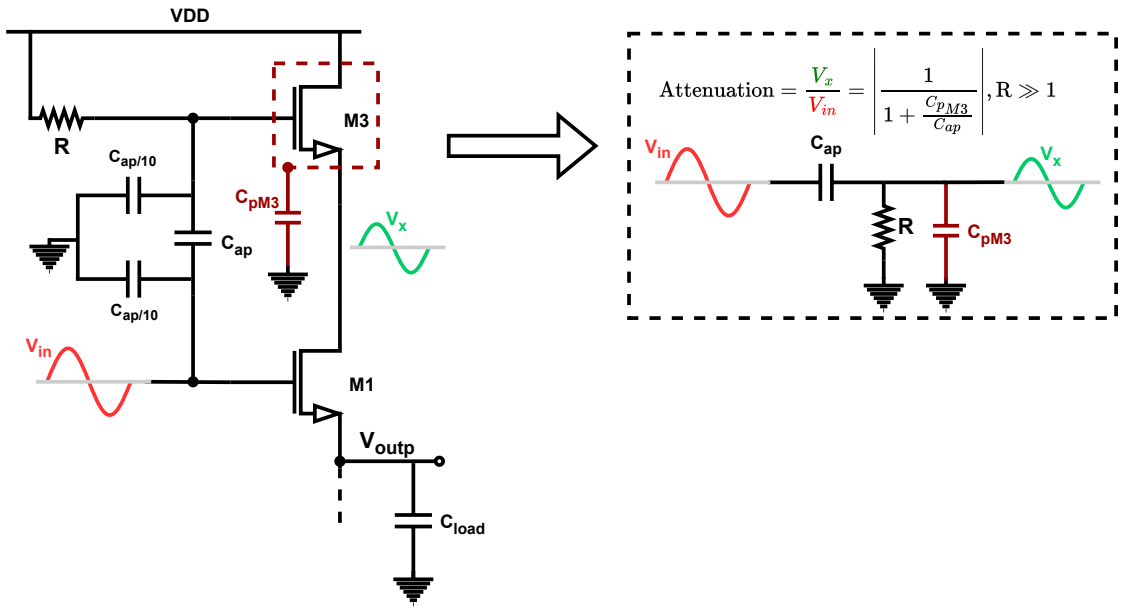


Figure 4.16: Trade-off linearity versus bandwidth

The value of the M3 multiplier has to be as low as possible because a lower M3 width means a smaller $C_{p_{M3}}$. Therefore, a smaller Cap is required to compensate for the attenuation due to M3, leading to higher bandwidth. On the other hand, a lower capacity has a higher voltage drop. Thus, increasing V_{DS3}.

Moreover, the transistor M3 is in a diode configuration that improves the linearity by increasing the output swing.

To sum up, the design strategy for this topology consists of the following steps:

1. Choose R to be large and $I_D = I_{BSF} = 49 \quad mA$.
2. Choose the M3 multiplier as low as possible with $V_{OCM} = 0.7 \quad V$.
3. Choose $C_{ap} \rightarrow$ Attenuation $= \frac{V_x}{V_{in}} = \left| \frac{1}{1+\frac{C_{pM3}}{C_{ap}}} \right| > 0.8$
4. Scale I_D, M, M1 and M2 multiplier, and Cap for optimum bandwidth.

It has to be noted that R, in the first step, has to be big to prevent any AC signal from going to the supply voltage and not influence the voltage divider.

Three scenarios with different $Caps$ will be simulated to demonstrate the trade-off of linearity versus bandwidth.

M2 multiplier is parameterized with a value of 66 to obtain 22 mA of DC current and M1 multiplier with 146, and M3 is sized as small as possible, 54, to reduce the M3 parasitic capacitance while maintaining the output common mode.

4.3.2 DC Analysis

The DC operating point is displayed in Figure 4.17, all transistors are in saturation, and the output common mode is approximately 0.7 V.

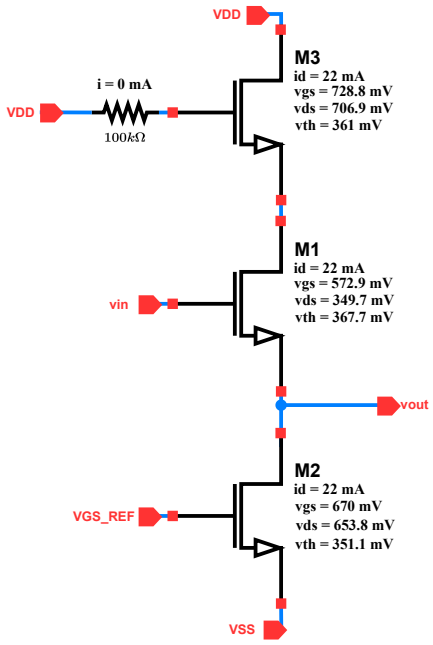


Figure 4.17: RC assisted buffer DC operating point

The RC assisted buffer consumes 22 mA with I_{BIAS} equal to 1 mA and M_{REF} multiplier equal to 3, which is only 45% of the current consumed by the Basic source follower.

4.3.3 AC Analysis

The Bode diagrams for the three scenarios are given in Figure 4.10, the DC gain is entirely flat at low frequencies, and the bandwidth for scenario 1, 2, and 3 is approximately 9.88, 9.11, and 4.74 GHz, respectively. The only difference between the 3 circuits is the value of Cap.

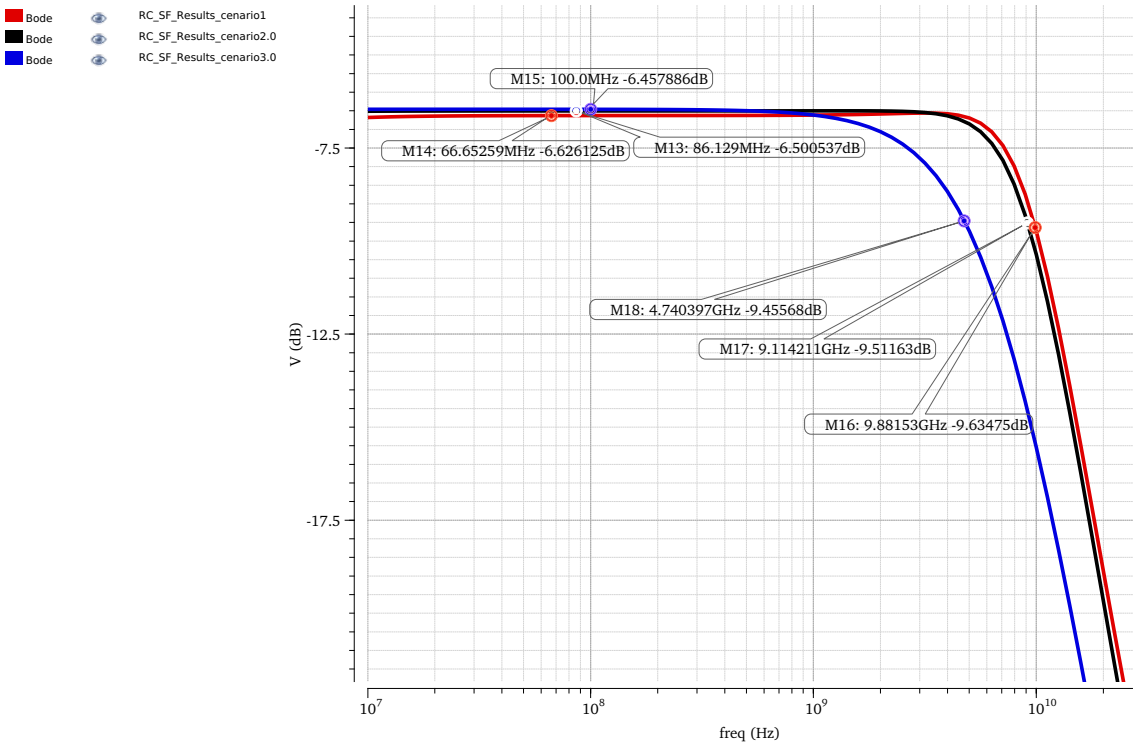


Figure 4.18: RC assisted buffer frequency response for the three scenarios

In Figure 4.18, the red line is scenario 1, where the bandwidth is equal to 9.88 GHz, the attenuation is approximately 0.57 V with a Cap of 0.2 pF. Scenario 2, the black line, has 9.11 GHz, attenuation of 0.8 V, and a Cap of 0.9 pF. Finally, scenario 3 has 4.74 GHz with an attenuation of 0.89 V and a Cap of 5 pF.

Figure 4.18 shows the trade-off of linearity versus bandwidth. In order to decrease the attenuation from V_{in} to V_x, a large Cap is needed, which inherently increases the input RC time constant, leading to bandwidth reduction.

In addition, linearity is related to attenuation and this can be demonstrated by plotting the M1 drain-source potential variation over the frequency, as shown in Figure 4.19.

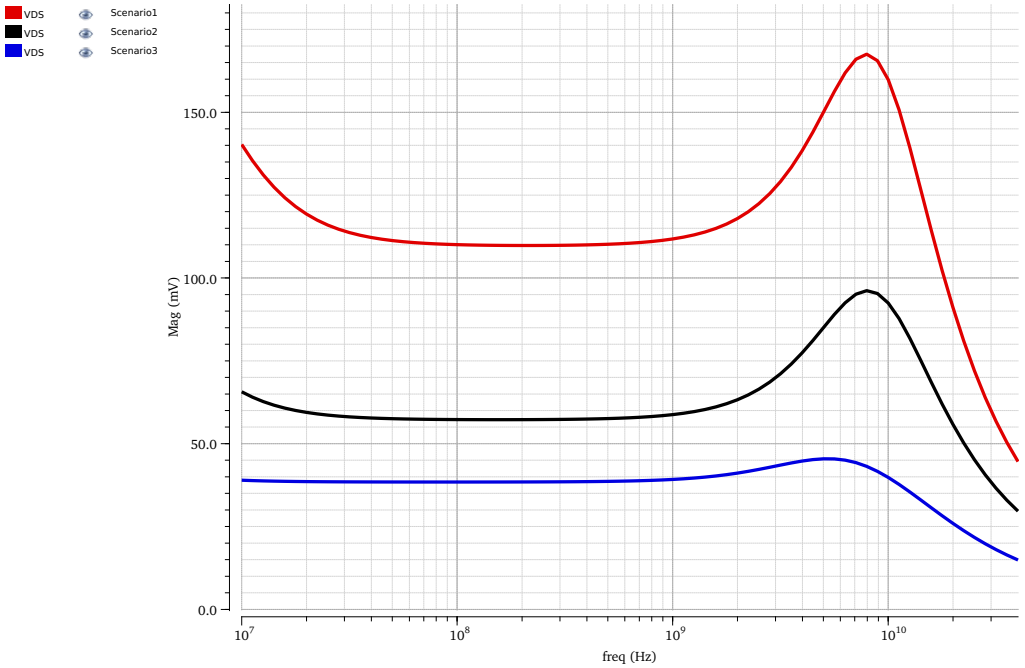


Figure 4.19: $V_{DS_{M1}}$ variation with frequency for the three scenarios

From Figure 4.19, it is possible to see that a higher Cap produces a less $V_{DS_{M1}}$ variation. As a result, there is a minimization of the channel length modulation effect.

4.3.4 Noise Analysis

For the RC assisted buffer, the integrated noise in the three scenarios is less than 200 μV_{rms}, meeting the specifications (see Figure 4.20).

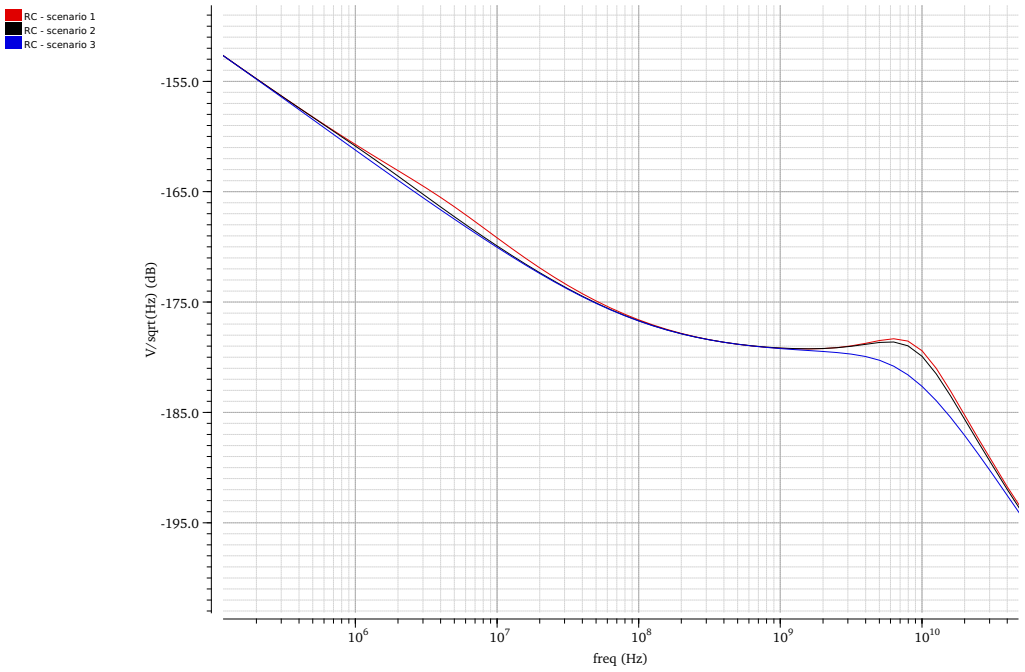
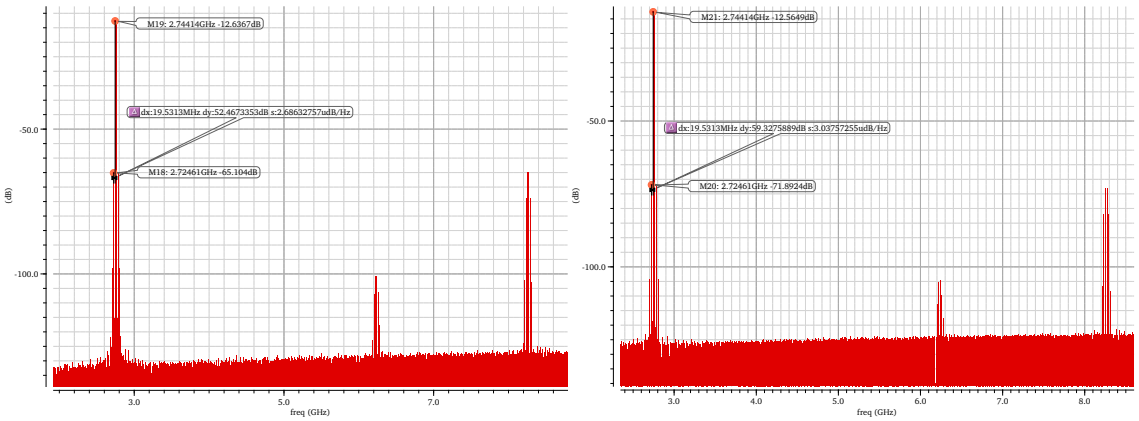


Figure 4.20: RC assisted buffer integrated noise

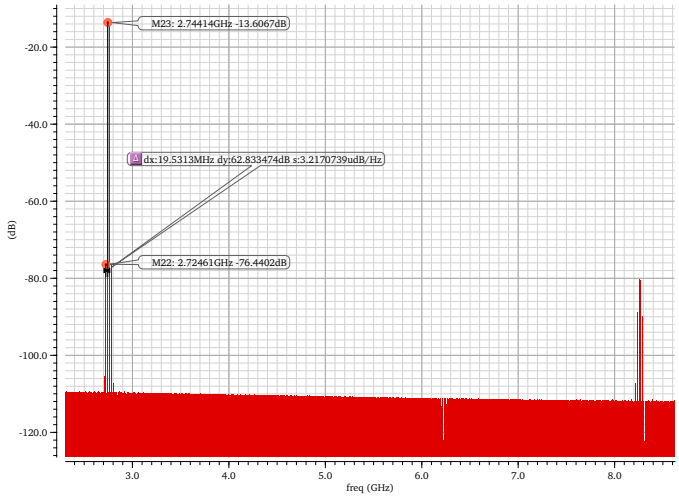
The three scenarios above exhibit the trade-off of noise versus bandwidth, a well know trade-off in electronics. Where scenario 1 with a BW of 9.88 GHz, scenario 2 with a BW of 9.11 GHz, and scenario 3 with a BW of 4.74 GHz have a noise of 151.5, 146.4, and 123.1 μV_{rms}, respectively.

4.3.5 Transient Analysis

The IM3 values for 2.744 GHz input frequency are 52.47, 59.33, and 62.83 dB, as shown in Figure 4.21. As a result, IIP3 is approximately 24.19, 27.62, and 29.38 dBm.



(a) BW =9.88 GHz, $\frac{V_x}{V_{in}}$ =0.57 V, IIP3 =24.19 dBm (b) BW =9.11 GHz, $\frac{V_x}{V_{in}}$ =0.80 V, IIP3 =27.62 dBm

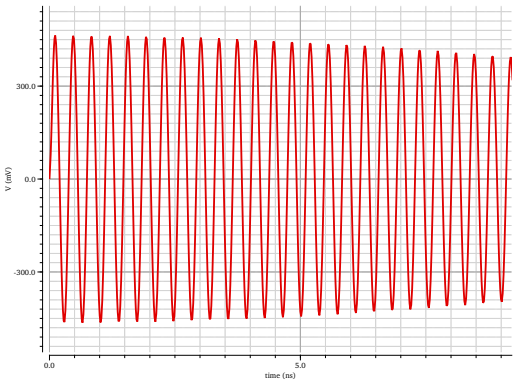


(c) BW =4.74 GHz, $\frac{V_x}{V_{in}}$ =0.89 V, and IIP3 =29.38 dBm

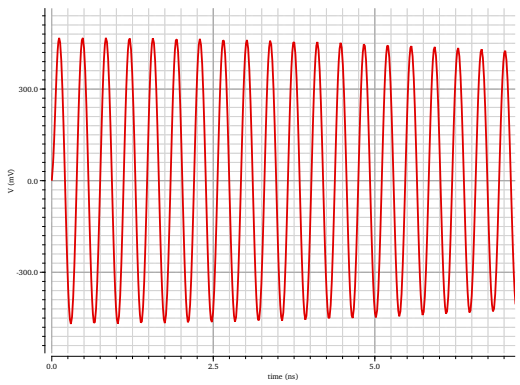
Figure 4.21: RC assisted buffer two-tone test spectrum

It has been argued that a lower attenuation from V_{in} to V_x improves linearity, however, it was not possible to verify the claim with AC analysis. From the transient analysis it can be seen that decreasing the attenuation improves the linearity by increasing IIP3.

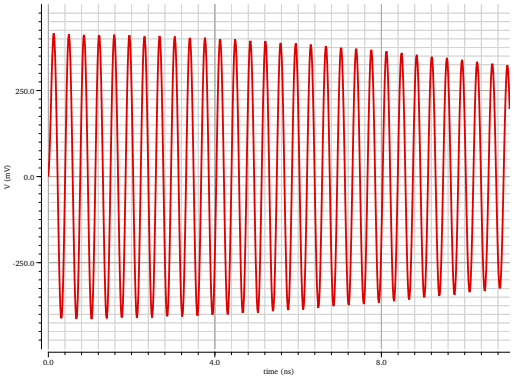
In the time domain, the output voltage is represented in Figure 4.13, where the differential output voltage peak-to-peak ($V_{out_{pp}}$) is approximately 929, 939, and 833 mV, respectively.



(a) BW =9.88 GHz, $V_{out_{pp}}$ = 929 mV



(b) BW =9.11 GHz, $V_{out_{pp}}$ = 939 mV



(c) BW =4.74 GHz, $V_{out_{pp}}$ = 833 mV

Figure 4.22: RC assisted buffer two-tone test time domain

As the BSF, the linearity drops as the frequency increases, see Figure 4.14.

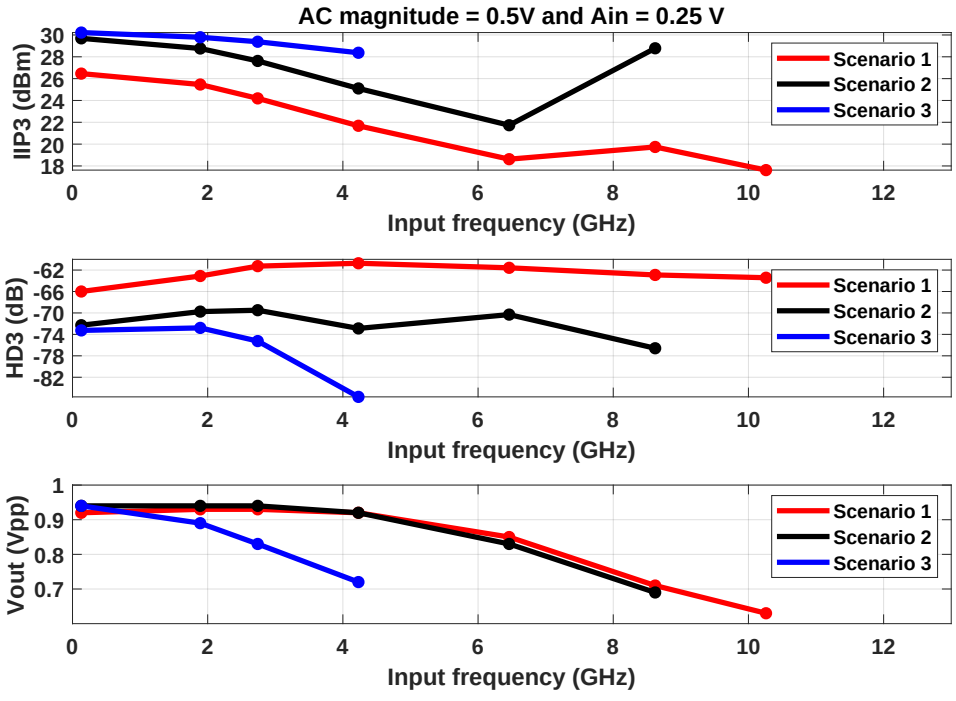


Figure 4.23: RC assisted buffer linearity results

For the RC assisted buffer, the worst linearity cases within the band are 17.62, 21.73, and 28.37 dBm, respectively.

4.3.6 RC Assisted Buffer Results

With the simulations performed, all the results are summarised in Table 4.5.

Table 4.5: RC assisted buffer results

Topology	**RC Assisted Buffer**			
Scenario	**1**	**2**	**3**	**Specification**
Bandwidth (GHz)	9.88	9.11	4.74	18
Noise (μV_{rms})	151.5	146.4	123.1	200
DC gain (dB)	-6.63	-6.50	-6.46	$\approx$ - 6
IIP3$_{min}$ (dBm)	17.62	21.73	28.37	$\approx$ 23
Input common-mode (V)	1.27			< 1.5
R (KΩ)	100			-
Cap (pF)	0.2	0.9	5.0	-
Attenuation (V)	0.57	0.80	0.89	-
Output common-mode (V)	0.69			0.70
DC power (mW)	2×41.4			-
Current (mA)	22			-

The results show that the RC assisted buffer meets the linearity and noise requirements in scenarios 3 but does not meet the bandwidth requirement. Moreover, from these simulations, it is possible to conclude that the drain bootstrap technique helps to improve the linearity.

4.4 Basic Push-pull

The Basic push-pull is biased with a replica-buffer and with an ideal amplifier that implements the common-mode feedback to achieve output common-mode voltage stabilization, as shown in Figure 4.24. Additionally, the replica-buffer has a huge capacitor (10 pF) to stabilize the negative feedback loop, and replica-buffer size is scaled-down to reduce the power consumption.

Simplified theoretical analysis for the Basic push-pull is presented in Table 4.6.

Table 4.6: Basic push-pull theoretical analysis

DC gain	0
Rout	$\frac{1}{2 \cdot (g_m + g_{mb} + g_{ds})}$
Output Pole	$\frac{2 \cdot g_m}{C_{load}}$
Input Pole	$\frac{1}{2 \cdot Rs \left[C_{gs} + Cap \right]}$
Input referred noise	$4kT\gamma \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} \right)$

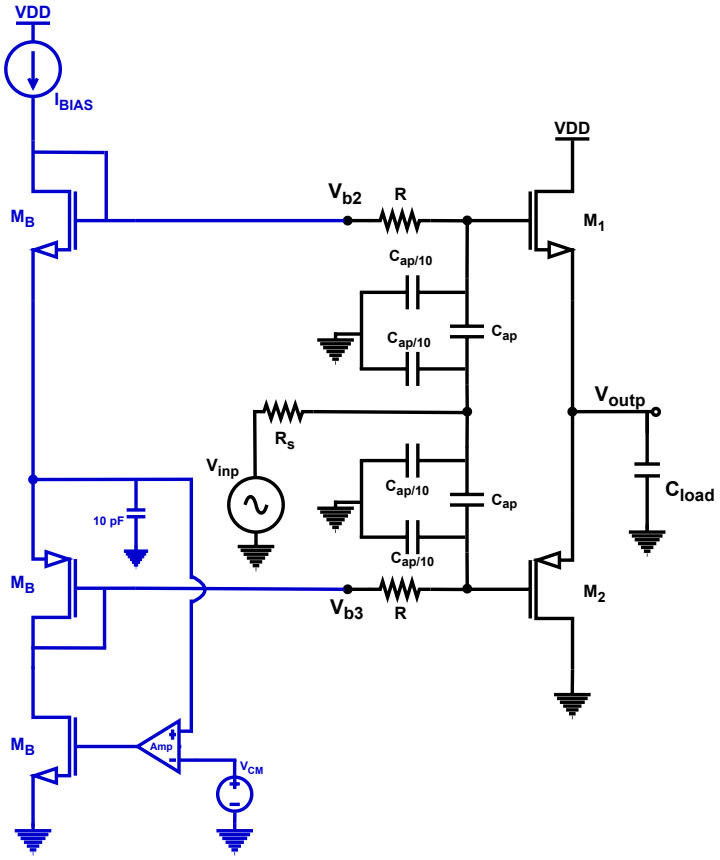


Figure 4.24: Basic push-pull bias with a replica bias circuit

In this design, the degrees of freedom are the M1 and M2 multipliers, the bias current I_{BIAS}, and the capacitance Cap value.

4.4.1 Design Strategy and Sizes

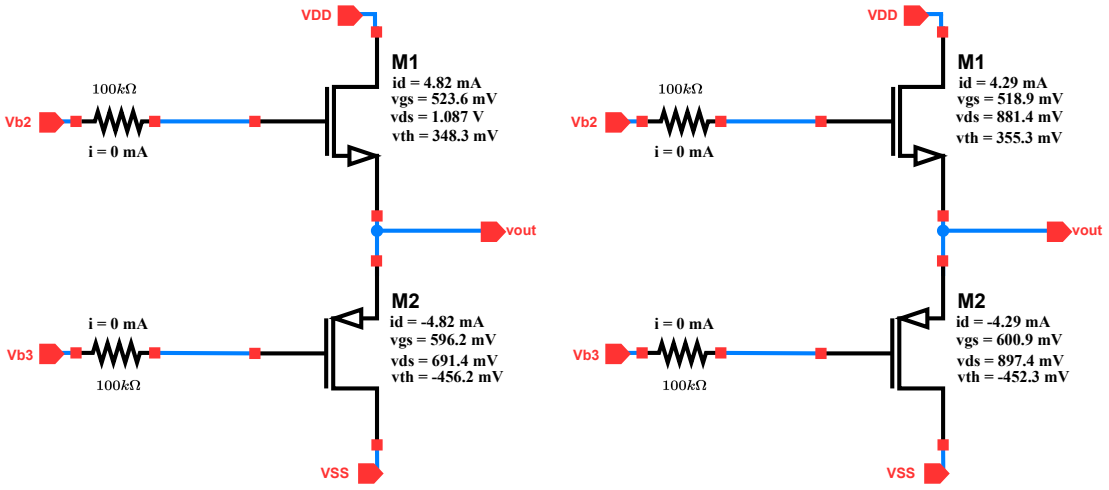
The main trade-off present in this architecture is gain versus bandwidth, created by the capacitance Cap. To increase the frequency of the input pole small Cap is required. However, a small Cap produces a higher attenuation, thus reducing the DC gain.

The design strategy is to size for the maximum bandwidth without compromising the DC gain - sizing Cap to have a DC gain no less than -9 dB. Furthermore, a higher Cap allows the use of a larger multiplier.

Two scenarios were simulated, with the common mode output voltage equal to 0.7 and 0.9 V. In the first scenario, M1 is sized with 40 and M2 with 50, and Cap has a value of 2.5 pF. With an output common mode equal to 0.9 V, M1 and M2 are sized with 40, and Cap with 2.4 pF. Both cases use MB multiplier of 10 and 1 mA of bias current.

4.4.2 DC Analysis

As depicted in Figure 4.25, all transistors are in saturation, and the common mode output voltage is approximately 700 and 900 mV, respectively.



(a) $I_D = 4.82$ mA, $V_{out_{CM}} = 700$ mV (b) $I_D = 4.29$ mA, $V_{out_{CM}} = 900$ mV

Figure 4.25: Basic push-pull DC operating point

Comparing the Basic push-pull with the previous topologies, this architecture dissipates much less DC current. Note that this topology consumes 22% of the current consumed by RC assisted buffer and only 10% of the current consumed by the Basic source follower.

4.4.3 AC Analysis

The Bode diagrams are provided in Figure 4.26, the DC gain is entirely flat at low frequencies, and the bandwidth is approximately 4.63 and 4.68 GHz, respectively.

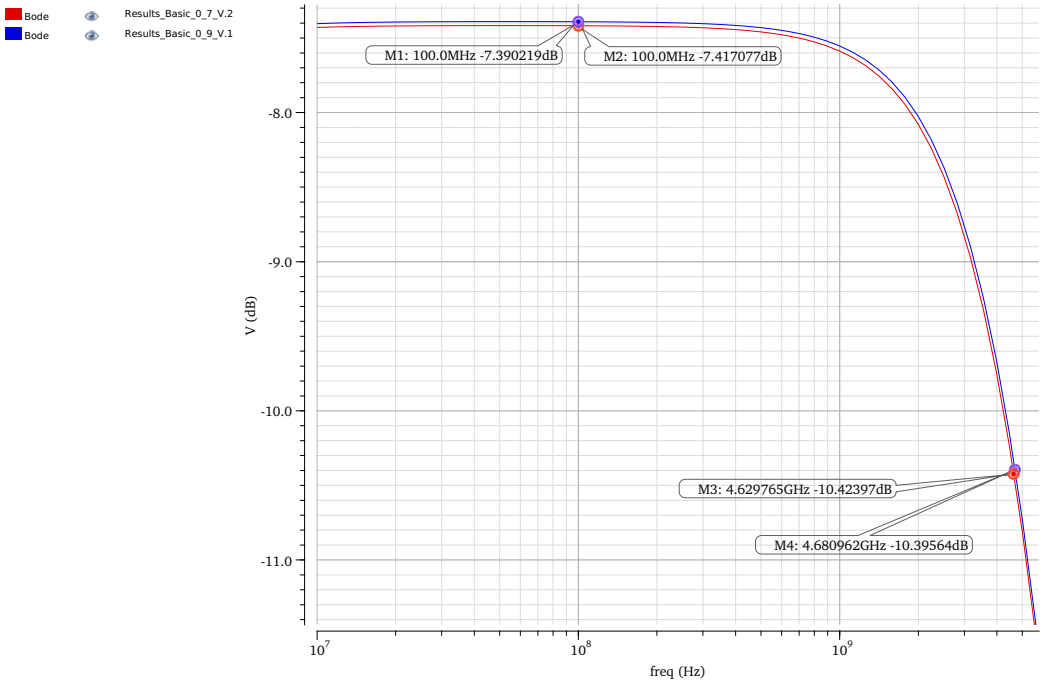


Figure 4.26: Basic push-pull frequency response

As detailed in Figure 4.26, the bandwidth and the DC gain are barely sensitive to the common mode output voltage variation. The blue line corresponds to scenario $V_{out_{CM}}$ of 0.9V, while the red line depicts scenario with $V_{out_{CM}}$ of 0.7V.

4.4.4 Noise Analysis

The integrated noise in both scenarios is less than 200 μVrms (see Figure 4.27), to be precise scenario 1 and 2 have 98.11 and 99.25 μV_{rms}, respectively.

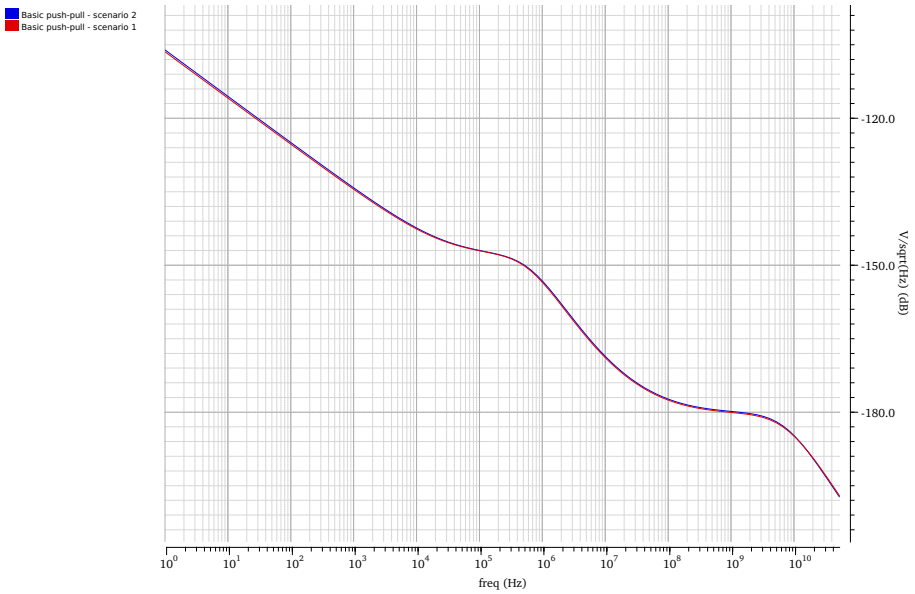
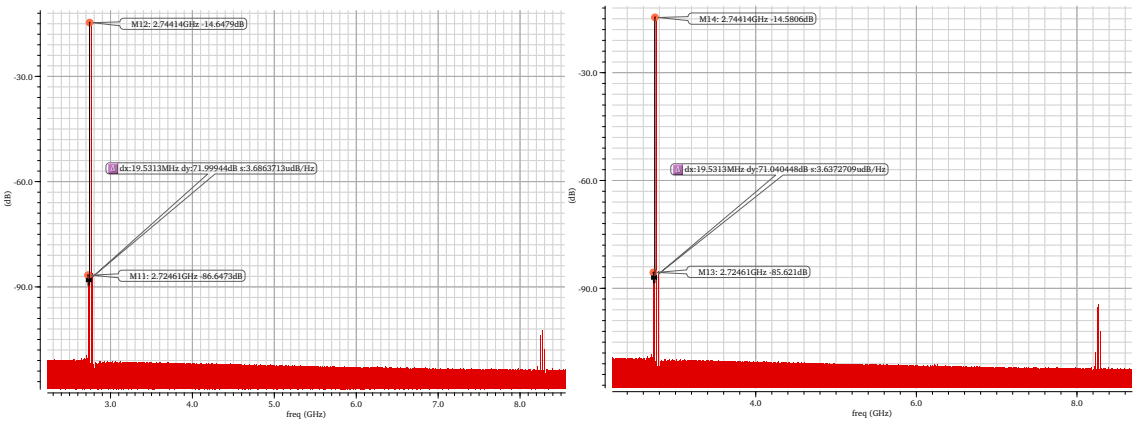


Figure 4.27: Basic push-pull integrated noise

4.4.5 Transient Analysis

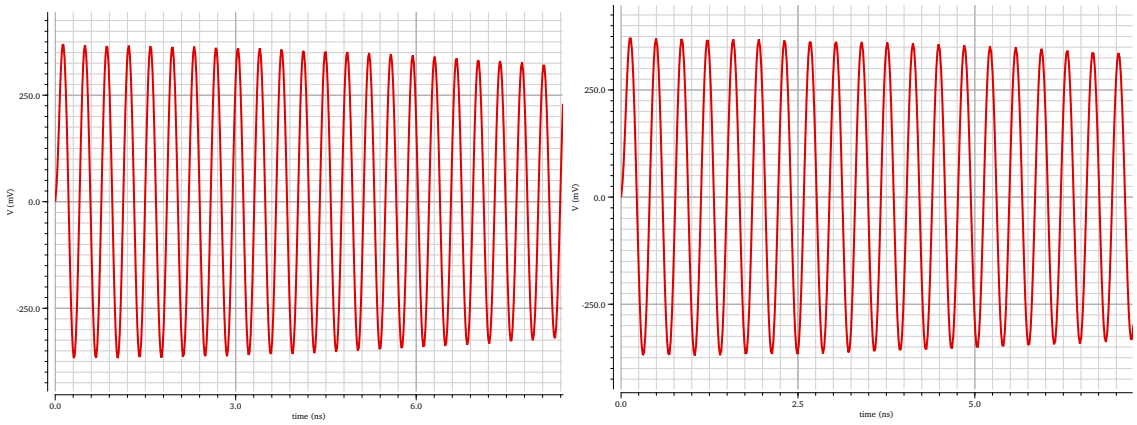
The IIP3 values are approximately 33.96 and 33.48 dBm as the IM3 values for 2.744 GHz input frequency are 72 and 71 dB, as displayed in Figure 4.28.



(a) $V_{out_{CM}}$ = 0.7V, IIP3 =33.96 dBm (b) $V_{out_{CM}}$ = 0.9V, IIP3 =33.48 dBm

Figure 4.28: Basic push-pull two-tone test spectrum

The output voltage is represented in Figure 4.13, where the differential output voltage peak-to-peak ($V_{out_{pp}}$) is approximately 740 and 746 mV, respectively.



(a) $V_{out_{CM}} = 0.7$V, $V_{out_{pp}} = 740$ mV (b) $V_{out_{CM}} = 0.9$V, $V_{out_{pp}} = 746$ mV

For the Basic push-pull, the worst cases of linearity within the band are 30.94 and 30.03 dBm, respectively, as detailed in Figure 4.30.

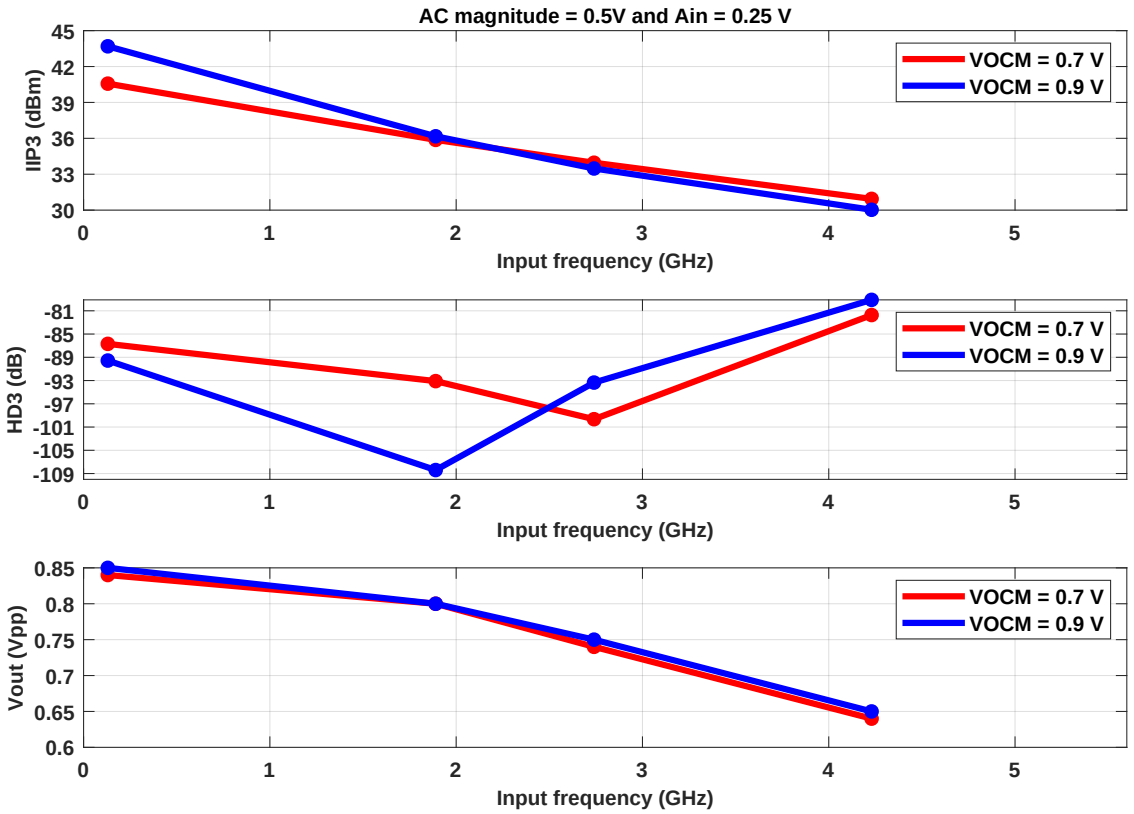


Figure 4.30: Basic push-pull linearity results

4.4.6 Basic push-pull Results

With the simulations performed, all the results are summarised in Table 4.7.

Table 4.7: Basic push-pull results

Topology	**Basic push-pull**		
Scenario	**1**	**2**	**Specification**
Bandwidth (GHz)	4.63	4.68	18
Noise (μV_{rms})	98.11	99.25	$\approx$ 200
DC gain (dB)	-7.42	-7.39	> - 9
IIP3$_{min}$ (dBm)	30.94	30.03	$\approx$ 23
R (KΩ)	100		-
Cap (pF)	2.5	2.4	-
Output common-mode (V)	0.70	0.91	0.70/0.90
Attenuation (V)	0.88		-
DC power (mW)	2$\times$ 10.5	2$\times$ 9.5	-
Current (mA)	4.82	4.29	-

It is worth mentioning that the attenuation value is the signal attenuation through the capacitance Cap.

The Basic push-pull meets the linearity and noise requirements but does not meet the bandwidth requirement. Additionally, comparing the third scenario of the RC assisted buffer with this topology it may be inferred that for the same bandwidth (4.7 GHz), this topology has better linearity (2 dBm more) less noise, and a drastic reduction in DC power consumption. On the other hand, there is a slight reduction in the DC gain (1 dB).

4.5 Push-pull

This section covers a Basic push-pull topology from the previous section with the bootstrap technique applied, as shown in Figure 4.31.

An approximate theoretical analysis for the Push-pull is presented in Table 4.8.

Table 4.8: Push-pull theoretical analysis

DC gain	0
Rout	$\frac{1}{2\cdot(g_m+g_{mb}+g_{ds})}$
Output Pole	$\frac{2\cdot g_m}{C_{load}}$
Input Pole	$\frac{1}{Rs\left[2\cdot C_{gs}+4\cdot Cap\right]}$
Input referred noise	$4kT\gamma\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right)$

The degrees of freedom are the MB, M1, M2, M3, and M4 multipliers, the bias current (I_{BIAS}), and the capacitance Cap value.

4.5.1 Design Strategy and Sizes

The Push-pull source follower is an RC assisted buffer with a complementary branch or a Basic push-pull with the drain bootstrap technique.

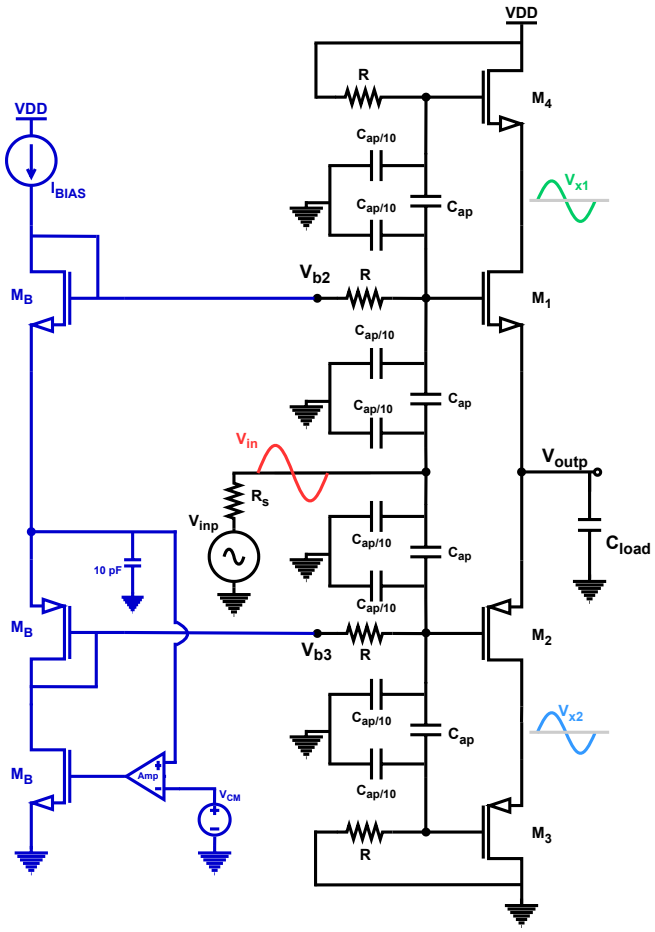


Figure 4.31: Push-pull bias with a replica bias circuit

Therefore, the Push-pull topology has the trade-off linearity versus bandwidth as the RC assisted buffer and the trade-off gain versus bandwidth as the Basic push-pull.

This design uses thick oxide devices that have a V_{TH} of approximately 400 mV. Because of this, it is very complicated to put the output common mode equal to 0.7 V while maintaining some saturation margin. Transistors M2 and M3 need approximately 0.8 V to be in saturation, something difficult to achieve with $V_{out_{CM}}$ equal to 700 mV. Therefore, this topology is designed with 0.9 V $V_{out_{CM}}$.

The multipliers M4 and M3 are sized to be 15, M1 and M2 with 30, and Cap is given a value of $2.4pF$. These result in a DC gain higher than -9 dB.

4.5.2 DC Analysis

The DC operating point is displayed in Figure 4.32, all transistors are in saturation, and the output common mode is approximately 0.9 V. The Push-pull consumes 2.7 mA with I_{BIAS} equal to 0.3 mA and MB multiplier equal to 3.

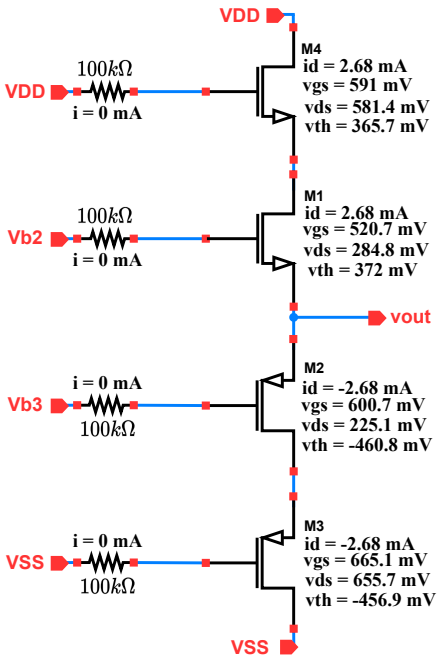


Figure 4.32: Push-pull DC operating point

4.5.3 AC Analysis

The Bode diagram from the Push-pull is in Figure 4.33, the DC gain is entirely flat at low frequencies, and the bandwidth is approximately 3.0 GHz.

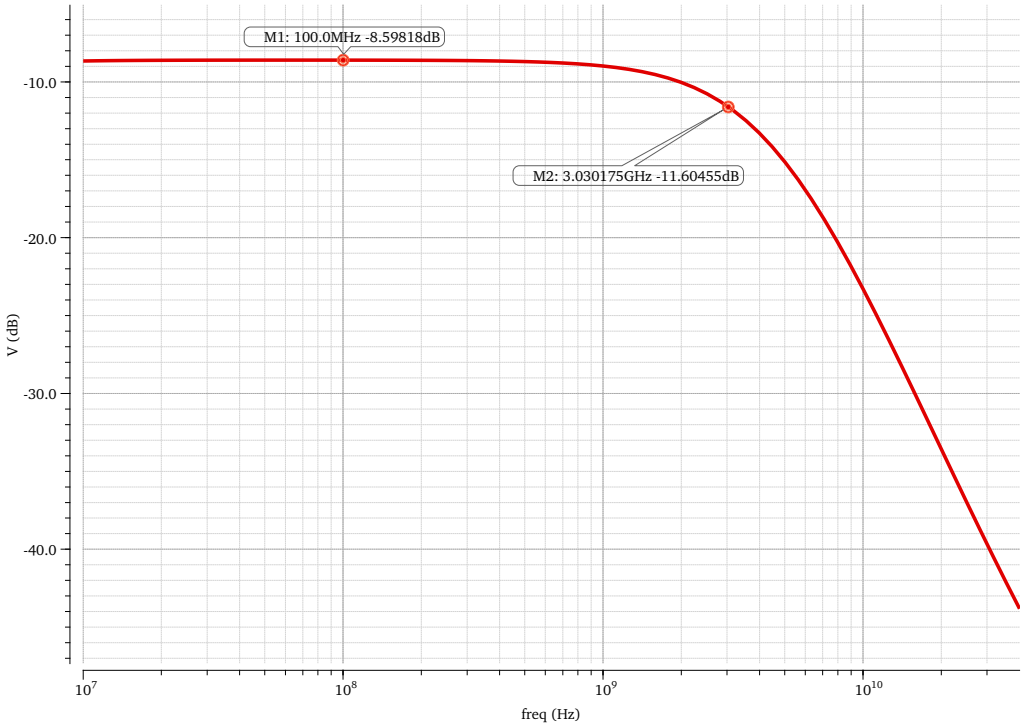


Figure 4.33: Push-pull frequency response

4.5.4 Noise Analysis

For the Push-pull the integrated noise is 82.28 μVrms (see Figure 4.34).

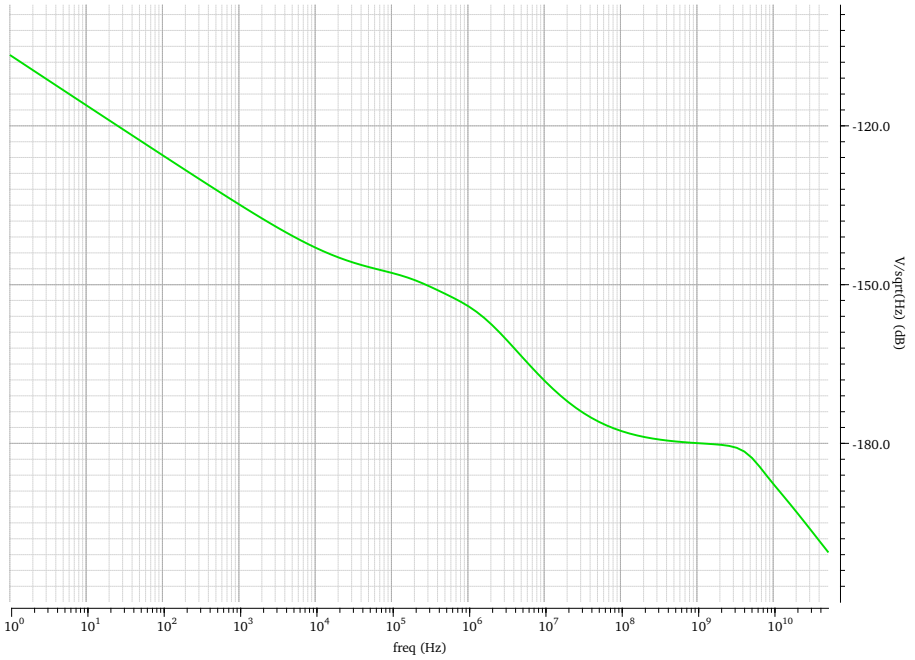


Figure 4.34: Push-pull integrated noise

4.5.5 Transient Analysis

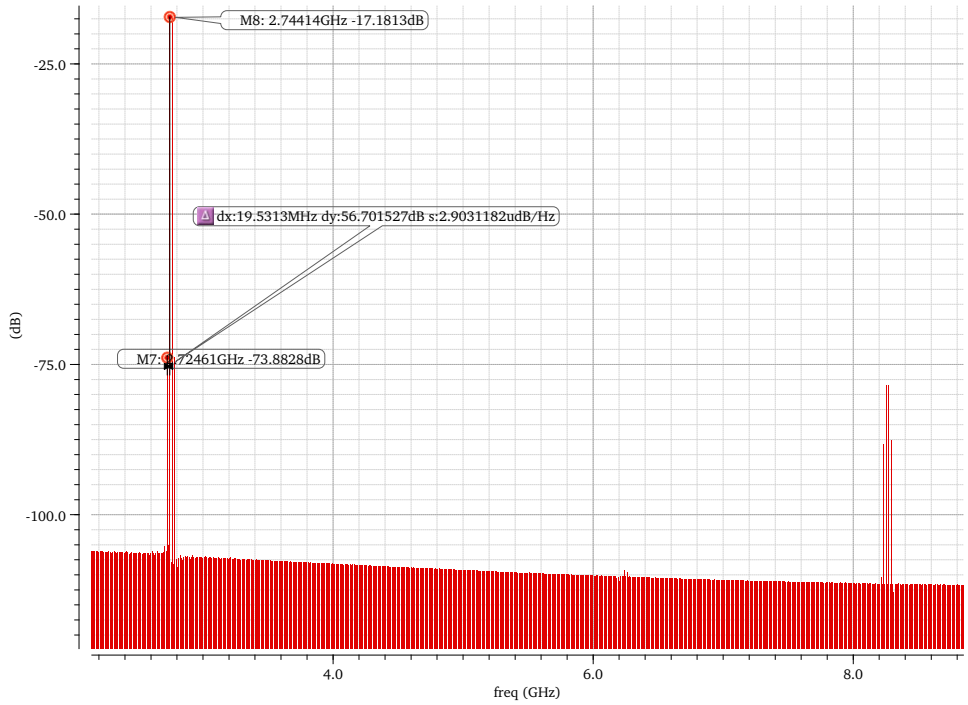


Figure 4.35: Push-pull two-tone test spectrum

The IM3 value for the 2.744 GHz input frequency is 56.7 dB, as shown in Figure 4.35. Thus, IIP3 is approximately 26.31 dBm.

In the time domain, the output voltage is represented in Figure 4.36, where the differential output voltage peak-to-peak ($V_{out_{pp}}$) is approximately 560 mV.

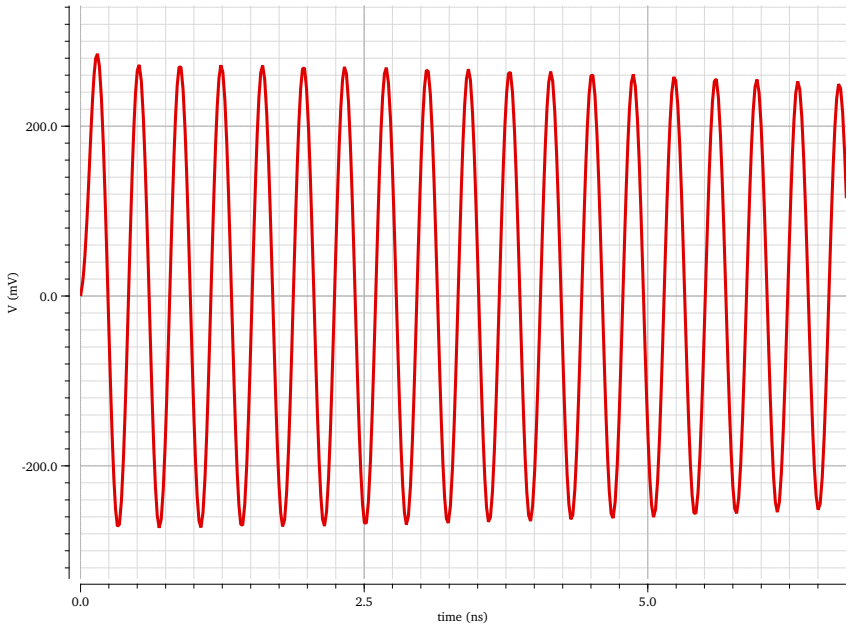


Figure 4.36: Push-pull two-tone test time domain

For the Push-pull the linearity worst-case scenario is 26.31 dBm, as shown in Figure 4.37.

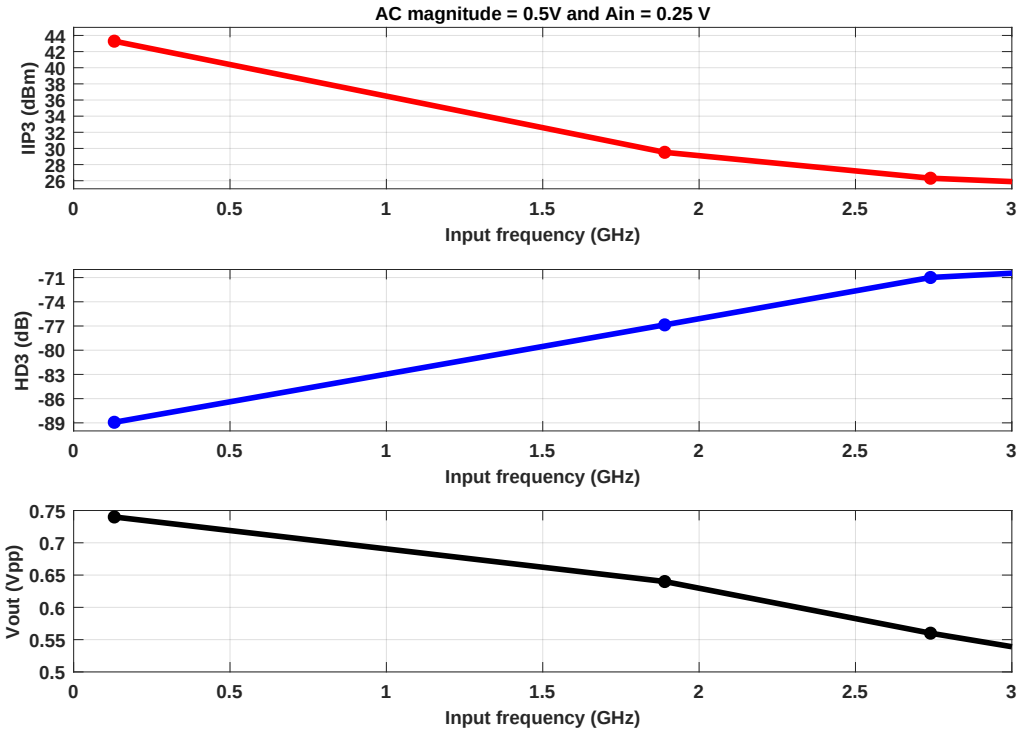


Figure 4.37: Push-pull linearity results

4.5.6 Push-pull Results

With the Push-pull simulations performed, all the results are summarised in Table 4.9.

Table 4.9: Push-pull results

	Push-pull	**Specification**
Output common-mode (V)	0.91	0.90
Bandwidth (GHz)	3.03	18
Noise (μV_{rms})	82.28	$\approx$ 200
DC gain (dB)	- 8.6	> - 9
IIP3$_{min}$ (dBm)	26.31	$\approx$ 23
R (KΩ)	100	-
Cap (pF)	2.4	-
Attenuation (V)	0.76	-
DC power (mW)	2×5.4	-
Current (mA)	2.7	-

In this case, the attenuation measurement is related to the signal attenuation due to Cap connected between the input node and the M1 gate. This attenuation could be optimized by having different values for each Cap.

The results show that the Push-pull meets the linearity and noise requirements but does not meet the bandwidth requirement. Moreover, it is the topology with the lowest bandwidth and power consumption.

4.6 Conclusion

The results for the four topologies are compared in Table 4.10. It can be argued that the Push-pull and the Basic push-pull are the topologies that consume the least power consumption because they have the lowest output resistance. However, these two topologies have a high input capacity that causes a reduction in gain and bandwidth.

The Basic source follower with a low input capacitance is the fastest architecture but the one with the highest power consumption.

Table 4.10: Simulation results

Topology	**BSF**	**RC assisted buffer**			**Basic push-pull**		**Push-pull**
V$_{OCM}$ (V)	0.7	0.7			0.7	0.9	0.9
DC power (mW)	178.20	81.00			19.15	17.24	9.83
Bandwidth (GHz)	13.85	9.88	9.11	4.74	4.63	4.68	3.03
DC gain (dB)	-6.91	-6.63	-6.5	-6.46	-7.42	-7.39	-8.6
IIP3$_{min}$ (dBm)	25.13	17.62	21.73	28.37	30.94	30.03	26.31
Noise (μV_{rms})	172.3	151.5	146.4	123.1	98.11	99.25	82.28

Moreover, the linearity and bandwidth results for all topologies are detailed in Figure 4.38. The curves in the graph represent how IIP3 varies with frequency for each

topology.

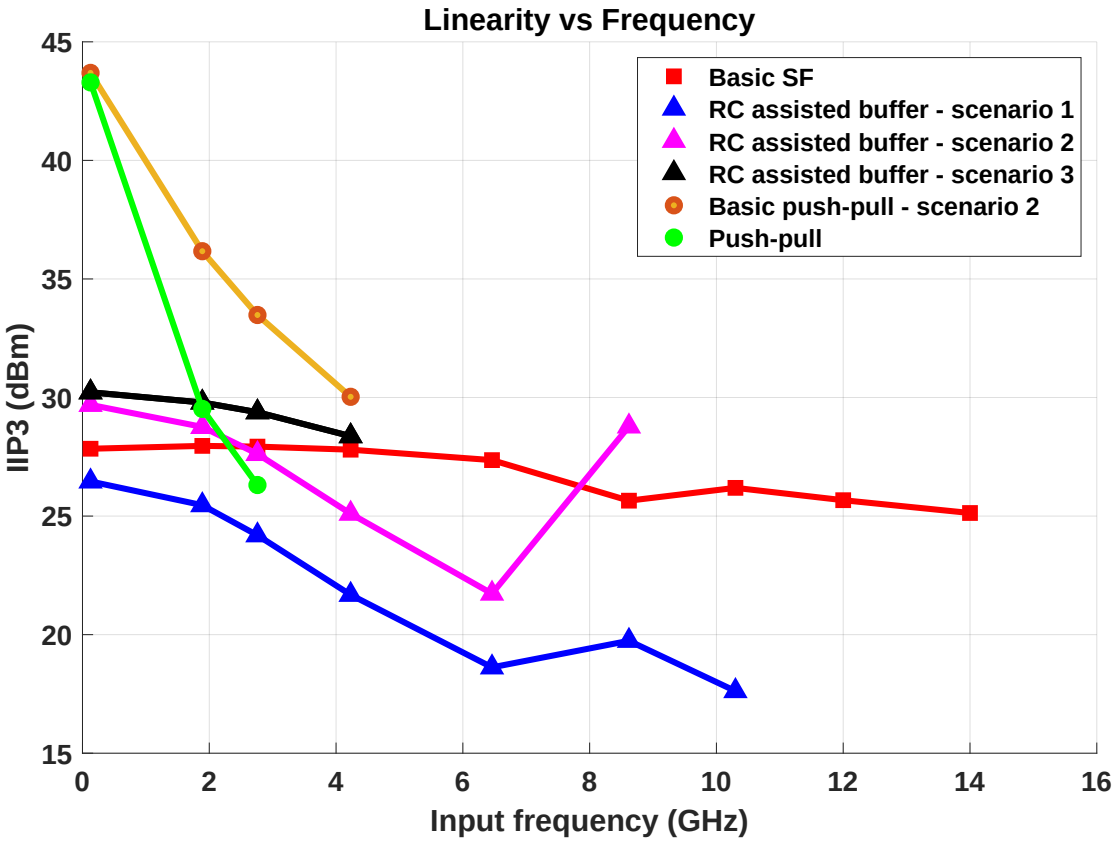


Figure 4.38: Linearity versus Frequency for all topologies

Figure 4.38 shows that the best architectures in terms of linearity are the Basic push-pull (yellow line) and the Push-pull (green line). Interestingly, it was assumed that using the bootstrap technique would increase the linearity of the Push-pull, which turned out to be inaccurate. However, two extra transistors improve linearity by decreasing the V_{DS} variation but degrade the linearity even more by reducing the output swing.

As thoroughly explained in this thesis, the trade-off linearity versus bandwidth for the RC assisted buffer is exhibited in Figure 4.38. Scenarios one, two, and three for the RC assisted buffer are the black, the pink, and the blue line, respectively. The black and blue line shows that for an increase in the linearity of 17.62 to 28.37 dBm (10.75 dBm increase), the bandwidth has to decreases from approximately 10 to 5 GHz (5 GHz reduction).

The Basic source follower has the highest bandwidth (13.88 GHz) as a consequence of its low input capacitance. On the other hand, it has the worst linearity but with IIP3 more or less constant over the frequency.

Finally, it can be concluded that none of the topologies meets the bandwidth requirements. One of the reasons is the use of thick gate devices and one pico farad of sampling capacitance as simulation constraints. Therefore, the next chapter investigates bandwidth extension techniques to achieve the 18 GHz bandwidth.

5

Bandwidth Extension Techniques in Input Buffers

This chapter explores bandwidth extension techniques, for instance, the bridged T-coil with series peaking and a distributed approach. These techniques can drastically increase the bandwidth and improve the return loss.

The loss factor is the reduction in maximum available power due to input impedance miss match. Thereafter it is critical to reduce it such that secondary reflections are extinguished. Nevertheless, large inductors are required, meaning that a huge increase in area is unavoidable [42, 43].

In this project, the performance metric to measure return loss is chosen to be the differential input port voltage reflection coefficient ($S_{11_{dd}}$). Software such as Cadence and Advanced Design System (ADS) are capable of simulating the input return loss over the frequency.

5.1 The Bridged T-coil

In a receiver, the ADC input network deals with its capacitance and the capacitance associated with electrostatic discharge (ESD) protection devices that lowers the bandwidth. Figure 5.1 presents a single-ended input port in which a T-coil is driven by a transmission line with a characteristic impedance of 50 Ω that delivers the signal to the input buffer (IB) and to the termination resistor R_T.

The bridge T-coil consists of two mutually coupled inductors (L_1 and L_2) and a bridge capacitor C_B. These noiseless coils can absorb the buffer capacitance and create a constant, resistive impedance across a wide frequency range.

Ideally, to suppress any input reflection Z_{in} must be equal to $R_S = R_T = 50\,\Omega$, meaning that S_{11} is equal to zero (see Equation 5.1).

$$S_{11} = \left| \frac{Z_{in} - R_s}{Z_{in} + R_s} \right| \tag{5.1}$$

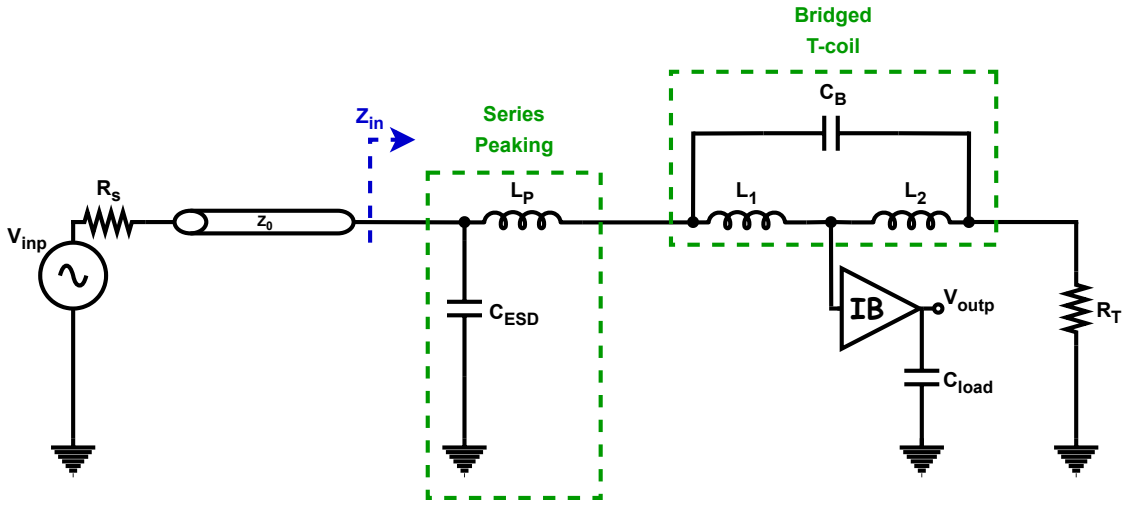


Figure 5.1: The use of series peaking and bridged T-coil

In this thesis a differential architecture is selected in order to investigate the interaction between the common mode and differential signals. One way to measure this interaction is using the mixed-mode S-parameters, for instance, $S_{11_{dd}}$. By definition, $S_{11_{dd}}$ is a complex number equal to:

$$S_{11_{dd}} = \frac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \tag{5.2}$$

where each S-parameter S_{xz} is the ratio of the sine wave voltage coming out of a port (x) to the sine wave voltage that was going into a port (z). A sign convention where port 1 is positive and port 2 is negative was chosen for the study.

5.1.1 Methodology

The T-coil is implemented in ADS software by sweeping values to achieve $S_{11_{dd}}$ lower than -10 dB and no signal attenuation due to L_p, L_1, L_2, and C_B.

Firstly, the S-parameters of the buffer and the ESD protection are extracted from cadence to a Touchstone file by using the test bench in Figure 5.2. Secondly, the Touchstone file with the S-parameters is placed in a two-port box (S2P) in ADS. Lastly, the ADS optimizer is used to find the circuit values that meet the requirements.

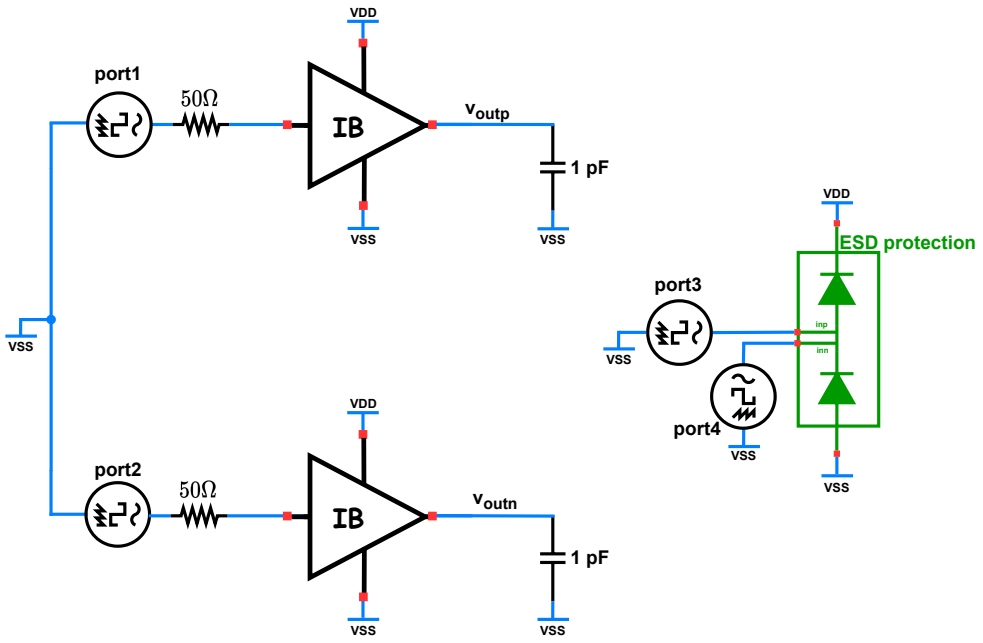


Figure 5.2: Test bench used in cadence to extracted buffer and ESD S-parameters

The ADS schematic is shown in Figure 5.3, where an AC simulation is performed to verify if the bridge T-coil and the series peaking introduce any attenuation. In addition, an S-parameter simulation is computed to inspect the return loss.

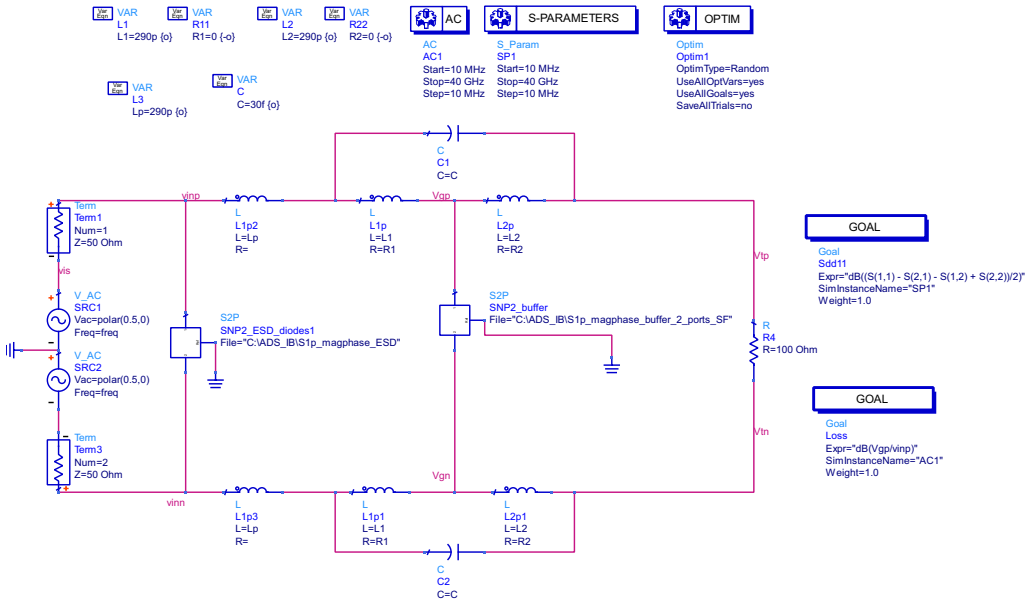


Figure 5.3: Test bench used in ADS for input-match

ADS optimizer varies the component values to achieve the design goals "Loss" and

"Sdd11" displayed in Figure 5.3. The goal "Sdd11" computes and measures if $S_{11_{dd}}$ is lower than -10 dB by using Equation 5.2, and "Loss" measures if the transfer function from $vinp$ to Vgp has a gain higher or equal to 1 dB.

It is worth mentioning that all simulations are performed with the designs provided in chapter 4.

5.1.2 Basic Source Follower

The ADS optimizer is shown in Figure 5.4, where the C represents C_B and the dashed red line on the right-hand side of the figure represents - 10 dB and 1 dB for the goals "Sdd11" and "Loss", respectively. Furthermore, the dotted blue line is the initial curve without the T-coil technique.

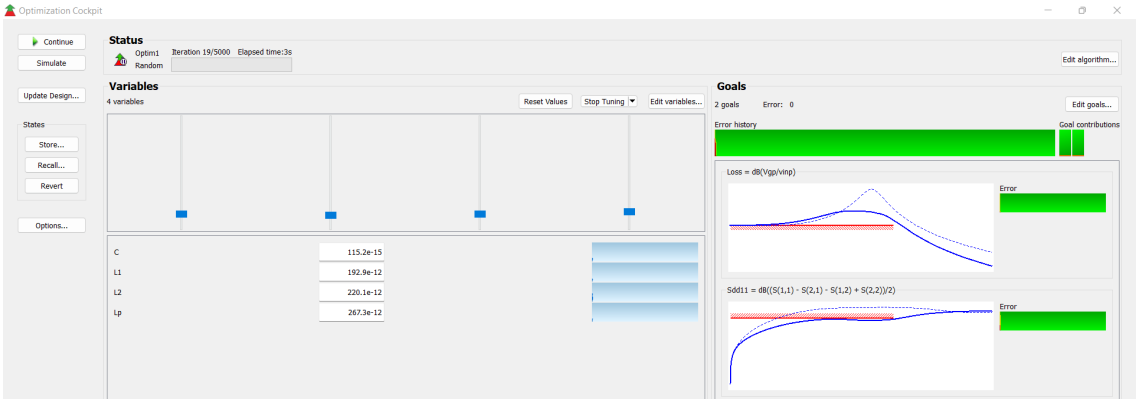


Figure 5.4: ADS optimizer

The BSF ADS results are $S_{11_{dd}}$ lower than -10 dB up to 25.59 GHz and no T-coil attenuation until 25.52 GHz, as shown in Figure 5.5.

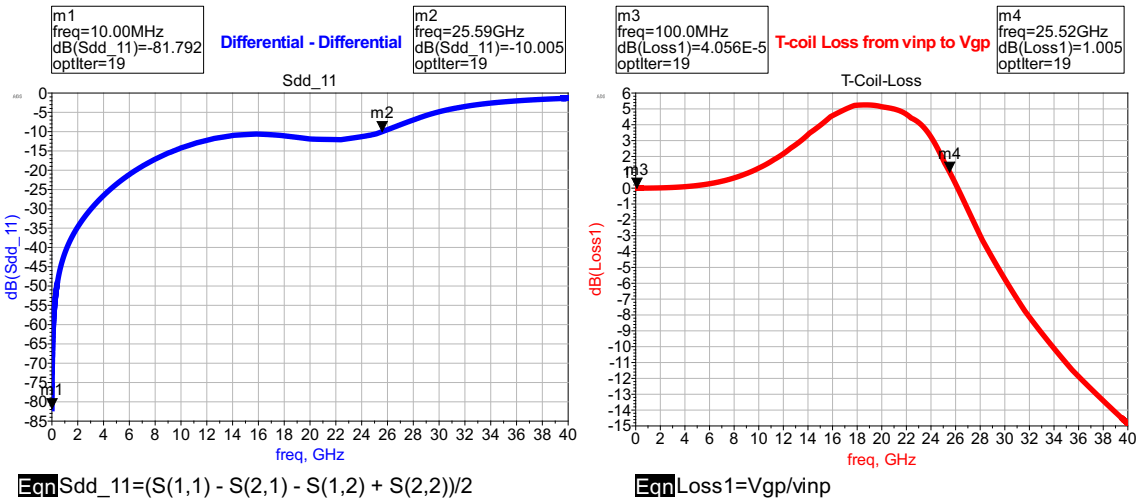


Figure 5.5: ADS results BSF

Using L_p, L_1, L_2, and C_B equal 267.3 pH, 192.9 pH, 220.1 pH, and 115.2 fF, respectively. The bandwidth results from cadence are plotted in Figure 5.6.

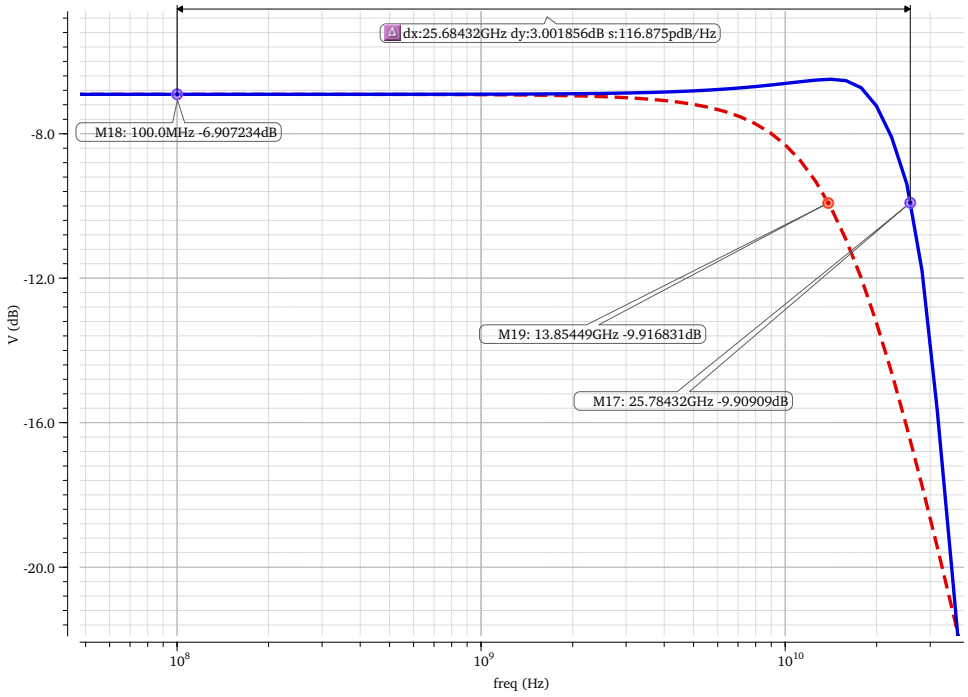


Figure 5.6: BSF frequency response in Cadence

Figure 5.6 shows the initial Bode diagram (red dashed curve) without the bridge T-coil, and the Bode diagram after the bridge T-coil implementation (blue curve). It can be concluded that the T-coil approach increases the initial bandwidth from 13.85 to 25.78 GHz, which means that the T-coil multiplies the original bandwidth by a factor of 1.86.

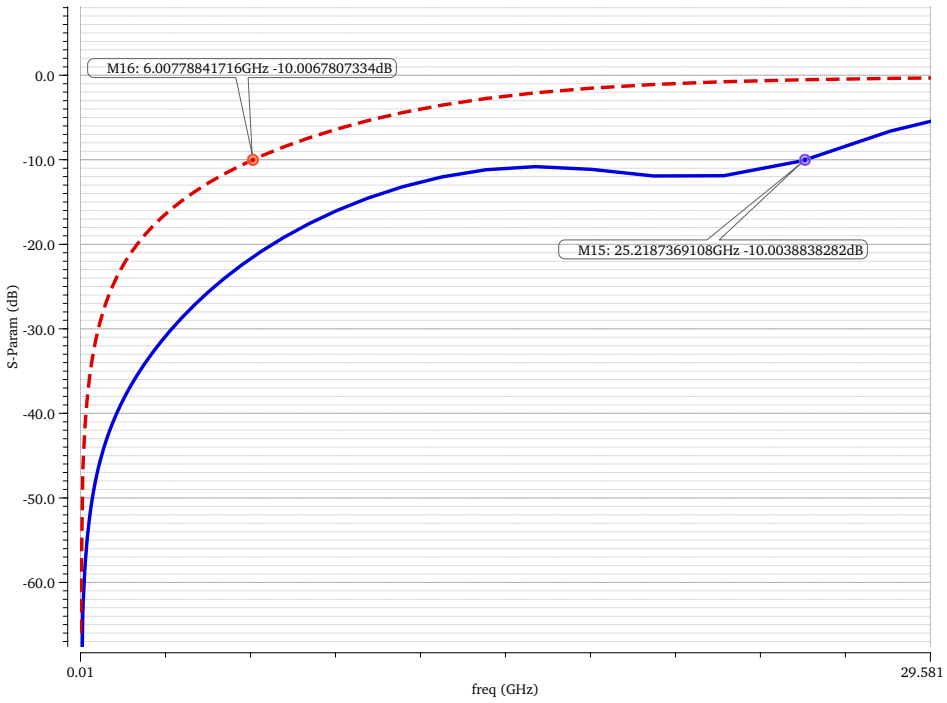


Figure 5.7: BSF return loss simulation in Cadence

In terms of input return loss, the cadence results are displayed in Figure 5.7, and it is possible to see that $S11_{dd}$ is lower than -10 dB up to 25.21 GHz whereas in the original bandwidth (red dashed line) was only lower than -10 dB until 6.01 GHz.

The linearity results obtained from Cadence are summarised in Figure 5.8.

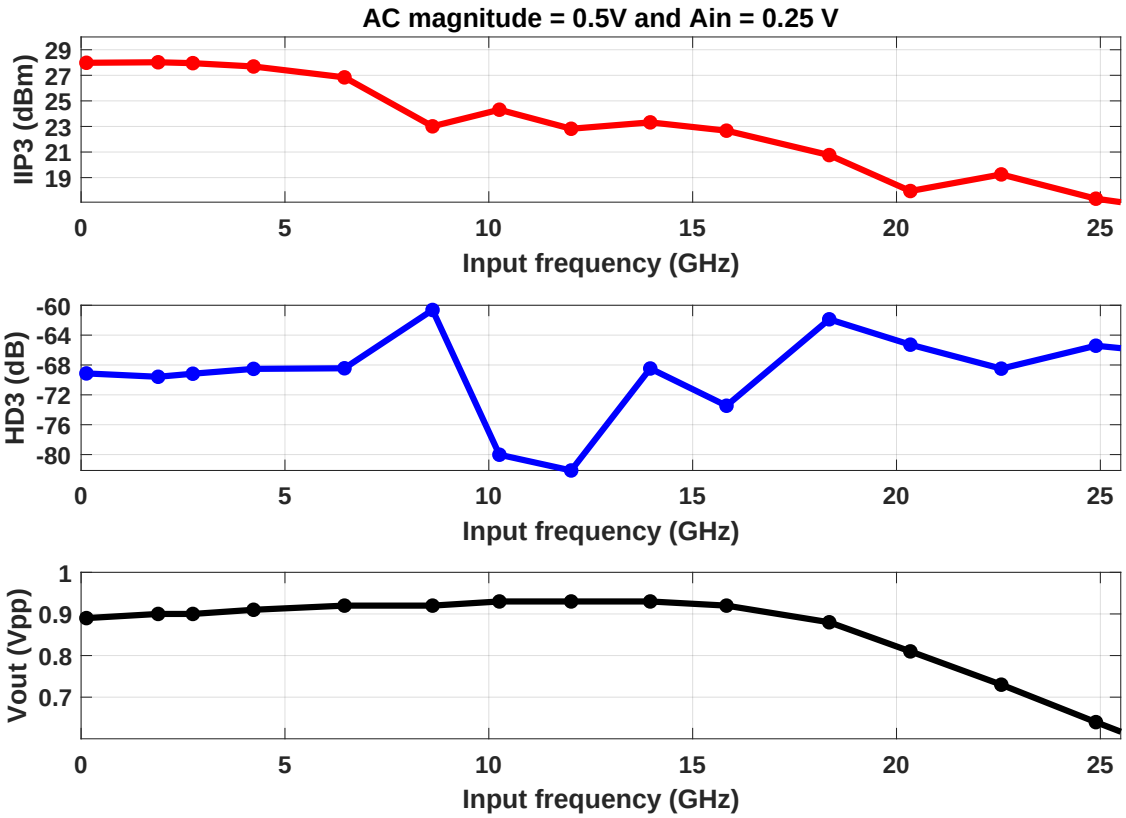


Figure 5.8: BSF linearity results with the bridge T-coil

Figure 5.8 revels that the $\mathbf{Vout}_{pp}$ is improved with the bridge T-coil and the $\mathbf{IIP3}_{LOW}$ values are only slightly worse than original values, Figure 4.14.

As a final point, Figure 5.5 and Figure 5.7 demonstrates that the simulated results match in ADS and in Cadence.

5.1.3 RC Assisted Buffer

As stated before, only third scenario from the RC assisted buffer meets the linearity requirements as IIP3 is higher than 23 dBm. Therefore, only the third scenario methodology is displayed in detail.

The results from the RC assisted buffer-scenario 3 in ADS are $S11_{dd}$ lower than -10 dB up to 7.70 GHz and no T-coil attenuation until 7.60 GHz. The former is true with C_B, L_1, L_1, and L_p of 367.7 fF, 843.0 pH, 914.7 pH, and 415.8 pH, respectively, as shown in Figure 5.9.

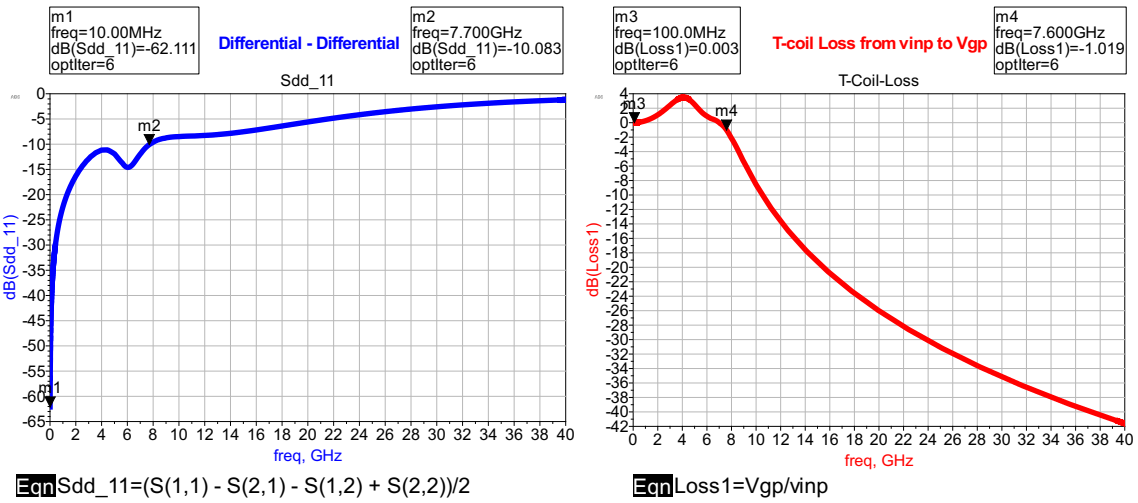


Figure 5.9: ADS results RC assisted buffer-scenario 3

Figure 5.10 details the bandwidth improvement in the RC assisted buffer, where the T-coil multiplies the original bandwidth by a factor of 1.50. Quantitatively from 4.74 to 7.10 GHz.

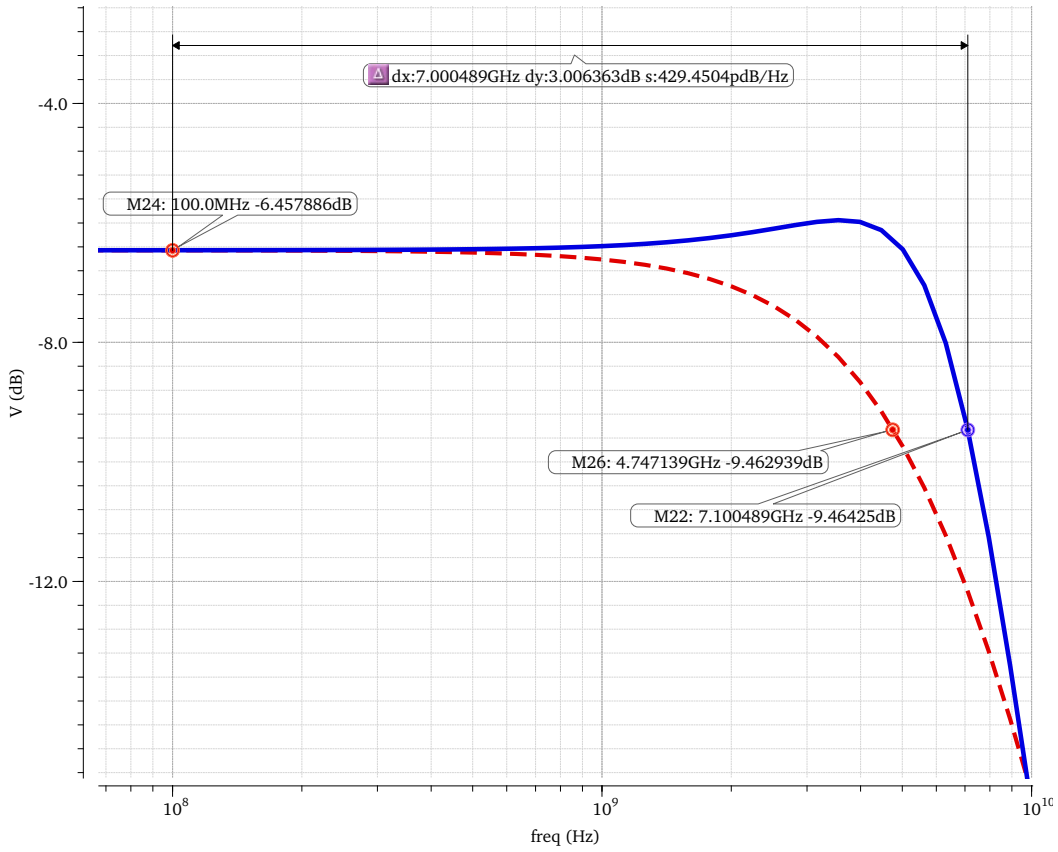


Figure 5.10: RC assisted buffer-scenario 3 frequency response in Cadence

Moreover, the measurement results for the input-match are depicted in Figure 5.11, and they are approximately the same as in the ADS software.

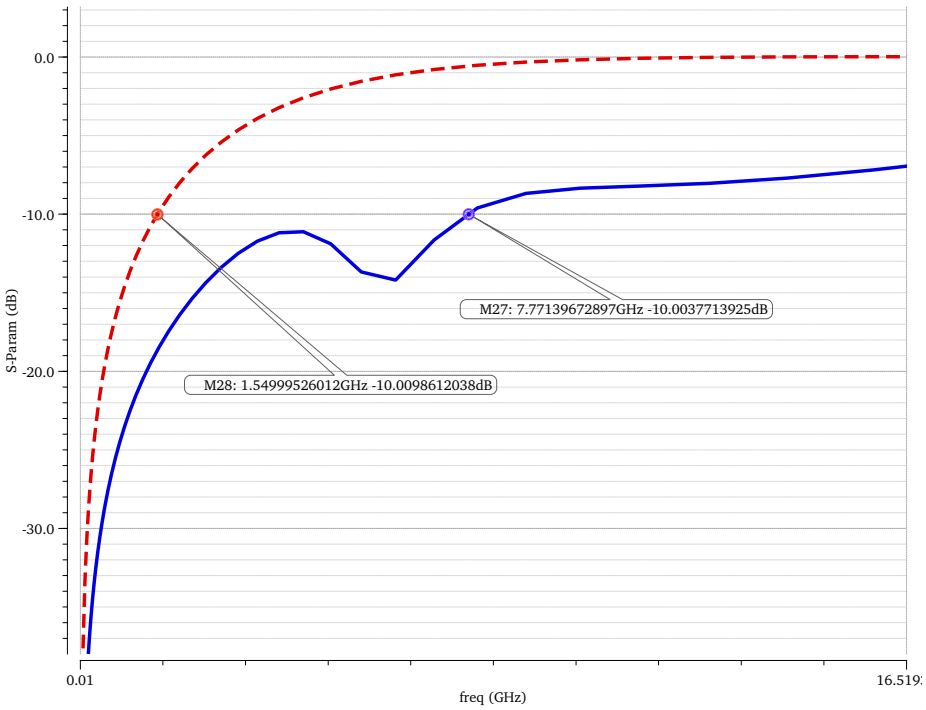


Figure 5.11: RC assisted buffer-scenario 3 return loss simulation in Cadence

It has to be noted that without the bridge T-coil the RC assisted buffer has 4.68 GHz of bandwidth but could only work up to 1.55 GHz with an acceptable input-match. On the other hand, the bridge T-coil and the series peaking set the RC assisted buffer to work until 7.77 GHz with a bandwidth extension of 2.36 GHz.

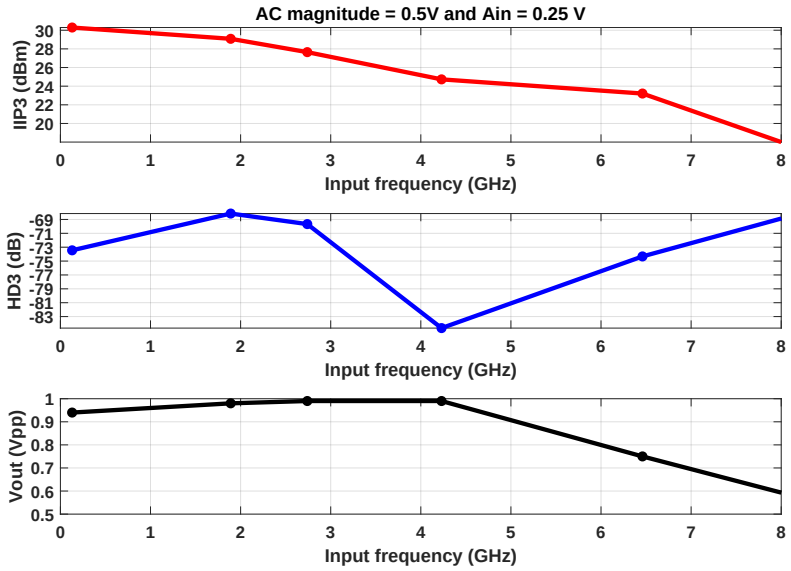


Figure 5.12: RC assisted buffer linearity results with the bridge T-coil

The transient results in Figure 5.12 show that the worst case of linearity inside the bandwidth equals 23.21 dBm, which is slightly higher than 23 dBm.

5.1.4 Basic push-pull

The Basic push-pull with output common mode voltage of 0.9V (scenario 2) is implemented in ADS and the results are displayed in Figure 5.13.

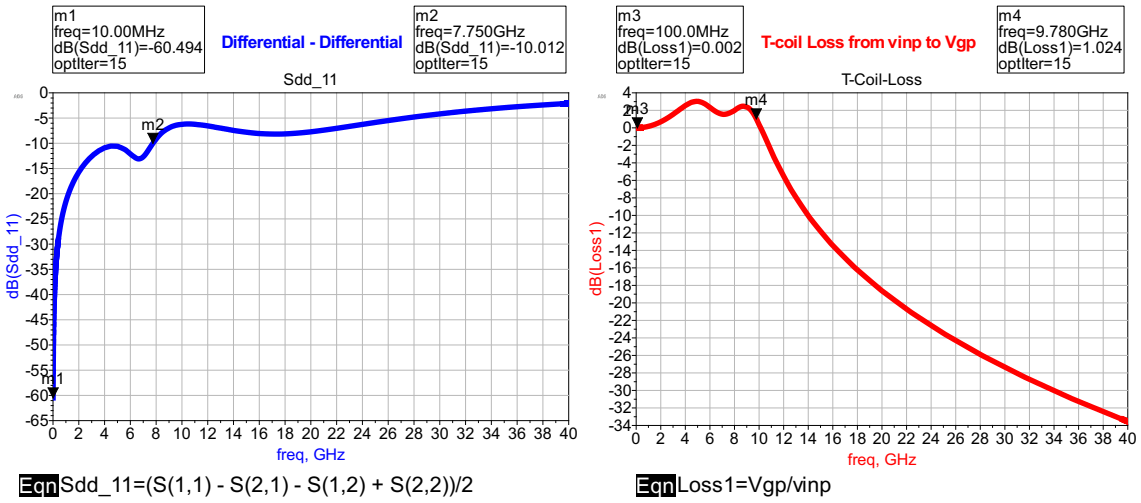


Figure 5.13: ADS results Basic push-pull

As detailed in Figure 5.13, the return loss is lower than -10 dB up to 7.75 GHz and no signal attenuation until 9.78 GHz.

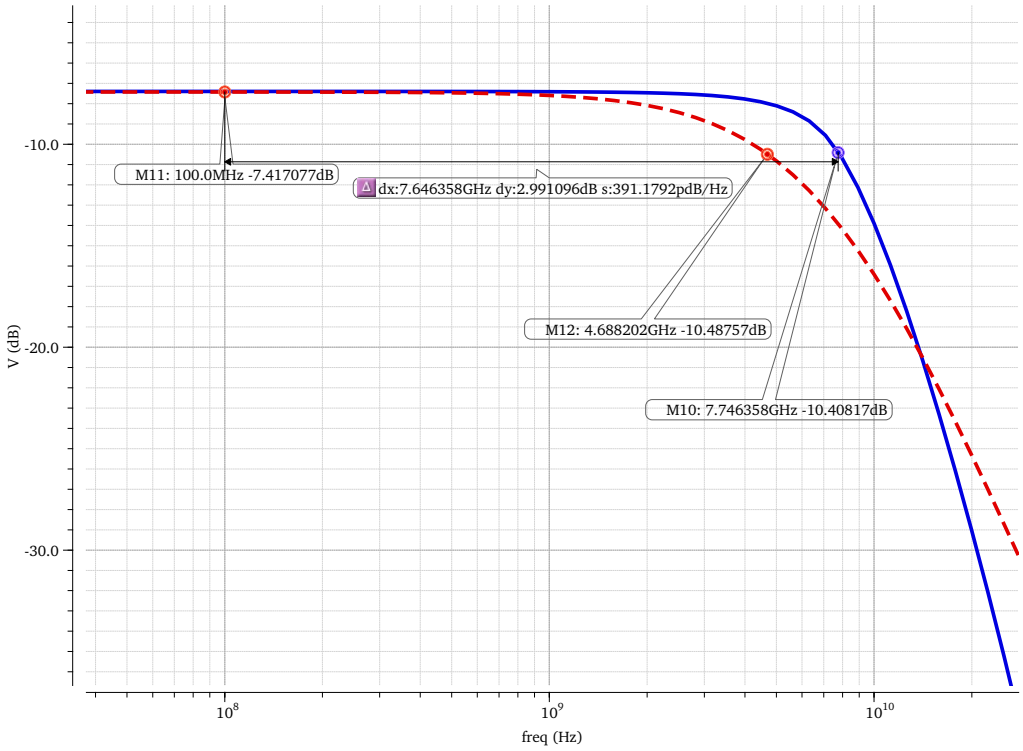


Figure 5.14: Basic push-pull frequency response in Cadence

The original bandwidth is increased from 4.68 to 7.74 GHz, a factor of 1.65 (see Figure 5.14).

With C_B, L_1, L_1, and L_p of 339.9 fF, 582.5 pH, 728.3 pH, and 270.3 pH, respectively, the return loss requirement is achieved up to 7.76 GHz, as shown in Figure 5.15.

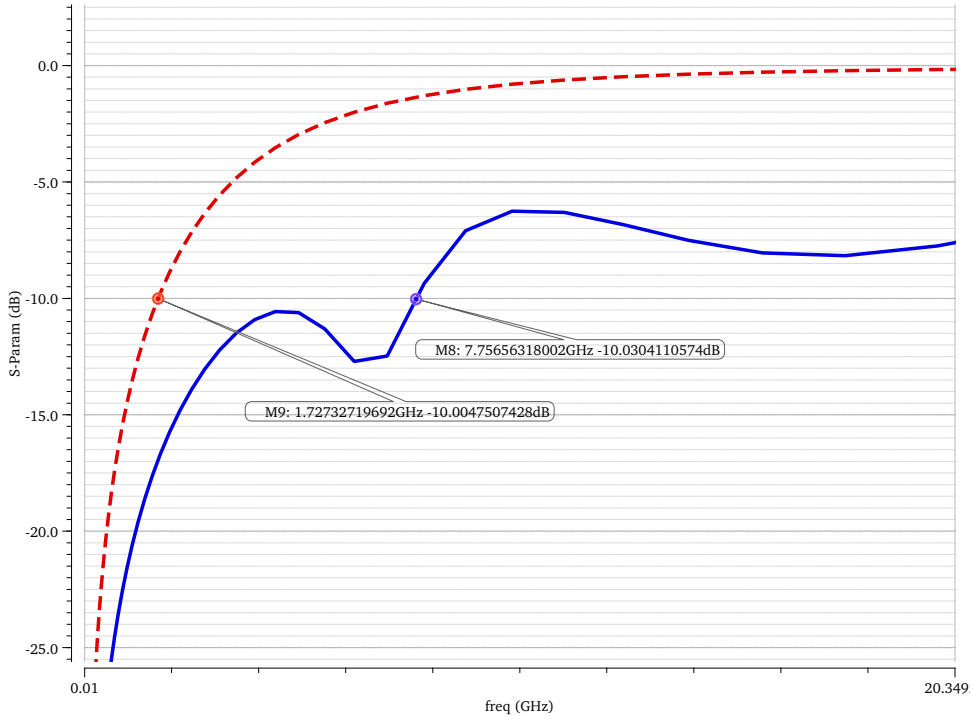


Figure 5.15: Basic push-pull return loss simulation in Cadence

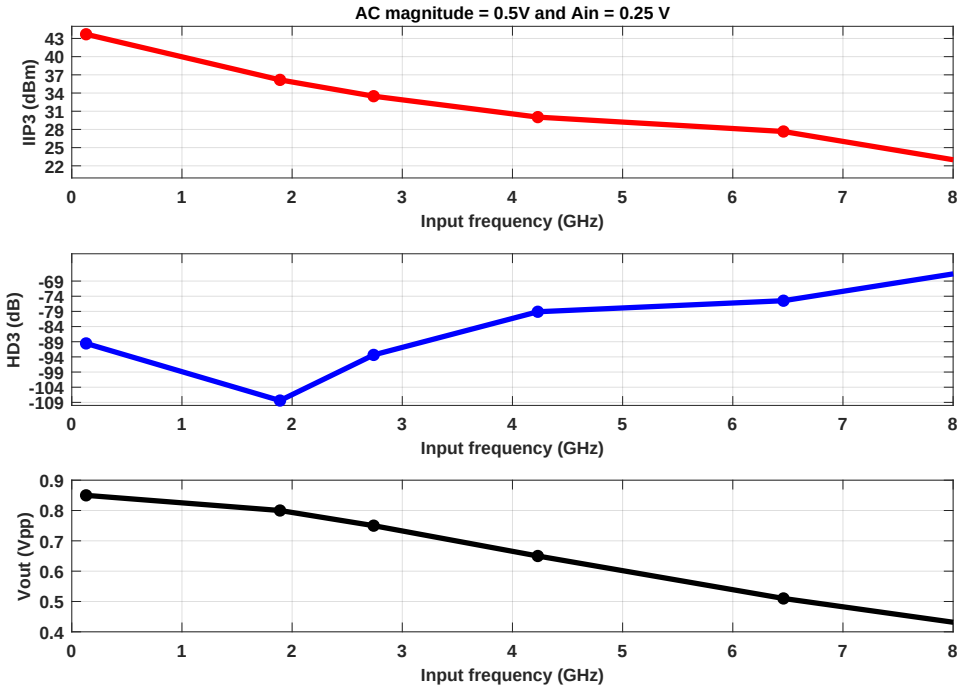


Figure 5.16: Basic push-pull linearity results with the bridge T-coil

Regarding linearity, the Basic push-pull has good linearity values. For instance, in band

the worst value is 27.66 dBm, which is 4.66 dBm higher than the linearity specification (see Figure 5.16).

5.1.5 Push-pull

The Push-pull results are provided in Figure 5.17 with C_B, L_1, L_1, and L_p of 425.2 fF, 1079 pH, 1400 pH, and 151.6 pH, respectively.

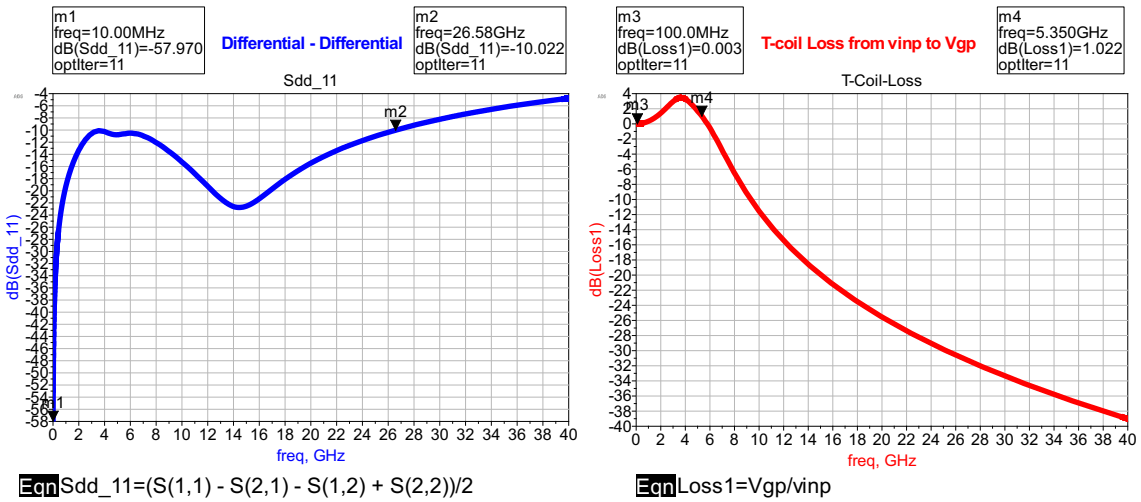


Figure 5.17: ADS results Push-pull

Interestingly, the Push-pull with the highest input capacitance improves the return loss up to 26.58 GHz, according to Figure 5.17.

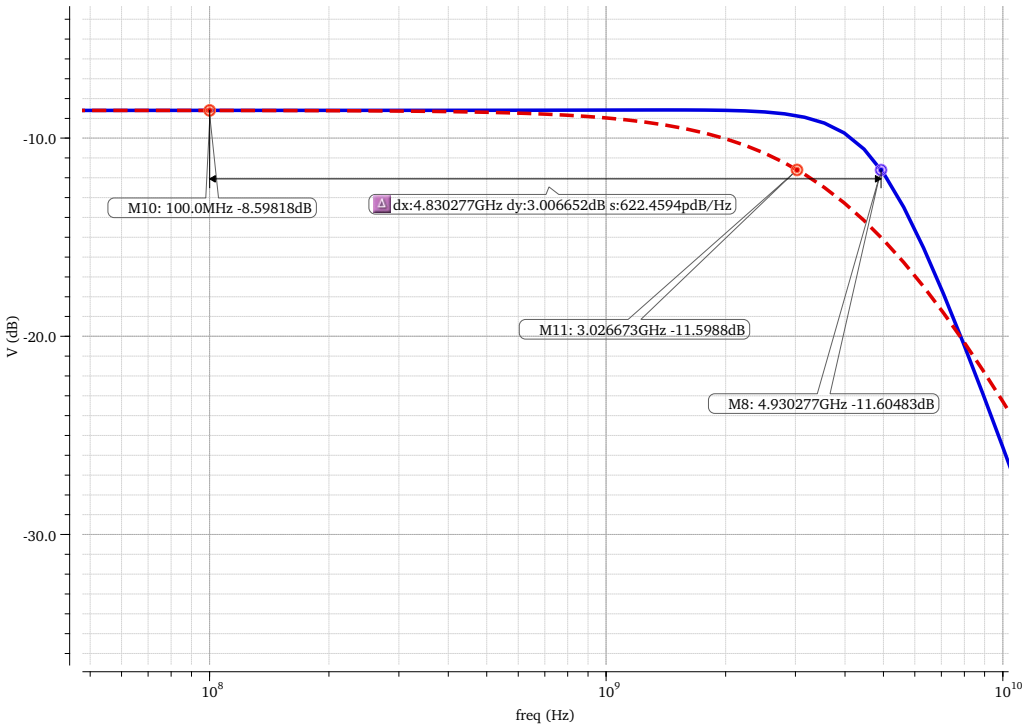


Figure 5.18: Push-pull frequency response in Cadence

Figure 5.18 details the bandwidth improvement for the Push-pull, where the T-coil multiplies the original bandwidth by a factor of 1.63, an increase of 1.9 GHz compared to the initial 3.03 GHz of bandwidth.

Additionally, the S-parameter analysis in Cadence returns the same results as ADS (see Figure 5.19).

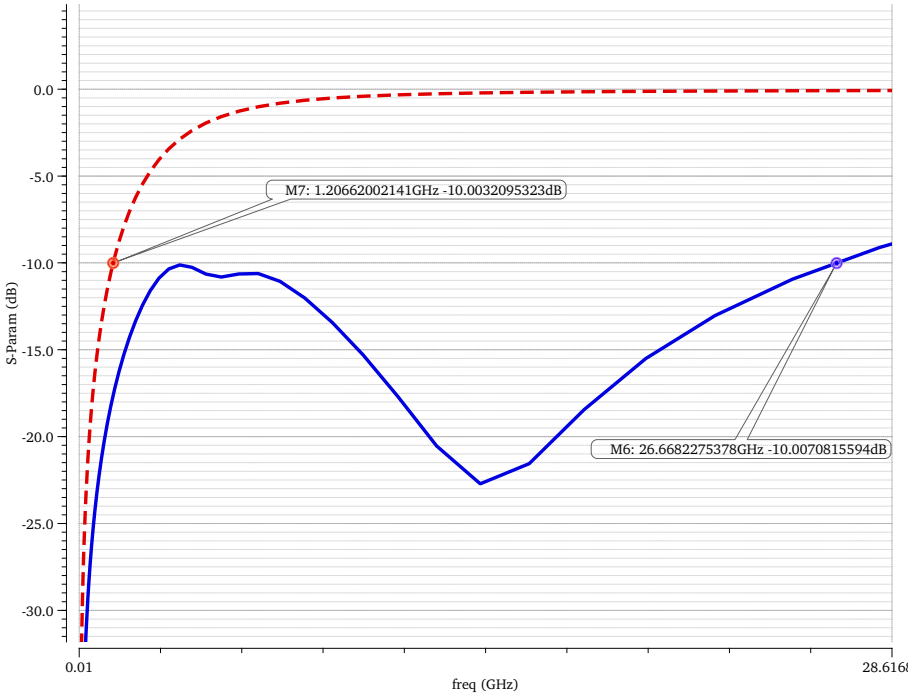


Figure 5.19: Push-pull return loss simulation in Cadence

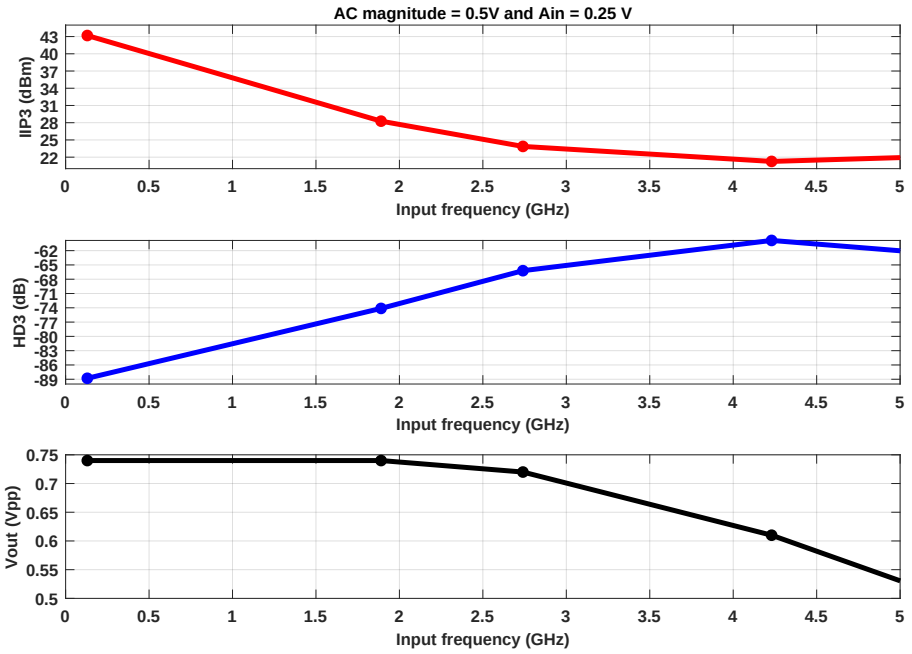


Figure 5.20: Push-pull linearity results with the bridge T-coil

Finally, the linearity results are exhibit in Figure 5.20, where the Push-pull achieves 21.26 dBm within band. Therefore, approximately meeting the linearity requirements.

An important thing to note is how small the differential output voltage is and how easily it degrades with frequency. The Push-pull has the higher number of $Caps$ in the input node leading to signal attenuation that reduces $Vout_{pp}$, as discussed in chapter 4.

5.1.6 Results

With the simulations performed, all the results are summarised in Table 5.1.

Table 5.1: T-coil simulation results

Topology	**BSF**	**RC assisted buffer**			**Basic push-pull**		**Push-pull**
$\mathbf{V}_{OCM}$ (V)	0.7	0.7			0.7	0.9	0.9
$\mathbf{C}_B$ (fF)	115.2	246.2	234.1	367.7	357.4	339.9	425.2
$\mathbf{L}_1$ (pF)	192.9	366.6	437.9	843.0	587.8	582.5	1079
$\mathbf{L}_2$(pF)	220.1	311.2	398.4	914.7	722.3	728.3	1400
$\mathbf{L}_p$ (pF)	267.3	410.2	406.8	415.8	565.9	270.3	151.6
Original BW (GHz)	13.85	9.88	9.11	4.74	4.63	4.68	3.03
Increasing factor	1.86	1.35	1.36	1.50	1.67	1.65	1.63
Bandwidth (GHz)	**25.78**	**13.29**	**12.35**	**7.10**	**7.71**	**7.74**	**4.93**
$\mathbf{S}_{11_{dd}}$ = -10 dB (GHz)	**25.21**	**13.44**	**13.50**	**7.77**	**8.00**	**7.76**	**26.67**
$\mathbf{IIP3}_{min}$ (dBm)	**17.35**	**14.17**	**16.6**	**23.21**	**29.47**	**27.66**	**21.26**
Noise (μV_{rms})	205.2	185.7	177.4	133.9	104.4	105.2	85.3

It is worth mentioning that the DC gain are not included in Table 5.1 because the T-coil components are without ohmic resistance, which means that the DC gain did not changed from chapter 4.

The simulation results demonstrate that linearity and the noise results are slightly worse compared to chapter 4. However, the bandwidth is improved between 1.35 and 1.86 with input-match, which is a significant improvement.

5.2 Distributed Approach

The idea behind distributed approach is to increase the bandwidth and improve the return loss by using the buffer parasitic capacitance as an element to build the transmission line equivalent schematic.

A transmission line could be represented as two coils and one capacitance or one coil and two capacitances, as shown in Figure 5.21, where Z_0 is the real part and is equal to $Z_0 = \sqrt{\frac{L}{C}}$.

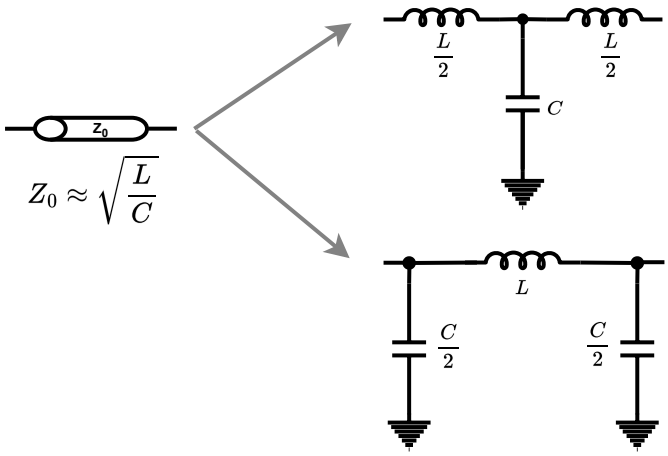


Figure 5.21: Transmission line equivalent schematic

It is clear that the equivalent schematic is an approximation, but mathematically can be proven that $Z_0 = \sqrt{\frac{L}{C}}$. If the T-line equivalent schematic is considered, to have input-match Z_{in} has to be equal to Z_0 with a source impedance of 50 Ω.

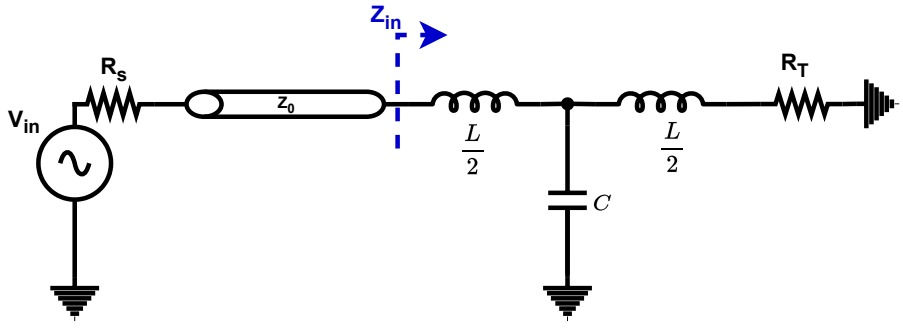


Figure 5.22: Input-match calculation

From Figure 5.22 Z_{in} is equal to:

$$Z_{in} = \left[\left(s \cdot \frac{L}{2} + R_T\right) // \frac{1}{s \cdot C}\right] + s \cdot \frac{L}{2} \tag{5.3}$$

where the real part and the imaginary part are equal to:

$$\begin{aligned}\Re(Z_{in}) &= \left\{\frac{R_T}{s^4\left(\frac{L}{2}\right)^2 c^2 + s^2\left(LC - C^2R_T^2\right) + 1}\right\} \\ \Im(Z_{in}) &= \left\{\frac{s^5\left(\frac{L}{2}\right)^3 C^2 + s^3\left(2\left(\frac{L}{2}\right)^2 C - C^2\frac{L}{2}R_T^2 + \left(\frac{L}{2}\right)^2 C\right) + s\left(L - CR_T^2\right)}{s^4\left(\frac{L}{2}\right)^2 c^2 + s^2\left(LC - C^2R_T^2\right) + 1}\right\}\end{aligned} \tag{5.4}$$

To have input-match $\Re(Z_{in}) = R_s$ and $\Im(Z_{in}) = 0$, meaning that the circuit is sized to deliver the maximum available power. Nevertheless, the price to pay for the added power is the increased noise figure because there is always a trade-off between noise and return loss. By performing some algebraic manipulations, $\Re(Z_{in}) = R_s$ and $\Im(Z_{in}) = 0$, provide the following equations:

$$s = j\omega = \pm\sqrt{\frac{{R_T}^2}{\left(\frac{L}{2}\right)^2} - \frac{4}{LC}} \quad \cup \quad s = \pm\frac{j}{\sqrt{C}\sqrt{\left(\frac{L}{2}\right)^2}} \quad \cup \quad s = \pm\frac{\sqrt{C{R_T}^2 - L}}{\sqrt{C}\frac{L}{\sqrt{2}}} \tag{5.5}$$

Equalizing the Laplace variable, the solution is $L = {R_T}^2 C$.

$$\sqrt{\frac{R_T^2}{\left(\frac{L}{L}\right)^2} - \frac{4}{LC}} = \sqrt{\frac{C{R_T}^2 - L}{C \cdot \frac{L^2}{2}}} \quad (=) \tag{5.6}$$

$$(=) \quad \cancel{L = 0} \quad \cup \quad L = {R_T}^2 C \tag{5.7}$$

Equation 5.7 with the termination resistor R_T equal to Z_0 demonstrates that it's possible to have input-match if both inductors in the schematic are 1250 times bigger than the capacitance C.

5.2.1 Topology and Sizing Strategy

The topology for this distributed approach is detailed in Figure 5.23. As stated before, the buffer parasitic capacitance can be used as a component to build the transmission line equivalent schematic. Figure 5.23 indicates how to convert circuit capacitances into T-line structures by associating each capacitor with two inductors.

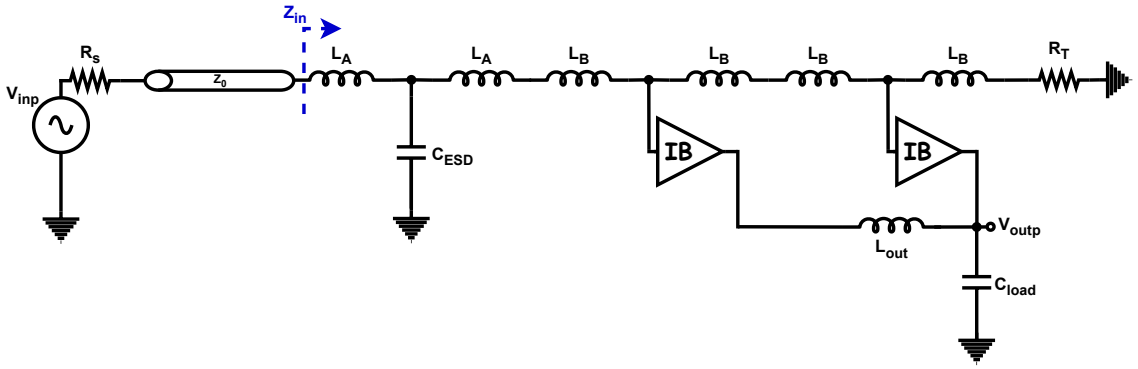


Figure 5.23: Distributed approach architecture

As demonstrated above, the inductors L_A and L_B are parameterized using the formula $L = \frac{50^2}{2}C$.

The circuit components C_{Buffer}, C_{ESD}, and L_{out} are estimated through simulation, such that the signals coming out of the two IB are added constructively. Additionally, L_A is equal to $\frac{50^2}{2}C_{ESD}$, and L_B is $\frac{50^2}{2}C_{Buffer}$.

The achieved bandwidth and input-match for each topology is shown in the following sections.

5.2.2 Basic Source Follower

With M2 multiplier equal to 49 and M1 multiplier equal 30 the BSF capacitance (C_{buffer}) has the maximum value of 130 fF across frequency. C_{ESD} has the maximum value of 115 fF and is the same for all topologies.

The BSF Bode diagram is displayed in Figure 5.24, where the BSF bandwidth with the distributed approach is 24.26 GHz.

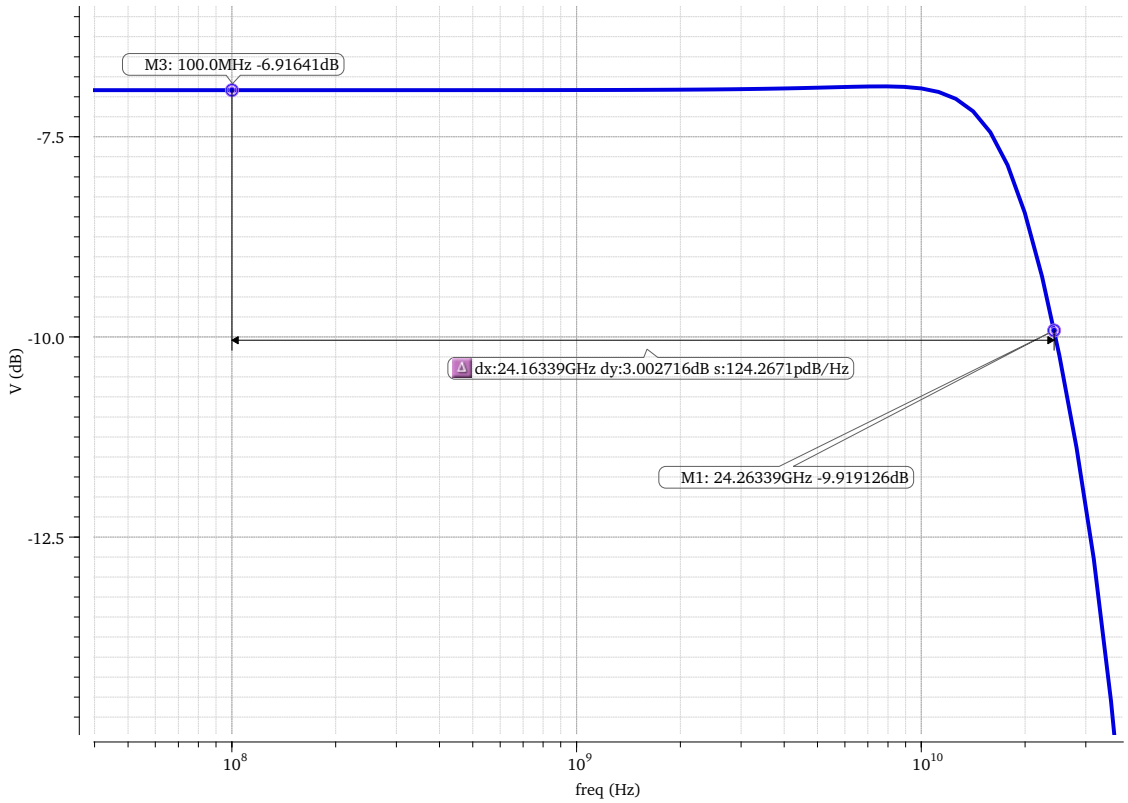


Figure 5.24: BSF frequency response - distributed approach

The return loss across frequency is in Figure 5.25, and the input-match is acceptable until 34.31 GHz.

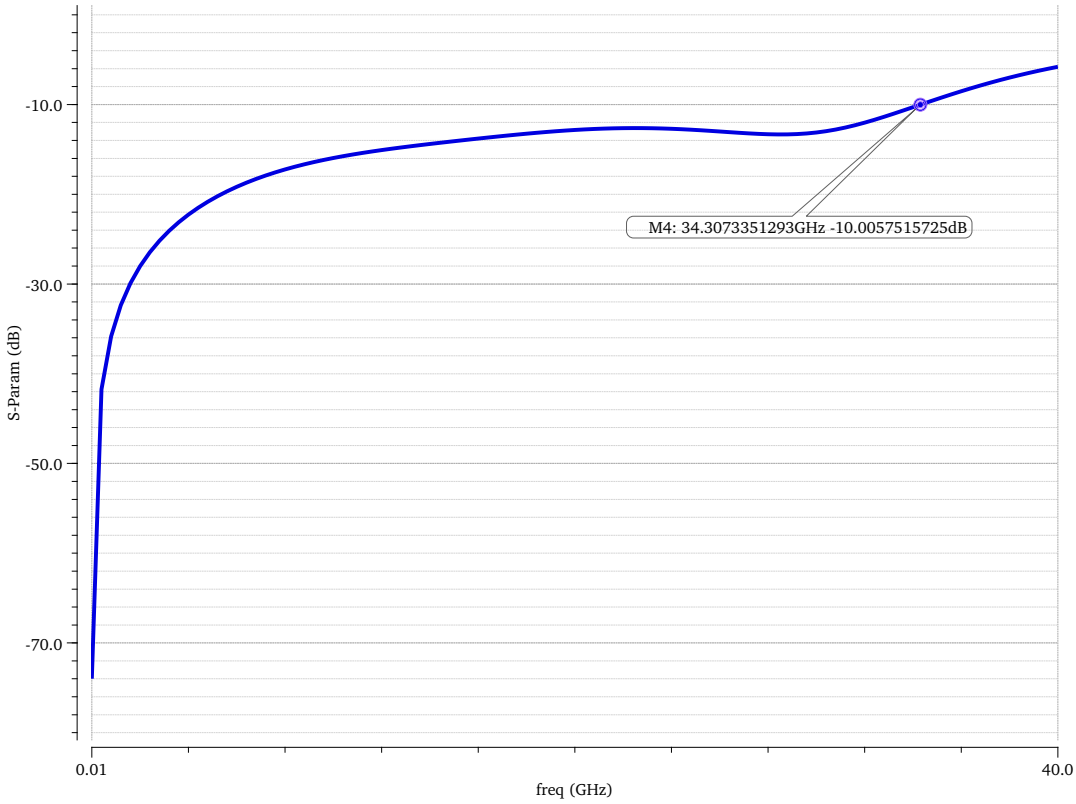


Figure 5.25: BSF return loss simulation - distributed approach

The BSF linearity results with the distributed approach are in Figure 5.26.

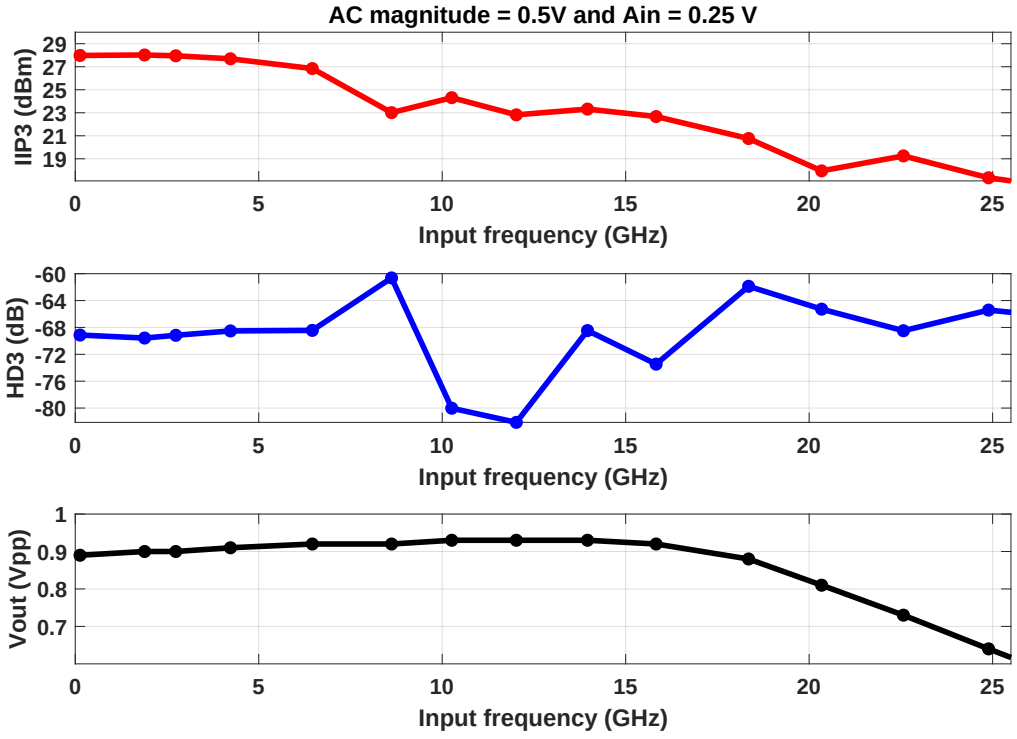


Figure 5.26: BSF linearity results with the distributed approach

Figure 5.26 demonstrates that the linearity results from the distributed approach are much worse than the T-coil results.

5.2.3 RC Assisted Buffer

The RC assisted buffer is sized with M2, M1, and M3 multiplier of 14, 30, and 11, respectively. C_{Buffer} max value is 500 fF for a capacitance Cap value of 1 pF. Lastly, the best extracted value for L_{out} from simulation was 560 pH.

As result, the bandwidth is approximately 13.38 GHz.

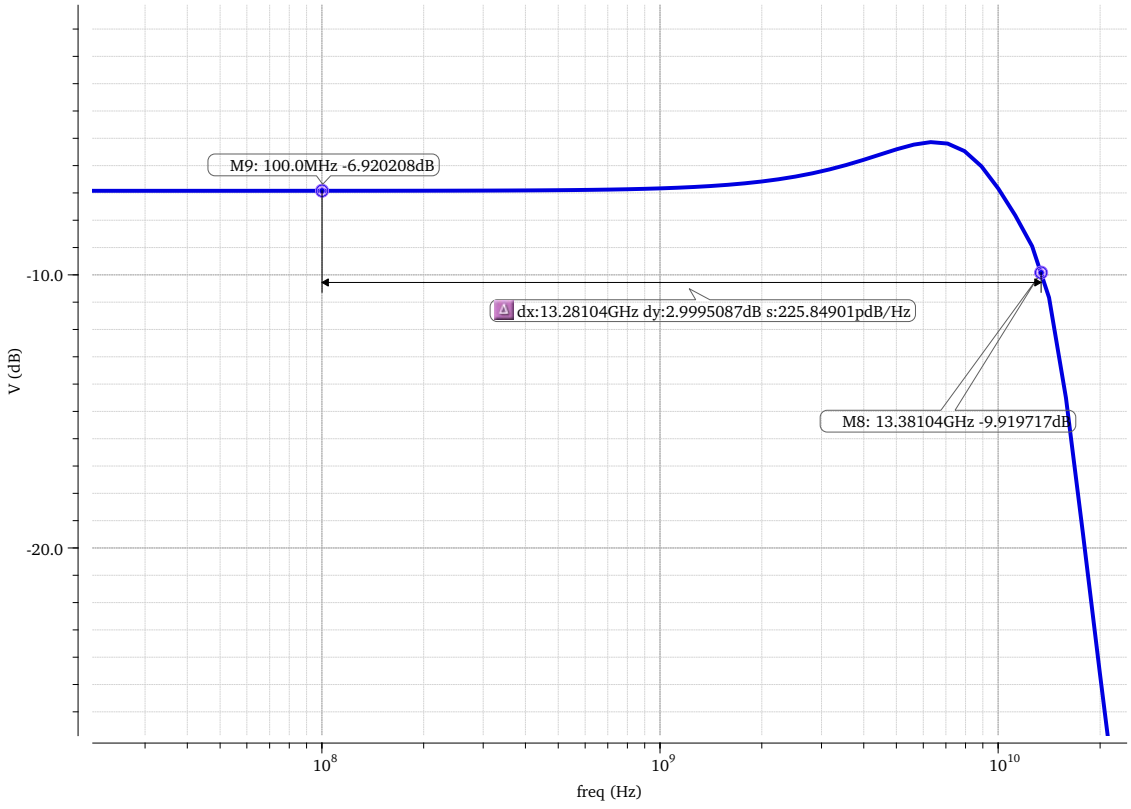


Figure 5.27: RC assisted buffer frequency response - distributed approach

The return loss across frequency is given in Figure 5.28, and the input-match is acceptable until 14.24 GHz.

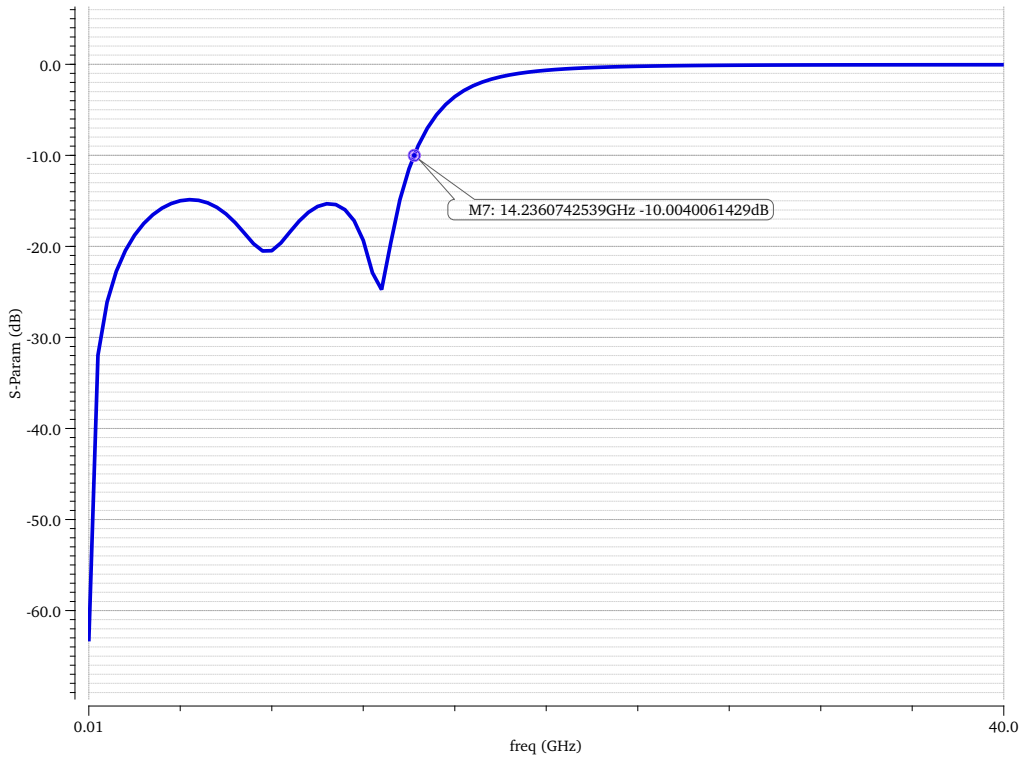


Figure 5.28: RC assisted buffer return loss simulation - distributed approach

It has to be noted that the linearity results for this topology are degraded compared to the T-coil results, as detailed in Figure 5.29.

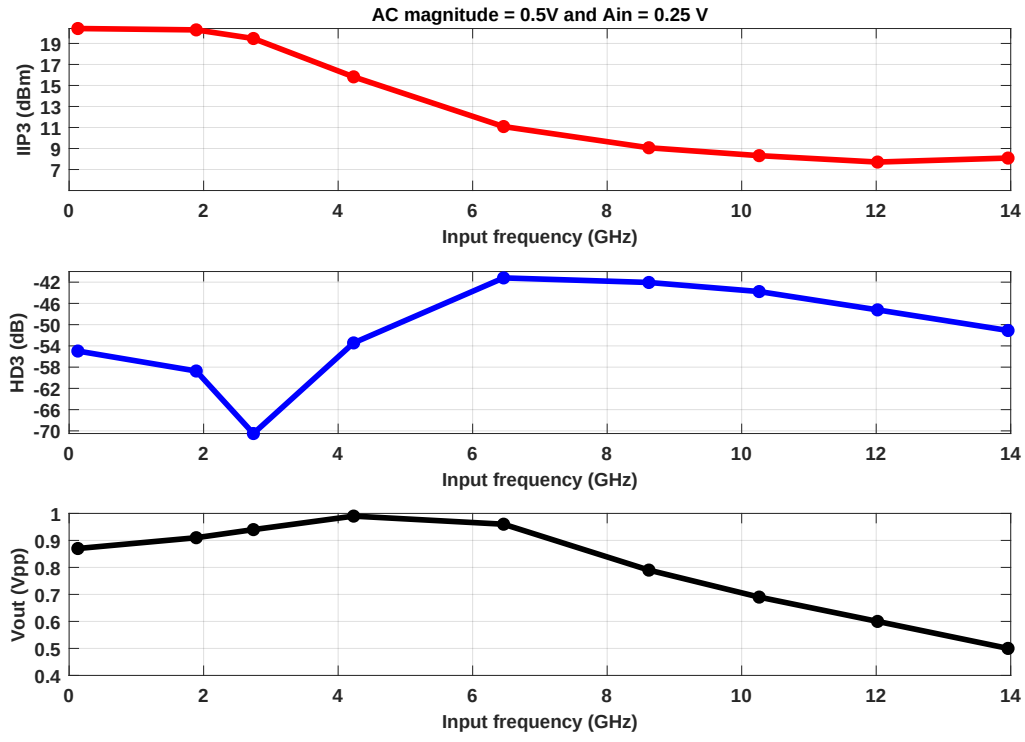


Figure 5.29: RC assisted buffer linearity results with the distributed approach

5.2.4 Basic push-pull

For the Basic push-pull, a Cap of 1pF, multipliers of 40, results in a buffer capacitance of 610 fF with L_{out} equal to 610 pH. The circuit bandwidth is 11.11 GHz (see Figure 5.30).

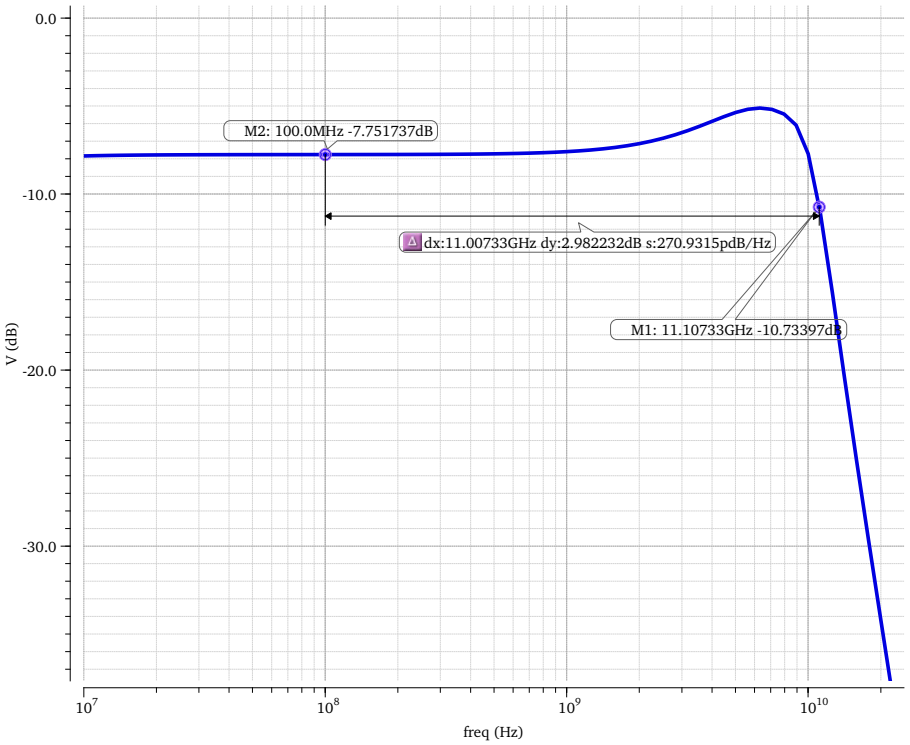


Figure 5.30: Basic push-pull frequency response - distributed approach

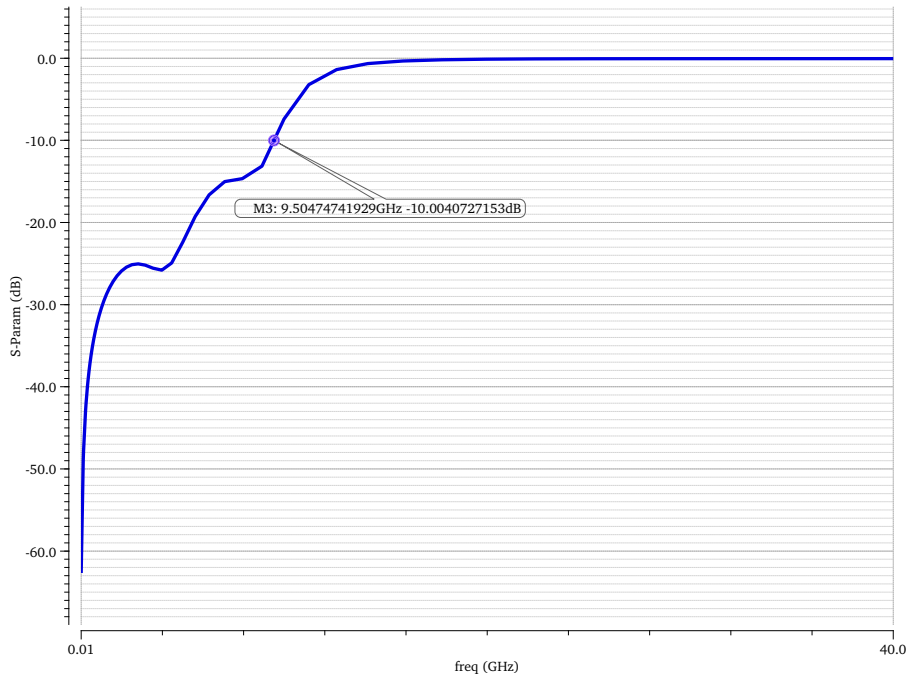


Figure 5.31: Basic push-pull return loss simulation - distributed approach

The return loss equals to -10 dB at 9.5 GHz, which is not a satisfactory result as bandwidth is 11.11 GHz, as shown in Figure 5.31.

Regarding linearity, the Basic push-pull is the one with the best linearity values. For instance, in the band the worst value is 20.49, which however is still lower than the linearity specification.

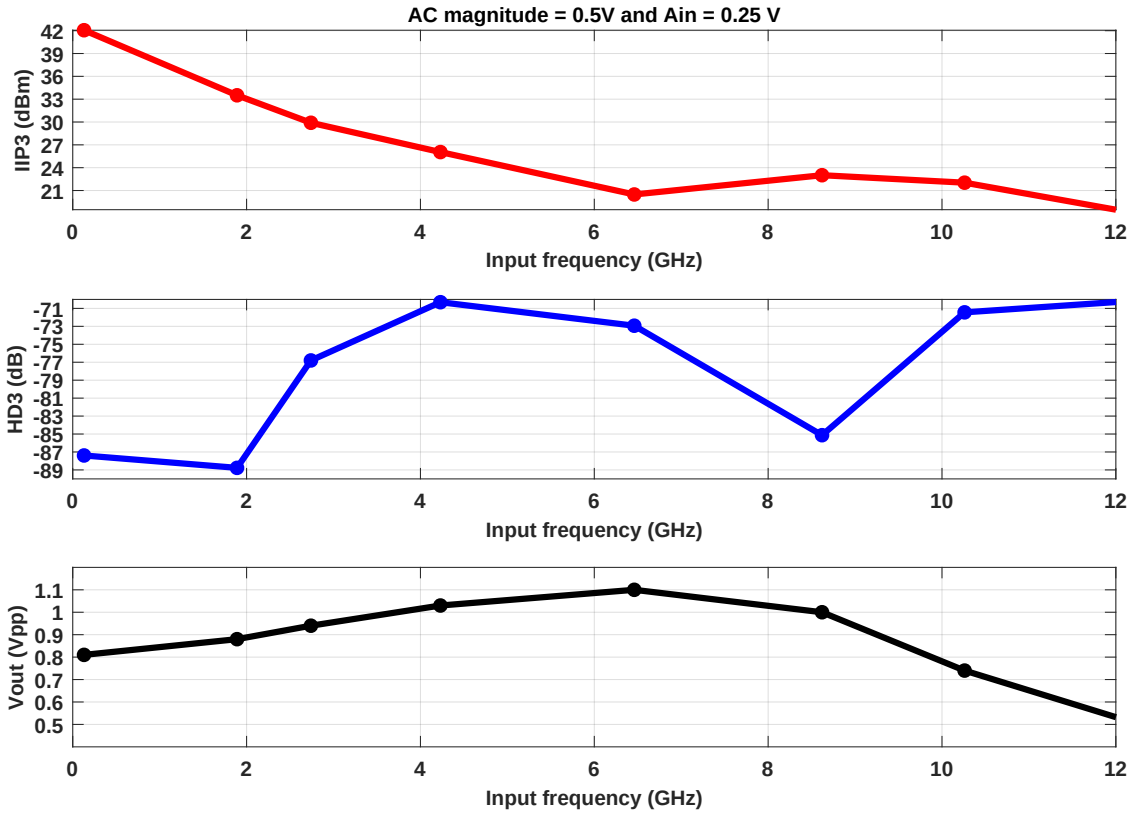


Figure 5.32: Basic push-pull linearity results with the distributed approach

5.2.5 Push-pull

The Push-pull bandwidth results are shown in Figure 5.17 with C_{ap}, M1, M2, M3, and M4 multipliers of 0.8 pF, 5, 5, 10, 10, respectively. This results in a bandwidth of 5.11 GHz with L_{out} of 360 pH and C_{buffer} of 600 fF.

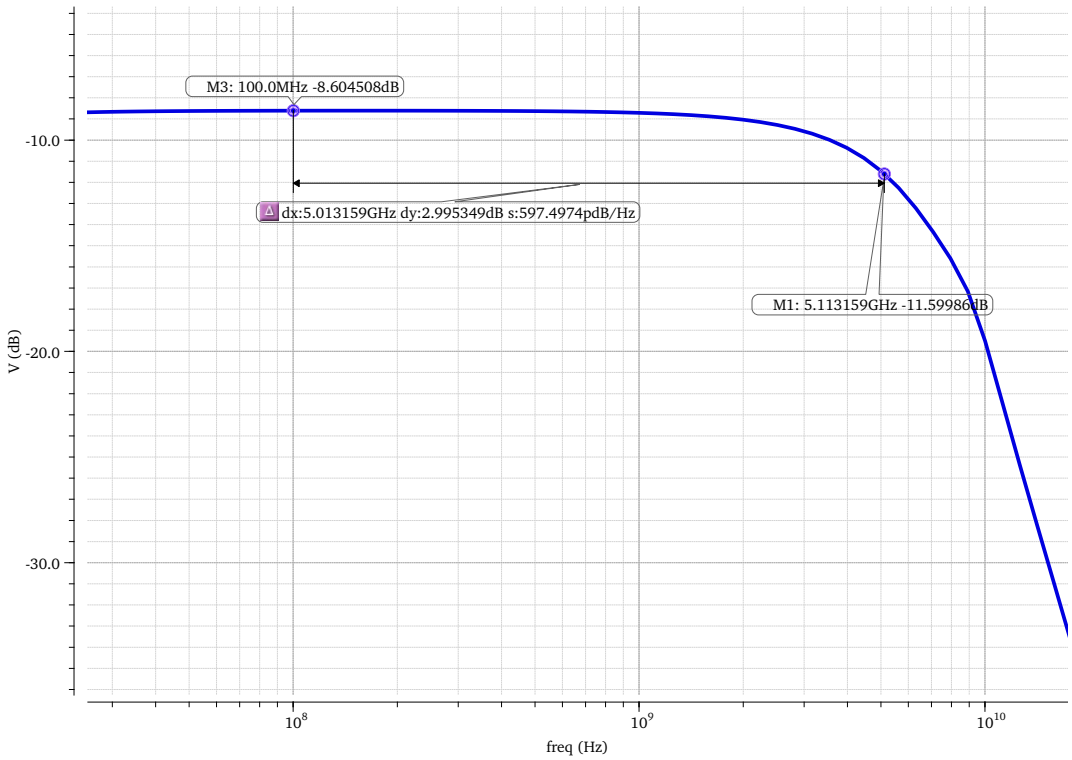


Figure 5.33: Push-pull frequency response - distributed approach

Figure 5.34 details the return loss improvement for the Push-pull, where $S_{11_{dd}}$ is lower than -10 dB up to 8.76 GHz.

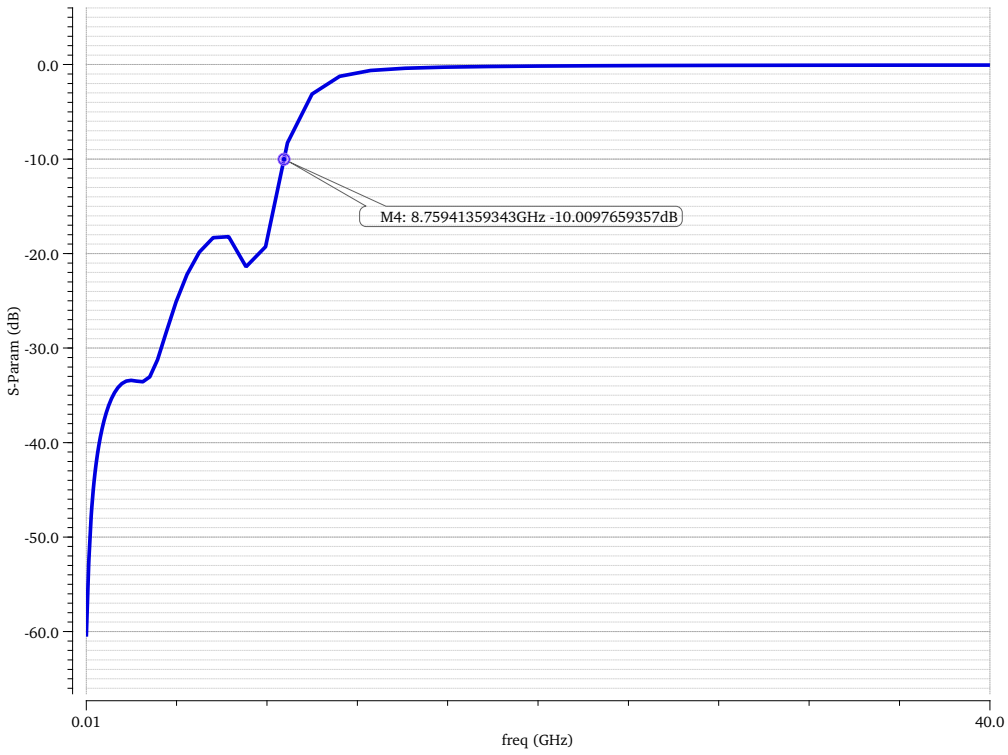


Figure 5.34: Push-pull frequency response in Cadence

Finally, the linearity results are exhibited in Figure 5.35, where the Push-pull assumes 15.28 dBm within band. Therefore, not meeting the linearity requirements.

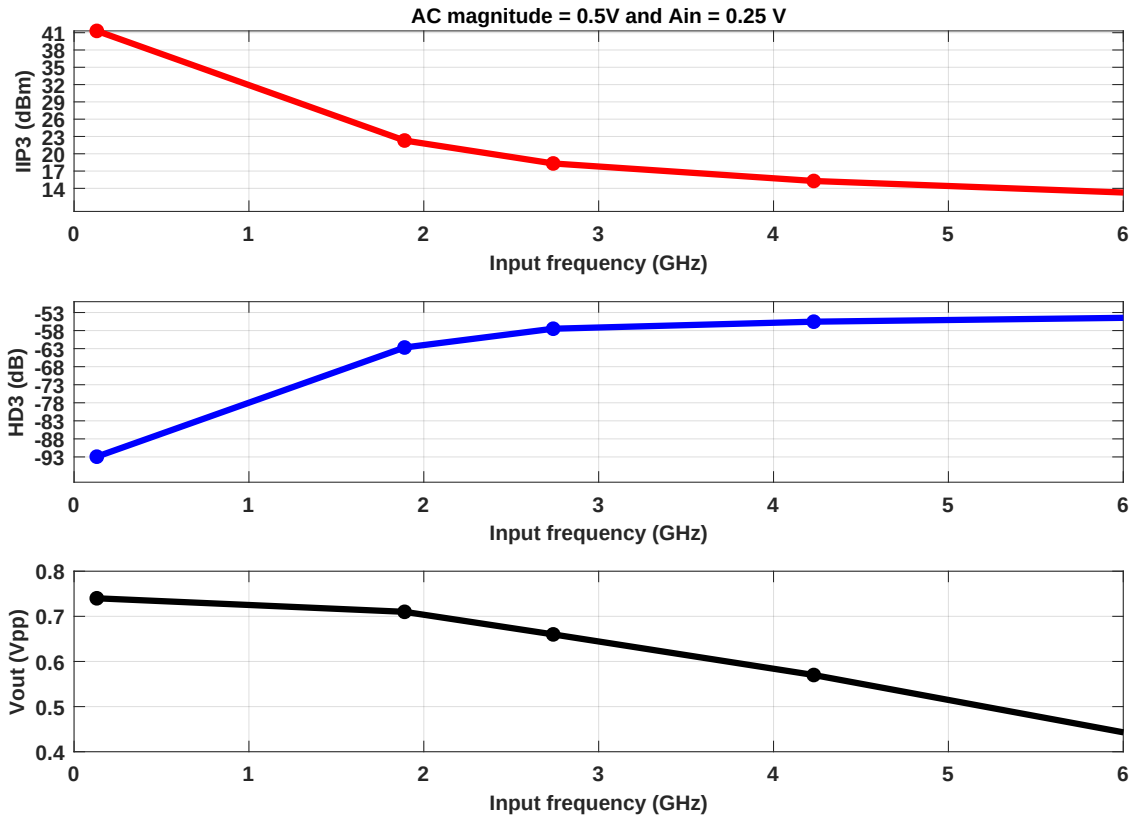


Figure 5.35: Push-pull linearity results with the distributed approach

5.2.6 Results

With the distributed approach simulations performed, all the results are summarised in Table 5.2.

Table 5.2: Distributed approach simulation results

Topology	**BSF**	**RC Assisted Buffer**	**Basic push-pull**	**Push-pull**
V_{OCM} (V)	0.7	0.7	0.9	0.9
C_{ESD} (fF)	118			
C_{buffer} (fF)	130	500	610	600
L_{out} (pH)	69	560	510	360
DC gain (dB)	-6.92	-6.92	-7.75	-8.60
Bandwidth (GHz)	**24.26**	**13.38**	**11.11**	**5.11**
$S_{11_{dd}}$ = -10 dB (GHz)	**34.31**	**14.24**	**9.50**	**8.76**
IIP3$_{min}$ (dBm)	17.68	7.71	20.48	15.28
Noise (μV_{rms})	200.0	151.7	122.1	90.7

It can be seen that only the BSF has more than 18 GHz of bandwidth but does not meet the linearity requirements. Furthermore, all designs have a noise level of less or equal to

200 μV_{rms}, and none of the topologies with the distributed approach reaches the 23 dBm of IIP3.

5.3 Conclusion

With both bandwidth extension techniques analyzed it can be concluded that the bridge T-coil and the distributed approach degrades the area, noise, and linearity compared with the results obtained in chapter 4. However, there is a considerable bandwidth extension when a low input capacitance is driven by both techniques, for instance the BSF (see Table 5.3).

Table 5.3: Bandwidth extension techniques simulation results

Topology	**BSF**	**RC Assisted Buffer**	**Basic push-pull**	**Push-pull**
$\mathbf{V}_{OCM}$ (V)	0.7	0.7	0.9	0.9
	Bridge T-coil and Series Peaking			
DC gain (dB)	-6.91	-6.46	-7.39	-8.60
Bandwidth (GHz)	**25.78**	**7.10**	**7.74**	**4.93**
$\mathbf{S11}_{dd}$ = -10 dB (GHz)	**25.21**	**7.77**	**7.76**	**26.67**
$\mathbf{IIP3}_{min}$ (dBm)	17.35	23.21	27.66	21.26
Noise (μV_{rms})	205.2	133.9	105.2	85.3
DC power (mW)	178.20	81.00	17.24	9.83
	Distributed Approach			
DC gain (dB)	-6.92	-6.92	-7.75	-8.60
Bandwidth (GHz)	**24.26**	**13.38**	**11.11**	**5.11**
$\mathbf{S11}_{dd}$ = -10 dB (GHz)	**34.31**	**14.24**	**9.50**	**8.76**
$\mathbf{IIP3}_{min}$ (dBm)	17.68	7.71	20.48	18.32
Noise (μV_{rms})	200.0	151.7	122.1	90.7
DC power (mW)	119.02	35.35	32.69	6.60

As detailed in the simulation results, the bridge T-coil has better linearity and area. On the other hand, the distributed approach has a low power consumption for the same bandwidth.

Moreover, the linearity and bandwidth results for all topologies are detailed in Figure 5.36. The curves in the graph represent how IIP3 varies with frequency for each topology.

Where dashed lines represent the distributed approach technique, and the full curves represent the T-Coil technique. Furthermore, the curves terminate at a frequency equal to the bandwidth.

It is worth noting that if the inductors used in both techniques have a resistive part, the DC gain from the distributed approach will be much lower than in the bridge T-coil as more inductors are used for the distributed approach, meaning larger signal attenuation.

At this point of the project, the closest topology to meet the specifications is the BSF with series peaking and bridge T-coil implementation. It has 25.78 GHz of bandwidth

with an input-match up to 25.21 GHz. However, the noise and the linearity requirements are almost reached, $IIP3_{min}$ of 20.76 dBm until 18 GHz and 205.2 μV_{rms}.

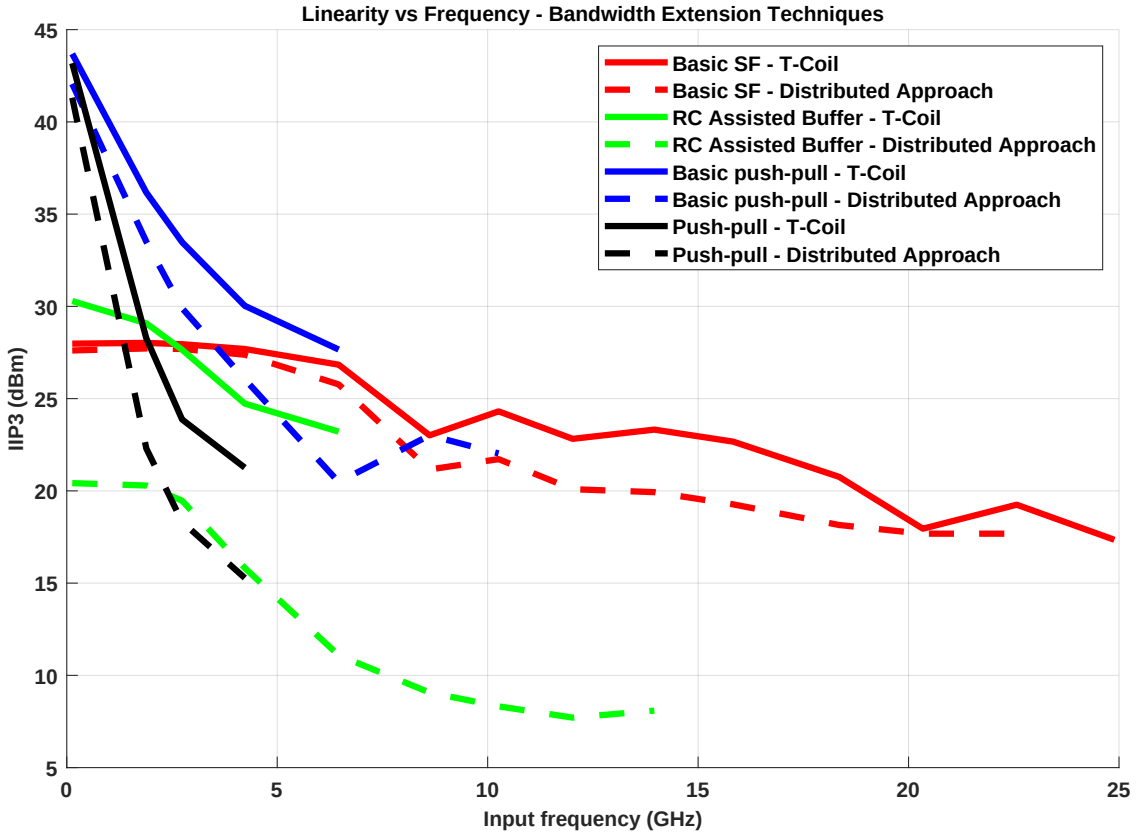


Figure 5.36: Linearity versus Frequency for all topologies - bandwidth extension techniques

6

Two-stages with Input Buffer

Most of the time, the presence of a high capacitive node dictates the circuit bandwidth. One way to deal with this large-time constant is using a two-stage structure. A two-stage topology can divide a low-frequency pole into two high-frequency poles. Nevertheless, the bandwidth improvement cannot be achieved without the increase of noise and area.

Moreover, a two-stage structure enables the use of thick gate devices and thin gate devices without the need for secondary ESD protection. In practice, the first stage is implemented with thick oxide devices, while the second stage with thin oxide devices. As mentioned previously, thin-ox devices improve the bandwidth due to their low intrinsic capacitance.

Earlier simulations demonstrate that the BSF achieves the maximum bandwidth in thick gate devices with and without bandwidth extension techniques, and because of that, the first stage is always a BSF.

6.1 Design Strategy

As demonstrated in previous designs, the optimum design is achieved when all circuit poles are at the same frequency. However, some frequencies are unreachable due to intrinsic limitations. Nonetheless, the following designs attempt to have a bandwidth higher than 18 GHz at an optimal point.

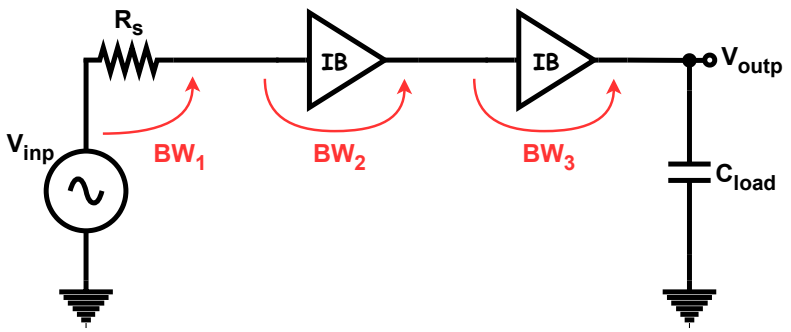


Figure 6.1: Two-stages optimum bandwidth

Therefore, for an optimum design, the bandwidth BW_1, BW_2, and BW_3 in Figure 6.1 must be equal.

6.2 Basic Source Follower and Basic Source Follower

The cascade source follower topology is depicted in Figure 6.2, where the first stage uses devices with L_{min} equal to 72 nm and the second stage with 8 nm.

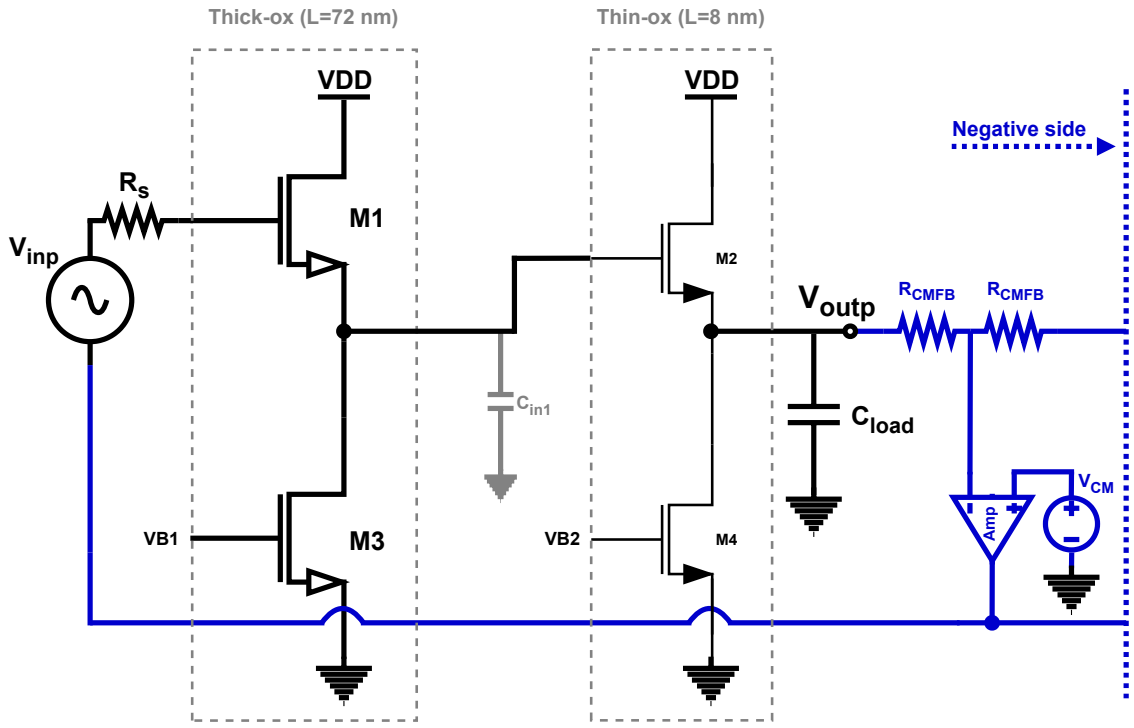
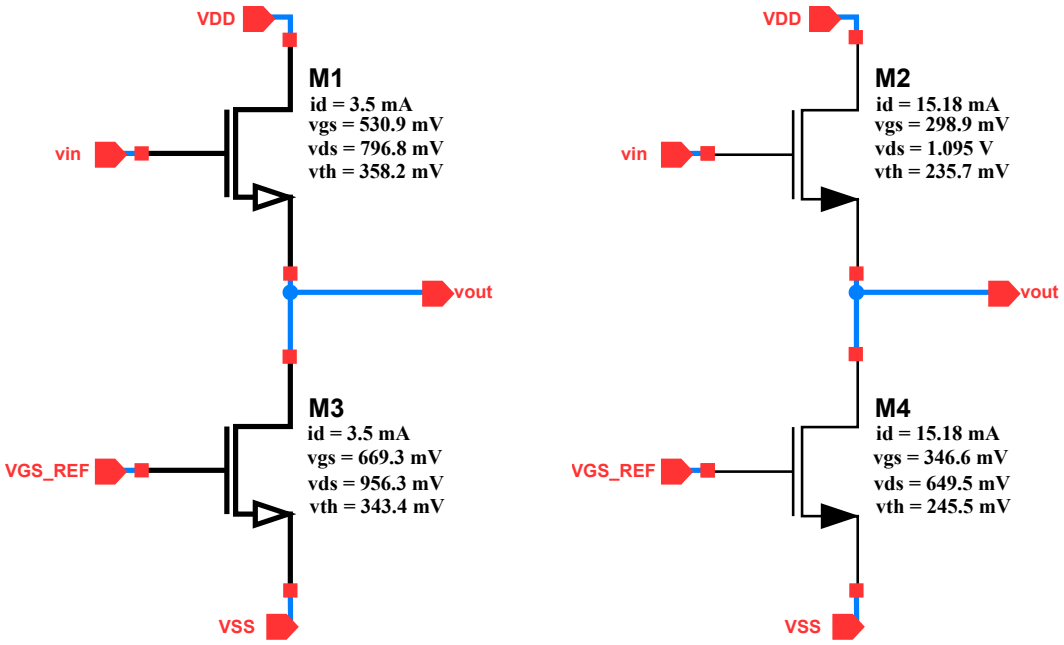


Figure 6.2: Basic Source Follower - Basic Source Follower

By inspection, it can be seen that the first stage drives the capacitance C_{in1} that is smaller than C_{load}, mainly because M2 is a thin oxide device, which means that the M1 multiplier can be smaller than M2. In theory, the pole between stages is approximately $\frac{g_{m1}}{C_{in1}}$ and the output pole is $\frac{g_{m2}}{C_{load}}$, where C_{in1} is a fictitious capacity representing the node capacity between stages. Therefore, g_{m2} has to be greater than g_{m1} to compensate for the large capacity C_{load}.

Using a current mirror for bias M1 and M2, and sizing M1, M2, M3, and M4 multipliers with 30, 70, 10, and 40, respectively, the DC operating point results are detailed in Figure 6.3.

The DC operating point reveals that the dissipated current for dual stage is much lower than for a single stage source follower (49 mA). Therefore, for an increase of approximately 7 GHz, the consumed DC current is reduced by 29.32 mA, which is a massive improvement.



(a) First stage operation point (b) Second stage operation point

Figure 6.3: BSF - BSF operating point

The Bode diagram is displayed in Figure 6.4, where the circuit bandwidth is 20.83 GHz without T-coil implementation. Thus, meeting the 18 GHz requirement.

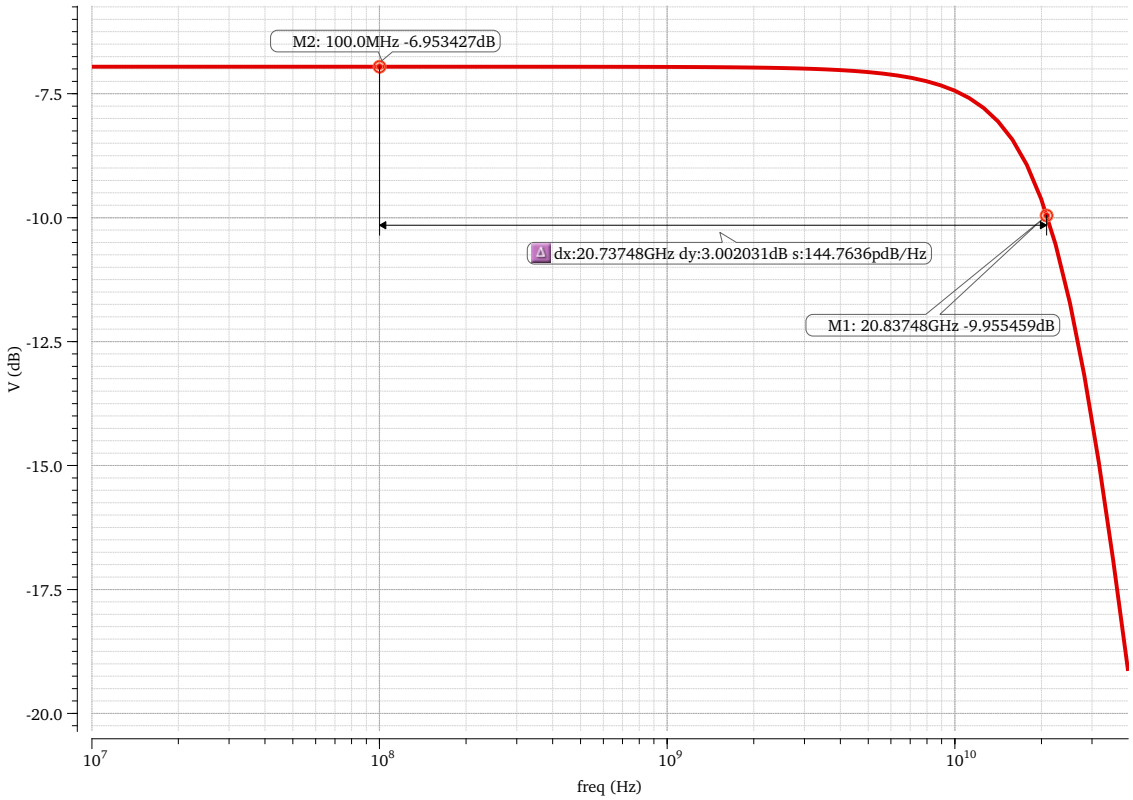


Figure 6.4: BSF - BSF frequency response

One drawback of the dual stage design is the linearity performance, as detailed in Figure 6.5. Implementing two BSFs in series increases the number of non-linear sources compared with only one BSF, which leads to low IIP3 values.

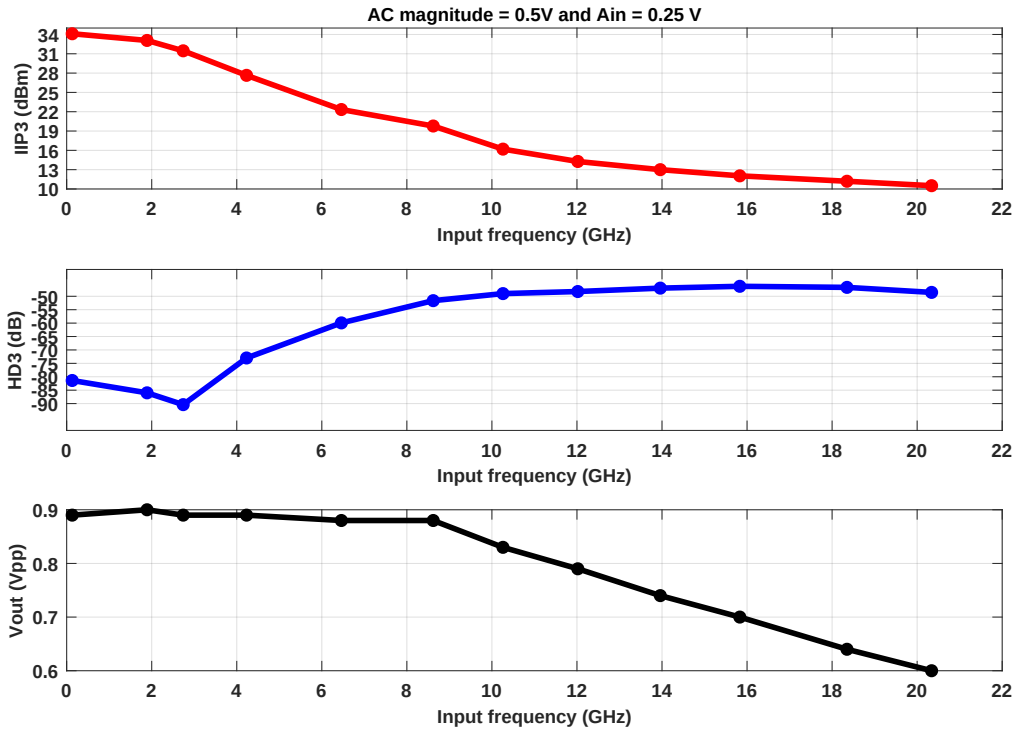


Figure 6.5: BSF - BSF linearity results

As detailed in Figure 6.5, the minimum in-band value of IIP3 is 10.51 dBm.

6.2.1 BSF and BSF with T-coil technique

Although the previous architecture reached 18 GHz without any bandwidth extension technique, the T-coil implementation minimizes the dissipated power by increasing the area. For instance, if inductors are used, the buffer intrinsic capacity is absorbed and the transistor transconductances are decreased, leading to higher frequency poles. However, decreasing g_m increases the noise and degrades linearity by making the transistor more frequency dependent, as studied in subsubsection 3.1.6.3.

In this particular case, the ADS optimizer had difficulty converging to a solution that improves the return loss with the T-coil and series peaking technique presented in section 5.1. Therefore, in this topology and only in this topology, the series peaking was not implemented, and the ESD protection was placed in another location, as shown in Figure 6.6.

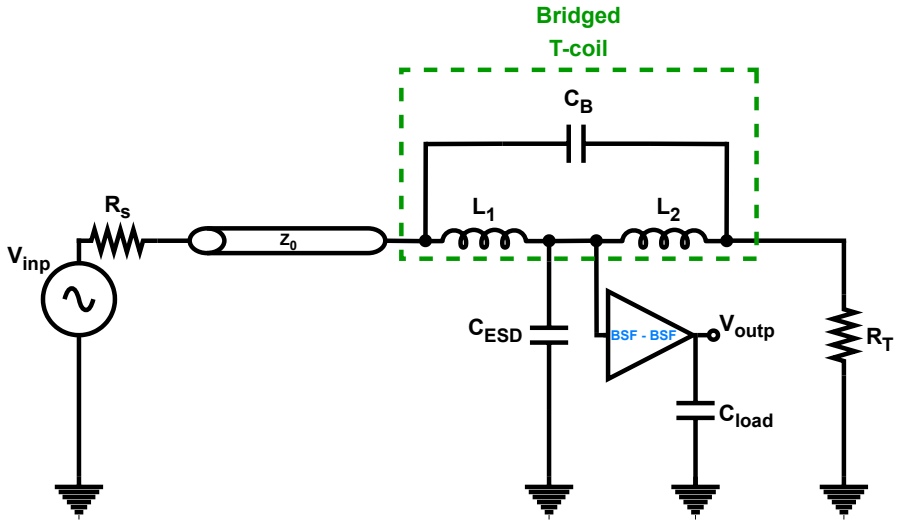


Figure 6.6: The bridged T-coil technique without series peaking

By sizing C_B, L_1, and L_2 equal 17.4 fF, 317.9, and 199.1 pH, respectively, and sizing M1, M2, M3, and M4 multipliers with 20, 40, 3, and 30, respectively. The resulting BW is 20.33 GHz, as detailed in Figure 6.7.

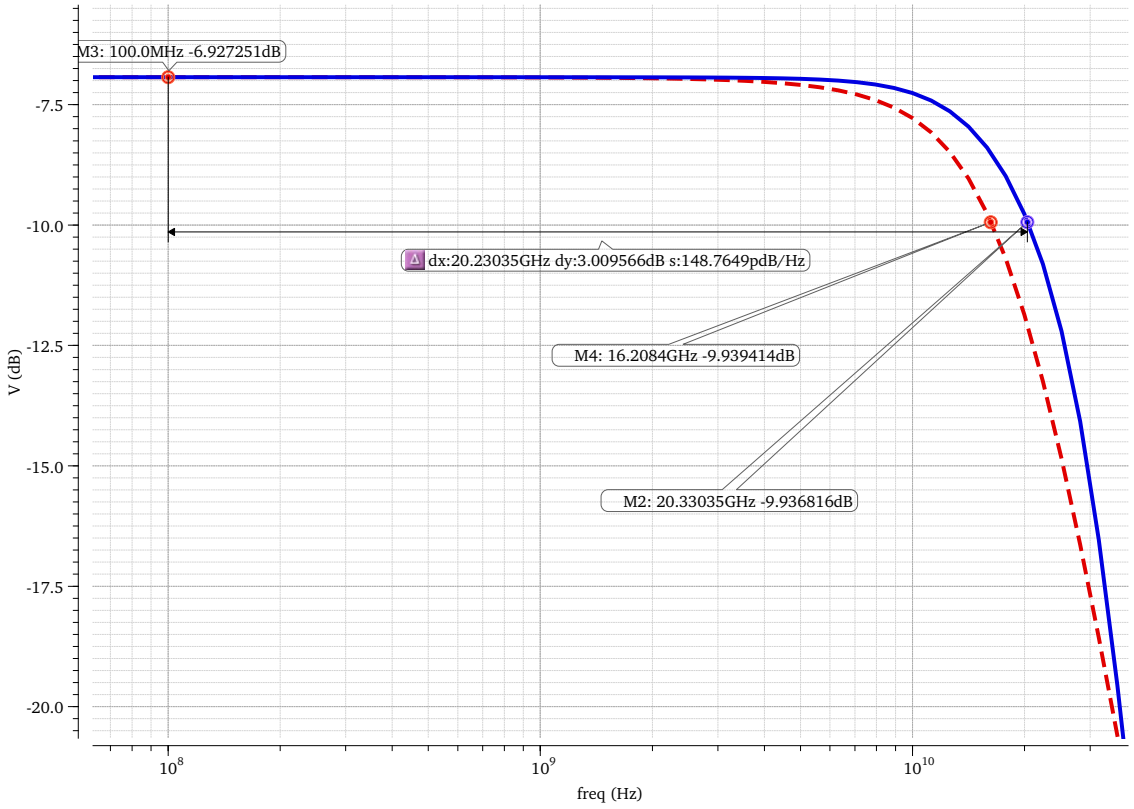


Figure 6.7: BSF - BSF frequency response with T-coil technique

The return loss is displayed in Figure 6.8, where $S_{11_{dd}}$ is lower than -10 dB up to 25.86 GHz.

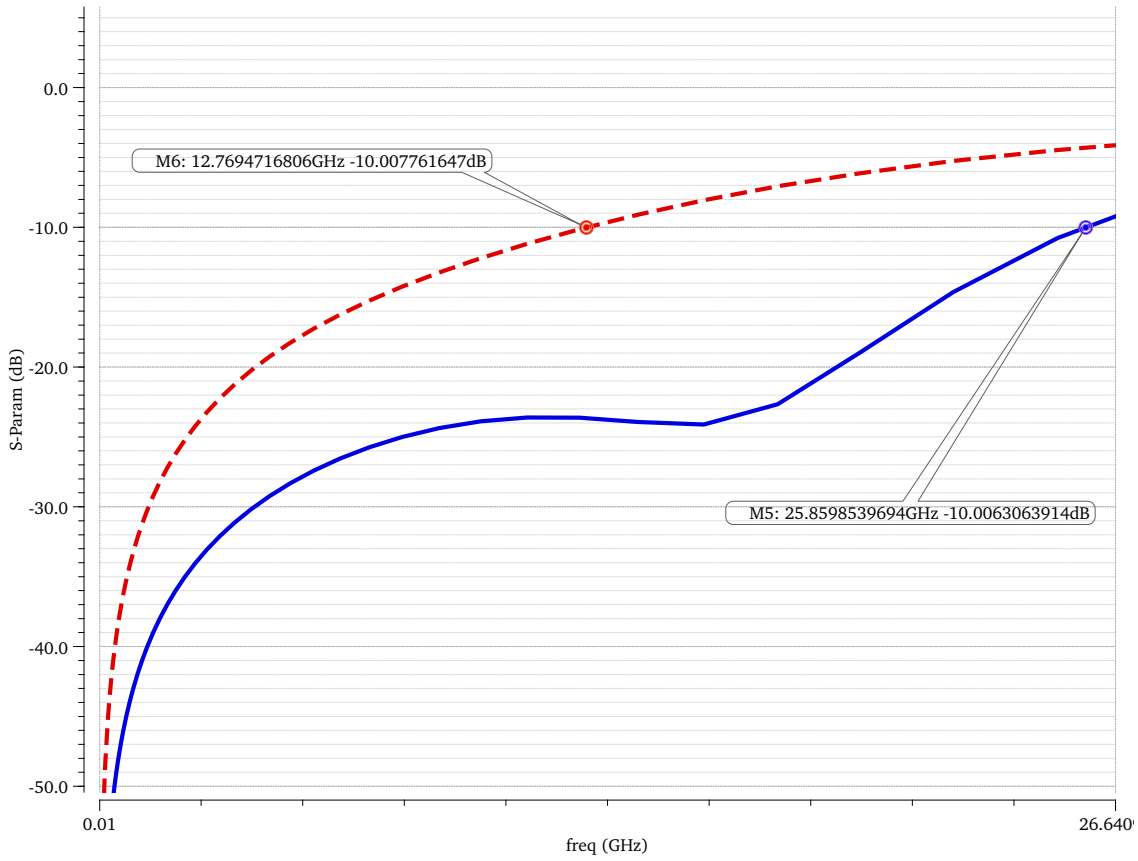


Figure 6.8: BSF - BSF input return loss with T-coil technique

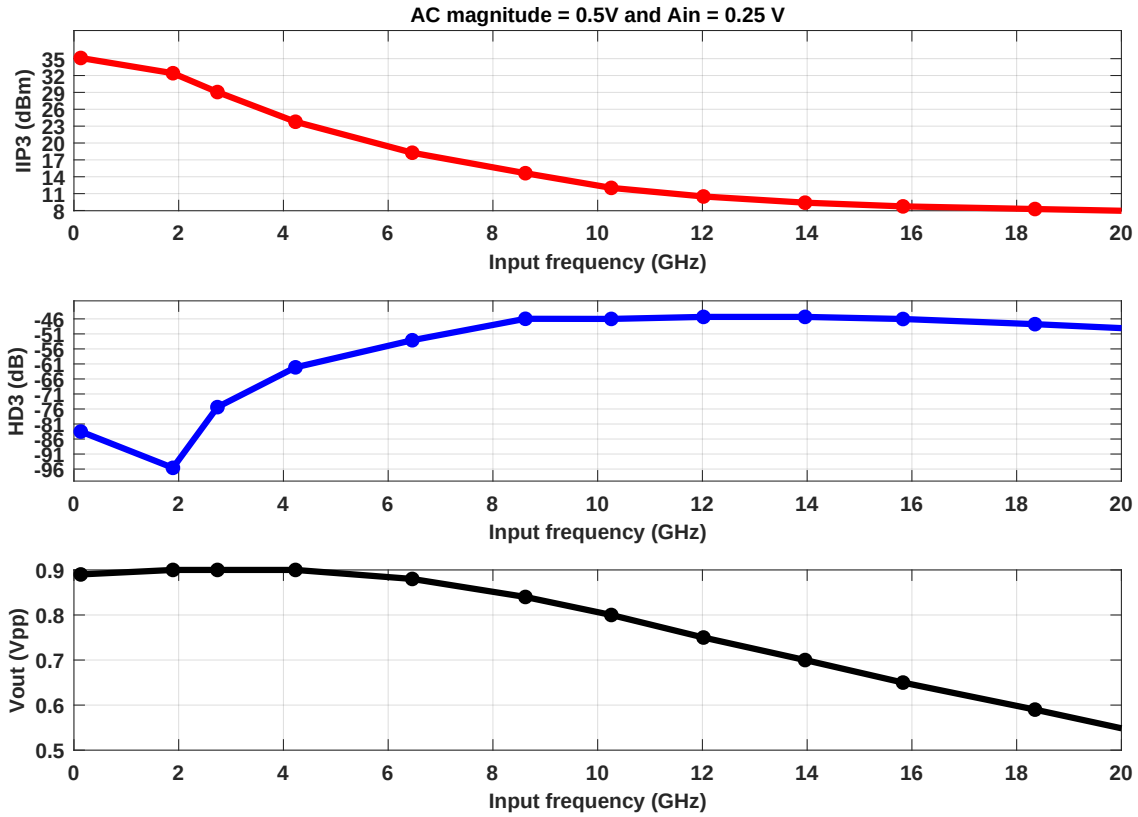


Figure 6.9: BSF - BSF linearity results with T-coil technique

As it usually happens, after the T-coil implementation, the linearity is reduced. In this case, $IIP3_{min}$ drops from 10.51 to 8.27 dBm (see Figure 6.9). On the other hand, the power consumption is reduced from 70.85 to 48.39 mW, 22 mW less.

6.3 Basic Source Follower and Basic push-pull

As discussed above, the Cascade Source Follower can easily have a 30 GHz bandwidth by dissipating power. Although, a two-stage topology degrades the linearity and increases the noise. One way to improve the linearity is to implement the second stage with a Basic push-pull, as shown in Figure 6.10.

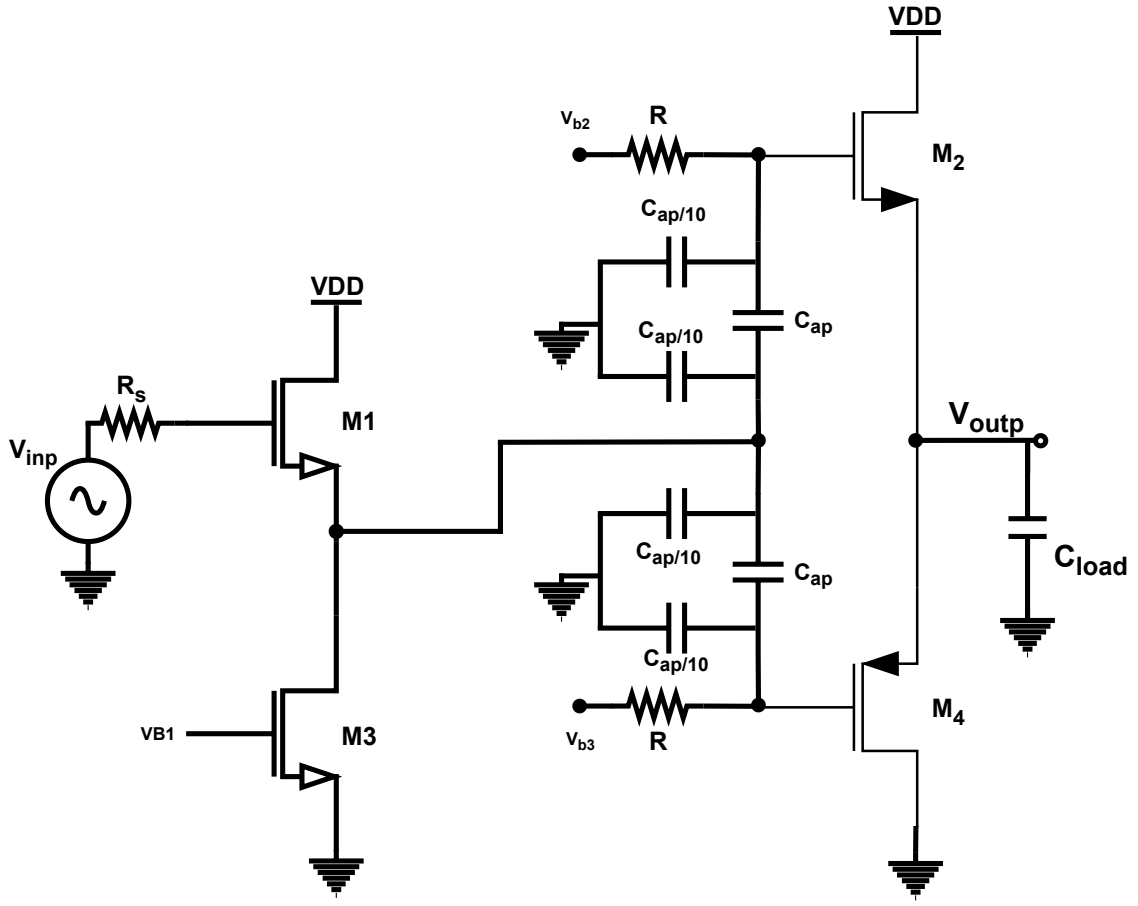
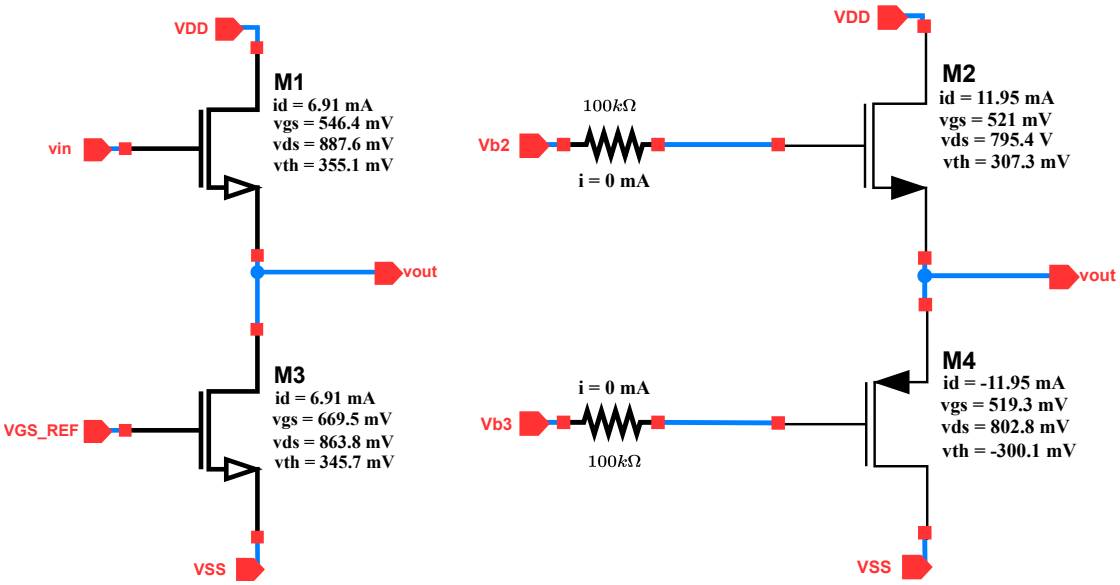


Figure 6.10: Basic Source Follower - Basic push-pull

The first stage is parameterized with M1 and M3 multiplier of 50 and 20, the second stage is with M1 and M2 of 11 with a C_{ap} of 0.8 pF. The DC behavior can be seen in Figure 6.11.



(a) First stage operation point (b) Second stage operation point

Figure 6.11: BSF - Basic push-pull operating point

The high input capacitance of the second stage lowers the bandwidth from 20.83 to 12.58 GHz. In addition, the input capacitance of the second stage creates a capacitive divider that attenuates the signal by about 1 dB more, as detailed in Figure 6.12.

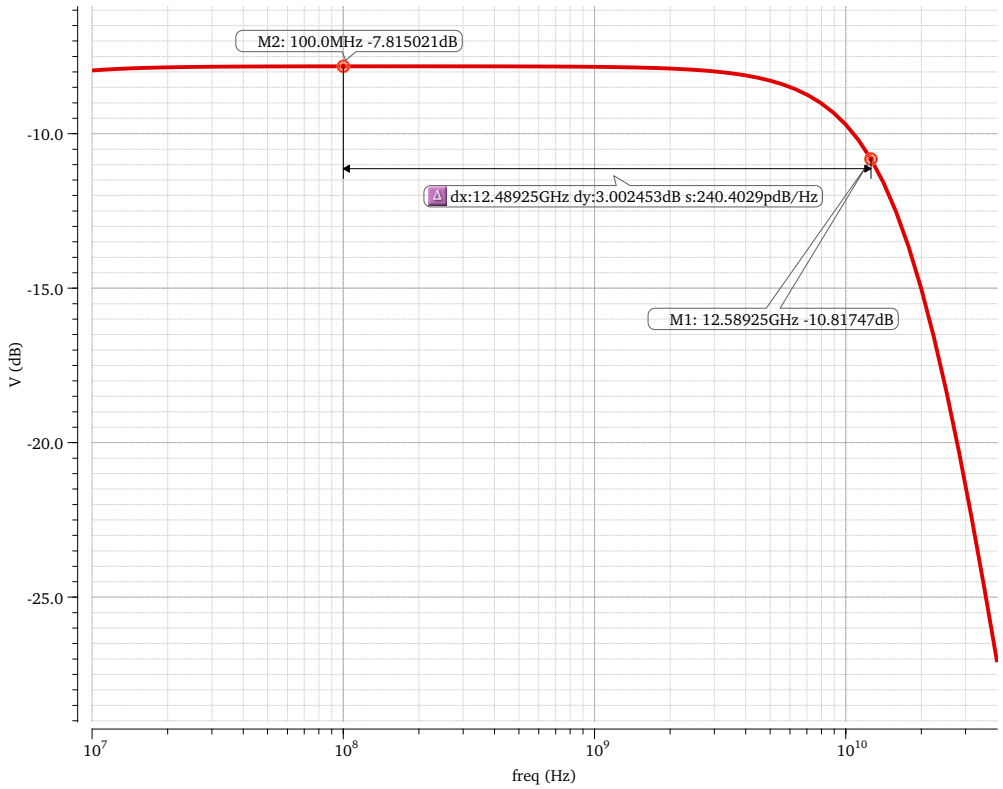


Figure 6.12: BSF - Basic push-pull frequency response

As expected, the linearity significantly improves by using a Basic push-pull, because the Basic push-pull is more linear than a simple source follower, as studied before.

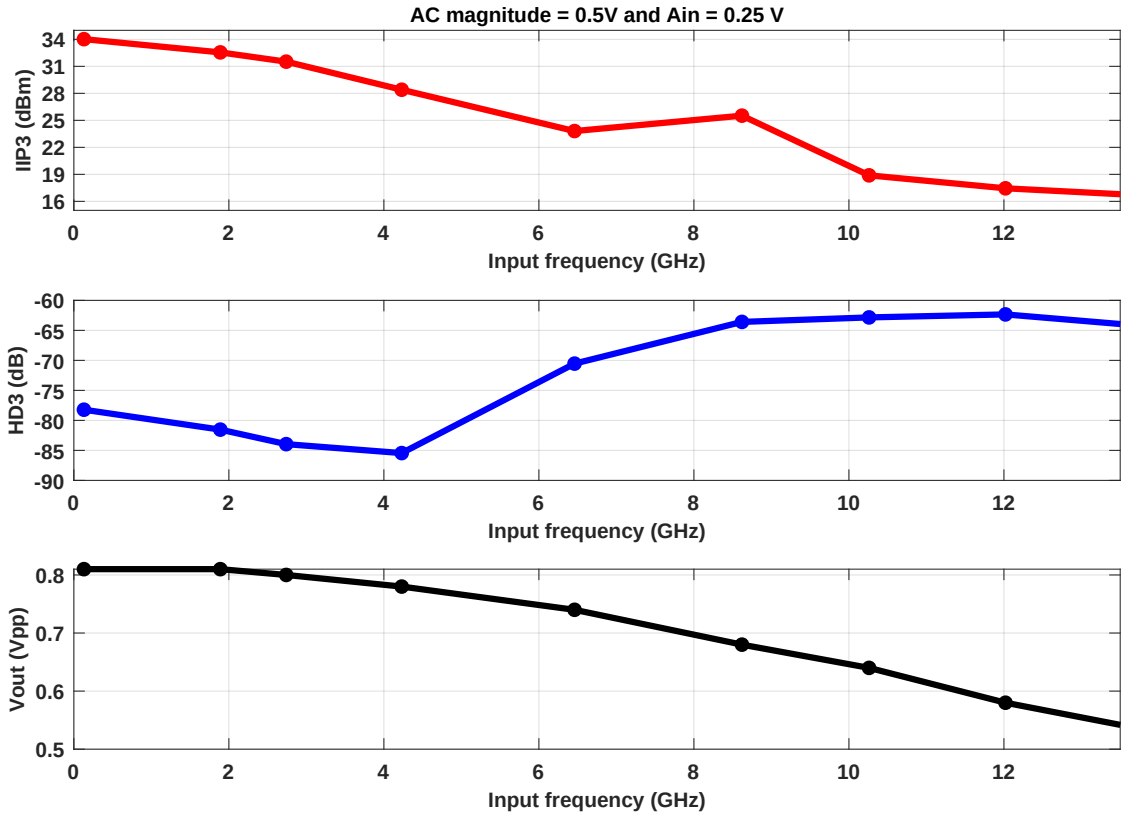


Figure 6.13: BSF - Basic push-pull linearity results

6.3.1 BSF and Basic push-pull with T-coil technique

The circuit bandwidth does not reach the bandwidth requirements. The most straightforward way to achieve 18GHz is to implement the T-coil technique. With the T-coil technique, the optimum design is no longer the same, and because of this, the transistors have to be resized.

By sizing C_B, L_1, L_2, and L_p equal to 71.26 fF, 41.93, 94.08, and 269.6 pH, respectively, and parameterising M1, M3, M2, and M4 multipliers with 55, 28, 13, and 13, respectively the resulting bandwidth is 19.77 GHz with a C_{ap} of 0.8 pF (see Figure 6.14).

Consequently, the input return loss is lower than -10 dB until the 32.44 GHz, as displayed in Figure 6.15.

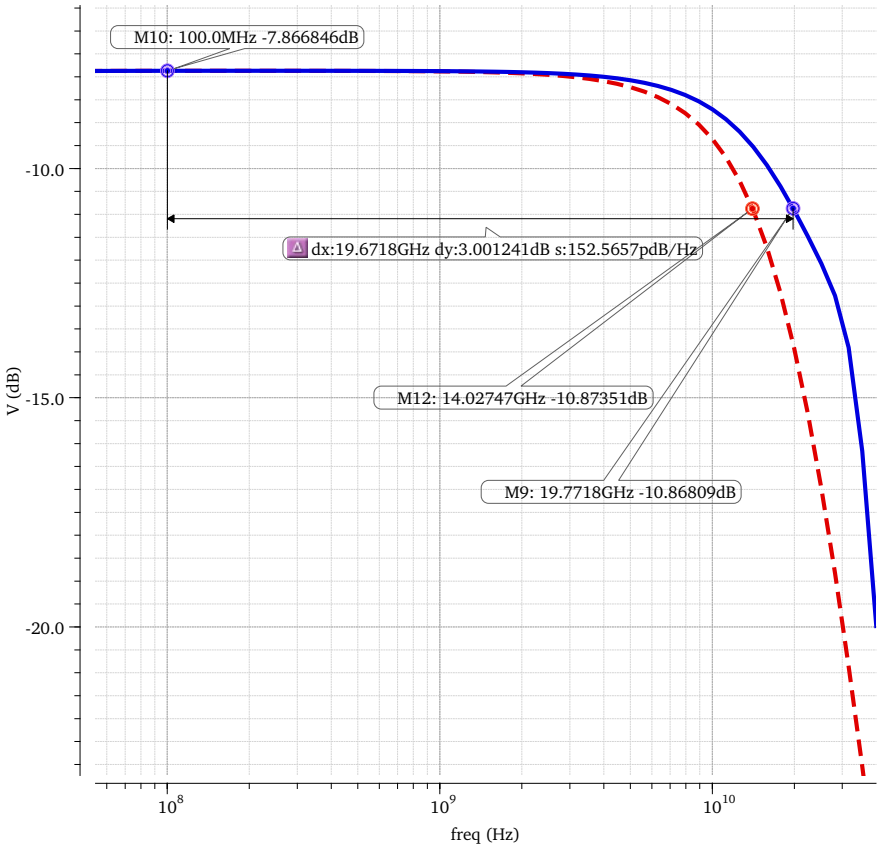


Figure 6.14: BSF - Basic push-pull frequency response with T-coil technique

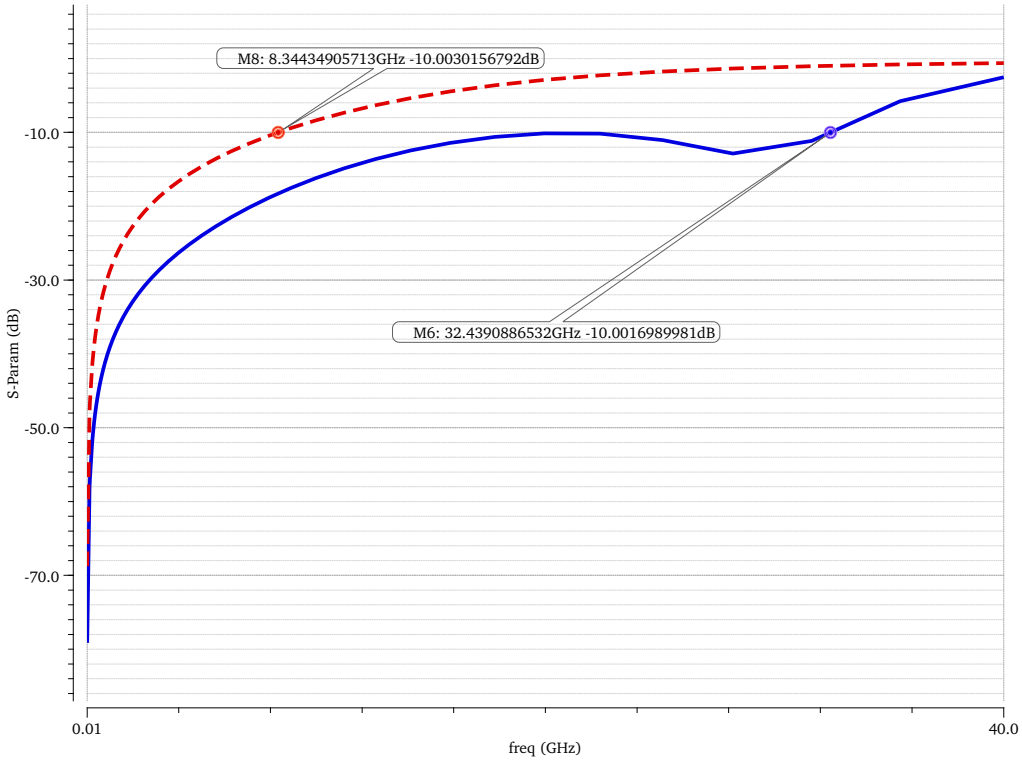


Figure 6.15: BSF - Basic push-pull input return loss with T-coil technique

Finally, the linearity results after the T-coil implementation are shown in Figure 6.16, where the IIP3 values have a slight reduction.

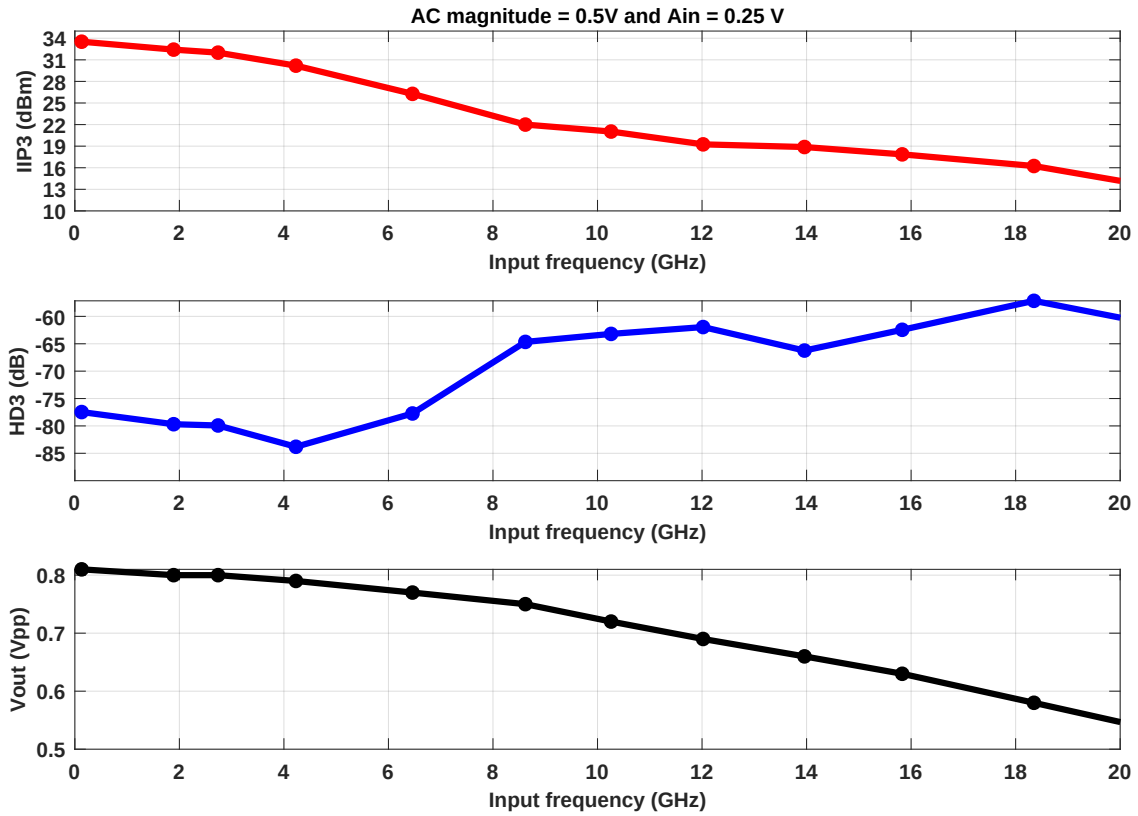


Figure 6.16: BSF - Basic push-pull linearity results with T-coil technique

Replacing the second stage BSF with a Basic push-pull improves the linearity from 10.51 to 16.30 dBm.

6.4 Basic Source Follower and Push-pull

The two-stages Basic Source Follower and Push-pull architecture is shown in Figure 6.17. The only difference between this design and the design in chapter 4 is the existence of two different $Caps$ in the second stage, $Cap1$ and $Cap2$.

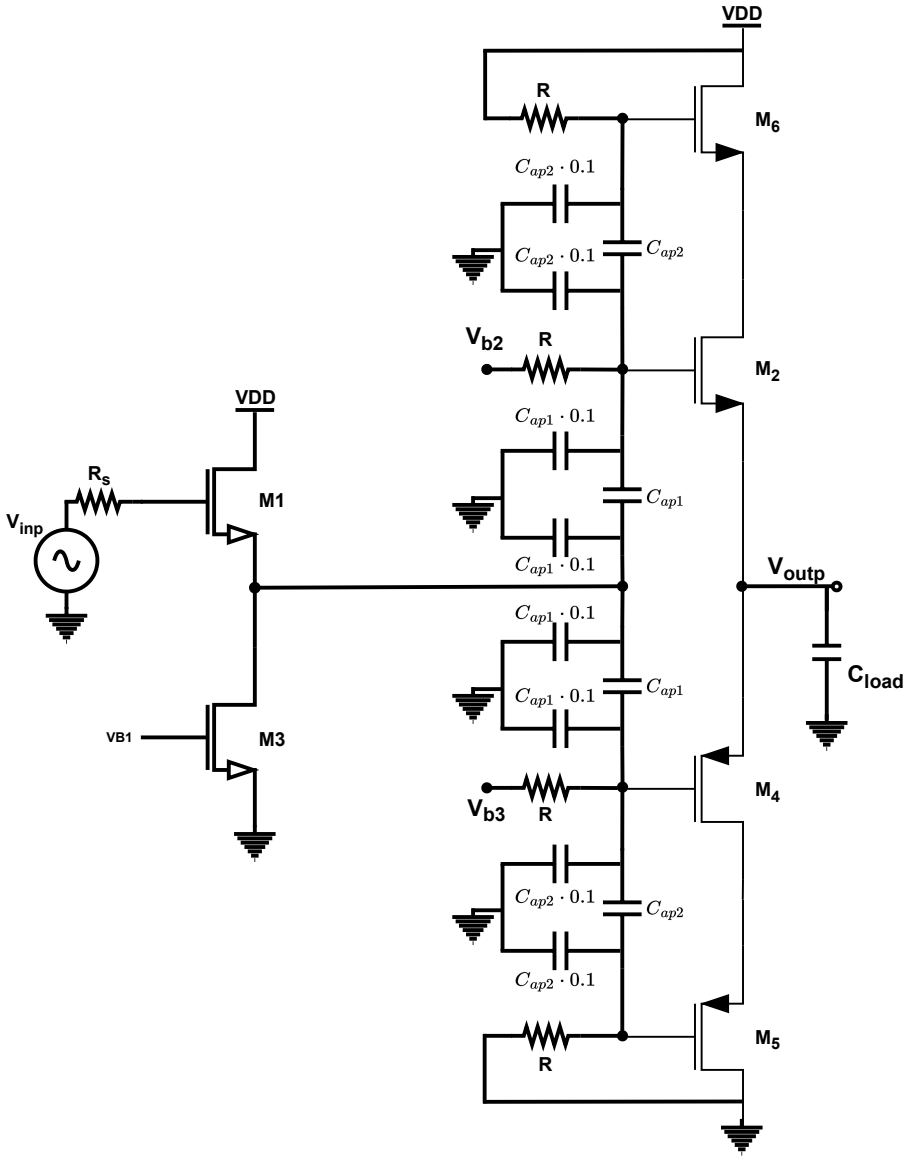
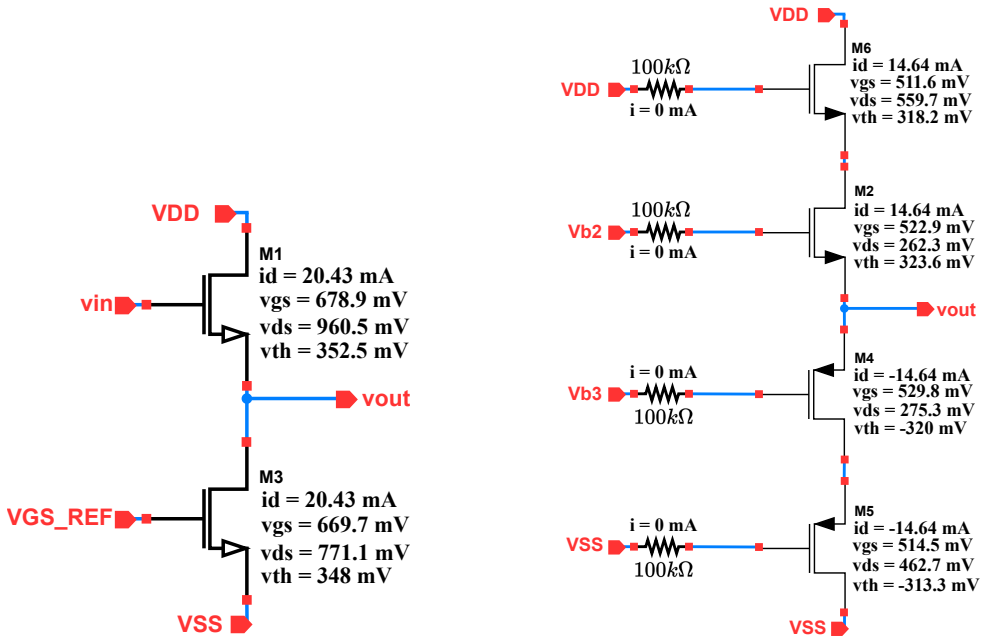


Figure 6.17: Basic Source Follower - Push-pull

The DC operating point is displayed in Figure 6.18, where the BSF is sized with M1 and M3 multipliers equal to 60, while the Push-pull is sized with M2, M4, M5, and M6 of 16. Furthermore, all transistors are in saturation, and the output common mode voltage is approximately 0.9 V.

Figure 6.18 details that for a optimum design, the first stage DC current has to be 40% higher than the second stage DC current, caused by the dominant pole located between the two-stages.



(a) First stage operation point (b) Second stage operation point

Figure 6.18: BSF - Push-pull operating point

The Bode diagram is exhibited in Figure 6.19, with C_{ap1} and C_{ap2} equal to 0.8 pF and 0.4 pF, respectively.

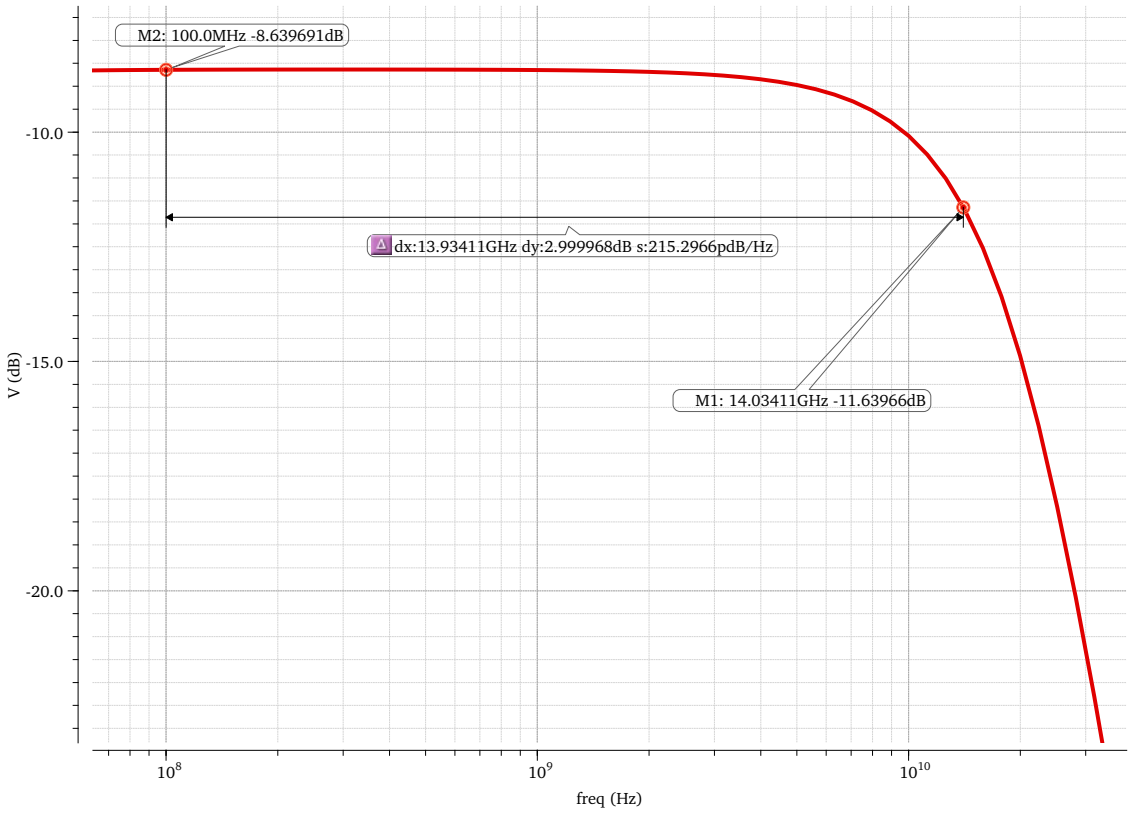


Figure 6.19: BSF - Push-pull frequency response

Figure 6.19 shows that the -3dB bandwidth is 14.03 GHz, lower than the 18 GHz requirement.

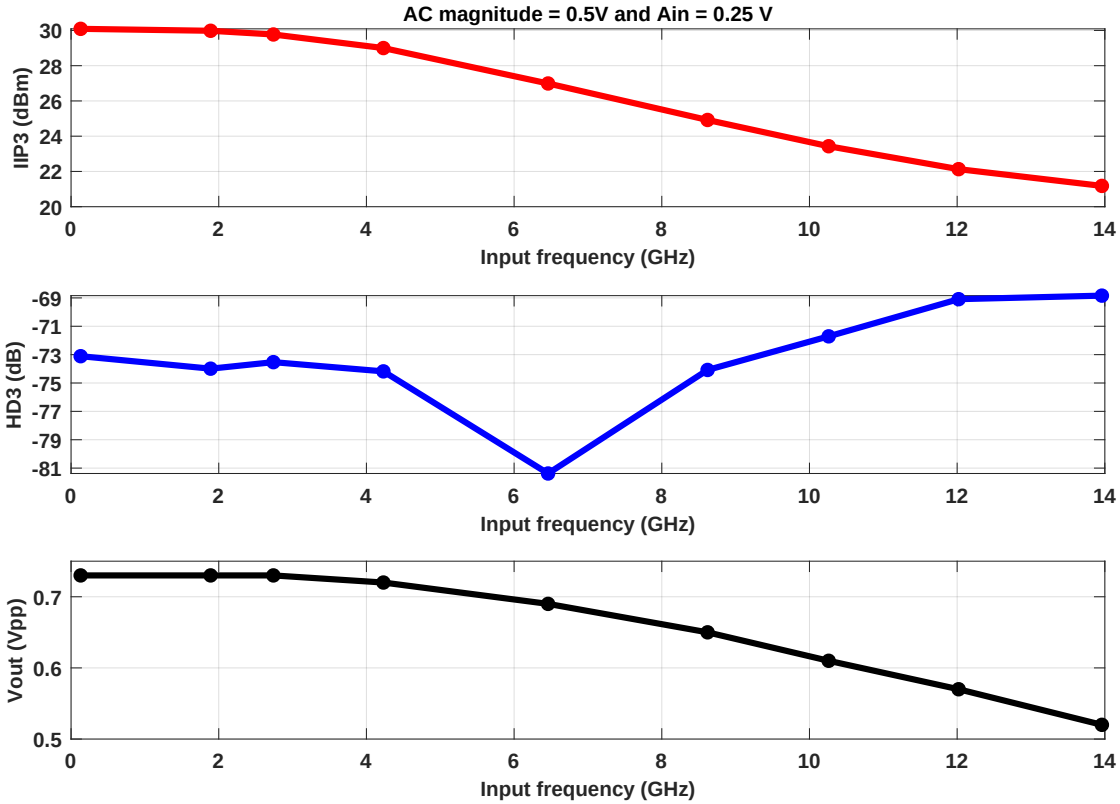


Figure 6.20: BSF - Basic push-pull linearity results

As discussed previously, due to the Push-pull high input capacitance, the differential output peak-to-peak voltage and the DC gain are lower than the other topologies (see Figure 6.20).

6.4.1 BSF and Push-pull with T-coil technique

In the previous section, an optimal bandwidth greater than 18 GHz was not achieved and to deal with this circuit limitation, the T-coil technique is implemented.

By sizing C_B, L_1, L_2, and L_p equal 107.7 fF, 156.3, 37.62, and 227.5 pH, respectively, the resulting bandwidth is 19.86 GHz, as shown in Figure 6.21.

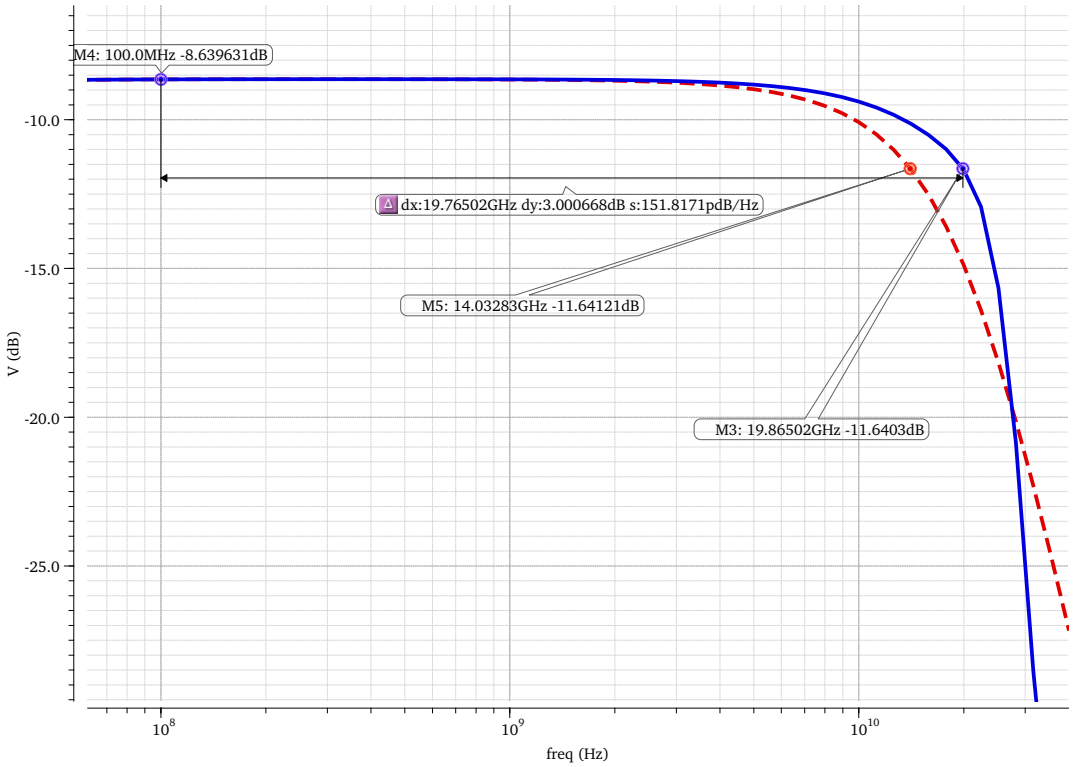


Figure 6.21: BSF - Push-pull frequency response with T-coil

Moreover, the input return loss is lower than -10 dB until the 23 GHz, as displayed in Figure 6.22.

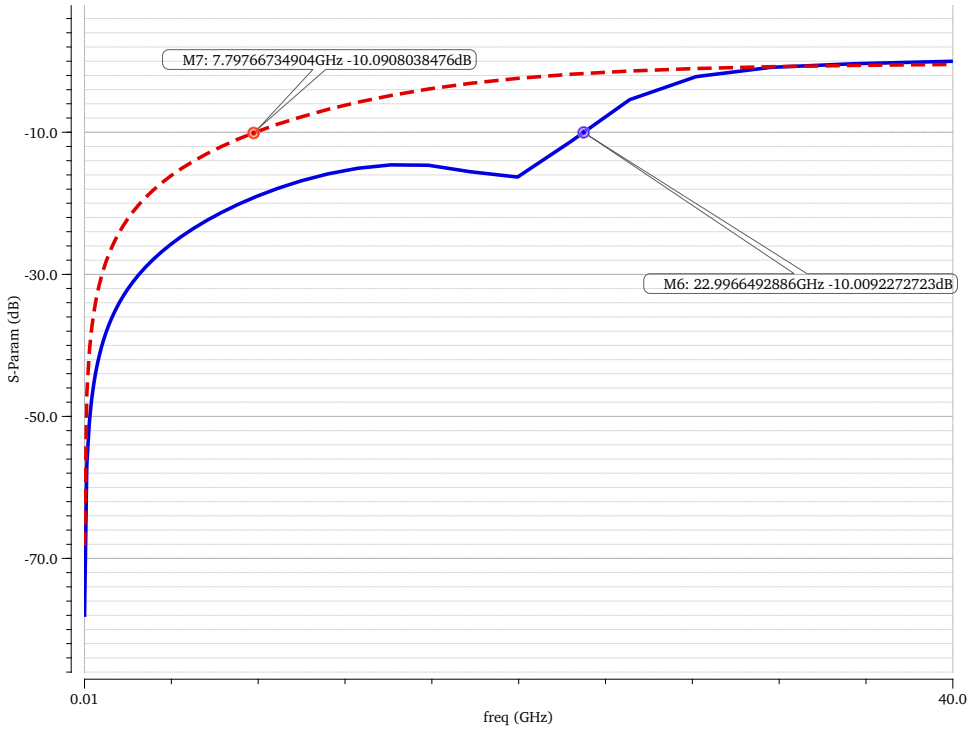


Figure 6.22: BSF - Push-pull input return loss with T-coil technique

The IIP3 results show slight linearity improvement compared to the two-stages BSF and Basic push-pull topology, where $IIP3_{min}$ is equal to 19.72, which is higher than the 16.30 dBm (Figure 6.23).

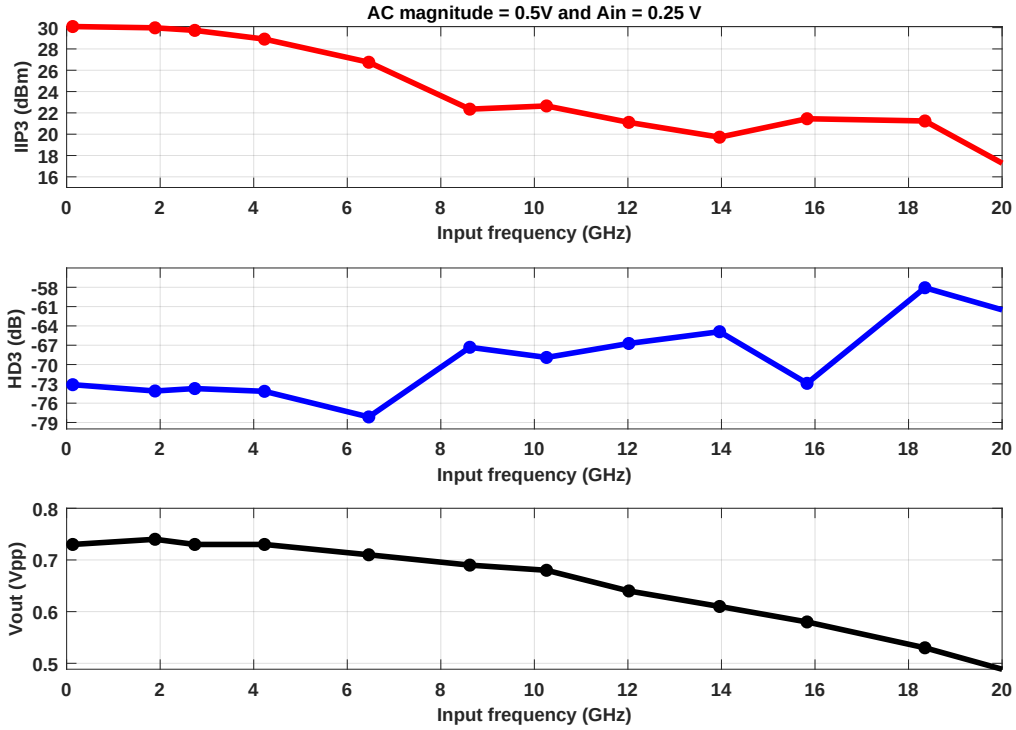


Figure 6.23: BSF - Push-pull linearity results with T-coil technique

6.5 Conclusion

With the two-stage typology simulations performed, all the results are summarised in Table 6.1. The simulations results demonstrate that a two-stage architecture with IBs can easily improve the bandwidth and the power consumption by degrading the linearity and increasing the noise.

Implementing the first stage with thick gate devices limits the overall bandwidth. Due to this, the topologies with the highest second-stage input capacitance require a bandwidth extension technique.

As detailed in Table 6.1, two-stage BSF achieves the 18 GHz with and without bandwidth extension techniques with the lowest DC power. However, reducing the drain current creates linearity and noise issues.

Table 6.1: Two-stages with input buffers simulation results

Topology	**BSF - BSF**	**BSF - Basic push-pull**	**BSF - Push-pull**
$\mathbf{V}_{OCM}$ (V)	0.7	0.9	
DC gain (dB)	-6.95	-7.82	-8.64
Bandwidth (GHz)	**20.83**	**12.58**	**14.03**
IIP3$_{min}$ (dBm)	**10.51**	**17.45**	**21.18**
Noise (μV_{rms})	286.8	227.2	197.9
DC power (mW)	70.85	71.50	129.85
		Bridge T-coil	
$\mathbf{C}_B$ (fF)	17.4	71.26	107.7
$\mathbf{L}_1$ (pF)	317.9	41.93	156.3
$\mathbf{L}_2$(pF)	199.1	94.08	37.62
$\mathbf{L}_p$ (pF)	-	269.6	227.5
Bandwidth (GHz)	**20.33**	**19.77**	**19.86**
$\mathbf{S}_{11_{dd}}$ = -10 dB (GHz)	**25.86**	**32.44**	**23.00**
IIP3$_{min}$ (dBm)	**8.27**	**16.30**	**19.72**
Noise (μV_{rms})	329.7	236.2	206.5
DC power (mW)	48.39	89.28	129.85

Furthermore, the linearity as a function of frequency is shown in Figure 6.24.

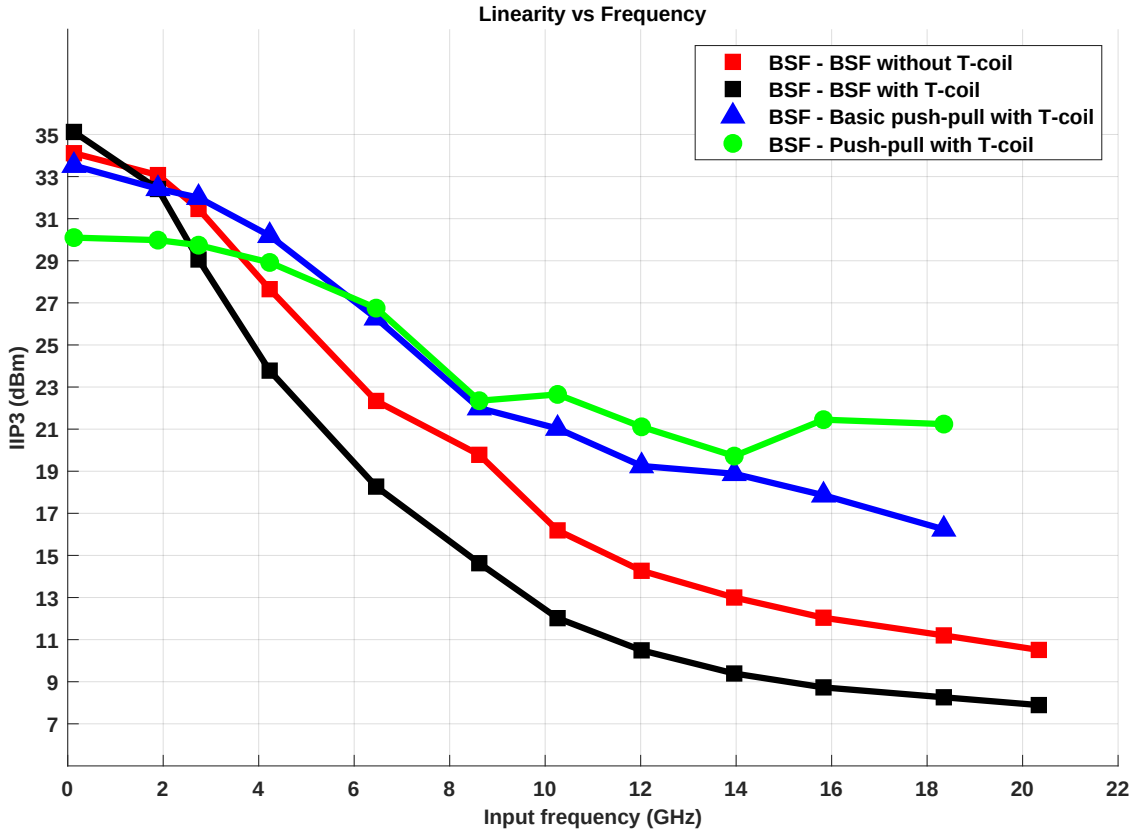


Figure 6.24: Linearity versus Frequency for two-stages IB topologies

From Figure 6.24, it can be argued that the two-stage BSF with T-coil has the best

linearity at lower frequencies (0-2 GHz) and the worst linearity at higher frequencies. As already discussed, comparing the two-stage BSF implemented with and without the T-coil technique, it can be concluded that the T-coil causes a slight linearity degradation.

Moreover, the BSF - Push-pull topology is the one with the highest linearity at higher frequencies, for instance, from 6 to 19 GHz. Interestingly, according to chapter 4, the Basic push-pull topology in thick gate devices is more linear than the Push-pull topology. However, in thin gate devices it is no longer true, which means that the bootstrap technique used by the Push-pull works in thin oxide transistors due to their low threshold voltage.

Lastly, the BSF - Push-pull architecture implemented with the bridge T-coil and the series peaking is closest topology to meeting the specifications with 19.86 GHz bandwidth, 206.5 μV_{rms}, and 19.72 dBm. As a result, it is the most "power-hungry" two-stage topology.

7

Conclusions and Future Directions

In this thesis, theoretical concepts, design trade-offs, and implementation of wideband, high-linearity input buffers in 7 nm FinFET process are discussed. Section 7.1 summarizes the dissertation and repeats the accomplishments achieved. Finally, section 7.2 proposes techniques to mitigate drawbacks related to input buffers, and indicates direction for future improvements by stating the recommendations.

7.1 The Thesis Outcome

The concise review of the different input buffer topologies has revealed that a low output resistance and a low input capacitance are required to decrease the power consumption and increase the bandwidth. Additionally, a high output swing and a linearization technique, for example, the V_{DS} "bootstrap" improves the linearity.

As demonstrated in chapter 4, the single-stage Basic push-pull and the Push-pull are the architectures that improve the linearity and consume the least power consumption because they have the lowest output resistance. However, these two topologies have a high input capacity that causes a reduction in gain and bandwidth. On the other hand, the single-stage Basic Source follower (BSF) is the fastest topology with a low input capacitance but the one with the highest power consumption and linearity degradation. As a result, none of the single-stage topologies with thick gate devices and one pico farad of sampling capacitance achieves 18 GHz of bandwidth.

With both bandwidth extension techniques - bridge T-coil with series peaking and the distributed approach - it is possible to reach the bandwidth requirements with the single-stage BSF, although, with a slight degradation of the linearity, noise and area. Moreover, comparing the two techniques, the bridge T-coil has better linearity and area but the distributed approach has a lower power dissipation.

The implementation of a two-stage architecture enables the use of thick oxide transistors and thin oxide transistors without the need for secondary ESD protection. Therefore, the bandwidth and the power dissipation are easily improved by degrading the linearity and increasing the noise. All the two-stage topologies achieve 18 GHz with a bandwidth

extension technique. The only topology able to reach 18 GHz without BW extension is the two-stage BSF. Consequently, the two series BSF has the best power consumption with the worst linearity and noise.

Interestingly, the "bootstrap" technique used throughout this thesis only improves the linearity when there is a minimization of the channel-length modulation without compromising the output swing. For this reason the Basic push-pull is the most linear topology in thick gate devices and the Push-pull topology in thin gate devices.

The measurement results (see Table 7.1) confirm that is possible to have 18 GHz in thick gate devices with the BSF topology by implementing a bandwidth extension technique. Moreover, using thick and thin gate devices together in a two-stage architecture improves the DC power consumption for almost the same $IIP3_{min}$ and noise.

Table 7.1: All results from the best topologies with more than 18 GHz

Topology	**BSF**	**BSF**	**BSF-Basic push-pull**	**BSF - Push-pull**
Bandwidth technique	T-coil	Distributed	T-coil	T-coil
Bandwidth (GHz)	25.78	24.26	19.77	19.86
IIP3$_{min}$ (dBm)	20.76	17.68	16.30	19.72
S11$_{dd}$ = -10 dB (GHz)	25.21	34.21	32.44	23.00
Noise (μV_{rms})	205.2	200.0	236.2	206.5
DC gain (dB)	-6.91	-6.92	-7.82	-8.64
DC power (mW)	178.20	119.02	89.28	129.85

It is worth mentioning that in this case, $IIP3_{min}$ is the minimum value of linearity up to 18 GHz and not over the entire bandwidth. The linearity results across frequency for the best topologies with more than 18 GHz are detailed in Figure 7.1.

Figure 7.1 reveals that the two-stage BSF and Basic push-pull topology implemented with the T-coil technique have the higher linearity until 6 GHz and the single-stage BSF with T-coil from 6 to 18 GHz. Moreover, the two-stage BSF and Push-pull is a good optimum for low and high frequencies.

To conclude, this work presents various new input buffers solutions for high-speed applications with high linearity, low power, and low noise without compromising reliability and robustness issues.

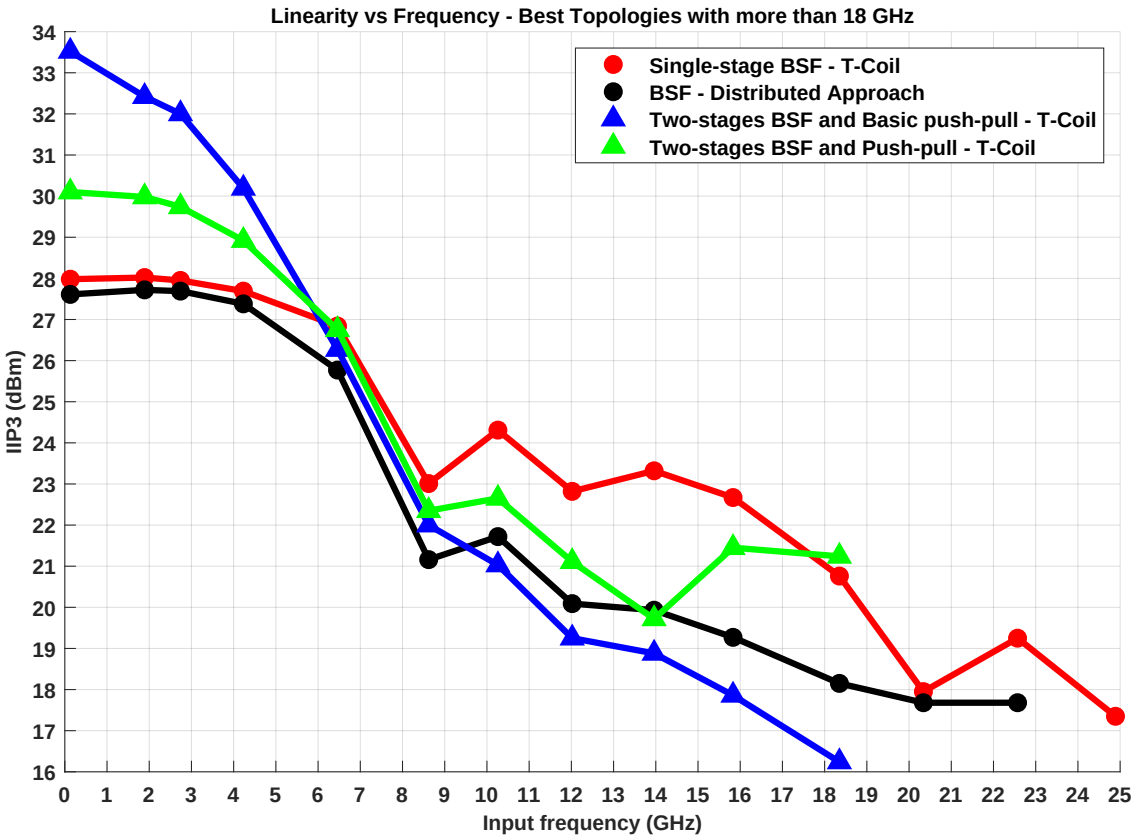


Figure 7.1: Linearity versus Frequency for best topologies with more than 18 GHz of bandwidth

7.2 Some Suggestions For Future Developments

Although, this work implements various input buffers that are able to operate up to 18 GHz of bandwidth with one pico farad of sampling capacitance, it requires further developments to arrive at an architecture that easily reaches 18 GHz without dramatically degrading power and linearity.

The following solutions are recommended in order to improve this work:

A two-stage topology with linearity techniques or/and one stage noise cancellation. Also, introducing bandwidth extension techniques between stages and a higher supply voltage could be beneficial.

Another prominent performance enhancement is the change of technology - going for smaller intrinsic capacitance and use of fully thin gate devices, for instance, a single-stage Push-pull. Another concept for investigation is the use of multiple ESD protections - determine whether two ESD protections with thin gate devices reach higher bandwidth than one ESD protection with thick gate devices.

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Design of an 18 GHz Wide-Band Input Buffer

***Abstract*—With the communication speed requirements growing more rapidly than the technology is advancing, new and enhanced ADCs have to be developed to ensure the required performance. Thereafter, this work investigates several different input buffers (IBs) for direct-conversion ADCs, implemented in a 7 nm FinFET technology. To achieve a thorough analysis of the concepts, the study begins with exploration of promising single-stage topologies in thick-gate devices. It was found that, single-stage design lacks in several performance aspects. Hence, bandwidth (BW) extension techniques as T-coil with series peaking and distributed approach are applied to ensure high enough BW to meet the requirements. Lastly, two-stage IB architectures with thick-oxide devices together with thin-oxide devices are designed to obtain full analysis of relevant study cases. The new solutions presented exhibit more than 18 GHz of BW with a linearity (IIP3) higher than 16.3 dBm, and a DC power dissipation lower than 178.2 mW without compromising reliability and robustness.**

***Index Terms*—ADC, Input Buffer, Direct-conversion, 7 nm FinFET, Wide-Band, High linearity, Power efficiency, Reliability.**

I. Introduction

Recent developments in wireless communication and systems, such as sixth-generation (6G), radar and instrumentation have led to massive use of high-frequency carriers. As a result, there is a high demand for ADCs in direct-conversion architectures with high BW, high-resolution, and with the highest possible power efficiency and spectral purity.

A voltage IB could potentially enhance the receiver's performance, with provisory benefits provided in Fig. 1. First of all, the sample-and-hold (S/H) circuit and the low noise amplifier (LNA) cannot be linked directly without significantly rising the power dissipation and degrading the driving of the ADC. Secondly, the high input and low output impedances isolate the input signal either from any load injection or any kickback noise coming through the sampling capacitance C_s. [1], [2]

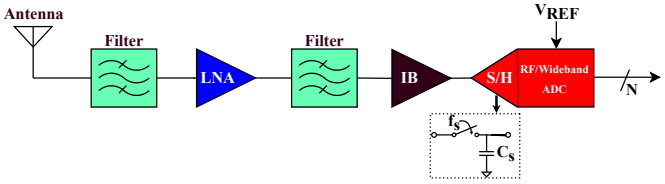


Fig. 1: Direct RF Receiver architecture.

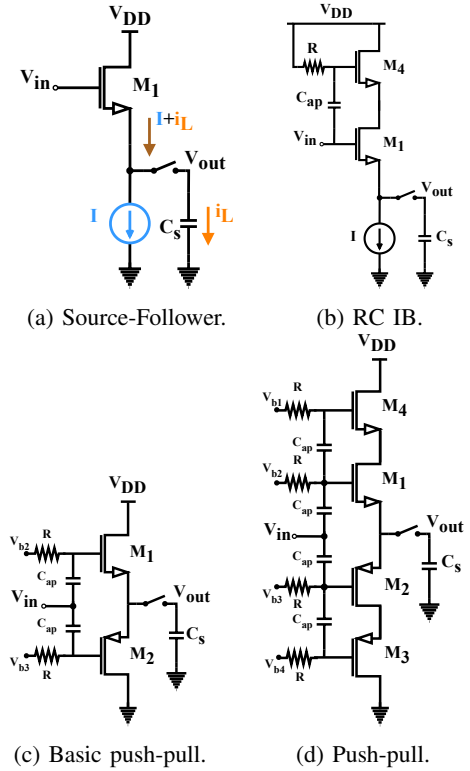
However, the IB limited bandwidth (BW) and the added distortion are potential drawbacks of using IB. To minimize the negatives and the sampling circuit distortion, low output impedance has to be realized at a cost of IB power dissipation being greater than combined power of other circuitry. [3]–[5]

In recent years, due to the high ADC resolution and quantization range, the existing approaches use IBs with supply voltages above the nominal rails, for instance, 2.5 or 4.0 V, to increase the linearity and to not limit the ADC output swing. However, it inherently creates reliability and robustness issues.

Therefore, the aim of this work is to obtain an IB which reaches 18 GHz bandwidth, while driving a total effective load of 1 pF, consisting of both sampling capacitance and routing parasitics in similar parts. Finally, to ensure ESD robustness of the ADC input, the 7 nm thick-oxide devices with 1.8 V supply voltage are used. To aid the reader in comprehending the concepts, the paper is structured in the following way. Section II starts by exploring four single-stage topologies in thick-gate devices with and without linearity techniques. Two bandwidth extension techniques are introduced in Section III. In Section IV mixed two-stage IB architectures are designed and simulated. Lastly, Section V presents the conclusions.

II. State of the Art

The easiest topology for implementation as IB is the source follower (SF). The upsides to using SF are the high input and the low output impedances [6], [7] while the drawbacks are the channel-length modulation effect and the output current variation (I+i_L), as shown in Fig. 2a.



(a) Source-Follower. (b) RC IB.

(c) Basic push-pull. (d) Push-pull.

Fig. 2: Single-stage topologies.

A. Circuit Techniques and Trade-offs

To alleviate the channel current frequency dependency the load impedance and/or the transconductance can be increased. Linearity can be improved by implementing a replica capacitance assisted buffer [8], [9], which provides only marginal increase in the bias current. This approach leads to isolation degrading due to reduced input impedance and an introduction of low-frequency input pole while fixing replica capacitance to value C_s. Another way to improve the SF's linearity is to apply the drain-bootstrap technique (see Fig. 2b and 2d), which reduces the channel-length modulation effect.

To properly analyze this technique, the RC assisted buffer was simulated. Capacitance values of 0.2, 0.9, 5 pF in constant DC operating point conditions. To obtain more realistic results two 10x. parasitic flying capacitances were attached to the main capacitor (Cap).

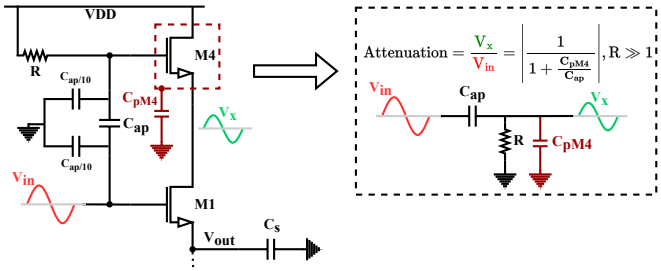


Fig. 3: Trade-off linearity versus bandwidth.

There is clearly a trade-off between the linearity and BW for the bootstrapping method. That is, if V_{DS1} is kept almost constant $V_x \approx V_{in}$, implying that Cap value has to be large, leading to low bandwidth as $|\frac{1}{1+\frac{C_{pM4}}{C_{ap}}}| = 1$ (see Fig. 3).

In addition, linearity is related to attenuation and this can be demonstrated by plotting the M1 drain-source potential variation over the frequency, as shown in Fig. 4.

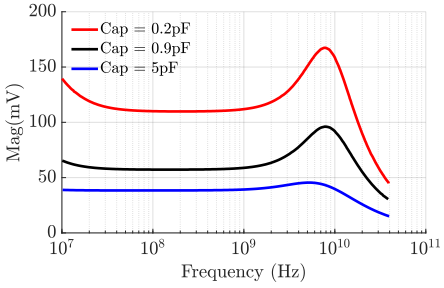


Fig. 4: V_{DS1} variation with frequency-Cap of 0.2, 0.9 and 5pF.

The SF output resistance can be reduced by expanding the SF with complementary devices [10], thus increasing the linearity (see Fig. 2c). However, it creates a new trade-off between gain and BW. Lastly, the push-pull follower (Fig. 2d) is a combination of the three aforementioned. Therefore, the push-pull has the two trade-offs which are inherited from the other topologies.

Interestingly, it was assumed that using the bootstrap technique would increase the linearity of the push-pull, which turned out to be inaccurate. The reason for the false identification of the benefit is caused by the assumption that V_{DS} decreased variation outweighs the output swing reduction term in the linearity evaluation.

B. Simulations

The four topologies have been designed and simulated with thick devices (L_{min} = 72 nm) in a pseudodifferential operation with 50 Ω resistance, 4 fins, 10 fingers, a standard ESD protection, and a two-tone spacing of 19.53 MHz, the results are compared in Table. I.

TABLE I: Results - single-stage topologies.

Topology (72 nm)	**SF**	**RC assisted buffer**		**Basic push-pull**	**Push-pull**
Cap (pF)	-	0.2	5.0	2.4	
BW (GHz)	13.9	9.9	4.7	4.7	3.0
IIP3$_{min}$ (dBm)	25.1	17.6	28.4	30.0	26.3
Power (mW)	178.2	81.0		17.2	9.8
DC gain (dB)	-6.9	-6.6	-6.5	-7.4	-8.6
Noise (μV_{rms})	172.3	151.5	123.1	99.3	82.3

It can be argued that the SF with a low input capacitance is the fastest architecture (13.9 GHz). On the other hand, it has the highest power consumption and the worst linearity but with IIP3 more or less constant over the frequency. The linearity and 3dB bandwidth for each topology are plotted in Fig. 5, where curves represent the IIP3 variation with the frequency.

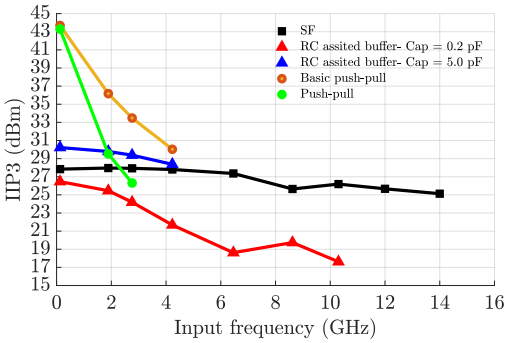


Fig. 5: Linearity versus frequency - single-stage.

Fig. 5 shows that the best architectures in terms of linearity are the basic push-pull (yellow line) and the push-pull (green line). As can be seen in Fig. 5, due to a lack of headroom in the 1.8V supply, we did not obtain any improvement in static linearity by adding drain bootstrapping to the basic push-pull.

The red and blue curves in Fig. 5, representing Cap values of 0.2 and 5 pF in RC IB, show that a linearity increase from 17 to 28 dBm requires a bandwidth reduction of 10 to 5 GHz.

Finally, it can be concluded that none of the single-stage topologies achieves more than 14 GHz of BW. This is due to large size required for the thick-gate devices to drive the 1 pF load.

III. Bandwidth Extension Techniques

Since none of the single-stage topologies reach the 18 GHz required BW, the use of inductance to cancel out some

of the capacitance is required, at the cost of considerable chip area [11], [12]. We investigated a bridged T-coil with series peaking, and a distributed SF approach. In addition to improving the BW, these techniques have been also optimized to improve the return loss.

A. The Bridged T-coil with Series Peaking

The main culprits for reducing the BW of an IB are the ESD protection and the buffer's input capacitance. Fig. 6 presents a possible countermeasure for the aforementioned capacitance in the form of single-ended input port in which a T-coil is driven by a transmission line with a characteristic impedance of 50 Ω that delivers the signal to the IB and to the termination resistor R_T.

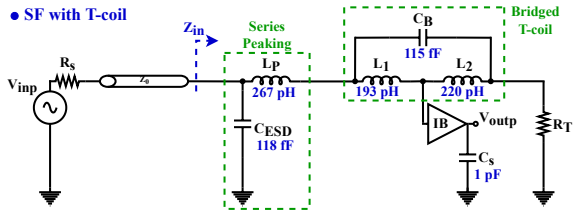


Fig. 6: The use of series peaking and bridged T-coil.

The bridge T-coil consists of two mutually coupled inductors (L_1 and L_2) and a bridge capacitor C_B. These noiseless coils can absorb the buffer capacitance and create a constant, resistive impedance across a wide frequency range. [11] Ideally, to suppress any input reflection Z_{in} must be equal to $R_S = 50\ \Omega$, meaning that $S_{11_{dd}}$ is equal to zero. The simulated results can be found in Fig. 7.

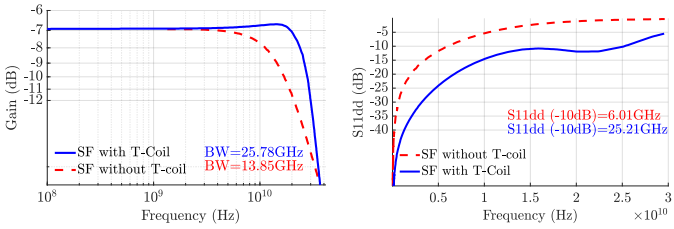


Fig. 7: SF: (a) Bode diagram; (b) Input return loss.

Fig. 7a shows the initial Bode diagram (red dashed curve) without the bridge T-coil, and the Bode diagram after the bridge T-coil implementation (blue curve). It can be concluded that the T-coil approach increases the initial bandwidth from 13.85 to 25.78 GHz, which means that the T-coil extends the original BW by a factor of 1.86.

In terms of input return loss, the results are displayed in Fig. 7b, and it is possible to see that $S_{11_{dd}}$ is lower than -10 dB up to 25.21 GHz whereas in the original bandwidth (red dashed line) it was only lower than -10 dB up to 6.01 GHz.

B. Distributed Approach

The idea behind distributed approach is to increase the BW and improve the return loss by using the buffer's parasitic capacitance as an element to build the transmission line equivalent schematic.

A transmission line can be represented as an infinite series of π or T segments with capacitance and inductance per length given in Fig. 8, where Z_0 is the real part.

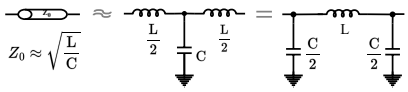


Fig. 8: Transmission line equivalent schematic.

The topology used for the distributed approach in this paper is presented in Fig. 9. Contrary to the bridged T-coil implementation, the IB itself is also split into two halves to further distribute its capacitance. The outputs of the two IB segments are combined through an output inductor L_{out}, which is optimized to maximize bandwidth. This approach is inspired by the well-known distributed amplifier topology. It should be noted that, because of the low output impedance of the IB, scaling this approach beyond two segments of IB is not expected to provide further improvements.

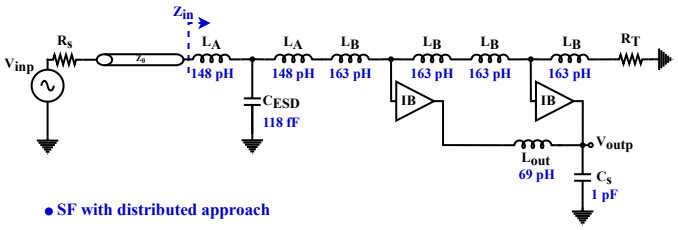


Fig. 9: Distributed approach for BW extension.

The achieved bandwidth and input-match for the SF are shown in Fig. 10, where the BW is 24.26 GHz and the return loss across frequency is acceptable until 34.31 GHz.

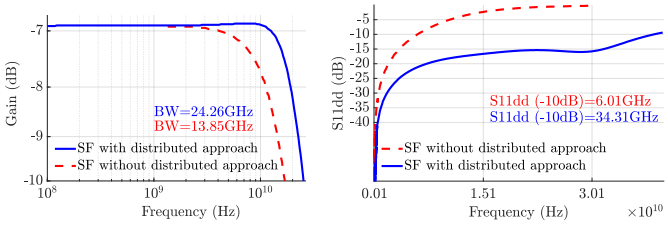


Fig. 10: SF: (a) Bode diagram; (b) Input return loss.

C. Results - Bandwidth Extension Techniques

Both, the bridge T-coil and the distributed approach degrade the area, noise, and linearity compared with the results obtained in subsection II-B. However, there is a considerable BW extension when a low input capacitance is driven by both techniques, for instance the SF (see Table. II).

As detailed in the simulation results, the bridge T-coil has better linearity and area, while the distributed approach has a low power dissipation for the same BW. The linearity and BW simulation results for all topologies are shown in Fig. 11.

TABLE II: Results - BW extension techniques.

Topology (72 nm)	SF	RC Buffer	Basic Push-pull	Push-pull
Bridge T-coil - Series Peaking				
DC gain (dB)	-6.9	-6.5	-7.4	-8.6
Bandwidth (GHz)	**25.8**	**7.1**	**7.7**	**4.9**
$S_{11_{dd}}$ = -10 dB (GHz)	**25.2**	**7.8**	**7.8**	**26.7**
IIP3$_{min}$ (dBm)	17.35	23.2	27.7	21.3
Noise (μV_{rms})	205.2	133.9	105.2	85.3
Power (mW)	178.2	81.0	17.2	9.8
Distributed Approach				
DC gain (dB)	-6.9	-6.9	-7.8	-8.6
Bandwidth (GHz)	**24.3**	**13.4**	**11.1**	**5.1**
$S_{11_{dd}}$ = -10 dB (GHz)	**34.3**	**14.2**	**9.5**	**8.8**
IIP3$_{min}$ (dBm)	17.7	7.7	20.5	18.3
Noise (μV_{rms})	200.0	151.7	122.1	90.7
Power (mW)	119.0	35.4	32.7	6.6

where dashed-lines represent the distributed approach technique, and the continues-lines represent the T-Coil technique. Once more, the curves terminate at a frequency equal to the effective BW.

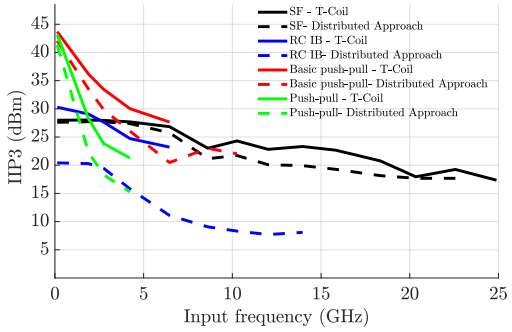


Fig. 11: IIP3 versus f - bandwidth extension techniques.

IV. Two-stage Cascaded Input Buffer

Most of the time, the presence of a high capacitive node dictates the circuit BW. One way to deal with this large-time constant is using a two-stage structure. A two-stage topology can divide a low-frequency pole into two high-frequency poles. Nevertheless, the BW improvement cannot be achieved without degrading noise, area and linearity.

A two-stage structure enables the use of thick-gate and thin-gate devices, without the need for secondary ESD protection. In practice, the first-stage is still implemented with thick-oxide devices, while the second-stage uses thin-oxide devices (L_{min} = 8 nm). The topologies assessed here are shown in Fig. 12. Here, we have combined a thick-oxide SF, followed either by a thin-oxide basic push-pull buffer or by a push-pull version with drain bootstrapping.

In a two-stage topology the capacitance between the stages can be sized to less than C_s as the main building-block of the second-stage are thin-oxide devices. As a result, the M_{11} multiplier can be smaller, thus increasing the input pole frequency and decreasing the power consumption. The simulation results across frequency for the two-stage topologies and for

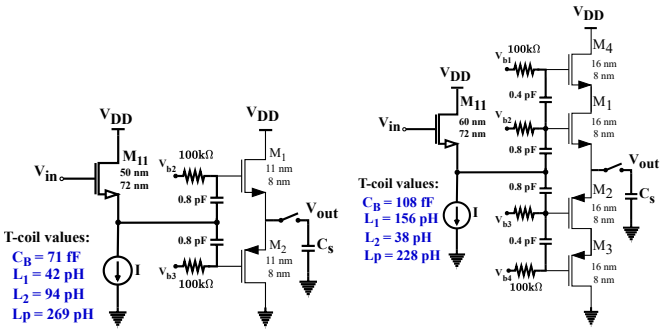


Fig. 12: (a) SF - Basic push-pull; (b) SF - Push-pull.

the single-stage topologies with >18 GHz are summarized in Table III and Fig. 13.

TABLE III: Results - topologies with more than 18 GHz.

Topology	SF	SF	SF - Basic push-pull	SF - push-pull
Bandwidth technique	T-coil	Distributed	T-coil	T-coil
Bandwidth (GHz)	25.8	24.3	19.8	19.9
IIP3$_{min}$ (dBm)	20.7	17.7	16.3	19.7
$S_{11_{dd}}$ = -10 dB (GHz)	25.2	34.2	32.4	23.0
Noise (μV_{rms})	205.2	200.0	236.2	206.5
DC gain (dB)	-6.9	-6.9	-7.8	-8.6
Power (mW)	178.2	119.0	89.3	129.9

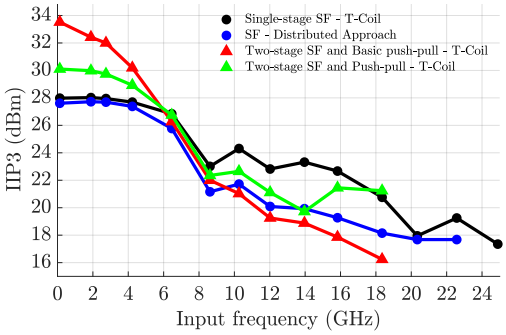


Fig. 13: IIP3 versus f - topologies with more than 18 GHz.

Fig. 13 shows that the two-stage SF and Basic push-pull topologies implemented with the T-coil technique have the higher linearity up to 6 GHz and the single-stage SF with T-coil from 6 to 18 GHz. Moreover, the two-stage SF and push-pull is a good choice for both low, and high frequencies.

V. Conclusions

This paper provided a concise review of IB topologies. It has shown that low output resistance and low input capacitance are required to achieve 18 GHz bandwidth. Linearity improvement techniques, such as drain bootstrapping come at a bandwidth cost. We have shown that the use of bandwidth extension techniques either in a conventional bridged T-coil or a distributed SF approach enabled over 18 GHz BW, albeit with a slight cost to linearity and noise. Likewise, the use of a two-stage topology, using a combination of thick and thin oxide devices allows achieving over 18 GHz BW.

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