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Design Approaches to Enhance Power Density in Power Converters for Traction Applications

Shamar Christian
University of Arkansas-Fayetteville

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Shamar Christian
Howard University
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University of Arkansas

This dissertation is approved for recommendation to the Graduate Council.

_____
Juan C. Balda, Ph.D.
Dissertation Director

_____
Yue Zhao, Ph.D.
Committee Member

_____
Alan Mantooth, Ph.D.
Committee Member

_____
David Huitink, Ph.D.
Committee Member

ABSTRACT

This dissertation presents a design strategy to increase the power density for automotive Power Conversion Units (PCUs) consisting of DC-DC and DC-AC stages. The strategy significantly improves the volumetric power density, as evident by a proposed PCU constructed and tested having 55.6 kW/L, representing an 11.2 % improvement on the Department of Energy's 2025 goal of 50 kW/L for the same power electronics architecture. The dissertation begins with a custom magnetic design procedure, based on optimization of a predetermined C-core geometrical relationship and custom Litz wire. It accounts for electrical and thermal tradeoffs to produce a magnetic structure to best accomplish volume and thermal constraints. This work is coupled with a control strategy for the DC-DC converter whereby a variable-frequency Discontinuous Conduction Mode (DCM) control is used to further reduce the required values of the passive components, to provide an increase in power density and a large improvement of low-power-level efficiency, experimentally demonstrated at full power through an 80 kW Interleaved Boost Converter. Integration of this enhanced DC-DC stage to the DC-AC stage requires a DC-Link capacitor, which hinders achieving power density targets. Increasing the switching frequency is an established method of reducing the size of passives. However, it is the RMS current sizing requirements that diminishes any gains achieved by raising the switching frequency. A synchronous carrier phase shift-based control algorithm, that aligns the output current of the boost stage with the input current of an inverter, is proposed to reduce the RMS current in the DC-Link capacitor by up to 25% and an average 20% smaller capacitor volume. Lastly, a new electrothermal platform based on paralleled discrete devices is presented for a 50 kW traction inverter. Embedded capacitors within the vacant volume of the hybrid material thermal management structure enables higher power density (155 kW/L) and significantly reduces cost.

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DEDICATION

This dissertation is dedicated to my beloved wife, Kirsten Christian, my ever-supportive parents, Fitzmaurice and Patricia Christian, and my trailblazing sister, Dr. LaNyka Weekes.

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   Chapter 2 is made up of this paper.

2. S. Christian, R. A. Fantino, R. Amir Gomez, Y. Zhao and J. C. Balda, "Variable-Frequency Controlled Interleaved Boost Converter," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 2020, pp. 601-606, doi: 10.1109/ECCE44975.2020.9235926.

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6. S. Christian, R. A. Fantino, R. A. Gomez, Y. Zhao and J. C. Balda, " Comprehensive PCU Design Methodology Enabling Reduced DC-Link Capacitor," in IEEE Transactions in Vehicular Technology (pending publication).

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7. S. Christian, Aniket Lad, Nenad Miljokovic and J. C. Balda, " A 155 kW/L 800V Traction Inverter Using Discrete Devices," in ECCE 2023 (pending publication).

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CHAPTER 1

INTRODUCTION

1.1. Motivation and Challenges

The pathway to a more sustainable future avoiding the adverse issue of high levels of CO2 emissions has led to various industrial challenges on traditional fossil fuel economies and technologies. The transportation sector is experiencing increasing demands for commercially viable solutions to reduce global carbon footprints [1], [2]. Recent accomplishments in semiconductor technology with the advent of SiC MOSFETs [3]–[5] (with advantages over Si IGBTs in switching losses, switching frequency and thermal capacity [6]–[8]), and breakthroughs in battery technologies [9], [10] have made the realization of electric vehicles (EVs) a feasible endeavor when compared to vehicles based on internal combustion engines (ICEs).

EVs boast numerous advantages over their ICE counterparts in that they are far more efficient than fossil fuel dependent vehicles, require less maintenance, reduce operational costs, and even boast better safety margins. As such, the demand continues to be met technologically with fully electric and hybrid electric vehicles.

These advantages have technological implications in EV design. However, for these solutions to be profitable, the Department of Energy (DOE) in collaboration with major automotive stakeholders have implemented an all-encompassing metric for the power conversion unit (PCU) and traction systems (i.e., encompassing the electric motor) [11] by which the perfect balance of all technical advantages are achieved through power density. From an engineering perspective, meeting volumetric power density constraints institutes technical objectives that are polysemous for frugal manufacturing intents. Having a smaller footprint requires less materials, reducing the costs to produce the PCU. Smaller volume places demand on the thermal management solutions

with a much larger heat flux leading to control strategies and topologies with reduced system losses for higher efficiency [12].

To this end, the DOE has proposed the US Drive Electrical and Electronics Technical Team (EETT) Roadmap [11] increasing power density to a 2025 target of 33 kW/L for the entire power stage. The decomposition of the power stage and their respective components and their target power densities are shown in Table 1-1.

For the specifications in Table 1-1, it is important to denote the system topology to best accomplish the metrics. Multi-level topologies have been investigated for traction use in [13]. For example, the three-level neutral-point clamped (NPC) inverter [14]–[16] has been considered a great candidate topology to realize a traction drive as it is possible to synthesize lower losses due to each device withstanding half the DC-link voltage. The output THD performance with reduced

Table 1-1 DOE EETT Roadmap for Power Electronics Converters

		2020	2025
ETDS	Power Density (kW/L)	13.4	100
	Cost ($/kW)	3.3	2.7
On-board Charger	Power density (kW/L)	3.5	4.6
	Cost ($/kW)	50	35
DC-DC Buck Converter	Power Density (kW/L)	3	4.6
	Cost ($/kW)	50	30

current ripple also limit losses on the motor stator in this topology [17]. However, it must be noted that there are significant disadvantages that arise with these three-level inverters. Voltage balancing on split DC-link capacitors [18], load current in the DC-link capacitors [19], required complex control strategies and ultimately more switching devices have negative connotations for both cost and power density objectives for manufacturers.

This has led to two-level converters widely adopted for realizing a PCU. For the EV, there are various overall configurations of two-level converters that are typically implemented. Figure 1-1 illustrates the two commonly used traction configurations. The first configuration consists of a two-level inverter directly connected to the high voltage battery via a DC-link capacitor to smooth the ripple current. Offering a reduced component count, weight and volume, this configuration also boasts the opportunity for higher voltage batteries (700-800V) for fast charging within the EV

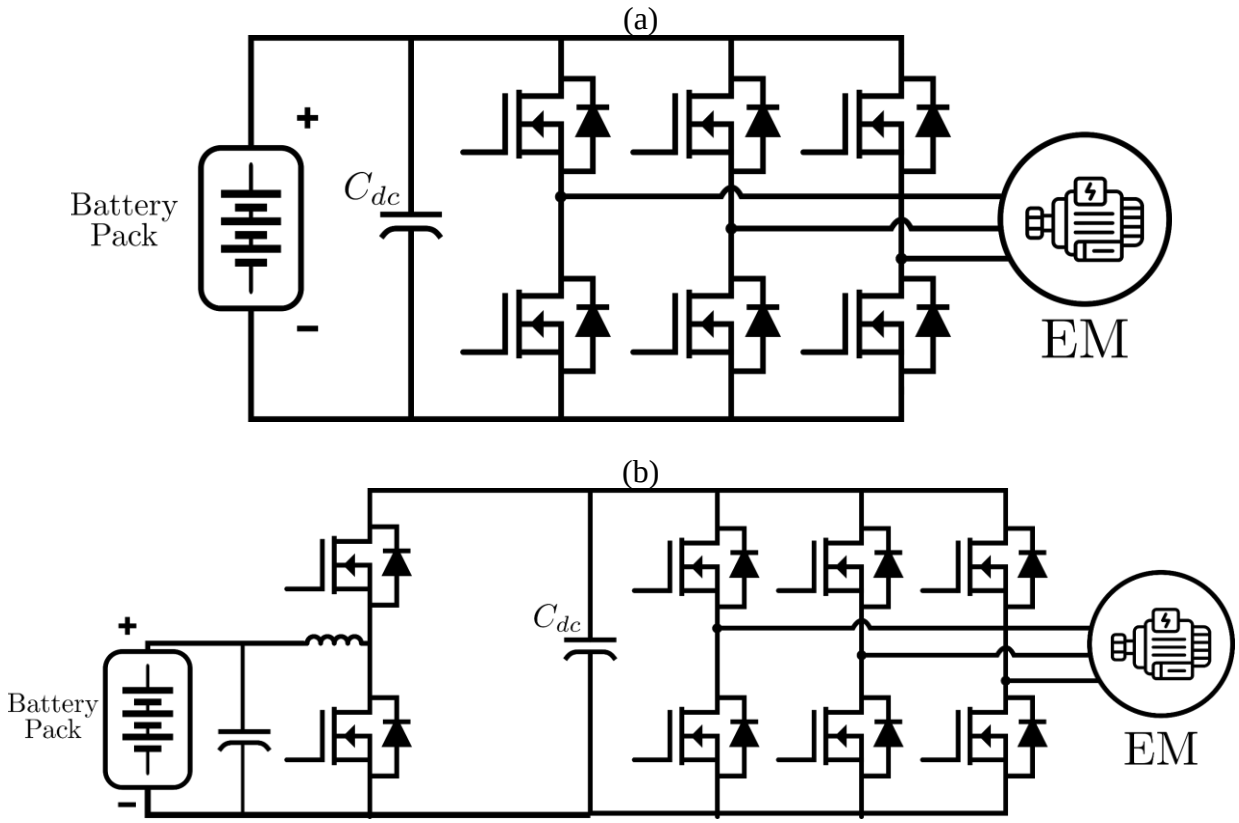

Figure 1-1. (a) Two-level voltage source inverter. (b) Boost-connected voltage source inverter.

[20]. The second configuration in Figure 1-1(b) consists of an intermediate boost converter stage between the battery and inverter. This boosting stage significantly reduces the overall manufacturing cost of the vehicle [21], since a smaller battery pack with voltages, typically 300-400V [22], can be used. Because of the flexibility of this arrangement in "use case" scenarios for EV's and hybrid EV implementations, it is selected as the topology of focus for this dissertation.

To tackle power density for the PCU, it is important to address the sources of large volumes. Typically, the problematic subcomponents of a PCU in addressing power density are the size of the passive components and the thermal management system [23]. Reference [24] indicated that passive components occupy up to 30% of the total converter volume on average, while in [25], cooling methods require 14-33% of the total volume. Therefore, an electro-thermal comprehensive design strategy that both reduces the volume of the passive components and increases the system efficiency is needed to advance power density goals for automotive converters. Beyond power density, efficiency plays a vital role in the determination of battery utilization and range for an EVs [26].

1.2. Existing Volume Reduction Techniques

Passive components play a vital role within a power converter for the storage and release of energy. To reduce energy storage requirements and thus sizes of capacitors or inductors, increasing the switching frequency is a simple and well explored solution, as the storage is inversely proportional to the switching frequency [27]. However, intrinsic to increasing the switching frequency is the undesired effect of increased switching losses in magnetics and active devices. Larger heat fluxes in switching devices give rise to reliability and efficiency related failure [28], necessitating a larger thermal architecture i.e. a cold plate or heat sink, offsetting any advantages

gained in volume. Therefore, increasing switching frequency may not be the best straight-forward approach.

1.2.1. Techniques in DC-DC Converters

Within the boosting DC-DC stage for PCUs, the inductor often occupies significant volume and produces large losses in traditional fixed PWM control strategies under continuous conduction mode (CCM) operation [29]. At low power levels, the inductor and switching devices must still process switching losses. In [30], a comparison of several topologies and configurations for the DC-DC converter to reduce the converter overall volume was presented as possible solutions. However, the topologies presented provide marginal increments of low power levels efficiency increase at the expense of power density and cost.

Soft-switching approaches in [31], [32] have been investigated extensively in applications since the significantly reduced losses can minimize the volume of the thermal solution. For example, [33] implemented a snubber assisted soft-switching converter with an auxiliary resonant tank. However, almost all implementations of these converters require auxiliary circuitry which increases cost, complexity and ultimately volume, while having a limited soft-switching range.

References [34], [35] proposed the use of two coupled inductors to interleave boost converters. The switching devices only see half of the frequency of the coupled inductor, therefore lowering switching losses. However, the additional ripple in the inductor leads to additional magnetic losses. With increasing the switching frequency also comes additional undesired EMI. The induced currents from non-operating phases through the coupled inductor can be a hindrance in stability and performance [36]. Interleaving boost converters effectively reduces the rms currents applied to the output capacitor, and allows operation at reduced switching frequencies, which results in

reduced switching losses. Thus, an interleaved DC-DC converter is advisable for the boosting stage.

1.2.2. Techniques in DC-DC + DC-AC Converters

Integrating of both stages has been studied for motor drive applications with a high DC-bus voltage requirement [37]. However, integration for EV applications have been seldom explored. Implementations of these configurations primarily focus on varying the DC-link voltage at low power levels to keep a large modulation index as possible for decreased THD in the inverter and overall higher efficiency [38].

Regarding power density, the authors in [39] made the output current in the DC-link equal to that of the inverter input current such that the capacitor current is essentially null. However, this is achieved using large inductors in the DC-DC converter operating under hard-switching conditions under CCM, resulting in both a low power density and low system efficiency. There is a need for an algorithm reducing the RMS current of the DC-link capacitor over a wide range of power levels.

1.2.3. Inverter Design Platforms

For modern high-power inverters, SiC power modules have been the leading driver of the converter overall layout due to the electrothermal relationship between the power module and the thermal management system [5], [40]. Traditionally, the power modules construction consists of electrical terminals for the positive and negative buses, as well as the midpoint connection parallel to the baseplate for heat transfer [41]. The cold plate matches the baseplate surface area to maximizing the flow of heat [42], often leading to a monolithic form with internal features on which the modules are secured. In this manner, the converter design follows this simplistic

unidirectional arrangement, with the cold plate stacked below the module, and the bussing atop the terminals.

However, in this arrangement, the integration of the required DC-link capacitors becomes difficult. To mitigate parasitic stray inductances, it is common practice to minimize the commutation loop by placing the capacitor as close as possible to the power module [43]. As a result of the module's planar construction, additional converter volume must be taken to place the capacitor atop or in proximity to the module; a compromise which hampers any power density potential.

1.3. Proposed Solution and Objectives of the Dissertation

Given the requirement for reducing the size of all the passive elements within the PCU in conjunction with high efficiency, a phase-shift based modulation strategy for an interleaved boost converter operated with a variable DC-bus voltage under discontinuous conduction mode (DCM) [44] and synchronized with a two-level inverter is proposed in this dissertation. This method not only reduces the RMS current in the DC-link capacitor leading to decreased capacitor volume and increased reliability, but it also allows for a reduction in the inductor volume due to low inductance requirements under DCM that enhances efficiency due to the zero-current switching (ZCS) in the boost stage [45], [46] with DCM in conjunction with a variable DC-link voltage [47], [48].

Half-bridge converters are fundamental in realizing the entire system. Typically, power modules are considered in high-power applications where this configuration is needed, as there is provision for cooling the module base plate and electrical isolation from the power devices inside [49]. However, power modules are typically expensive and occupy significant volume with their necessary cold plate-based thermal management. Discrete-packaged semiconductor devices

provide a flexible and cost-effective solution for scalable highly dense power electronics [3]. Therefore, a new power electronic platform based on paralleled discrete devices is presented to further the power density of the traction inverter. Because the electrical connections can be perpendicular to the thermal path, a hybrid cold plate structure consisting of additively manufactured materials and aluminum can be produced to significantly reduce both, volume and even mass without thermal performance compromise. The capacitors are embedded within the useful volume of the thermal management structure, enabling higher power density (155 kW/L) and significantly reducing overall cost. The specific objectives of the dissertation are as follows in the flow chart shown in Figure 1-2.

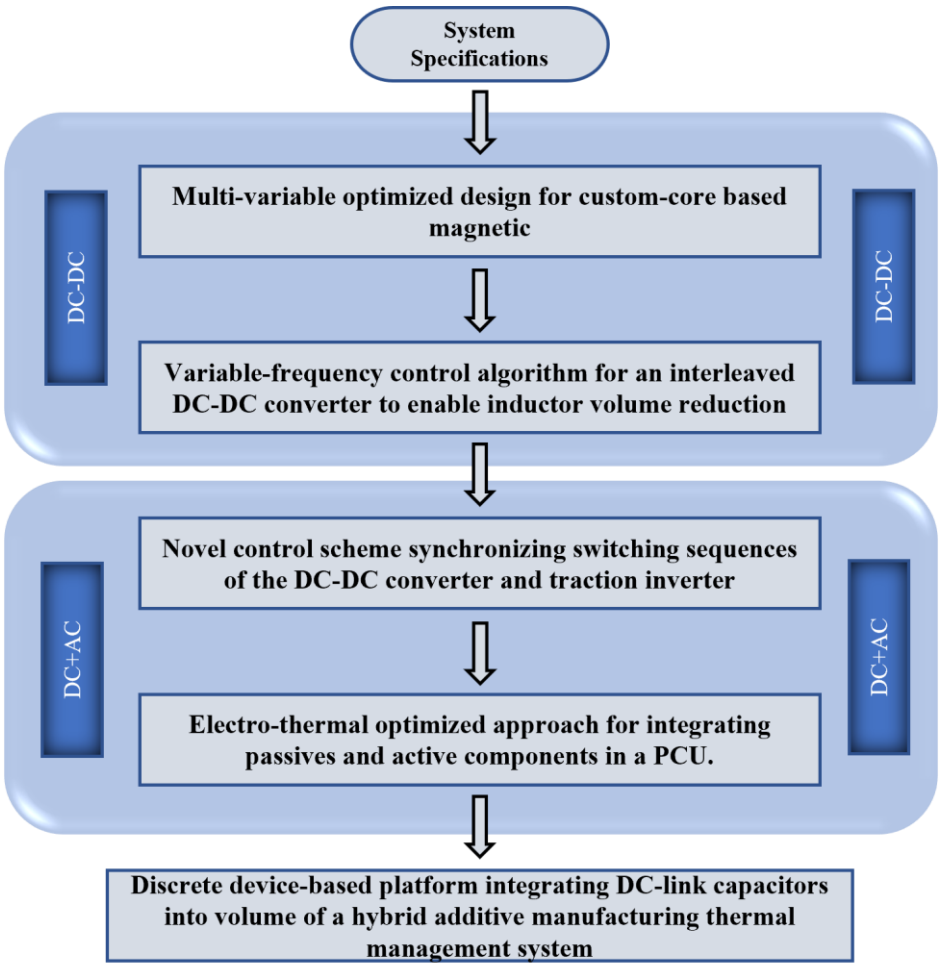

Figure 1-2. Flowchart depicting specific objectives of the dissertation.

The tangential thermal management work addressed for these converter systems are done in collaboration with researchers at the University of Illinois Urbana-Champaign through the NSF Power Optimization of Electro-Thermal Systems (POETS) Engineering Research Center.

1.4. Organization of the Dissertation

The organization of this dissertation is broken into three distinct tiers. The first one addresses the DC-DC converter as an individual entity. A custom-core optimized design method for the inductor is presented in Chapter 2. The DCM variable-frequency control strategy for the converter is presented afterwards in Chapter 3 as a means to increase the efficiency of the stage with smaller passive requirements.

In the second tier, system level integration is presented through the thermal management of the inductors with encapsulation in Chapter 4. All the previous work for a comprehensive design method for the DC-DC stage, culminating in an 80 kW prototype being fabricated and experimentally tested with a power density of 55.6 kW/L comes together in Chapter 5.

The third tier focuses on the integration of the DC-DC converter and the DC-AC inverter. The synchronous control strategy that phase shifts a traditional space vector modulation to reduce the RMS currents in the DC-link capacitor is given in Chapter 6. A design approach for an 80 kW PCU with said strategy, entailing the detail of the design and working from the DC-DC stage to the inverter is outlined in Chapter 7. Chapter 8 covers the design of a 50 kW 155 kW/L traction inverter using parallel discrete devices and embedded capacitors within a hybrid thermal structure.

The major conclusions from this work and future work are presented in Chapter 9.

1.5. Contributions of this Research

The main contribution of the presented research is a novel control method which synchronizes the switching sequences of the DC-DC converter and DC-AC inverter stage of a PCU to produce cancellation of currents in the DC-link capacitor between the stages [50]. Because of the capacitor RMS current reduction, a smaller volume capacitor can be selected as the RMS current handling capacity is typically proportional to the capacitor volume. This increases the power density by 20% and the lifetime of the capacitor itself, enhancing PCU reliability. Furthermore, this control is coupled with a loss-reducing strategy in the DC-DC boosting stage, whereby a variable-frequency DCM state reduces the inductor size while providing advantages in efficiency.

A comprehensive design methodology encompassing the aforementioned is summarized below:

1. Custom-core magnetic design strategy and lamination acid etching process.
2. Variable-frequency DCM control strategy for DC-DC converters.
3. Electro-thermal considerations and analysis for both passive and active components.
4. Novel synchronous PCU control algorithm.

This results in the design and testing of an 80 kW 55.6 kW/L interleaved boost converter, 80 kW PCU with 55.6 kW/L and a 50 kW discrete device traction inverter with 155 kW/L.

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CHAPTER 2

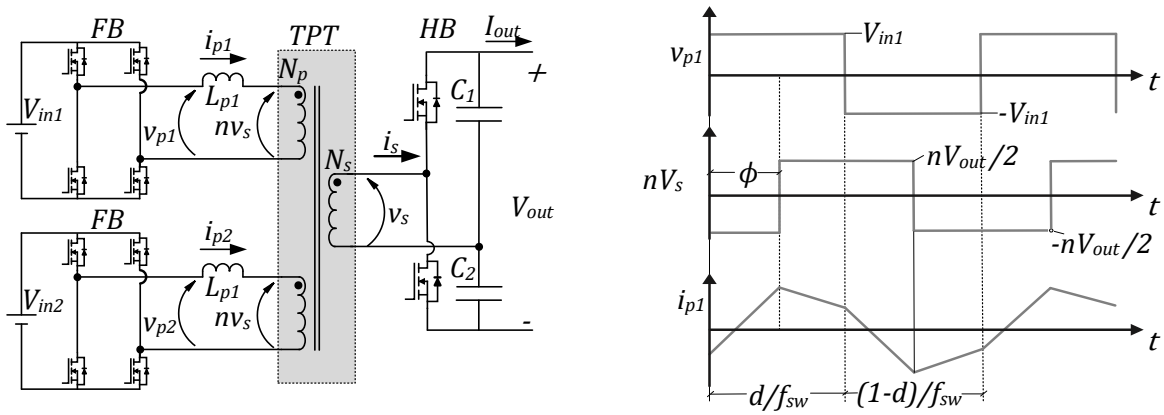
MAGNETIC DESIGN METHODOLOGY

2.1. Abstract

The design of a 150-kW high-frequency three-port transformer (TPT) for a triple active bridge (TAB) converter application is the focus of this paper. A non-tradeoff inclusive design methodology for custom-core transformers is proposed. Classic transformer design methodologies based on complex trade-offs mechanisms require significant effort to adjust the design for commercially available pre-sized cores. The proposed design is based on the development of a set of design equations that allows to select the core dimensions and the turns numbers for the windings that best accomplish the transformer specifications. Experimental evidence verifying the proposed theoretical design methodology is presented in this work.

2.2. Introduction

Renewable energy distribution is heavily dependent upon the development and reliability of power electronic high-power conversion systems [1], [2]. In general, these systems require the use of transformers to meet galvanic isolation requirements. Development of high-efficiency high-frequency transformers is a growing trend to pursue size reduction and increasing power density [3], [4]. Typical transformer design methodologies involve the implementation of complex trade-off design algorithms that should be adjusted to commercially available pre-sized cores [3]–[7]. However, recent developments in manufacturing capabilities of core materials allow for producing geometrically customized cores. This work presents the design of a 150-kW TPT for a TAB converter [8]–[10]. A design methodology that allows an optimized selection of a customized core



(a) (b)

Figure 2-1. (a) TAB topology, (b) Main theoretical TPT waveforms at rated power.

avoiding undesirable trade-offs when using commercial cores is proposed. By developing a set of equations as a function of on one core dimension and the number of turns of one winding, the best solution for these two parameters will define all the remaining transformer characteristics. The proposed method is verified by building and experimentally testing the designed transformer.

2.3. Operating Conditions of TPT in TAB

Figure 2-1 (a) shows the TAB circuit topology [1]–[3]. The input stage DC voltages V_{in1} and V_{in2} feed two full-bridge (FB) converters whose AC output voltages v_{p1} and v_{p2} inject the currents i_{p1} and i_{p2} to the TPT primaries through the external inductors L_{p1} and L_{p2} (whose design is outside the scope of this report). The TPT turns ratio is $n = N_p/N_s$, where N_p and N_s are the numbers of turns of the two primaries and the secondary, respectively. The TPT AC output voltage v_s, feeds the current i_s to the half-bridge (HB) converter stage with a fixed controlled DC output voltage V_{out}. The three converters operate at a switching frequency f_{sw} and a fixed duty cycle $d = 0.5$.

Figure 2-1 (b) shows the TPT typical waveforms for maximum power transfer. In the shown conditions, v_{p1} and v_{p2} are in phase at nominal value while the current through the TPT is controlled by phase-shifting v_s by an angle ϕ [10].

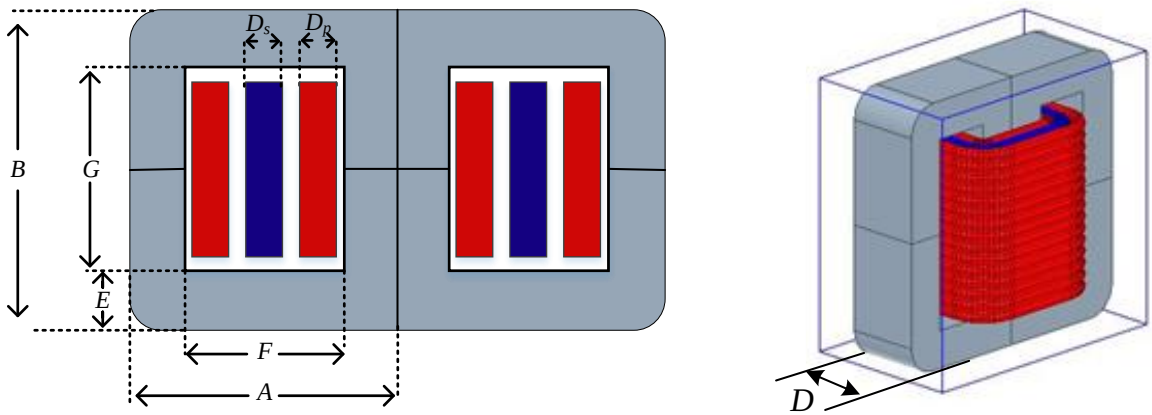


Figure 2-2. Transformer structure and dimensions.

2.4. TPT Design Methodology

2.4.1. Selection of Magnetic Core material and Wire

The TPT design begins with the magnetic core material and winding wire selection. Figure 2-2 shows the considered E type core transformer structure with core geometric dimensions (A, B, F, G, D, E). It is selected $E = D/2$ to have a square shape central leg. Each winding is built in a single layer to reduce losses and leakage inductance, with the secondary placed (concentrically wound) between the two primaries [11]. To reduce high-frequency skin effect losses, S_p and S_s strands of Litz wire with cross section area A_{litz} [12], are used for the primaries and secondary, respectively. Let $A_p = \delta A_{litz} S_p$ and $A_s = \delta A_{litz} S_s$ be the total areas of the two primaries and secondary windings, respectively, where δ is the wire fill factor (including insulation). The total diameter of the wires can be expressed as $D_p = 2\sqrt{A_p/\pi}$ and $D_s = D_p\sqrt{S_s/S_p}$. The mean lengths per turn of the primaries and the secondary can be estimated as $l_{p1} = 4(D + D_p)$, $l_{p2} = 4\left[D + \left(3 + 2\sqrt{S_s/S_p}\right)D_p\right]$ and $l_s = 4\left[D + \left(2 + \sqrt{S_s/S_p}\right)D_p\right]$. Remaining dimensions are $F = D_p\left(2 + \sqrt{S_s/S_p} + K_{ext}\right)$, $A = (F + D)$, $G = D_p\left(N_p + K_{ext}\right)$ and $B = (G + D)$, where $K_{ext} = 1$ is a coefficient used to leave extra space $D_{ext} = K_{ext} D_p$ for the wire insulation and bobbin.

2.4.2. Copper Losses, Core Losses and Temperature Rise

Design equations depending only on N_p and D are developed. Due to Litz wire utilization, the AC resistance of the windings can be considered approximately equal to its DC resistance [13]. Hence, an estimation of the copper losses in the windings are made as follows:

$$P_{cu} = \frac{\rho_{cu} N_p}{A_{litz}} \left[\frac{(l_{p1} + l_{p2})}{S_p} I_p^2 + \frac{l_s}{nS_s} I_s^2 \right] = k_{cu}\left[D + D_p\left(2 + \sqrt{S_s/Sp}\right)\right], \quad (1)$$

where I_p and I_s are the rms values of i_p and i_s respectively, $\rho_{cu} = 1.68 \times 10^{-8}\Omega/m$ and $k_{cu} = (4\rho_{cu}N_p/A_{litz})\left[2I_p^2/S_p + I_s^2/(nS_s)\right]$. A square-wave voltage magnetizing the TPT (see nv_s in Figure 2-1) will produce a triangular flux density waveform with peak value $B_{max} = \frac{V_{max}}{4f_{sw}N_pA_c}$ [14], [15]. Core losses are estimated by using the Improved Generalized Steinmetz Equation [5], [14], [15]:

$$P_{fe} = V_{fe} k_i f_{sw}^{\alpha} B_{max}^{\beta} \quad ; \qquad with \quad k_i = \frac{2^{(\alpha+1)} K_c}{\pi^{(\alpha-1)}\left(1.1044 + \frac{6.8244}{\alpha + 1.354}\right)} \ , \quad (2)$$

where α, β and K_c are the core Steinmetz coefficients. In (2), the core volume can be expressed as $V_{fe} = 2D^2\left[D + D_p\left(5 + N_p\right)\right]$, with $A_c = D^2 K_{eff}$ being the core effective cross-sectional area, and K_{eff} the core stacking factor. By combining equations (1) and (2), the total TPT losses are given by:

$$P_T = P_{fe} + P_{cu} = k_{fe} D^{2(1-\beta)} N_p^{-\beta}\left[D + D_p\left(5 + N_p\right)\right] + k_{cu}\left[D + D_p\left(2 + \sqrt{S_s/S_p}\right)\right], \quad (3)$$

where $k_{fe} = \left[2^{(1-\beta)} f_{sw}^{(\alpha-\beta)} V_{max}^{\beta} K_{eff}{}^{-\beta} k_i\right]$. Note that in (3), N_p and D are the only two parameters that need to be selected, while the remainder are system parameters or previously determined core material and wire parameters. To obtain an estimate of the transformer rise in temperature, the basic relationship for heat transfer by convection $P_T = hA_{surf}\Delta T$ is used [17], where ΔT is the rise

in temperature of the TPT surface (of area A_{surf}) with respect to the ambient, and h is an empirical heat transfer coefficient ($h = 22\ W/m^2$ is used in this work). By using the core plus windings volume $V_{fecu} = V_{fe} + V_{cu}$, with $V_{cu} = \pi D_p^2 N_p\left[2 + S_s/(nS_p)\right]\left[D + \left(2 + \sqrt{S_s/S_p}\right)\right]$, the simplified expression $A_{surf} \approx \sqrt[3]{36\pi V_{fecu}^2}$ that corresponds to the surface area of a sphere with a volume V_{fecu} is generated. By inserting the losses from (3), the transformer surface rise in temperature can be estimated by:

$$\Delta T \approx \frac{k_{fe} D^{2(1-\beta)} N_p^{-\beta}\left[D + D_T(5 + N_p)\right] + k_{cu}\left[D + D_p\left(2 + \sqrt{S_s/S_p}\right)\right]}{h\sqrt[3]{36\pi}\left\{2D^2\left[D + D_p(5 + N_p)\right] + \pi D_p^2 N_p\left[2 + \frac{S_s}{nS_p}\right]\left[D + \left(2 + \sqrt{S_s/S_p}\right)\right]\right\}^{2/3}}. \quad (4)$$

Furthermore, it is desirable to limit the total transformer volume V_T that it will occupy in a cabinet:

$$V_T = D^2\left[2D + D_p\left(N_p + 2\sqrt{S_s/S_p} + 7\right)\right] + D_p(N_p + 1)\left[D + 2D_p\left(3 + \sqrt{S_s/S_p}\right)\right]\left[D + 2D_p\left(2 + \sqrt{S_s/S_p}\right)\right]. \quad (5)$$

Unlike V_{fecu}, V_T additionally considers the extra space volume for bobbin and insulation.

2.5. Transformer Prototype Design

In this section, a TPT for a TAB with the specifications listed in Table 2-1 is designed. Because of its advantages considering the design requirements [5], [18], [19] nanocrystalline core material with the parameters listed in Table 2-2 is selected. To satisfy J_{max}, commercially-available

Table 2-1: System Specifications

Symbol	Value
n	1
f_{sw}	20 kHz
η	> 99.6 %
J_{max}	3A/mm^2
V_{in} ; V_{out}	1.3 kV ; 2.6 kV
I_{smax}; I_{pmax}	135Arms; 67.5Arms
V_T	< 20 L
ΔT	<100 °C

Table 2-2: Core Characteristics

Symbol	Value
α	1.2077
β	1.6456
K_c	2.2991 W/m^3
K_{eff}	0.78

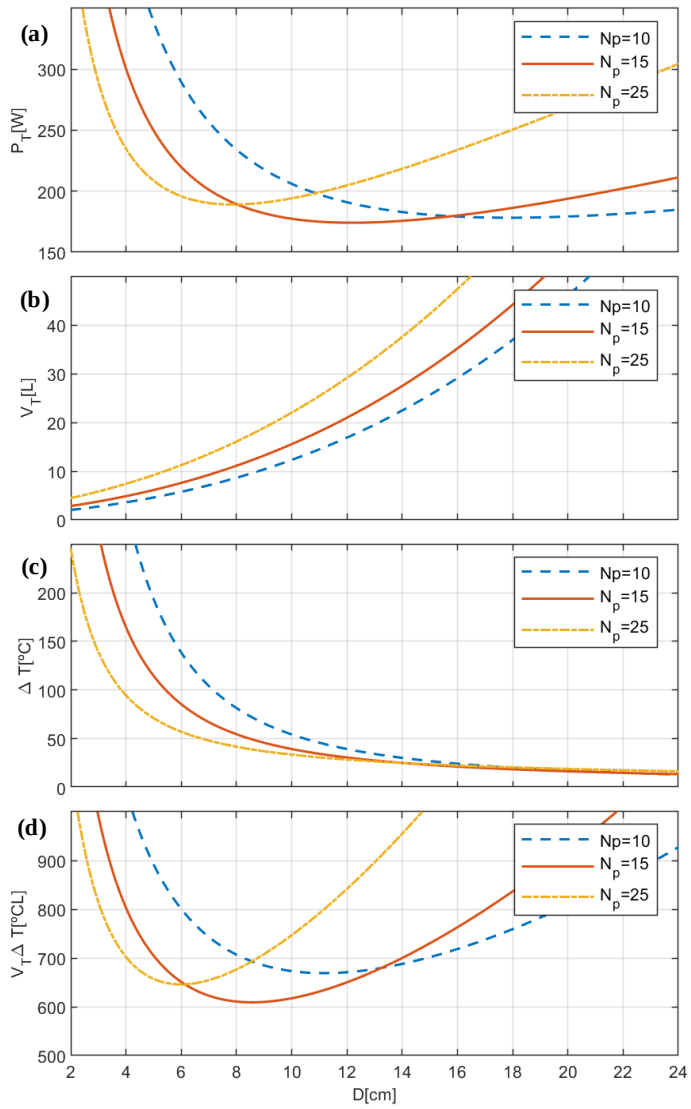


Figure 2-3. (a) P_T[W]. (b) V_T[L]. (c) ΔT[ºC]. (d) $V_T \Delta T$.

Litz wire with 4000 strands of $A_{litz} = 0.0131mm^2$ (adequate for $f_{sw} = 20kHz$) is selected. With the aim of keeping low copper losses and low building complexity, this wire is selected for all

windings, resulting $S_s/S_p = 1$ and D_p =12.39mm. Having selected the core material and the wire, the equations presented in Section 2.4 can be analyzed in order to select the parameters N_p and D that best satisfy the TPT design requirements. For the converter operating at nominal conditions and maximum power transferred $P_o = 150$kW, Figure 2-3 (a) shows P_T (3), evaluated for three values of N_p (10,15 and 25), and for $2cm < D < 24cm$. Similarly, Figure 2-3 (b) shows the total volume V_T (5), and Figure 2-3 (c) shows the temperature rise ΔT (4). Minimum P_T is the target usually considered in transformer design [15], however this does not occur at optimum values of V_T. The goals in this work are to minimize ΔT to avoid introducing system losses via complex cooling methods [3], and to minimize V_T for cost and size reductions. To consider these goals (oppositely related through D), the cost function $\Delta T x V_T$ plotted in Figure 2-3 (d) is obtained; For each N_p, there is a value of D for which $\Delta T V_T$ has a minimum, and there is a global minimum for a particular N_p. The set of N_p and D that minimizes $\Delta T V_T$ can be analytically obtained by evaluating the equation obtained by multiplying (4) and (5). For the current design, the minimum occurs for $N_P = 15$ and $D \approx 8$ cm. By selecting these values, the remaining core parameters are determined following the procedure presented in section III. The resultant designed TPT, with a theoretical efficiency of η_{th} =99.875%, has been constructed and is shown in Figure 2-4(a). The TPT design methodology can be summarized as follows:

- Select core material and geometry.
- Select winding wires based on operating frequency and J_{max} requirement.
- Express core and winding dimensions based on N_p and D.
- Compute (3), (4) and (5) through iterations of N_p and D.

(a)

(b)

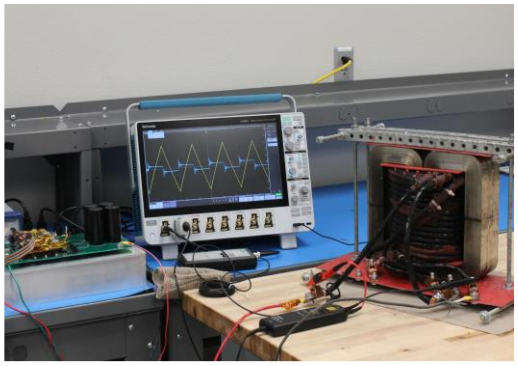


Figure 2-4. (a) Designed TPT. (b) Experimental setup.

- Select the values of N_p and D that best accomplish design targets. In the presented design, the solution minimizing the cost function ΔTV_T has been selected.

2.6. Experimental Results

In order to calculate the losses produced in the constructed TPT, open-circuit (OC) at nominal voltage operation and short-circuit (SC) at nominal current operation were performed by using an available 2000V – 100A FB converter. The picture in Figure 2-4(b) shows part of the experimental setup used to implement the tests. Supporting waveforms of current and voltage for the OC and SC tests are shown in Figure 2-5(a) and Figure 2-5(b) respectively. For an applied nominal 1300V square wave, $P_{oc} = 129$ W of core losses were measured in the OC test, corresponding to a $R_m = (1300V)^2/129W \approx 13$ kΩ magnetizing resistance. By using the slope of the OC current shown

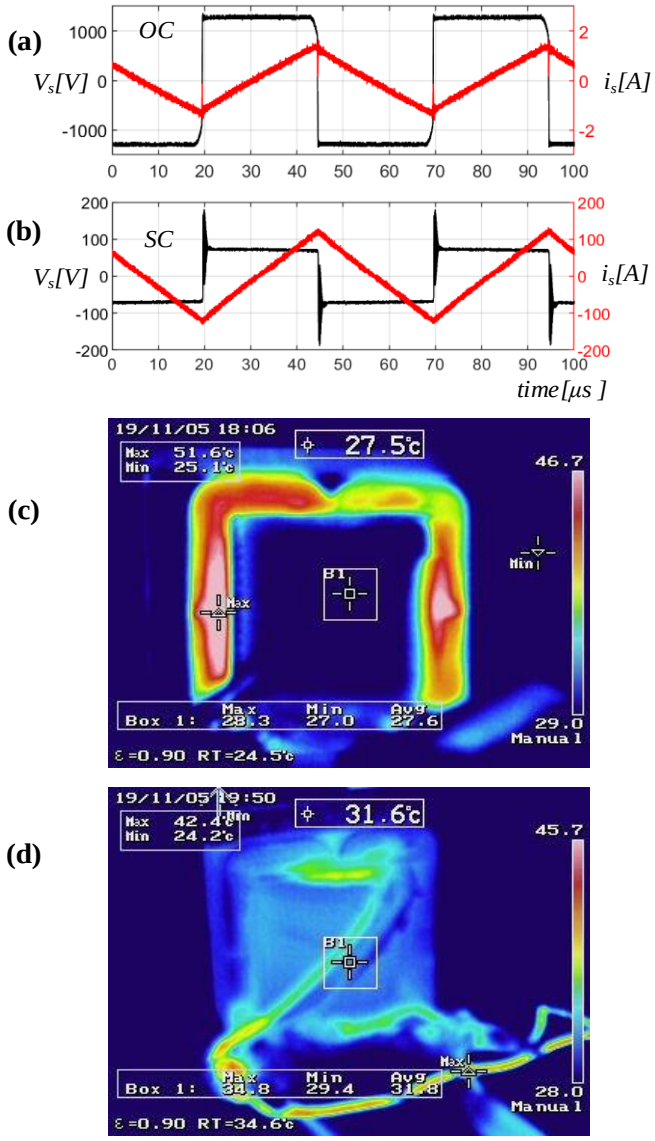


Figure 2-5. (a) OC Test Waveform. (b) SC Test Waveform. (c) Thermal image for OC. (c) Thermal image for SC.

in Figure 2-5(a), a $L_m \approx 12.5$ mH magnetizing inductance can be calculated. For the same condition, the theoretical losses obtained by using (2) results in $P_{fe} = 118$ W, the difference could be attributed to a slight error in the used core Steinmetz coefficients or staking factor. By using the measured OC losses in (4), $\Delta T \approx 31°C$ is expected in the OC test, close to the rise in temperature $\Delta T \approx 27°C$ that can be seen in the thermal image shown in Figure 2-4(c). The SC test was

implemented for a $I_{sc} \approx 67.5A_{rms}$ current applied between one primary winding and the secondary (short-circuited winding). For this test, the measured losses were $P_{sc} \approx 100$ W, with which the resistance of the two windings in series can be calculated as $R_{sc}=P_{sc}/I_{sc}^2 \approx 20m\Omega$. By assuming that the two windings have the same impedance, the per winding series resistance can be approximated as $R_s \approx 10\ m\Omega$. The slope of the SC current shown in Figure 2-5(b), corresponds to a per winding leakage inductance $L_{lk} \approx 3.5\ \mu H$ can be calculated. By using the estimated per winding resistance, the copper losses in the three winding for the TPT operating in nominal conditions can be estimated as $P_{cu} \approx (2I_{pmax}^2+I_{smax}^2)R_s \approx 273W$, then expected total losses at rated power are $P_T = P_{oc} + P_{cu} \approx 402W$, yielding an efficiency of $\eta = 99.73\%$, satisfying the design specifications given in Table 2-1.

2.7. Conclusion

A design methodology for a custom-core transformer design was proposed and experimentally verified for the design of a 150-kW 20-kHz three-port transformer for a triple active bridge converter application. The open-circuit and short-circuit tests were implemented on the constructed transformer at nominal voltage and current ratings, producing results very close to the theoretically calculated values. In accordance with the obtained results, a high efficiency of 99.73% is expected for the transformer operating at nominal conditions.

2.8. Acknowledgements

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CHAPTER 3

VARIABLE FREQUENCY CONTROL STRATEGY

3.1. Abstract

Efficiency over the entire power range is an important performance metric for traction applications since electric vehicles (EVs) operate at very different power levels, in particular, lower power levels are more common for city driving. DC-DC converters operated under conventional pulse-width modulation (PWM) techniques at constant switching frequency experience significantly lower efficiencies at low power levels. To cope with this issue, this work addresses a bidirectional discontinuous-conduction mode (DCM) and variable-frequency control strategy for a three-phase interleaved boost converter to provide an improvement of the system efficiency at low power levels. The validity and effectiveness of the proposed approach are demonstrated by both simulation and experimental results on a 10-kW prototype.

3.2. Introduction

The increasing demand for environmentally friendly transportation has driven the development of electric vehicles (EV) within the automotive sector [1], [2]. The development of these EVs must meet efficiency specifications in order to realize increased performance and savings in fuel economy. In EV traction systems, there are typically two configurations to achieve the aforementioned goals. The battery of the EV is directly connected to the inverter in the first one [3], [4]. The battery to the propulsion inverter connected through a bidirectional DC-DC converter (typically a boost converter) in the second one. Advantages arising from the latter are due to the ability to optimize individually the design of the traction drive subsystems (battery,

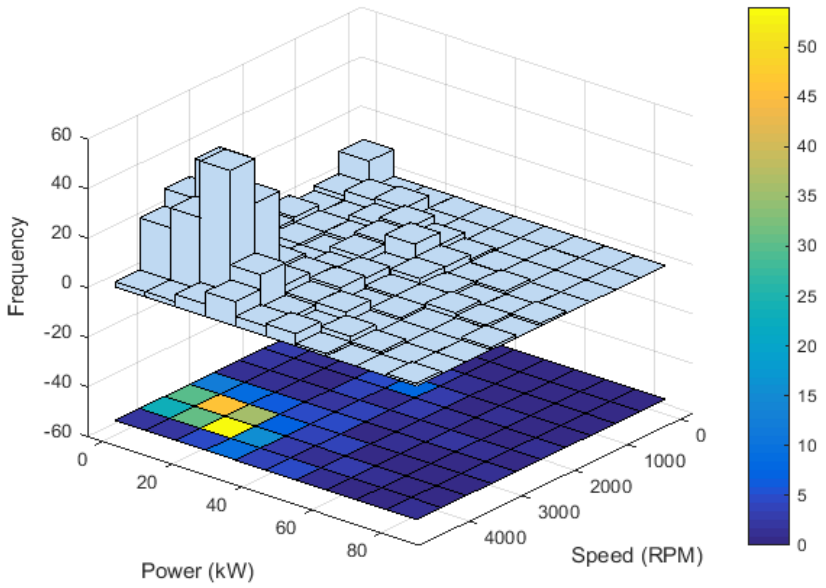


Figure 3-1. Power vs speed operating point density for US06 driving schedule.

motor etc.) [5]. However, overall advantage of this configuration is hinged upon the efficiency of the DC-DC stage, particularly over an entire driving schedule. Figure3-1 [6] is an example of the US06 driving schedule for an 80-kW rated system. It illustrates that the most frequent operation takes place for power levels less than 20% of the nominal rating. This implies that the use of a converter providing high efficiency within such power levels is decisive in enhancing battery performance. Therefore, the technological challenge addressed here is the design of DC-DC converters providing high efficiency at both high and low power levels. Bidirectional DC-DC boost converters are typically implemented with conventional complementary PWM control strategies with constant switching frequency, which exhibit reduced efficiency at low power levels [7], [8]. In such conditions or even when there is no power transferred to the load, the system is still coping with high switching and conduction losses due to current circulating among the reactive components of the converter.

Alternatively, discontinuous conduction mode (DCM) variable-frequency control techniques allow for the minimization of losses at low power levels because the switching frequency and its

associated losses are reduced proportionally to the load [9]. These techniques are usually limited to low power applications [10], as switching devices are required to operate with large current peaks that can increase conduction losses. However, wide band gap materials (particularly silicon carbide (SiC)) are providing MOSFET devices with large current peak capabilities and very low drain to source on-resistance, opening the possibility to implement DCM frequency control techniques for high power applications [11].

This work proposes increasing the low-power level efficiency of SiC-based DC-DC converters in traction applications through a control strategy implemented for a three-phase interleaved boost converter. The control strategy is based upon varying the converter switching frequency according to operating power requirements, while simultaneously remaining at DCM with a fixed value of peak current. The approach combines the advantages of interleaved operation at medium and high power levels [12], with the advantages of loss reduction of the frequency control at low-power levels. Also, the proposed control strategy provides a mechanism that naturally changes from boost to buck operation allowing bidirectional power flow. Additionally, the DCM operation assists in reducing the size of the filter inductors thus increasing the power density of the overall converter [13].

Through the proposed control method to the converter design in this work, a fairly constant value of efficiency can be realized through all power levels, as opposed to conventional duty-based control techniques that experience lower efficiencies at low power levels. The DCM variable-frequency control is validated through the design of a 10-kW three-phase interleaved boost converter.

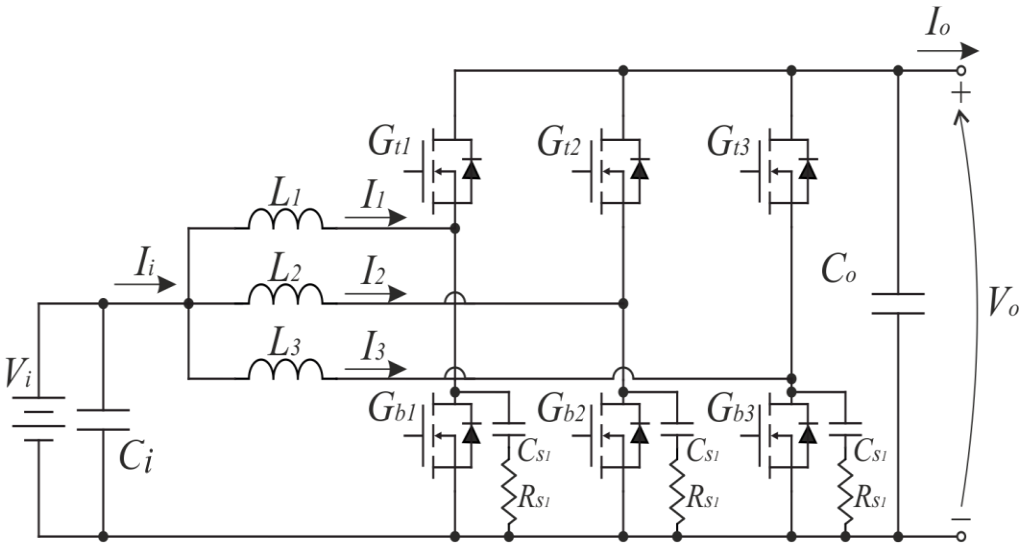


Figure 3-2. Proposed three-phase boost interleaved DC-DC converter topology.

The topology of the converter and the proposed control algorithm are addressed in Section 3.3. Analysis of the system loss mechanisms are made in Section 3.4. Featured design elements following the control strategy are highlighted in Section 3.5. The proposed ideas are then validated through simulation and experiments in Section 3.6 and 3.7, respectively.

3.3. System Description and Control Strategy

The bidirectional three-phase interleaved boost converter circuit is shown in Figure 3-2. The input stage represents a battery bank of voltage V_i with a parallel filtering capacitor C_i, which supplies the total input current I_i to the inductors L_1, L_2 *and* L_3, corresponding to the three boost stages composed of the bottom switches G_{b1}, G_{b2}, and G_{b3}, and top switches G_{t1}, G_{t2}, and G_{t3}, respectively. The three boost phases of the converter are connected to the output capacitor C_o that filters the converter output voltage V_o applied to a load represented by the current I_o. Figure 3-3 illustrates the block diagram representation of the proposed DCM control strategy. The measured value of the output voltage V_o is compared to a specified reference voltage V_{or}. The produced error is then applied to a proportional-integral (PI) controller. The output of the PI controller generates

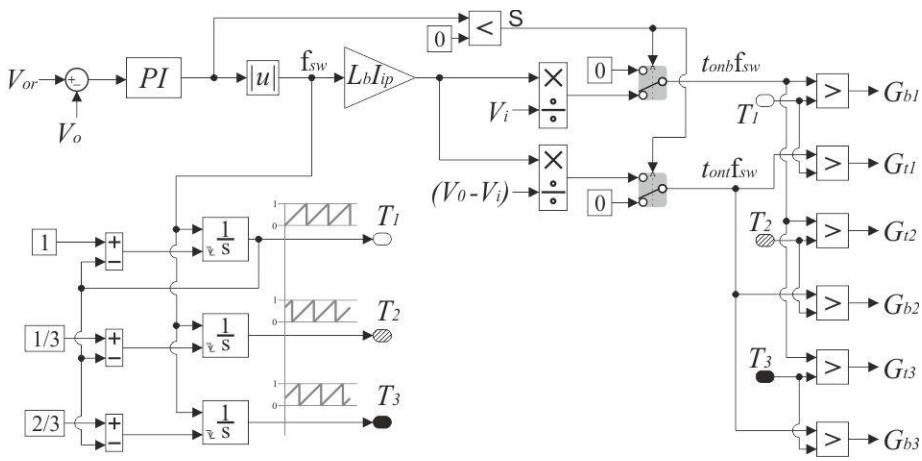


Figure 3-3. Control strategy implementation block diagram.

the magnitude value of the switching frequency f_{sw}. Three equally delayed sawtooth carriers T_1, T_2 and T_3, of frequency f_{sw}. are generated by using the block diagram in Figure 3-3. Note that if $V_{or} > V_o$, the output of the PI controller will be positive, and the signal S will be zero. In this condition, the system delivers power to the output in boost mode operation, being the gate signals G_{t1}, G_{t2}, and G_{t3} equal to zero. The turn-on time t_{onb} of the bottom switches G_{b1}, G_{b2}, and G_{b3}, is generated as:

$$t_{onb} = L_b \frac{I_p}{V_i}, \tag{1}$$

where L_b is the value of the boost inductances (i.e. $L_1 = L_2 = L_3 = L_b$), I_p is the desired inductors current peak, and V_i is the measurement of the input voltage.

Alternatively, if $V_{or} < V_o$, the output of the PI controller will be negative and the signal S will be 1. In this condition the system operates in buck mode, with the direction of the power flowing from the output to the input, and being G_{b1}, G_{b2}, and G_{b3} equal to zero. The turn-on time t_{ont} of the top switches G_{t1}, G_{t2}, and G_{t3}, is generated as:

$$t_{ont} = L_b \frac{I_p}{(V_o - V_i)}, \tag{2}$$

where $(V_o - V_i)$ is the difference between the measured values of the output and input voltages. The value of f_{sw} generated by the controller is a function of the load magnitude. Ideally, if the load current is zero (i.e., $I_o = 0$) and the output capacitor C_o is charged to V_{or}, f_{sw} will be zero because no current pulses are required to supply power to the load. Note that the converter losses will be zero in this ideal condition. From this condition, if I_o increases, f_{sw} of the current-pulse-train also increases supplying power to the load while the capacitor voltage is kept at the reference value. The converter losses are hence a function of f_{sw}, being reduced as the load and switching frequency are reduced; thus, improving the low power efficiency of the system.

3.4. Loss Mechanisms

For a theoretical understanding of the motivation and effectiveness of the converter DCM variable-frequency control strategy in reducing the losses at low power levels, the main loss mechanisms in the converter are analyzed next. For simplicity, the analysis is done considering boost mode operation at nominal values V_i and V_o of the input and output voltage, respectively.

3.4.1. Inductor Losses

The losses produced in the inductor magnetic cores can be analyzed by considering a singular DCM inductor current pulse of peak I_p, as is shown in Figure 3-4(a). When this current pulse is applied to an inductor with N number of turns, the B-H hysteresis loop displayed in Figure 3-4(b) is generated in the core [14]–[17]. The eddy current and hysteresis energy per unit volume dissipated in the core during this current pulse is given by the area W enclosed by the hysteresis loop. As the same current pulse is applied to the three interleaved boost stages in Figure 3-2 with a frequency f_{sw}, the total core losses of the converter can be represented as:

$$P_{core} = 3V_c W f_{sw}, \tag{3}$$

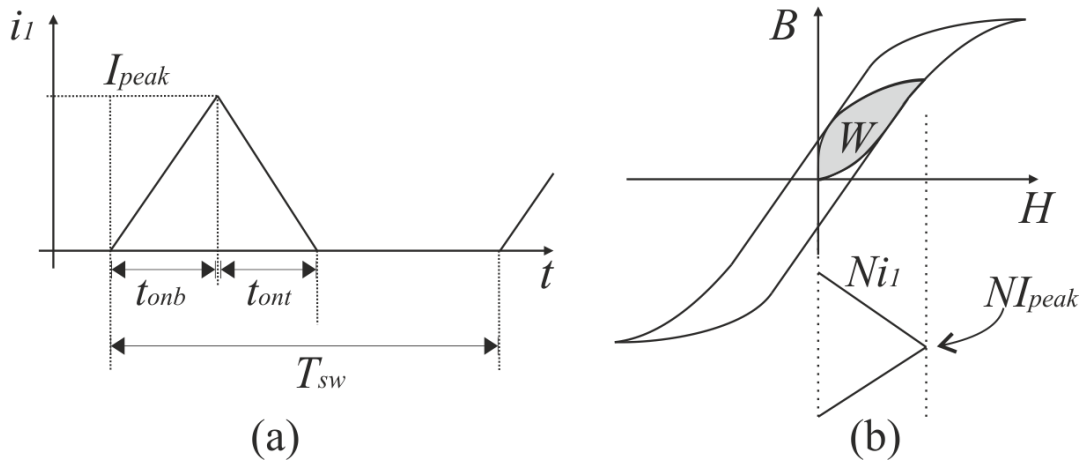


Figure 3-4. (a) Inductor current. (b) Inductor core hysteresis loop for one current pulse.

where V_c is the volume of the three equal sized inductors. The rms value of the inductor current shown in Figure 3-4(a) is given by $I_{prms} = I_{peak}\sqrt{(t_{onb} + t_{ont})f_{sw}/3}$. By using this expression, the copper losses of the three inductors can be represented as:

$$P_{cu} = R_{cu}{I_p}^2(t_{onb} + t_{ont})f_{sw} \tag{4}$$

3.4.2. Switching Devices Losses

In DCM operation, the bottom switches of the three boost stages in Figure 3-2 turn on under zero-current switching (ZCS) condition, and turn off under quasi zero-voltage switching (ZVS) condition because of the RC snubber circuits. By using the turn-off energy E_{off} provided in the technical datasheet of the devices[18], a conservative estimation of the switching losses can be obtained as follows:

$$P_{sw} = 3E_{off}f_{sw} \tag{5}$$

For a given cycle of pulsed current through the converter, the RMS value of the current in the bottom and top switches can be defined respectively as:

$$I_{gbrms} = I_p\sqrt{\frac{t_{onb}f_{sw}}{3}}\ ;\ I_{gtrms} = I_p\sqrt{\frac{t_{ont}f_{sw}}{3}} \tag{6}$$

By summing the currents in (6) and considering the resistance R_{ds} of the MOSFET when turned on, conduction losses for the switching devices can therefore be modeled as:

$$P_{cond} = R_{ds}{I_p}^2(t_{onb} + t_{ont})f_{sw} \tag{7}$$

3.4.3. Snubber Losses

Large dv/dt ringing during bottom MOSFET turn off due to the resonance between the boost inductor connected to the phase and the parasitic capacitance are mitigated by using the RC snubbers shown in Figure 3-2. The snubber capacitor C_s captures energy during the bottom switch turn off interval and dissipates this energy through the resistor R_s during the turn on interval. The power losses associated with the energy captured by the snubber is given by:

$$P_{sn} = 3C_s{V_o}^2 f_{sw} \tag{8}$$

Considering the sum of the main loss mechanisms in (3), (4), (5), (7) and (8), the total converter losses can be obtained as $P_{tot} = P_{core} + P_{cu} + P_{sw} + P_{cond} + P_{sn}$. Furthermore, the mean value of the converter input power can be expressed as $P_i = (3/2)V_i(t_{onb} + t_{ont})I_p f_{sw}$. Therefore, the converter efficiency can be calculated as:

$$\eta = 1 - \frac{V_c W + E_{off} + \frac{(R_{cu} + R_{ds}){I_p}^2(t_{onb} + t_{ont})}{3} + C_s{V_o}^2}{V_i(t_{onb} + t_{ont})I_p/2} \tag{9}$$

For a given input and output voltage, the system efficiency as based on (9) is independent of the switching frequency and the load current of the converter. Therefore, fairly constant efficiency can be achieved for the entire power range with the implementation of this control method.

3.5. Boost Converter Inductor Sizing

To ensure that the converter operates in DCM for all load values, the design point of consideration is specified for the nominal power ratings of the converter. At nominal power, the input current is at a state defined as maximum overlap, whereby all three phases are working just at the border of DCM at the maximum value of switching frequency. Because of the interleaving

action of all three phases, the input current experiences a reduced ripple when the three currents are summed. The minimum inductor peak current value required to ensure full-range DCM given this operating point can be calculated as:

$$I_{pmin} = \frac{2P_{nom}}{3V_{imin}} \tag{10}$$

where V_{imin} is the worse case scenario for V_i. In order to operate in such a scenario, at the desired maximum frequency of operation f_{swmax}, the inductors of the converter must be selected as:

$$L_b = \frac{V_{imin}(V_o - V_{imin})}{V_o I_{pmin} f_{swmax}} \tag{11}$$

3.6. Simulation Results

The proposed control strategy is simulated in MATLAB/Simulink™. The parameters of the simulated system are listed in Table 3-1, with the inductor sized based on (12). The red waveform shown in Figure 3-5(a) corresponds to the output voltage V_o when it is controlled by the strategy explained in Section 3.3 (see Figure 3-3), while the black line corresponds to the controlled output

Table 3-1: Prototype specifications

Variable	Parameter	Value
Pnom	Rated Power	10 kW
Vi	Battery Voltage	200 V
Vo	Bus Voltage	600 V
Lb	Inductance	80 μH
C	Capacitance	140 μF
I_p	Peak Current	33 A
f_{sw}	Switching Frequency	50 kHz
Kp	PI Proportional Coefficient	2
Ki	PI Integral Coefficient	200000

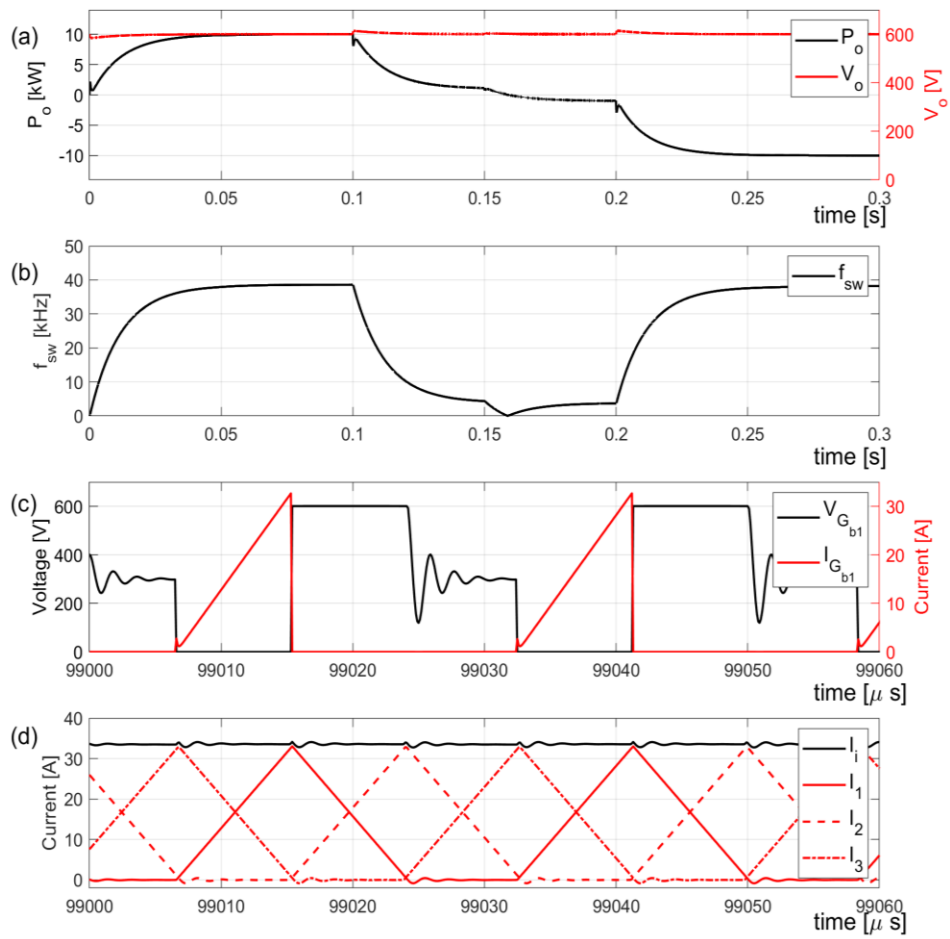


Figure 3-5. Simulation results: (a) P_o and V_o. (b) f_{sw}. (c) V_{Gb1} and I_{Gb1}. (c) I_i, I_1, I_2 and I_3.

power $P_o=V_oI_o$. The voltage reference is set to V_{on} $=600$ V, while the output current profile changes to test the controller dynamic response. Initially, the system delivers 10 kW from the battery to the load. At the instant t = 0.1 s the load is changed so the system delivers 1 kW from battery to the load. At the instant t $=0.15$ s, I_o is changed in such a way that 1 kW flow from the load to the battery. Finally, at t $=0.2$ s, I_o is changed in such a way 10 kW flows from the load to the battery. Figure 3-5(b) shows that the controlled switching frequency f_{sw} is changing in concordance with load requirement, decreasing when the power magnitude decrease and vice versa. The obtained simulation results in the voltage and current waveforms in Figure 3-4(c) confirm that soft-switching operation (ZCS turn-on) is achieved. The waveforms in Figure 3-5(d)

displays the three phase currents with a set peak current value of $I_p = 33\ A$. The total input current shown in black experiences a reduced ripple due to the overlapping phase currents.

3.7. Experimental Results

A boost converter with specifications listed in Table 3-1 is built to further validate the variable frequency DCM control method. A DSP board is utilized to implement the controller and generate the gate signals of the six MOSFETs. Wolfspeed's C2M0025120D 1200V 90A SiC MOSFETs are selected as the switching devices. Adequate snubber circuitry is used to damp oscillations produced between the inductors and MOSFET output capacitance. Figure 3-6 shows the constructed converter that is set to operate in two distinct modes while maintaining the same input-output specifications in order to compare the effectiveness of the proposed control method. Furthermore, ≈ 20 % (2.1 kW) of the 10-kW rating is selected to represent a low-power level in a drive schedule. The first mode utilizes the conventional DCM-PWM with f_{sw} ≈ 41 kHz for full range power operation. The waveforms for the converter are shown in Figure 3-7. For a peak

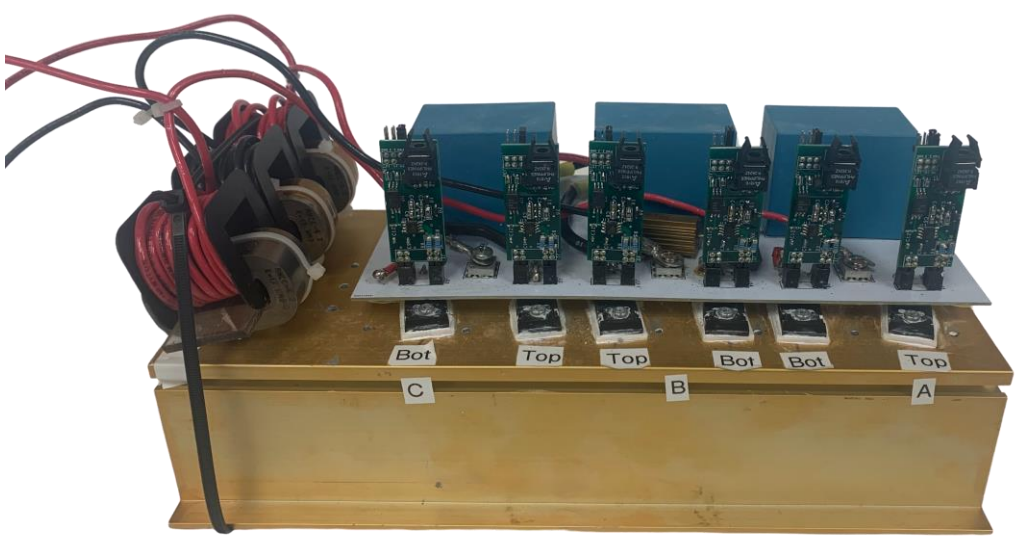


Figure 3-6. Prototyped 10-kW interleaved boost converter.

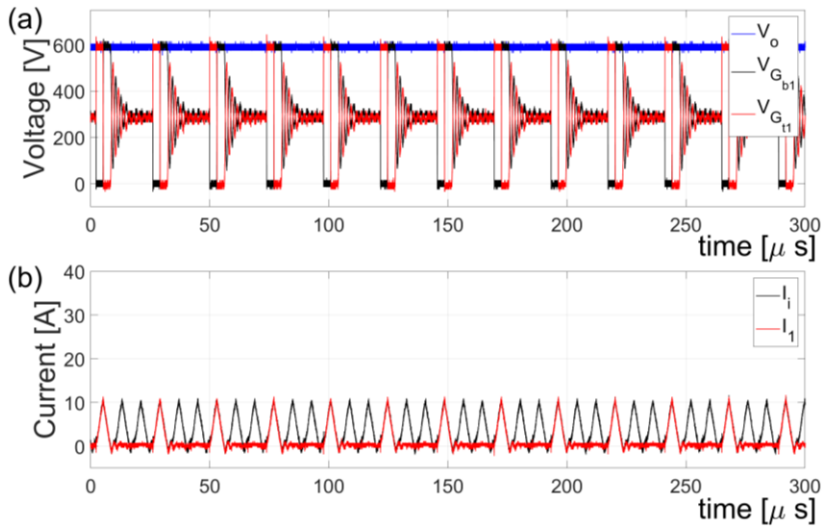


Figure 3-7. Conventional PWM: (a) V_o , V_{Gb1} and V_{Gt1}. (b) I_i and I_1

current of 10.85 A in this mode, an efficiency of 91.45 % was measured. The proposed control algorithm is used in the second mode. For the 2.1 kW load applied, the converter operates at f_{sw} = 3.3 kHz. The peak current was selected as $I_p = 33\ A$, based on the switching device's safe operating area from the MOSFET datasheet. The value of the converter inductances is designed following (12) in order to ensure full range DCM operation. Waveforms for the converter in this mode are presented in Figure 3-8. The voltage across the switch shows significantly less ringing

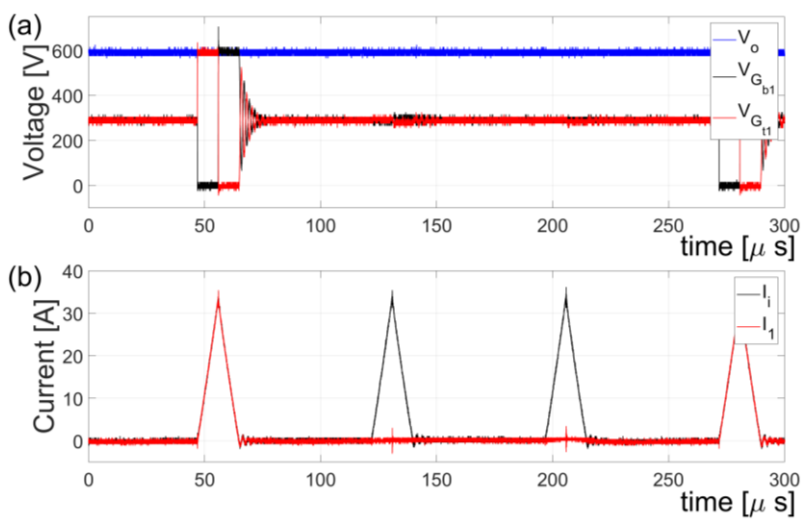
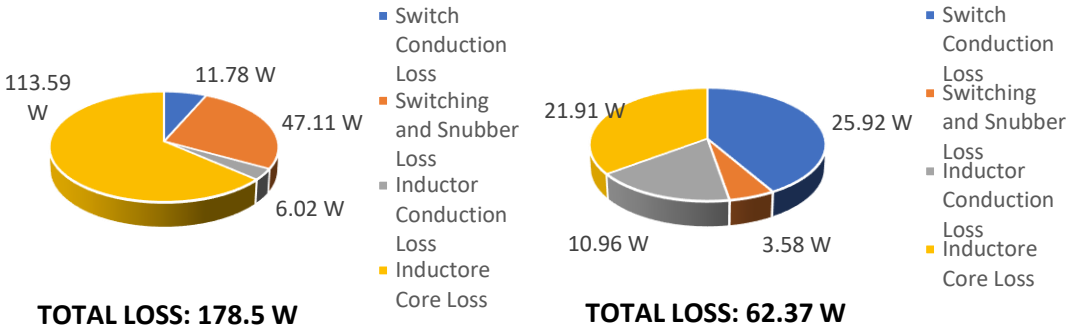


Figure 3-8. Variable-frequency control: (a) V_o , V_{Gb1} and V_{Gt1}. (b) I_i and I_1



(a) (b)

Figure 3-9. (a) Boost converter loss breakdown for cases with conventional PWM algorithm and (b) the proposed variable-frequency control algorithm.

than that observed in Figure 3-7(a) due to the reduced switching frequency. The measured efficiency at this operating point of 2.1 kW was 97 %. Using the loss mechanisms in (3), (4), (5), (6) and (7), Figure 3-9(a) and (b) display an approximate statistical breakdown of the losses obtained for both experimental operating modes. The variable-frequency control method displays a 27.4 % and 50 % reduction in both the inductor and switching and snubber losses, respectively. Despite operating with a higher peak current, the increase in conduction losses in the switches and inductors are marginal compared with the decrease in the other loss components. Figure 3-10 shows the efficiency comparison between the conventional and variable-frequency PWM control

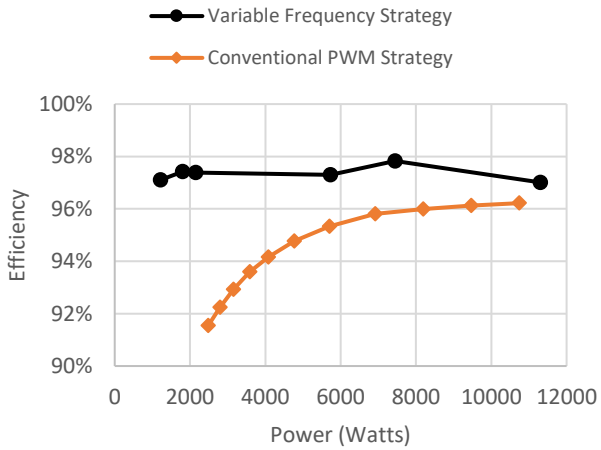


Figure 3-10. Converter efficiency comparison.

techniques. The proposed control strategy shows both an increase of efficiency at low power levels and a fairly constant efficiency over the entire power range compared to the conventional PWM control technique, satisfying the technological requirement presented.

3.8. Conclusions

A control method for increasing the efficiency at low power levels for a three-phase bidirectional interleaved boost converter typically used in automotive applications was proposed in this work. The control strategy consists of operating with a fixed inductor current peak while the converter switching frequency is varied over the entire power range. It has been analytically and experimentally demonstrated through efficiency throughout the entire operating range.

3.9. Acknowledgements

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3.10. References

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CHAPTER 4

INDUCTOR ENCAPSULATION-BASED THERMAL MANAGEMENT ENABLING INCREASED POWER DENSITY

4.1. Abstract

Inductors occupy significant volume in dc-dc converters where power density is an important figure of merit. This research work addresses an improved design of a power-dense nanocrystalline-based inductor employing potting materials with high thermal conductivity. Contrary to traditional inductor design methods which require larger volumes to accommodate for temperature rise limits, this work presents an analytical framework to decrease the inductor volume through encapsulation. Particularly, it analyzes the effectiveness of employing a hybrid potting material, through experimental investigation of various filler compositions as compared to the classical silicone gel-based materials. Experimental evidence verifying the theoretically designed method is presented in this work.

4.2. Introduction

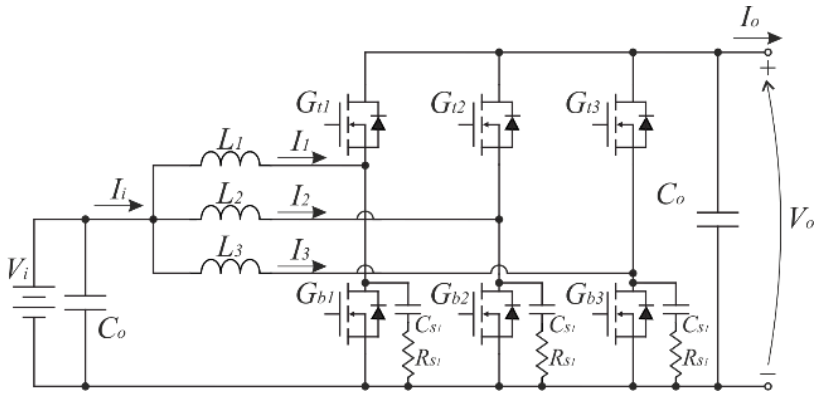
Increasing environmental concerns within the transportation industry has driven the development of more energy efficient and eco-friendly electric vehicles (EVs) [1]. In order to achieve the material cost benefits associated with the manufacturing of EVs, increasing system power density is a heavily pursued metric [2]. Within dc-dc converters, volumetric density is dependent upon the inductors which generally encompass a significant volume of the overall converter [3]. Therefore, considerable improvement to system power density can be attained through reducing the size of the inductors. Increasing the operating frequency of the switching

devices and therefore the inductors is a trend utilized in order to pursue magnetic component size reduction [4]. However, the designs for power dense inductors cannot be performed exclusively within the magnetic domain as higher frequency within inductors also realize more switching, hysteresis and eddy current losses [5]. Additionally, as the inductor size is reduced, dissipating the same (or more) power from a smaller surface area and volume yields an increase in temperature, limiting their reliability as proximity to Curie temperatures degrades the magnetic properties, along with degradation of winding insulation [6]. This work therefore presents a reduced inductor design based on encapsulation as a mitigating thermal approach for handling the associated increased temperature [7]. In encapsulation, the inductor is placed within an enclosure made of a high thermal conductivity material such as aluminum and a potting material to minimize the thermal resistance between heat sources and heat extraction surfaces. Inductors for a three-phase interleaved dc-dc boost converter operated in discontinuous conduction mode (DCM) are considered for the scope of this work. This paper is organized as follows: the inductor design method is presented in Section 4.3, the encapsulant analysis is done in Section 4.4 and the experimental results are analyzed in Section 4.5.

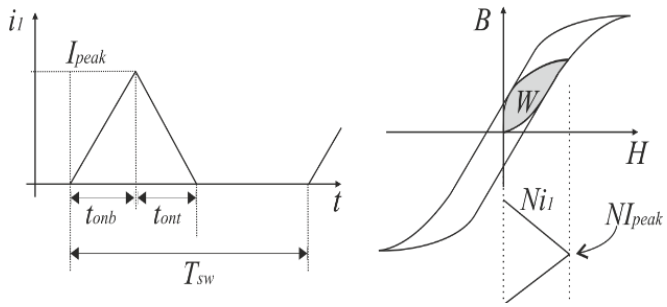
4.3. Inductor Design Consideration

4.3.1. Topology Description

Figure 4-1(a) shows the three-phase bidirectional interleaved boost converter circuit for which the design of the inductors L_1, L_2 *and* L_3, is addressed in this work. A voltage source V_i with a parallel filtering capacitor C_i, supplies the total input current I_i. Bottom switches G_{b1}, G_{b2}, and G_{b3}, and top switches G_{t1}, G_{t2}, and G_{t3}, respectively connect the three legs of the converter to the output capacitor C_o that filters the converter output voltage V_o applied to a load represented by the current source I_o. Fig 4-1(b) illustrates the DCM inductor current waveform in one of the inductors. The



(a)



(b)

Figure 4-1. Interleaved three-phase boost topology and (b) Inductor current waveform and hysteresis loop.

peak current I_{peak} generates the corresponding B-H curve with N number of turns. The area of the loop produced in the B-H curve reflects the total energy (loss) within the inductor.

4.3.2. Design Method

Nanocrystalline core material has great advantages in terms of losses and high flux density at high frequencies when compared to ferrite-based cores [8]. The design methodology presented for E-type cores in [9] for a medium frequency transformer is customized, whereby an optimum selection of the core thickness D and N number of turns of the inductor can be selected as to determine the inductor loss and magnetic characteristics, to meet a temperature rise and volume design criteria. One such magnetic property is the inductance L, defined as $L = \mu_o D^2 N^2 / 2 l_g$, where μ_o is the permeability of air and l_g the airgap length. The temperature rise is determined by

the total copper and core losses of the inductor The magnetization of the inductor produces a DCM triangular flux density waveform according to the current in Fig. 1(b), with a peak $B_m = NI_{peak}\mu_o/l_g$. Core losses associated with hysteresis and eddy current phenomena are estimated by applying the Improved Generalized Steinmetz equation [10]–[12] to a piecewise decomposition of the flux density waveform:

$$P_c = \frac{V_c K_i}{T}\int_0^T \left|\frac{dB}{dt}\right|^{\alpha} |\Delta B|^{\beta-\alpha}\, dt = K_i f_{sw} {B_m}^{\beta}({t_{onb}}^{1-\alpha} + {t_{ont}}^{1-\alpha}) \quad with \quad k_i = \frac{2^{(\alpha+1)}K_c}{\pi^{(\alpha-1)}\left(1.1044 + \frac{6.8244}{\alpha + 1.354}\right)} \tag{1}$$

where α, β and Kc are the core Steinmetz coefficients. Summing the core losses and copper losses produces total losses P_T:

$$P_T = \left(K_i f_{sw}\left[{B_m}^{\beta}\left({t_{onb}}^{1-\beta} + (t_{ont} - t_{onb})^{1-\alpha}\right)\right]\right) + P_{cu} \tag{2}$$

where P_{cu} is the wire AC resistance related conduction losses.

4.3.3. Wire Size Selection

At high operating frequencies, Litz wire is used in this work to reduce skin and proximity effects related losses [13]. The required cross-sectional area of the individual strands A_{litz} is determined by the maximum switching frequency [14]. For a J_{max} current density, the required overall area of the inductor wire is $A_{wire} = I_{rms}/J_{max}$. Considering a fill factor ∂ that encompasses the insulation, the required number of strands for the wire are $N_{strands} = A_{wire}/A_{litz}\partial$.

4.3.4. Core Geometry

The inductor core geometry displayed in Figure 4-2 has six variables that are all related to the selected wire dimensions, N and D. The relationship between these parameters is determined by the manufacturer capabilities. The core window height and width are expressed as $F = C_{extra} + D_{wire}$ and $G = ND_{wire} + C_{extra}$, respectively, where C_{extra} is a coefficient for extra space for the

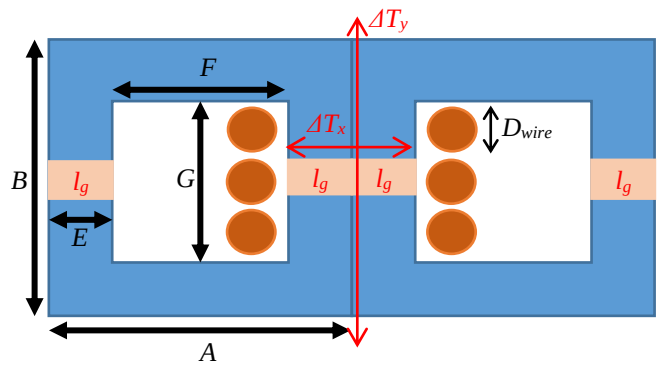


Figure 4-2. Inductor dimensions.

inductor bobbin and wire insulation and D_{wire} the wire overall diameter. The core width A is set equal to the cooling platform, thus allowing for the derivation of the remaining parameters: core thickness $E = (A - F)/2$ and core height $B = G + 2E$. The cross-sectional area is $A_c = 2ED$. The mean path length $MPL = 2(F + G) + FE$ produces an overall core volume $V_t = 2A_c MPL$.

4.3.5. Thermal Model

An averaged thermal circuit equivalent of the inductor as per [15] is used to estimate the temperature rise ΔT. The horizontal and vertical components of temperature rise ΔT_y and ΔT_x are averaged about the core center to represent the highest inductor temperature $\overline{\Delta T}$. Their expressions are as follows:

$$\Delta T_y = 0.5P_T\left(\frac{0.25E}{k_{core}EB} + \frac{0.5t_{pot}}{k_{pot}EB}\right) + T_c \tag{3}$$

$$\Delta T_x = P_c\left(\frac{0.25E}{k_{core}EF}\right) + P_T\left(\frac{D_p}{0.5k_{cu}EF}\right) + T_c \tag{4}$$

$$\overline{\Delta T} = 0.5(\Delta T_y + \Delta T_x) \tag{5}$$

where k_{core} , k_{pot} and k_{pot} are the thermal conductivities of the core, copper wire and potting material, respectively, t_{pot} the thickness of the potting material and T_c the cold plate temperature.

4.3.6. Inductor Design Selection

A thermal-volume co-optimization procedure is conducted through sweeping the core thickness D for varying N. For every inductor geometry generated with the unit increase in the parameter, corresponding ΔT, V_t total volume, and P_T profiles are produced as illustrated in Figure 4-3. From the minimization of the cost function of $\Delta T V_t$ shown in Figure 4-3, the corresponding N and D are selected to then define the core geometry. To verify the design integrity and non-saturation, B_m is also considered in the selection. The cost function has a global minimum for $N = 5$ and $D \approx 25\ mm$, so they are selected for the inductor design.

4.4. Encapsulant Analysis

In [16], epoxy based encapsulant has been investigated for use in encapsulation which generally possess a thermal conductivity of 1-2 W/mK, representing a 100x improvement of the thermal conductivity compared to air (0.02 W/mK). Filler particles of high thermal conductivity (> 100 W/mK) can be added in different concentrations to yield incremental improvements to the bulk encapsulant thermal conductivity. Using the radial heat flow method [17], [18], the temperature

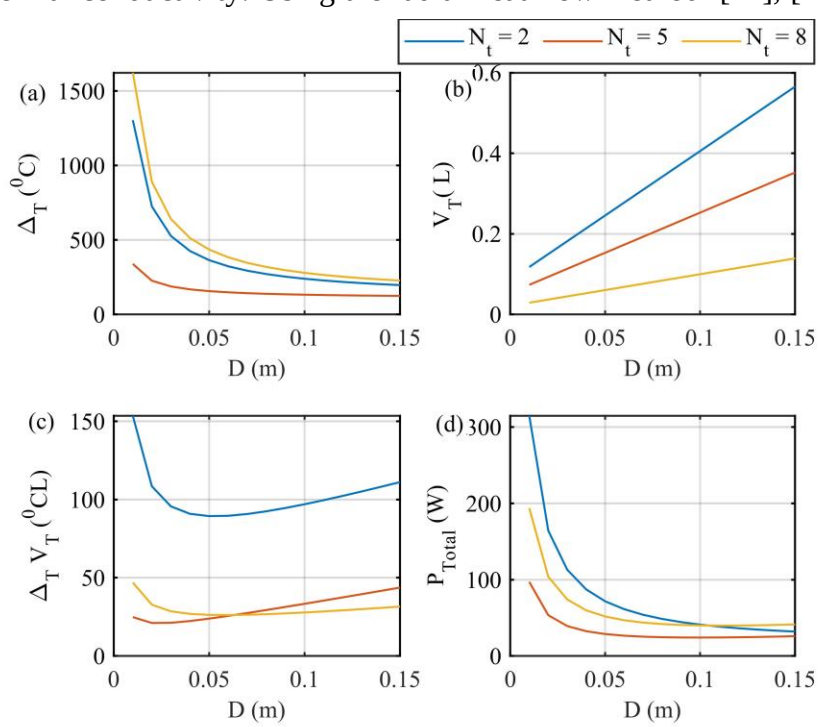


Figure 4-3. Design optimization and selection

reduction as related to the thermal conductivity of the different bulk encapsulants listed in Table 4-1 can be empirically experimentally deduced. Aluminum nitride (AlN) was mixed as a filler material in various mass ratios to a 10 W/mK thermal putty. Figure 4-4 shows the resultant temperatures of the heating element obtained from the radial flow method according to the different encapsulants being considered. The heat transfer achieved with air produces an internal temperature of 163 °C. However, the best temperature reduction occurs with the use of the 10 W/mK rated potty, which boasts the lowest steady state temperature of 45 °C; a reduction of almost 73 %. The various filler compositions that were tested show reduction in the internal temperature but they are than that of the putty itself. Their reductions are between 32 % and 61% approximately. These results can be attributed to the small-grain uneven particle surface of the AlN interacting with the highly viscous putty. The irregularities in the geometry of both substances

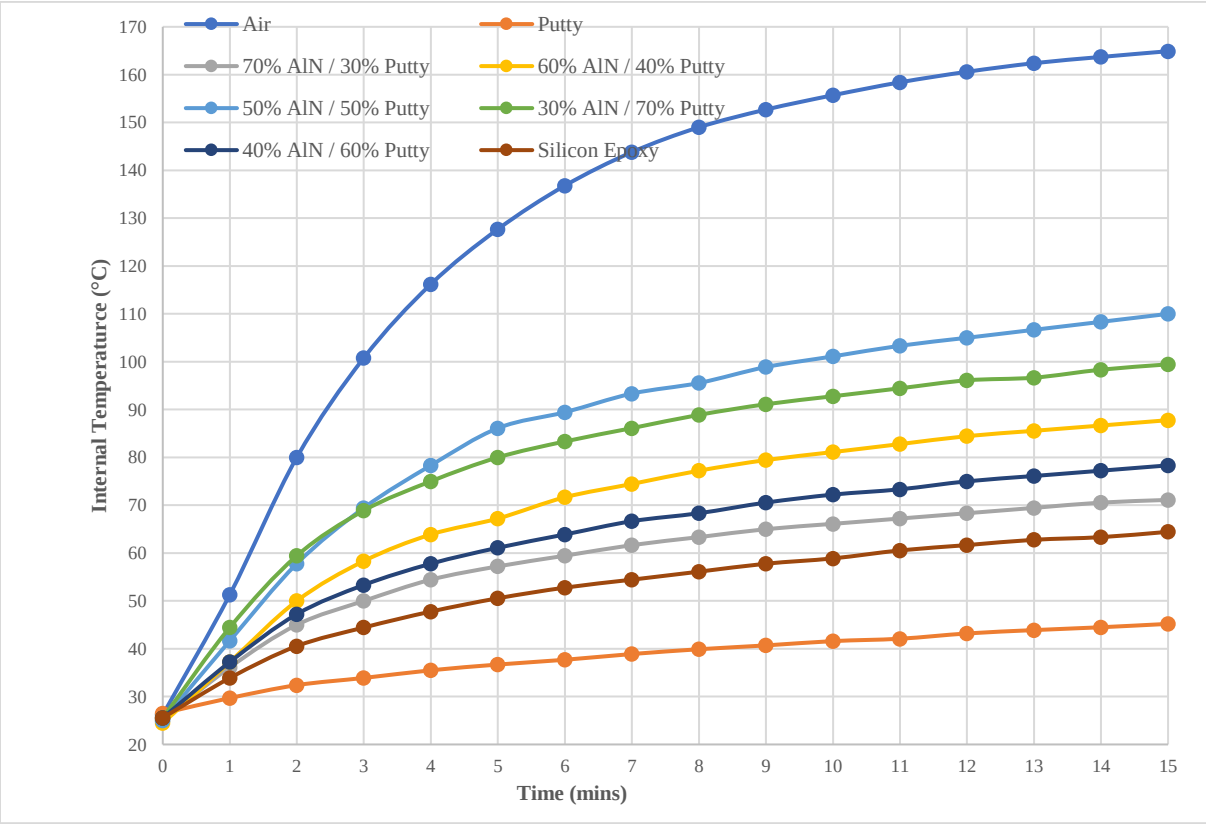


Figure 4-4. Radial heat flow temperature results

Table 4-1: Inductor Specifications

Parameter	Value
I_{peak}	250 A
N	5
f_{sw}	*50 kHz*
B_m	0.56 T
I_{rms}	88 A
J_{max}	3 A/mm^2
k	10 W/mK
L	12 µH

on an atomic scale leads to a non-tessellation of the bulk compound. It is hypothesized that using a larger grain sized AlN would achieve tessellation with the putty thus synthesizing a higher thermal conductivity bulk compound.

4.5. Experimental Results

Identical inductor sets shown in Figure 4-5 with specifications listed in Table 4-1 are designed in this section using the theoretical design in Section 4.3, with an optimum value for N and D iteratively solved for to minimize ΔT and total volume. One inductor set was enclosed in an aluminum enclosure in air, while the other inductor was potted using a 10 W/mK putty. Using the

Figure 4-5. Designed inductors.

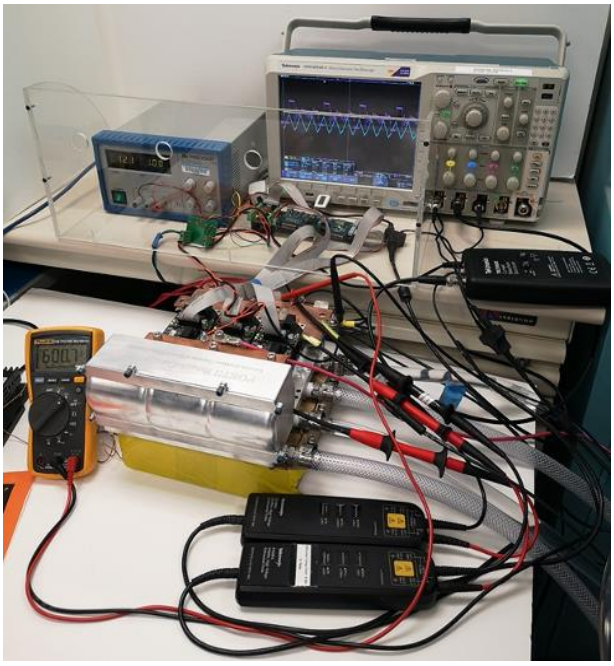


Figure 4-6. Experimental setup.

experimental setup in Figure 4-6 with an interleaved boost converter, both inductors were subject to duplicate testing conditions. Figure 4-7 shows that a ≈ 50% temperature reduction is achieved from the potted inductor, with a maximum temperature of 42 °C being achieved as opposed to 92.7 °C in the unpotted inductor.

4.6. Conclusions

Techniques for mitigating high temperature within power dense inductors design based on encapsulation and etching were proposed and experimentally verified. Initial experimental results gathered from the encapsulant indicated a thermal conductivity of 10 W/mK, capable of reducing the inductor temperature by ≈ 50 %. Because of the enhanced thermal pathway incorporated into the inductor design method enabled through encapsulation, there is flexibility in the final inductor output dependent upon the overall design objective. Utilizing the same requirement of allowable ΔT for the specifications in Table 4-1, it is possible through the extension of the design methodology proposed in this paper to design an inductor with a higher power density. However,

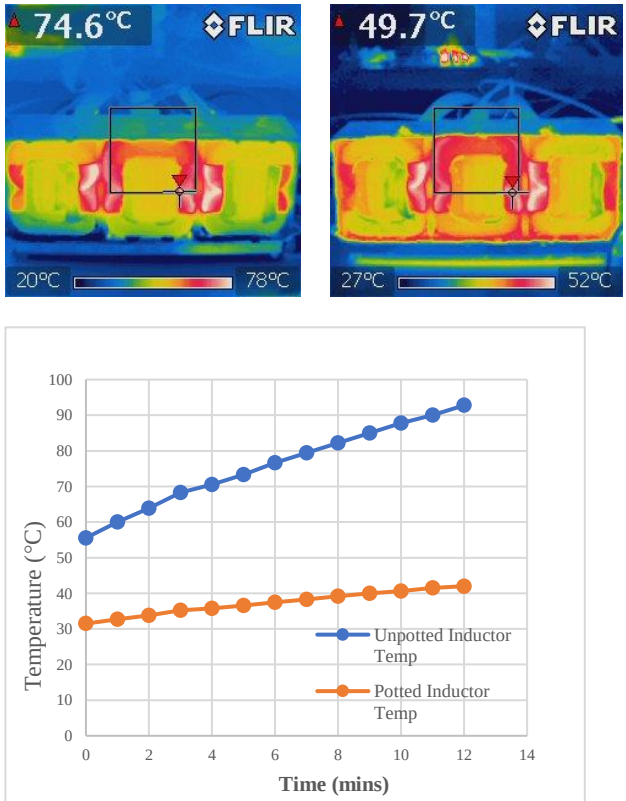


Figure 4-7. Thermal camera images and resultant temperature profiles.

the drawbacks associated with this is an increased heat flux which is associated with long term system reliability. If ambient air is considered as encapsulant material for within the methodology for the same ΔT objective, the volume obtained in the final design is 28% more than that obtained with the encapsulant.

4.7. Acknowledgements

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CHAPTER 5

COMPREHENSIVE DC-DC CONVERTER DESIGN METHODOLOGY

5.1. Abstract

High system efficiency at all power levels is desired for electric vehicle (EV) propulsion systems. Conventional boost converters employed in EV traction architectures exhibit significantly lower efficiencies at low power levels when operated under traditional fixed-frequency pulse-width modulation (PWM) techniques. Also, low system power densities are associated with conventional boost converters due to their bulky inductors. These two shortcomings are addressed here through a comprehensive design methodology for an 80-kW interleaved boost converter stepping a low battery voltage up to an 800-V DC link. The designed converter employs a discontinuous conduction mode (DCM) variable-frequency control strategy to achieve an efficiency increase at low power levels, and thus, a constant efficiency throughout the entire drive schedule. A system loss model is developed to decompose analytically the loss mechanisms, and thus, determine the optimized design parameters for the variable-frequency control strategy and converter magnetics. Moreover, a custom inductor design based on distributed airgaps and aggressive thermal management through potting is integrated into the design methodology to further increase the converter power density. An 80-kW prototype is fabricated achieving a total power density of 55.6 kW/L, and experimentally tested, yielding system efficiencies above 96% for all power levels.

5.2. Introduction

Growing environmental concerns due to increased greenhouse gas emission from fossil fuel consumption within transportation has driven the development of more energy efficient and eco-friendly electric vehicles (EVs) [1]–[3]. Paramount to realizing the material cost benefits associated with the manufacturing of EVs is increased power density of the powertrain architecture along with increased full range efficiency to improve battery utilization [4]. Generally, the EV architecture based on power electronics that constitute the powertrain is realized in two configurations [5], [6]. The first configuration has the battery connected directly to the inverter while the second one has a bidirectional DC-DC converter (typically a boost converter) interfacing the battery and inverter. The advantages that arise out of the latter architecture are due to the possibility of independently designing and optimizing the electric motor and battery, respectively. Also, a battery pack consisting of less cells in series (lower voltage) can synthesize volumetric and material cost savings for manufacturers [7].

However, the benefits arising from having an interfacing DC-DC converter are dependent upon its efficiency over the entire power range of any EV driving schedule. As an example, Figure 5-1 illustrates the battery power consumption over the US06 driving schedule. The most frequent instantaneous power levels are below 50% of the system rating. Hence, a design challenge for EV DC-DC converters is increasing their efficiency for low power levels. Fixed-frequency PWM control strategies are typically employed in boost converters [8]. They exhibit drastically reduced efficiencies at low power levels, even when no power is being transferred to the load due to high switching losses associated with their continuous conduction mode (CCM) operation. DCM mode alternatively, allows for zero current switching (ZCS) of the on-time for the switching devices, and thus reduces losses; especially at low-power as the switching related losses are reduced proportionally to the load [9], [10]. DCM also allows for a reduced inductor volume, increasing

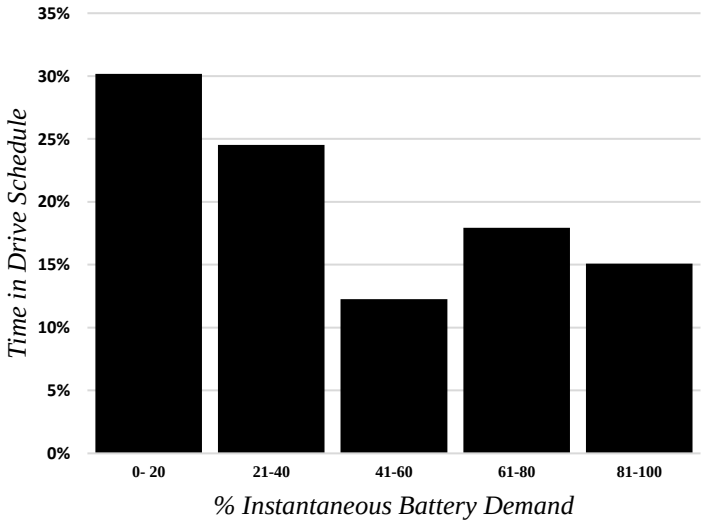

Figure 5-1. Normalized battery demand versus operating time in the US06 driving schedule.

the power density of the converter [11] with negligible effects [12]. Variable-frequency control strategies have been explored in literature [9], [10], [13], [14],for high efficiency at low power levels. The large current peaks associated with these techniques limit the application of these strategies to lower power applications [13], [15] as the switching devices are not capable of operating with increased conduction losses. However, with the advent of wide bandgap devices, particularly SiC, MOSFET devices are now able to operate with very large current peaks with low resistance, making feasible DCM variable frequency control strategies for high power[16]–[18].

Volumetric density within DC-DC converters hinges upon the inductors which generally encompasses a significant volume of the overall converter [19], [20]. Considerable improvement to system power density can be attained by reducing their sizes. Increasing the operating frequency is utilized to pursue magnetic component size reductions [20], [21]. However, power dense inductor designs cannot be performed solely within the magnetic domain as higher frequencies also realize more hysteresis and eddy current losses [22]. As the inductor size is reduced, dissipating the same (or more) power from a smaller surface area yields an increase in temperature,

limiting their effectiveness as proximity to Curie temperatures degrades not only the magnetic properties bus also the winding insulation [23]. Therefore, thermal management becomes an important aspect of consideration. Mitigation of the associated temperature rise with reduced inductor volume is achieved through encapsulation [24].

Reference [25] proposed inserting heat spreaders in the airgaps to remove the heat produced by eddy current losses in nanocrystalline cores. However, this does not address the heat source itself which is due to the circulating eddy currents in the core cross-sectional area. The airgap losses within ribbon-based cores are due to the short-circuited laminations in the manufacturing process [26]. A relatively safe procedure of ferric chloride etching of the short-circuited surface is presented in [26]; however, it was reported that the benefits are short-lived due to a reduced quality of the core over time. The enhanced etching procedure in this paper is applicable to nanocrystalline cores and includes a neutralization process mitigating aging effects which by extension minimizes losses and airgap temperature.

In summary, this paper presents a comprehensive design methodology for an 80-kW interleaved bidirectional boost converter for increasing the low-power level efficiency while also increasing system volumetric power density for automotive applications, through the implementation of a DCM variable-frequency control strategy. The converter design is detailed in Section 5.3. The inductor design procedure for reduced volumetric footprint and integrated thermal management considerations, together with the effective core etching method to reduce eddy current losses on ribbon-based cores are given in Section 5.4. The converter loss assessment is described in Section

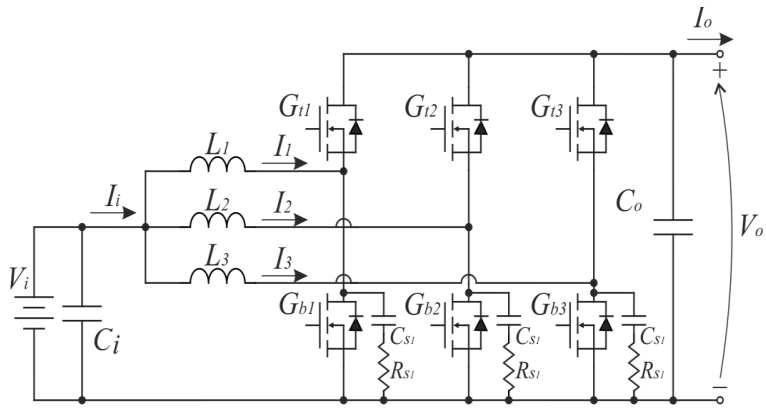

Figure 5-2. Circuit configuration of the interleaved boost DC-DC converter.

5.5 followed by the thermal design in Section 5.6 and the converter implementation and simulation results in Section 5.7.

5.3. System Design Methodology

5.3.1. Converter Topology and Control Strategy

The bidirectional three-phase interleaved boost converter circuit is shown in Figure 5-2. The input stage represents a battery bank of voltage V_i with a parallel filtering capacitor C_i, which supplies the total input current I_i to boost inductors L_1, L_2 and L_3, corresponding to the three boost stages composed of the bottom switches G_{b1}, G_{b2}, and G_{b3}, and top switches G_{t1}, G_{t2}, and G_{t3}, respectively. The three boost phases are connected to the output capacitor C_o filtering the output voltage V_o applied to a load represented by current I_o. Figure 5-3 also illustrates the block diagram representation of the proposed DCM control strategy. The measured output voltage V_o is compared to a specified reference voltage V_{or}. The error is then applied to a proportional-integral (PI) controller whose output generates the magnitude value of the switching frequency f_{sw}. Three sawtooth carriers T_1, T_2 and T_3, of frequency f_{sw} are then generated delayed by $1/3f_{sw}$. The output of the PI controller will be positive if $V_{or} > V_o$, so the signal S will be zero. In this condition, the

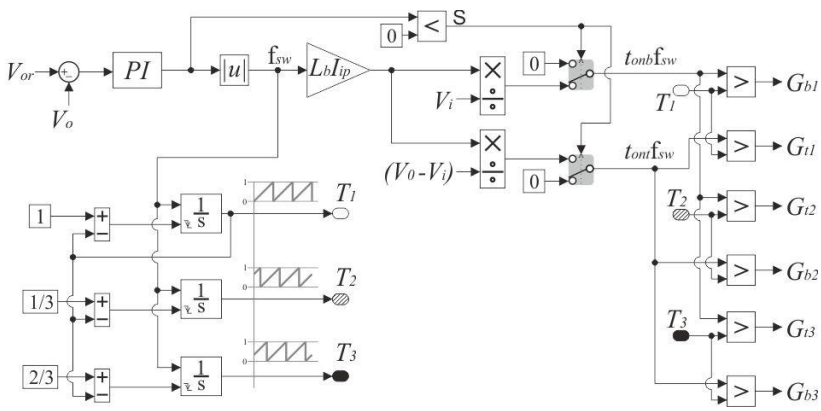

Figure 5-3. Variable-frequency DCM control strategy for the DC-DC converter.

system delivers power to the output under boost mode operation, being the gate signals G_{t1}, G_{t2}, and G_{t3} equal to zero. The average output voltage for a given cycle of the boost converter operation is defined as follows:

$$V_o = \frac{1}{2} L I_{peak}{}^2 \frac{f_{sw}}{I_o} + V_i \,, \tag{1}$$

where I_{peak} is the peak inductor current. From (1) the switching frequency should be increased or decreased according to I_o to control V_o. The control strategy dictates that for a given input voltage, a finite amount of energy is stored in the inductor due to a constant-on time and meets the demanded power according to the switching frequency (*Power = Energy x* $\cdot f_{sw}$). The inductor is then sized considering the maximum power rating, output voltage and minimum input voltage to be on the border of Continuous Conduction Mode (CCM) and DCM to ensure that at reduced loads (i.e., reduced switching frequency), the system maintains DCM mode and ZCS operation.

5.3.2. Inductor Sizing

The inductors are sized to maintain DCM operation under all power levels. The required inductance is defined by considering the nominal power rating, P_{nom} since the variable-frequency DCM control strategy [27] stipulates that the switching frequency is at its maximum (f_{swmax}) at nominal power, P_{nom}, and maintains DCM for all lower power levels experienced. The input

current is at maximum overlap in that all three phases of the boost are working at the point of DCM and CCM. The interleaving action causes a reduced resultant ripple in the input and output currents [28]. The I_{peak} required to ensure the full DCM for the entire converter power range can then be calculated by:

$$I_{peak} = \frac{2P_{nom}}{3V_{imin}}, \tag{2}$$

where V_{imin} is the minimum input voltage; then, L at the maximum switching frequency f_{swmax} to ensure DCM throughout the full converter operation range is given by:

$$L \leq \frac{3{V_{imin}}^2(V_o - V_{imin})}{2V_o\, P_o\, f_{swmax}}. \tag{3}$$

5.3.3. Capacitor Sizing

The output capacitor must achieve a desired voltage ripple while handling the maximum rms current when operating the converter at rated power. Based on the ripple voltage requirement ΔV_o, the minimum required capacitance is calculated as:

$$C_{min} \geq \frac{P_{nom}}{V_{omax} 3 f_{swmax} \Delta V_o} \tag{4}$$

and the rms current rating of the capacitor is:

$$I_{caprms} = \max\left(\sqrt{3(I_{trms})^2 - (I_o)^2}\right), \tag{5}$$

where I_{trms} is the rms current of the top switch.

5.3.4. Switching Frequency Selection

For an automotive application, it is desirable for the effective switching frequency ($3f_{sw}$) of the converter to be outside the human audible range (≈ 20 kHz). The minimum switching frequency f_{swmin} is therefore selected with this consideration. The maximum value f_{swmax} is selected based on the gate driver power supply capacity at the maximum operating temperature of the converter [29].

5.4. Inductor Design Procedure

A magnetic design method based on the optimization of a predetermined core geometry relationship and custom wire sizes was proposed in [30] to best accomplish volume and temperature design metrics based on convection cooling. Taking advantage of the liquid cooling loop within HEVs/EVs, volumetric reductions of the inductor are possible by attaching them to the same cold plate having the power modules [31]. Encapsulating the inductors increases the surface area removing the generated heat, and thus, reduces the thermal resistance to the cold plate enabling further volumetric reductions. This section therefore proposes an improvement in the design method in [30] by considering a lumped thermal resistance model of the inductor based on encapsulation to realize power density and efficiency objectives.

The optimization consists of sweeping the core depth D and inductor number of turns N_t determining the custom physical geometry, magnetic properties, and associated losses. The best fit design solution defined by the volume and losses is then selected. C-type cores are considered for ease of design and fabrication. A distributed airgap design is considered for reducing fringing flux related losses [32].

5.4.1. Wire Sizing

The first step is selecting a suitable winding wire. At high frequencies, Litz wire is used to mitigate skin and proximity effects related losses [33]. The required cross-sectional area of the individual strands A_{litz} is determined by the maximum switching frequency [34] to approximate the AC resistance of the wire to the DC resistance as per [35]. The resistance of the winding is measured with an LCR meter at the maximum switching frequency for loss calculation. For a J_{max} current density (constrained to 3 A/mm^2 to consider volume and insulation deterioration due to temperature rise [36]), the required overall area of the inductor wire is $A_{wire} = I_{rms} J_{max}$.

Considering a fill factor ∂ that encompasses the insulation, the required number of strands for the wire are $N_{strands} = A_{wire}/A_{litz}\partial$.

5.4.2. Core Material Selection and Geometry

As per the high peak current required for the proposed control strategy and high switching frequency, a magnetic core material with high saturation flux density is required to avoid saturation and excess losses. Nanocrystalline material is chosen due to its high saturation flux density and advantages at high frequencies [37], [38]. The inductor core geometry displayed in Figure 5-4 has six parameters that are all related to the selected wire dimensions, N_t and D. The relationship between these parameters are determined by the manufacturer capabilities. The core window height and width are expressed as $F = C_{extra} + D_{wire}$ and $G = N_t D_{wire} + C_{extra}$, respectively, where C_{extra} is a coefficient for extra space for the inductor bobbin and wire insulation and D_{wire} the wire overall diameter. The core width A is fixed to half the size of the cold plate reservoir to utilize maximum space. The remaining parameters are as follows: core thickness $E = (A - F)/2$ and core height $B = G + 2E$. The cross-sectional area is defined as $A_c = 2ED$. The mean path length $MPL = 2(F + G) + FE$ produces an overall core volume $V_c = 2A_c MPL$

5.5. Airgap and Flux Density

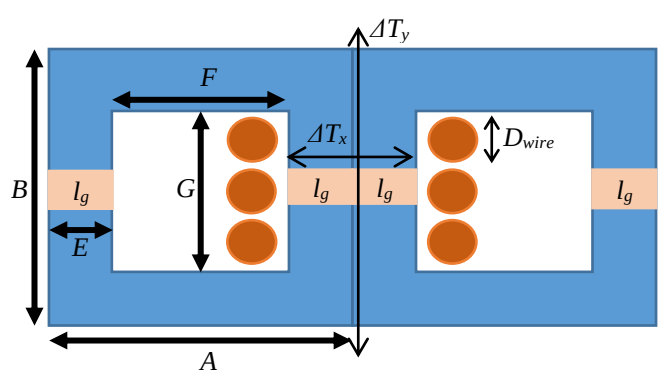

Figure 5-4. Inductor dimensions.

As the reluctance of air is far greater than the reluctance of the core, the assumption is made that all the energy in the inductor is stored in the airgap [39]. Per the required inductance in (3) to satisfy DCM operation, the airgap can be approximated as:

$$l_g \approx \frac{\mu_o A_c {N_t}^2}{L}, \tag{6}$$

where μ_o is the vacuum permeability. Then, the maximum flux density, B_m, using:

$$B_m = \frac{\mu_o N_t I_{peak}}{L}, \tag{7}$$

that is constrained to be less than the saturation flux density of the core material, B_{sat}.

5.5.1. Inductor Losses

Core losses due to hysteresis and eddy current phenomena are estimated per the Improved Generalized Steinmetz equation [39]–[41] using a piecewise decomposition of the flux density waveform yielding:

$$P_c = \frac{3V_c K_i}{T}\int_0^T \left|\frac{dB}{dt}\right|^{\alpha} |\Delta B|^{\beta-\alpha}\, dt = K_i f_{sw} {B_m}^{\beta}\left({t_{onb}}^{1-\alpha} + {t_{ont}}^{1-\alpha}\right) \tag{8}$$

$$P_c = 3V_c K_i f_{sw}\left[\left(\frac{\mu_o N_t I_{peak}}{L}\right)^{\beta}\left({t_{onb}}^{1-\beta} + (t_{ont} - t_{onb})^{1-\alpha}\right)\right] \tag{9}$$

$$with \quad K_i = \frac{2^{(\alpha+1)} K_c}{\pi^{(\alpha-1)}\left(1.1044 + \frac{6.8244}{\alpha + 1.354}\right)}$$

where α, β and K_c are the Steinmetz coefficients of the core material. The conduction losses within the inductor windings of resistance R_{cu} for a current $I_{prms} = I_{peak}\sqrt{(t_{onb} + t_{ont}) f_{sw}/3}$ are given by:

$$P_{cu} = 3R_{cu}{I_{prms}}^2 \tag{10}$$

The total inductor loss is then given by $P_{ind} = P_c + P_{cu}$.

5.5.2. Inductor Temperature Rise

A lumped thermal circuit equivalent of the inductor is developed per [42] to estimate the temperature rise ΔT. The horizontal and vertical components ΔT_y and ΔT_x as shown in Figure 5-4 are averaged about the center of the inductor to represent the highest inductor temperature $\overline{\Delta T}$. Their expressions are as follows:

$$\Delta T_y = 0.5P_c\left(\frac{0.25E}{k_{core}EB} + \frac{0.5t_{pot}}{k_{pot}EB}\right) + T_c \tag{11}$$

$$\Delta T_x = P_c\left(\frac{0.25E}{k_{core}EF}\right) + P_{cu}\left(\frac{D_{wire}}{0.5k_{litz}EF}\right) + T_c \tag{12}$$

$$\overline{\Delta T}(f_{sw}, I_{peak}, T_c) = 0.5(\Delta T_y + \Delta T_x) \tag{13}$$

where k_{core} , k_{litz} and k_{pot} are the thermal conductivities of the core, copper wire and potting material, respectively, t_{pot} the thickness of the potting material and T_c the cold plate coolant temperature.

5.5.3. Inductor Design Selection

With design specifications of high-power density and efficiency, a thermal-volume co-optimization procedure is conducted through sweeping the core thickness D for different N_t. For every inductor geometry generated with the increment in the parameter, corresponding ΔT, V_t and P_{total} profiles are produced as illustrated in Figure 5-5. From the minimization of the cost function of $[\Delta T V_t]$ shown in Figure 5-5, the corresponding N_t and D are selected to then define the core geometry. To verify the design integrity and non-saturation, B_m is considered in the selection. The final ΔT obtained is also checked to ensure that the design is limited to the rated operating

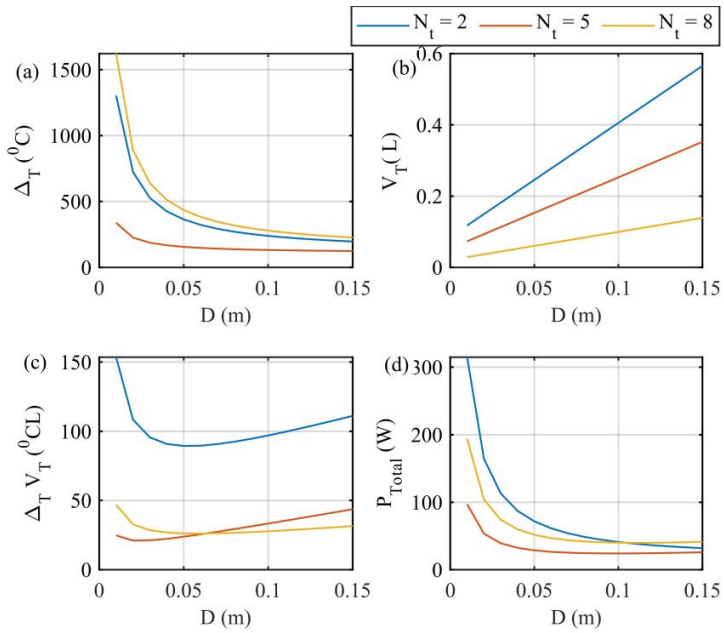

Figure 5-5. Design optimization and selection.

temperature of the core, T_{lim} given by the core material datasheet. The cost function has a global minimum for $N_t = 5$ and $D \approx 25\ mm$, so they are selected for the inductor design.

5.5.4. Core Etching Method

Industrial cutting techniques of tape wound cores produce C-core/E-core structures in inductors and transformers involving two generally utilized processes: metal saw cutting and electrical discharge machining (EDM) [43]. Both methods cause the lamination sheets to cross domains and come in contact beyond the layers of epoxy that typically separate them. This *short-circuit* phenomenon causes eddy currents to circulate between the laminations, increasing core losses and temperature in the cut cross section. A method proposed in [26] utilizes 40 % $FeCl_3$ to etch the fused surface of the core to mitigate this problem. However, a significant hindrance in the process is the inter-lamination oxidation that occurs over time that worsens achieved improvement. To address this problem, an additional neutralization step is added here to stop the etch process and remove oxidization elements. By using sodium bicarbonate ($NaHCO_3$) and Isopropyl Alcohol

(IPA) instead of water, the acid can be neutralized and the resultant water and salt that forms through interaction of the acid and base (cause of oxidation) is flushed. The method steps are now as follows:

1. Lightly sand the core cross section to remove surface oxidation.
2. Rinse the cores with IPA and air dry them to remove any metallic sediments.
3. Immerse the cores in $FeCl_3$ on a level mounted platform to start the etching. The level mounting ensures an equally distributed etch at an equal rate across the entire surface.
4. After 14 hours of etching, immediately remove the cores from the acid and remove surface acid only with deionized water.
5. Flush the surface water with IPA and dry with nitrogen.
6. Dump the cores in $NaHCO_3$ to complete the neutralization process.
7. Remove the sodium bicarbonate with an IPA rinse and dry the cores with nitrogen.

Figure 5-6 shows microscopic images of the cross-sectional area of a nanocrystalline core subject to the proposed etching procedure. Before the etching procedure, a uniform surface can be observed with few distinct laminations being visible due to an overlap of metallic regions over the insulating epoxy. However, after the etch, the layers of epoxy between each lamination can now be seen alongside every lamination. Figure 5-7 further validates the etch physically with a 5μm increase in the surface profile roughness vertically after the process.

5.6. Converter Loss Assessment

Pertinent to realizing the efficiency advantages of the intended control strategy and thermal architecture, a component-by-component theoretical loss analysis is performed. Each loss component analysis is done under the assumption of a worst-case scenario of converter operation, i.e., maximum power, output voltage, coolant and junction temperatures. The respective switching

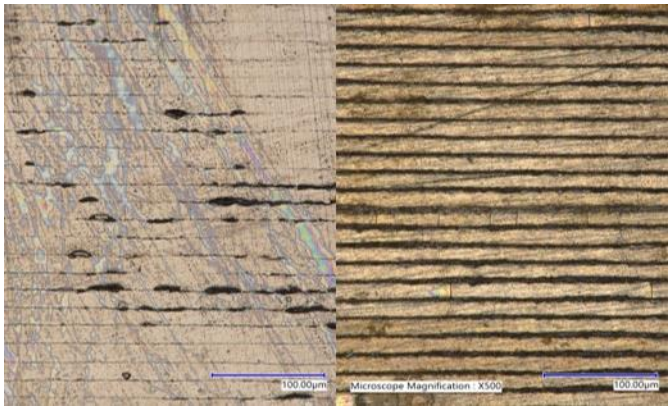

Figure 5-6. Comparison of core cross sectional area before and after etching.

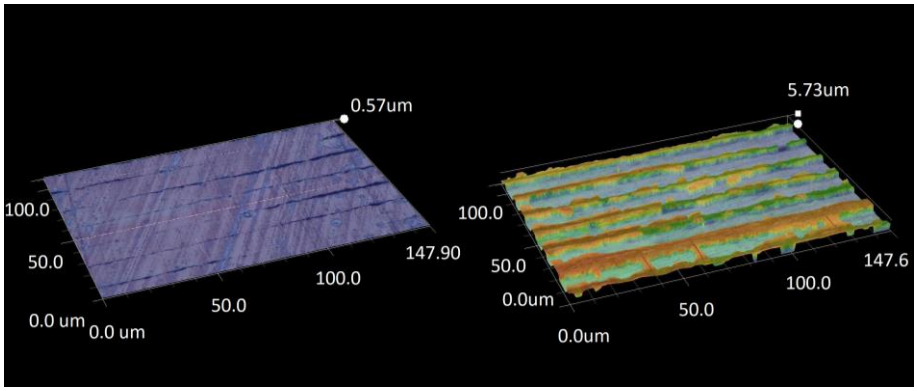

Figure 5-7. Core surface profile before and after etching.

device parameters are therefore extracted at these conditions for examination. The main loss mechanisms are the following:

Switching Device Losses – Turn-off transients of SiC MOSFETs result in energy E_{off} and switching losses given by:

$$P_{sw} = 3(E_{off})f_{sw} \ , \tag{14}$$

where E_{off} values are determined by the technical datasheet of the switching device.

The conduction losses given by the drain-to-source resistance R_{ds} of the device is:

$$P_{cond} = R_{ds} {I_{peak}}^2 (t_{onb} + t_{ont}) f_{sw} \tag{15}$$

A dead-time interval between the top switch turning on and the bottom switch being on is inserted to implement shoot through protection. During this interval, the MOSFET body diode loss is given by:

$$P_{diode} = 3 t_d I_{peak} V_d f_{sw} \,, \tag{16}$$

where t_d is the device dead time and V_d is the body diode forward voltage.

Snubber Loss - Voltage oscillations caused by the resonance between the inductor and the parasitic capacitance during the turn off of the MOSFET are dampened using RC snubbers [44]. Excess energy is captured in the bottom MOSFET turn off interval and later discharged in the series resistor when the device is turned on. The power discharged through the resistor is given as

$$P_{sn} = 3 C_s {V_o}^2 f_{sw}, \tag{17}$$

where C_s is the snubber capacitance.

Summing (9), (10) and (14)-(17) yields the total losses as: $P_{tot} = P_{core} + P_{cu} + P_{sw} + P_{cond} + P_{sn} + P_{diode}$.

5.7. Converter Thermal Design

The thermal management architecture is an important metric due to device temperature limits that are exacerbated with reduced system volume. The worst-case scenario occurs at the system nominal power rating of 80 kW. For hybrid vehicles, a coolant temperature of 105°C and a flow rate of 9 L/min are considered as a tap from the coolant loop from the radiator. The SiC MOSFET junction for the 1.2-kV Wolfspeed XM3 half bridge [45] has a temperature limit T_J of 175°C and

junction-to-case thermal resistance $R_{\theta JC}$ of 0.14 °C/W. A commercial CP3012-XP cold plate with a cold plate-to-case thermal resistance $R_{\theta CC}$ is rated at 0.0087 °C/W at 9L/min [46]. Therefore, by considering the thermal circuit equivalent, the maximum power that can be dissipated using this cold plate is 403 W. Comparing that value to the maximum power dissipation given by the XM3 datasheet [47], the module is able to dissipate 469 W at 105 °C. The anticipated switching device loss using the control strategy at 80 kW is 393 W. The cold plate and modules are modeled using ANSYS Fluent™ and the corresponding simulation is shown in Figure 5-8. The maximum case temperature acquired in the simulation is 145 °C

5.8. Converter Implementation and Results

Following the outlined design method from Sections III-V, the converter rated for 80 kW shown in Figure 5-9 was designed and fabricated according to the specifications listed in Table 5-1. A wide battery voltage range (250-400 V) has been selected to represent battery voltages commonly used [17]. Electric motor requirements dictate the 600-800 V specified DC-link voltage for the inverter. The DOE 2025 EV roadmap targets for DC-DC converters in electric traction drive system [48] stipulate a power density of 33 kW/L. Therefore, a volume < 2.42 L is required for a nominal power rating of 80 kW to meet/exceed power density targets. Meeting stringent power density goals requires optimizing the layout of components to minimize unused spaces within the

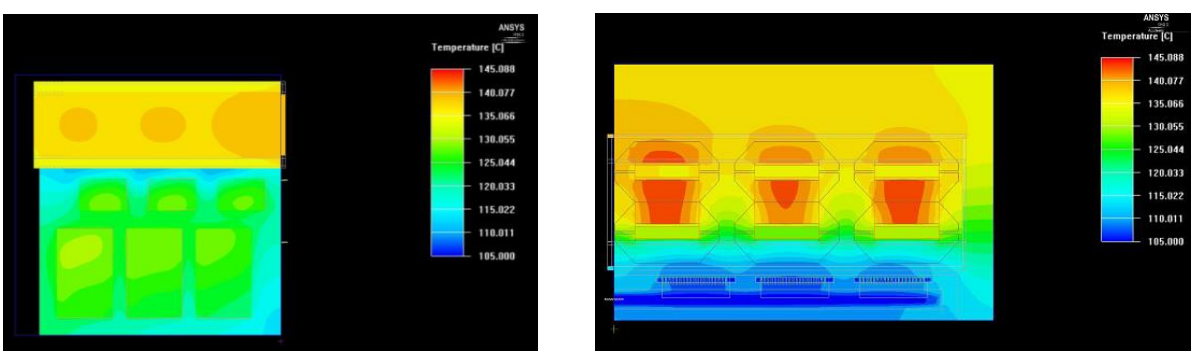

Figure 5-8. Cold plate temperature simulation at nominal power.

Table 5-1: Interleaved Boost Converter Specifications

Parameter	Value
Nominal Power P_{nom}	80 kW
Input Voltage V_{in}	250-400 V
Output Voltage V_{out}	800 V
Efficiency n	> 96 %
Ripple Voltage ΔV_O	1 %
System Volume Vol	< 2.42 L
Inductance L	12.5 µH
Peak Current I_{peak}	≈ 250 A
Potting material thermal conductivity k_{pot}	10 W/mK
Output Capacitance C_o	120 µF
Current Density J_{max}	3 A/mm^2
Maximum Switching Frequency f_{swmax}	50 kHz
Saturation Flux Density B_{sat}	1.5 T
Maximum Flux Density	0.56 T
Steinmetz Coefficient α	1.5319
Stenmetz Coefficient β	1.9632
Steinmetz Coefficient K_c	0.2281
Permeability μ_c	400000μ_0
Kp	38.4
Ki	15360
kg	10000

Figure 5-9. 80 kW interleaved boost converter.

converter enclosure. Maintaining low parasitic inductances is also important such that overshoots are kept to a minimum to protect devices and reduce noise [49]. The encapsulated inductor and

case, power module and snubber resistor are all mounted in well locations on the cold plate to allow for maximum heat transfer.

The gate driver for each half bridge sits directly atop the module with allotted creepage space from the busbar structure. The output capacitors are directly soldered to the laminated busbar, with a height that allows them to sit parallel to the bottom of the cold plate. Nomex 410 paper with 21-kV dielectric strength is used to insulate bus bar layers. The DC bus output has a symmetric arrangement over 6 alternated negative and positive terminals to reduce the current density distribution over the width of the busbar [50].

The volume of the entire converter with the given layout is 1.79 L, representing a power density of 55.6 kW/L at a maximum battery voltage of 400 V. The CGD12HBXMP gate drivers were utilized to accompany the SiC XM3 half bridge modules. The controller gains are shown in Table 5-1. Figure 5-10 shows the laboratory setup used to test the converter, with power resistors used as load. The cold plate is attached to a chiller representing an HEV coolant loop. The inlet and outlet temperatures are measured by thermocouples. A Hioki PW6001-16 power analyzer is connected to measure the system efficiency.

Figure 5-10. Experimental setup.

5.8.1. Simulation and Experimental Results

Power ratings of 16-kW (20%) and 80-kW (100%) are chosen to represent low- and high-power levels in a drive schedule, respectively at V_{bat} = 300 V and V_o = 800 V. The converter with the parameters in Table 5-1 is simulated in MATLAB/Simulink™. Figure 5-11(a) shows the waveforms corresponding to the operation of the converter at 16 kW. The device voltage (magenta) and corresponding phase current (blue) confirms that soft switching (ZCS turn on) is achieved for the bottom switch. At 20% load, there is no overlapping of the phase currents (≈ 8 kHz). At 80 kW in Figure 5-11(b), the phase currents overlap. The resultant ripple current in the input is now reduced at this stage, with a frequency 3 times that of the switching frequency (≈ 49 kHz) of one phase. A peak current of 253 A set for these two low- and high-power levels is observed, which is close to the calculated value. For the same power levels, the experimental results in Figure 5-12 are similar to those in the simulations, satisfying the operation requirements for the converter.

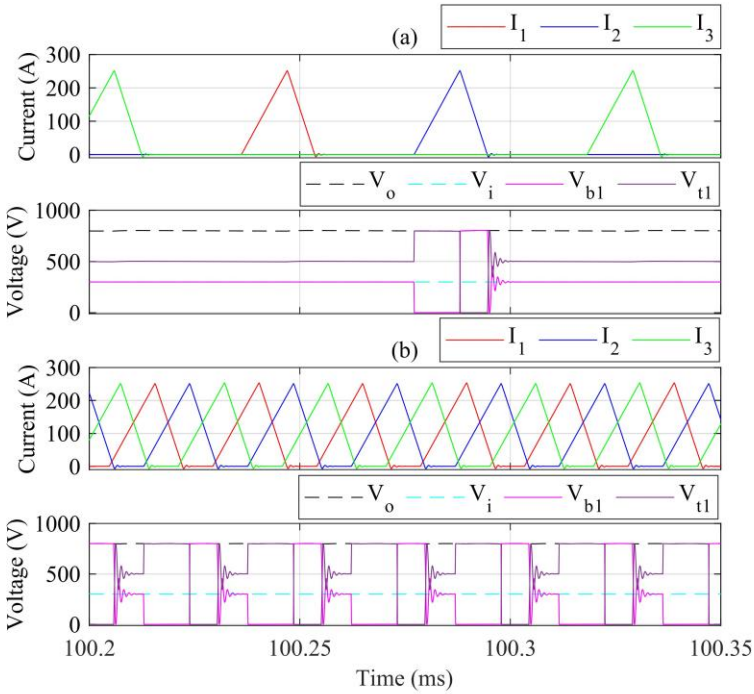

Figure 5-11. Simulation waveforms at (a) 16 kW and (b) 80 kW.

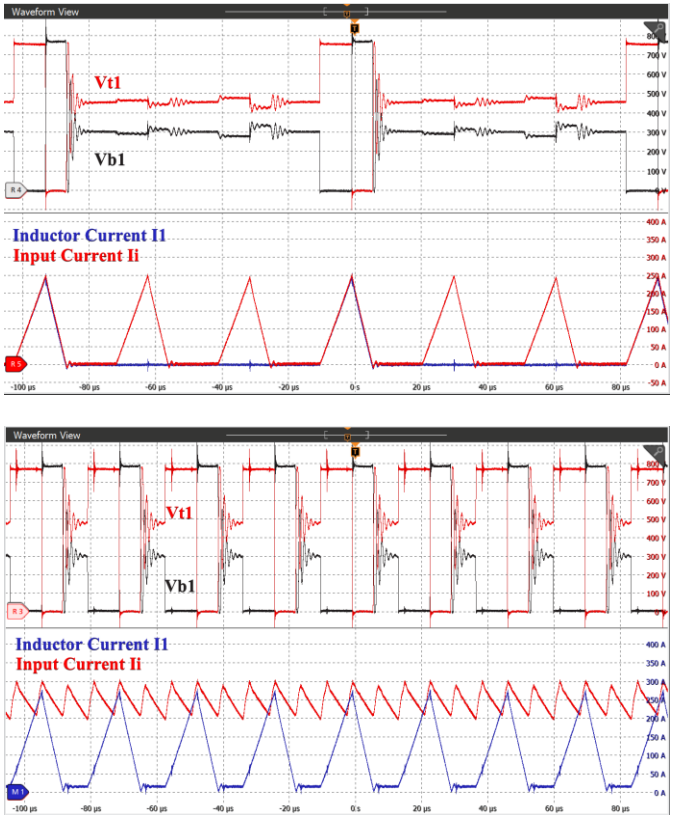

Figure 5-12. Boost converter experimental waveforms at (a) 20-kW and (b) 80-kW. Time scale: 10 µs/div; Vertical scale: 100 V/div, 50 A/div.

5.8.2. System Efficiency

Efficiency data calculated by the power analyzer is shown in Figure 5-13 and compared to the theoretical model for the entire power range of operation, as well as to a fixed frequency 50-kHz PWM control strategy. The measured system efficiency varies between 96 % and 97 % for all power levels. Utilizing the loss mechanisms in (9), (10) and (14)-(17), the componential converter losses are approximated for the considered control strategies and compared in Figure. 5-14. The proposed control strategy achieves an efficiency increase of 3 % at the lowest power level. Switching frequency-related losses in the inductors, switches and snubbers are significantly reduced under the variable-frequency control strategy.

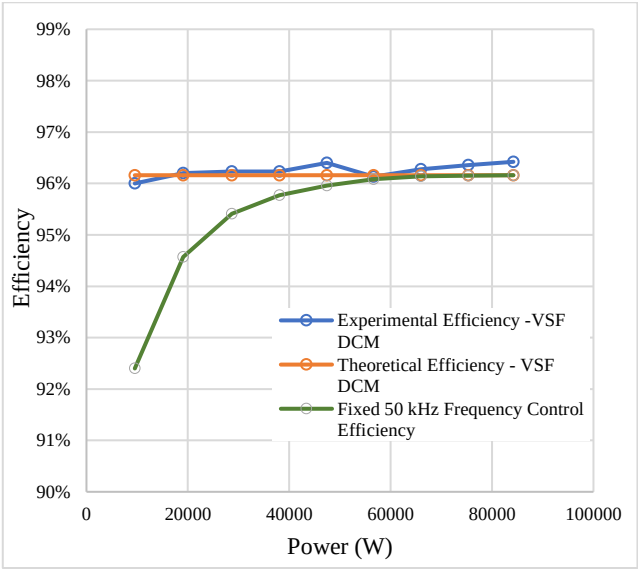

Figure 5-13. Boost converter experimental and theoretical efficiency.

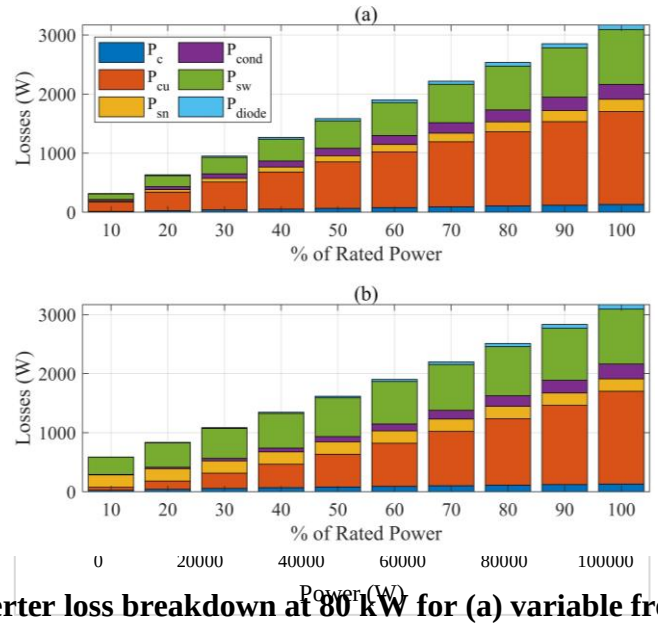

Figure 5-14. Converter loss breakdown at 80 kW for (a) variable frequency strategy and (b) fixed 50 kHz switching frequency.

5.9. Conclusions

A comprehensive design methodology for an interleaved boost converter with high power density and efficiency over a wide power range was presented. An optimization procedure based on sweeping two inductor parameters which are only needed to determine the inductor overall

Table 5-2: Interleaved Boost Converter Efficiency Comparison

Interleaved Boost Converter	η at 20% Rated Load (%)	η at 100% Rated Load (%)	Power Density (kW/L)
DCM VSF	96.16	97	53.3
[51]	94	97	7
[52]	91.8	98	44.2

geometry was developed. The control strategy based on a variable frequency over the entire power range was analytically and experimentally demonstrated to improve the system efficiency at lower power levels, representing an improvement of the battery utilization for e-mobility applications. Experimental verification of the proposed design methodology and control strategy demonstrated that the system efficiency remained within 96 % and 97 % across the entire power range. The final design had a volume of 1.79 L with a 55.6 kW/L power density. The proposed converter is compared to existing high power interleaved boost converters of comparable power in literature in Table 5-2.

5.10. Acknowledgments

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CHAPTER 6

MINIMIZING DC LINK CAPACITOR CONTROL STRATEGY

6.1. Abstract

Link filtering capacitors occupy a significant volume in DC-DC-AC power conversion unit (PCU) for electric vehicle (EV) applications, where manufacturing costs and power density are related metrics and are important. Typically, the DC-Link capacitor is sized electrically based on the desired voltage ripple and rms current capacity, with the latter being the ultimate deciding factor in the capacitor overall physical volume. This paper proposes a synchronous modulation strategy that matches the current of an interleaved DC-DC converter in discontinuous conduction mode (DCM) with that of the inverter-drawn current to significantly reduce the RMS current ripple in the DC-link capacitor, and thus enabling a volumetric reduction when considering system design and increasing capacitor lifetime. Simulation and experimental results are presented to validate the claims of this work.

6.2. Introduction

EV configurations consisting of series-connected DC-DC converter and DC-AC inverter stages as shown in Fig. 1 provide system level cost advantage for manufacturers in that a smaller and more power dense battery packs can be utilized within EVs [1]–[3]. If increased global market penetration of EVs are to be realized to combat fossil fuel emission within the transportation industry [4], the system level component utilization must therefore be assessed and be optimized to meet cost, efficiency, and manufacturability. The metric of power density holistically touches

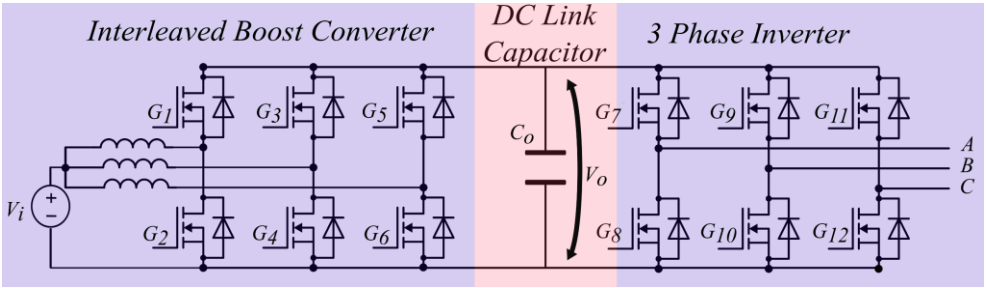


Figure 6-1. EV PCU circuit topology.

the aforementioned factors, making it a significant figure of merit in the system design process. Therefore, volumetric reduction of individual components; particularly the passive components is vital [5]. The DC-link capacitor located between the DC-DC and DC-AC stages in the EV configuration in Figure 6-1 is required to provide a suitable voltage ripple and also absorb RMS current. However, the RMS current rating of the capacitor usually determines the volume of the capacitor as opposed to the capacitance requirement for the application voltage ripple tolerance [6]. Repeated thermal cycling from excessive RMS current in the capacitor also significantly deteriorates system reliability due to film degradation [7]. It is consequently advantageous to reduce the RMS current in the dc-link capacitor to increase system power density while simultaneously increasing the overall lifetime of the capacitor, thus enhancing system reliability.

It was proposed in [8] to make the output DC-link current from the DC-DC converter equal to the inverter input current such that no current flows theoretically into the capacitor. The main drawback that can be observed from this method is that a large reduction in the converter output ripple current is required which is synthesized through the use of a large inductor operating under continuous conduction mode (CCM). As a result, increased switching-related losses in the inductor and also the switching devices (due to hard switching) alongside an increase in the system volume are realized. In [9], a synchronizing carrier modulation strategy was proposed by making a single-phase boost converter operate with twice the switching frequency of the inverter, and thus

decreasing significantly the ripple current. However, CCM operation combined with doubling the switching frequency leads to higher losses in the switching devices and especially the inductor, thus decreasing lifetime and increasing cost/complexity in thermal management solutions for the PCU. Additionally, any power density increase gained from the reduction of the capacitor, is neutralized by the increased size of the inductor.

A phase-shift based modulation strategy for an interleaved DCM boost converter operated with a variable DC bus [10] synchronized with a two level inverter is proposed in this paper. This method not only reduces the RMS current in the DC-link capacitor leading to decreased capacitor volume and increased reliability, but it also allows for a reduction in the inductor volume due to low inductance requirements for DCM an enhanced efficiency with the zero-current switching (ZCS) in the boost stage of the PCU [11], [12] with DCM in conjunction with a variable dc-link voltage [13], [14].

6.3. Converter operating conditions

The control structure for the system configuration shown in Figure 6-1 is described in this section. Typical inverter control methods normally are dependent on a constant DC bus voltage with a varying modulation index to realize motor speed and torque requirements. However, for the proposed control algorithm, a variable DC-link voltage is required, as a variable output current peak is also realized enhancing the RMS current minimization. As such, the DC-DC converter is utilized in the proposed control strategy to control the DC-bus voltage. Examining one phase of the boost converter (for simplicity and theoretical derivation), a turn-on time of DT_{sw}, where T_{sw} is the switching period, synthesizes an average converter output current $\overline{I_o}$:

$$\overline{I_o} = \frac{3{V_i}^2 D^2 T_{sw}}{2L(V_o - V_i)} \tag{1}$$

$$\overline{I_o} = \frac{3{V_i}^2 D^2 T_{sw}}{2L(V_o - V_i)} \tag{1}$$

where V_i is the input voltage, V_o is the output voltage, D the duty cycle of the converter and L the boost inductance value. The duty cycle D is therefore modified accordingly to meet the load demand.

Considering the DC-AC inverter stage of the system, a traditional space vector pulse width (SVPWM) is used to change the DC-link voltage into the three-phase voltages at the motor stator [15] with a constant modulation index MI implemented (synthesizing benefits in THD). The stator reference voltage can be derived as $V_{ref} = 0.5MIV_o$ As such, the average inverter input current (equal to the average converter out current) is $\overline{I_o} = 0.75MII_m cos\varphi$ in the constant torque region. The instantaneous current waveforms of the system are illustrated in Figure 6-2 Applying KCL at the capacitor node in Fig. 1, the current in the dc-link capacitor I_{cap} will be the difference between the converter output current I_{conv} and inverter input current I_{inv}. From Figure 2(c), I_{cap} will be minimized when the cancellation between I_{inv} and I_{conv} is at its maximum.

6.4. Inverter carrier phase shift calculation and current derivation

To realize maximum cancellation under the proposed control method, two conditions must be recognized. Firstly, the inverter switching frequency f_{inv} must be a multiple n times of the

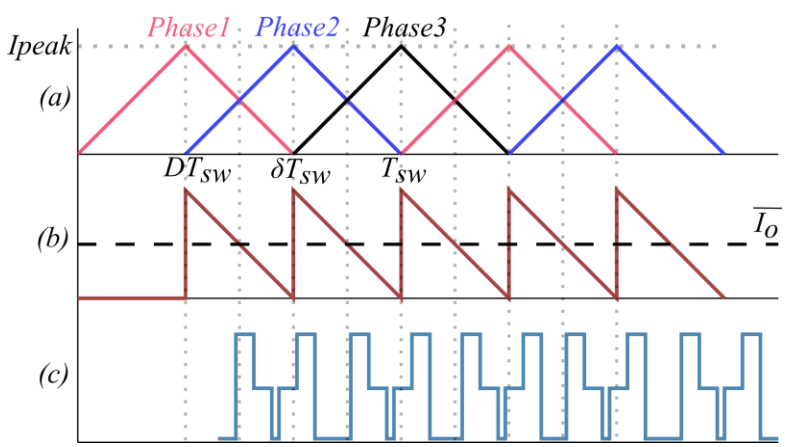


Figure 6-2. Instantaneous current waveforms of: (a) Converter input, (b) Converter output, (c) Inverter input.

converter switching frequency f_{conv} corresponding to the number of phases in the converter. Secondly, maximum I_{inv} must occur simultaneously with the maximum I_{conv}. Under space vector modulation (SVM), any synthesized vector begins and is terminated symmetrically with a zero or seven vector applied, under which the load current is freewheeling. The triangular waveform responsible for the PWM generation in the inverter phases according to the vector reference must therefore be shifted to synchronize I_{inv} to I_{conv}. The phase shift, φ, as seen in Figure 6-3 can be expressed as a sum of time interval components Δt and t_0 respectively; Δt is a compensation for the phase turn-off time given as $\Delta t = T_{swc} - \frac{LV_iD}{V_o - V_i}$, and t_0 a compensation for the zero-vector duration applied under SVM. For any desired synthesized vector, the duty cycles for each applied vector is [16]:

$$D_{x1} = \frac{t_{x1}}{T_{Swc}} = \frac{\sqrt{3}\mathrm{MI}}{2}\sin\left(\theta - \frac{\pi}{3}\right) \tag{2}$$

$$D_{x2} = \frac{t_{x2}}{T_{Swc}} = \frac{\sqrt{3}\mathrm{MI}}{2}\sin\left(\theta + \frac{\pi}{3}\right) \tag{3}$$

where θ is the vector angle. The duration of the zero vector is then derived as follows:

$$D_0 = D_7 = 0.5(1 - D_1 - D_2) \tag{4}$$

The total phase shift φ to be applied at every cycle is then given by:

$$\varphi = 360 * 3f_{sw} * \left[\left(T_{swc} - \frac{LV_iD}{V_o - V_i}\right) - D_0T_{swc}\right] \tag{5}$$

Considering I_{conv} in Figure 6-3, the RMS current $I_{convrms}$ can geometrically be deduced to be $I_{convrms} = dI\sqrt{\frac{\delta T}{3T_{swc}}}$. The inverter RMS input current can also be derived as $I_{invrms} = \frac{I_m}{\sqrt{2}}\sqrt{\frac{2\sqrt{3}MI\left(\frac{1}{4}+cos^2\varphi\right)}{\pi}}$ where $cos\varphi$ is the power factor. The minimized in-phase capacitor RMS current

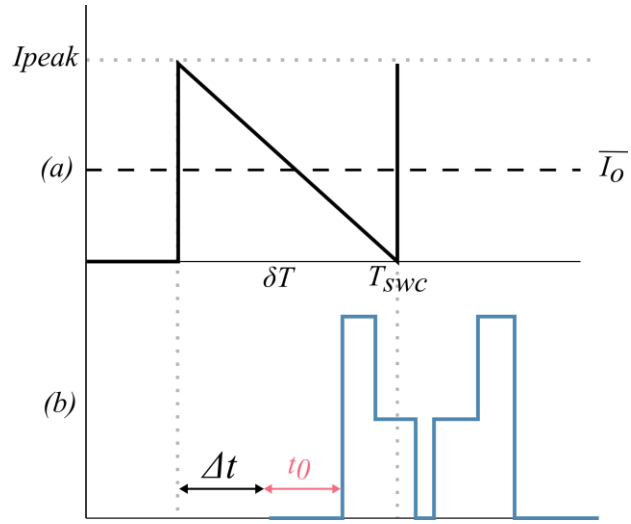


Figure 6-3. (a) Converter output current, (b) Phase shift for inverter input current.

under the proposed synchronous conditions can therefore be expressed as the square root of the square of the difference of the two currents:

$$I_{caprms} = \sqrt{dI^2 \frac{\delta T}{3T_{swc}} - \left(\frac{I_m}{2}\frac{2\sqrt{3}MI\left(\frac{1}{4}+cos^2\varphi\right)}{\pi}\right)} \tag{6}$$

From (6) under synchronization, it is advantageous to operate with a lower peak current (as dictated by the variable dc-link voltage strategy) and also to operate with a high modulation index, in order to reduce I_{caprms} at any power level.

6.5. Simulation and Experimental results

With the specifications in Table 6-1, a PCU was simulated to detremine the effectiveness of the proposed synchronous control method. A power rating of 1 kW for the converter is simulated in MATLAB/Simulink™. The PCU is simulated with a traditional unsynchronized control method as shown in Figure 6-4(I). Figure 6-4(II) shows the PCU's corresponding current waveforms after the phase shift is applied. The resultant instantaneous capacitor current shows a 30% reduction in RMS current from 1.6 A to 1.1 A RMS) due to the cancellation of the converter and inverter currents in Figure 6-4(a) and Figure 6-4(c), respectively. Following the simulation results, a

Table 6-1: Prototype Specifications

Variable	Value
P_{nom}	1 kW
V_{in}; V_{out}	100 V; 175 V
f_{sw}	20 kHz
L	100 µH
C	240 µF
I_{peak}	4.6 A
MI	0.9

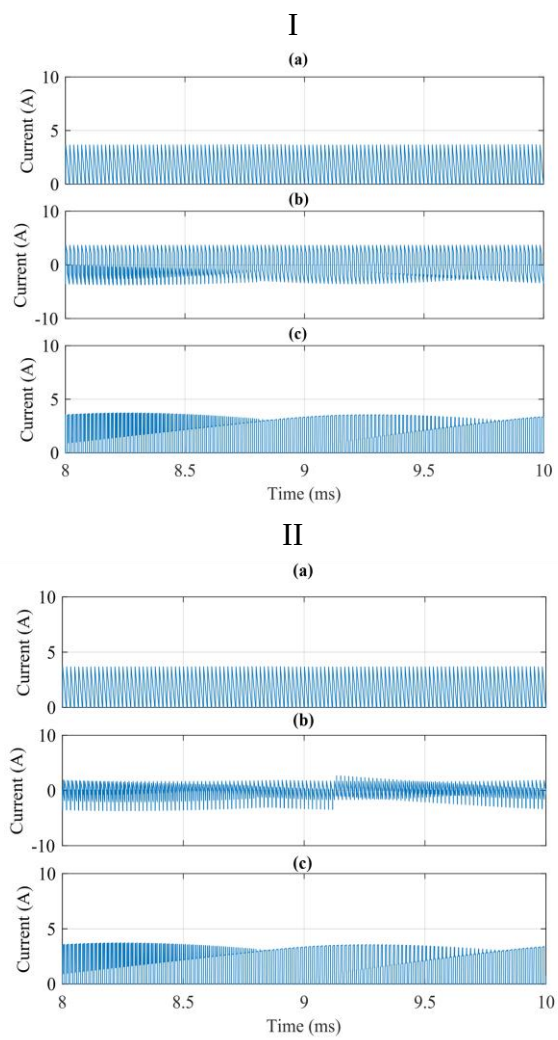


Figure 6-4. Simulation current waveforms of: (a) Converter input, (b) Converter output, (c) Inverter input.

prototype is built and experimentally tested under the same simulation conditions. Figure 6-5 shows the designed prototype and test setup. The experimental results under the same conditions

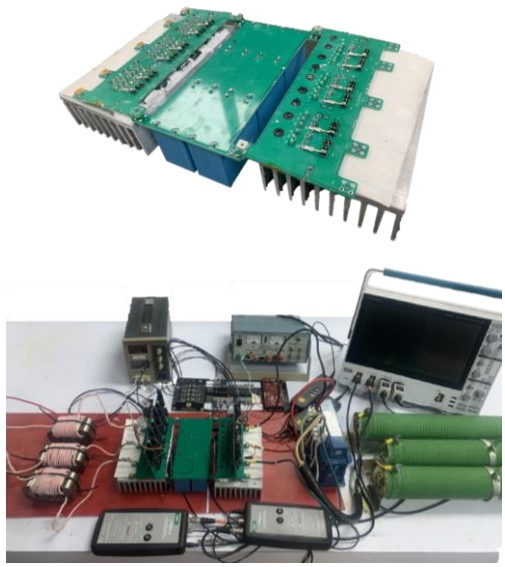


Figure 6-5. Prototype and Experimental setup

follow that of the simulation in Figure 6-6. I_{caprms} before the proposed control method is 1.619 A. After the phase shift is applied, I_{caprms} is reduced to 1 A, ≈ 30% reduction in the capacitor current.

6.6. Capacitor lifetime and volume reduction

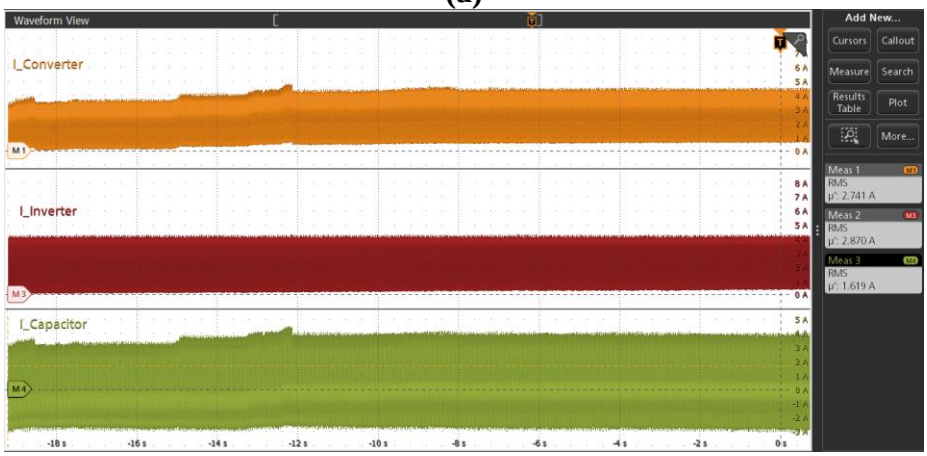
A comparison of capacitors from four manufacturers are selected to evaluate the effectiveness of the proposed synchronization method in reducing the volume of the required capacitor in the selection process of the overall converter design. The capacitor lifetime model to derive its operational hours as based on the theory in [17], [18] is defined as:

$$Lifetime\ (hours)\ =\ L_b M_v 2^{(T_m - \frac{T_{HS}}{10})} \tag{7}$$

where L_b is the capacitor rated lifetime hours, M_v the voltage rating ratio and T_m the ambient temperature. T_{HS} is the hotspot temperature and is:

$$T_{HS} = R_{th} {I_{CAPRMS}}^2 R_{ESR} \tag{8}$$

(a)



(b)

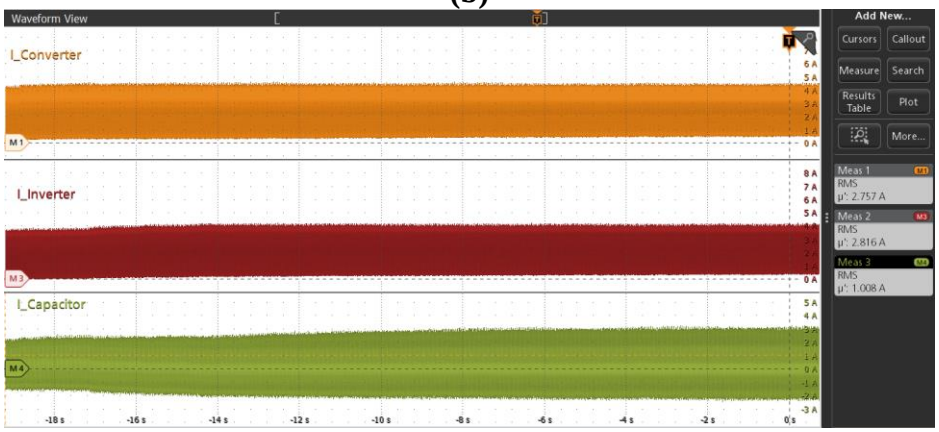


Figure 6-6. Instantaneous current waveforms of converter input, inverter input and converter output (a) no phase shift (b) proposed phase shift applied.

where R_{th} is the package thermal resistance and R_{ESR} is the equivalent series resistance. A database is populated from said manufacturers, with the RMS current capability, R_{th}, volume *Vol*, and capacitance of each capacitor being a field of interest. Using the same voltage class of capacitors, an optimization algorithm selects the least number of capacitors depending on the manufacturer availability to satisfy design requirements for μF and RMS current based on the specifications in Table 6-1. Figure 6-7 displays the design resultant volume requirements and expected lifetime hours for scenarios before and after the proposed synchronized phase shift is applied. From Figure 6-7(a), an average volume reduction of ≈ 20% can be observed with the phase shift applied,

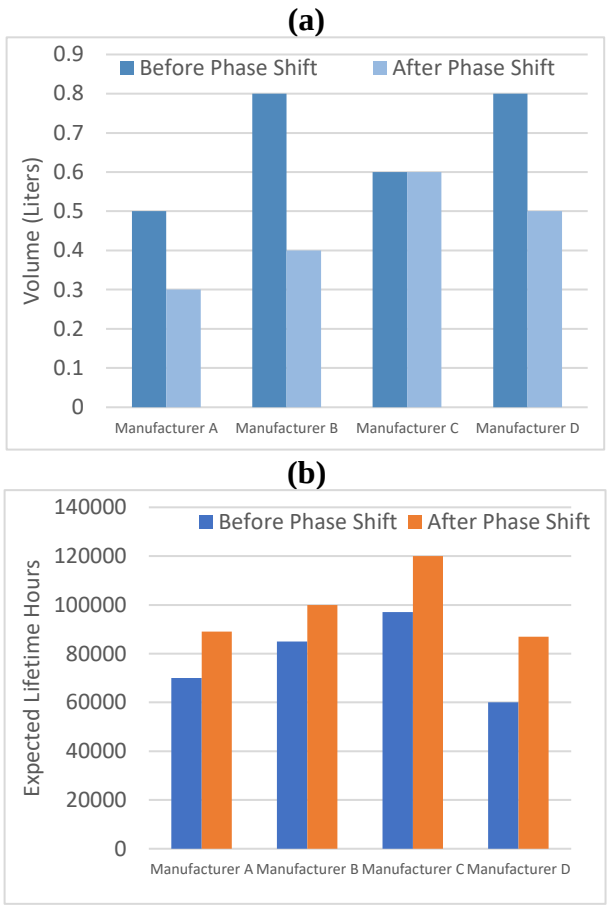


Figure 6-7 (a) Capacitor Volume and (b) Expected lifetime hours before and after phase shift is applied.

translating to benefits in power density. Additionally, Figure 6-7(b) shows an average capacitor lifetime increase of ≈ 25% due to the reduced capacitor RMS current.

6.7. Conclusions

A control technique to minimize the RMS current in the dc-link capacitor has been theoretically and experimentally demonstrated though the implementation of a synchronized switching methodology between a DC-DC converter and a DC-AC inverter. The proposed method effectively reduces the RMS current in the capacitor by 30% compared to traditional unsynchronized PCU control, allowing for an average 20% smaller capacitor volume to be used in the design of the PCU due to the reduced RMS current handling capability. Additionally, the

implementation of this control method can reduce thermal degradation of DC-link capacitors thus improving system lifetime by an average of 25%.

6.8. Acknowledgements

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CHAPTER 7

REDUCED CAPACITOR RMS CURRENT ENABLING HIGH POWER DENSITY PCU

7.1. Abstract

DC-link capacitors are often the source of excessive volume and electrical failures in power conversion units (PCU) for electric and hybrid electric vehicles (EVs and HEVs) [1]. The RMS current capacity requirement ultimately determines the bulk dimensions of DC-link capacitors as opposed to the required voltage ripple. This current is also responsible for the capacitor lifetime degradation through Ohmic heating arising from the inherit capacitor ESR. A variable-frequency synchronous-carrier shift-based control algorithm that juxtapositions the output current of an interleaved boost converter with the input current of an inverter is presented. It allows for a significant reduction in the capacitor RMS current resulting in size reductions. In addition, the proposed algorithm increases the system reliability by extending the capacitor estimated lifetime by up to 25 %. A 50-kW PCU prototype with a power density of 55.6 kW/L has been designed in this chapter. Simulation and experimental results are presented to validate the proposed ideas.

7.2. Introduction

The global pursuit of optimized EV/HEV PCUs in an effort to reduce greenhouse emissions by replacing the conventional internal combustion engine has given rise to techno-economic requirements on EV manufacturers to meet the rising market demand. On both fronts, there are unique optimization challenges that manufacturers face to extract the best possible solution without compromising cost and system performance. Comprehensive PCU design methods can be implemented by tackling comprehensive system metrics such as power density, efficiency and reliability which all demonstrate strong correlation to manufacturing costs and technical performance [2], [3]. In addressing power density specifically, reducing the system volume

becomes advantageous since less volume may imply a reduced system cost. Furthermore, there is a need for higher efficiencies, which requires minimizing PCU losses over a wide power range for the expected higher heat fluxes, to improve battery utilization.

A PCU architectures comprising of a bidirectional DC-DC converter in series with the motor inverter as shown in Figure 7-1 may offer great advantages as opposed to those configurations in which the battery is directly connected to the motor inverter, in that the battery voltage is regulated minimizing the occurrence of voltage drops while the system is being used [4]. The regulation of the DC-link voltage mitigates common-mode noise for various power levels while also increasing overall system efficiency [5], [6]. In control methods in which the DC-link voltage is varied according to the desired motor speed, losses in the motor inverter stage and the motor itself are greatly reduced, even offsetting the net losses through the inclusion of an additional stage [7], [8].

Parallel to the increase in demand of EVs is the increased penetration and availability of wide bandgap (WBG) semiconductor devices, which are significantly improving the field of power electronics. Silicon carbide (SiC) utilization within EV has shown to exhibit superior performance considering withstand voltage levels and switching losses in comparison to traditional silicon based semiconductors [9], with the former allowing for higher switching frequencies, and thus

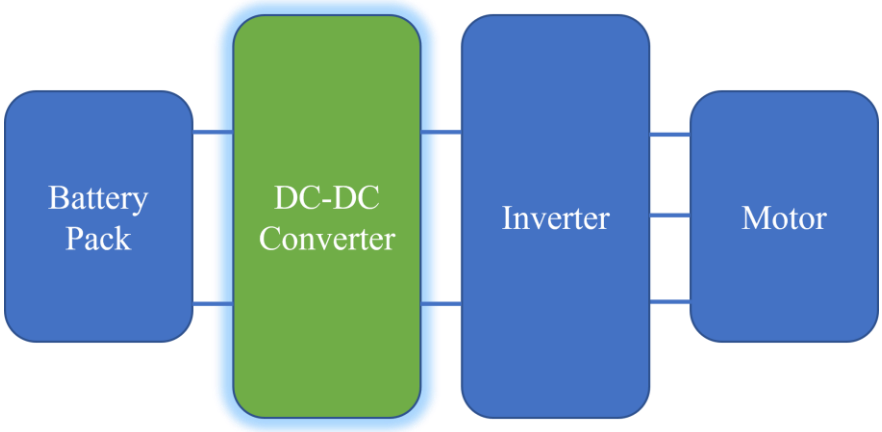


Figure 7-1. HEV PCU architecture including DC-DC converter.

reducing filter sizing requirements [10]. Theoretically, this approach is generally the route to realize the aforementioned power density goals in PCU designs, particularly as passive components (capacitor) generally comprise 30% of the total converter volume [11]. In practice, the DC-link capacitor size is determined by RMS current ripple requirements, reducing any volume saving benefits gained by ripple voltage reduction that may have been achieved by increasing the switching frequency.

In general, the role of the DC-link capacitor is two-fold: to provide a suitable voltage ripple, and to withstand the inverter RMS current. Therefore, reducing the capacitor RMS current can provide the possibility of selecting a capacitor with a smaller volume, and thus increasing power density, as well as extend its lifetime.

Considering the DC-link capacitor structure, typically two types are utilized within the power converters: ceramic and film whose failure modes are illustrated in Figure 7-2. Ceramic capacitors offer advantages in high current density, peak temperatures, and lifetime due to its PLZT layered construction [12]. However, higher costs and having mainly a short-circuit failure mode have hindered their insertion in HEV applications. Film capacitors have lower costs and mainly an open-

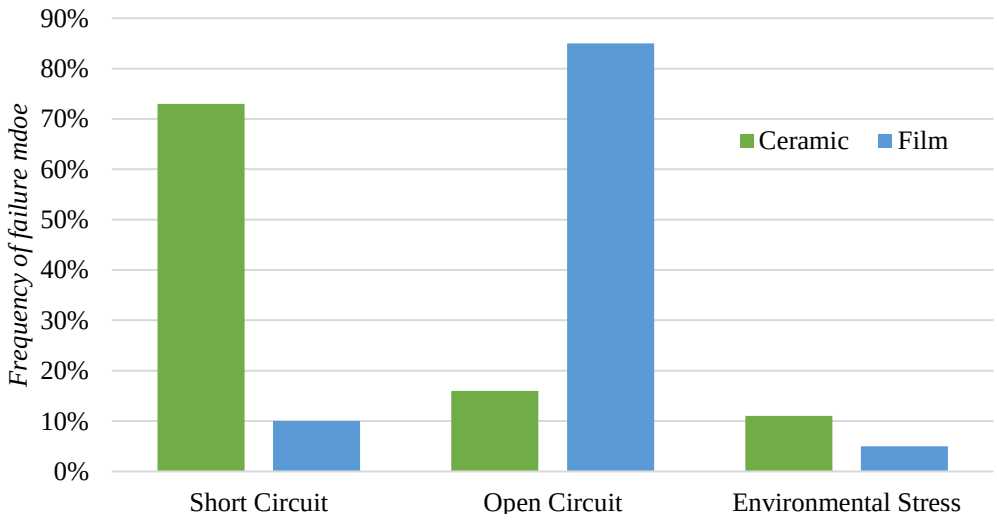


Figure 7-2. Capacitor failure mode distributions [10].

circuit failure mode making them a better alternative. Unfortunately, film capacitor reliability and lifetime are significantly hampered by excessive high temperature cycling which causes damage to the layered film structure [13]. This high temperature is the result of the internal Ohmic heating due to the capacitor RMS current and equivalent series resistance (ESR). As degradation occurs within the capacitor, the ESR increases while the capacitance typically decreases, causing an increase in the ripple voltage [14]. It is quite established that the status of capacitor ESR and/or capacitance are essential to determine overall lifetime and reliability models [15]–[17]. Several control methods have been explored to attempt reducing the RMS current with significant tradeoffs that often outweigh any benefits achieved [17]-[18]. Most of these efforts are aimed at DC-DC-AC related applications with a single-phase implementation.

The converter output current waveform i_{conv} and the inverter input current i_{inv} are typically unique in geometric shape as shown in Figure 7-3, under the assumption that the switching frequency is large enough such that the inverter current is considered constant within a switching interval. Because the instantaneous current in the capacitor is the difference between i_{conv} and

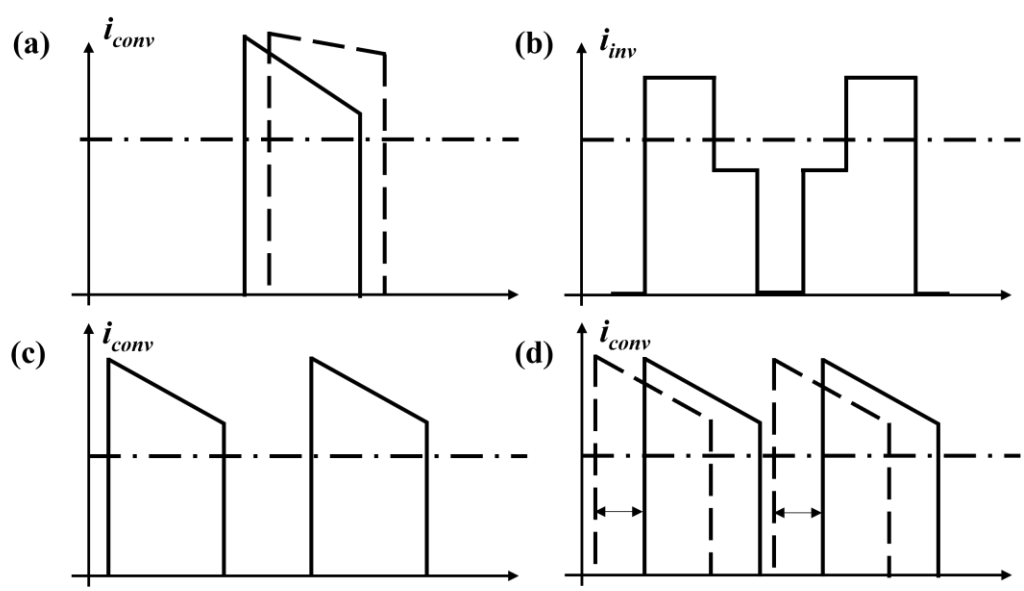


Figure 7-3. Considered converter and inverter currents.

i_{inv}, having complete cancellation of the two waveforms effectively makes the capacitor RMS current negligible. Reference [18] uses the topology in Figure 7-1 to propose an equalization of i_{conv} and i_{inv} such that no current flows *theoretically* into the capacitor. The authors achieve this reduction in ripple by flattening the typically distinct i_{conv} slope in Figure 7-3(a) to achieve a better geometric waveform matching with i_{inv} in Figure 7-3(b). However, the disadvantage that arises from this method is that the ripple reduction in i_{conv} is synthesized through the use of an exorbitant 0.857 mH inductor operating under continuous conduction mode (CCM). This large inductor poses a threat to overarching goal of power density as it requires a significant volume. Additionally, the CCM increases switching-related losses in the inductor and devices due to hard-switching operation, hampering overall efficiency.

Another approach for reducing the RMS current in the capacitor takes advantage of the respective waveform geometries. Through the commonly used Sine Pulse-Width-Modulation (SPWM) or Space Vector Modulation (SVM) inverter control strategies, i_{inv} produces a symmetrical non-linear pulse shape characterized by two distinct pulses separated by a period of zero current as illustrated in Figure 7-3(b). The authors in [19] seek to take advantage of this phenomena through the development of a synchronizing carrier modulation strategy by making a single-phase boost converter operate at twice the inverter switching frequency. For a single-phase DC-DC based system, doubling the switching frequency results in two pulses of i_{conv} shown in Figure 7-3(c). The carrier responsible for generating the switching reference of the converter can therefore be shifted so that the two pulses of i_{conv} are superimposed on i_{inv} to reduce the capacitor current quite effectively; see Figure 7-3(d). Furthermore, CCM operation combined with the increased switching frequency leads to much higher losses in both the devices and inductor. This increases the complexity and potentially the size of the thermal management solution with reduced

efficiency at higher power. Additionally, any power density increase gained from the reduction of the capacitor, is neutralized by the increased size of the inductor for CCM.

Reference [20] also proposes a unique approach to RMS current reduction. As opposed to increasing the switching frequency as done in [19], the authors utilize a four-phase interleaved boost converter in conjunction with the inverter to realize the PCU. The current i_{conv} is quadrupled without an effective increase in each device's switching frequency such that low losses are maintained. This method is an extension of the previous efforts, in that it decomposes i_{inv} even further into four non-zero states. The method then optimizes the duration and sequence of each DC-DC converter phase and resultant i_{conv} through phase-shifting to match that of i_{inv} to create the best scenario for current cancellation. The optimization is however extremely computationally intensive; each phase's shift and duration are stored and accessed in a large lookup table depending on the system state. This can lead to controller related problems at high switching frequency when the access time and computation period are on the same order of clock cycles. The non-uniform operation of the DC-DC phases can also lead to stability issues at the DC-link voltage which can cause distortion related losses on the motor considering the application. The voltage instability can also make dynamic events such as rapid changes in torque/speed requirements quite cumbersome.

This chapter proposes a phase-shift based modulation strategy for a three-phase interleaved boost converter operated under discontinuous conduction mode (DCM) and a variable DC-bus voltage [7] synchronized with a two-level inverter enabling high power density in a 50 kW PCU. The control method not only reduces the RMS current in the DC-link capacitor leading to reduced capacitor volume and increased reliability, but it also allows for a reduction in the inductor volume due to low inductance requirements under DCM operation. Thus, an enhanced efficiency results from the zero-current switching (ZCS) under DCM in the PCU boost stage [21], [22] in

conjunction with a variable DC-link voltage [8], [23]. Unlike previously researched methods, the proposed one requires the inverter stage to have a switching frequency equal to one-thirds of the DC-DC stage f_{swconv}, as opposed to the doubling, further improving efficiency. The method deduces the phase-shift online and can be simply implemented with minimal computational effort. Simulation and experimental results demonstrate the validity and effectiveness of the proposed ideas. The experimental validation makes use of an 50-kW PCU prototype. The chapter is organized as follows: the PCU topology is described in Section 7.3. The implementation of the control strategy is given in Section 7.4. System losses and thermal management are addressed in Section 7.5. The capacitor selection is presented in Section 7.6. The system design procedure is described in Section 7.7. Lastly, experimental results are analyzed in Section 7.8.

7.3. PCU Topology Description

Figure 7-4 shows the circuit diagram of the proposed PCU that consists of two series connected stages. The first stage directly connecting to the battery bank with a parallel filtering capacitor C_i at voltage V_i consists of an interleaved three-phase boost stage when the PCU operates in forward power flow mode. The converter output is connected to capacitor $C_o$which filters the output voltage V_o while also absorbing the RMS current two-level three-phase inverter supplying phase AC currents I_a, I_b and I_c to the electric motor. Assuming operation when the PCU is transferring power from the battery to the motor (boost mode), the bottom switches G_2, G_4 and G_6

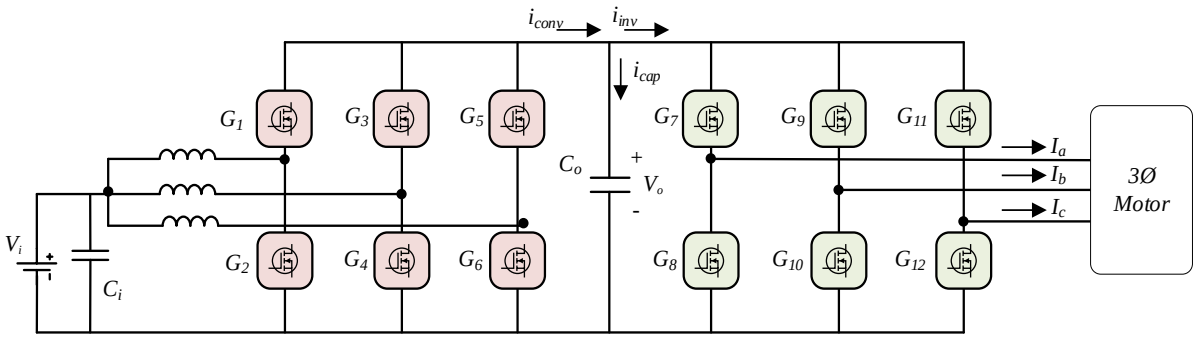


Figure 7-4. Circuit topology for the proposed PCU.

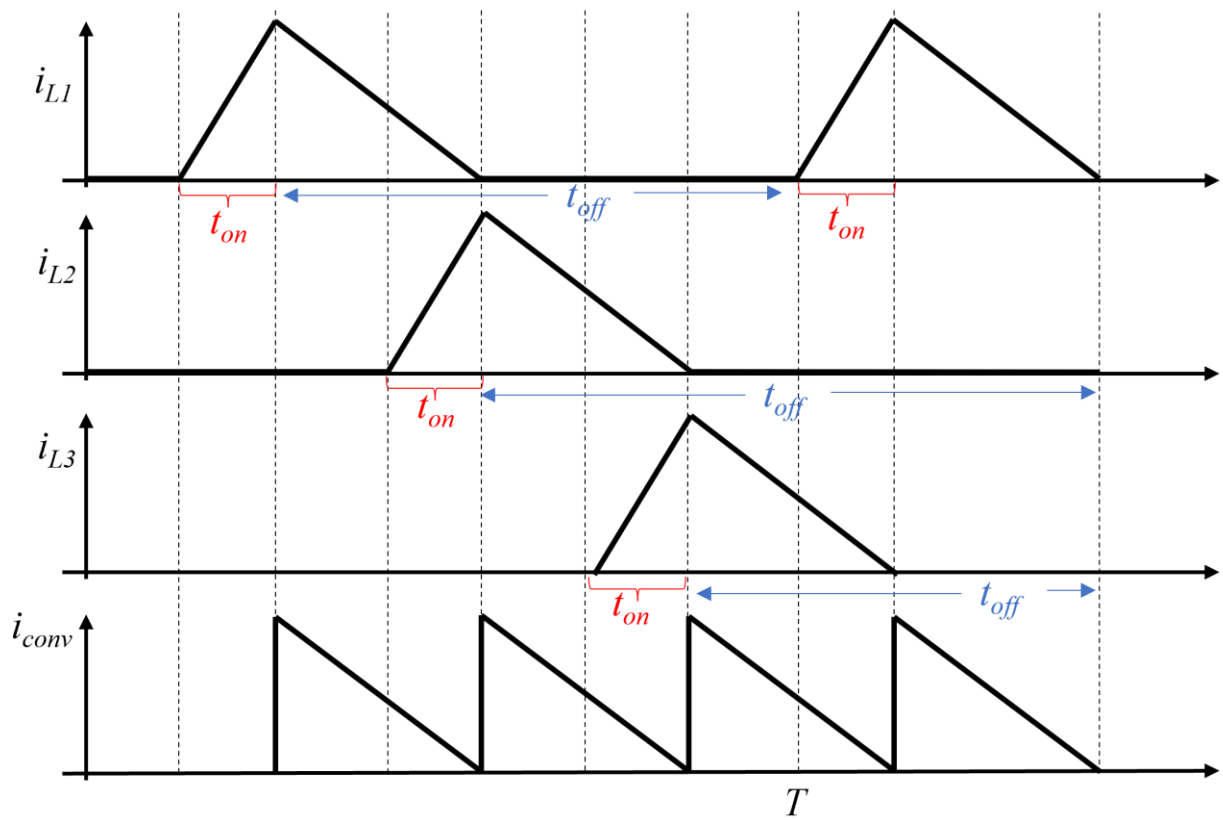


Figure 7-5. PCU interleaved inductor phase currents and resultant converter output.

of the boost stage are turned on during time t_{on} in which the corresponding inductors L_1, L_2 and L_3 of inductance L for each phase are charged with currents i_{L1}, i_{L2} and i_{L3}, respectively. During the turn off interval t_{off}, the energies in the inductors are discharged to the output load (i.e., DC link) to meet synchronous operation conditions under DCM [24]. Figure 7-5 shows the boost converter desired phase currents under which the design considerations are made.

Assessing the DC-AC inverter stage, the modulation index alongside the fundamental frequency of the inverter is traditionally varied to meet the electric motor torque and speed requirements, respectively [25]. However, within the proposed implementation of the system, a space vector pulse width modulation (SVPWM) with a constant modulation index (MI) is utilized to produce the three-phase voltages at the stator of the motor [8], producing benefits in low THD.

The amplitude of the stator voltage is therefore regulated by a variable voltage V_o synthesized by modifying the duty cycle *D* of the boost stage.

7.4. PCU Control Methodology and Proposed Phase Shift

Assuming a completely lossless system, the average output voltage V_o of the three-phase interleaved boost stage is controlled according to *D* by [26]:

$$V_o = \frac{3V_i D^2}{MI f_{swconv} L(I_a + I_b + I_c)\cos(\theta)} + V_i. \tag{1}$$

where I_a, I_b and I_c are the inverter RMS phase currents, *L* the boost converter phase inductance. At maximum power P_{nom}, the operating condition for the strategy dictates that the average output current $\bar{I}_o$ is at boundary CCM-DCM (implying each interleaved phase operates with DCM) to ensure DCM at lower load conditions, sustaining ZCS [24]. The output power under this condition can therefore be expressed as follows:

$$P_o = \frac{V_o(V_o - V_i)}{6L f_{swconv}} \tag{2}$$

Since the DC-link voltage can be controlled by the boost stage, the modulation index *MI* can be held at a high constant value, as by extension, the PCU output power is controlled by duty cycle which varies the DC-link voltage [27].

Figure 7-6(a) illustrates the main output waveforms of the circuit shown in Figure 7-4. Through the implementation of SVM, any voltage vector V_{ref} can be transformed in a αβ vector frame in accordance with the Clarke transformation [28] as shown in the space vector diagram in Figure 7-6(b). Therefore, expressing any space vector within this method corresponds to the application of the two adjacent vectors for a duty cycle of D_1 and D_2, and a zero vector:

$$\begin{gathered} D_1 = \frac{3t_1}{T_{swinv}} = \frac{\sqrt{3}M}{2} sin\left(\theta - \frac{k\pi}{3}\right) \\ D_2 = \frac{3t_2}{T_{swinv}} = \frac{\sqrt{3}\mathrm{M}}{2}\sin\left(\theta + \frac{k\pi}{3}\right) \\ D_0 = 0.5(1 - D_1 - D_2) \end{gathered} \tag{3}$$

where k corresponds to the sector location. Utilizing KCL, the instantaneous current in the DC-link capacitor is a result of the difference in i_{conv} and i_{inv}. However, if there is an offset of the starting time whereby peak values of both currents occur the resultant RMS current in the capacitor is negatively affected.

An active phase shift is therefore the novel proposition of this chapter. It is applied on every switching cycle to the sawtooth carrier which generates the inverter duty cycle to compensate for this offset. The duration D_0T_{sw} of the zero or seventh vector and the t_{on} duration derived in [26] can be summed to derive the phase shift required to synchronize i_{conv} and i_{inv}:

$$-\varphi = 2\pi * 3f_{swconv}(t_{on} + D_0T_{swinv}) \tag{4}$$

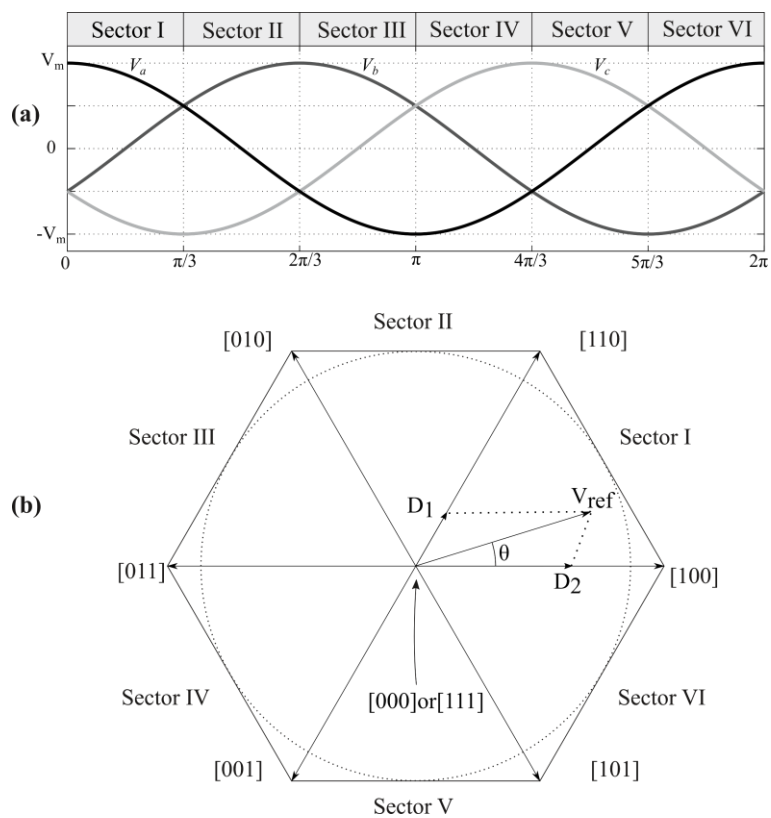


Figure 7-6. (a) PCU filtered voltage output, and (b) Space-vector implementation for inverter.

According to (4), shifting the inverter carrier by φ creates synchronous conditions for current cancellation. Figure 7-7 illustrates the proposed active phase shift. For the non-phase shifted inverter current i_{inv} waveform in Figure 7-7(b) mismatches with i_{conv} in Figure 7-7(a), the resultant i_{cap} is shown in Figure 7-7(c). The synchronized i_{inv} in Figure 7-5(d) causes a 25% reduction in i_{cap} ripple, peak and ultimately RMS in Figure 7-7(e).

7.5. Deriving RMS Current

Now that the conditions for the converter operation have been established, the derivation of i_{capRMS} can be addressed. The capacitor current i_{cap} is an extremely discontinuous waveform derived from the difference between i_{conv} and i_{inv}, so typical mathematical methods to extract the RMS value can be over analytical and lengthy as performed in [29] through a numerical method.

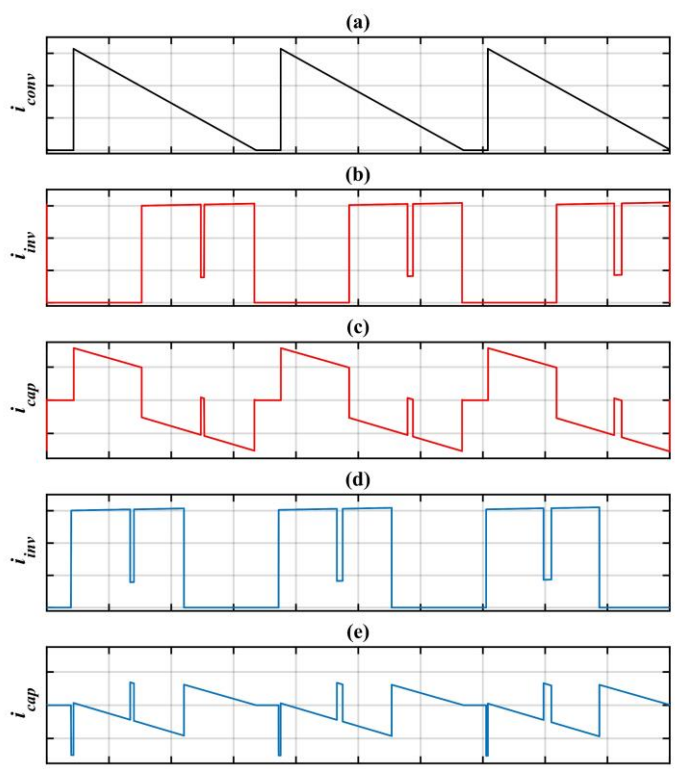


Figure 7-7. (a) i_{conv}, (b) i_{inv}, (c) i_{cap} without control synchronization. (d) i_{inv}, (e) i_{cap} after control synchronization.

However, because of its difficulty to solve, real-time implementation is not feasible. Although individually, i_{conv} and i_{inv} can be derived [30], the phase difference between them makes their subtraction non-trivial. To this end, an alternative method of solving the RMS current is proposed by looking at its relation to the charge the capacitor must process.

The DC-DC converter's role in the PCU is to transfer energy from the battery to the DC-link It is the responsibility of the inverter to transfer this energy towards the motor. Because the pattern of energy provided by the converter does not match the absorption into the inverter stage, the DC-link capacitor acts as a buffer or storage mechanism to balance the energy difference as shown in Figure 7-8. Since we can assume that the DC-link voltage is the same at the capacitor node, we can consider the charge to represent the energy.

For a given pulse of i_{conv}, the charge generated is given as:

$$Q_{conv} = 0.5 t_{off} I_{peak} \tag{5}$$

Since the phase shift φ moves i_{conv} to the first non-zero value of i_{inv}, the initial and last zero/seventh vectors can be ignored. Consequently, the D7, D5, D4, D0, D4, D5, D7 example sequence consumes the energy Q_{inv} as:

$$Q_{inv} = 2(S_5 I_{p1} + S_4 I_{p2}) \tag{6}$$

where I_{p1} and I_{p2} correspond to the inverter current peaks. The charge Q_{cap} denotes the change in charge that the capacitor has to process and is determined by $Q_{conv} - [(cos\varphi)Q_{inv}]$. Since I_{capRMS} is equal to the same current used to move charge and discharge the capacitor, it can be derived by:

$$I_{capRMS}{}' = \frac{2Q_{cap}}{t_{off}} \tag{7}$$

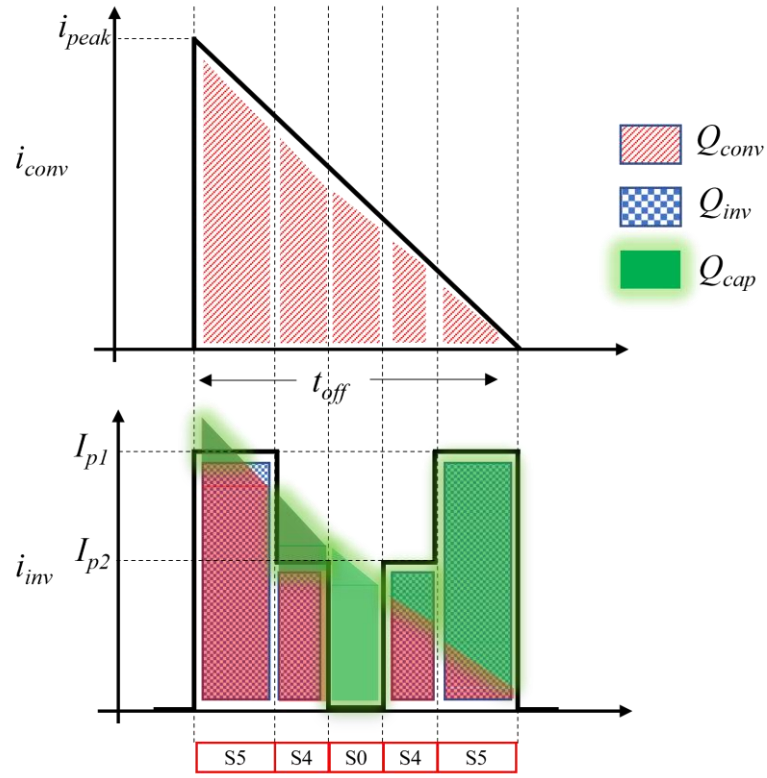


Figure 7-8. Representation of charge transfer from converter to inverter and capacitor storage mechanism.

where $I_{capRMS}{}'$ reflects the RMS value over the simultaneous switching activity of both converters. Over the entire period, I_{capRMS} is defined as $I_{capRMS} = I_{capRMS}{}'\sqrt{\frac{t_{off}}{T_{swconv}}}$.

7.6. Capacitance Requirement

To determine the volume reduction enabled by the implementation of the proposed control method, parameters around the DC-link capacitor selection must be established. Satisfying voltage ripple requirements for the system dictates that the minimum capacitance C_{min} defines the maximum allowable ripple on the DC-link voltage. This capacitance C_{min} can be determined as follows:

$$C_{min} \leq \frac{\Delta P_{nom}\, N_d}{2V_{DC} \cdot \Delta V_{DC}}\ , \tag{8}$$

where $\Delta P_{nom}$is the maximum allowable change in power over N_d switching cycles; and ΔV_{DC} the voltage ripple [31]. Typically, ΔP_{nom} is set to 40% over 10 switching cycles of operation. This capacitance value in conjunction with i_{capRMS} determine a suitable capacitor whose selection is done here by evaluating arbitrarily four manufacturer catalogs. A developed algorithm filters through the capacitors, determines the ones that meet the required voltage class, populating a custom database of potential options. Selection of the least number of capacitors to meet C_{min} and satisfy i_{capRMS} while minimizing volume is finally done to meet design needs. The database also extracts parameters paramount to deriving the operational hours as given by the capacitor lifetime model [32]–[34]:

$$Lifetime\ (hours) = L_b M_v 2^{\left(T_m - \frac{T_{HS}}{10}\right)}, \quad \text{with} \quad T_{HS} = R_{th} {i_{capRMS}}^2 R_{ESR} \tag{9}$$

where L_b, M_v and T_m are the capacitor rated lifetime hours, voltage rating ratio and ambient temperature; T_{HS} is the hotspot temperature given by the package thermal resistance R_{th} and capacitor ESR R_{ESR}. Figure 7-9 displays the comparison of the volume and lifetime hours without and with the implemented control method. Using equation (7) to determine the RMS current specification of the required capacitor across all the listed manufacturers, the control method realizes a potential 20% reduction. Similarly, for a given design, there is an opportunity to increase the lifetime hours of the capacitor by 25%, yielding higher reliability for long-term operation of the system.

7.7. PCU Implementation

The PCU with specifications listed in Table 7-1 was designed and built as shown in Figure 7-10. The input voltage reflects traditionally utilized levels for automotive applications [35]. Effective thermal management is needed to ensure that the switching devices and other heat generating components do not exceed their thermal limits. Using the 1.2-kV Wolfspeed XM3 SiC

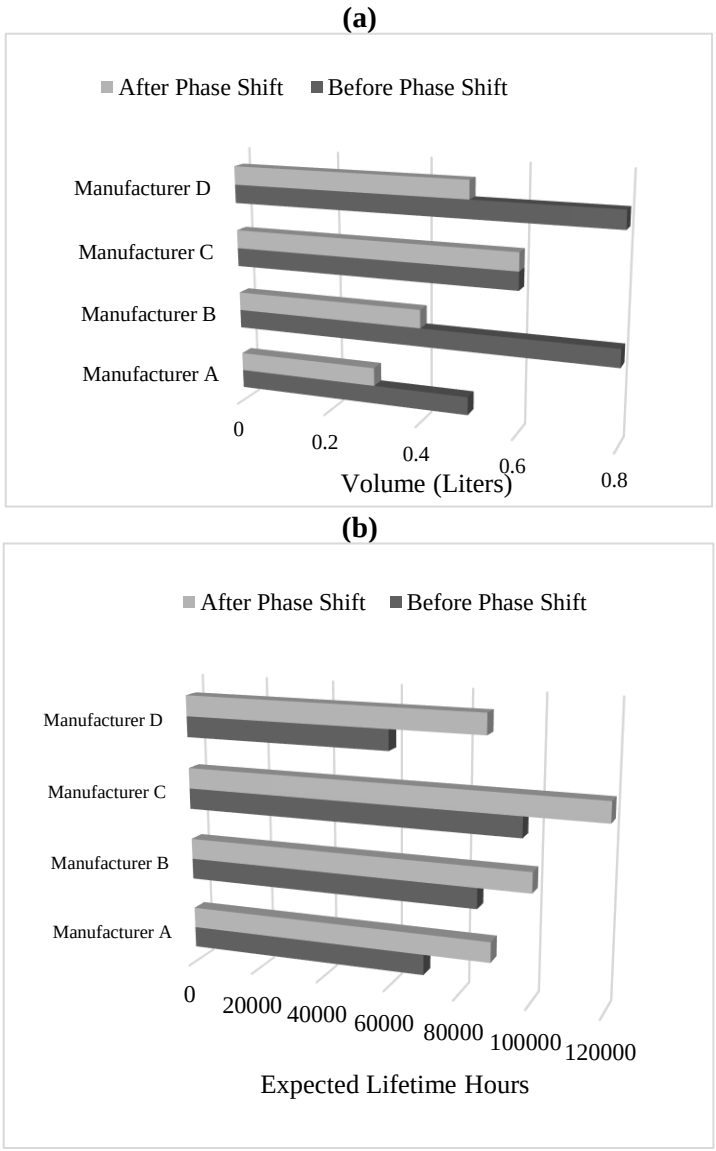


Figure 7-9. Volume and lifetime of the DC-link capacitors for the PCU prototype.

half bridges [36], a series-three back-to-back configuration allows for a symmetrical distribution of heat through a custom liquid cooling aluminum manifold and wells. The gate drivers used were Wolfspeed CGD12HBXMP. To minimize the overall system volume, the custom cold plate is double-side cooled, utilizing the entire length as the base for an encapsulated inductor and thus allowing for a reduced height [24].

Table 7-1: PCU Electrical Specifications

Parameter	Value
Nominal Power P_{nom}	50 kW
Input Voltage V_{in}	250-400 V
Max Output Voltage V_{out}	800 V
Switching Frequency f_{sw}	16.6 kHz
Ripple Voltage ΔV_O	1%
Inductance L	18 µH
Peak Current I_{peak}	≈ 250 A
Potting material thermal conductivity k_{pot}	10 W/mK
Output Capacitance C_o	120 µF

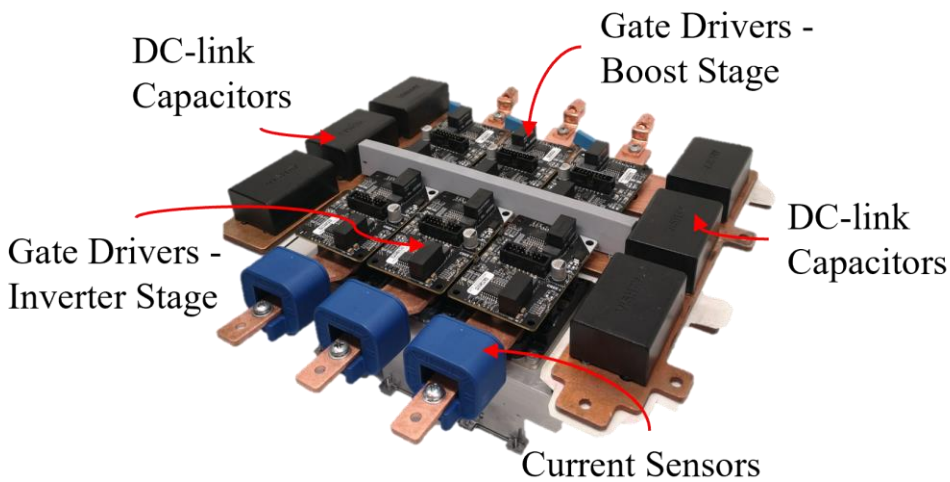


Figure 7-10. Assembled PCU prototype.

The DC-link capacitors sit atop an interleaved busbar structure insulated by Nomex 419 paper with high dielectric strength. Gate drivers are placed atop each half bridge horizontally, so as to not increase PCU volume. The entire converter volume with the given layout is 1.79 L, representing a power density of 55.6 kW/L at maximum power.

7.7.1. Thermal Management

To preserve the thermal integrity of the entire system at high power density, the thermal management architecture must be designed to sustain the rated power module loss related temperatures. Using the junction to case thermal resistance of 0.14°C/W and the lumped inductor thermal model per [37] applied for the inductor chosen for the design, an ANSYS Icepak™ simulation is performed to determine the required cold plate specifications so as to not exceed the module junction temperature of 175°C. The aluminum custom cold plate is modeled and is designed to house the six modules in two symmetrical rows for the power stage. The bottom side contains channels running the entire length of the cold plate equal to the width of each inductor's aluminum housing. Figure 7-11 shows the simulated model of the converter with 75 °C coolant temperature at 6 L/min flow rate. The maximum temperature at the rated losses of the converter obtained in the simulation is 159 °C observed at the SiC die. The observed potted inductor maximum temperature was 100.6 °C.

7.8. Simulation and Experimental Results

Demonstration of the validity of the control method and its implementation is done through a converter simulation and experiment under similar operating conditions listed in Table I. Using MATLAB/Simulink™, Figure 7-12(a) and Figure 7-12(b) show the current waveforms under

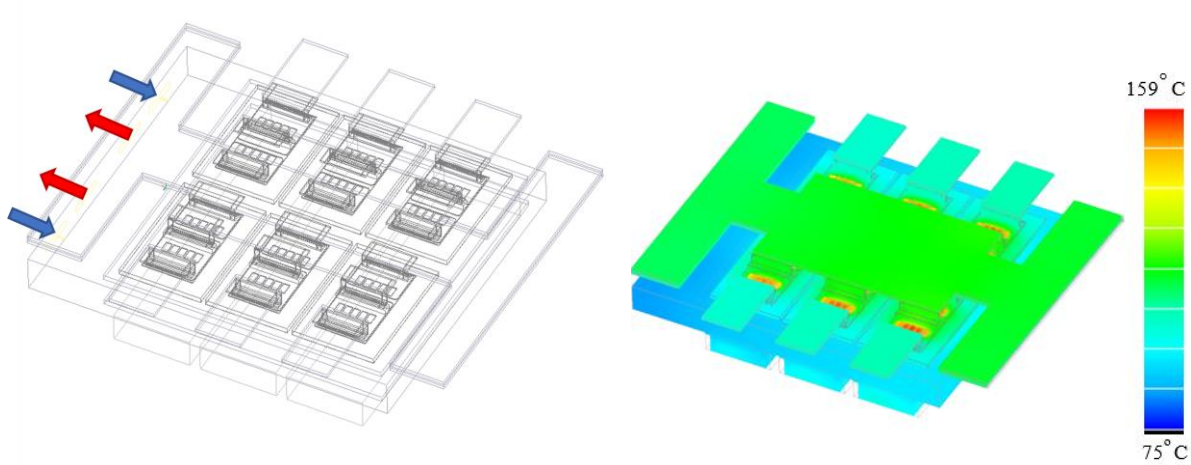
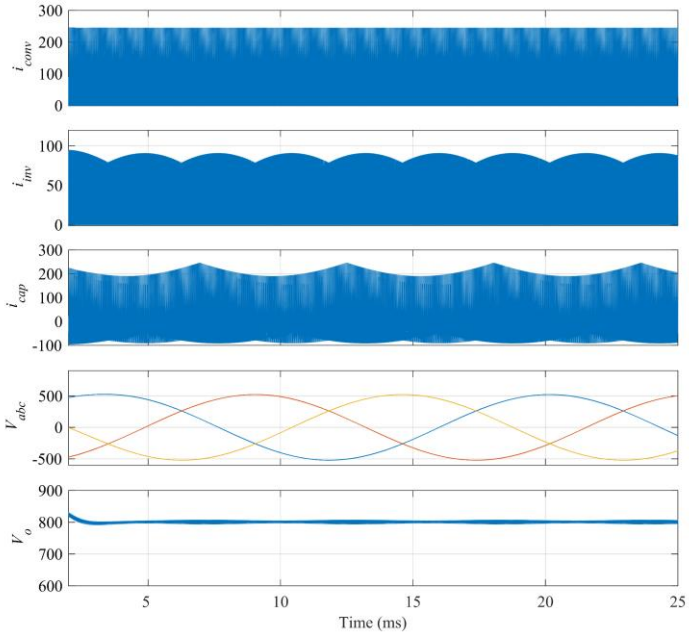


Figure 7-11. Thermal simulation of PCU under rated power.

(a)



(b)

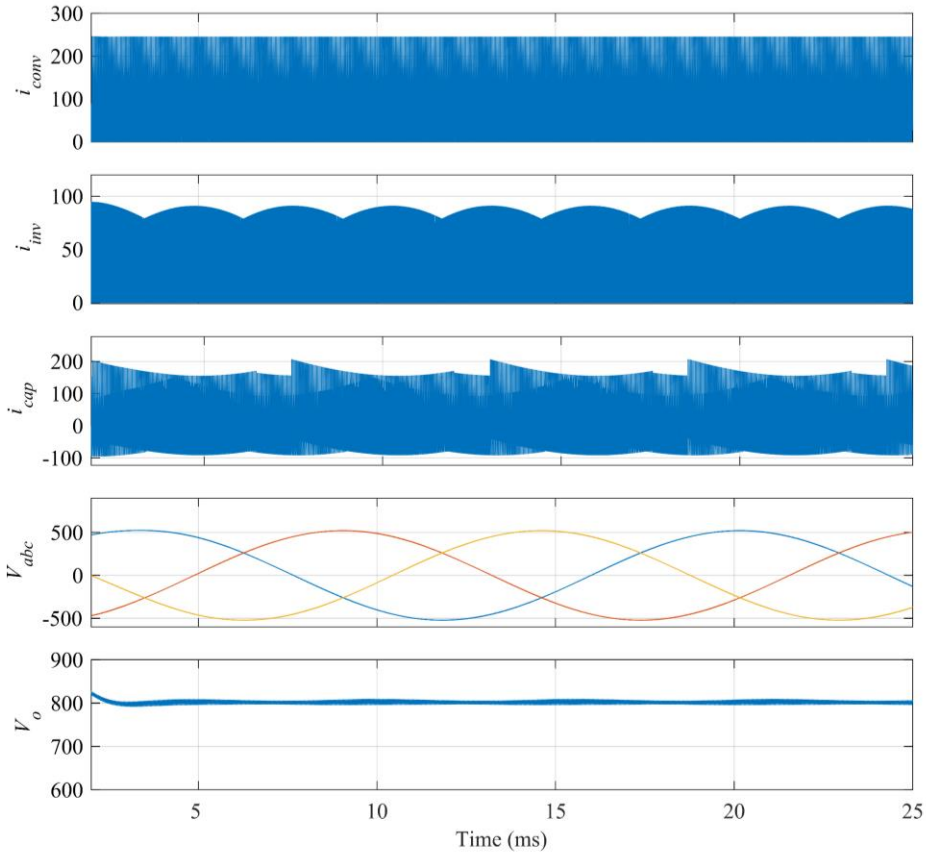


Figure 7-12. PCU simulation waveforms of i_{conv}, i_{inv}, i_{cap}, V_{abc} and V_o, of: (a) Converter without synchronization, and (b) with synchronization.

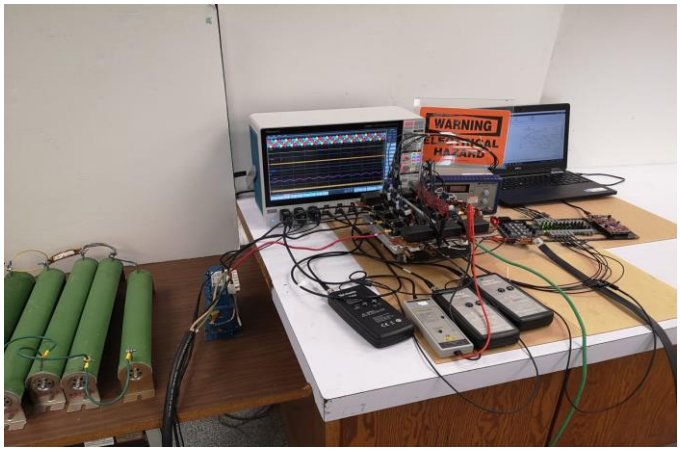
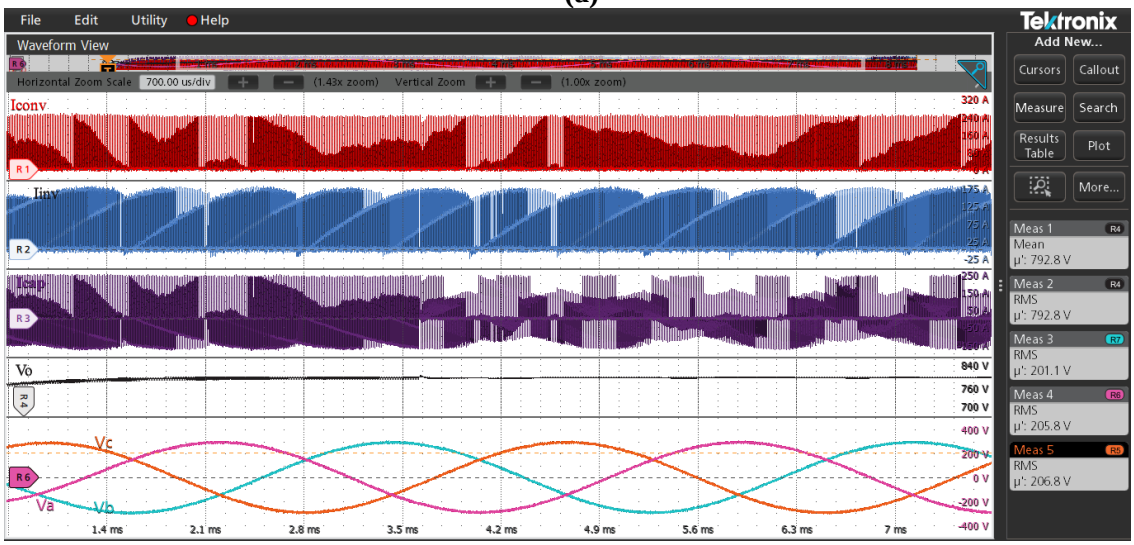


Figure 7-13. Experimental setup.

50-kW operation of the converter under unsynchronized and synchronized conditions when the active phase shift is applied, respectively. The current i_{cap} from Figure 7-12(a) to Figure 7-12(b) shows a ~25% reduction in the RMS current, from 132 A to 100 A.

For simplicity of observation of the capacitor current, one of the terminals of the capacitor soldered to the busbar is elongated to 2mm, to provide sufficient clearance for a Rogowski current probe to fit around the capacitor lead. The current observed is then multiplied by 12 to reflect the total current in the entire DC link capacitor (x2 for lead, x6 for number of capacitors). The experimental setup is shown in Figure 7-13 where the PCU was controlled using a TI F28379D Launchpad DSP system connected to the gate drivers via an array of fiber optic cables for radiated EMI immunity mitigation [38]. The cold plate is connected to a chiller to provide the heat exchange for the converter loss producing elements. Figure 7-14(a) shows the experimental waveforms corresponding to 35kW operation to safely demonstrate the phase shift. When unsynchronized, the resultant RMS current in the DC-link capacitor i_{cap} has a value of 87.6 A. However, there is a noticeable ≈29% reduction in i_{cap} with a value of 61.3 A when the control strategy is applied at 3.5ms. Figure 7-14(b) shows a zoomed in version of the waveforms under synchronous conditions.

(a)



(b)

Figure 7-14. Experimental results: (a) With synchronization applied after 3.5ms, and (b) Closer examination of waveforms under synchronization. Time scale: (a) 700μs/div; (b) 4μs/div.

The results in the experiment aligns with those of the simulation and proposed theory, satisfying the operational requirements of the converter and demonstrating the feasibility of the phase-shift method.

7.9. Conclusions

A control technique to minimize the RMS current in the DC-link capacitors through an active phase shift was theoretically deduced and experimentally validated. though the implementation

of a synchronized switching methodology encompassing a DC-DC converter and a DC-AC inverter. The proposed method effectively reduced the RMS current in the capacitor by 25 % in a 50 kW rated PCU compared to traditional unsynchronized PCU control, allowing for an average 20% smaller capacitor volume in the designed PCU. Additionally, the implementation of this control method can reduce thermal degradation of DC-link capacitors; thus, improving system lifetime by an average of 25 %. The overall system has a power density of 55.6 kW/L.

7.10. Acknowledgments

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CHAPTER 8

A 155 KW/L 800 V TRACTION INVERTER USING DISCRETE SIC DEVICES

8.1. Abstract

SiC power modules are typically considered for the construction of traction inverters due to provisions for cooling the module base plate and electrical isolation from the internal power devices. However, they are costly and occupy significant volume. In addition, the in-tandem supporting thermal architecture and energy storage (DC-link capacitor) are limited in mechanical layout to facilitate the module's typical planar electrothermal arrangement. This limitation in design freedom inhibits power density and cost pursuits for the overall system. Discrete-packaged semiconductors provide a flexible and cost-effective solution for scalable highly dense power electronics. Therefore, a new power electronic platform based on paralleled discrete devices and a hybrid material modular thermal management structure is presented for traction inverters. Placing capacitors within the unused volume of the thermal management structure enables higher power density for a 50 kW traction inverter (155 kW/L) and significantly reduces system cost.

8.2. Introduction

The surge in EV/HEV development has largely enabled the development of propulsion systems based on wide bandgap semiconductors [1]. In particular, SiC MOSFETs offer superior electrical switching performance due to negligible reverse recovery current and lower switching energy in comparison to Si IGBTs [2]. Possessing a higher thermal conductivity allows for reduced thermal

management profile, additionally increasing the system power density [3]. As such, there are numerous examples of SiC adoption within traction inverters in both literature and industry [4]–[6]. Typically, SiC half-bridge power modules are considered for realizing traction inverters due to convenience for cooling through the base plate and electrical isolation from the die [7]. The layout of power module-based inverters has been primarily driven by the electrothermal relationship in the constructions of the power module and cold plate. The latter is typically a monolithic cooling structure upon which the power module baseplate transfers heat. The gate drivers are normally placed atop of the modules. It is from this platform that the integration of the DC-link capacitors must be determined. Hence, the passive components are placed external to this electrothermal structure, utilizing more volume. Additionally, the bus bar structure essential for making electrical connections must follow this asymmetrical planar structure to mitigate parasitic effects. However, because of these combined features, power modules and their co-dependent thermal management structures are often bulky and expensive.

The use of smaller ampacity-rated discrete devices offers a cost-effective alternative to power modules [8]. However, they are typically limited to a 100 A. Therefore, realizing an equivalent power-module-based automotive traction inverter requires paralleling several discrete devices, but it is a cost effective option. This paper presents a systematic approach for designing a 50 kW, two-level traction inverter with a 800 V DC bus using a novel segmented electrothermal platform which incorporates parallel discrete SiC devices. The inverter is designed to surpass the DOE 2025 goal on power density for power electronics [9]. The operating characteristics of the inverter are given in Table 8-1.

Table 8-1. Traction Inverter Specifications

Parameter	Value
Rated Power P_{nom}	50 kW
Peak Power (15s) P_{peak}	125 kW
DC-link Voltage V_{DC}	800 V
Line to Line Voltage V_{L-L}	480 L-L
Switching Frequency f_{sw}	>15 kHz
Coolant Temperature T_c	105 °C
Power Density	155 kW/L
Voltage Ripple ΔV_{DC}	5%

8.3. Design Method for a Traction Inverter using Discrete SiC Devices

For the given targets in Table 8-1, the design method begins by the selection of the appropriate discrete devices. The peak line current in a single phase of the inverter output is given by $I_L = P_{peak}/(\sqrt{3} * V_{L-L} * 0.9)$ where an arbitrary power factor of 0.9 is considered. This value determining the required current rating of the half-bridge position is calculated to be 133 A for the system specifications. It is favorable for cost and system complexity to realize I_L with as few discrete devices as possible. To maintain a high system efficiency to aid with thermal management and battery utilization [10], it is important to consider the turn-on and turn-off energies $E_{on}$and E_{off} of the devices at rated operating temperature, alongside $R_{DS(ON)}$ which determines conduction losses [11]. Therefore, taking into account the matrix of I_L, E_{on}, E_{off} and $R_{DS(ON)}$, Wolfspeed C3M0016120D 115A 1.2kV TO-247 package offers competitive system efficiency and current carrying capacity with only two devices needed per switching position.

The influence of the asymmetrical circuit layout is often overlooked, even though the effects of the circuit parasitic parameters on a single device have been well investigated in the literature [12]–[14]. Using impedance matching symmetrical traces for the gate signals, and duplicating layer pours for the DC-link to reduce loop inductance, the four-layer PCB half bridge in Figure 8-1(a) is designed such that the device package is attached to that PCB at a right angle, so the

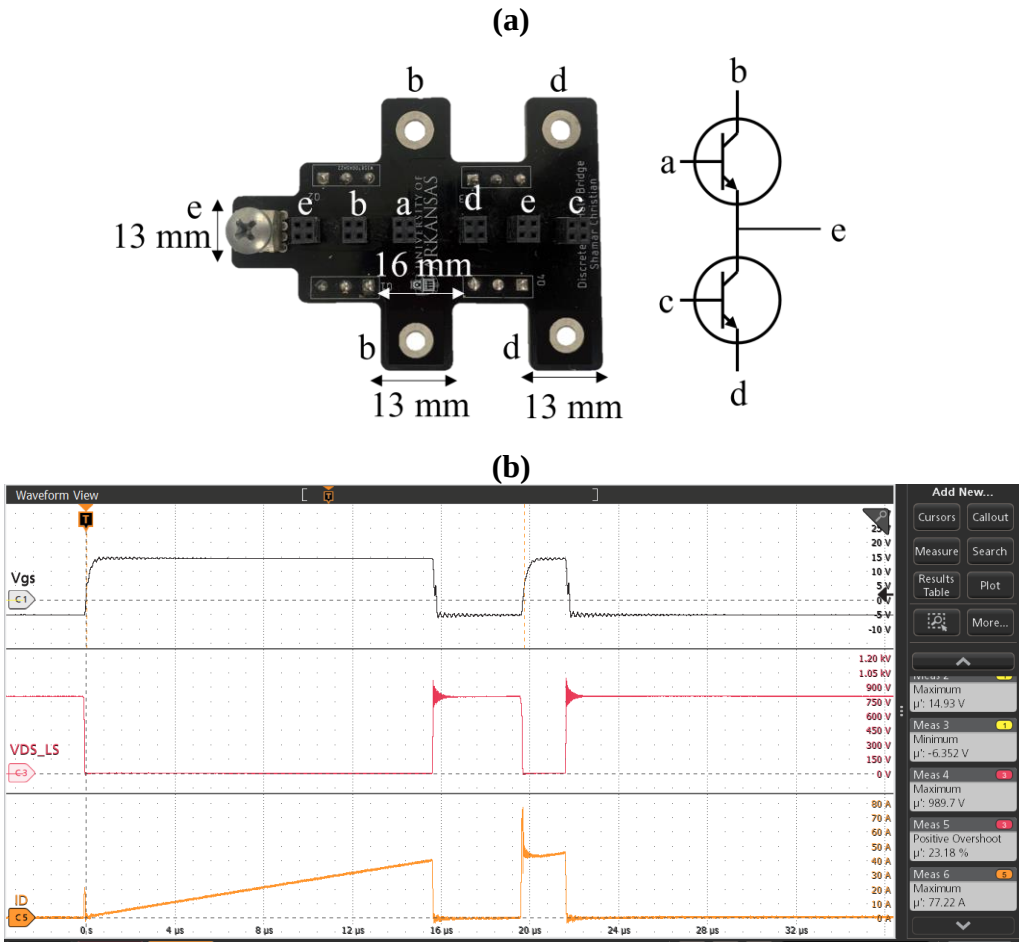


Figure 8-1(a). Half-bridge PCB layout, and (b) Double pulse test results at 800 V 100 A.

electrical bussing can be implemented horizontally in each layer, and the thermal management can be treated vertically. This PCBs hold four discrete SiC MOSFETs and meet IPC-221A and IPC-222B standards for voltage isolation with 4 oz. copper for current density. Using these metrics, the minimum required copper trace is 51.3 mm for a 175°C temperature rise under peak current ratings. For a four-layer PCB, this width can be divided equally to conserve space. Therefore, the terminal “b”, “d” and “e” widths for connecting to an interconnecting dedicated DC-link PCB similarly designed for connections to the capacitor connections and DC source, and also the half-bridge midpoint of the PCB is 13 mm. The spacing between the devices is 16 mm as determined by the thermal constraints regarding coupling [15] and anticipated heat flux. Figure 8-1(b)

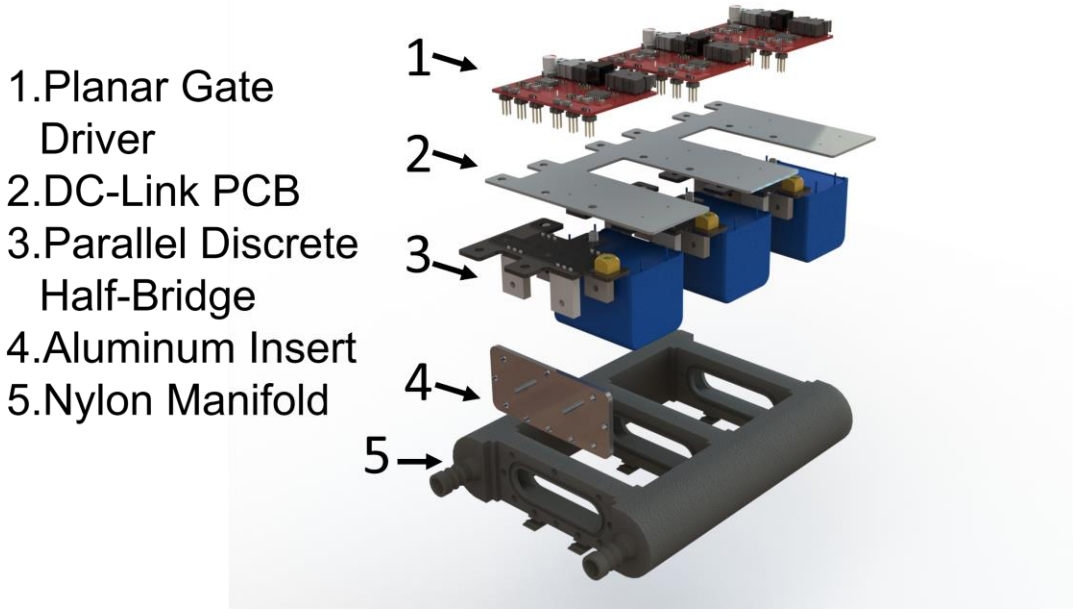
illustrates the resultant double-pulse test at 800 V where the DC-bus overshoot of 990 V is well within the device limit. Performing the test at 100 A which translates to 50 A per device, the maximum transient on-state current for a single device was 77 A which is acceptable for the package rating.

The capacitance required must satisfy ripple voltage and rms current requirements based on Table 8-1. Classical equations for the required capacitance and capacitor RMS current in [16] can be used to determine the capacitor specifications. Anticipating a 30% change in P_{nom} over 10 switching cycles, the required capacitance is determined to be 117 uF with a 40.5 A_{RMS} rating. Three TDK EPCOS 40 µF 1.2kV capacitors (x3) with 21.5 A_{RMS} ripple current ratings are therefore appropriately selected for the system. They are soldered to the DC-link PCB board and slot in between the thermal manifold housing. The designed gate drivers are based on Wolfspeed's CGD15SG00D2 design [17] with a planar orientation for reducing volume and sit atop the DC-link PCB.

8.4. Inverter Layout with Discrete Devices

With the power electronic platform established, the thermal management architecture must be developed so that the device junction temperature does not reach its maximum limit. A hybrid additive manufactured (AM) cold plate depicted in Figure 8-2 is realized by team members with the POETS NSF ERC at the University of Illinois-Urbana Champaign. The AM manifold made from Nylon 12 guides the coolant to finned aluminum heat sinks which interface with the power devices. Thermally conductive electrically isolating AlN sheets isolate the devices from the assembly. Because the manifold only distributes liquid to the critical areas of heat exchange, 43% of the volume of the manifold can be removed. This not only reduces material use and mass of the thermal structure but allows for the DC-link capacitors to be integrated into the space that would

(a)



(b)

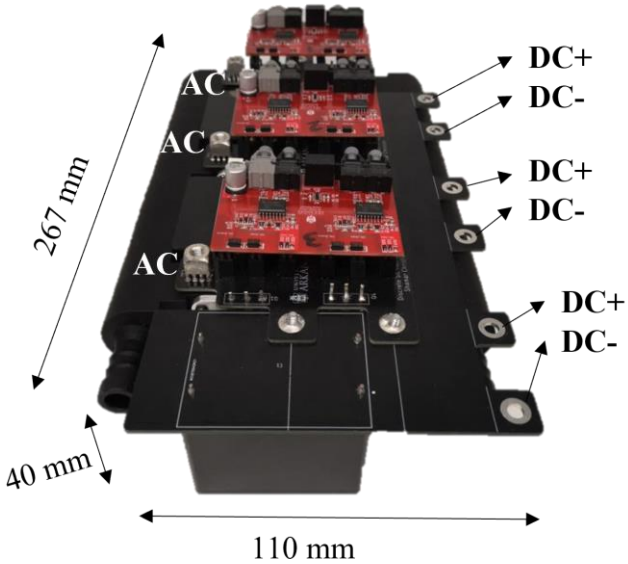


Figure 8-2. (a) Exploded view of inverter, and (b) Photograph of inverter prototype.

be normally occupied by free space. Figure 8-2(a) shows an exploded view of the system illustrating the main components. Figure 8-2(b) depicts the full construction, respectively. The DC-link capacitors are soldered to the separate DC-Link PCB from the half bridge PCBs with ample spacing. This spacing is determined by 110 % of the sum of the following widths: 35 mm

standard width of the capacitor package, 5.21 mm of the width of the two TO-247 devices and 11 mm width of the insulating AlN plate. The DC source is connected at three separate points to achieve better current distribution and minimize parasitic inductance [18].

8.5. Experimental Results

A continuous power test is done for the inverter prototype connected to a resistive-inductive (RL) load bank (R = 2.5Ω; L = 1 mH). The gate signals were generated by a TI F28379D DSP connected to the gate drivers using fiber optic cables via an in-house interface board. The cold plate is connected to a chiller to provide heat exchange for the inverter. The phase current and voltages are captured into an oscilloscope. Figure 8-3 shows the experimental setup. Figure 8-4 presents the experimental line currents waveforms of the inverter operating under full load with a

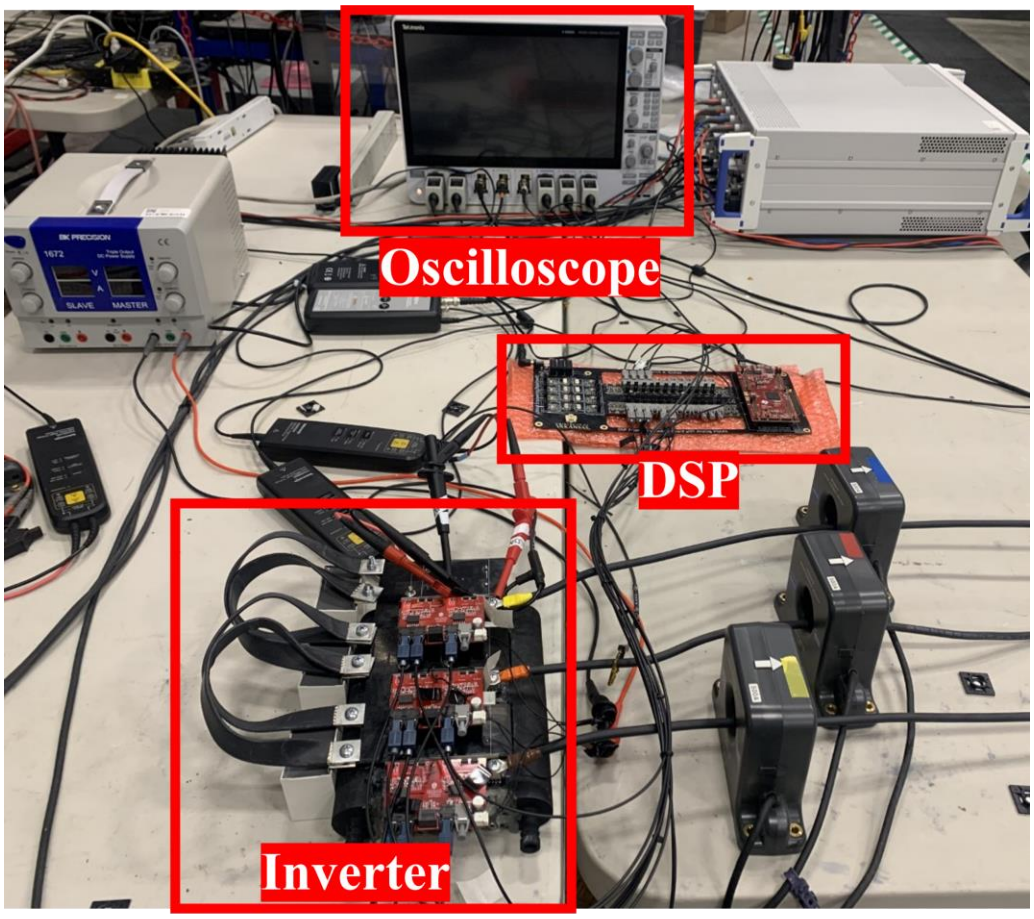


Figure 8-3. Experimental setup.

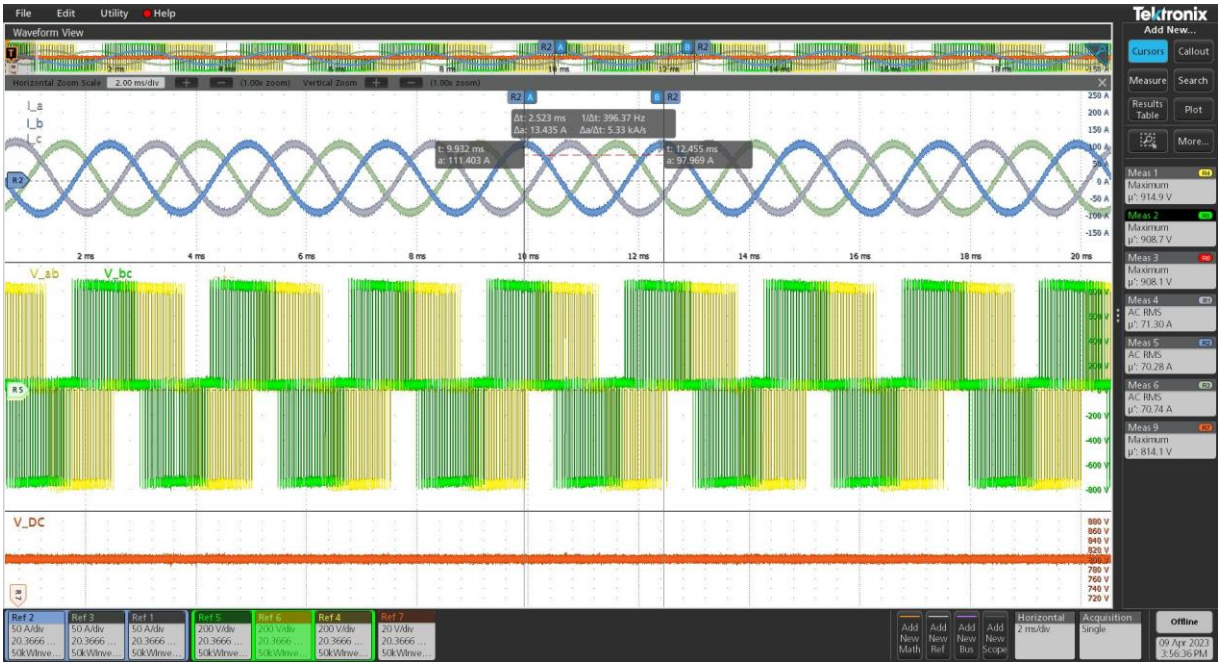


Figure 8-4. Experimental waveforms of the inverter. Time scale: 10 ms/div; Vertical scales: 50 A/div, 200 V/div and 20V/div.

0.9 modulation index. Two line-to-line output voltages V_{ab} and V_{ac} are measured before the RL load and shown to validate three phase operation. Testing at 50 kW and a fundamental frequency of 400 Hz, the maximum voltage of 914 V on the line-to-line voltage is within the 24% percentage overshoot margin experienced on the double pulse test for a 800 V bus voltage.

Thermal validation of the inverter is done using a FLIR thermal camera and thermocouple insertion at each device case. Due to safety considerations for the operator, thermal images cannot be captured while the converter is operating at full power. Therefore, validation takes place by shorting the phase legs of the inverter to a high current source, dissipating Ohmic losses to mimic P_{peak} loss conditions (100 W per device). Figure 8-5 shows the resultant temperature of a single position under duress, comparing the infrared images to an inserted thermocouple. With the additional thermal resistance of the AlN spacer and thermal interface material, the hybrid cold plate ensured that the discrete device operated at an equilibrium temperature of 110°C which is far below its 175°C junction maximum temperature. The system experiences robust thermal

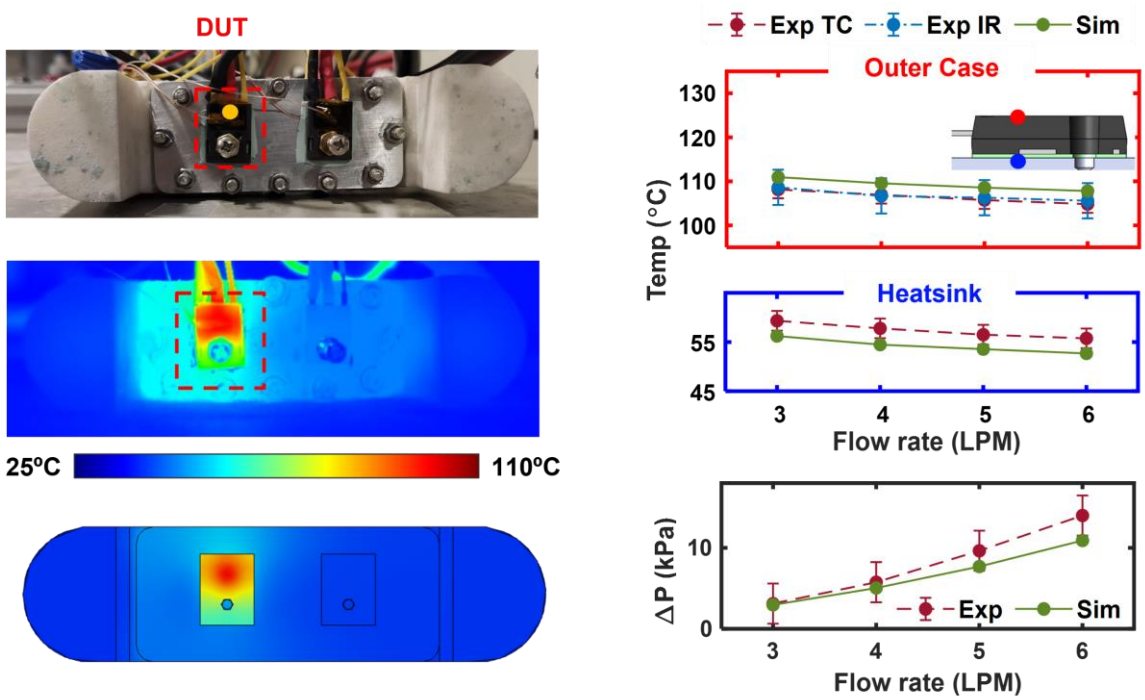


Figure 8-5. Inverter thermal validation test results.

performance even at flow rates of 3 LPM. This can lead to advantages in pumping costs for the system as the pressure drop is significantly lower at low flow rates. The obtained temperatures from the thermal camera and the thermocouple show very strong correlation to that of the simulated performance in Figure 8-5.

8.6. Conclusions

A 50 kW traction inverter was designed, built and successfully tested using parallel discrete SiC devices. The inverter featured a novel hybrid thermal management structure comprised of Nylon 12 3D printed manifolds with aluminum inserts capable of handling the large heat fluxes of the discrete devices at low flow rates. The capacitors were embedded within the space of the phase manifolds to minimize volume. The low inductance PCB design facilitates even current sharing in

the devices with low overshoot and was experimentally validated at 800 V. The 50 kW inverter has a power density of 155 kW/L.

8.7. References

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CHAPTER 9

CONCLUSIONS AND RECOMMENDED FUTURE WORK

9.1. Conclusions

This dissertation comprehensively addressed considerations required for increasing the power density of PCUs for automotive applications. For meeting the DOE's 2025 Roadmap target in power density to accelerate EV development, it was important to identify the bulky components and the resultant contributing systems that may impede reaching the goal. To this end, the most voluminous components were firstly identified within the topology; i.e., the boosting inductors and DC-link capacitors between the DC-DC converter and traction inverter. They are addressed below.

9.1.2. Inductor Volume Reduction

Beginning with the inductors, the composition and construction of the magnetic structure was defined so that its footprint could be reduced without compromising material temperature limits. Typical design methods involve a multidomain tradeoff mechanism largely based on fitting design requirements to commercially available pre-sized cores. Here, a non-tradeoff inclusive design methodology for custom-core magnetics based on the development of a set of design equations was developed [1]. It allowed for the selection of only the core dimensions and the turn numbers for the windings that best accomplish the magnetic specifications. The design made use of nanocrystalline cores and was validated using a transformer as a design scenario. The 150 kW 20 kHz rated transformer demonstrated a 99.73% efficiency with a 13 L total volume.

9.1.3. Increasing Efficiency at Low Power Levels

Because larger inductances typically require more turns on a magnetic core, therefore increasing system volume, it was essential to address the control mechanisms that dictate the necessity for larger inductance values. Within the boost converter stage, traditional CCM stipulated by fixed frequency PWM control techniques require a bulky inductor. Additionally, the switching devices undergo hard switching, which especially reduces efficiency at a low-power-levels where the most battery demand takes place. This was addressed in the dissertation through the implementation of a ZCS-DCM variable switching frequency control methodology [2]. This strategy not only lowered the required inductance value in designing the converter for power density, but also enabled a fairly constant efficiency of 96% over the system entire power range. This was demonstrated experimentally in an 80 kW DC-DC 55.6 kW/L boost converter. With the improved efficiency at low power levels, research is needed to determine how these benefits can translate to a possible reduction on the battery pack size, or improvements on additional mileage range for the EV.

9.2. Capacitor Size Reduction

Linking the DC-DC stage with the traction inverter requires a DC-link capacitor bank to supply the instantaneous current to supply the electric motor and to decouple the inductive effects from the DC converter to the switching phases [3], [4]. Trends increasing switching frequency were pursued by improved switching device characteristics. This reduced the energy storage requirements and, therefore, the volume in passives. However, the capacitor sizing requirements are mainly determined by its RMS current, which is the dominant factor when selecting an appropriate capacitor. By synchronizing the switching sequences of the two power stages such that there is as much current cancelation as possible flowing through the capacitor, the RMS current is reduced by 30%. For an 80 kW rated PCU, it was discovered that this reduction permitted an average 20% volume reduction across four capacitor manufacturers in the selection stage of the

design method. Because of the correlation between the cycling RMS current and internal degradation of the capacitor [5], the theoretical lifetime hours of operation under this synchronous control method was increased by 25%.

9.3. Power Density Gains in Converter Layout

Subsequent research involved considering the overall platform from which the converter was designed. Replacing the half-bridge power modules with discrete devices offered advantages in system cost as explored in [6]. However, the necessary electrothermal platform to bind together the electrical benefits with thermal performance for standardized discrete packages was not explored for feasibility within EV applications. Therefore, this dissertation presented a hybrid cold plate architecture for discrete devices, in which the thermal management and electrical connections were separated into perpendicular planes. The hybrid structure not only effectively cooled the devices below their junction limit, but also allowed for the embedding of the DC-link capacitor among the inverter phases enabling extremely high-power density. This work results in the design and testing of a 50 kW 155 kW/L traction inverter.

Figure 9-1 illustrates the progressive improvements in power density that has been accomplished in the prototypes within this dissertation. Building upon previous research efforts within POETS at the University of Arkansas in 2018 [7], [8], the inverter prototype presented in this dissertation has surpassed the DOE's 2025 target of 100 kW/L by 55%. Additionally, the PCU and boost converter stages have bettered the DOE target of 33 kW/L by 68%.

9.4. Recommendations for future Research Work

Further gains in power density can be potentially obtained by considering several systemic factors for the PCU. For example, extending the discrete platform proposed in Chapter 8 of the dissertation to fabricate a PCU, such as the one shown in Figure 9-2, allows for the embedding of

both capacitors and encapsulated inductors within the volume of the cold plate resulting in a hypothetical 90 kW/L PCU.

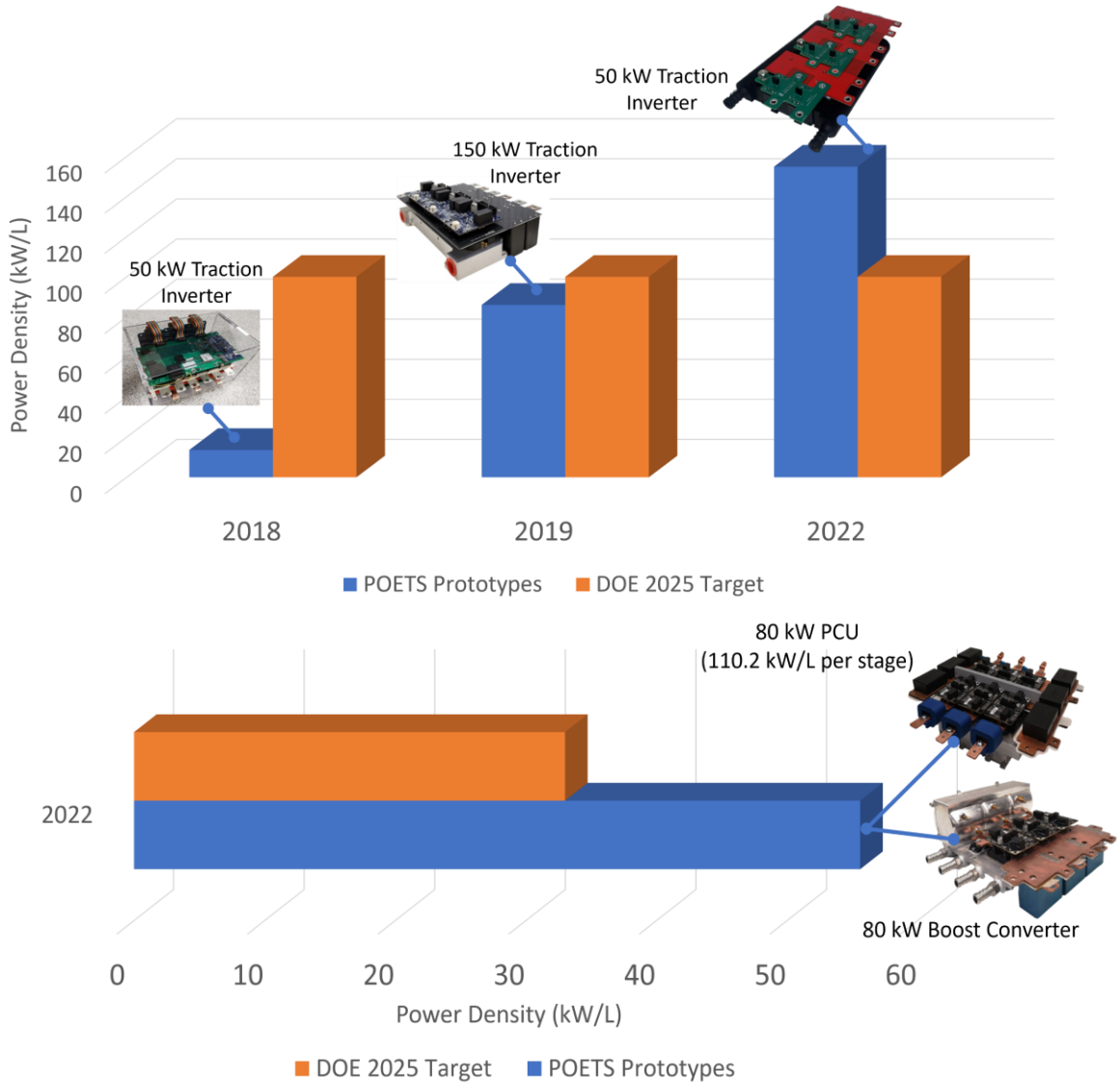

Figure 9-1. University of Arkansas improvements in PCU power density.

Assessing the PCU on the basis of its power electronic components, breakthrough in specific technologies can greatly contribute to increasing both power density and performance. Improvements in capacitor construction to reduce both ESL and ESR can take advantage of faster

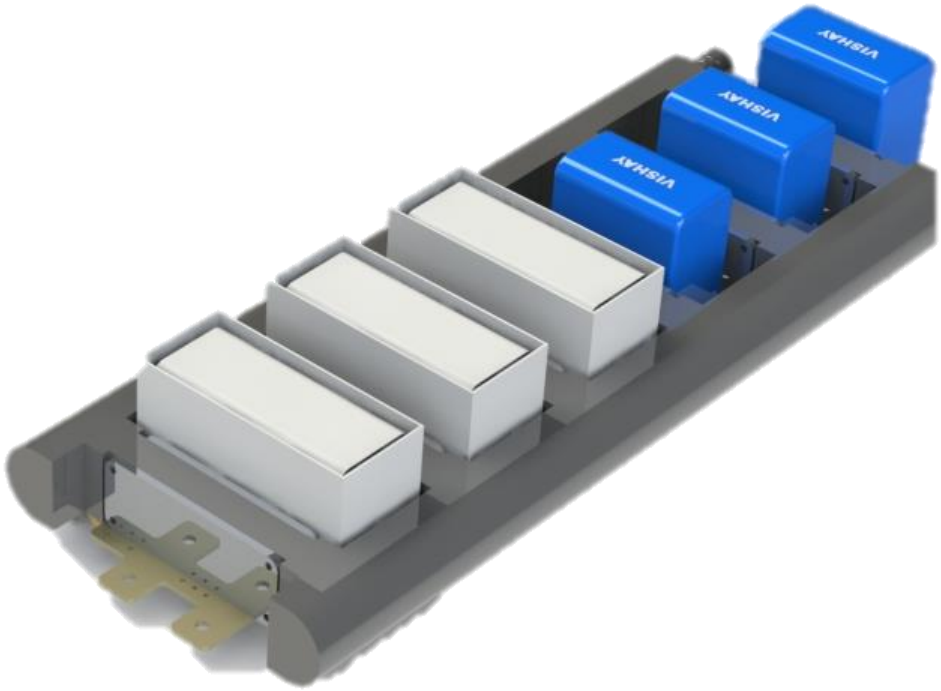

Figure 9-2. Rendition of a discrete SiC PCU using the platform in Chapter 8.

switching speeds and lower Ohmic heating. Reference [9] highlights that an improvement on the capacitor dielectric enables smaller packaging, resulting in significant power density gains. Additionally, the pin-style termination of most compact film capacitors lacks sufficient surface area to dissipate the internal heat. Broadening these terminals to form tabs or planar structure as a simple solution could decrease the ESR of the capacitor or equivalently, facilitating much better dissipation into the busbar/PCB bussing.

Thermal management for high power converters will always play a vital role in the determination of system volume. The smaller device footprints and higher heat fluxes will demand interfaces with high thermal conductivity and cold plates with lower thermal resistance. Pin-fin based cold plates and thermal inserts show great potential for reducing thermal resistance. However, there is need for advanced research in the metal processing and material usage to make it viable at scale.

Most switching devices whether discrete or power module, offer unidirectional heat extraction through the baseplate located at the bottom. Double-sided devices with virtually half the thermal resistance can dissipate much more heat-related loss as opposed to conventional ones. Systems can be operated with much higher power levels with more current to boost power density. Nevertheless, current commercial double-sided devices are limited to IGBTs and have yet to be commercialized at meaningful ratings for SiC. A CAD rendition of a traction inverter using the Infineon FS200R07A02E3 HybridPak six-pack IGBT module with double-sided cooling is shown in Figure 9-3. The design of the cooling structure coupled with the tight integration of the DC-link capacitors and gate driver array lends itself to modularity for ease of paralleling inverters to multiply the power output of the total inverter system.

This dissertation addresses PCUs in which there is an intermediate DC-DC stage. However, current commercial realizations of PCUs only have a traction inverter [10]. The current implementations leverage the possibility of using a larger 800 V battery for fast charging [11], along with a significantly reduced component count. However, the larger battery has a larger mass and cost association. Having the DC-DC stage allows for a smaller 400 V battery to decrease weight, but the increased component count incurs additional system cost with slower charging

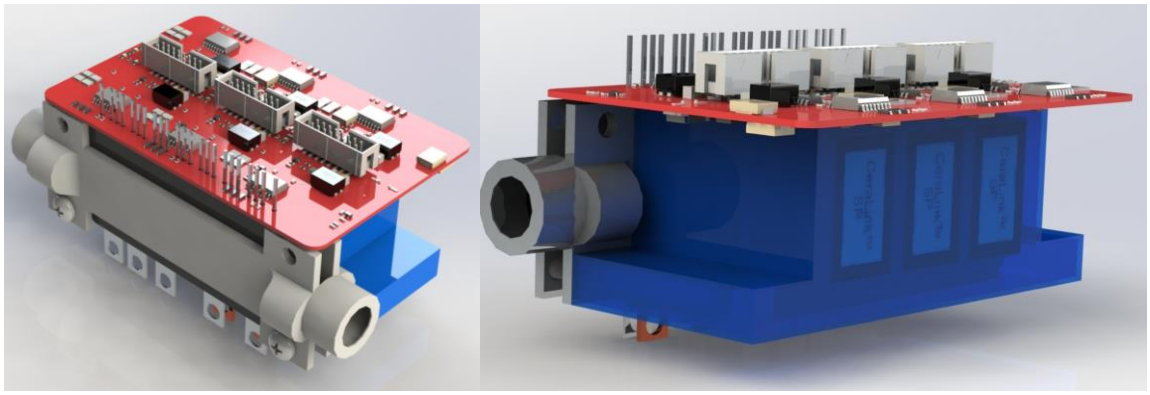

Figure 9-3. CAD display of a traction inverter featuring double-side cooling.

capability. A system level cost analysis would be required to contrast and compare between both architectures to determine profitability for manufacturers.

9.5. References

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