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A low-noise, wide-band CMOS charge-sensitive preamplifier for use with a cadmium zinc telluride strip detector in a high-resolution small animal x-ray CT system

Lemuel Herbert Thompson

To the Graduate Council:

I am submitting herewith a thesis written by Lemuel Herbert Thompson entitled "A low-noise, wide-band CMOS charge-sensitive preamplifier for use with a cadmium zinc telluride strip detector in a high-resolution small animal x-ray CT system." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Theron Vaughn Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Michael Paulus, J. M. Rochelle

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

To the Graduate Council:

I am submitting herewith a thesis written by Lemuel Herbert Thompson entitled "*A Low-Noise, Wide-Band CMOS Charge-Sensitive Preamplifier for use with a Cadmium Zinc Telluride Strip Detector in a High-Resolution, Small Animal X-ray CT System.*" I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

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and recommend its acceptance:

James M. Rochelle

Albert P. Pisano

Accepted for the Council:

Carolyn R. Winkler

Associate Vice Chancellor and
Dean of the Graduate School

A Low–Noise, Wide–Band CMOS Charge-Sensitive Preamplifier for use with a Cadmium Zinc Telluride Strip Detector in a High-Resolution, Small Animal *X-ray* CT System

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Lemuel Herbert Thompson II

August 1999

DEDICATION

This thesis is dedicated to my parents,

Mr. JM Thompson

and

Mrs. Patsy R. Thompson

who have always done their best to make every opportunity possible available to me.

ACKNOWLEDGEMENTS

This project could not have been completed without the support of several friends and colleagues to whom I am most grateful. I would like to thank Dr. Michael Paulus for being a wonderful mentor both before and during this project. I would also like to thank my major professor, Dr. T.V. Blalock, not only for his support during this project, but for his excellent teaching in analog electronics during my undergraduate career at UTK, which inspired me to make analog electronics my career choice. I would like to thank Dr. J.M. Rochelle for both serving on my thesis committee, and for his enthusiasm and effort in making my graduate electronics classes as full and enriching as possible. Thanks are due also to Kevin Behel for our many helpful conversations as we struggled through the MicroCAT project together.

I would also like to thank my many friends, colleagues, and professors both at the University of Tennessee and at the Oak Ridge National Laboratory who have given me wonderful support and encouragement during this project. I only hope that I have returned the favor equally to them. I am also grateful for Oak Ridge National Laboratory and University of Tennessee's Joint Program in Mixed Signal VLSI and Monolithic Sensors, which sponsored my graduate work at UTK.

I would like to thank my family members who have encouraged me throughout my childhood and college career. I also would like to thank Donald and Lynda Gillon, for their everlasting encouragement and support, without which I may not have entered college at all. Finally, I would like to thank Donna Thompson for her support and friendship during this stressful time.

This research was sponsored by the Laboratory Directed Research and Development Program of the Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corp. for the United States Department of Energy under Contract No. DE-AC05-960R22464.

ABSTRACT

A low-noise, wide-band CMOS charge-sensitive preamplifier has been designed for use with a Cadmium Zinc Telluride (CZT) strip detector in the Oak Ridge National Laboratory's (ORNL) MicroCAT small animal x-ray CT imaging system. The characteristics of the CZT strip detector have been studied to optimize the design of the preamplifier, and are presented herein. The design of the charge-sensitive preamplifier (CSP) is discussed in detail, and test results are presented and discussed. The CSP was found to have a 10 – 90 % rise time of 23 ns, a charge gain of 3.06 x 10^{12} $^{V}/_{C}$, a dynamic range of + 0.9 V and – 2 V, and an equivalent input noise of 13 $\frac{nV}{\sqrt{Hz}}$ at 1 kHz and 2.2 $\frac{nV}{\sqrt{Hz}}$ at 1 MHz. The CSP coupled to an Ortec 571 shaping amplifier has an Equivalent Noise Charge (ENC) minimum of 400 rms electrons for unipolar shaping at peaking time of 14 μs with a 4 pF detector capacitance. The system, with the same configuration, has an ENC minimum of 550 rms electrons for bipolar shaping at the zero crossover of 15 μs. The prototype preamplifier has been fabricated in the AMI 1.2 μm process through the MOSIS microelectronics prototyping program.

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Chapter 1 Introduction

1.1 MicroCAT Overview

1.1.1 Historical Background

Shortly after World War II, the Oak Ridge National Laboratory (ORNL) established an animal genetics program to study the biological effects of ionizing radiation on mammals. The experiments of this program, which all involved the study of induced mutations in mice, provided the data upon which assessments of human risk following exposure to ionizing radiation are based. As a result of this program the Oak Ridge colony is now the largest experimental mouse colony in the world, and houses more than 70,000 mice representing about 400 mutant strains [1]. ORNL has recently identified the area of Functional Genomics to be the next significant challenge in genome research. The goal of this program is to determine the function of each gene in the mouse genome.

Each time a mutagenesis experiment is performed, the mice must be screened for the presence of mutations. The probability of obtaining a mouse with a phenotype of interest is less than 0.2%, which means to find a mouse that exhibits a phenotype of interest, over 500 mice must be screened. The screening process currently depends on a physical examination and a behavioral analysis of each mouse. Thus, the screening process is both time consuming and costly. For subtle phenotypes, such as abnormal organ development, the mouse must be sacrificed in order to determine if it exhibits the desired phenotype. Obviously once the mouse has been sacrificed it can not be studied further.

A program to develop a high-resolution, high-throughput, low cost small animal imaging system was recently initiated by ORNL in 1997 in order to increase the accuracy and to decrease the time of the mouse examinations. The initial goals of the system were to provide a data acquisition time of one minute or less, and to provide a nominal structural image resolution of about 50 μm Full Width at Half Maximum (FWHM) with sensitivity to both skeletal and soft tissues. The first task in the mouse imaging program was to identify the optimal imaging modality for mouse scanning.

1.1.2 Comparison of Scanning Modalities

For the purpose of high-resolution medical imaging, there are three dominant modalities [2]. These are *x-ray* computed tomography (*X-ray* CT), nuclear medicine, which includes positron emission tomography (PET) and single photon emission tomography (SPECT), and magnetic resonance imaging (MRI).

1.1.2.1 X-ray CT

X-ray CT utilizes a narrow beam of *x-rays* that pass transversely through the test subject. This produces one-dimensional projection data in the form of detected *x-ray* intensity, I_d, along the axis of the *x-ray* path. The *x-ray* source is then rotated by a small angle and projection data is taken on that axis. The process is repeated until projection data has been acquired for 180 degrees of rotation around the subject. The one-dimensional data sets are combined mathematically using a filtered back projection algorithm [3] to construct a two-dimensional image that represents a transverse "slice" of

the subject (Figure 1.1). Three-dimensional images can then be constructed by 'stacking' the two-dimensional slices.

X-ray CT offers several positive qualities. These are (1) high resolution, (2) short data acquisition times (from one second to less than an hour), (3) low cost, and (4) excellent distinction between soft and hard tissue, and recent research indicates the ability to obtain good quality soft-tissue contrast images [4]. The most apparent disadvantage of *x-ray* CT is the use of ionizing radiation to obtain the image projection data.

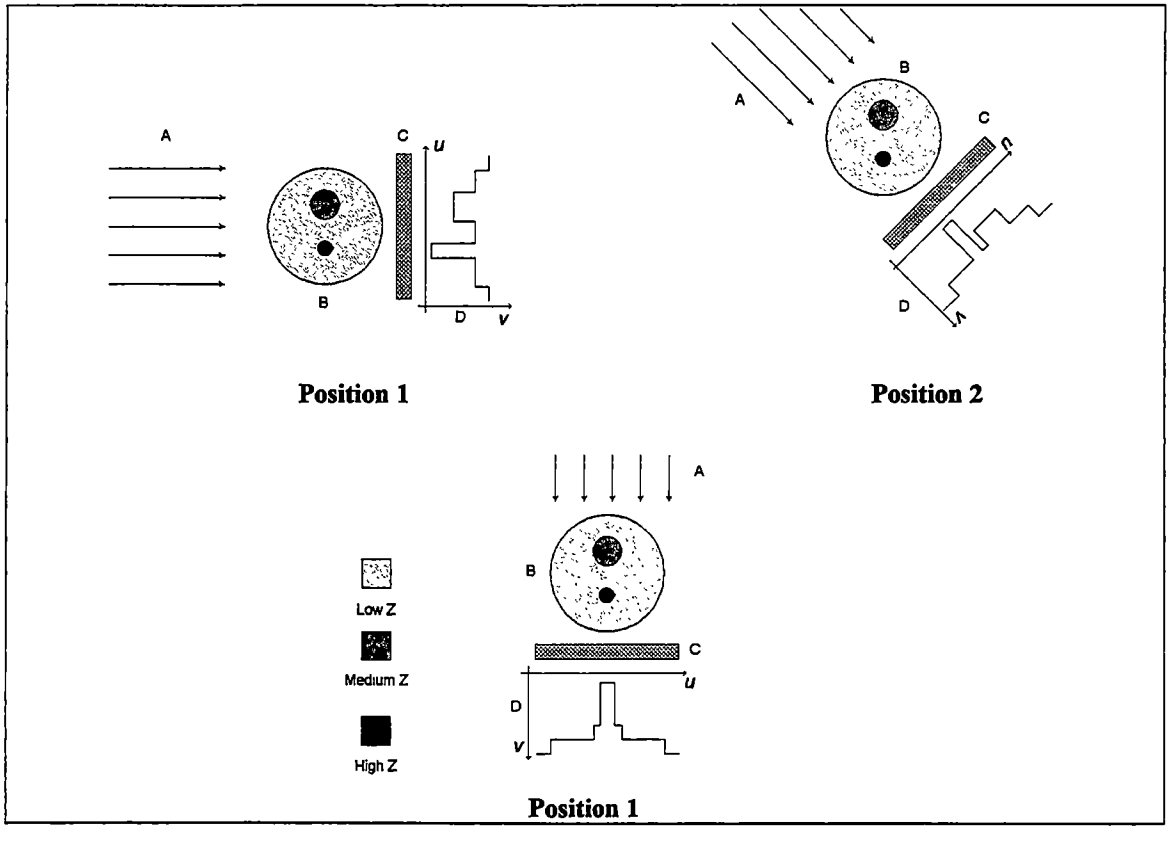


Figure 1.1: *X-ray* CT projection data acquisition A) X-rays, B) Subject, C) Detector and D) Attenuation data

Figure 1.2 illustrates a typical human brain scan done with the *x-ray* CT modality. Note the sharp contrast between the bone of the skull and the soft tissue of the brain.

1.1.2.2 Nuclear Medicine

Nuclear medicine technologies employ tracer compounds that are injected into the subject prior to the imaging process. The tracer compounds either emit gamma rays (*γ-rays*), as in the case of SPECT, or positrons that annihilate with nearby electrons to produce *γ-rays*, as in the case of PET.

In the case of SPECT a *γ-ray* emitting compound is tagged to a metabolically important chemical. This tracer compound is selectively taken up in the tissue to be imaged. The emitted *γ-rays* are collected via collimated detectors that rotate around the subject. Only the *γ-rays* that travel along the axis of the collimator will contribute to the image (Figure 1.3). The projection data set from each detector is combined using reconstruction algorithms to produce two-dimensional images that represent "slices" of the subject.

In a PET system, positron-emitting tracers are tagged to a metabolically important compound, which is injected into the subject prior to the scanning process. As in the case of SPECT, the compound is selectively taken up in the tissue of interest. The positron, a particle that has the same mass as an electron but with a positive charge, is emitted and collides almost immediately with an electron. Both the electron and the positron are annihilated and two γ-rays, each with energy of 511 keV, are emitted at a 180 degree relative angle. Thus, the detection of two γ-rays simultaneously at 180 degrees apart indicates an emission of a positron (Figure 1.4).

Figure 1.2: Typical *x-ray* CT image of a human brain [10]

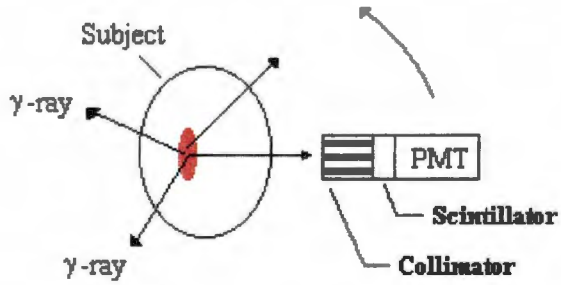


Figure 1.3: SPECT gamma ray collection technique

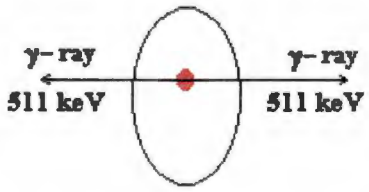


Figure 1.4: PET gamma ray emission

Unlike *x-ray* CT, nuclear medicine (PET, SPECT) provides a means to monitor metabolic activity rather than anatomic structure. However, it has several disadvantages: (1) a radioactive tracer must be injected into the subject prior to imaging, (2) the resolution is limited to several mm, (3) the cost is high, and (4) the data acquisition time is long (often longer than an hour). For example, research performed at UCLA with their microPET small animal positron emission tomography system has provided images with less than 2mm FWHM spatial resolution of ^{18}F-FDG uptake in a monkey brain [5]. The acquisition time reported was approximately one hour. Figure 1.5 illustrates a human brain scan, performed with a PET system. Note that only the tissues that absorb the tracer compound are imaged.

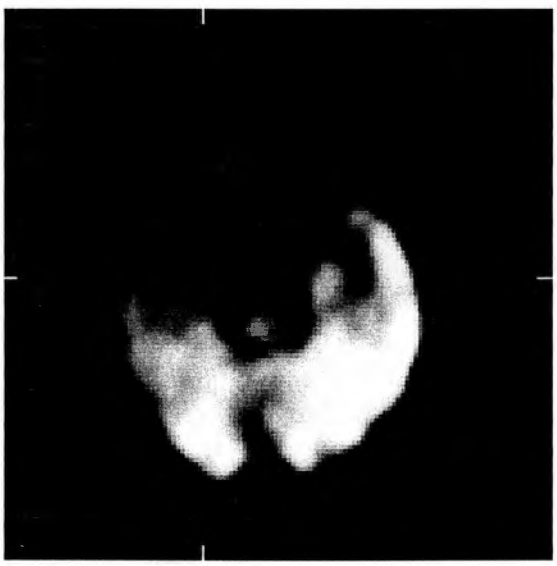


Figure 1.5: Typical PET image of a human brain [7]

1.1.2.3 Magnetic Resonance Imaging

The basis of MRI is the presence of nuclei with unpaired nucleons (neutrons or protons), the most abundant being the protons (nucleus of the hydrogen atom) found in water within the tissue. These unpaired nuclei posses a magnetic moment that arises from the angular momentum of the "spinning" nuclei. An MRI scan requires three basic steps. First a large, steady magnetic gradient is imposed across the subject. The unpaired nuclei align with the magnetic field lines and begin to precess, similar to a toy top motion when placed upon a pedestal, around the axis of the magnetic field lines in a steady state. The resonant frequency of the precession is a function of the imposed magnetic field strength, which is typically on the order of one Tesla (T), but can be as high as 16 T for higher resolution images [6]. This precession causes the emission of an electro-magnetic signal that can be detected if a significant number of nuclei are precessing at the same frequency. Next, radio waves that are tuned to the specific resonant frequency of precession are used to stimulate the subject in order to disrupt the steady state precession. The precessing nuclei absorb the energy of the applied radio waves, and when the radio waves are stopped the nuclei release the energy over a period of time, termed the *relaxation rate*. The relaxation rate, which is a function of water density and tissue specific parameters, is detected and measured using a specialized probe giving a projection data set along the axis of the magnetic field. A two-dimensional image can then be produced from the projection data sets. The gradient of the applied magnetic field allows individual "slices" of the subject anatomy to be extracted since the resonate frequency of precession is dependent on the magnetic field intensity (Figure 1.6).

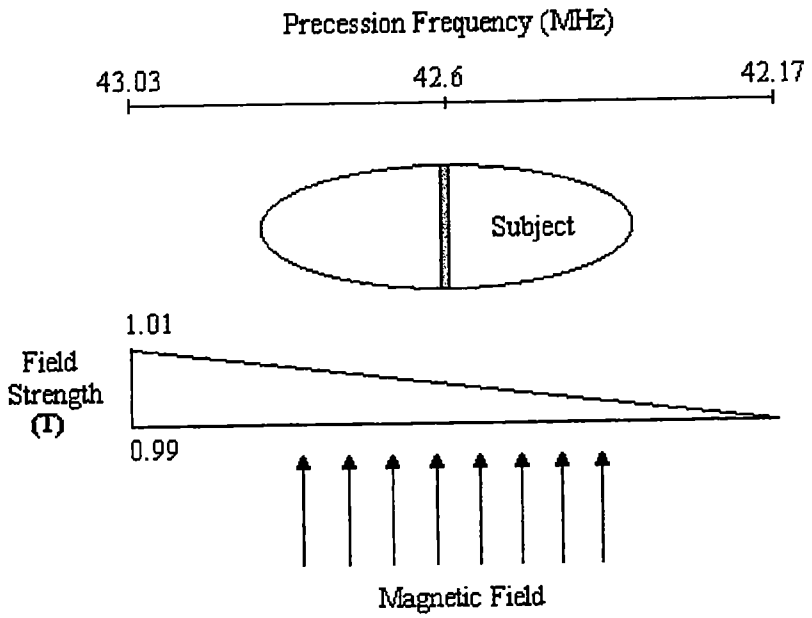


Figure 1.6: MRI modality

MRI presents several advantages, the most prominent being the lack of ionizing radiation and the potential for excellent high resolution soft tissue detection. Tissues can be characterized in several ways and since MRI is more sensitive to tissues with a larger concentration of water, bone tissue, which is roughly 30 percent water, does not interfere with the imaging process. The disadvantages of MRI are (1) long scan time for high-resolution images (more than an hour typically), (2) low resolution when compared to *x-ray* CT, and (3) high cost of the system. MRI small animal imaging has been reported by the Duke University Center for In Vivo Microscopy [6]. This research reports a data acquisition time of approximately two hours. A typical MRI human brain scan is shown in Figure 1.7. Note the absence of the bone, and the high resolution of the soft tissues.

Figure 1.7: Typical MRI human brain scan [7]

1.1.3 Scanning Modality Selected

Based on the project requirements of high-resolution, high-throughput and low-cost, *x-ray* CT was the imaging modality chosen for this application. In addition to the aforementioned advantages of *x-ray* CT, since the maximum energy to be used in the *x-ray* CT system is low (50keV), a SPECT imaging modality may be added to the scanner, thus, making it a dual-modality imaging system. The proposed *x-ray* computed tomography system consists of five major components, the *x-ray* source, the *x-ray* detector, the signal processing electronics, the mechanical structure and a dedicated work station that executes a system control program, stores the *x-ray* attenuation data and executes the image reconstruction algorithms. In the following sections all of these major components are described. A general illustration of the miniature *x-ray* CT system is shown in Figure 1.8.

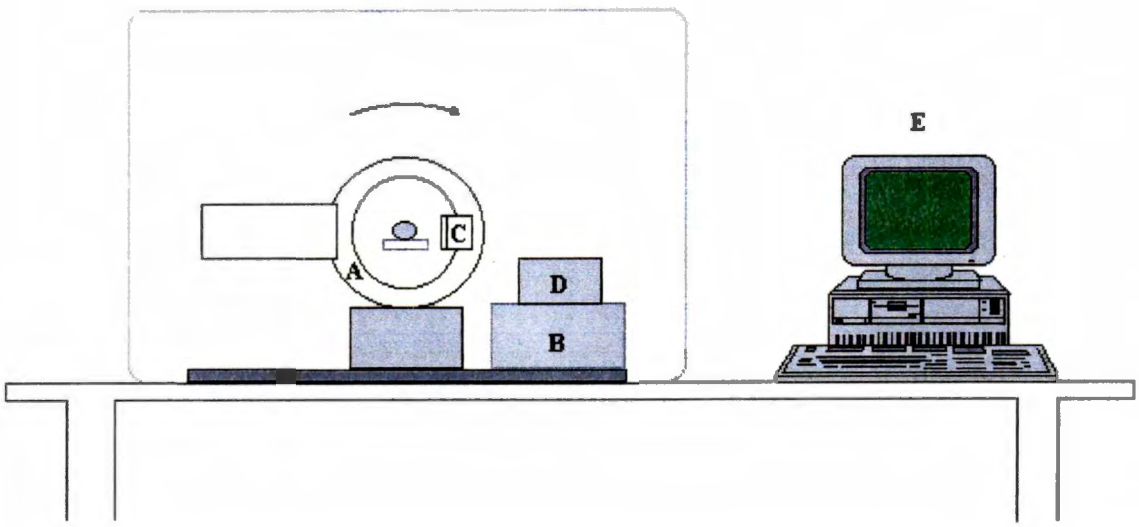


Figure 1.8: Diagram of the MicroCAT system illustrating A) the rotating gantry B) the motion controllers C) the detector D) the low-noise electronics and E) dedicated work station

1.2 Description of System Components

1.2.1 X-ray Source

The *x-ray* source used in this project is a 50 Watt, side-windowed *x-ray* tube (part # XTF5011) manufactured by Oxford Instruments, Inc. The glass envelope is packaged in an oil-filled, lead-lined housing that provides *x-ray* shielding to 0.25 mR/hr at 2 inches. The window is Beryllium (Be, Z=4) with a thickness of 10 mils, and the target is Tungsten (W, Z=74). The tube is powered by a 50 kV, 1mA power supply (series XRM) manufactured by Spellman High Voltage Electronics Corporation. A cutaway drawing of the *x-ray* tube is presented in Figure 1.9 [8].

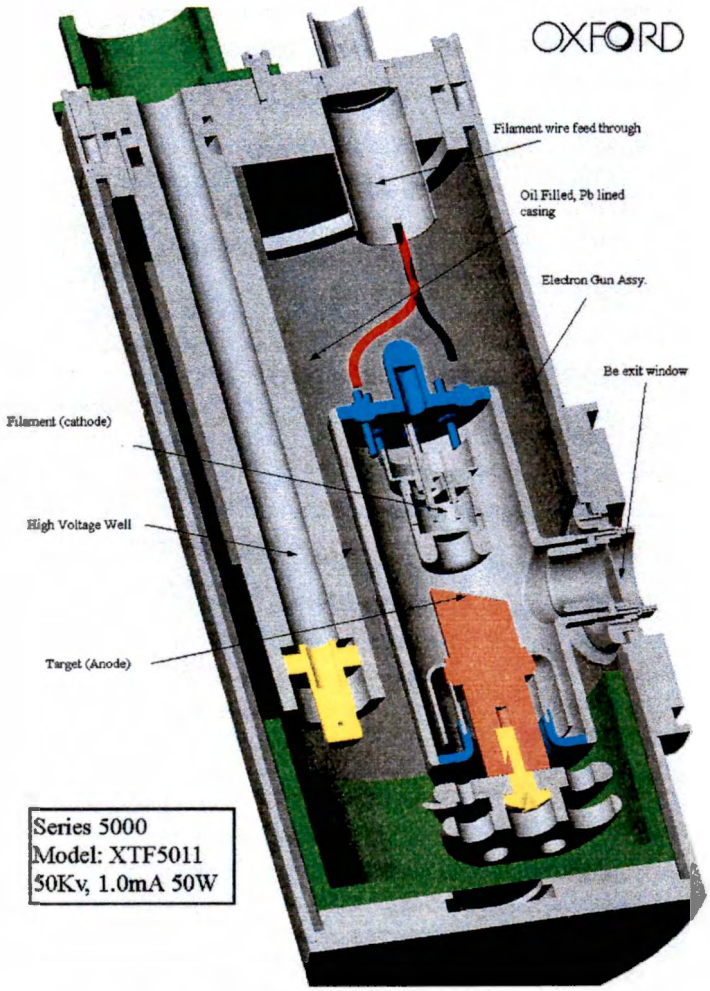


Figure 1.9: Oxford series 5011 *x-ray* tube [8]

1.2.2 Detector

The detector used in this project is a custom Cadmium Zinc Telluride (CdZnTe or CZT) strip detector manufactured by eV Products. The detector body measures 12 mm by 12 mm by 2 mm, and the top and bottom surfaces are patterned with orthogonal 100 μm wide strips on a 200 μm pitch. Each surface has 42 strips that are flared out at each end to allow room for the bonding pads, so that the central area of the crystal measures 8.2 mm by 8.2 mm. The detector is mounted to a substrate with 21 pins per

side for a total of 84 pins, and each strip is wire bonded out to a pin (Figure 1.10). No other electronics are included on this device. CZT properties are further discussed in Chapter 2.

1.2.3 Signal Processing Electronics

Each strip of the detector is connected to a custom analog electronics channel that converts the collected charge from the detector to a voltage signal. The electronics channel allows not only for the counting of x-ray collection events but also the measurement of the energy of each event. Each x-ray incident on the detector will produce between 2,000 and 10,000 electron hole pairs in the detector. The charge carriers then drift (in the presence of an electric field imposed by an applied voltage bias) to the surfaces of the detector. The charge is collected from the strip by a charge sensitive preamplifier, which converts the charge to a voltage signal with useful amplitude. The preamplifier provides inputs to a shaping amplifier and a timing discriminator. The timing discriminator detects the occurrence of an event and prepares the sample-and-hold circuit for the capture of the shaping amplifier's output signal. The decoding logic determines which channels have detected signals and connects them to an analog-to-digital converter (ADC). Both the digitized data and the address of the signal-bearing channel are stored by the dedicated work station. A schematic block diagram of two electronics channels is shown in Figure 1.11.

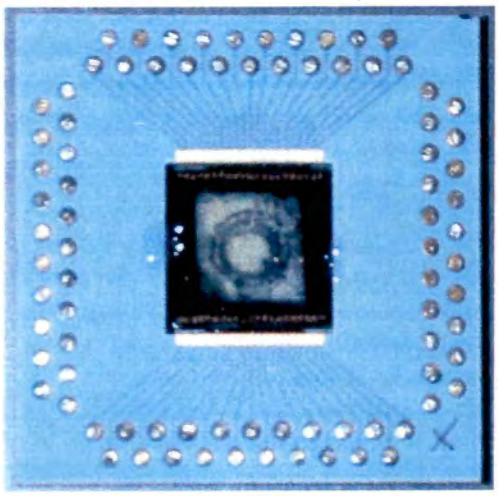


Figure 1.10: Cadmium Zinc Telluride Strip Detector

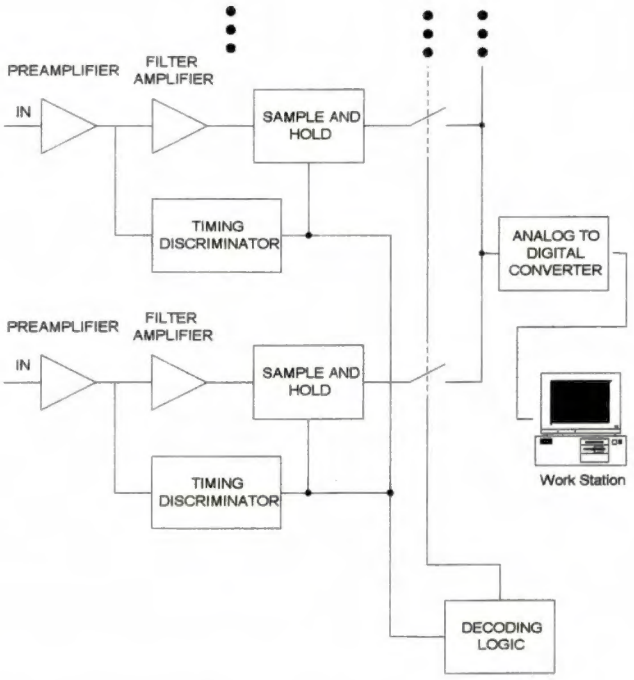


Figure 1.11: Schematic block diagram of two channels of the signal processing electronics

1.2.4 Mechanical Structure

The scanner mechanical structure (Figure 1.12) consists of a rotating gantry, a translating subject bed, a translating detector mounting assembly, support table and a lead lined enclosure. Rotation of the gantry and translation of the bed and detector assemblies is accomplished using stepping motors and motor controllers. The subject support is made of low-density balsa wood, so that its interference with the imaging process is minimized. Several safety features were incorporated into the system. (1) When the *x-ray* tube high voltage power supply is powered, a red light is illuminated on the front of the machine. (2) The enclosure doors are equipped with safety interlock switches so that the *x-ray* tube is disabled if a door is opened. (3) A main disconnect switch is located near the operator's work station, and (4) the side of the machine nearer to the operator's work station is lined with stainless steel.

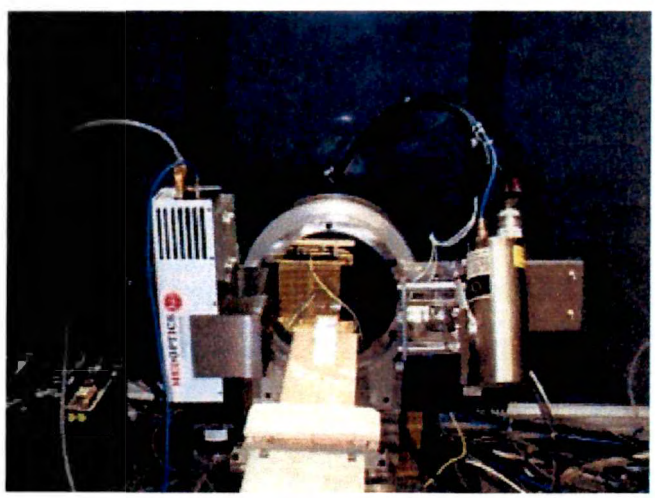


Figure 1.12: Mechanical Assembly of the MicroCAT system [9]

1.2.5 *Dedicated Work Station*

The computer used for this project was assembled by Gateway. It has a Pentium II, 300 MHz processor, over 45 Gigabytes of hard disk storage space and the operating system is Windows NT. The system control program was written using the LabWindows CVI application building software. The system control program manages all of the imaging setup parameters, such as x-ray tube power, stepping motor motion, safety interlocks, and data collection documentation. This interface also allows direct access to the image reconstruction software module. Thus, a subject can be scanned and the image reconstructed and viewed in a matter of only a few minutes. The operator interface is shown in Figure 1.13.

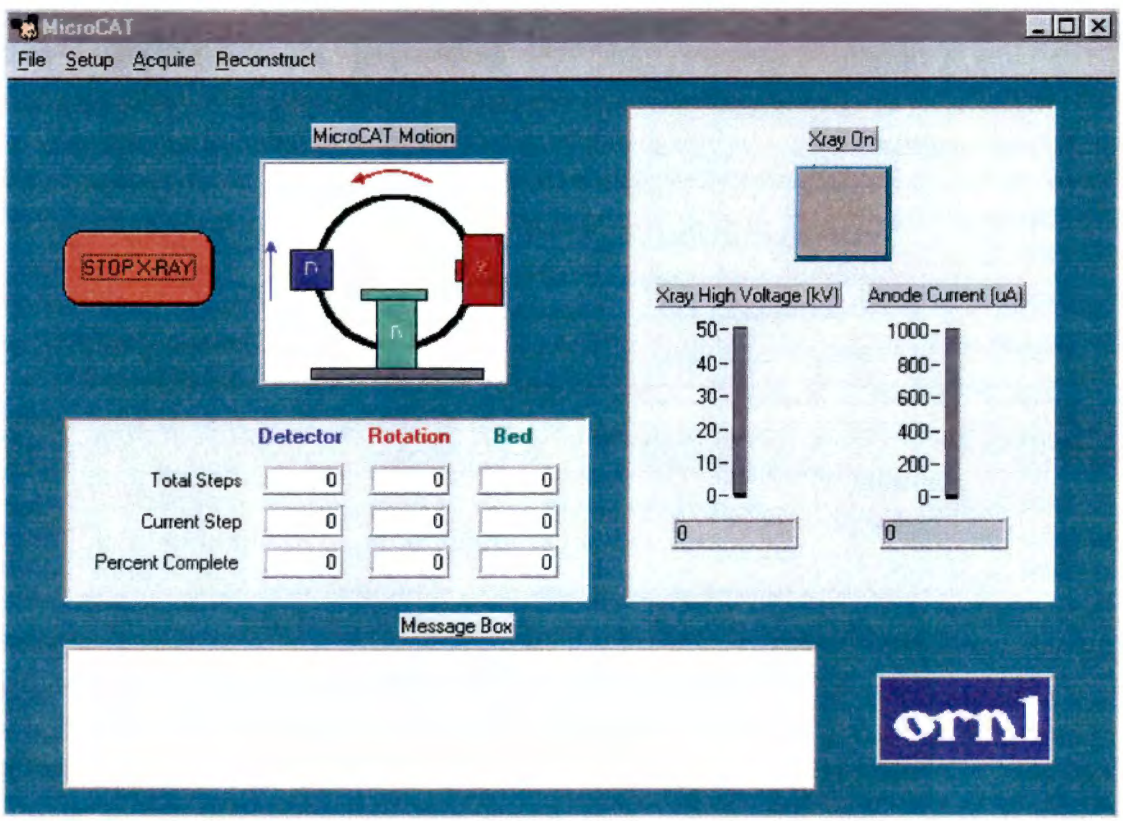


Figure 1.13: Operator interface for MicroCAT system

1.3 Objective of This Thesis

The primary objective of this thesis is the development of a low noise, high pulse rate, monolithic CMOS preamplifier to be used on the front end of the signal processing channels. This development will include an investigation to determine the most appropriate amplifier topology, the design, fabrication, and final testing of the preamplifier both with the x-ray system and alone. The preamplifier must interact directly with the CZT strip detector, and many properties of the detector, such as parasitic capacitance and charge collection time have vital roles in the design of the preamplifier. Therefore, the secondary objective of this thesis is the investigation of the electrical properties of the detector.

In Chapter 2 the analog electronics channel is described in detail and the CZT strip detector properties are examined with both a thorough literature review and direct measurements of the detector properties. In Chapter 3 the topology selection and design of the preamplifier is examined, and the desired performance specifications of the preamplifier are discussed. Pertinent literature is reviewed in order to narrow the selection of possible topologies, and the desired performance specifications are used to choose a final preamplifier topology. The design and analysis of the preamplifier is addressed in Chapter 3 as well. Critical issues such as noise performance and stability against oscillations are considered in detail, and the hand calculations are compared to pre-layout simulation results. In Chapter 4 the fabrication process parameters are described, and layout issues such as correct device matching are addressed. The layout of the preamplifier is discussed, and comparisons between the pre-layout and post-layout simulations are made. The testing of the preamplifier is discussed in Chapter 5. Test

results are presented, and are compared to the expected results. The thesis is completed with discussion and concluding remarks in Chapter 6.

Chapter 2 Electronics Channel Description and CZT Characterization

2.1 A General Pulse Counting Analog Electronics Channel

Since it is desired for this project to measure the energy of each incident *x-ray* onto the detector, the system must be operated in a pulse counting mode. A pulse counting *x-ray* spectroscopy system, illustrated in Figure 2.1, normally consists of a detector, a preamplifier, a pulse-shaper and pulse counting and measurement circuitry.

2.1.1 Detector

In an *x-ray* spectroscopy system the purpose of the detector is to convert the energy of the incident *x-ray* (photon) into an electrical signal; one measure of how well the detector performs this task is the *conversion efficiency.* Classical *x-ray* spectroscopy systems have incorporated detectors such as scintillators coupled to photomultiplier tubes (PMT) and semiconductor devices such as pn junction diodes.

An incident photon loses energy to the detector by three processes. These are the photoelectric effect, the Compton effect, and pair production [13]. The probability of any of the three effects occurring within the detector is a function of the detector's atomic number (Z) and thickness. The total probability of absorption of a photon into a detector medium, ζ_T, is the sum of the individual probabilities:

$$\zeta_T = \zeta_{photo} + \zeta_{Compt} + \zeta_{pair} \quad . \tag{2.1}$$

The probability of the photoelectric effect contribution is given by [13]

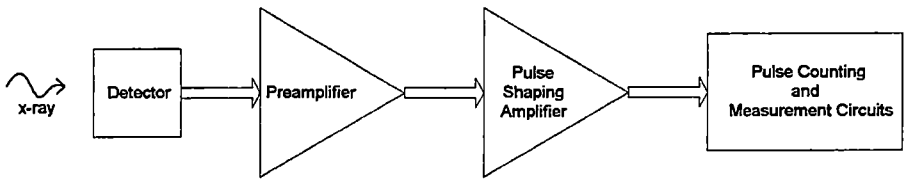


Figure 2.1: Pulse Counting *X-ray* Spectroscopy Block Diagram

$$\zeta_{photo} \propto \frac{N \cdot Z^5}{(h\nu)^{3.5}}, \tag{2.2}$$

where N is a constant equal to the number of atoms per unit volume of the detector medium that has an atomic number Z.

The photoelectric effect provides a complete transfer of photon energy to the detector medium, and thus is the desired effect. From Equation 2.2 it can be seen that the probability of the photoelectric effect is greatly increased as the atomic number is increased and the photon energy is decreased.

2.1.2 Preamplifier

The preamplifier of a spectroscopy system may serve different purposes depending on the type of detector being used [14]. For example, the signal level from a scintillation detector coupled to a PMT is usually sufficiently large so that the preamplifier serves only to help stabilize the system time constant against cabling and equipment changes. In contrast, the signal level from a semiconductor detector is usually so small that it must be amplified to a usable level. In this situation, the preamplifier

must be designed with adequate signal gain and noise performance to prevent degradation of the system resolution.

Historically, voltage-sensitive and charge-sensitive configurations have been used. The signal gain of voltage-sensitive preamplifiers is sensitive to changes in the detector capacitance, while the charge-sensitive preamplifier's signal gain is almost completely independent of the detector capacitance. The charge-sensitive topology has the additional advantage of little noise contribution from the feedback resistor, because the feedback resistor is typically much larger for this topology since its only purposes are to provide DC feedback and to set the pulse decay time. In some cases the feedback resistor is replaced with a switching circuit to reset the preamplifier, and this usually results in further decrease of the feedback noise contribution.

2.1.3 Pulse Shaper

A pulse-shaping amplifier may be required to increase the signal – to – noise ratio (SNR) of the system, to reduce the effect of pulse pile-up from the preamplifier and to give additional signal gain if needed. Pulse pile-up occurs in systems with a large event rate, and it is a function of the detector's charge collection time and the preamplifier's pulse decay time. In order to ensure complete charge collection from the detector, the pulse decay time is made much larger than the charge collection time. If the next event occurs before the detector pulse has decayed completely, the pulse will tend to pile up as shown in Figure 2.2. This can result in the incorrect measurement of pulse height and number of pulses and the system resolution will suffer. The output pulse duration is

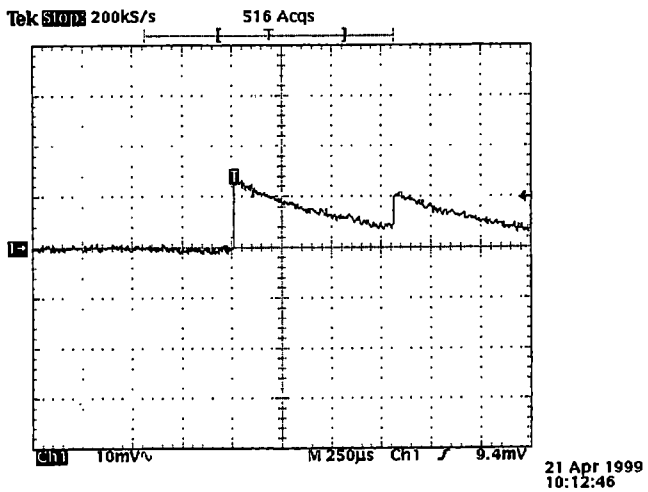


Figure 2.2: Pulse pile-up example captured using a single pixel CZT detector and a commercial preamplifier

set so that it is much less than the preamplifier pulse decay time, but it must remain long enough so that complete charge collection from the detector takes place. The shaping time is a parameter used throughout the literature to describe the pulse duration; however, the use of the parameter is inconsistent from paper to paper. For the purpose of this thesis the shaping time will refer to the time to peak for unipolar pulse shapes and to the time of the first crossover for bipolar pulses.

The most common pulse shaping technique used is a linear amplifier with a number of integrating and differentiating stages. This type of shaper is known as a CR-$(RC)^n$ filter, where n is the number of integrating (RC) stages. Depending on the value of n, the shape of the output pulse of this circuit approaches a Gaussian shape. In practice, four stages of integration (n=4) have been shown to produce a sufficiently Gaussian shaped pulse [14]. Pulse shaping allows the system to operate at a higher pulse rate with a much-improved accuracy.

2.1.4 *Pulse Counting and Measuring Circuitry*

The content of this signal processing block may vary greatly from system to system. In order to count the individual incident photons, a discriminator can be used to increment a counter, which may be implemented in either software or hardware. If the energy of the individual *x-rays* is to be measured, then a track-and-hold or peak stretching circuit may be used to capture the maximum pulse amplitude, which is proportional to the energy of the *x-ray* incident on the detector. This analog value can then be converted to a digital signal with an analog-to-digital converter (ADC) for digital processing with a work station.

2.2 *MicroCAT Analog Channel*

The desired MicroCAT analog channel consists of the previously described components of a typical pulse mode system. The CZT detector is operated at a DC bias voltage, typically on the order of a few hundred volts, and is coupled to the charge-sensitive preamplifier (CSA) input via a high voltage capacitor. Two comparators monitor the CSA output voltage and issue a reset signal when this voltage approaches either the high or low threshold voltage (Figure 2.3). A PMOS switch, which replaces the feedback resistor in parallel with the integrating capacitor, resets the CSA on command of the comparators or an externally issued reset signal. The CSA drives the shaping amplifier, which is a Transconductance - C shaper (Gm-C) with the shaping time set to 920 ns, for a bipolar pulse [40]. The shaper output is fed into a peak – stretching circuit that retains the maximum value of the input pulse as the channel output for that event.

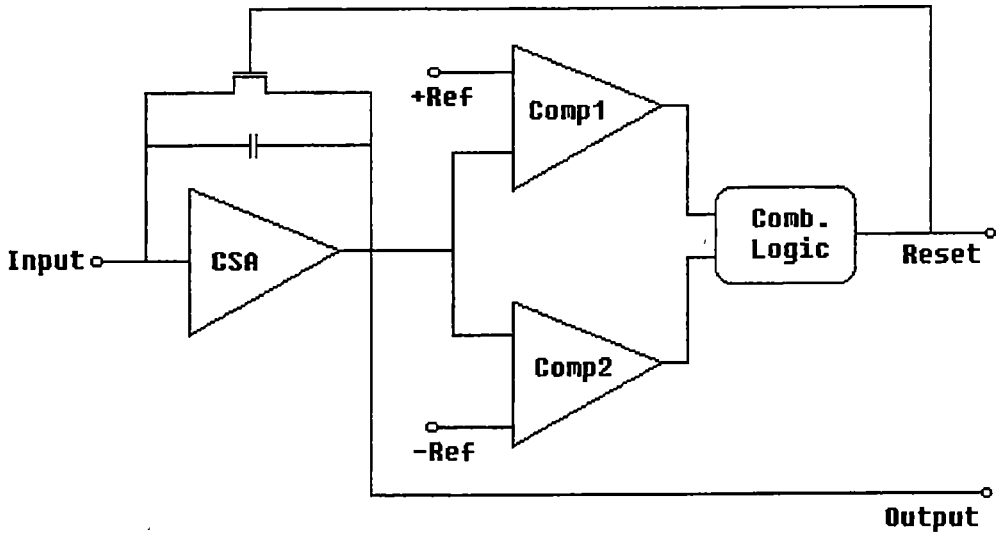


Figure 2.3: Proposed MicroCAT analog channel preamplifier configuration

The CSA also drives a discriminator circuit that, upon the occurrence of a detected event, issues an active high signal indicating the presence of valid data (pulse amplitude) on that channel. A control unit then connects an ADC to that channel and the analog data is converted to a 10 – bit digital signal, the event is counted into an energy bin based on its energy level.

2.3 *Analog Channel Noise Sources*

Although all of the electronics of the channel produce noise, the noise sources at the front end of the analog channel are the major contributors to the degradation of the signal to noise ratio (SNR) because the signal amplitude at that point is at its lowest value. Therefore, the most important contributors to the noise are (1) the shot noise [42] due to the detector's leakage current, and (2) the preamplifier equivalent input noise

voltage. The former has two components that are the flicker noise and the thermal noise [31].

Additional sources of noise are a non-constant ballistic deficit that results from a fluctuating charge collection time, pulse pile-up errors, and preamplifier saturation [13,14]. The ballistic deficit is the difference between the pulse height for an infinite shaping time and that for a finite shaping time (Figure 2.4). If the charge collection time varies from pulse to pulse and a short shaping time is used in the system, then the shaped output pulse amplitude will fluctuate, and as a consequence of this fluctuation the ballistic deficit varies.

The preamplifier has a finite dynamic range at its output stage, and if the output signal voltage approaches the output voltage limit set by the dynamic range, the preamplifier will 'saturate'. Events that occur while the preamplifier is saturated will not be seen by the shaper, and will not be counted or measured. To prevent this from occuring, the preamplifier must be designed with a decay time fast enough to prevent the

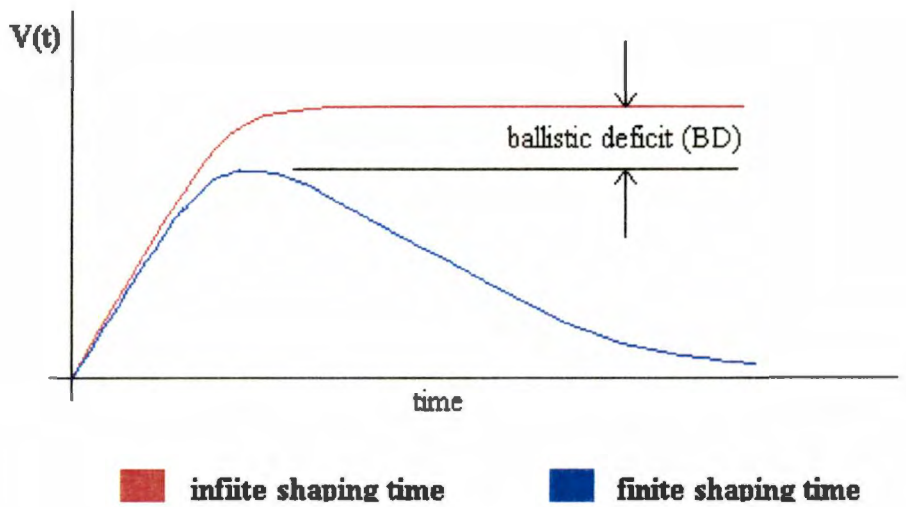


Figure 2.4: Ballistic deficit

output signal from approaching the dynamic range limit. However, for very high pulse rate systems this may not be possible, in which case a resetable topology can be used to reset the preamplifier output to baseline. This method introduces dead time into the system because the preamplifier can not be used while it is being reset.

2.4 *Cadmium Zinc Telluride (CZT) Detector*

2.4.1 *CZT Compound Semiconductor Properties*

Cadmium Zinc Telluride ($Cd_{1-x}Zn_xTe$ or CZT) is a relatively new compound semiconductor detector that has undergone much development within the past six years [15,16,18,20]. For the purpose of room temperature *x-ray* spectroscopy, the material possesses several advantages over traditional semiconductor detectors such as silicon, Si, and germanium, Ge. CZT has a bandgap of 1.56 eV (1.12 eV for Si and 0.66 for Ge), an effective atomic number of about 50 (14 for Si and 32 for Ge), a conversion efficiency of 1 electron – hole pair per 4.5 eV and an energy resolution of approximately 7% FWHM at 60keV. The material suffers, however, from a large difference in the electron and hole mobilities. The effective electron mobility is excellent at about 690 $cm^2V^{-1}sec^{-1}$, but the effective hole mobility is only about 4.7 $cm^2V^{-1}sec^{-1}$ [15]. The effects of this deficiency may be offset for the case of low – energy photons by biasing the detector such that the photons are incident on the negatively biased side of the detector so that the holes travel the shortest distance possible.

Much work has been done to characterize CZT strip detector architectures so that an accurate charge collection model could be developed. Tousignant *et al.* [15] have evaluated the charge transport properties of a CZT strip detector 1.5 mm thick with gold

strips that are 225 μm wide on a 375 μm pitch. The results of this study are summarized in Table 2.1. The hole mobility presented by Tousignant *et al.* is lower than the value generally stated in the literature, which is on the order of 50 $cm^2V^{-1}sec^{-1}$. Heanue *et al.* [17] have tested larger geometry strip detectors and found a hole mobility of 90 $cm^2V^{-1}sec^{-1}$.

CZT has also shown excellent spatial resolution. The most promising work, done by Tousignant *et al.* [22, 15], has shown that sub – pitch event location as good as 10 μm may be possible. Their work indicates that this is made possible due to the fact that the charge induced by photons that are incident in the area between electrodes (strips) is shared linearly with the neighboring electrodes. Kurczynski *et al.* [18] reports sub – pitch resolution capability using a CZT detector with 50 μm wide strips on a 100 μm pitch, and Mayer *et al.* [25] also reports sub – pitch resolution using a CZT detector fabricated with 225 μm wide strips on a 375 μm pitch.

Table 2.1: Charge transport properties of $Cd_{0.9}Zn_{0.1}Te$ [15]

	Electrons	Holes
Mobility ($cm^2V^{-1}sec^{-1}$)	1000	7
Trapping time	55ns	4.2μs
Detrapping time	25ns	2μs
Deep trapping time	---	4μs
Effective mobility ($cm^2V^{-1}sec^{-1}$)	690	4.7
μτ product (cm^2V^{-1})	---	2.8×10^{-5}

For an ideal system with no noise sources, the energy resolution is limited only by the random fluctuations in the number of charge carriers produced within the detector for a given amount of incident radiation. Assuming that the formation of charge carriers is a Poisson process, Knoll [14] presents Equation 2.3 as a theoretical statistical limit of the energy resolution.

$$R|_{Poisson} = \frac{2.35}{\sqrt{N}} \cdot 100\% \qquad (2.3)$$

Where N is the number of charge carriers produced and is dependent on the detector. For CZT about 4.5 eV of energy is required to produce an electron – hole pair, therefore the limiting resolution for CZT at 60 keV is 2.04% and at 22 keV is 3.36%. Energy resolutions as high as 22% FWHM for a 60 keV source (detector thickness 2 mm) [18] and as low as 4.54% FWHM for a 60 keV source (detector thickness 2 mm) [16] without the use of cryogenic cooling of the detector have been reported. However, research has shown that by reducing the leakage current of the detector with cryogenic cooling to –30 °C, energy resolutions of less than 2% FWHM at 60 keV are obtainable for low energy sources [16, 20].

2.4.2 MicroCAT CZT Strip Detector Measured Properties

Several important properties of the strip detector were measured in order to obtain information required for designing the preamplifier. The detector strip – to – strip

capacitance, strip leakage current, energy resolution, charge collection time and conversion efficiency were investigated.

2.4.2.1 Detector Capacitance

The detector capacitance was measured using a Hewlett Packard 4192A impedance analyzer. The detector bias voltage was varied from zero to 35 volts (the maximum bias voltage allowed by the instrument) and at each bias voltage the capacitance was measured at 1 kHz, 10 kHz, 100 kHz and 500 kHz. All strips were connected to ground potential except for the strip being measured. The results of these measurements, illustrated in Figure 2.5, give a maximum strip capacitance of 8.4 pF and a minimum of 2.7 pF. The capacitance drops to approximately 3.5 pF at the higher bias voltages. 4 pF was chosen as a design parameter for the CZT strip detector.

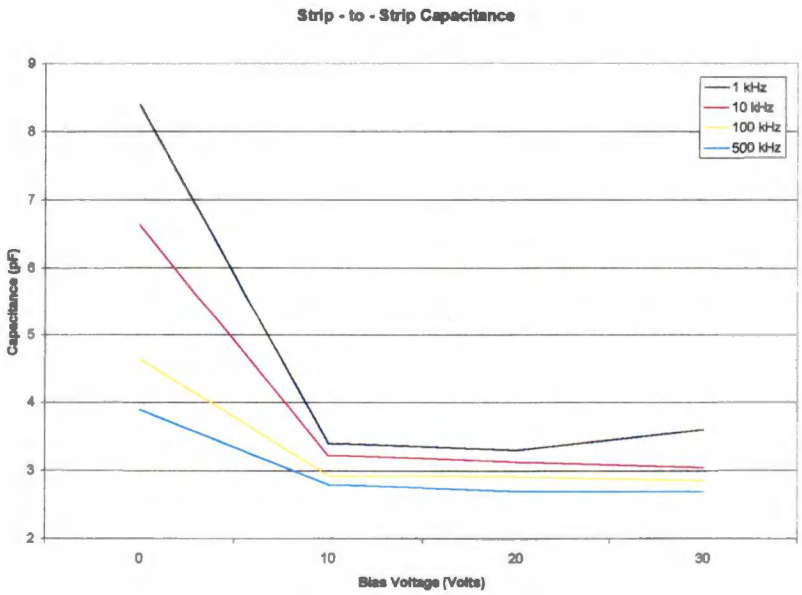


Figure 2.5: Capacitance of the CZT strip detector

2.4.2.2 *Leakage Current*

The leakage current was determined for each strip for bias voltages ranging from 10 volts to 200 volts. For this experiment, illustrated in Figure 2.6, the detector was placed in a darkened enclosure with the bias voltage and signal output supplied via BNC connections on the enclosure. An Ortec model 556 high voltage power supply was used to provide the bias voltage, a Stanford Research Systems model SR570 low – noise transimpedance preamplifier was used to amplify and convert the leakage current to a voltage and a Fluke model 77 digital multimeter was used to measure the output voltage. All strips of one side of the detector were connected to the bias voltage supply and all strips on the opposite side except the one being tested were connected to ground. The leakage current for each strip of one side of the detector was measured and recorded. The measured leakage currents (in nA) are plotted versus the strip number in Figure 2.7.

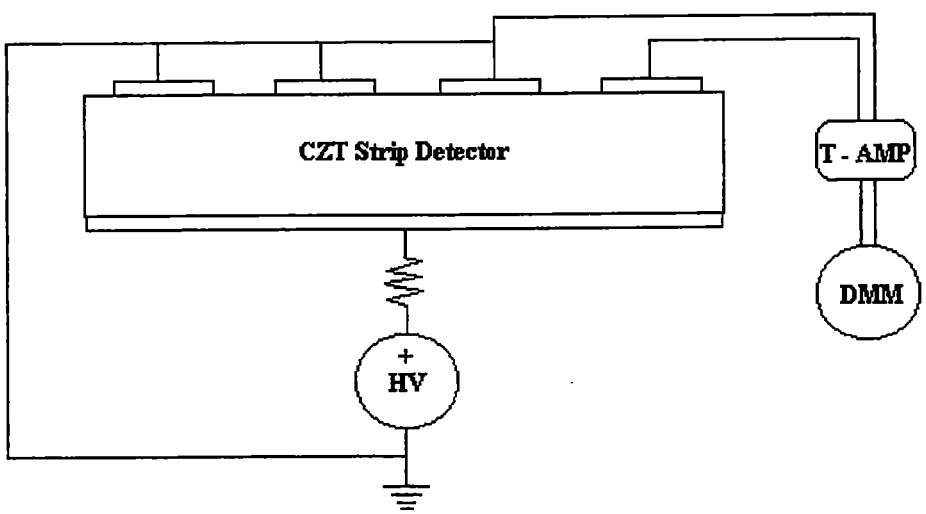


Figure 2.6: Block diagram for measuring CZT leakage current

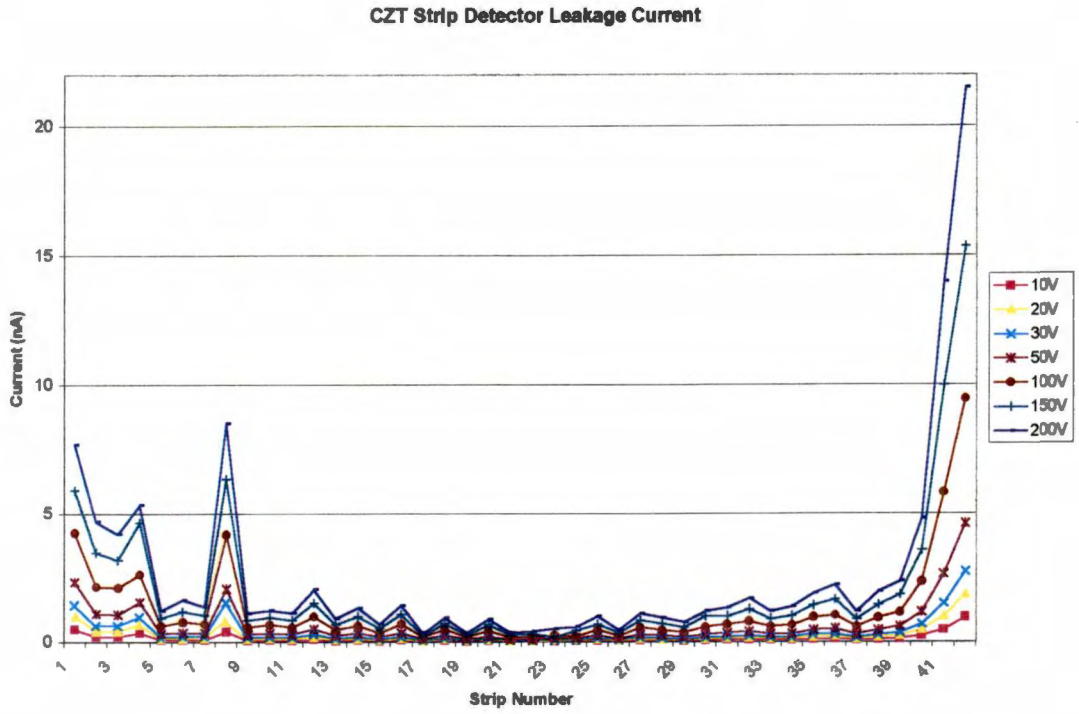


Figure 2.7: CZT Strip detector leakage current

There are two components to the strip leakage currents. The bulk leakage current is the current that flows from the strip through the bulk of the detector to ground, and the surface leakage current is the current that flows from the strip over the surface of the detector to ground. As expected, neglecting strip number eight, the maximum values of leakage currents are found on the outer strips, because the surface leakage current is greater for those strips. The larger leakage current of strip eight could be the result of an impurity in the CZT bulk at that location. As the bias voltage is increased the leakage current should increase linearly depending only on the resistivity of the detector plus the biasing resistance, which is approximately 22 MΩ. The average leakage current was taken, neglecting the first and last three strips and strip eight, and plotted versus the

applied bias voltage (Figure 2.8). The inverse of the slope of the line that best fits those data points is the sum of the detector resistance and the biasing resistance. Thus, the detector resistivity was found to be 158 GΩ. A maximum leakage current value of 25 nA and a nominal value of 1nA was used for the purpose of designing the preamplifier.

2.4.2.3 Energy Resolution

A single pixel CZT detector that measured 3 mm square by 1 mm thick was used to investigate the energy resolution. This detector was also manufactured by eV Products using the same High Pressure Bridgman (HPB) process [16] as was used for the strip detector. The CZT detector was coupled to an Ortec model 142A charge – sensitive preamplifier,

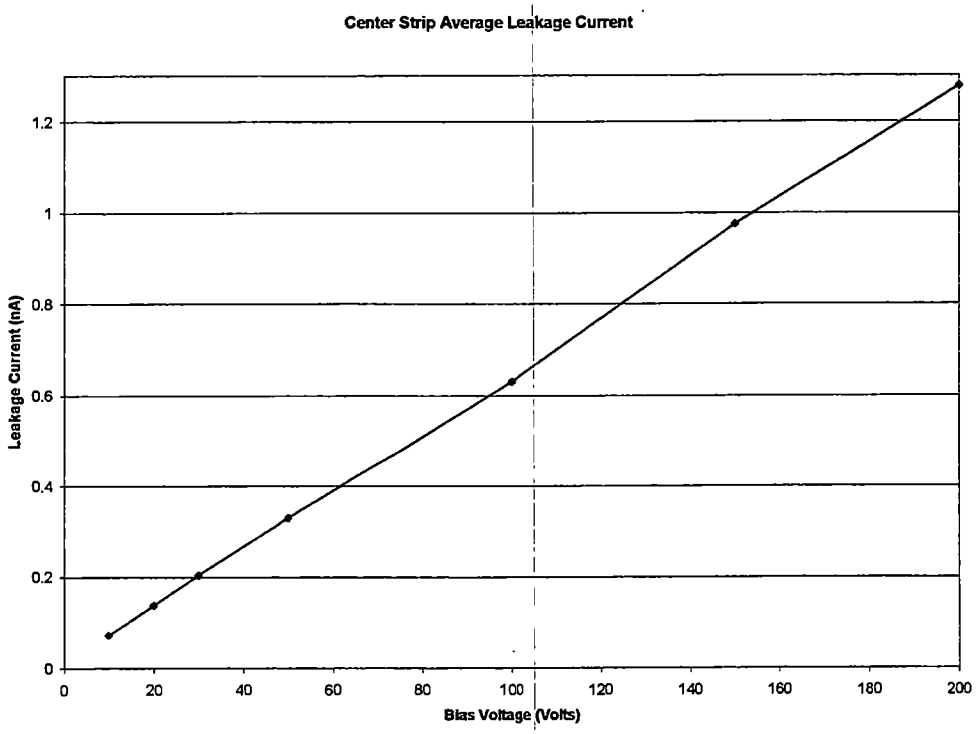


Figure 2.8: Average center strip leakage current versus applied bias voltage

and an Ortec model 571 shaping amplifier was used to provide pulse shaping. The test configuration is presented in Figure 2.9. The output of the shaping amplifier was fed into a 12-bit data acquisition board in a personal computer and was histogramed using a multi-channel analyzer (MCA). Data was taken in 10 minute intervals using a ^{109}Cd source (22 keV) for each shaping time constant. The system resolution was studied for both unipolar and bipolar pulse shaping. The resulting histogram for unipolar shaping with the time constant set to 2.1 μs is illustrated in Figure 2.10. The FWHM resolution was calculated using Equation 2.4, and plotted versus the shaping time constant for both unipolar and bipolar pulse shaping (Figure 2.11).

$$R(keV) = \frac{22keV}{Centroid(channel)} \cdot FWHM(channels), \qquad \textbf{(2.4)}$$

where *Centroid* and *FWHM* are expressed in a number of channels from the MCA.

As shown by Knoll [14], unipolar pulse shaping provides a higher signal to noise ratio than provided by bipolar shaping, however, bipolar shaping was the chosen method for the MicroCAT system primarily to eliminate the need for baseline restoration circuitry. The optimum time constant for bipolar shaping for this detector and electronics configuration is approximately 5 μs. The shaping time chosen for the MicroCAT system was 500 ns in order to improve the response to higher pulse rate sources.

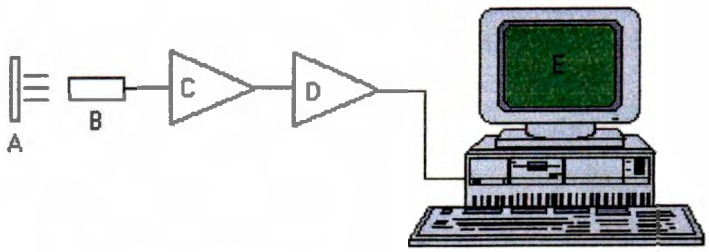


Figure 2.9: Resolution measurement configuration, A) Source, B) CZT detector, C) Charge sensitive preamplifier, D) Shaping amplifier and E) Personal computer with MCA software

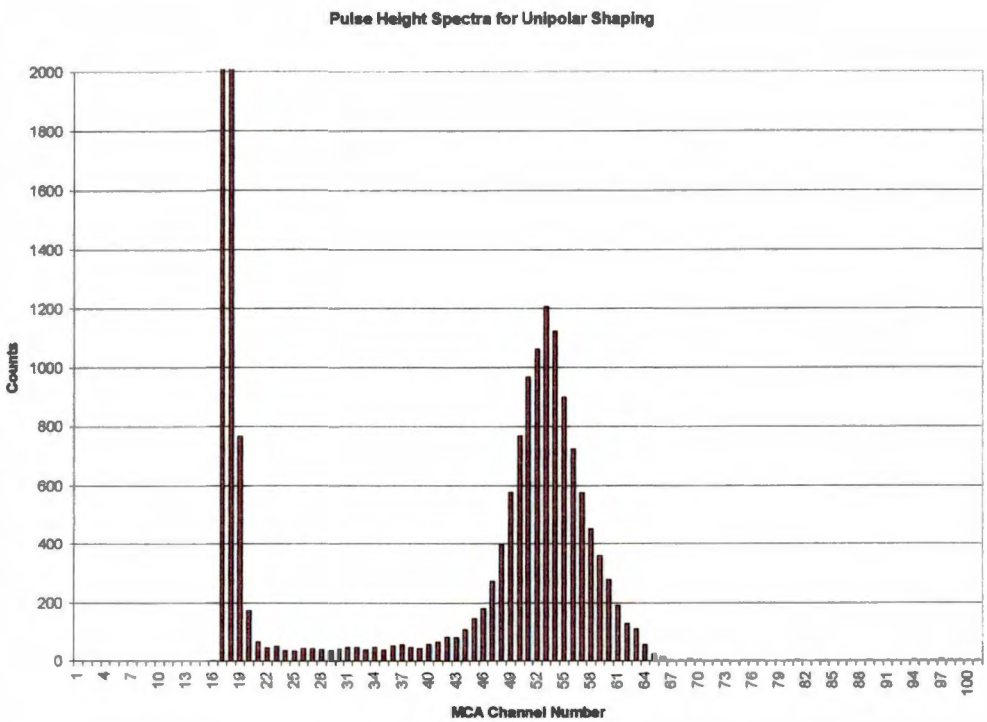


Figure 2.10: Pulse Height Spectrum for Unipolar Shaping (τ = 2.1 μs)

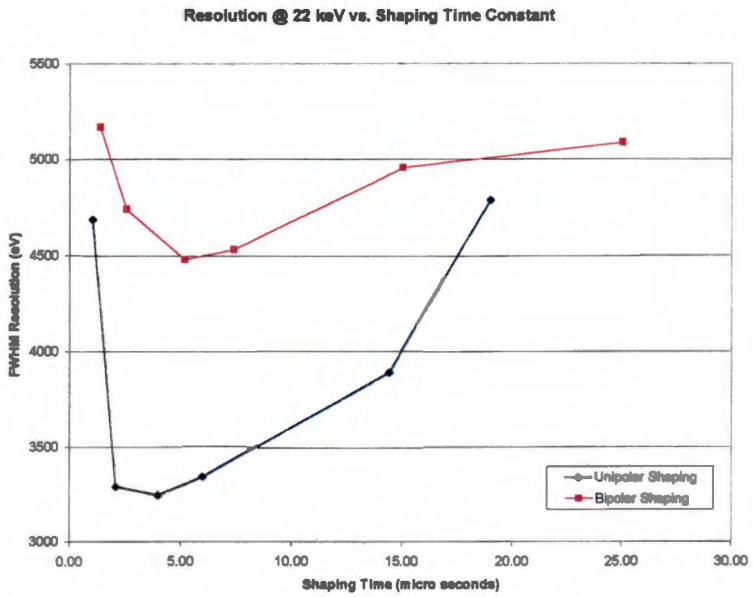


Figure 2.11: FWHM resolution for both unipolar and bipolar pulse shaping

2.4.2.4 Charge Conversion Efficiency

The conversion efficiency is a measure of the quantum of energy required to produce an electron – hole pair within the detector bulk, and for CZT the generally reported number from the literature ranges from 4 to 5 eV. In order to measure this property the circuit used to determine the energy resolution was used with the shaping time constant set to 2.1 μs and unipolar shaping. The first step was to inject a known number of electrons into the preamplifier and then find the resulting centroid on the MCA. The detector was removed and a test voltage pulse with amplitude 0.54 mV was applied to the test input of the Ortec 142A preamplifier, which provides a charge input determined by a 1 pF capacitor. The number of electrons injected, N, was calculated to be 3386.4 using Equation 2.5, and the centroid was recorded from the MCA to be channel number 44.46.

$$N = \frac{C(Farads) \cdot v(Volts)}{1.602 \times 10^{-19}(Coulombs)}. \quad \textbf{(2.5)}$$

C is the charge determining capacitance and v is the input pulse amplitude in volts. For the shaping time constant chosen, the centroid that corresponds to the 22 keV ^{109}Cd source was channel number 51.93. Therefore, the conversion efficiency was calculated to be approximately 5.5 eV per one electron-hole pair, as shown in Equation 2.6.

$$E = \frac{22keV}{51.93} \cdot \frac{44.4}{3386.4} \quad \textbf{(2.6)}$$

This number is slightly higher than values reported in the literature, which are between 4.5 and 5 eV per electron-hole pair. Possible sources of error are (1) imprecise measurement of the input test pulse and (2) inability to precisely measure the charge determining capacitor.

2.4.2.5 Charge Collection Time

The charge collection time was investigated using the single pixel CZT detector, the Ortec 142A preamplifier and a digital oscilloscope (Figure 2.12). Several random detected events were captured on the oscilloscope that were representative of all the detected events. One such event is illustrated in Figure 2.13. This output pulse has an initial fast rising edge followed by a much slower rising edge, corresponding to the

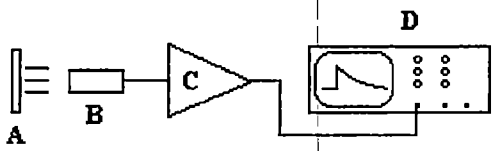


Figure 2.12: Charge collection time circuit configuration illustrating A) the 22 keV source, B) the CZT detector, C) the Ortec charge – sensitive preamplifier and D) the digital oscilloscope

collection of electrons and holes, respectively. The electron charge is collected quickly, while the hole charge is collected more slowly, a result of the much lower hole mobility.

The 10 to 90 percent rise time of the Ortec 142A preamplifier is less than 7 ns, and therefore has a negligible effect on the rise time of the output pulse. The low energy photons of the ^{109}Cd source are absorbed only a few microns below the surface of the detector, so that the electrons must travel nearly the entire thickness of the detector to be collected at the positive electrode. The complete rise time of the initial slope of the output pulse was measured to be approximately 80 ns. With this timing information, the electron mobility was calculated to first order using Equation 2.7,

$$\mu|_{electrons}\left(\frac{cm^2}{v\cdot s}\right) \cong \frac{v\left(\frac{cm}{s}\right)}{E\left(\frac{v}{cm}\right)}, \qquad (2.7)$$

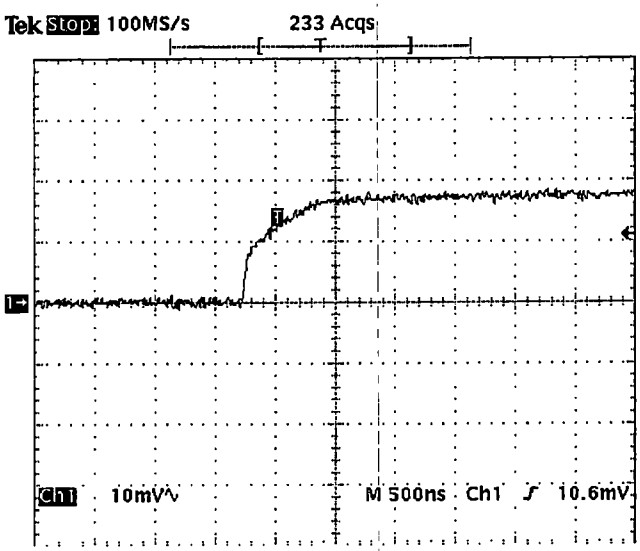


Figure 2.13: Charge-sensitive preamplifier output pulse for a bias voltage of +100V

where v is the charge carrier velocity calculated to be 1.25×10^6 (cm/sec), and E is the electric field across the detector calculated to be 1000 (V/cm). The electron mobility was calculated to be 1,250 (cm^2/volt-second), which is in agreement with the published data.

The output signal was approximated to a first order using straight lines that matched the two distinct slopes. The derivative was taken of the approximated pulse, and the result is shown in Figure 2.14. The derivative begins at zero and rises quickly corresponding to the initial large slope of the output pulse, and then drops corresponding to the second slope of the output pulse. The derivative looks like a fast pulse with a trailing 'tail'. Complete charge collection can only take place if the shaping time constant is made large enough so that the charge-sensitive preamplifier integrates the entire pulse, including the tail. Error will be introduced into the measurements if the entire charge is not collected; however, if the shaping time is made sufficiently large to collect all of the charge, the maximum possible pulse rate will be reduced because of the

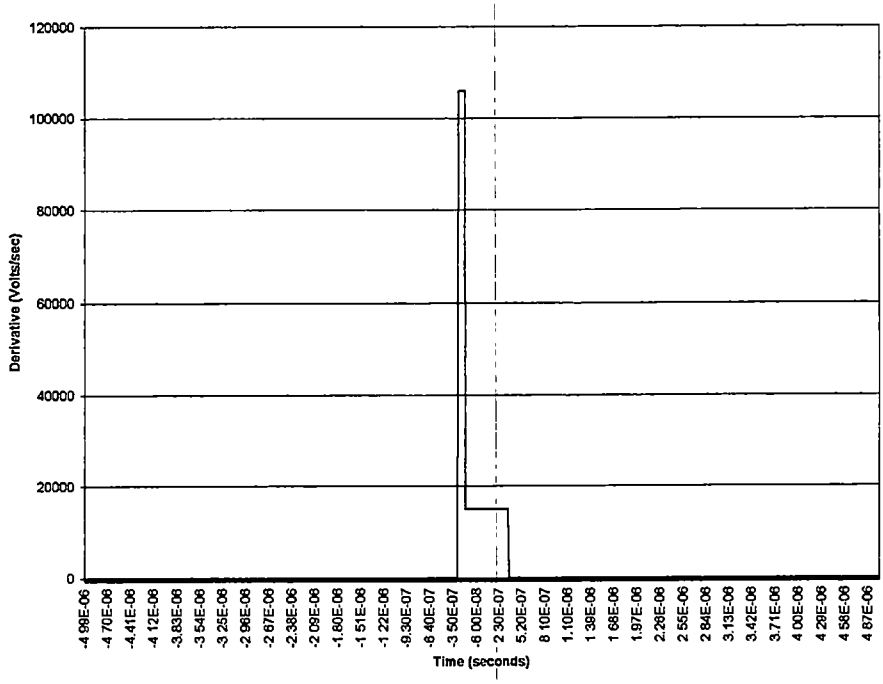


Figure 2.14: Derivative of preamplifier output signal

increased system dead time. The original shaping time chosen for the MicroCAT system was 500 ns, which was a compromise between maximum charge collection and maximum pulse rate.

2.4.2.6 Summary of Test Results

The extracted parameters found in these experiments were in good agreement with those presented in the literature. Some parameter values that were chosen for the MicroCAT system (i.e. shaping time and pulse shape) are not the optimum values. The primary disadvantage invoked by choosing non-optimum values was a decrease in the system signal – to – noise ratio. The parameter values chosen for the MicroCAT system are listed in Table 2.2.

Table 2.2: Design parameters for the MicroCAT system

Parameter	Chosen for MicroCAT Design
Detector Capacitance	4 pF
Maximum Detector Leakage Current	25 nA (max), 1nA (nominal)
Pulse Shaping	Bipolar (not optimum for noise)
Shaping Time	500 ns
Charge Conversion Efficiency	5.5 eV per one electron-hole pair
Collection Time	~1 μs

Chapter 3 Circuit Design and Analysis

3.1 *Introduction to the Preamplifier Design Requirements*

Design considerations for the preamplifier involving overall system components were presented in Chapter 2. From the specifications developed there, a preamplifier topology will be selected. In this section each of the specification's impact on the preamplifier design is considered, and in Section 3.2 the preamplifier topology is selected and discussed.

3.1.1 *Signal Gain, Input and Output Impedance*

The detector generates a current pulse that has a duration given by the charge collection time, τ_c, of the CZT detector. The detector may be modeled as a high impedance current source with a load capacitance, C_L, (Figure 3.1). It is desired to have a voltage output, V_o, that is proportional to the input current pulse. Because the detector impedance is very large, the preamplifier's input impedance should be kept small so that the load capacitance does not limit the signal bandwidth.

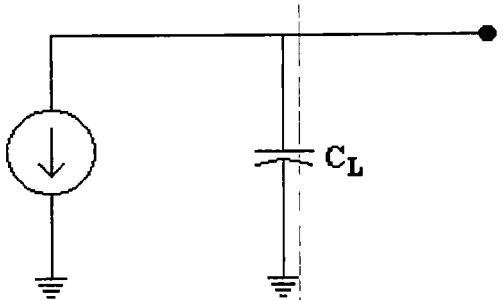


Figure 3.1: Simple Model of the CZT Detector

The preamplifier is expected to drive a shaping amplifier circuit with an input resistance of 10 kΩ. Therefore, the output impedance should be kept low to prevent signal loss. These characteristics are provided by a transresistance feedback topology [29], and also by a charge-sensitive feedback topology [14,30]. Both topologies are discussed in Section 3.2.

3.1.2 Noise Performance

CZT detectors have a charge collection time on the order of 1 μs. The larger charge collection time requires the shaping filter to operate at a larger shaping time, and thus a lower center frequency. Bipolar shaping with a shaping time of 500 ns was chosen for the MicroCAT system. The shaping filter is of the form, $(CR)^2$-$(RC)^4$, which was implemented with a Gm-C filter topology [40]. The transfer function for this shaping filter in the s-domain is;

$$H(s) = \frac{K \cdot \left(\frac{1}{\tau}\right)^4 \cdot s^2}{\left(s + \frac{1}{\tau}\right)^6}, \qquad \textbf{(3.1)}$$

where τ = 100 ns and K = 1000, nominally. This transfer function has a center frequency at approximately 1.2 MHz with a low frequency roll-off of –40 dB per decade and a high frequency roll-off of –80 dB per decade (Figure 3.2). The noise performance of the system is determined by the placement of the shaping filter's center frequency in that the

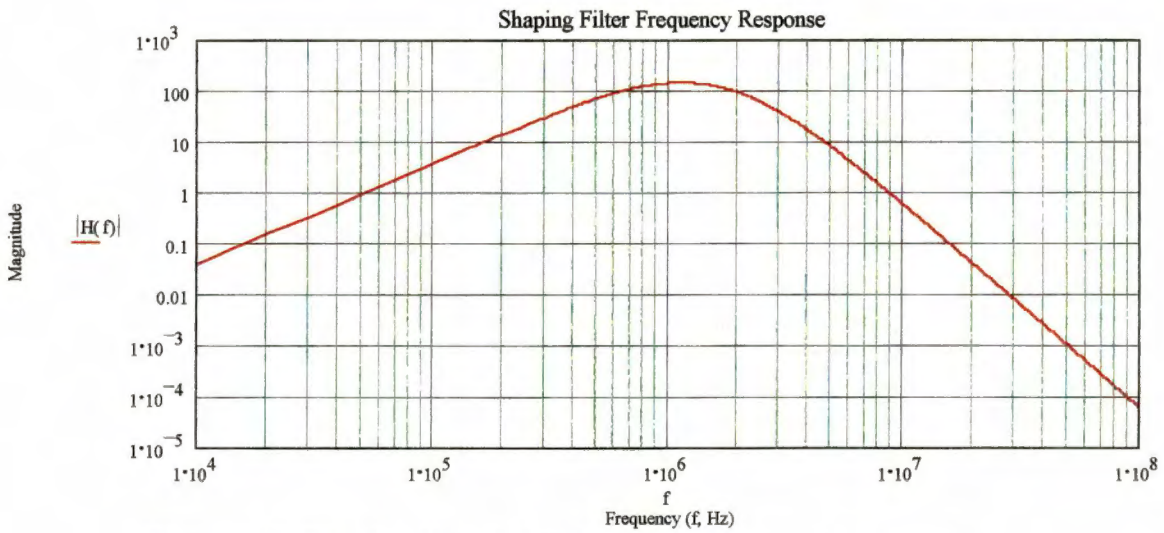


Figure 3.2: Bipolar Gm-C shaping filter frequency response

dominate noise sources that appear at the input will be passed only near that center frequency and within the bandwidth of the shaping filter.

The dominant noise sources can be modeled as equivalent voltages and currents at the input of the preamplifier. They are (1) the CZT shot noise current, (2) the preamplifier equivalent input noise voltage, and (3) the thermal noise current of the feedback elements of the preamplifier. The preamplifier's equivalent input noise voltage consists of a channel thermal noise component and a channel flicker ($^1/_f$) noise component. The flicker noise corner for MOSFET transistors can extend well into the megahertz region [31], which is a concern when using a large shaping time. A simple noise model is illustrated in Figure 3.3 for a charge-sensitive feedback topology with a large value feedback resistor as a reset element.

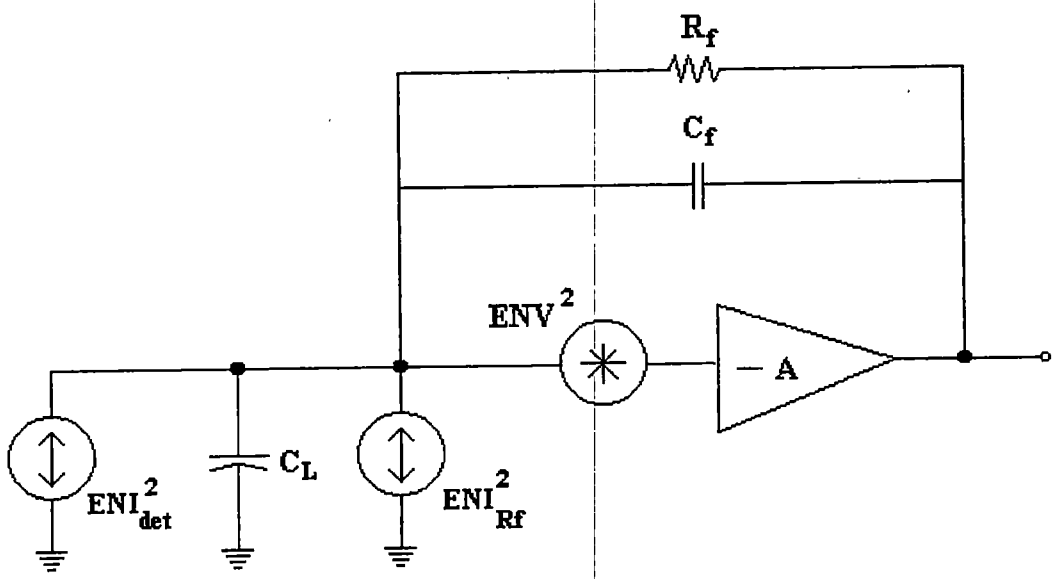


Figure 3.3: Equivalent noise circuit for CZT detector coupled to a charge-sensitive preamplifier with a resistive reset element

3.1.2.1 *CZT Shot Noise*

The leakage current of the CZT detector, $I_{leakage}$, was studied in Chapter 2. The noise current associated with the detector leakage current can be modeled as a shot noise current [42] with a spectral density given by

$$ENI^2_{\det}\left(\frac{A^2}{Hz}\right) = 2qI_{leakage}, \tag{3.2}$$

where q is the charge of a single electron (1.602×10^{-19} C). The value of the detector current noise for a leakage current of 25 nA is 8.01×10^{-27} (A^2Hz^{-1}), and it is frequency independent.

3.1.2.1 *Preamplifier's Equivalent Input Noise Voltage*

The core amplifier is fabricated in the AMI 1.2 μm CMOS technology. Each MOSFET device used in the core amplifier will contribute to the equivalent input noise voltage to some extent. However, in some designs the input FET is made to be the dominant noise source. In either case, the equivalent input noise voltage will have two components; (1) a thermal noise component due to the channel thermal noise, equivalent gate resistance, and the equivalent bulk resistance, and (2) a flicker noise component. The thermal noise component can be modeled as a current source connected between the drain and source of the FET with a spectral density given by [32],

$$ENI^2_{thermal}\left(\frac{A^2}{Hz}\right) = 4kT\left[\gamma \cdot g_m + \left(R_g + R_b\right)\cdot g_m^2\right], \qquad \textbf{(3.3)}$$

where k is Boltzmann's constant (1.38×10^{-23} JK^{-1}), T is the temperature in Kelvins, g_m is the device's transconductance, γ is a process dependent constant usually taken to be $^2/_3$ for a MOSFET in strong inversion, R_g is the equivalent gate resistance, and R_b is the equivalent bulk resistance. Equation 3.3 can also be expressed as an equivalent noise voltage in series with the gate of the FET by dividing it by the squared transconductance, g_m^2, to obtain the spectral density,

$$ENV^2_{thermal}\left(\frac{V^2}{Hz}\right) = 4kT\cdot\left[\frac{\gamma}{g_m} + R_g + R_b\right]. \qquad \textbf{(3.4)}$$

The current and voltage noise models are illustrated in Figure 3.4 A and B, respectively.

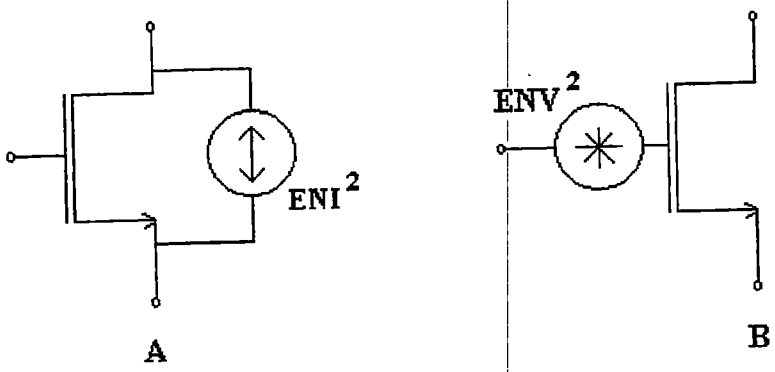


Figure 3.4: MOSFET noise models A) Modeled as a parallel current, and B) a series voltage

The flicker noise is modeled as a noise voltage in series with the gate of the FET with spectral density [32],

$$ENV^2_{1/f}\left(\frac{V^2}{Hz}\right) = \frac{K_f}{C_{ox}^2 WLf^{AF}}, \tag{3.5}$$

where K_f is an empirical parameter with units of V^2F, AF is a constant that is usually taken to be unity for true $^1/_f$ noise, W and L are the transistor active area width and length, respectively, and Cox is the MOSFET capacitance. Equation 3.5 can also be expressed as a current noise generator connected from the drain to the source of the FET by multiplying by the squared transconductance, g_m^2, to obtain,

$$ENI^2_{1/f}\left(\frac{A^2}{Hz}\right) = \frac{K_f \cdot g_m^2}{C_{ox}^2 WLf^{AF}} \tag{3.6}$$

3.1.2.2 *Feedback Element Thermal Noise*

For transresistance topologies the feedback element is a resistor, R_f, and is usually on the order 10 to 100 kΩ. This resistor has a thermal noise current with a current spectral density given by,

$$ENI_{Rf}^2\left(\frac{A^2}{Hz}\right)=\frac{4kT}{R_f} \quad , \tag{3.7}$$

that is in parallel with the resistor. This current noise is injected into the input of the preamplifier, and therefore has the same noise gain as the detector thermal noise. For a feedback resistance of 100 kΩ the noise spectral density is 165.68×10^{-27} (A^2Hz^{-1}), which completely dominates the detector's current noise.

For charge-sensitive topologies the feedback element is a capacitor, which does not contribute anything to the total noise input. However, in practice, a reset element such as a large value resistor or a switch is placed in parallel with the capacitor. The resistor has the same noise current spectral density as given by Equation 3.7, but it is on the order of 100 to 1000 MΩ. Thus, the charge-sensitive topology has a slightly better noise performance than the transresistance topology.

3.2 *Preamplifier Topology Selection*

In Section 3.1 the requirements that the preamplifier must satisfy were discussed. In this section the feedback topology selection is made. Both the charge-sensitive and the transresistance topologies provide the desired signal gain, input and output impedance,

but the charge-sensitive topology provides superior noise performance. Since both topologies require an inverting voltage amplifier the power consumption will be the same and is not an issue in the topology selection.

The charge-sensitive topology was chosen for the MicroCAT system because of its superior noise performance.

3.3 *Noise Optimization of the Charge-Sensitive Amplifier*

The resolution of the electronics channel is determined by the statistical properties of the CZT detector and the random noise sources that are distributed throughout the electronics channel, with the dominant ones being at the input of the preamplifier. Therefore it is desired to reduce the noise contributions of the preamplifier so that the best possible resolution can be obtained. This section will focus on improving the system resolution by optimizing the input characteristics of the preamplifier. The concept of the equivalent noise charge (ENC) is introduced, and related to the FWHM resolution.

3.3.1 *Equivalent Noise Charge (ENC)*

The equivalent noise charge is defined as the ratio of the total r.m.s. noise in electrons at the output of the pulse shaper to the signal amplitude due to one electron charge [33]. The ENC at the preamplifier input is related to the FWHM resolution referred to the detector input by Equation 3.8,

$$ENC(rms-electrons)=\frac{FWHM(eV)}{2.35\cdot\varepsilon\left(\frac{eV}{electron}\right)}, \qquad \textbf{(3.8)}$$

where ε is the detector's conversion efficiency. Each noise source can be considered separately to find their individual ENC, and the total ENC is given by Equation 3.9,

$$ENC_T(rms-electrons)=\sqrt{\overline{ENC_{\det}^2}+\overline{ENC_{thermal}^2}+\overline{ENC_{flicker}^2}+\overline{ENC_{Rf}^2}}\ . \qquad \textbf{(3.9)}$$

3.3.1.1 *Thermal Noise ENC*

For the purpose of this development the input device is considered to be the dominant noise source of the core amplifier. If this is not the case for the core amplifier designed for the CSA, then the final equation developed here will be revised in a later section. The ENV^2 that appears at the input of the amplifier will have the channel thermal noise component given by Equation 3.10,

$$ENV_{thermal}^2\left(\frac{V^2}{Hz}\right)=4kT\cdot\left[\frac{\gamma}{g_m}+R_g+R_b\right], \qquad \textbf{(3.10)}$$

where all device parameters are of the input device. R_b can be reduced at layout by heavily plugging the substrate, and using short, low resistivity connections to the gate of the input device will reduce R_g. For the sake of this analysis, the contributions of R_b and R_g will be neglected.

The noise voltage spectrum that appears at the output of the preamplifier is related to the input noise voltage spectrum, assuming an ideal core amplifier, by

$$ENV_{oA}^2\left(\frac{V^2}{Hz}\right) = \left|\frac{\left(C_d + C_{stray} + C_f + C_{amp}\right)}{C_f}\right|^2 \cdot ENV_{iA}^2 \quad , \tag{3.11}$$

where C_d is the detector capacitance, C_{stray} is the stray capacitance at the detector – preamplifier connection, C_f is the feedback capacitance of the preamplifier, and C_{amp} is the input capacitance of the preamplifier, which consists of the gate-to-drain and gate-to-source capacitance of the input FET. The total mean-squared voltage noise at the output of the shaping amplifier is given by Equation 3.12,

$$\overline{V_{tot}^2}(V_{ms}) = \int_0^\infty \left|ENV_{oA}(j2\pi f)\right|^2 \cdot \left|H(j2\pi f)\right|^2 df \quad , \tag{3.12}$$

where $H(j2\pi f)$ is the pulse shaper transfer function in the frequency domain, and is given by Equation 3.13,

$$H(j2\pi f) = \frac{K(j2\pi f)^2}{\tau^4\left[(j2\pi f) + \frac{1}{\tau}\right]^6} \quad . \tag{3.13}$$

Substituting Equation 3.10, neglecting R_g and R_b, into Equation 3.11 gives Equation 3.14,

$$ENV_{oA}^2\left(\frac{V^2}{Hz}\right) = \left|\frac{(C_i)}{C_f}\right|^2 \cdot \frac{4kT\gamma}{g_m} \quad , \tag{3.14}$$

where C_t is sum of the capacitances that appear in the numerator of Equation 3.11. Substituting Equation 3.14 into Equation 3.12 gives an expression for the mean-squared noise voltage at the output of the pulse shaper due to the input FET's channel thermal noise (Equation 3.15), and performing the integration yields Equation 3.16.

$$\overline{V_{thermal}^2} = \int_0^\infty \frac{2}{3} \cdot \frac{4kT}{g_{m1}} \left(\frac{C_t}{C_f} \right)^2 \left(\frac{16K^2\tau^4\pi^4 f^4}{\left[1+(2\pi f\tau)^2\right]^6} \right) df \qquad \textbf{(3.15)}$$

$$\overline{V_{thermal}^2} = \frac{K^2 kTC_t^2}{128 g_{m1} C_f^2 \tau} \qquad \textbf{(3.16)}$$

Before an expression for the ENC can be found, an expression for the signal amplitude at the output of the pulse shaper due to a single electron charge at the input must be found. If the rise time of the CSA is sufficiently small, the transfer function of the CSA and the pulse shaper in the s-domain is given by Equation 3.17,

$$H(s) = \frac{K\left(\frac{1}{\tau}\right)^4 s}{C_f\left[s+\frac{1}{\tau}\right]^6} \quad , \qquad \textbf{(3.17)}$$

which has the inverse Laplace transform given in Equation 3.18. This expression must

be multiplied by the charge of an electron, q (1.602×10^{-19} C), and evaluated at the pulse peaking time to obtain an expression for the output pulse amplitude due to the input charge of one electron.

$$V_o(t) = \frac{Kt^4 \cdot (-t + 5\tau)}{120 \cdot C_f \tau^5} \cdot e^{\left(\frac{-t}{\tau}\right)} \tag{3.18}$$

The output signal peaking time is determined by taking the derivative of Equation 3.18 with respect to time, t, setting the result equal to zero, and then solving for t. The peaking time was found to be at time $t = 2.764\tau$. Substituting this peaking time into Equation 3.18, and multiplying by the charge of an electron yields,

$$V_{op}\left(\frac{Volts}{electron}\right) = 0.068557 \cdot \left(\frac{qK}{C_f}\right). \tag{3.19}$$

From the definition of the ENC it follows that,

$$\overline{ENC^2_{thermal}}(rms - electrons)^2 = \frac{\overline{V^2_{thermal}}}{V^2_{op}}. \tag{3.20}$$

Substituting Equations 3.16 and 3.19 into Equation 3.20 yields Equation 3.21, an expression for the mean-squared equivalent noise charge due to the channel thermal noise of the input FET alone. Equation 3.21 can be expanded by substituting the equation for

g_m to obtain an expression in terms of the input device's parameters (i.e. length and width).

$$\overline{ENC_{thermal}^2} = 1.662 \cdot \frac{kT}{g_m \tau} \cdot \left(\frac{C_t}{q}\right)^2 \qquad \textbf{(3.21)}$$

3.3.1.2 *Flicker Noise ENC*

The flicker noise component of the ENV^2 at the output of the CSA is related to the input of the CSA by Equation 3.11, as was the thermal noise component. Therefore, the ENC due to the flicker noise is found by first substituting Equation 3.5 into Equation 3.11 to obtain Equation 3.22,

$$ENV_{oA}^2\left(\frac{V^2}{Hz}\right) = \left|\frac{(C_t)}{C_f}\right|^2 \cdot \frac{K_f}{C_{ox}^2 WL f^{AF}} \qquad \textbf{(3.22)}$$

Substituting Equations 3.22 and 3.13 into Equation 3.12 with AF set to unity and integrating over frequency yields the mean-squared noise voltage at the output of the pulse shaper, Equation 3.23.

$$\overline{V_{flicker}^2} = \frac{K_f K^2}{40\left(C_{ox}^2 WL\right)} \cdot \left(\frac{C_t^2}{C_f^2}\right) \qquad \textbf{(3.23)}$$

The $\overline{ENC^2}$ due to the flicker noise is found by substituting Equations 3.23 and 3.19 into Equation 3.20 to obtain Equation 3.24,

$$\overline{ENC^2_{flicker}} = 5.32 \cdot \frac{K_f}{\left[C_{ox}^2 WL\right]} \cdot \left(\frac{C_t^2}{q^2}\right) . \tag{3.24}$$

3.3.1.3 *Detector Noise ENC*

The voltage noise spectrum at the output of the CSA is related to a current noise spectrum at the input of the CSA by Equation 3.25.

$$ENV_{oA}^2 = \left|\frac{1}{j2\pi f C_f}\right|^2 \cdot ENA_{iA}^2 . \tag{3.25}$$

The voltage noise spectrum at the output of the pulse shaper due to the leakage current of the detector is found, as in the previous analysis, by substituting Equation 3.2 into Equation 3.25. The result and Equation 3.13 are substituted into Equation 3.12, and integrating over frequency yields Equation 3.26,

$$\overline{V_{\text{det}}^2} = \frac{7qI_{leakage}K^2\tau}{512C_f^2} . \tag{3.26}$$

Substituting Equations 3.26 and 3.19 into Equation 3.20 gives the $\overline{ENC^2}$ due to the detector shot noise, Equation 3.27.

$$\overline{ENC_{\det}^2} = \frac{2.909 I_{leakage} \tau}{q} \quad . \tag{3.27}$$

3.3.1.4 Feedback Resistor ENC

The thermal noise of a feedback resistor will also appear at the input of the CSA as a current noise spectrum, and the noise voltage spectrum at the output of the CSA is obtained from Equation 3.25. Following the same analysis technique as presented for the detector noise current, the ENC at the output of the pulse shaper due only to the feedback resistor noise current is given by Equation 3.28.

$$\overline{ENC_{Rf}^2} = \frac{5.818 kT\tau}{R_f q^2} \tag{3.28}$$

3.3.2 Noise Optimization of the Input MOSFET

The total output equivalent noise charge is the geometric sum of the individual ENC contributors, Equation 3.9. Other than the flicker noise, each ENC component is dependent on the choice of τ in the pulse shaper's transfer function, Equation 3.1, which has been defined for the project to be 100 ns. Without the flexibility of choosing an optimum τ, the total output ENC must be minimized by minimizing the individual contributors. Unfortunately, the detector's leakage noise and the feedback resistor's ENC can only be reduced by decreasing the leakage current and increasing the value of the feedback resistance, respectively. However, both the thermal ENC and the flicker ENC

of the input FET are dependent on the dimensions of the device, which suggest that minimization is possible by finding an optimum size of the input device. It is a common practice to optimize the input device separately for thermal and flicker noise at first, then use those optimizations to find a global optimization [33, 34]. This can be done by determining which noise source is the dominant one for the shaping filter's time constant, and choosing the device parameters based on that [35]. Since the MicroCAT shaping filter has a center frequency of approximately 1.2 MHz, the choice of the input FET's dimensions will be based on the results of both optimizations.

3.3.2.1 *Optimization of Channel Thermal Noise*

The expression for the $\overline{ENC^2}$ due to the channel thermal noise is given by Equation 3.21. The device dependant parameters of Equation 3.21 that can be optimized are the total capacitance, C_t, and the transconductance, g_m. Thus, in order to minimize Equation 3.21, the quotient of Equation 3.29 must be minimized.

$$\frac{C_t^2}{g_m} \Rightarrow \text{minimum} \tag{3.29}$$

The total capacitance can be expanded and expressed in terms of the input device's parameters, as can the transconductance, which gives Equation 3.30,

$$\frac{(C_{\det} + C_{stray} + C_f + \frac{2}{3}\alpha C_{ox} WL)^2}{\sqrt{2\mu C_{ox} Id \frac{W}{L}}}, \tag{3.30}$$

where $\alpha L = (L + 3L_D)$, and L_D is the underdiffusion parameter specific to the fabrication process [33]. Equation 3.30 is minimized by taking the derivative with respect to W, setting the result equal to zero, and then solving for W. The final result is presented in Equation 3.31, and is in agreement with the minimization presented by Chang & Sansen [33, 34].

$$W_{opt} = \frac{(C_{\det} + C_f + C_{stray})}{2\alpha C_{ox} L} \tag{3.31}$$

This result suggests that when thermal noise dominates, the CSA input capacitance should be made equal the sum of the detector, feedback, and stray capacitance divided by three. However, if one assumes that the feedback and stray capacitance are small compared to the detector capacitance, the input capacitance should approximately equal the detector capacitance divided by three ($C_{det}/3$).

3.3.2.2 *Optimization of Flicker Noise*

The expression for the $\overline{ENC^2}$ due to the flicker noise is given by Equation 3.24, which suggests that optimization can be accomplished by minimizing the quotient of Equation 3.32.

$$\frac{C_t^2}{WL} \Rightarrow \text{minimum} \qquad \textbf{(3.32)}$$

The optimization process is the same as it was for thermal noise, except the optimum FET area is determined by

$$WL_{opt} = \frac{3(C_{det} + C_f + C_{stray})}{2\alpha C_{ox}} \quad . \qquad \textbf{(3.33)}$$

This result, also in agreement with that presented by Change & Sansen [33, 34], suggests that the optimum input capacitance is equal to the sum of the detector, feedback, and the stray capacitance. The flicker noise coefficient, K_f, has often been found to be a factor of 40 less for a PMOS device than that of an NMOS device [32], therefore the input device should be a PMOS device.

3.3.2.3 *Input FET's Optimal Dimensions*

The device parameters taken from the PMOS level 3 SPICE model for the AMI 1.2 μm fabrication process are given in Table 3.1. With the parameters presented in Table 3.1, C_{det} = 4 pF, C_{stray} = 1 pF, and C_f = 100 fF, the optimum gate width found for thermal noise optimization, Equation 3.31, was 1285 μm (L = 1.8 μm). The gate width found for flicker noise optimization, Equation 3.33, was 3856 μm (L = 1.8 μm). As suggested by

Table 3.1: Level 3 SPICE model parameters for AMI 1.2 μm PMOS devices

Mobility, μ	203.6 $cm^2V^{-1}sec^{-1}$
Capacitance, C_{ox}	105.6 $nFcm^{-2}$
Underdiffusion, L_D	0.0263 μm

Chang & Sansen [33,34], the optimum gate width is not the same for thermal as for flicker noise and therefore some compromise must be made. Since the pulse shaper's center frequency lies in a region where both thermal and flicker noise (for MOSFET devices) can be major contributors to the total ENC, a midrange value of gate width was chosen. The input device's gate width was chosen to be 2160 μm, and the length was chosen to be 1.8 μm.

With these dimensions established, the ENC of each noise source and the total ENC was plotted versus the shaper's time constant, Figure 3.5. This plot was produced using a drain current of 500 μA to place the input device into strong inversion, a feedback resistance of 400 MΩ, a detector leakage current of 1 nA, a detector capacitance of 4 pF with 4 pF stray capacitance, and a flicker noise coefficient of $K_f = 3.2 \times 10^{-31}$ $F^2V^2cm^{-2}$ [31]. The total ENC is 290 electrons at the chosen shaping time constant, τ, of 100 ns. The optimum shaping time constant for the chosen device parameters is between 500 and 600 ns where the total ENC is 206 electrons. The graph also indicates that the thermal noise is dominant at 100 ns, and that further optimization may be possible by choosing a gate width closer to that given by the thermal noise optimization criterion, Equation 3.31. However, parameters such as the stray capacitance are merely estimates; therefore, it was

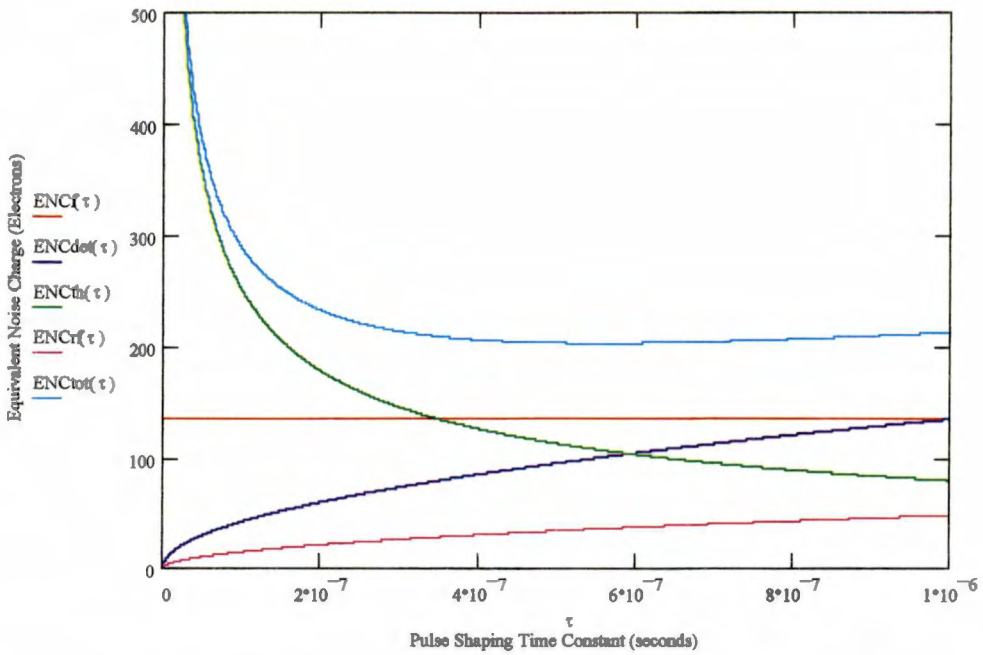


Figure 3.5: Theoretical ENC versus shaping time constant (τ = 100 ns for 500 ns shaping time, I_d = 500 μA, C_f = 4 pF, C_{stray} = 4 pF, and R_f = 400 MΩ)

decided to use the parameters that were initially chosen.

3.4 Inverting Voltage Amplifier Design and Analysis

An inverting voltage amplifier is required to produce the loop gain for the CSA. In this section the design and analysis of the CMOS voltage amplifier is discussed. The amplifier was fabricated in an AMI 1.2 μm process through the MOSIS program. Circuit simulations were performed with HSPICE simulation tools using the BSIM 3 (Level = 49) device models listed on the MOSIS World Wide Web site [36]. The device parameters used for hand calculations, such as mobility, μ, and C_{ox}, were taken from the

Table 3.2: AMI 1.2 μm level 3 SPICE model parameters

Parameter	NMOS	PMOS	Units
PHI, 2ϕ	0.7	0.7	V
TOX	327	327	Angstroms
VT0	0.7194	-0.8165	V
KP, μCox	69.56	21.5	μmV^{-2}
U0, μ	658.7	203.6	$cm^2V^{-1}s^{-1}$
NSUB	1.773E+16	4.875E+15	cm^{-3}
GAMMA, γ	0.7265	0.3809	$V^{0.5}$
L_D	0.1183	0.0263	μm

level 3 SPICE models [36], and are summarized in Table 3.2. The complete listing of both the level 49 and level 3 models are given in Appendix A.

3.4.1 Cascode Circuit Optimization Using Local Feedback

The cascode and folded cascode circuits are frequently used to provide an amplifier with a wide bandwidth and large DC signal gain [30, 33]. A basic PMOS cascode circuit is illustrated in Figure 3.6. Two important phenomena occur because of the low impedance looking into the source of M2. The capacitance at the drain of M1 is in parallel with a low impedance, and therefore the RC time constant is reduced, forcing the pole at that node to a higher frequency. The second important outcome is that M1 is not able to produce a large voltage gain from the gate to the drain, and as a result the

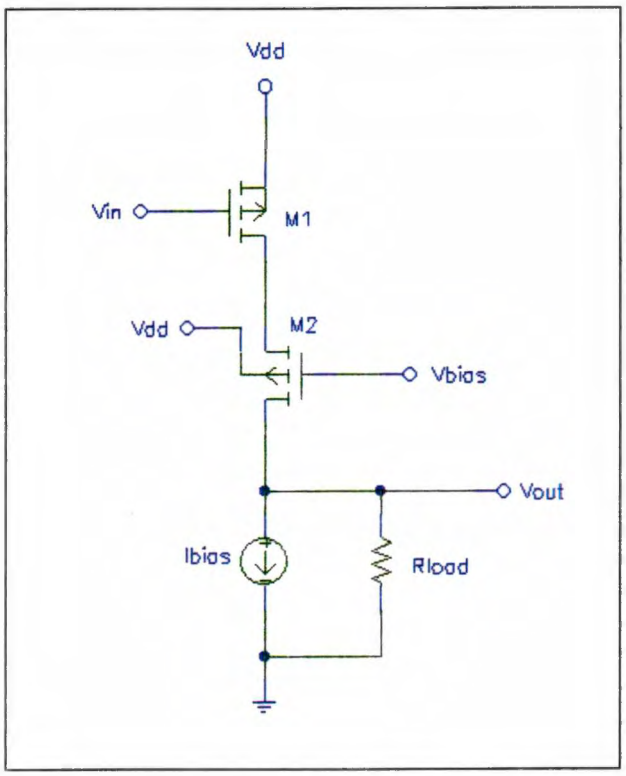


Figure 3.6: Basic cascode topology

capacitance at the gate of M1 is not increased significantly by the Miller effect. The circuit develops a dominate pole at the drain of M2, and if the pole at the drain of M1 has been pushed out to a very high frequency, the circuit exhibits a frequency response that approaches that of a single pole circuit. For the circuit to develop a large DC voltage gain, the load resistance, R_{load}, must be made large. Typically for CMOS circuits the load resistance is provided by a high impedance current source, and the value of the current source output impedance could be much larger than the drain to source impedance, r_{ds2}, of M2. Unfortunately, the impedance looking into the source of M2, given by Equation 3.34, can become large as the load impedance is increased above r_{ds2}, and the advantages of the cascode circuit become impaired. As an example, consider the circuit of Figure

3.6, with the W/L ratio of M1 set to the previously determined optimum dimensions (2160 μm/1.8 μm), and with the W/L ratio of M2 set to 240 μm/1.2 μm to provide a large transconductance.

$$R_{is2} = \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_{load}}{r_{ds2}}\right) \tag{3.34}$$

M1 and M2 have the same drain current of 500 μA, which provides a large g_m for both devices so that the DC gain is made large. R_{load} should be large also to improve the DC gain, therefore assume R_{load} is 565 kΩ. The drain to source resistance and transconductance for each device is listed in Table 3.3. The input resistance given by Equation 3.34 was calculated to be R_{is2} = 40.13 kΩ. The resistance looking into the drain of M2 is given by Equation 3.35, and was calculated to be R_{o2} = 57.4 kΩ.

$$R_{o2} = r_{ds2}\left(1 + r_{ds1}(g_{m2} + g_{mb2})\right) + r_{ds1} \tag{3.35}$$

The circuit voltage gain is given by Equation 3.36, and it was calculated to be A_v = -239.

$$Av = \frac{-g_{m1}R_{load}\left(g_{m2}r_{ds1}r_{ds2} + r_{ds1}\right)}{\left(g_{m2}r_{ds1}r_{ds2} + r_{ds1} + r_{ds2} + R_{load}\right)} \tag{3.36}$$

The large input impedance seen when looking into the source of M2 allows the input

Table 3.3: Parameters for Figure 3.6 (resistance taken from SPICE operating point)

Device	W	L	Id	rds	g_m
M1	2160 μm	1.8 μm	500 μA	3360 Ω	5.14 mS
M2	240 μm	1.2 μm	500 μA	6230 Ω	2.285 mS (with g_{mb} added)

device to develop it's maximum voltage gain, $A_{vM1} = -g_{m1}r_{ds1}$, which for the parameters given is equal to –17.3. Also, since the parasitic capacitance of M1 is larger than that of M2, the pole at that node could lie close to the pole at the drain of M2, preventing the circuit from having a near single pole frequency response.

One method of improving the common cascode circuit is to add a negative feedback loop around the cascode device, M2. This concept is not new, and has been used successfully by Paulus [30] and Britton et al. [37]. A simple method of implementing the "local" feedback loop is to add transistor M3, as shown in Figure 3.7. Transistor M3 is sized so that it's gate to source voltage biases transistor M1 well into the saturation region, and the gate to source voltage of M2 biases M3 in saturation as well. Not only does the local feedback loop act to restore the desired characteristics of the cascode circuit by lowering the impedance at the input (source of M2), but also improves the DC gain by increasing the impedance seen looking into the drain of M2. The new input impedance is determined using Blackman's theorem [29] as given by Equation 3.37,

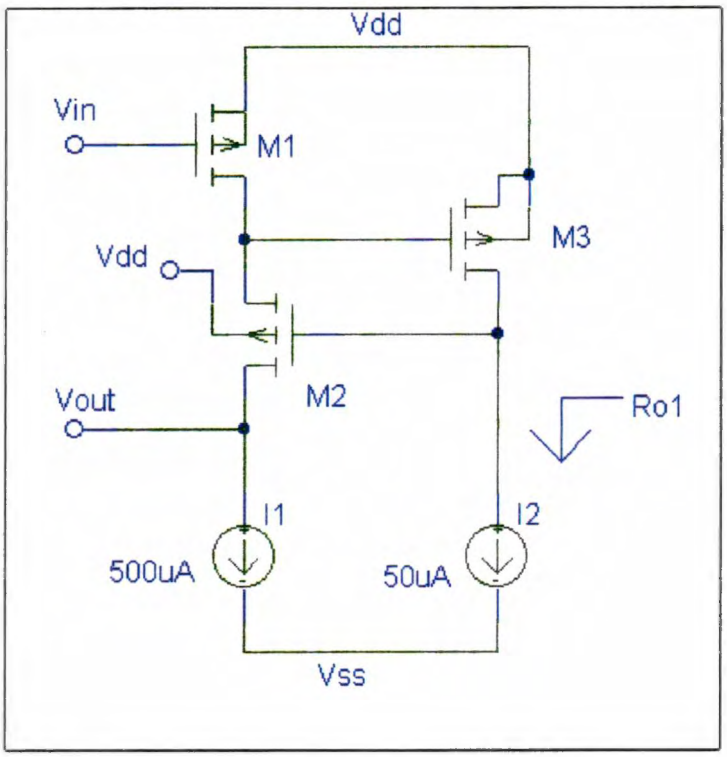


Figure 3.7: Cascode circuit with local feedback transistor, M3, added

$$R_{in}^{CL}(\Omega) = R_{in}^{OL}\left[\frac{1-T_{sc}}{1-T_{oc}}\right], \qquad \textbf{(3.37)}$$

where T_{sc} and T_{oc} are the short circuit and open circuit loop transmissions, respectively, and R_{in}^{OL} is the input impedance when the effects of the feedback path are neglected. The W/L ratio of M3 is 240 μm/1.8 μm with a bias current of 50 μA, which gives a drain to source resistance, r_{ds}, of 31.3 kΩ and a transconductance, g_m, of 0.56 mAV^{-1}. The open circuit loop transmission is calculated by finding the voltage gain around the local feedback loop with the source of M2 open circuited, which effectively takes the drain to source resistance of M1 out of the calculation, Equation 3.38.

$$T_{OC} = -g_{m3}\left(\frac{r_{ds3}R_{o1}}{r_{ds3}+R_{o1}}\right)\cdot\left(\frac{g_{m2}}{g_{m2}+g_{ds2}}\right) \qquad \textbf{(3.38)}$$

The first term is the common source voltage gain of M3, where the load resistance, R_{o1}, is much larger than the drain to source resistance of M3. The second term is the common drain voltage gain of M2. T_{oc} was calculated to be –16.32. T_{sc} is calculated by shorting the source of M2 to ground, which gives $T_{sc} = 0$ simply by observation. Substituting the values obtained for the short and open circuit loop transmissions into Equation 3.37 gives a closed loop input impedance of $R_{in}^{CL} = 2.32\ k\Omega$.

The closed loop output impedance is given by Equation 3.39,

$$R_{od2}^{CL} = R_{od2}^{OL}\left[\frac{1-T_{SC}}{1-T_{OC}}\right], \qquad \textbf{(3.39)}$$

where the short and open circuit loop transmission are determined by calculating the loop gain with the drain of M2 at short circuit and open circuit, respectively. T_{sc} is given by Equation 3.40,

$$T_{SC} = -g_{m3}\left(\frac{r_{ds3}R_{o1}}{r_{ds3}+R_{o1}}\right)\cdot\left(\frac{g_{m2}}{g_{m2}+g_{ds2}+g_{ds1}}\right), \qquad (3.40)$$

and was found to be –14.55. When the open circuit calculation is performed, R_{load} effectively goes to infinity, which forces the common drain voltage gain of M2 to zero so

that the open-circuit loop transmission is zero. Substituting the short and open circuit loop transmissions into Equation 3.39 gives the new output impedance of R_{od}^{CL} = 892.75 kΩ.

The DC loop transmission of the internal loop is determined by calculating the voltage gain around the local loop with both the input and output connections in place, and is given by Equation 3.41,

$$T_{DC} = -g_{m3}\left(\frac{r_{ds3}R_{o1}}{r_{ds3}+R_{o1}}\right)\cdot\left(\frac{g_{m2}}{g_{m2}+g_{ds2}+g_{ds1}+R_{load}g_{ds1}g_{ds2}}\right). \qquad \textbf{(3.41)}$$

The DC loop transmission is reduced significantly due to the low drain to source impedance of M1 and the high load resistance, R_{load}, and was found to be –1.34. The open loop voltage gain of the circuit, with local feedback, is given by Equation 3.42,

$$A_{Vactual}^{OL} = A_{Videal}^{OL}\left(\frac{-T_{DC}}{1-T_{DC}}\right), \qquad \textbf{(3.42)}$$

and the ideal open loop gain defined for $T_{DC} = \infty$ is given by Equation 3.43.

$$A_{Videal}^{OL} = -g_{m1}R_{load} \qquad \textbf{(3.43)}$$

The ideal gain was calculated to be –2904, and the actual gain was calculated to be -1663. The low value of DC loop transmission of the internal loop reduced the open loop gain of

the circuit by nearly half. The open loop voltage gain of the circuit may also be calculated by direct nodal analysis, as presented in Appendix B, and the DC voltage gain of the circuit, with local feedback, is given by Equation 3.44,

$$A_{VDC} = \frac{-R_{load}\left(r_{ds1}g_{m1}\left(g_{m2}g_{m3}r_{ds3}r_{ds2} + g_{m2}r_{ds2} + 1\right)\right)}{R_{load} + g_{m2}g_{m3}r_{ds3}r_{ds2}r_{ds1} + g_{m2}r_{ds2}r_{ds1} + r_{ds2} + r_{ds1}}, \qquad \textbf{(3.44)}$$

and was calculated to be –1770, a factor of 7.4 larger than that of the simple cascode circuit without local feedback.

Typically, a common drain output stage is added as a buffer to provide sufficient load driving capability, which will result in a small decrease in the open loop voltage gain of the amplifier. At DC the loop transmission of the complete CSA will be equal to the forward gain of the voltage amplifier, but at low frequencies the feedback network will attenuate the loop transmission by a factor of $C_f / (C_f + C_{det} + C_{stray} + C_{in})$.

3.4.2 *Improved Cascode Circuit*

As discussed in the previous section, the local feedback loop improves the performance of the simple cascode circuit by decreasing the impedance seen looking into the source of the cascoded device, M2, and increasing the impedance seen looking into the drain of M2. However, the DC loop transmission of that circuit was found to be just greater than unity, which degrades the ideal DC gain by a factor of nearly one half. In an effort to improve the performance of the preamplifier, the circuit of Figure 3.8 was designed. In this section, the preamplifier designed for the MicroCAT project, which

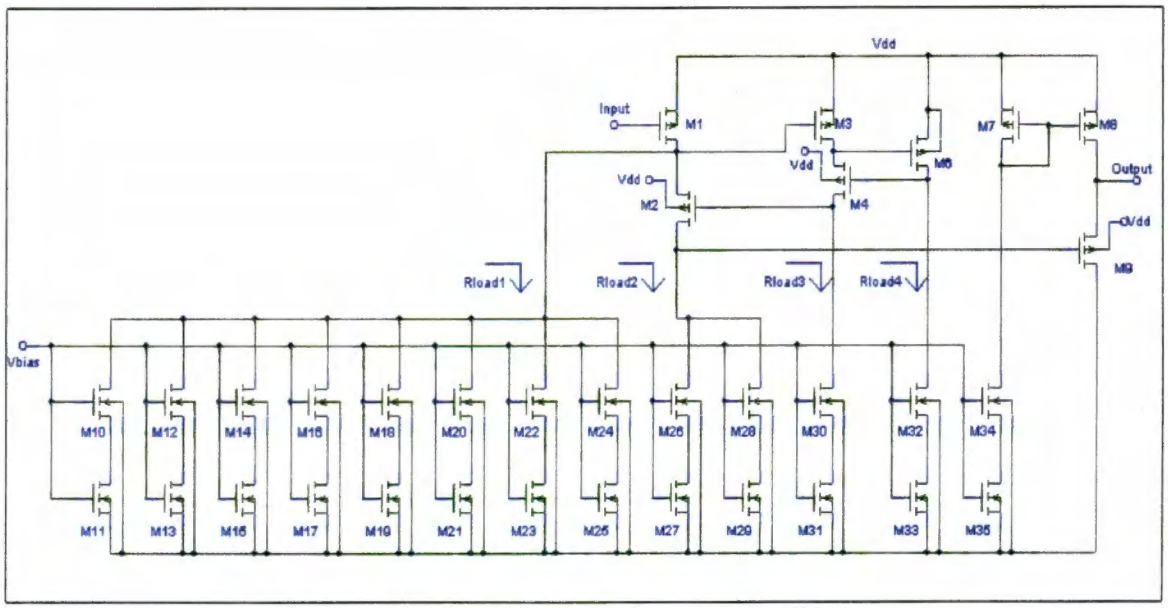


Figure 3.8: Improved cascode preamplifier schematic

makes use of the same local feedback technique, is evaluated. All aspects of the circuit design are discussed including biasing, circuit stability, and noise performance.

3.4.2.1 Circuit Design

The preamplifier designed for the MicroCAT project has two local feedback loops. The first feedback path is formed around M2 by transistors M3 and M4, and the second feedback path is formed around M4 by transistor M6. Upon close inspection, one should notice that transistors M3, M4 and M6 form the exact circuit that was analyzed in Section 3.4.1. Transistor M9 acts as an output buffer, and it is biased by transistors M7, M8, M34, and M35. Transistors M10 – M33 serve to bias the main circuit, where the current mirrors are shown in a parallel arrangement for better comparison to the actual

layout. The device parameters used for hand calculation of the preamplifier's performance are listed in Table 3.4. The gate dimensions of M1 were chosen to give an optimum noise performance, and to provide a large transconductance. The gate dimensions of transistors M2 through M6 were chosen to provide both moderate transconductance and to satisfy the biasing conditions of the circuit.

Analysis of the preamplifier shall begin with the performance of the inner most local feedback loop implemented with transistor M6. The impedance seen looking into the source of M4 with the feedback loop neglected is given by Equation 3.45,

$$R_{in4}^{OL} = \frac{1}{g_{m4} + g_{mb4}}\left(1 + \frac{R_{load3}}{r_{ds4}}\right), \tag{3.45}$$

where R_{load3} is the output impedance of the source-degenerated current mirror, which is given by Equation 3.46,

$$R_{load3} = r_{ds30}\left[1 + \left(g_{m30} + g_{mb30}\right)r_{ds31}\right] + r_{ds31}, \tag{3.46}$$

and was calculated to be 5.49 MΩ. Substituting this value into Equation 3.45 gives an open loop input impedance of 328.6 kΩ. The impedance seen looking into the drain of M4 with the feedback loop neglected is given by Equation 3.47,

$$R_{od4}^{OL} = r_{ds4}\left[1 + \left(g_{m4} + g_{mb4}\right)r_{ds3}\right] + r_{ds3}, \tag{3.47}$$

Table 3.4: Improved cascode preamplifier transistor parameters

Transistor	W (μm)	L (μm)	gds (S)	gm (S)	gmb (S)	Id (A)	Rds (Ω)
M1	2160	1.8	3.03E-04	5.25E-03	1.12E-03	5.00E-04	3.30E+03
M2	120	1.2	4.73E-05	6.80E-04	8.24E-05	1.00E-04	2.11E+04
M3	96	1.2	2.95E-05	4.42E-04	7.68E-05	5.00E-05	3.39E+04
M4	120	1.2	3.16E-05	4.86E-04	5.94E-05	5.00E-05	3.17E+04
M6	96	1.2	3.04E-05	4.64E-04	8.06E-05	5.00E-05	3.29E+04
M7	60	1.2	2.45E-05	3.52E-04	6.22E-05	5.00E-05	4.08E+04
M8	300	1.2	1.25E-04	1.79E-03	3.17E-04	2.50E-04	8.03E+03
M9	300	1.2	1.32E-04	2.00E-03	2.45E-04	2.50E-04	7.59E+03
M10	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M11	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M12	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M13	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M14	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M15	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M16	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M17	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M18	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M19	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M20	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M21	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M22	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M23	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M24	24	6	6.90E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M25	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04
M26	24	6	7.36E-07	1.40E-04	4.52E-05	5.00E-05	1.36E+06
M27	24	18	5.85E-05	4.39E-05	2.00E-05	5.00E-05	1.71E+04
M28	24	6	7.36E-07	1.40E-04	4.52E-05	5.00E-05	1.36E+06
M29	24	18	5.85E-05	4.39E-05	2.00E-05	5.00E-05	1.71E+04
M30	24	6	7.57E-07	1.40E-04	4.52E-05	5.00E-05	1.32E+06
M31	24	18	5.85E-05	4.39E-05	2.00E-05	5.00E-05	1.71E+04
M32	24	6	7.40E-07	1.40E-04	4.52E-05	5.00E-05	1.35E+06
M33	24	18	5.85E-05	4.39E-05	2.00E-05	5.00E-05	1.71E+04
M34	24	6	6.91E-07	1.40E-04	4.52E-05	5.00E-05	1.45E+06
M35	24	18	5.82E-05	4.39E-05	2.00E-05	5.00E-05	1.72E+04

and was calculated to be 651.7 kΩ. With the local feedback loop, M6, in place, the closed loop input impedance is determined using Blackman's theorem,

$$R_{in4}^{CL}(\Omega) = R_{in4}^{OL}\left[\frac{1-T_{sc}}{1-T_{oc}}\right], \tag{3.48}$$

where the open circuit loop transmission is determined by opening the circuit at the source of M4, and is given by Equation 3.49.

$$T_{OC} = -g_{m6}\left(\frac{r_{ds6}R_{load4}}{r_{ds6}+R_{load4}}\right)\cdot\left(\frac{g_{m4}}{g_{m4}+g_{ds4}}\right) \tag{3.49}$$

T_{oc} was calculated to be –14.25, and T_{sc}, which is determined by short circuiting the source of M4, is zero simply by observation. The closed loop input impedance was calculated to be 21.5 kΩ.

The closed loop output impedance is given by Equation 3.50,

$$R_{od4}^{CL} = R_{od4}^{OL}\left[\frac{1-T_{SC}}{1-T_{OC}}\right], \tag{3.50}$$

where T_{sc} is calculated with the drain of M4 shorted to ground, and is given by Equation 3.51.

$$T_{SC} = -g_{m6}\left(\frac{r_{ds6}R_{load4}}{r_{ds6}+R_{load4}}\right)\cdot\left(\frac{g_{m4}}{g_{m4}+g_{ds4}+g_{ds3}}\right) \tag{3.51}$$

T_{sc} was calculated to be –13.5. T_{oc} is calculated by open circuiting the drain of M4, which effectively takes R_{load3} to infinity, thus reducing the open loop transmission to zero. The closed loop impedance seen looking into the drain of M4 was calculated to be 9.44 MΩ.

The DC loop transmission of this local loop is given by Equation 5.52,

$$T_{DC} = -g_{m6}\left(\frac{r_{ds6}R_{load4}}{r_{ds6}+R_{load4}}\right)\cdot\left(\frac{g_{m4}}{g_{m4}+g_{ds4}+g_{ds3}+R_{load3}g_{ds3}g_{ds4}}\right), \tag{3.52}$$

and was calculated to be –1.3. The ideal voltage gain composed of transistors M3, M4 and M6 is given by Equation 5.53,

$$Av_{ideal} = -g_{m3}R_{load3}, \tag{3.53}$$

and was calculated to be –2427. However, the actual gain is given by Equation 3.54,

$$Av_{actual} = Av_{ideal}\left(\frac{-T_{DC}}{1-T_{DC}}\right), \tag{3.54}$$

and was calculated to be –1372. As seen in the example of the previous section, the voltage gain of this cascode circuit has been attenuated by a factor of nearly one half

because of poor DC loop transmission. By direct nodal analysis of this circuit, using Equation 3.44 and making the appropriate subscript changes, a voltage gain of –1473 is obtained, and simulations performed using HSPICE yield a voltage gain of –1480. The frequency response of this circuit was not considered here, but will be discussed in Section 3.4.2.2.

Now that the inner most local feedback loop has been analyzed, the outer local feedback loop can be examined. The analysis may be simplified by considering transistors M3, M4 and M6 as a single gain block that form a negative feedback loop around transistor M2, as shown in Figure 3.9. This gain block will have a voltage gain of $A_v = -1372$, as given by Equation 3.54. The analysis of this feedback loop shall proceed in the same manor as with the inner local feedback loop. The impedance seen looking into the source of M2, neglecting the feedback loop, is given by Equation 3.55,

$$R_{in2}^{OL} = \frac{1}{g_{m2} + g_{mb2}}\left(1 + \frac{R_{load2}}{r_{ds2}}\right). \tag{3.55}$$

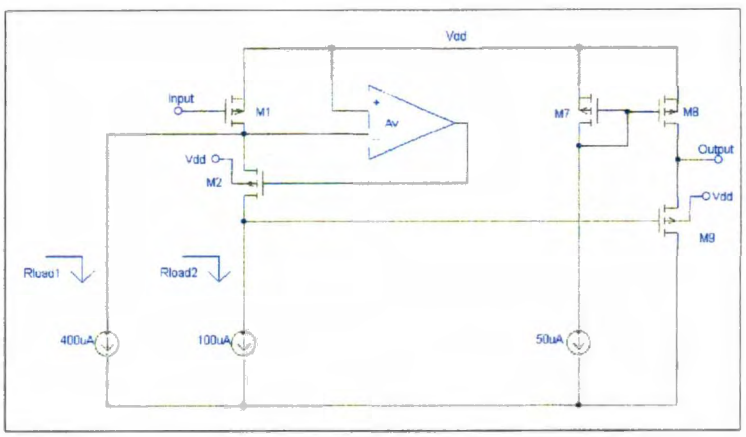


Figure 3.9: Preamp with outer feedback loop replaced with a gain block

Since each of the current source mirrors are identical, and M2 is biased with two of those mirrors, the load impedance R_{load2} is simply ½ R_{load3}. R_{load2} was calculated to be 2.74 MΩ, which gives an impedance looking into the source of M2 of 171.64 kΩ. As for the analysis of the inner feedback loop, the closed loop input impedance is given by Blackman's theorem, Equation 3.48. Tsc is determined with the source of M2 short-circuited to ground, which gives a Tsc of zero by observation. Toc is given by Equation 3.56,

$$T_{OC} = -A_V\left(\frac{g_{m2}}{g_{m2}+g_{ds2}}\right), \tag{3.56}$$

and was calculated to be –1283, which results in a closed loop input impedance of 134 Ω. The impedance seen looking into the drain of M2, neglecting the feedback loop, is given by Equation 3.57 neglecting the high impedance R_{load1},

$$R_{od2} = r_{ds2}\left[1+\left(g_{m2}+g_{mb2}\right)r_{ds1}\right]+r_{ds1}, \tag{3.57}$$

and was calculated to be 77.5 kΩ. The open circuit loop transmission is calculated by open circuiting the drain of M2, which results in a R_{load2} of infinity, and thus reduces T_{oc} to zero. The short circuit loop transmission is calculated by shorting the drain of M2 to ground, resulting in a T_{sc} given by Equation 3.58, again neglecting the high impedance of R_{load1},

$$T_{SC} = -A_V \cdot \left(\frac{g_{m2}}{g_{m2} + g_{ds2} + g_{ds1}} \right) \tag{3.58}$$

Tsc was calculated to be –1231.5, which when substituted into Blackman's theorem yields a closed loop output impedance of 95.52 MΩ. The DC loop transmission is given by Equation 3.59,

$$T_{DC} = -A_V \cdot \left(\frac{g_{m2}}{g_{m2} + g_{ds2} + g_{ds1} + R_{load2} g_{ds2} g_{ds1}} \right), \tag{3.59}$$

and was calculated to be –25.8. The ideal voltage gain from the gate of M1 to the drain of M2, given by Equation 3.60,

$$Av_{ideal} = -g_{m1} R_{load2}, \tag{3.60}$$

was calculated to be –14,385. The ideal gain is attenuated by the finite loop transmission, and the actual voltage gain was calculated using Equation 3.54 to be –13,850. Direct nodal analysis yields Equation 3.61 for the actual voltage gain,

$$A_{VDC} = \frac{R_{load2}\left(r_{ds1} g_{m1}\left(g_{m2} A_V r_{ds2} - g_{m2} r_{ds2} - 1\right)\right)}{R_{load2} - g_{m2} A_V r_{ds2} r_{ds1} + g_{m2} r_{ds2} r_{ds1} + r_{ds2} + r_{ds1}}, \tag{3.61}$$

where Av is the voltage gain of the outer most local feedback loop, calculated to be –1372 using Equation 3.54. Equation 3.61 gives –13,900 for the actual DC voltage gain, and HSPICE simulations give –13,910.

This gain is attenuated by the common drain buffer transistor, M9. The total open loop gain for the preamplifier is given by Equation 3.62,

$$A_V^{OL} = -13{,}850\left(\frac{g_{m9}}{g_{m9} + g_{ds9} + g_{ds8} + g_{mb9}}\right), \tag{3.62}$$

which yields a final open loop DC voltage gain of –11,071 for the preamplifier by hand analysis, and is comparable to the –11,150 obtained by HSPICE simulations.

3.4.2.2 Stability of the Local Feedback Loops

Each negative feedback loop of the preamplifier must be examined for stability, and if either of the loops displays a low phase margin it must be increased by some method of compensation. Analysis by hand of the local feedback loop transmission is very complex, especially for the outer loop because it has an embedded feedback loop. Therefore, HSPICE simulations will be relied on to study the stability of the negative feedback loops. However, a nodal analysis was done by hand for the innermost loop in order to validate the HSPICE results.

In order to determine the loop transmission using HSPICE, only the AC loop can be broken. The DC loop must remain intact so that the bias conditions are preserved. A variety of methods have been studied to accomplish this task, but the AC decoupling

circuit chosen for this analysis is presented in Figure 3.10. The RC time constant for the decoupling circuit is made very large by selecting a resistance of R = 500 MΩ, and a capacitance of C = 0.5 Farads. This creates a low-pass circuit with a –3dB frequency of 0.64×10^{-9} Hz. The test signal generator has an AC magnitude of 1, and the loop transmission magnitude and phase are measured directly from the input node of the decoupling circuit (V_r, the return signal). The complex impedance, Z_{load}, is the loading that the node would have seen prior to breaking the loop.

The innermost loop transmission and phase shift plots as predicted by HSPICE simulations are presented in Figures 3.11 and 3.12, respectively. The phase of the return signal at DC is shifted 180 degrees from that of the test signal, corresponding to the overall single inversion of the negative feedback loop. For the loop to be stable, at no frequency while the magnitude of the loop transmission is greater than unity can the phase deviate greater than 180 degrees from the phase shift at DC in either direction. The phase plots generated by HSPICE are measured with respect to ground, not the test signal phase, and therefore begin at zero.

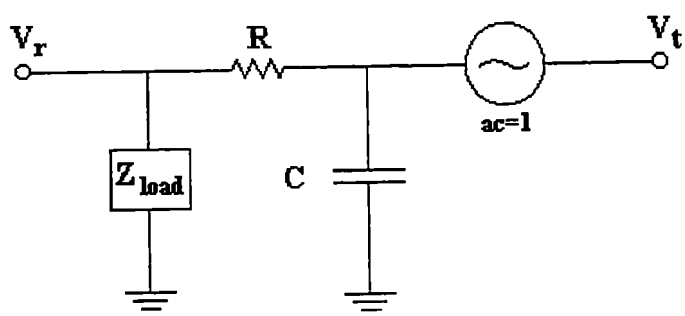


Figure 3.10: AC decoupling circuit for determining loop transmission

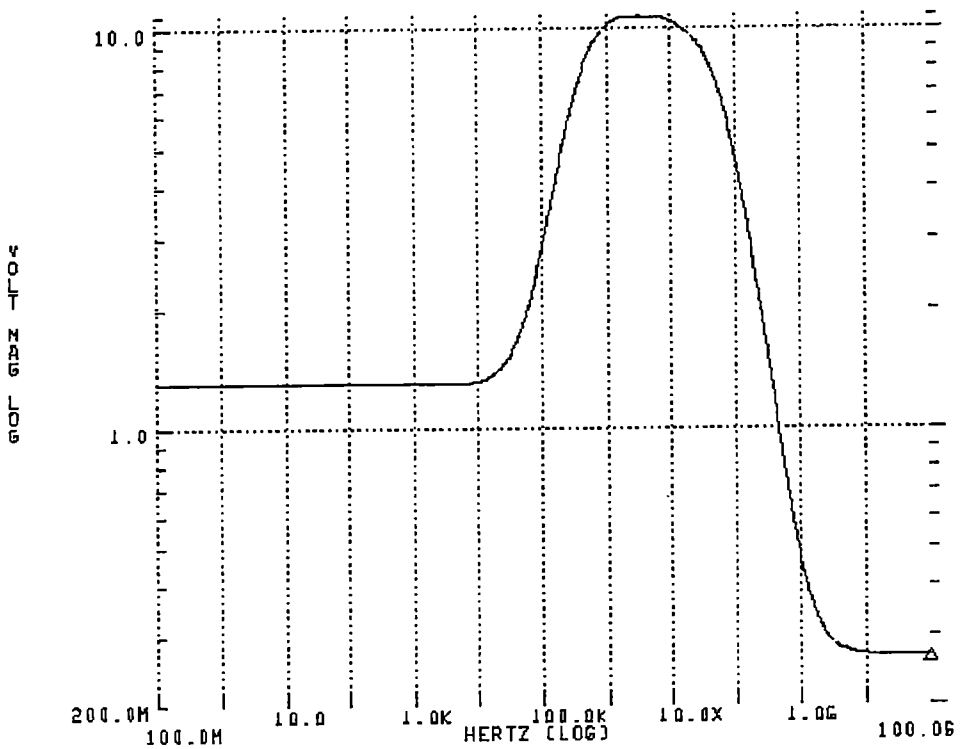


Figure 3.11: Loop transmission magnitude of the innermost feedback loop

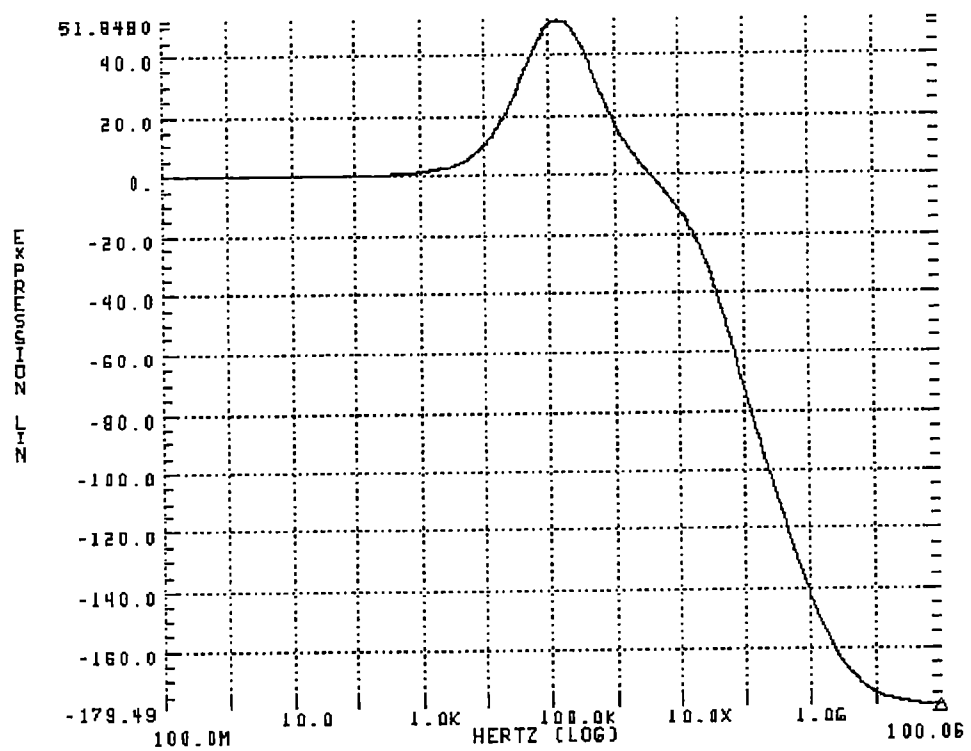


Figure 3.12: Loop transmission phase of innermost feedback loop

The innermost loop was broken at the gate of M4, where the test signal was applied, and the return signal was measured at the drain of M6. The gate of M3 was biased with a DC supply voltage, effectively breaking the outer loop to prevent feedback that could adversly affect the measurement. The loop transmission has a left half plane (LHP) zero at approximately 20 kHz that causes the magnitude to increase at 20 dB per decade. Poles at the gate of M6 and the gate of M4 cause the magnitude to turn back down, and drop at –20 dB per decade. A pole occuring at greater than 200 MHz causes the magnitude to drop at –40 dB per decade, and increases the total phase shift to –180 degrees. When the magnitude crosses the unity gain level, the largest phase shift that has occurred is approximately –105 degrees, leaving 75 degrees of phase margin. Therefore, this local feedback loop should remain stable.

For the purpose of verifing the HSPICE simulation to a first order, the loop transmission was found using small signal nodal anlaysis, and the magnitude and phase are plotted in Figures 3.13 and 3.14, respectively. Unlike the HSPICE simulation, this analysis does not consider any circuitry outside the local loop, nor does it consider the body effect that occurs since the source of M4 is not connected to its NWELL. Also, every capacitance that affects the circuit, such as drain to bulk capactiance, is not included in the analysis. Therefore, the exact location of the occurances of poles and zeros does not match between the simulation plots and the calculated plots, but the analysis does confirm the simulation results to a first order. It is important to verify that the zero does occur in the LHP, and the hand analysis does indeed confirm this.

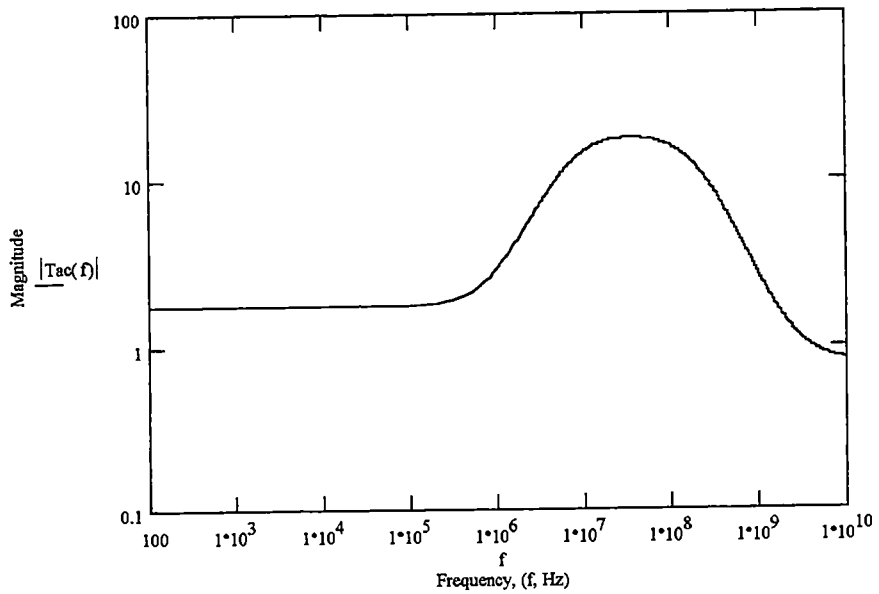


Figure 3.13: First order calculation of the innermost loop transmission magnitude

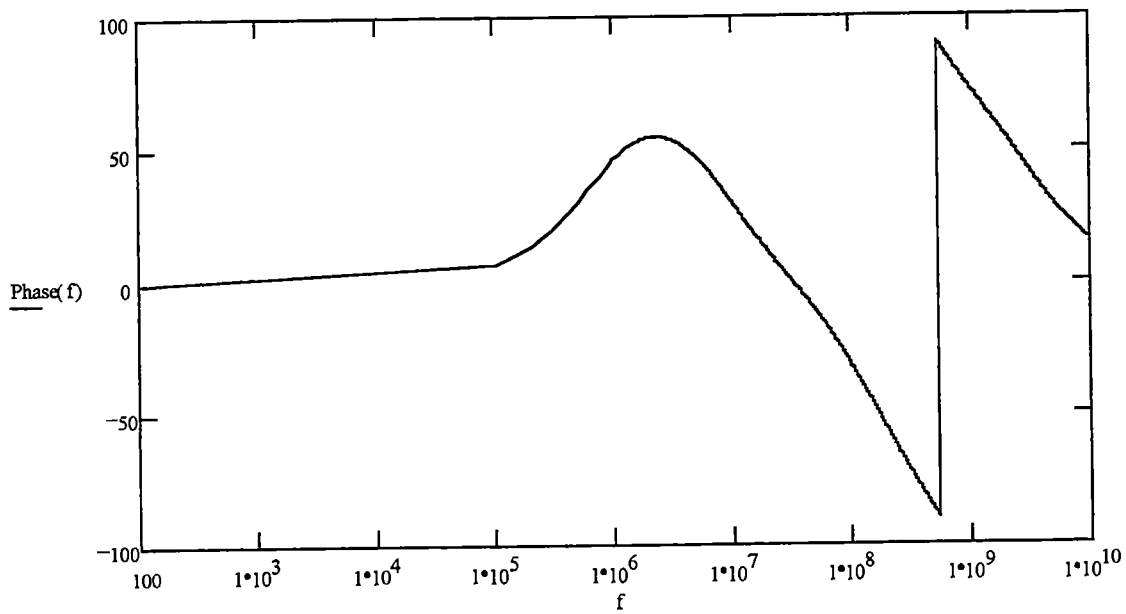


Figure 3.14: First order calculation of the innermost loop transmission phase

The loop transmission for the outer local feedback loop was examined with the innermost feedback loop intact. The loop was broken at the gate of M2, where the test signal was applied, and the return signal was measured at the drain of M4. The simulation results are presented in Figures 3.15 and 3.16. This feedback loop exhibits a frequency response that resembles that of the innermost loop, as expected from the symmetry of the circuit. The low-frequency magnitude is –24.5, which is in agreement with the value obtained in the DC analysis of the previous section. The loop transmission magnitude drops below unity at approximately 80 MHz, where the maximum phase shift that has occurred is -120 degrees, leaving a phase margin of 60 degrees. The outer loop should also remain stable.

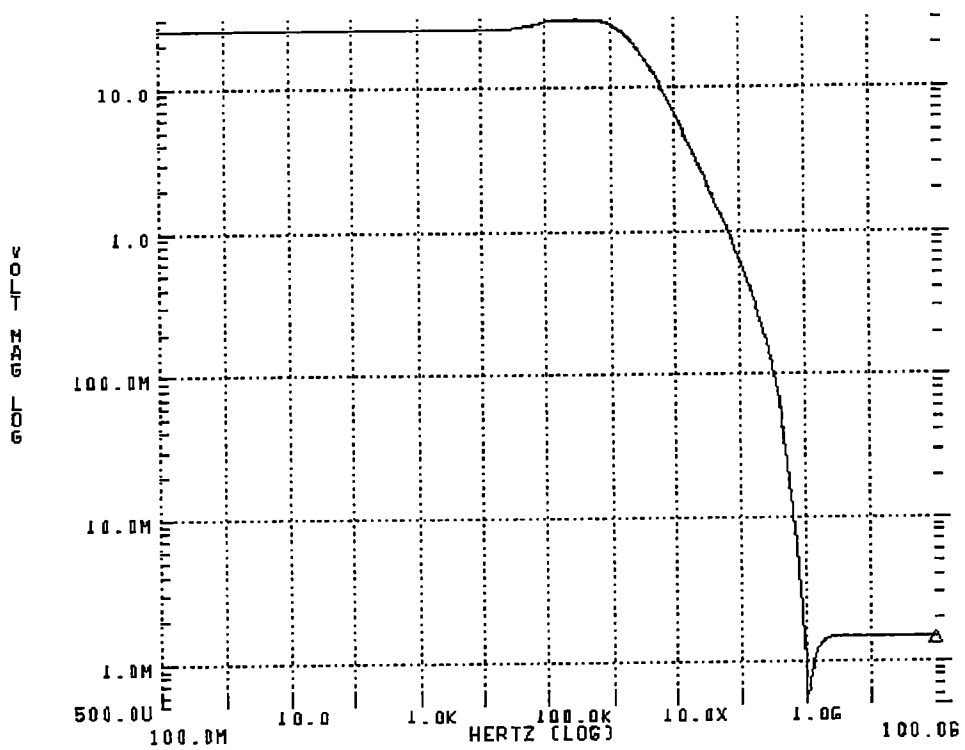


Figure 3.15: Outer local loop transimission magnitude

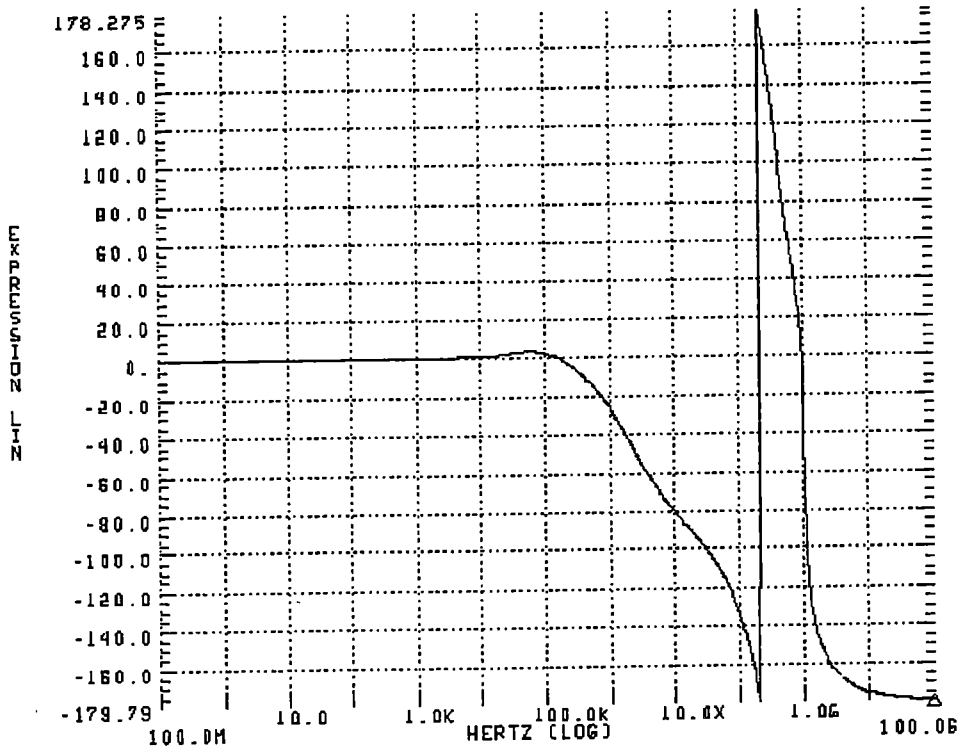


Figure 3.16: Outer local loop transmission phase shift

3.4.2.3 *Current Mirror Design*

A source degenerated current mirror was chosen to supply bias currents for the circuit. The degeneration was implemented using small W/L ratio NMOS transistors biased in the triode region. This bias circuit was chosen in a effort to increase the dynamic range, and to reduce the noise contribution of the current mirror. The bias voltage is supplied by a secondary circuit, Figure 3.17, which is composed of transistors that are identical to devices M10 – M35. An off chip reference current of 100 μA is fed into the I_{ref} input. The reference current splits into two 50 μA currents, each current biasing one side of the secondary circuit. In response to the reference current, the secondary circuit develops an input voltage at the connected gates of the transistors.

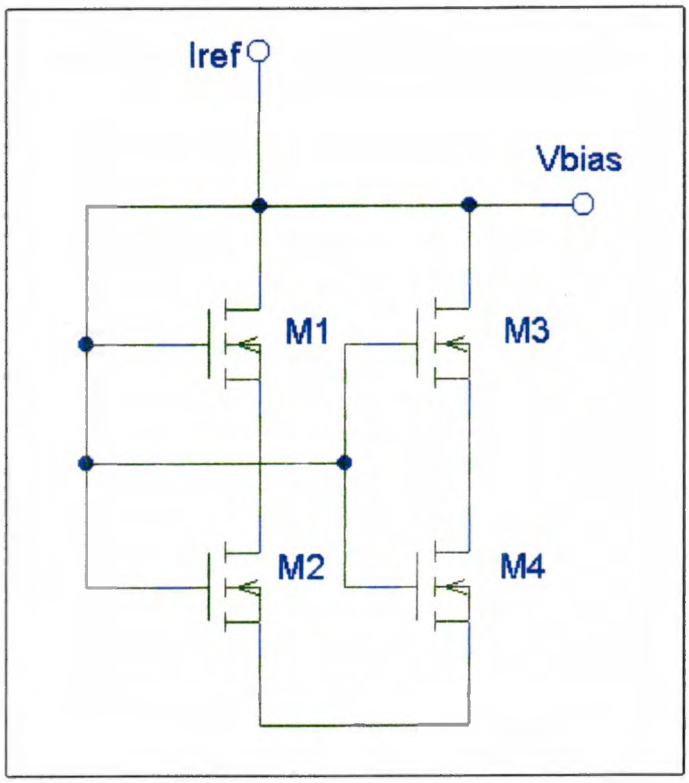


Figure 3.17: Bias voltage generating circuit

When connected to the preamplifier current mirror biasing node, the magnitude of V_{bias} forces the preamplifier current mirrors to sink 50 μA each, when I_{ref} is 100 μA.

The compliance of the current mirror is determined by performing a DC sweep over the output voltage. It is desired to have the current mirror operate with the drain voltage of the output device as low as 1.5 V. The voltage compliance for a set of eight mirrors was plotted versus the drain voltage of the output devices, Figure 3.18. The total current should be 400 μA. The current does not begin to drop significantly until the drain voltage reaches approximately 1.4 volts. At that voltage the top devices are beginning to drop out of saturation. As the drain voltage is increased, the current increases slightly because the voltage at the drains of the bottom devices increases slightly.

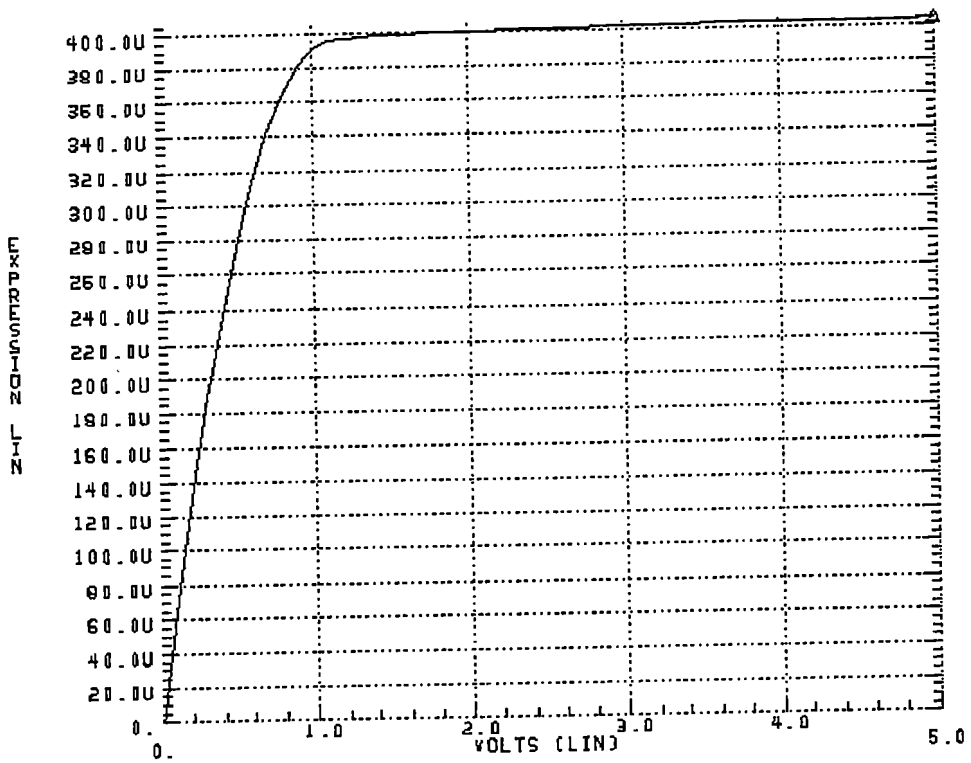


Figure 3.18: Current mirror compliance

3.4.2.4 *Preamplifier Closed Loop Response*

In the previous sections the design and analysis of the core voltage amplifier was examined. The closed loop response of the CSA will be examined in this section by first analyzing the stability of the main feedback loop, and then by analyzing the transient response. The preamplifier feedback capacitance was chosen to be 100 fF to provide a large charge gain, which ensures that the noise sources at the input of the CSA will be dominant. A 400 MΩ resistor was placed in parallel to the feedback capacitor to act as a reset element.

The main feedback loop was broken at the gate of M9, and the AC decoupling circuit was placed internal to the voltage amplifier. The test signal was injected at the

gate of M9, and the return signal magnitude and phase was measured at the drain of M2. Initally the loop was found to be marginally stable, with only a few degrees of phase margin. The circuit was compensated by placing a 500 fF capacitor at the drain of M2, the dominant node. The loop transmission magnitude and phase after compensation are illustrated in Figures 3.19 and 3.20, respectively. The feedback network contributes a pole and zero in the loop transmission, and they are given by Equaiton 3.63,

$$\frac{\left(1+j\cdot\frac{f}{2\pi C_f R_f}\right)}{\left(1+j\cdot\frac{f}{2\pi R_f(C_f+C_{in}+C_{det})}\right)}, \tag{3.63}$$

where C_f is the feedback capacitance, $R_f = 400$ MΩ is the feedback resistance, $C_{in} \cong 3$ pF is the input capacitance, and $C_{det} = 4$ pF is the detector capacitance. The pole that occurs at 80 kHz is the dominant node pole at the drain of M2, and several non-dominant poles are located at frequencies greater than 100 MHz. The peaking behavior in the magnitude could be the result of the peaking in the local feedback loops of the voltage amplifier, or a result of passive signal gain through the transistor capacitors since it occurs at several hundred mega-Hertz. However, it should not present a problem for the preamplifier operation. The unity gain crossover frequency is at approximately 20 MHz, where the phase has shifted by approximately -95 degrees. Thus, leaving a phase margin of 85 degrees, which is a conservative phase margin for circuit stability.

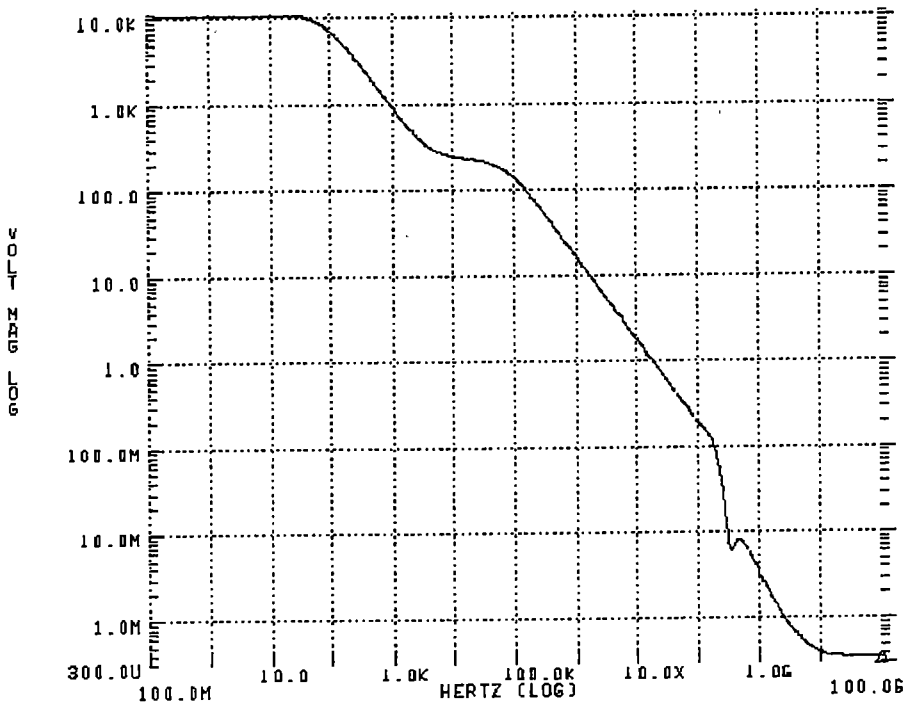


Figure 3.19: Loop transmission of the CSA

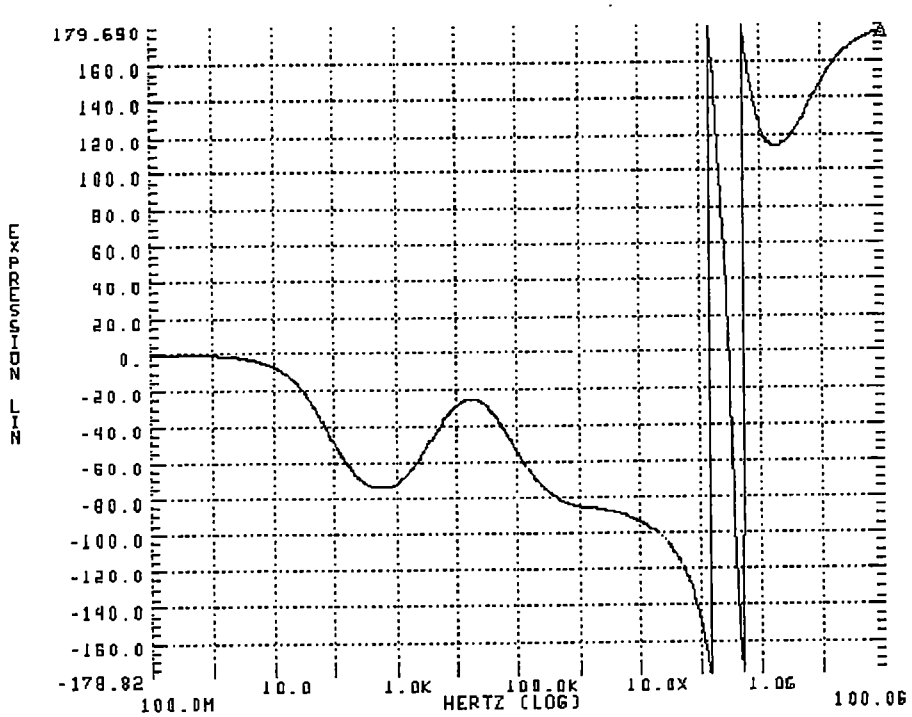


Figure 3.20: Loop transmission phase for the CSA

It was desired to have a preamplifier with a 10 to 90 percent rise time less than 50 ns. The rise time was examined by applying a step voltage to the input of the preamplifier through a 100 fF capacitor. The output pulse was plotted for a 50 mV input step voltage with a 1 ns rise time, and is displayed in Figure 3.21. The 10 to 90 percent rise time was found to be approximately 20 ns, which more than satisfies the design requirement. There is no overshoot or "ringing" in the transient response, which indicative of a stable circuit with a large phase margin. Adding parallel capacitance to the input node will reduce the rise time, therefore it will be important to reduce the parasitic capacitance when coupling the detector to the preamplifier.

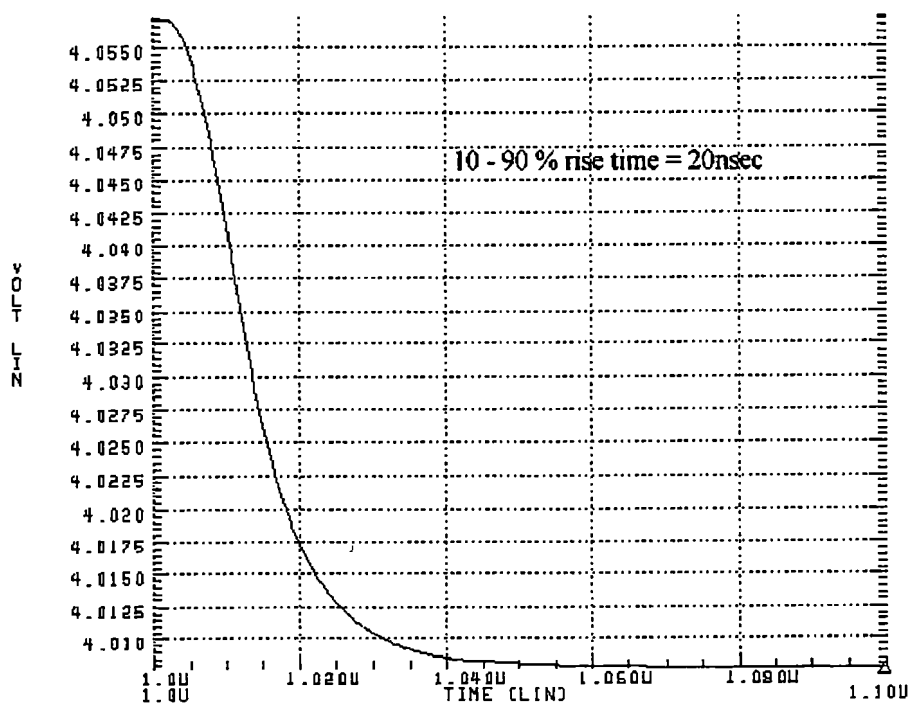


Figure 3.21: Transient response of CSA to a step input

3.4.2.5 *Preamplifer Noise Performance*

To perform the noise optimization in Section 3, it was assumed that the ENV^2 of the preamplifier was dominated by the input device, M1. This section will concentrate on a noise analysis of the MicroCAT preamplifier to determine if this assumption was a valid one. HSPICE simulations using the BSIM3 models were used to perform the noise analysis of the preamplifier, and hand calculations were used to verify the simulation results for the major noise contributers in the circuit.

A plot of the ENV ($^{V}/_{sqrt(Hz)}$) obtained from an HSPICE simulation is given in Figure 3.22. HSPICE was also used to obtain a listing of each transistor's noise contribution for frequencies ranging from 0.1 Hz to 100 GHz. The list values were used to identify the major noise contributers, and hand calculations were made for those transistors in order to validate the simulation data.

The major noise contributing transistors are the input device (M1), the current mirror transistors (M10 – M29), and the four transistors of the biasing circuit used to

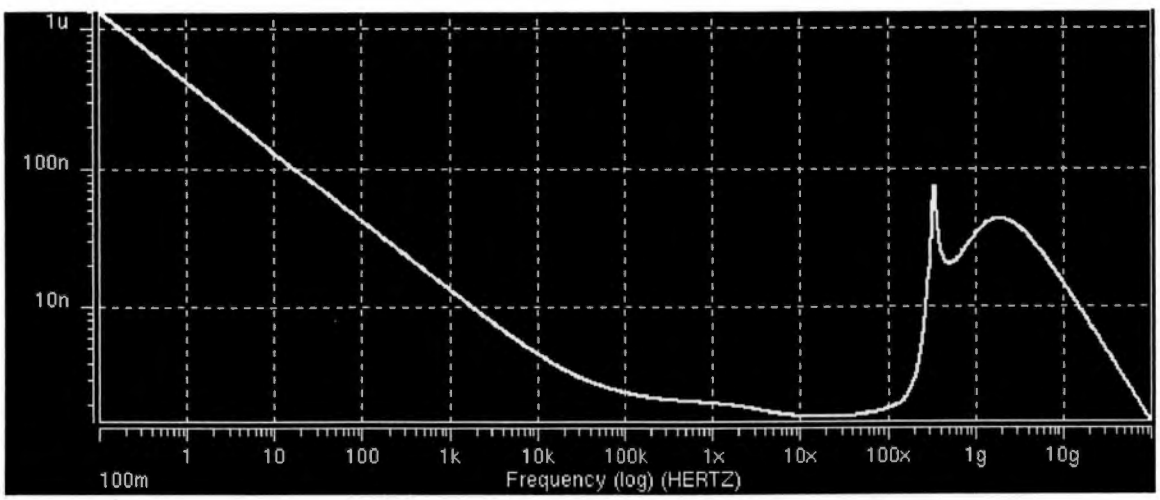


Figure 3.22: Preamplifier's ENV ($^{V}/_{sqrt(Hz)}$) from HSPICE simulation

generate V_{bias}. The noise currents ($A^2/_{Hz}$) that flow through transistor M2 degrade the signal to noise ratio, therefore, all noise sources were referred to a current flowing through M2, then divided by the squared transconductance of M1 to obtain the equivalent noise voltage spectrum ($v^2/_{Hz}$) at the input. The HSPICE simulations were performed using the parameters given in Table 3.5. The HSPICE parameter NLEV is used to choose the noise calculation equations. Choosing NLEV = 3 specifies that Equation 3.64 be used to calculate the flicker noise contribution, and Equation 3.65 be used to calculate the channel thermal noise contribution.

$$ENI^2_{flicker}\left(\frac{A^2}{Hz}\right) = \frac{KF \cdot g_m^2}{C_{ox} W L f^{AF}} \qquad \textbf{(3.64)}$$

KF and AF are empirical parameters that are dependent on the fabrication process. As noted previously, KF for PMOS transistors has been found to be as much as a factor of forty times less than that for NMOS devices [Binkley, 32].

Table 3.5: Noise model parameters

NLEV	3
KF (NMOS)	5.0×10^{-24} V^2F
KF (PMOS)	2.0×10^{-25} V^2F
AF	1
Model	BSIM3 (level = 49)

The channel thermal noise is given by [38],

$$ENI_{thermal}^2\left(\frac{A^2}{Hz}\right)=\left(\frac{2}{3}4kT\beta\left(V_{gs}-V_{th}\right)\left(\frac{1+\alpha+\alpha^2}{1+\alpha}\right)\right), \qquad \textbf{(3.65)}$$

where the parameter V_{gs} is the gate to source voltage, V_{th} is the device threshold voltage, and α is given by Equation 3.66,

$$\alpha=\begin{cases}1-\dfrac{V_{ds}}{V_{dsat}} & ;triode\\ 0 & ;saturation\end{cases}, \qquad \textbf{(3.66)}$$

where V_{ds} is the drain to source voltage, and V_{dsat} is the drain to source saturation voltage. When NLEV ≤ 2 is chosen, HSPICE does not distinguish between devices operating in saturation and devices operating in the triode region. Consequently, for the purpose of calculating channel thermal noise, all devices are treated as though they were operating in saturation. Since the source degenerating transistors of the current mirror operate in the triode region, only NLEV = 3 gives accurate noise calculations. Equation 3.65 was also used to calculate the channel thermal noise contributions of each device by hand.

The input transistor, M1, has the flicker noise component given by Equation 3.64 that appears directly in series with the gate. One portion of the channel thermal noise of M1 flows through the drain to source resistance of M1, thus not contributing to the degradation of the signal to noise ratio (SNR). The voltage spectrum that appears at the gate of M1 due to its channel thermal noise is given by Equation 3.67,

$$ENV^2_{thermal}\left(\frac{V^2}{Hz}\right)=\frac{\left[\frac{2}{3}4kT\beta\left(V_{gs}-V_{th}\right)\right]_1\cdot\left(\frac{r_{ds1}}{r_{ds1}+R_{in2}^{CL}}\right)^2}{g_{m1}^2}, \qquad \textbf{(3.67)}$$

where $R_{in2}{}^{CL}$ is the closed loop input impedance seen looking into the source of M2, and was found to be 134 Ω in Section 3.4.2.1. The channel thermal noise, calculated to be 2.17×10^{-18} $v^2/_{Hz}$, has a "white" spectrum, and is therefore independent of frequency. The calculated total equivalent noise voltage ($^{V}/_{rt(Hz)}$) due to the input device is plotted in Figure 3.23 as a line, and the HSPICE simulation values are superimposed onto the plot as circles at each decade interval.

The next largest contributor to the input ENV is the circuit used to generate V_{bias}. These devices are connected as diodes, and the noise voltage that appears at the V_{bias}

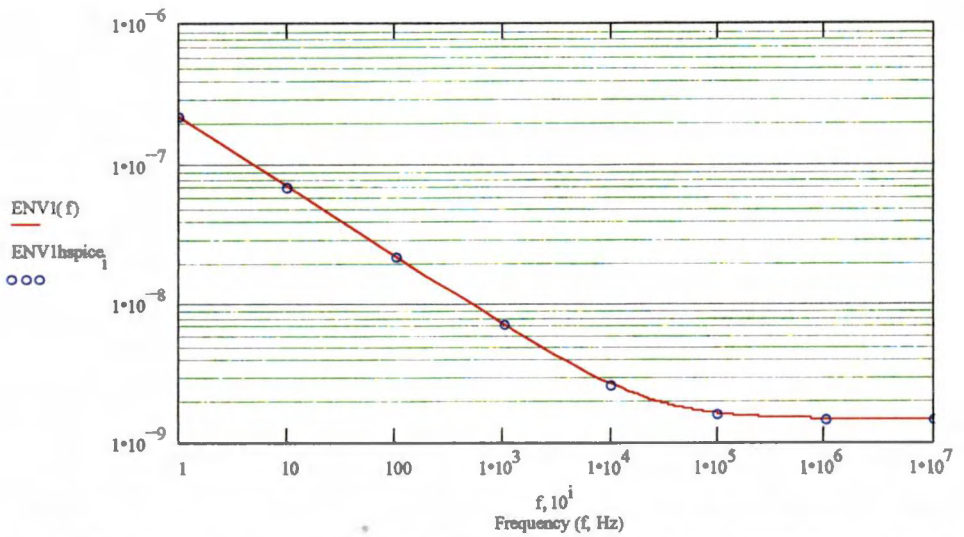


Figure 3.23: Equivalent noise voltage at the input due to M1 (line is hand calculations, circles are HSPICE results)

node due to these four transistors modulates each gate to source voltage in the current mirror. The noise of all four transistors was modeled as a noise current from the drain to the source, and a transfer function was derived using the DC small signal hybrid-π models to give the noise voltage from V_{bias} to ground for each device. These derivations are presented in Appendix B, and only the results are presented and used here. The bias circuit with all noise current sources is illustrated in Figure 3.24. The noise voltage spectrum that appears at node V_{bias}, with respect to ground, as a result of the noise current spectrum of device M2 of the bias circuit is given by Equation 3.68,

$$ENV^2_{@Vbias(due\text{-}to\text{-}M2)} = \frac{ENI^2_{M2}}{\left[2\left(\left(1+g_{m2}r_{ds2}\right)\left(g_{m1}+g_{ds1}\right)+\left(g_{mb1}g_{m2}r_{ds2}\right)\right)\right]^2}, \tag{3.68}$$

where g_{mb} is the backgate transconductance. The noise voltage spectrum that appears at node Vbias due to the noise current spectrum of M1 of the bias circuit is given by Equation 3.69,

$$ENV^2_{@Vbias(due\text{-}to\text{-}M1)} = \frac{ENI^2_{M1}}{\left[2\left(g_{g2}+g_{ds2}\left[\frac{1}{\frac{g_{mb1}}{g_{m1}+g_{ds1}}+1}\right]\right)\right]^2}. \tag{3.69}$$

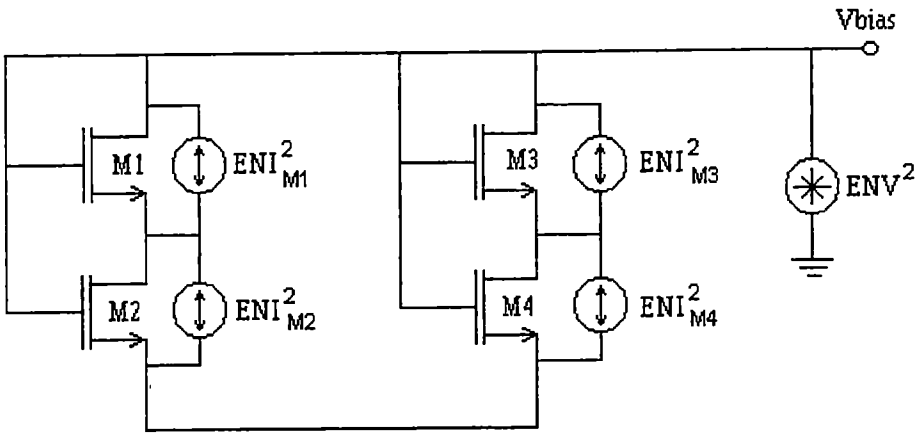


Figure 3.24: Preamplifier biasing circuit with noise sources

The transfer function from the gates of the current mirrors, node V_{bias}, to the gate of the preamplifier's input transistor, M1, was also found using nodal analysis of the DC small signal hybrid-π models. The result is given by Equation 3.70 for transistor M4 of the bias circuit.

$$ENV^2_{@M1gate} = \frac{\left(\sqrt{ENV^2_{@Vbias(due-to-M4)} \cdot TF^2} \cdot N\right)^2}{g^2_{m1}} \cdot \left(\frac{r_{ds1}}{r_{ds1} + R^{CL}_{in}}\right)^2 \qquad \textbf{(3.70)}$$

Where N = 10 is the number of current mirrors that contribute significantly to the noise current flowing through M2, and TF is the transfer function given in Equation 3.71, which relates a voltage at the V_{bias} node to an output current of a single current mirror. As an aid in understanding the transfer function of Equation 3.71, the parameters of the

transfer function are given in Figure 3.25, an illustration of the source degenerated current mirror circuit.

$$TF = \frac{I_{o1}}{V_{bias}} = \frac{\left[-g_{m11}\left(g_{m10}r_{ds10}+1\right) - \frac{r_{ds10}g_{m10}}{r_{ds11}} \right]}{\left[-R_{in2}^{CL}g_{m10} - g_{m10}r_{ds10} - \frac{R_{in2}^{CL}}{r_{ds10}} - \frac{R_{in2}^{CL}}{r_{ds11}} - 1 - \frac{r_{ds10}}{r_{ds11}} + \frac{g_{m10}}{R_{in2}^{CL}} + \frac{1}{R_{in2}^{CL}r_{ds10}} \right]} \qquad \textbf{(3.71)}$$

Note that the output currents of the mirrors due to the bias circuit are 100 percent correlated since the noise generators of the preamplifier bias circuit are common to all gates of the current mirror, and therefore the square roots of the current noise spectrums must be summed. The summation is then squared to obtain the total output noise current, as given by Equation 3.70. The transfer function calculation assumes a low impedance load, as provided by the closed loop input impedance at the source of M2 (134 Ω) of the preamplifier.

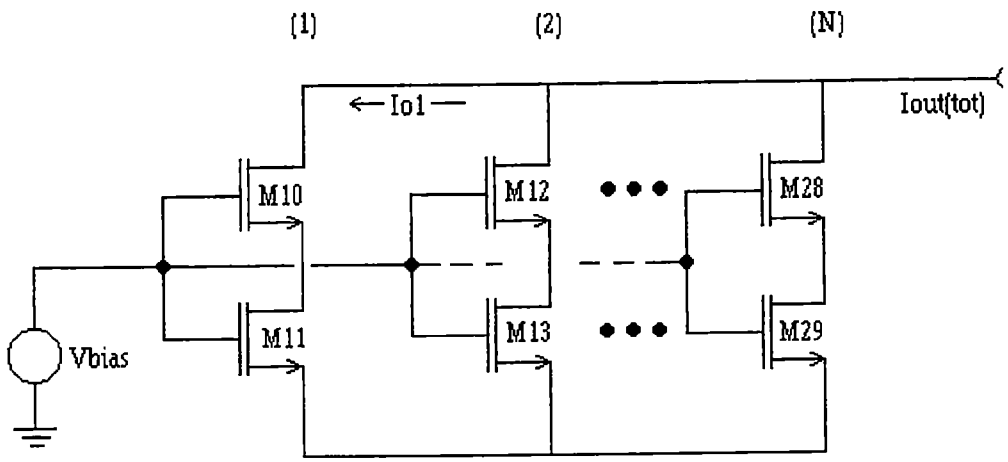


Figure 3.25: Source degenerated current mirror transfer function

The noise voltage spectral density that appears at the gate of the preamplifier input device, M1, was calculated for all four of transistors of the bias circuit, and the result is plotted in Figure 3.26. The HSPICE result is superimposed onto the plot at intervals of one decade. The hand calculation plot (red line) matches the simulation results (blue circles) quiet well at low frequencies. However, since the transfer functions for the hand calculations were derived with the DC hybrid-π models, the roll-off at high frequencies is not predicted by the hand calculations. The V_{bias} node was made available externally to the prototype chip for the purpose of biasing the circuit, therefore a large capacitance will be placed there to reduce this noise source as much as possible.

The third and final major noise contributor is the current mirror itself. Each mirror contributes a noise current that flows through M2, and thus degrades the SNR. A transfer function for each transistor of the mirror (i.e. for M10 and M11) was derived.

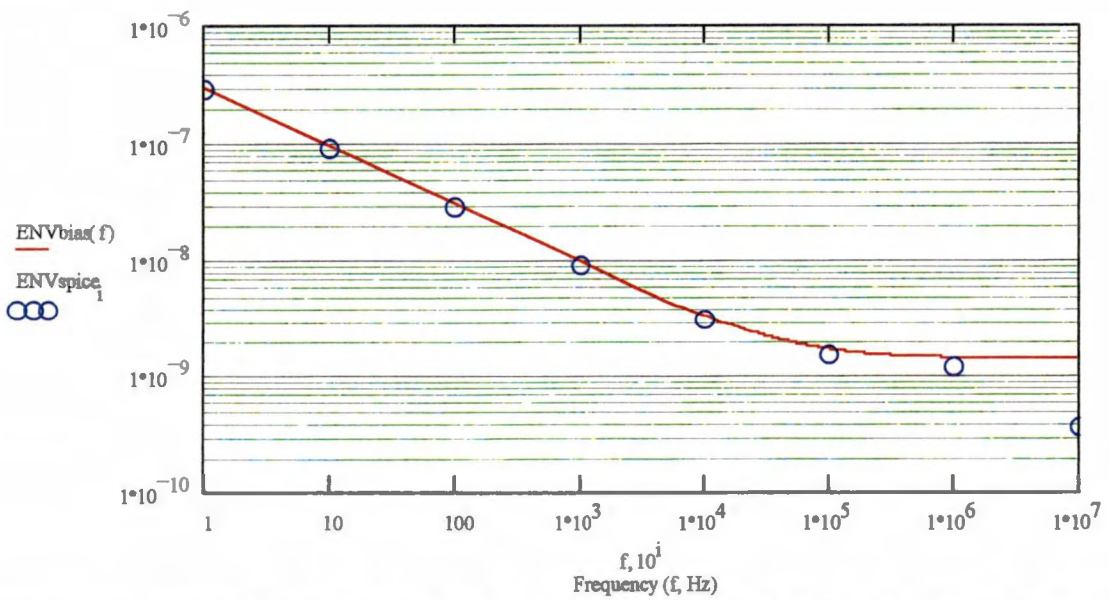


Figure 3.26: Equivalent noise voltage at the input due to the bias circuit (line is hand calculations, circles are HSPICE results)

Unlike the previous analysis, where the current noise flowing in each mirror was due to a common noise voltage at their gates, the current noise due to the mirror transistors themselves is completely uncorrelated. Thus, the current spectral density of each mirror is referred back to the gate of the preamplifier's input device, M1, and the noise voltage spectral densities are summed there to obtain a total due to the current mirror. The noise current spectral density for transistor M10 of the current mirror is given by Equation 3.72,

$$ENV^2_{@M1gate(due\text{-}to\text{-}M10)} = \frac{ENI^2_{M10}\left(\frac{G^2_{m10}}{g^2_{m10}}\right)\cdot\left(\frac{r_{ds1}}{r_{ds1}+R^{CL}_{in2}}\right)^2}{g^2_{m1}}, \qquad \textbf{(3.72)}$$

where G_{m10} is the degenerated transconductance of M10. The current noise spectrum of M11 generates a voltage noise spectrum at the gate of M1 given by Equation 3.73,

$$ENV^2_{@M1gate(due\text{-}to\text{-}M11)} = \frac{ENI^2_{M11}\left(\frac{r_{ds1}}{r_{ds1}+R^{CL}_{in2}}\right)^2\left(\frac{r_{ds11}}{r_{ds11}+\left(\frac{1}{g_{m10}+g_{mb10}}\right)}\right)^2}{g^2_{m1}}, \qquad \textbf{(3.73)}$$

where g_{mb10} is the backgate transconductance of M10. The noise voltage spectral densities due to the current mirror transistors were summed at the gate of M1 to obtain the total noise voltage spectrum due to the current mirror transistors, which is plotted in

Figure 3.27 along with the HSPICE simulation results. The hand calculations (red line) agree very well with the simulation results (blue circles) over the frequency range.

The noise voltage at the gate of M1 due to the major noise contributors considered here was obtained by summing the spectral density of each at the gate of M1 and taking the square root of the sum. This is plotted in Figure 3.28 along with the HSPICE simulation results for the noise voltage at the gate of M1 due to all noise contributors. The excellent match between the simulation results for all noise contributors and the total noise voltage calculated by hand for only the major noise contributors confirms that the major noise contributors have indeed been identified. Furthermore, the flicker noise corner given by the noise calculations indicates that the input device dimensions could be modified to give a better thermal noise performance, and thus improve the equivalent noise charge at the output. Since the thermal noise does indeed dominate the ENC seen

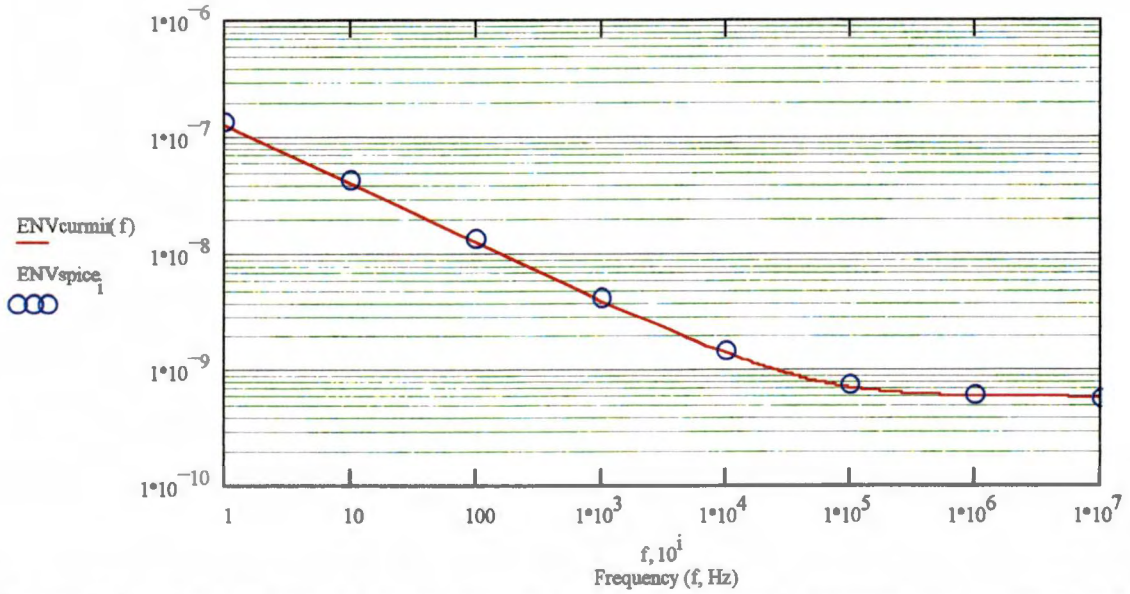


Figure 3.27: Equivalent noise voltage at the input due to the current mirrors (line is hand calculations, circles are HSPICE results)

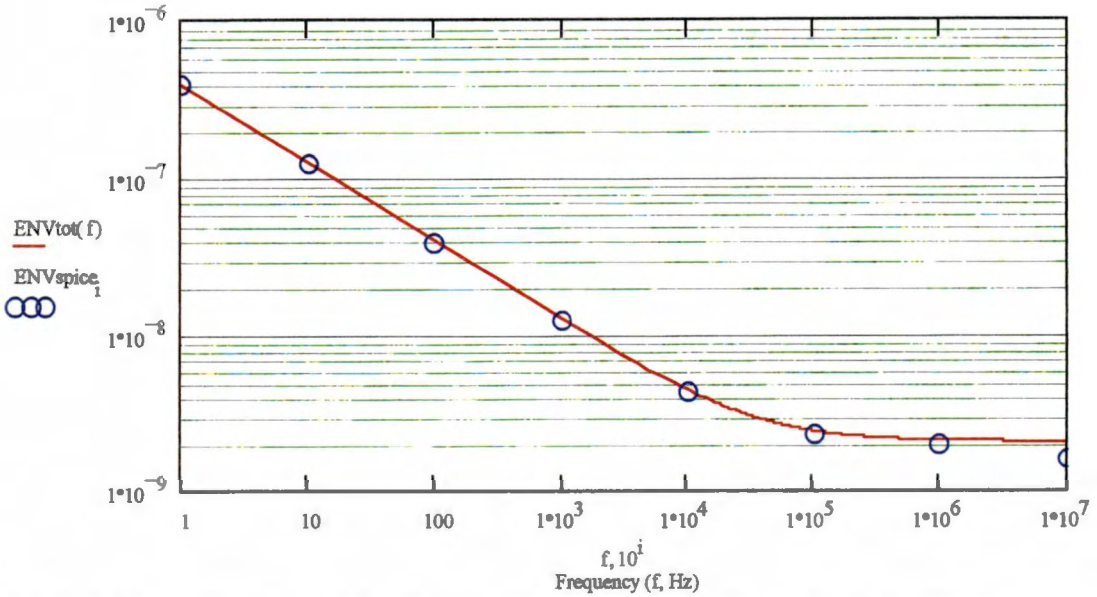


Figure 3.28: Equivalent noise voltage at the input due to the major contributors, and the HSPICE simulation result for all noise contributors (line is hand calculations, circles are HSPICE results)

at the output of the pulse shaper, the assumption that M1 dominates the noise performance was valid, because M1 does dominate in the thermal noise region if the bias circuit is low-pass filtered. The preamplifier biasing circuit contributes a large amount in that region as well, but the V_{bias} node can be filtered externally, thus reducing the noise contribution of the biasing circuit.

3.5 Design Summary

In this chapter the design of the core voltage amplifier has been evaluated beginning with the concept of the basic cascode circuit, and making performance improvements by adding two internal negative feedback loops. The charge-sensitive

amplifier has 10 % to 90 % rise time of 20 ns, a phase margin of 85 degrees, and at 100 kHz the input noise voltage is only 2 $\frac{nV}{\sqrt{Hz}}$.

Chapter 4 Layout and Post-layout Simulation

The preamplifier was fabricated in the AMI 1.2 μm n-well process through the MOSIS program [40], and laid out for fabrication using the layout tool Magic [39]. The prototype preamplifiers were fabricated on dice of size 2200 μm by 2200 μm. Several layout standards were defined prior to the layout process to ensure layout compatibility to other MicroCAT system blocks being designed by other team members. The final MicroCAT system chips will each have 16 channels of electronics; therefore a dense layout of each cell was required.

- The height of the cells must be 120 μm.
- The width of the cells must be kept as low as possible.
- The main power supply traces must be 32 μm tall, and extend over the entire length of the cell so that when the cells are adjoined, the traces butt together.

4.1 Preamplifier Layout

The layout of the preamplifier, illustrated in Figure 4.1, has a height of 120 μm and a length of 660 μm. When the bias circuit is adjoined to the preamplifier (at the left-hand side), the input device, M1, is positioned such that it and the current mirror share a vertical line of symmetry. This was done to improve the thermal matching of the input device. The feedback capacitor, C_f = 100 fF, is to the left of the input device, and the compensation capacitor, C_c = 500 fF, is to the right of the current mirrors. The slots in the power supply traces act as a strain relief, and also help to prevent the protective silicon nitride layer from peeling [41].

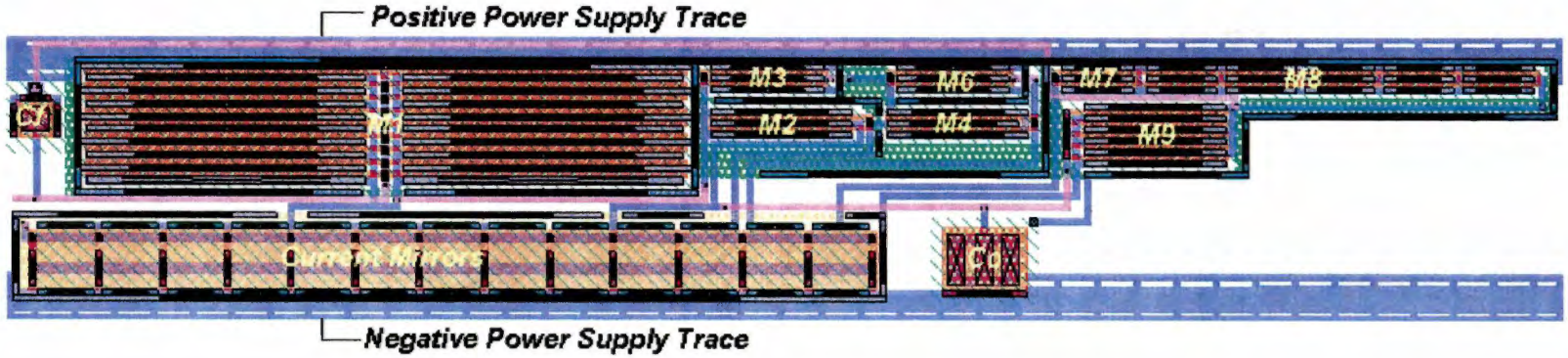


Figure 4.1: Preamplifier Magic layout

4.1.1 Input PMOS Device

The input PMOS device, illustrated in Figure 4.2a, was laid out as a 2 by 9 array for a total of 18 gate fingers, each having a length of 120 μm. The connections for drain diffusion contacts and the polysilicon gates are made symmetrically with metal-1 at the center of the device. The source diffusion contacts are connected on the outside edges by the metal-1 contact on top of the n-diffusion guard ring, which surrounds the transistor completely, and also is the backgate (substrate) connection. The device is directly adjoined to the positive power supply trace at the top, requiring no additional metal-1 traces to connect the source. The gate connection is brought out below the device and to the left with a metal-2 trace, and the drain connection is brought out below the device where the connection splits into two traces: A metal-1 trace that connects the drain to the current mirror, and a metal-2 trace that connects the drain to the source of M2. The input device consumes approximately $^1/_3$ of the area required for the complete preamplifier.

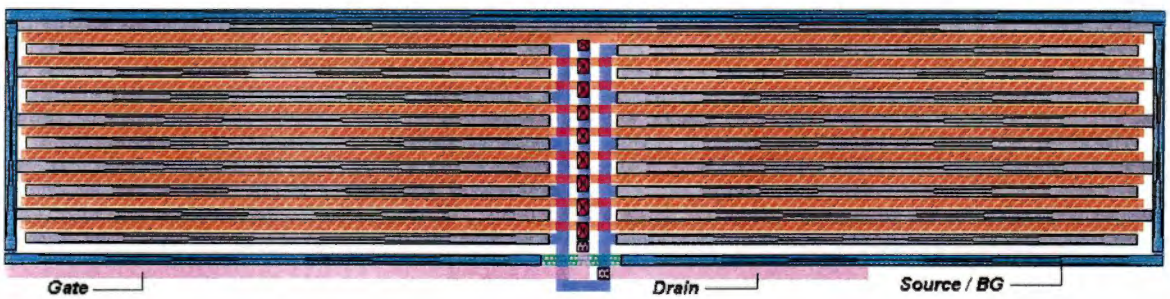
4.1.2 Current Mirrors

The current mirror is a source degenerated NMOS mirror, and current mirror transistors M10 through M35 are shown in Figure 4.2b. Each mirror sinks 50 μA of current, therefore in order to sink 100 μA of current, two mirrors are paralleled. This layout technique improves the matching between the current mirrors, because multiple copies of the same device are paralleled to scale the current, versus scaling the device width to scale the current. No external connection was required at the center node, so the layout is made more compact by leaving the source (for top device) and drain (for bottom

device) contacts out. The sources of the bottom devices are connected together by the negative power supply trace, and the drains of the top devices are made available through gaps in the p-diffusion metal-1 contact. The polysilicon gates are connected at each end with metal-1 traces, so that the gate resistance is kept low. The backgate is connected to the negative supply rail via the p-diffusion ring that surrounds the current mirror.

4.1.3 Transistors M2 through M9, and Capacitors C_c and C_f

Transistors M2 through M9 were laid out as compactly as possible, and the free areas around the devices were heavily plugged to reduce the substrate resistivity. The



(A)

(B)

Figure 4.2: Magic layouts of A) the input PMOS transistor M1, and B) the NMOS current mirror circuit

transistors were interdigitated to reduce the required contact diffusion area, and thus the source to bulk and drain to bulk capacitances. Although current matching between transistors M7 and M8 was not critical to the circuit performance, device M8 was laid out as five copies of transistor M7 to improve the matching.

The feedback capacitor was placed near the input device to reduce the trace length at the input. The feedback and compensation capacitors are polysilicon to polysilicon type capacitors, therefore each have a parasitic capacitance from the back plate to the bulk. Both capacitors were laid out over an n-well that is connected to the positive power supply rail.

4.1.4 Preamplifier Biasing Circuit

The preamplifier's bias circuit layout, Figure 4.3, is such that when the bias circuit is adjoined to the left side of the preamplifier, the input device, M1, and the current mirrors share a vertical line of symmetry. Although, a positive power supply rail was not required for the bias circuit, one was added to the layout of the cell. This was done so that when the cells are adjoined in an array, no top-level interconnection will be required for the power supply traces. The transistors of the bias circuit are exact copies of the current mirror transistors, to minimize current matching errors. The reference current will be sourced from off chip, so the input node will connect directly to a pad. This will also allow a large bypass capacitor to be placed off chip for the purpose of noise reduction.

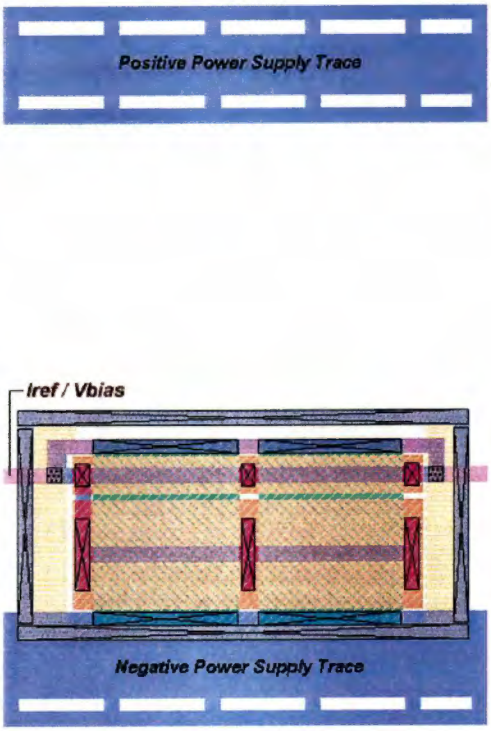


Figure 4.3: Preamplifier biasing circuit

4.2 Prototype Chip Layout

The Magic layout of the prototype chip is shown in Figure 4.4, and a photograph of the prototype chip is shown in Figure 4.5. In addition to the preamplifier design chosen for the MicroCAT system, seven other preamplifiers were included on the prototype chip for experimentation. Each preamplifier was isolated from the others with a p-type diffusion ring connected to the negative power supply. The preamplifier at the top left corner is the MicroCAT preamplifier, however, all preamplifiers on the left side have the same transistor topology. That is, they only differ with respect to the feedback and compensation capacitor size. The preamplifiers on the right hand side of the die have a slightly different topology than the one chosen for the MicroCAT project, in that they only have one local negative feedback loop.

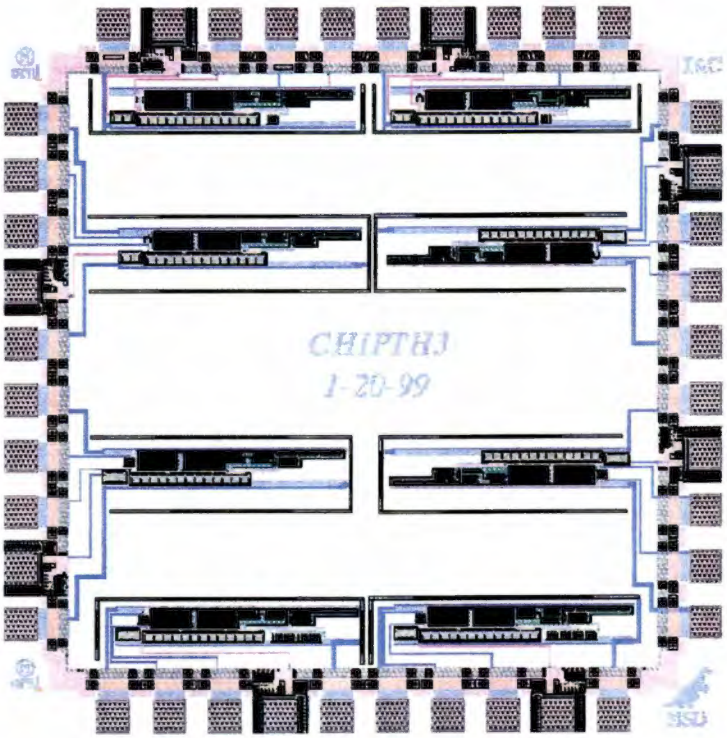


Figure 4.4: Magic layout of the prototype chip

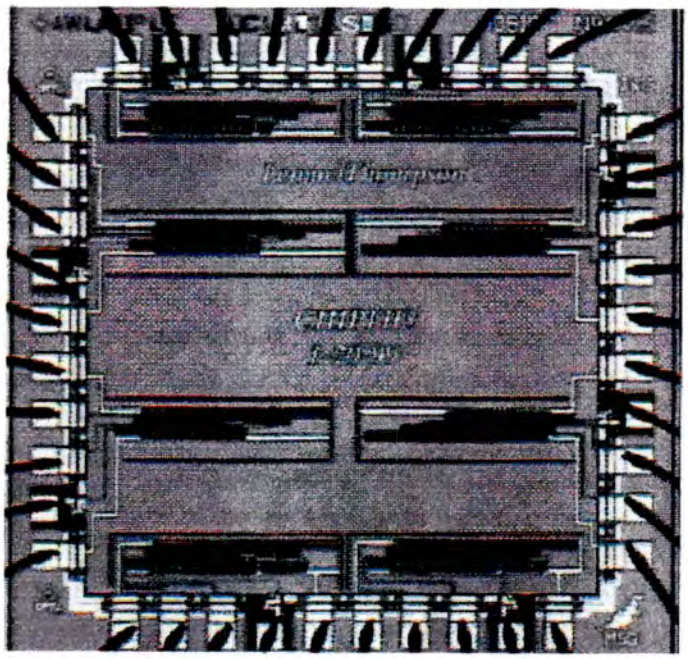


Figure 4.5: Fabricated prototype chip

4.3 *Post-layout Simulations*

After the layout process, it is considered good practice to simulate the circuit once again for two reasons. The main reason being to verify that the circuit has been laid out and interconnected correctly, and the second reason being to determine the effects that stray capacitance has on the circuit. The Magic tool allows a circuit netlist to be extracted from the Magic file that contains all parasitic capacitances with a capacitance value greater than a user defined threshold. The netlist extraction may be done at any stage of the design, so that the designer can verify the layout at any point.

In order to verify that the preamplifier's post-layout performance was satisfactory, the both the transient response and CSA loop transmission magnitude and phase were examined. The post-layout transient response was studied for 0 pF, 4 pF, and 10 pF added input capacitance. These plots are presented in Figures 4.6, 4.7 and 4.8, respectively.

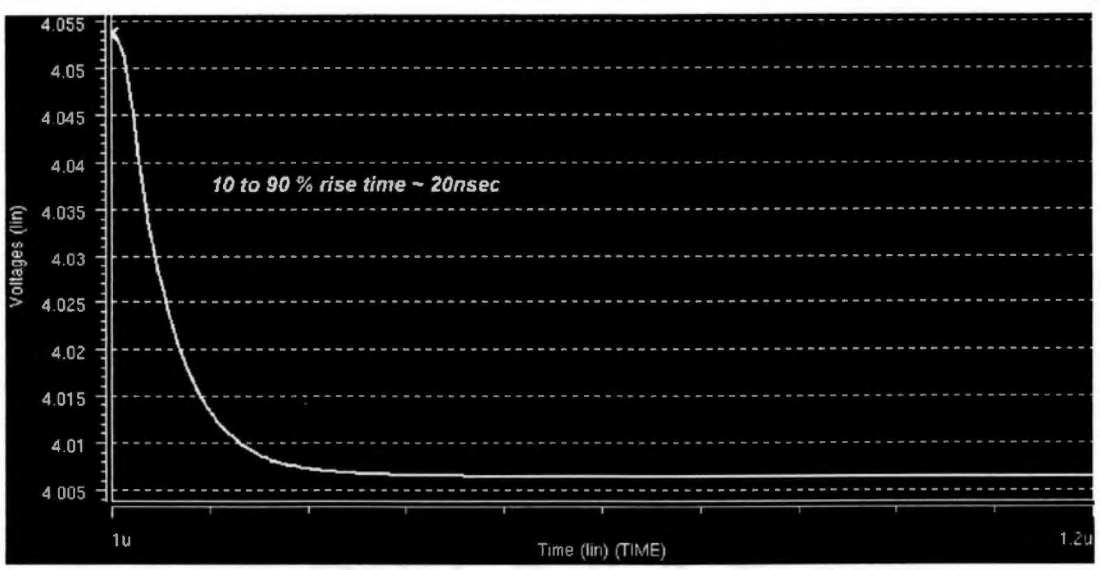


Figure 4.6: Post-layout transient response for 0 pF added input capacitance

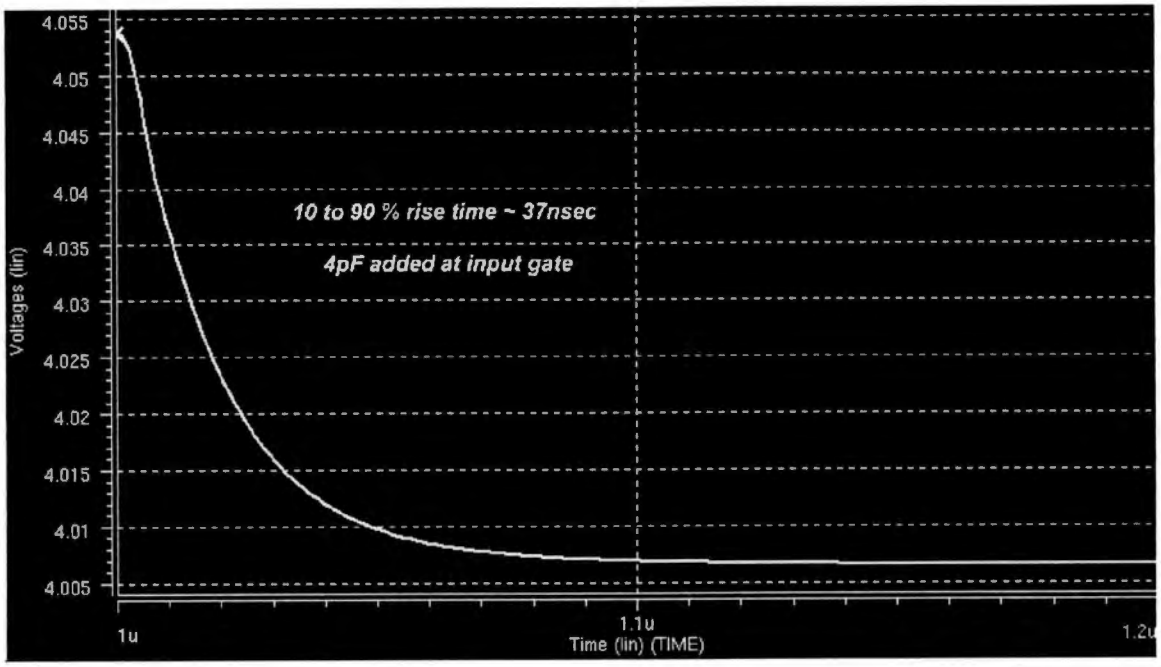


Figure 4.7: Post-layout transient response for 4 pF added input capacitance

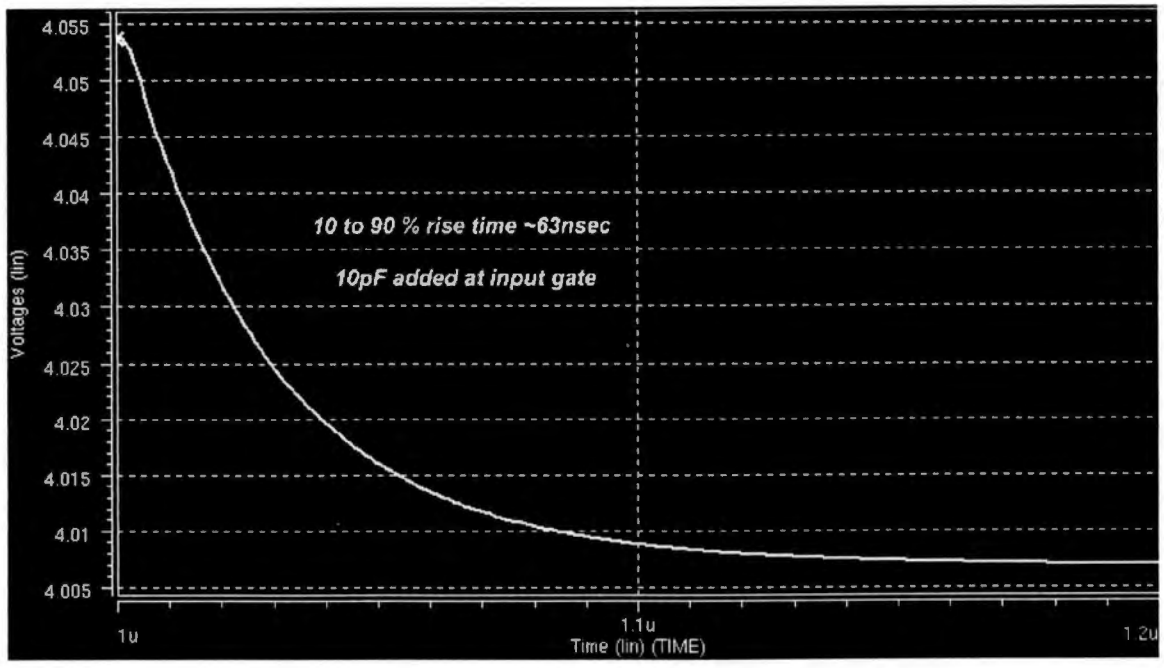


Figure 4.8: Post-layout transient response for 10 pF added input capacitance

The simulation was performed such that the response should be unity gain with respect to a 50 mV input pulse. The peak to peak response measured at the output was approximately 47 mV, which is indicative of a feedback capacitor that does not measure exactly 100 fF, as desired. The approximate 6% error is most likely the result of poor precision in the layout of the feedback capacitor (i.e. the feedback capacitor could not be laid out to be exactly 100 fF). However, parasitic capacitance could also contribute to the error. In either case, the small error is acceptable. By comparing the pre-layout and post-layout rise times, it can be seen that the parasitic capacitance added at layout had a negligible effect on the rise time of the output pulse.

The post-layout loop transmission magnitude and phase are presented in Figures 4.9 and 4.10, respectively. The unity gain cross over is at approximately 20 MHz, where

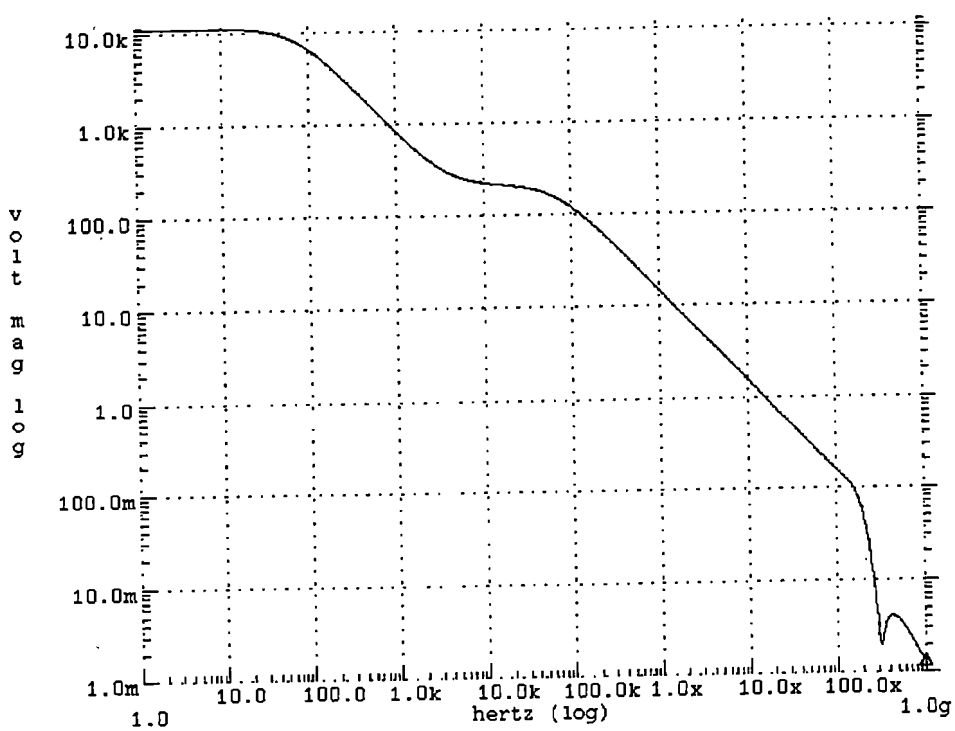


Figure 4.9: Post-layout loop transmission magnitude

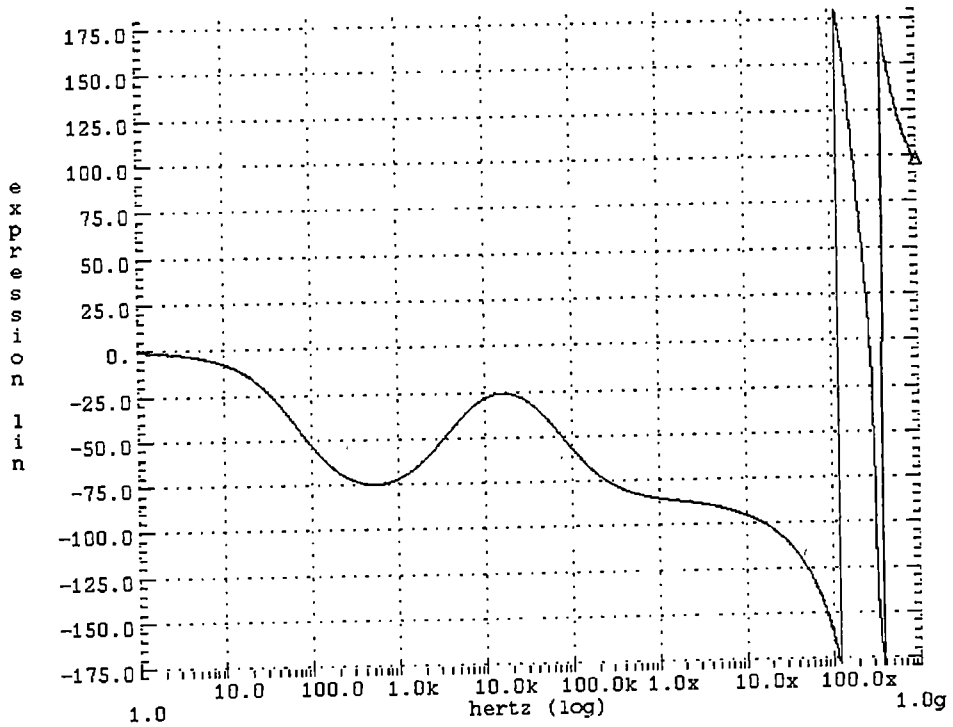


Figure 4.10: Post-layout loop transmission phase

the phase has shifted by –100 degrees, leaving 80 degrees of phase margin. Again, the post-layout response is very near the pre-layout response.

Chapter 5 Experimental Evaluation of the Preamplifier

At the time the prototype chip was being fabricated by MOSIS, a test board was designed and fabricated (Figure 5.1). The schematic diagram of the test board is shown in Figure 5.2. The ASIC chip was to be packaged in a standard 40-pin ceramic casing, and for ease of testing a chip socket was used on the prototype board to accommodate the ASIC. In order to reduce the number of parts used on the prototype board, only one current source was used. However, the current source is adjustable, and can accommodate several preamplifiers if desired. The jumpers on the board make it possible to select which preamplifier(s) are to be powered, and each current source and power supply line are heavily bypassed. The feedback resistors are located in close proximity to

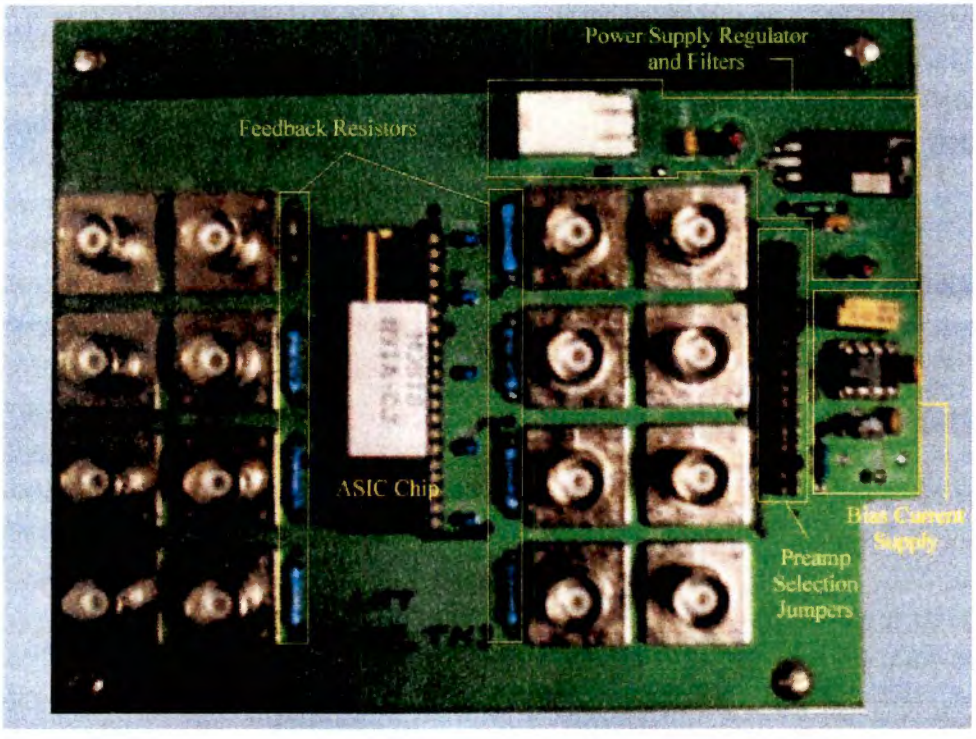


Figure 5.1: Prototype ASIC test board

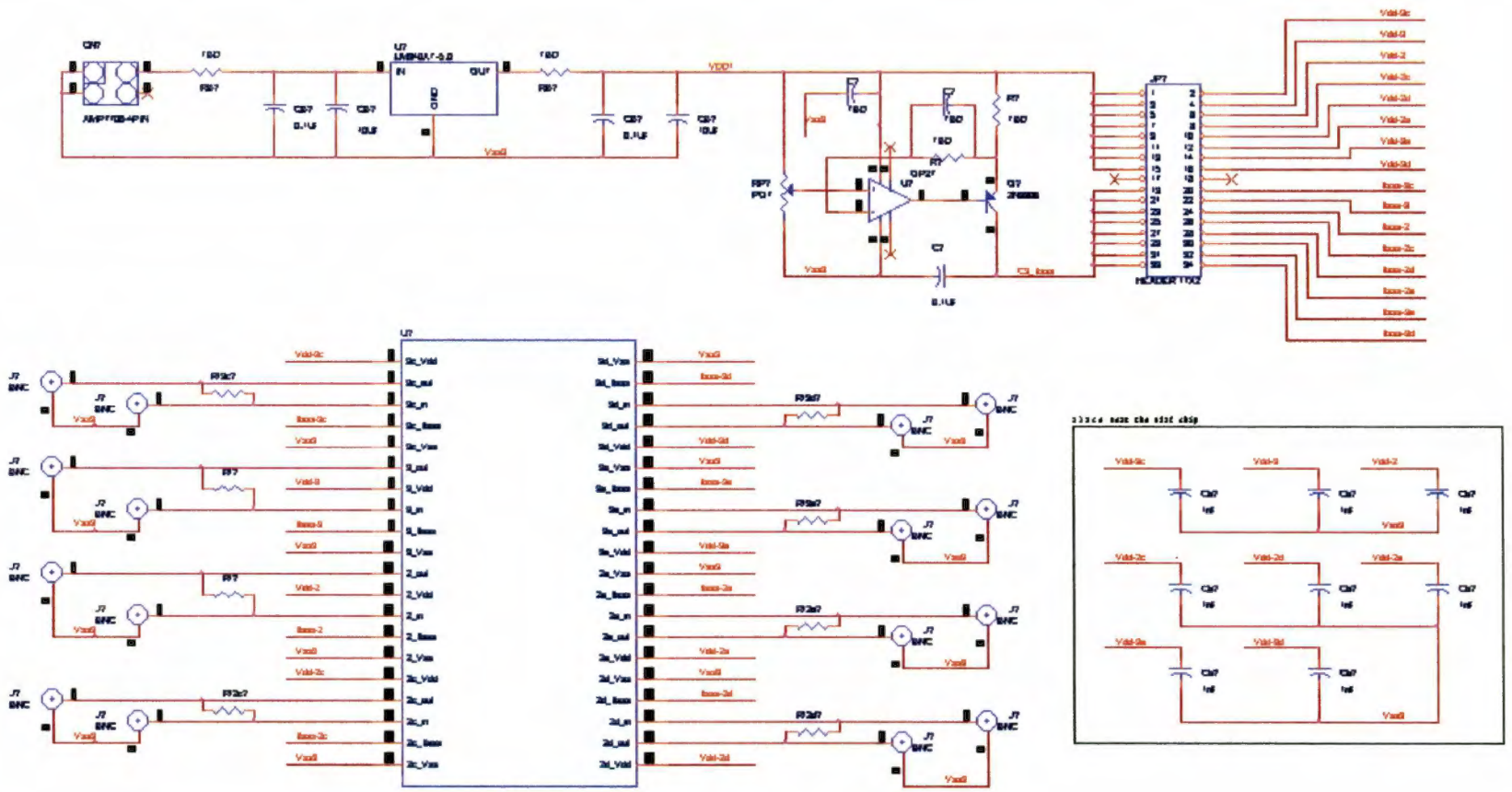


Figure 5.2: Prototype test board schematic for the MicroCAT preamplifier

the ASIC, as are the input and output BNC connectors. The input positive power supply is seven volts, and the negative power supply is ground. The voltage regulator supplies five Volts to the circuit at its output.

The preamplifier was subjected to many tests to verify its performance. The test board and ASIC were placed in an aluminum box for shielding during the testing process; however, this was found to produce varying results and a new test board was constructed and placed into a small metal box. In the following sections the results of the tests for charge gain and rise time, dynamic range, slew rate, noise performance, and the performance with a CZT detector are discussed.

5.1 *Charge Gain, Rise Time, and Decay Time*

The charge gain was measured by using a step function pulse generator and a 1 pF capacitor connected in series to the input of the preamplifier (Figure 5.3). The pulse height of the voltage step was measured using an oscilloscope to be 38 mV, and the capacitor value was measured to be 0.99 pF. The injected charge is easily calculated to be 37.62 fC using Equation 5.1,

$$Q(Coulombs) = C_t(Farads) \cdot v(Volts), \tag{5.1}$$

where C_t is the charge determining capacitor, and v is the amplitude of the input voltage step. By dividing the injected charge by the charge of one electron ($q = 1.602 \times 10^{-19}$ C), the number of input electrons was determined to be 234,832. The oscilloscope traces for both the input signal and the corresponding output signal are given in Figure 5.4. The

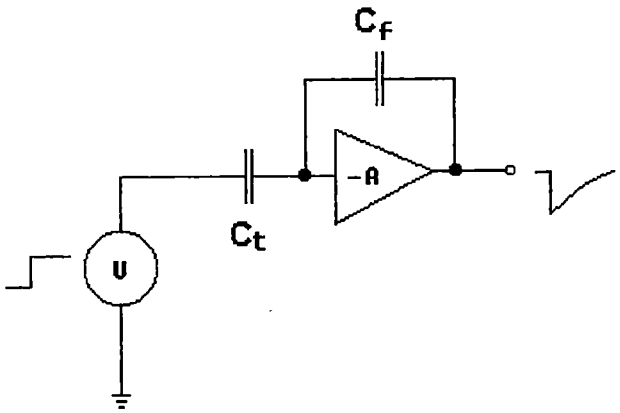


Figure 5.3: Charge gain test circuit

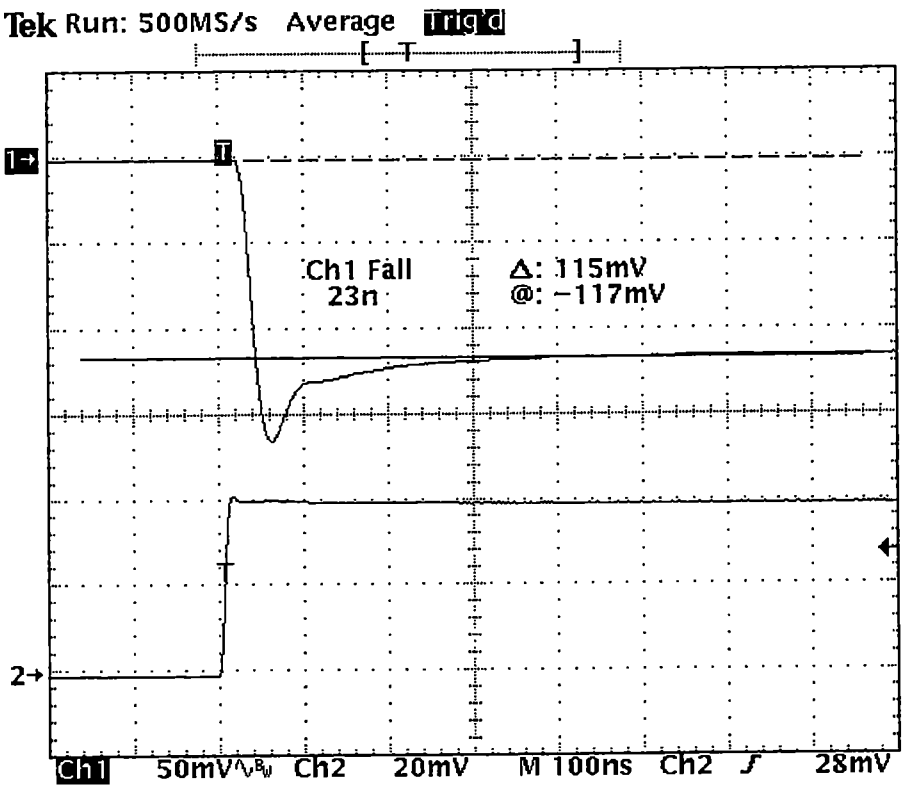


Figure 5.4: Input (channel 1) and output (channel 2) signals

amplitude of the output pulse was measured to be 115 mV at steady state, and prior to pulse decay. The charge gain is given by Equation 5.2,

$$A_c\left(\frac{V}{C}\right)=\frac{v_{out}}{Q_{in}}, \tag{5.2}$$

and was calculated to be 3.06 x 10^{12} Volts per Coulomb or 490 nV per electron. This charge gain calculation reveals that the feedback capacitance must be greater than the 100 fF for which the circuit was designed. The approximate value of the actual feedback capacitance was calculated to be 330 fF, a factor of 3.3 greater than the expected value. The additional feedback capacitance is a result of (1) having an external feedback resistor, which can have an end to end capacitance on the order of 1 pF, (2) small parasitic capacitances, and (3) capacitance parameters that vary slightly from the extraction parameters used by Magic. The additional capacitance not only reduces the charge gain, but also threatens the stability of the CSA, which may be seen in the output waveform of Figure 5.4 as an undesired overshoot in the transient response. This issue will be further discussed in the last section of this chapter.

The output rise time was measured to be 23 ns (Figure 5.4), and is slightly greater than the anticipated value of 20 ns. The rise time is under the influence of two effects, the first being the larger than expected feedback capacitance, which tends to reduce the rise time, while parasitic capacitance at the input tends to increase the rise time. The parasitic input capacitance was measured for the test board to be approximately 9 pF from the input to ground. The rise time was also measured to be 26 ns and 39 ns for

additional external capacitances of 6.6 pF and a 17 pF placed at the input, respectively. Note that the external capacitance is in addition to the 9 pF parasitic capacitance already at the input.

The output 10 to 90 percent decay time is given by,

$$T_{decay} = 2.2 R_f C_f , \tag{5.3}$$

where R_f and C_f are the feedback resistance and capacitance, respectively. The feedback capacitance value was also estimated by measuring the decay time (Figure 5.5), and directly calculating C_f using an R_f of 400 MΩ. The feedback capacitance was calculated to be approximately 323 fF, which is in good agreement with the value calculated using the charge gain.

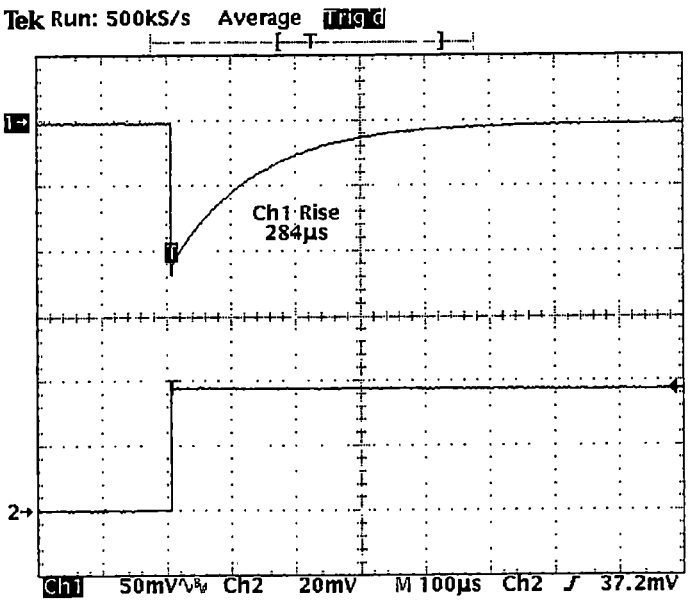


Figure 5.5: Input (channel 1) and output (channel 2) signals at 100 µs per division

5.2 *Dynamic Range*

The dynamic range of the preamplifier was tested using the same circuit as presented in Figure 5.3, but with an increased value of the input voltage amplitude. The dynamic range measurement was made for both positive and negative going input pulses, since this CSA will be used for both polarities. The negative going output pulse can approach a voltage that is the sum of the gate-to-source voltage of M9 and the drop out voltage of the current mirror. This sum is approximately two volts, and the measured value of the negative going dynamic range (Figure 5.6) is -2.09 V.

The positive going output pulse can approach the drain to source saturation voltage of M8, which is less than 300 mV. Therefore, the positive going dynamic range should approach the upper voltage rail minus ~300 mV. The plot of this measurement is given in Figure 5.7, and the dynamic range was measured to be +912 mV.

Using the charge gain calculated in Section 5.1, the maximum input that can be accommodated by the preamplifier, without overdrive, is $+2.942 \times 10^6$ or -6.452×10^6 electrons. This is well in excess of the maximum expected input of $\pm 11.11 \times 10^3$ electrons, which is given by the quotient of the maximum *x-ray* energy and the conversion efficiency of CZT. However, the difference between the positive and negative dynamic range is a concern. Ideally, the dynamic range would be symmetric around the DC bias point, so that an equal positive and negative charge could be accommodated. This is more important when a reset switch is used versus a resistor. The MicroCAT system will employ a reset switch in the final version, which has been designed and will be tested at a later date.

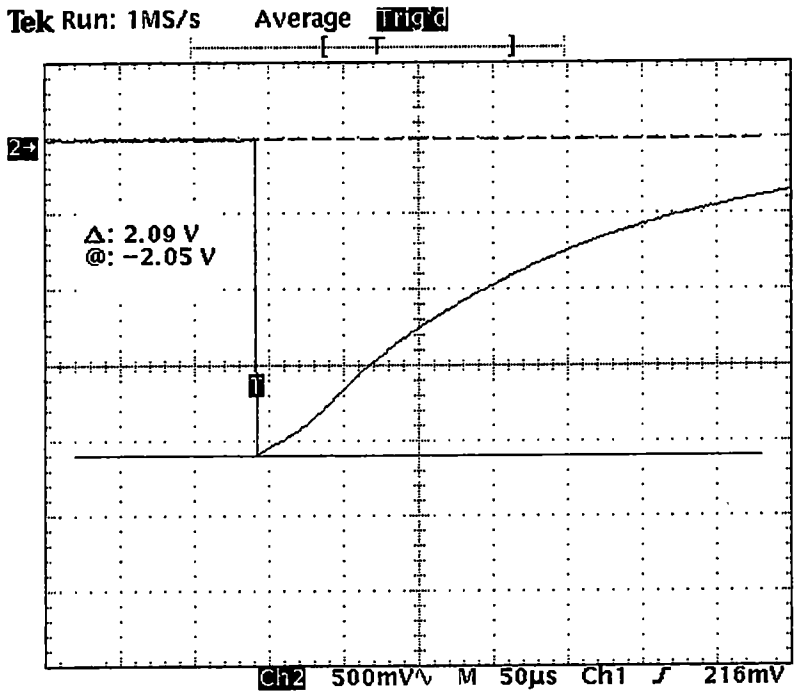


Figure 5.6: Negative going dynamic range

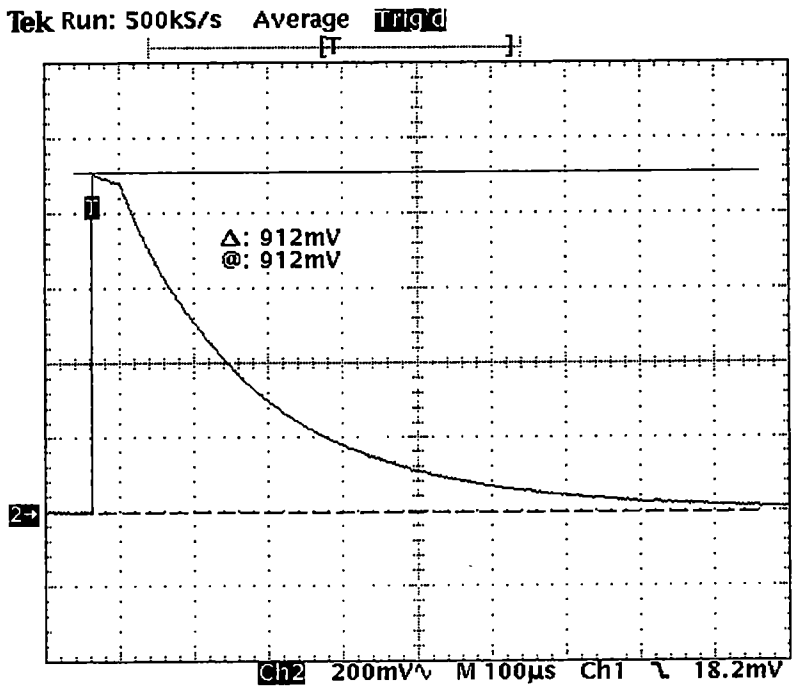


Figure 5.7: Positive going dynamic range

5.3 Slew Rate

The preamplifer slew rate for a positive going output pulse is determined by the current flowing in the drain of M8, $I_d = 250\ \mu A$, and the load capacitance, C_L. The load capacitance for the MicroCAT system is given by the shaper input capacitance to be 10 pF. However, for the purpose of the stand-alone testing of the preamplifier, the load capacitance is given by the sum of the paracitic test board capacitance, measured to be 7 pF, and the oscilloscope probe capacitance, 15 pF, which gives a total load capacitance of $C_L = 22$ pF. The positive slew rate is given by,

$$SR_{positive}\left(\frac{Volts}{\mu s}\right) = \frac{I_{d(M8)}}{C_L}, \tag{5.4}$$

and was calculated to be 11.4 ($^{Volts}/_{\mu s}$). The measured positive slew rate is presented in Figure 5.8, and is in good agreement with the calculated value.

The negative slew rate is not limited by the output buffer stage of the preamplifier, but is determined by the dominant node capacitance, C_d, and the drain current of M2, $I_d = 100\ \mu A$. Since the compensation capacitance, $C_c = 500$ fF, is small, the stray capacitances at the dominant node will decrease the negative slew rate. The dominate node capacitance is approximately 700 fF, and the negative slew rate is given by Equation 5.5,

$$SR_{negative}\left(\frac{Volts}{\mu s}\right) = \frac{I_{d(M2)}}{C_d}, \tag{5.5}$$

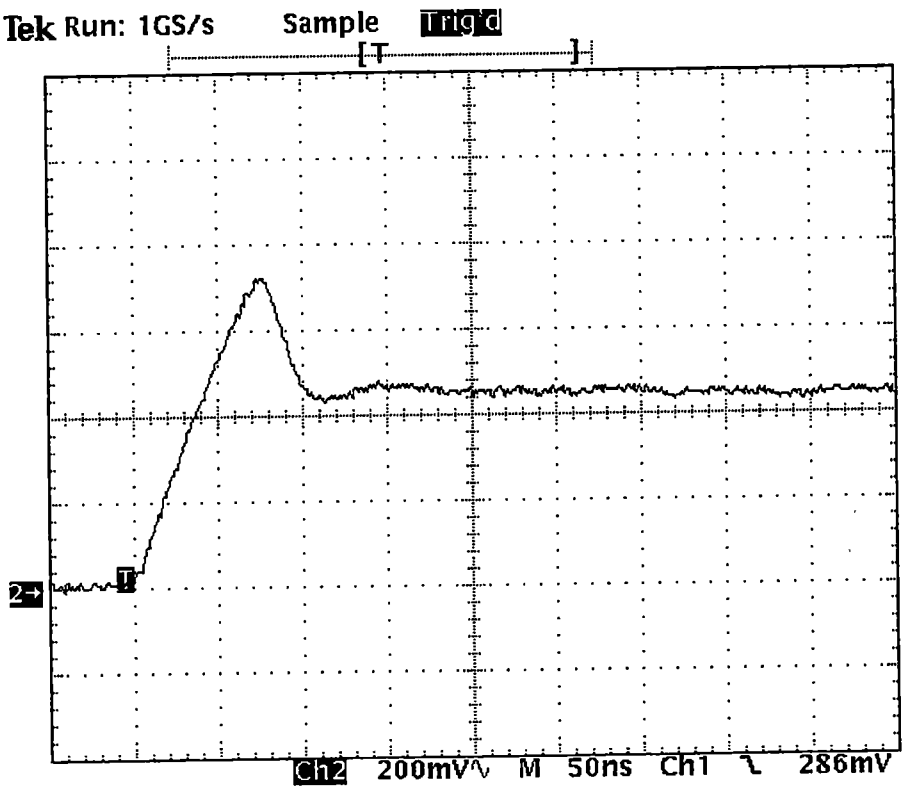


Figure 5.8: Slew rate limited large signal response

and was calculated to be 143 ($^{Volts}/_{\mu s}$). A positive, large signal input produced the measured response illustrated in Figure 5.9, and is not slew rate limited, but limited by the frequency response of the preamplifier.

5.4 Noise Performance

The noise performance of the preamplifier was verified by two methods. These tests are described in this section, and the results are related to the theoretical and simulated noise performance. The ENC of the preamplifier was determined in the first test, and in the second test the output noise voltage was measured directly.

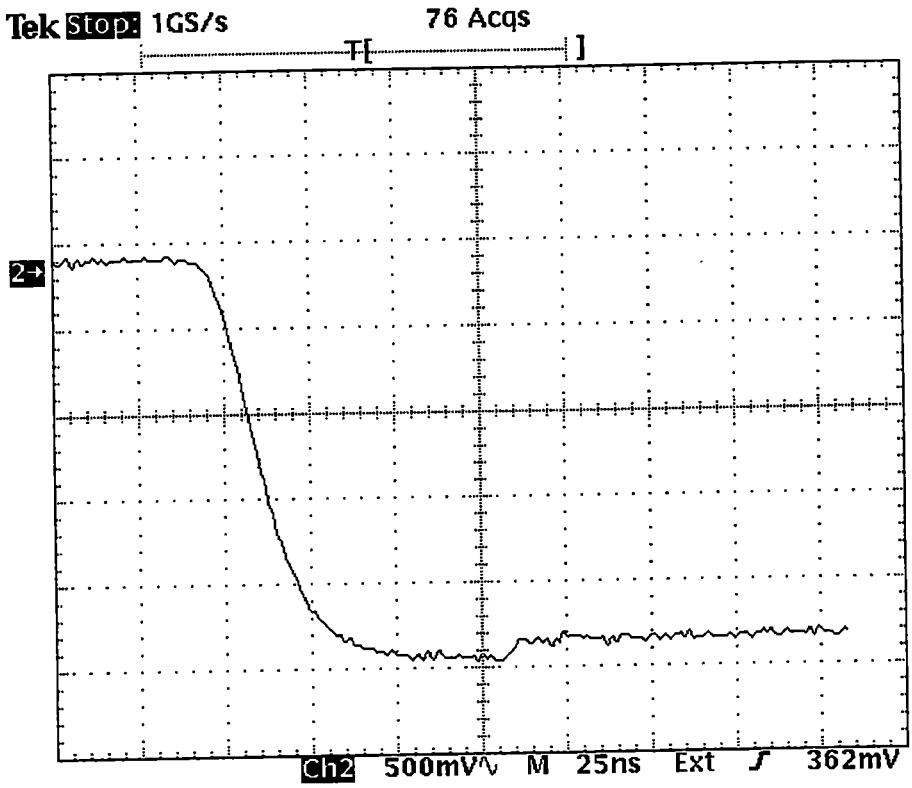


Figure 5.9: Frequency response limited, large signal response

5.4.1 ENC as a Function of Shaping Time

A block diagram of this test configuration is presented in Figure 5.10 A pulse generator was used to drive a variable attenuator that in turn drove the test circuit, and the charge input determining capacitor was measured to be 0.99 pF. The preamplifier was AC coupled to an Ortec 571 shaping amplifier with a 1 μF capacitor to accommadate the non-zero output bias voltage of the preamplifier. The Ortec 571 shaper has six shaping time settings that range from a minimum of 0.5 μs to 10 μs for both unipolar and bipolar output pulses (Table 5.1). The attenuated input voltage pulse was held constant throughout the experiment. The gain settings of the Ortec 571 were set to provide an output pulse amplitude of approximately 2 Volts, and were not changed throughout the

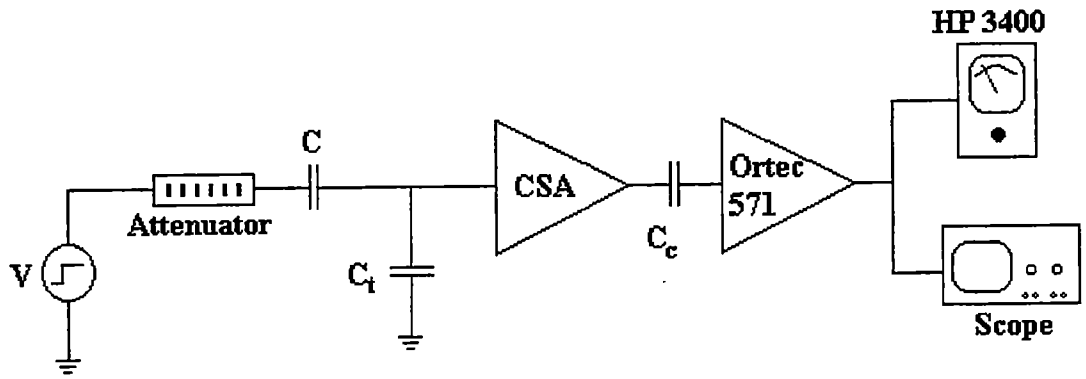


Figure 5.10: ENC measurement configuration

Table 5.1: Measured pulse shaping time versus front pannel time constant (Ortec 571)

Front Pannel (τ)	Shaping Time (Unipolar)	Shaping Time (Bipolar)
0.5 μs	1.05 μs	1.4 μs
1 μs	2.1 μs	2.6 μs
2 μs	4 μs	5.2 μs
3 μs	6 μs	7.4 μs
6 μs	14.4 μs	15 μs
10 μs	19 μs	25 μs

experiment. For each selection of time constant, the rms voltage was measured at the shaper output for both unipolar and bipolar pulse shapes using the Hewlett Packard 3400A rms voltmeter. The HP 3400A's calibration was verified by comparing the measured rms voltages of sinusoidal signals of several amplitudes to the calculated rms values. The calibration was found to have an accuracy less than 3%, and approximately half of the error can be attributed to signal generator noise, and error in measuring the signal amplitude. Although the gain of the pulse shaper (Ortec 571) is fairly constant over the range of shaping times, the output pulse amplitude was measured at each shaping time to reduce the experimental error. An example bipolar output pulse for τ = 0.5 μs is illustrated in Figure 5.11. The experiment was repeated for test capacitances of 6.6 pF, and 17 pF. Note that as previously mentioned, the input was loaded with 9 pF of parasitic capacitance from the test board; therefore, when this is considered the experiment was truly carried out for test capacitances of 9 pF, 15.6 pF, and 28 pF. The zero test capacitance data was extrapolated from the other tests. The final MicroCAT chip will be mounted in close proximity to the CZT detector, and connected using very short traces. Therefore, the input capacitance will be on the order of 1 pF, as considered in the theoretical noise analysis presented in Chapter 3. In order to verify the noise measurement technique, the pulse height spectra were measured for the 6.6 pF external capacitance and the FWHM resolution was calculated using Equation 3.8.

The output noise is a linear function of the external capacitance, therefore the approximate ENC for 4 pF external capacitance (detector capacitance is 4 pF) was extrapolated from the data of the measured ENC. The measured data and the extrpolated 4 pF data for unipolar shaping and bipolar shaping are presented in Figures 5.12, and 5.13

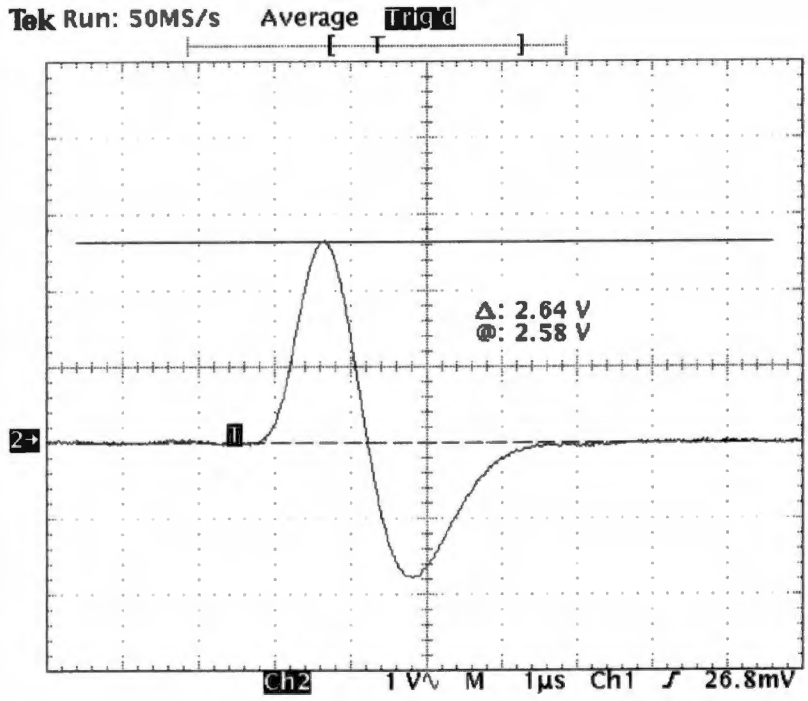


Figure 5.11: Bipolar output pulse for shaping time constant of 0.5 µs

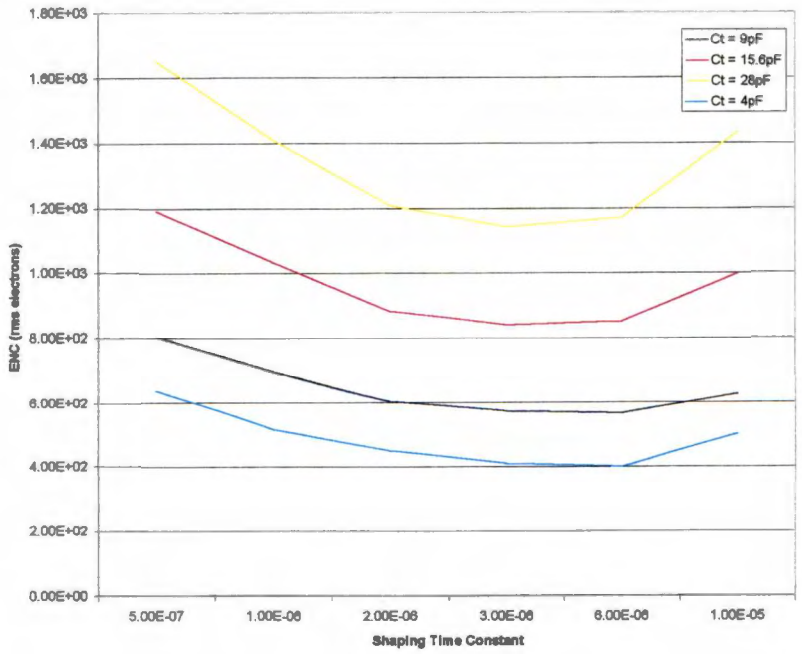


Figure 5.12: Measured unipolar ENC

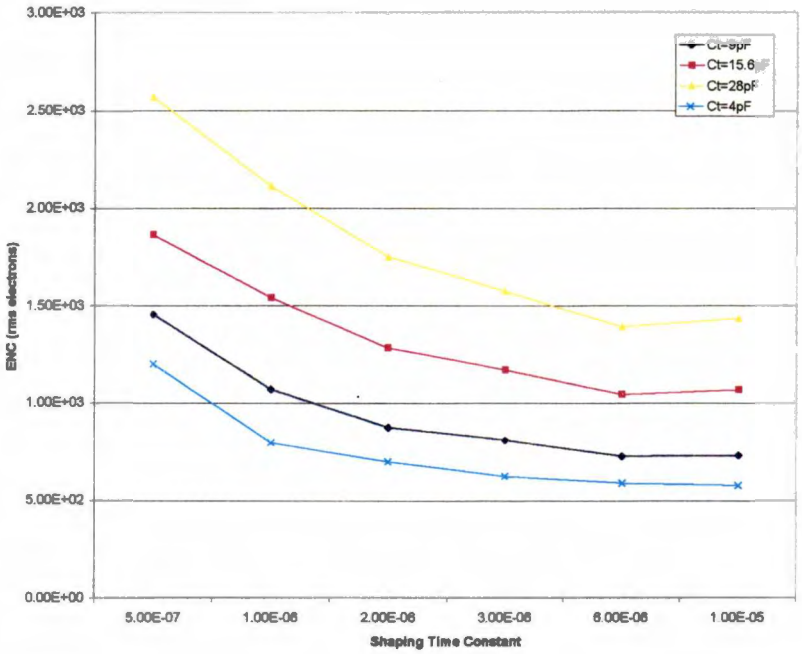


Figure 5.13: Measured bipolar ENC

respectively. The extrapolated 4 pF ENC values compared for unipolar and bipolar pulse shaping in Figure 5.14. The optimum shaping time constant for the Ortec 571 shaper was found to be approximately 6 μs for unipolar shaping, and greater than 6 μs for bipolar shaping. The Ortec 571 shaper's frequency response is given approximately, assuming that all poles are real, by Equaition 5.6,

$$H(s) = \frac{Ks}{\left(s + \frac{1}{\tau}\right)^5}, \tag{5.6}$$

where K is a gain constant. Using this transfer fuction, and assuming that the input device dominates the ENV of the preamplifier the ENC can be calculated. The

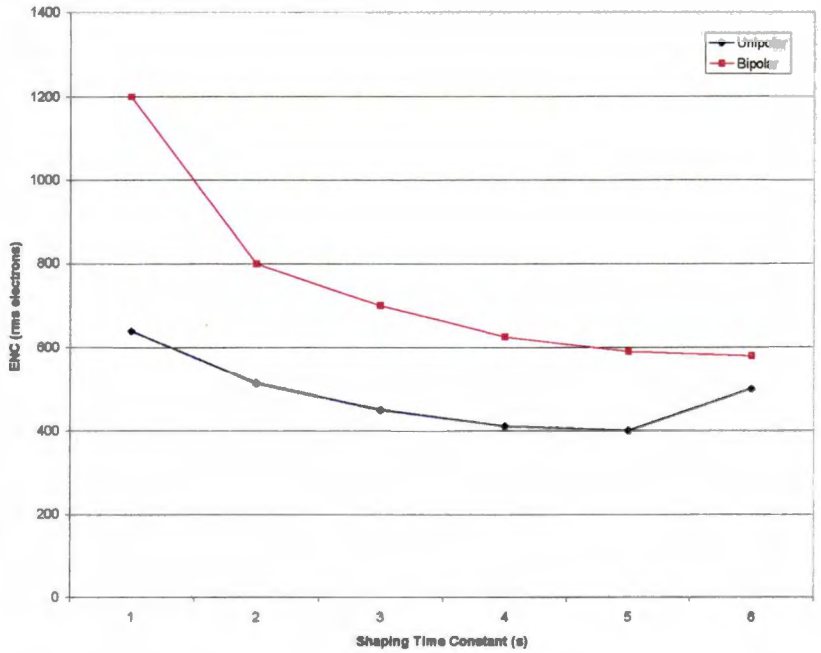


Figure 5.14: Measured ENC, Unipolar versus bipolar shaping for Ortec 571 shaper

shapers can be compared for a time constant that gives identical shaping times (zero crossing time for bipolar). The ENC for the Ortec 571 shaper for a bipolar pulse shape was found for thermal, flicker, and current input noise using the same technique of used in Chapter 3 to find the ENC for the MicroCAT shaper. Then the ENC ration was taken for a given crossover time, and for flicker noise the Ortec 571 shaper was found to give an ENC that was a factor of approximately 1.2 times the expected output of the MicroCAT shaper. Therefore the MicroCAT shaper would provide superior performance to the Ortec shaper at time constants where thermal noise dominates. The flicker noise ENC of the Ortec 571 was found to be a factor of 0.98 times the MicroCAT shaper's flicker noise ENC. For the ENC of the current noise the Ortec shaper was found to have superior performance to the MicroCAT shaper by a factor of 0.81. Taking these

calculations into effect has the effect of lowering the measured ENC at low time constants, and at longer time constants the ENC would be increased. This implies that the optimum time constant for the MicroCAT shaper will be less than that for the Ortec 571 shaper, as predicted in the Chapter 3 theoredical calculations. The measured output ENC of the preamplifier is greater than the predicted theoredical values by a factor of approximately 2.8; however, the theoredical work assumed that the input PMOS device dominated the amplifier's ENV, but in actuallity there are three dominate sources that contibute to the total ENV. The off chip feedback resistor also degrades the noise performance by way of adding parasitic capacitance, and rf pick-up.. The noise performance is expected to be much improved for a preamplifier that utilizes a switch versus a resistor for the reset element, and is directly coupled to the shaper on chip. A complete MicroCAT analog channel was fabricated using this preamplifier with a switch for a reset element, and it will be discused in the final section of this chapter.

5.4.2 *Preamplifier Output Noise Spectrum*

The output noise voltage of the preamplifer was measured to be 800 μVrms using the HP 3400 rms voltmeter, which has a bandwidth of approximatly 10 MHz. The output noise voltage was also measured using a Tektronix 494AP spectrum analyzer with a GPIB interface. The measurement is presented in Figure 5.15. The thermal noise component appears to be high, which reduced the flicker noise corner but increases the total output noise. The spectrum was measured by adding a wide-band gain stage with a voltage gain of approximately –260, which was modified from a previous use [28].

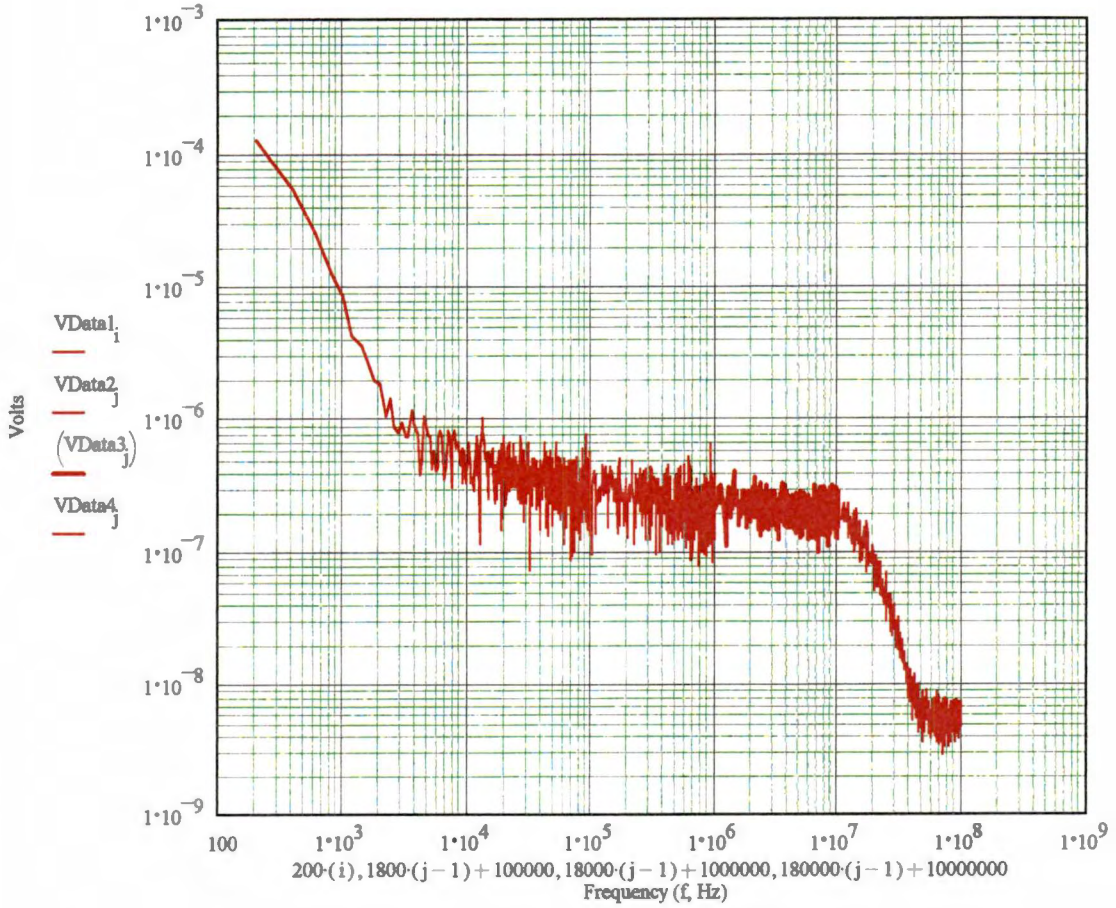


Figure 5.15: Output noise voltage spectrum

5.5 *Experimental Evaluation Summary*

The experimental test values and expected results are compared in Table 5.2. The main cause of deviation of the measured results from the expected results is the fact that total output noise voltage. The actual feedback capacitance is a factor of 5 greater than the expected value. Noise measurements were difficult to make accurately because the die was packaged. Better results could have been obtained with an unpackaged die mounted onto a test board that utilized surface mount devices. This

would allow for a much closer test board layout, thus reducing the stray capacitance, and allowing for much better shielding of the test circuit.

5.6 *MicroCAT Analog Channel*

A complete analog channel was fabricated which utilized a preamplifier with a switch as a reset element. Additional circuitry was designed and fabricated to allow for an automatic reset of the preamplifier as the output bias point approached a negative or positive rail. The circuit is presented in Figure 5.16 in block diagram form. Although simulations indicate correct functionality of the reset circuit, it has not been tested within the alalog channel. A much better noise performance is expected for this preamplifier curcuit because there is no feedback resistor noise, and the circuit is completely monolithic. However, other problems such as charge injection from the switching transistor had to be addressed for this design. Also, during the reseting period, the preamplifier is usless, which adds to the system dead time and thus may increase scan time.

Table 5.2: Experimental and expected results

Parameter	Expected	Measured	Units
Charge Gain	10×10^{12}	3.06×10^{12}	V/C
Rise Time	**20**	**23**	**ns**
Dynamic Range	**+0.8, -2.0**	**+0.9, -2.0**	**Volts**
Output Noise 10 MHz BW	**600**	**800**	μV_{rms}

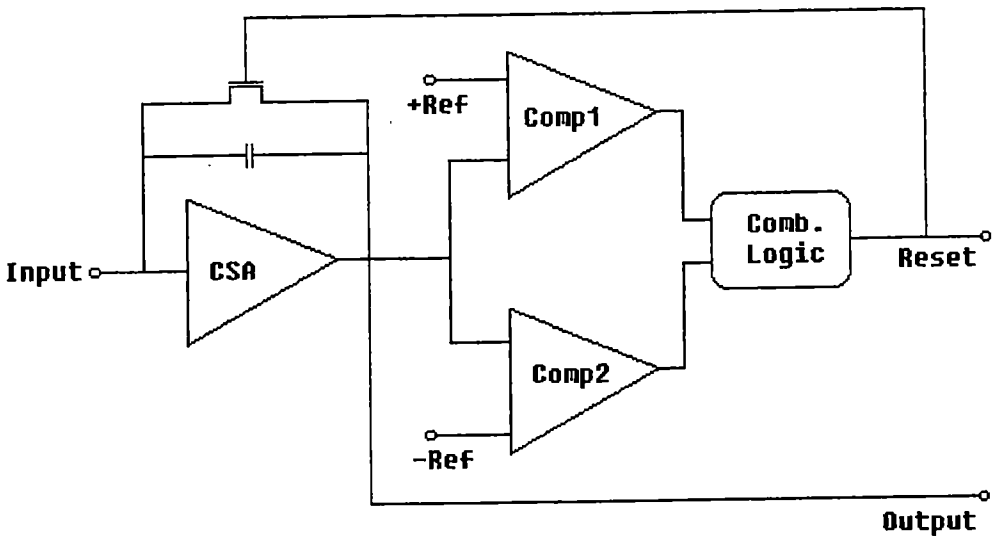


Figure 5.16: Switched reset preamplifier topology

Chapter 6 Discussion and Conclusions

6.1 Discussion

The design of a low-noise, wide-band CMOS charge-sensitive preamplifier for use with a CZT strip detector has been addressed in this thesis. The prototype preamplifier has been evaluated for charge gain, rise time, and noise performance.

One issue of concern is that of using an off chip resistor as a reset element, which degrades the performance of the preamplifier by reducing the charge gain, lowering the phase margin, and increasing the total equivalent noise voltage of the preamplifier. In an effort to increase the charge gain, the preamplifier was designed with a 100 fF feedback capacitor. Using this low size for the feedback capacitor makes the design more susceptible to parasitic capacitance, especially that due to the end-to-end capacitance of the off chip feedback resistor, which can be on the order of 1 pF. The prototype feedback capacitance was measured to be approximately 330 fF, a factor of 3.3 greater than the design value.

The core voltage amplifier's internal feedback loops provided an improvement in DC gain over the basic cascode circuit by a factor of 58.2. However, much attention is necessary at layout to prevent stray capacitance within the local feedback loops from degrading the phase margin of the preamplifier's overall feedback loop, because the phase margin rolls off quickly due to the many high frequency poles of the internal feedback loops. The equivalent noise voltage of the preamplifier is dominated by the input device provided that the input bias current node is low-pass filtered. The input device was sized to give the optimum noise performance for a bipolar shaping amplifier

with a shaping time on the order of 500 ns. The actual measured shaping time of the G_m-C filter designed for the MicroCAT was 920 ns.

6.2 *Future Work*

A full analog channel has been fabricated for the MicroCAT imaging system, and it will be tested in the near future. The preamplifier to be used in the MicroCAT analog channel does not utilize a resistive reset element, but is reset by discharging the feedback capacitor through an on chip transistor switch. The output voltage of the preamplifier is monitored, and when either a positive or negative reference is reached the preamplifier will be reset. This method has only one disadvantage, in that the preamplifier can not be used to detect an event while it is in reset mode, which adds dead time to the channel. However, the reset circuitry provides an output to the system that warns of a reset event in progress. The performance of this preamplifier is expected to be superior to that of the resistive reset preamplifier by providing more accurate charge gain, improved stability against oscillations, and reduced equivalent input noise current.

Additionally, in future revisions of the preamplifier the input PMOS device width should be lowered as given by the thermal noise optimization method presented in Chapter 3 to improve the noise performance of the system. Test results have shown that thermal noise is an major contributor to the ENC at the shaping time chosen; therefore, optimizing for the thermal noise criterion should improve the overall ENC performance.

Finally, one major issue that has not been fully addressed is the interconnections between the preamplifiers and the CZT strips. The preamplifiers should be on the same printed circuit board as the CZT detector to reduce the parasitic capacitance at the input

of the preamplifier, which degrades the system noise performance. A test board that allows for the direct mounting of unpackaged analog channel dice in close proximity to the CZT detector should be constructed.

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REFERENCES

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APPENDICES

APPENDIX A

Device Parameters and SPICE Models for an AMI 1.2 μm Fabrication Run

MOSIS PARAMETRIC TEST RESULTS

RUN: N91A VENDOR: AMI

TECHNOLOGY: SCN12 FEATURE SIZE: 1.2 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.72	-1.04	Volts
SHORT	10.8/1.2			
Idss		203	-102	uA/um
Vth		0.65	-0.84	Volts
Vpt		10.0	-14.2	Volts
WIDE	30/1.2		-6.1	Volts
Ids0		0.6	-469.6	pA/um
LARGE	10.8/10.8			
Vth		0.69	-0.84	Volts
Vjbkd		16.9	-15.0	Volts
Ijlk		-32.8	-10.0	pA
Gamma		0.71	0.94	V^0.5
K' (Uo*Cox/2)		34.4	-12.8	uA/V^2

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology XL

SCN (lambda=0.6)	0.00
AMI_ABN	0.00

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.6/2.4			
Vth		1.06	-1.11	Volts
SHORT	7.2/2.4			
Vth		1.04	-1.04	Volts
LARGE	21.6/21.			
Vth		1.03	-1.02	Volts
K' (Uo*Cox/2)		21.5	-7.0	uA/V^2

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2X1	2X1		
Beta		154	
V_early		37.8	Volts
Vce,sat		0.1	Volts
2X2	2X2		
Beta		156	
V_early		37.2	Volts
Vce,sat		0.1	Volts
2X4	2X4		
Beta		157	
V_early		36.7	Volts
Vce,sat		0.1	Volts
2X8	2X8		
Beta		158	
V_early		36.1	Volts
Vce,sat		0.1	Volts
BVceo		6.9	Volts
BVcbo		28.9	Volts
BVebo		7.9	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Sheet Resistance	51.5	73.8	29.0	20.7	0.05	0.03	1552	ohms/sq
Width Variation (measured - drawn)	-0.67	-0.76	-0.20	0.27	0.14	0.25		microns
Contact Resistance	59.8	38.2	36.2	16.3		0.05		ohms
Gate Oxide Thickness	327							angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	MTL1	MTL2	N_WELL	UNITS
Area (substrate)	297	300	34		19	13	49	aF/um^2
Area (N+active)			1055	692	50	27		aF/um^2
Area (P+active)			1039	686				aF/um^2
Area (poly)				611	45	23		aF/um^2
Area (poly2)					45			aF/um^2
Area (metal1)						42		aF/um^2
Fringe (substrate)	60	163			55	46		aF/um
Fringe (poly)					57	46		aF/um
Fringe (metal1)						59		aF/um
Overlap (N+active)			166					aF/um
Overlap (P+active)			218					aF/um

CIRCUIT PARAMETERS	K		UNITS
Inverters			
Vinv	1.0	1.92	Volts
Vinv	1.5	2.32	Volts
Vol (100 uA)	2.0	0.54	Volts
Voh (100 uA)	2.0	4.40	Volts
Vinv	2.0	2.56	Volts
Gain	2.0	-7.90	
Ring Oscillator Freq.			
MOSIS (31-stage,5V)		65.79	MHz
DIV64 (31-stage,5V)		65.44	MHz
NON_FEATU (31-stage,5V)		41.33	MHz
Ring Oscillator Power			
MOSIS (31-stage,5V)		46.49	uW/MHz/g
DIV64 (31-stage,5V)		0.62	uW/MHz/g
NON_FEATU (31-stage,5V)		0.92	uW/MHz/g

N91A SPICE LEVEL3 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.2700E-08 XJ=0.200000U
TPG=1
+ VTO=0.7194 DELTA=8.2850E-01 LD=1.1830E-07 KP=6.9559E-05
+ UO=658.7 THETA=7.6000E-02 RSH=5.5750E+01 GAMMA=0.7265
+ NSUB=1.7730E+16 NFS=7.1500E+11 VMAX=2.1000E+05 ETA=1.2470E-01
+ KAPPA=3.7710E-01 CGDO=1.8739E-10 CGSO=1.8739E-10
+ CGBO=4.4984E-10 CJ=2.8941E-04 MJ=5.2933E-01 CJSW=1.2265E-10
+ MJSW=1.0000E-01 PB=9.8929E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.4282E-06
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.2700E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.8165 DELTA=2.0000E+00 LD=2.6280E-08 KP=2.1500E-05
+ UO=203.6 THETA=1.0500E-01 RSH=9.1100E-02 GAMMA=0.3809
+ NSUB=4.8750E+15 NFS=6.5000E+11 VMAX=5.1080E+05 ETA=1.0010E-01
+ KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=4.5842E-10 CJ=2.9916E-04 MJ=4.3626E-01 CJSW=1.7444E-10
+ MJSW=1.0000E-01 PB=7.5986E-01
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.4690E-06
```

N91A SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

```
* DATE: Mar 12/99
* LOT: n91a                    WAF: 06
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 3.27E-8
+XJ      = 3E-7         NCH     = 7.5E16           VTH0    =
0.6708006
+K1      = 1.0000595    K2      = -0.0633694       K3      =
4.2938833
+K3B     = -1.4970595   W0      = 5.629407E-7      NLX     = 1E-10
+DVT0W   = 0            DVT1W   = 5.3E6            DVT2W   = -0.032
+DVT0    = 0.6691828    DVT1    = 0.2829494        DVT2    = -0.15
+U0      = 688.8142233  UA      = 2.278116E-9      UB      =
4.576128E-20
+UC      = 5.182443E-11 VSAT    = 1.144513E5       A0      =
0.7089752
+AGS     = 0.1203889    B0      = 1.309342E-6      B1      = 5E-6
+KETA    = -8.926928E-3 A1      = 0                A2      = 1
+RDSW    = 2.429811E3   PRWG    = -1E-3            PRWB    = -
5.383566E-6
+WR      = 1            WINT    = 7.901458E-7      LINT    =
2.538689E-7
+XL      = 0            XW      = 0                DWG     = -
2.163981E-8
+DWB     = 3.393331E-8  VOFF    = -0.15            NFACTOR =
3.751417E-3
+CIT     = 0            CDSC    = 1.506004E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.018881E-3      ETAB    = -
0.0903072
+DSUB    = 1.0165162    PCLM    = 0.8729818        PDIBLC1 =
6.52288E-3
+PDIBLC2 = 8.257221E-3  PDIBLCB = -1E-3            DROUT   =
0.0820569
+PSCBE1  = 3.895461E9   PSCBE2  = 5.359654E-8      PVAG    =
0.010096
+DELTA   = 0.01         MOBMOD  = 1                PRT     = 0
+UTE     = -1.5         KT1     = -0.11            KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9          UB1     = -7.61E-
18
+UC1     = -5.6E-11     AT      = 3.3E4            WL      = 0
+WLN     = 1            WW      = 0                WWN     = 1
+WWL     = 0            LL      = 0                LLN     = 1
+LW      = 0            LWN     = 1                LWL     = 0
+CAPMOD  = 2            XPART   = 0.4              CGDO    = 1.66E-
10
+CGSO    = 1.66E-10     CGBO    = 0                CJ      =
2.894139E-4
+PB      = 0.9892912    MJ      = 0.5293273        CJSW    =
1.226494E-10
+PBSW    = 0.9885823    MJSW    = 0.1              PVTH0   =
0.0591122
+PRDSW   = -816.757313  PK2     = -0.0204107       WKETA   =
3.473399E-3
+LKETA   = -0.0298621    )
```

```
*
.MODEL CMOSP PMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 3.27E-8
+XJ      = 3E-7         NCH     = 2.4E16           VTH0    = -
0.7752444
+K1      = 0.4874131    K2      = -9.478089E-5     K3      =
10.8005614
+K3B     = -2.4621963   W0      = 9.081404E-7      NLX     =
6.621691E-7
+DVT0W   = 0            DVT1W   = 5.3E6            DVT2W   = -0.032
+DVT0    = 1.4193884    DVT1    = 0.3279834        DVT2    = -
0.0527428
+U0      = 288.8781756  UA      = 5.524539E-9      UB      =
5.218147E-19
+UC      = -9.95794E-11 VSAT    = 1.760476E5       A0      =
0.8504225
+AGS     = 0.1545928    B0      = 4.426369E-6      B1      = 5E-6
+KETA    = 1.862657E-3  A1      = 0                A2      = 1
+RDSW    = 1.293667E3   PRWG    = 1.057524E-3      PRWB    = -1E-3
+WR      = 1            WINT    = 8.997552E-7      LINT    =
7.402531E-8
+XL      = 0            XW      = 0                DWG     = -
3.960993E-8
+DWB     = 2.115698E-8  VOFF    = -0.095849        NFACTOR = 1.5
+CIT     = 0            CDSC    = 4.036955E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0208893        ETAB    = 0
+DSUB    = 0.0136371    PCLM    = 1.3712959        PDIBLC1 =
9.081258E-4
+PDIBLC2 = 2.315992E-4  PDIBLCB = -2.370143E-8     DROUT   =
0.2443852
+PSCBE1  = 1.725341E10  PSCBE2  = 4.711905E-9      PVAG    =
7.473999E-3
+DELTA   = 0.01         MOBMOD  = 1                PRT     = 0
+UTE     = -1.5         KT1     = -0.11            KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9          UB1     = -7.61E-
18
+UC1     = -5.6E-11     AT      = 3.3E4            WL      = 0
+WLN     = 1            WW      = 0                WWN     = 1
+WWL     = 0            LL      = 0                LLN     = 1
+LW      = 0            LWN     = 1                LWL     = 0
+CAPMOD  = 2            XPART   = 0.4              CGDO    = 2.18E-
10
+CGSO    = 2.18E-10     CGBO    = 0                CJ      =
2.991556E-4
+PB      = 0.759856     MJ      = 0.436264         CJSW    =
1.744436E-10
+PBSW    = 0.989755     MJSW    = 0.1              PVTH0   =
0.1129185
+PRDSW   = -481.5148875 PK2     = 7.323198E-3      WKETA   =
0.0141729
+LKETA   = 2.713213E-3   )
*
```

APPENDIX B

Part 1: Small-Signal Derivation of Open Loop Gain with a Local Feedback Loop

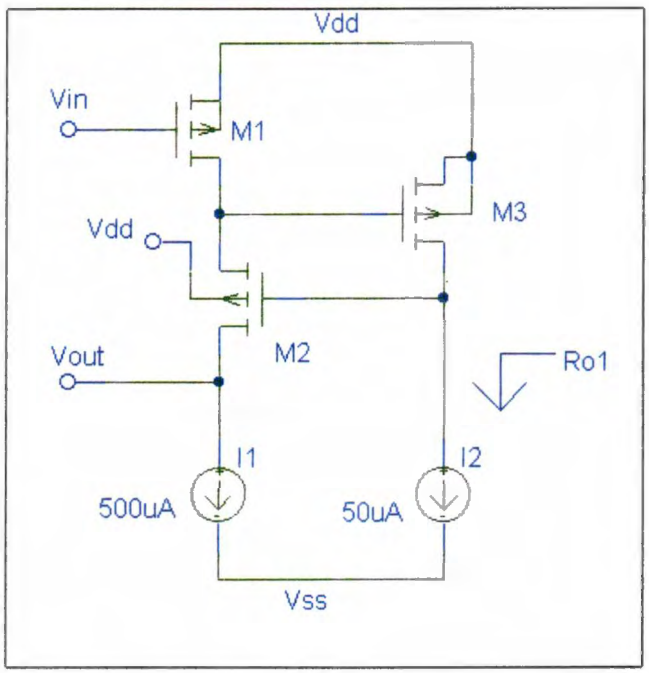

Figure B.1: Cascode with a local feedback loop

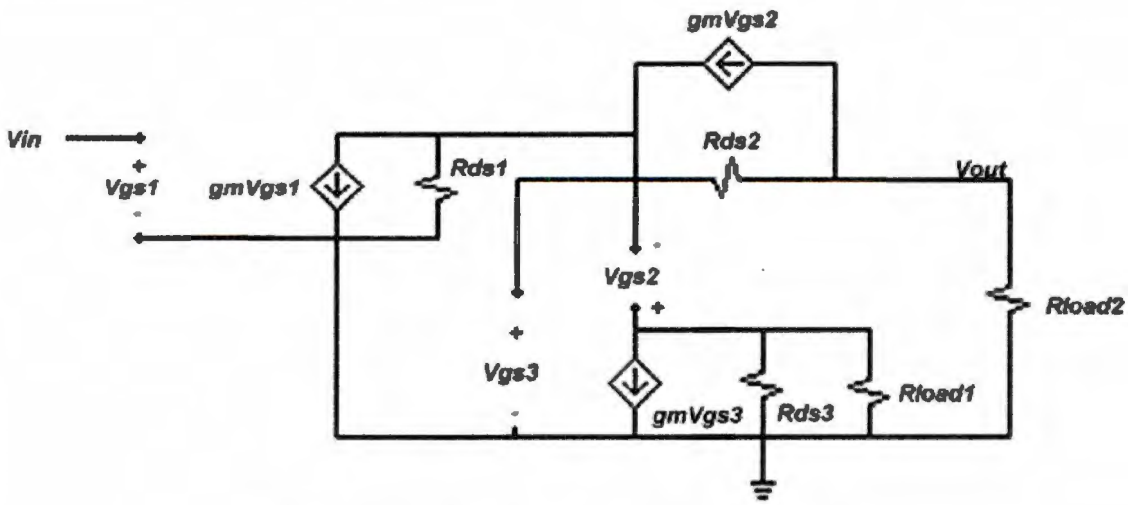

Figure B.2: Small-signal equivalent circuit

$$Vgs3 = rds1 \cdot \left(-\frac{Vout}{Rload2} - gm1 \cdot Vin \right) \tag{B.1}$$

$$gm1 \cdot Vin = Vout \cdot \left(\frac{1}{rds2} \right) + Vgs3 \cdot \left[gm2 \cdot (-gm3 \cdot rds3 - 1) - \frac{1}{rds1} - \frac{1}{rds2} \right] \tag{B.2}$$

$$gm1 \cdot Vin = \frac{Vout}{rds2} + rds1 \cdot \left(\frac{-Vout}{Rload2} - gm1 \cdot Vin \right) \cdot \left[gm2 \cdot (-gm3 \cdot rds3 - 1) - \frac{1}{rds1} - \frac{1}{rds2} \right] \tag{B.3}$$

$$Av = \frac{-\left(-gm1 \cdot gm2 \cdot rds1 \cdot gm3 \cdot rds3 - gm1 \cdot gm2 \cdot rds1 - rds1 \cdot gm1 \cdot \frac{1}{rds2} \right)}{\left[\frac{-1}{rds2} - \frac{rds1}{Rload2} \cdot gm2 \cdot gm3 \cdot rds3 - \frac{rds1}{Rload2} \cdot gm2 - \frac{1}{Rload2} - \frac{rds1}{(Rload2 \cdot rds2)} \right]} \tag{B.4}$$

$$Av = \frac{Rload2 \cdot (-rds1 \cdot gm1 \cdot (gm2 \cdot gm3 \cdot rds3 \cdot rds2 + gm2 \cdot rds2 + 1))}{(Rload2 + rds1 \cdot gm2 \cdot gm3 \cdot rds3 \cdot rds2 + rds1 \cdot gm2 \cdot rds2 + rds2 + rds1)} \tag{B.5}$$

Part 2: Preamplifier Bias Circuit Noise Current Transfer Function

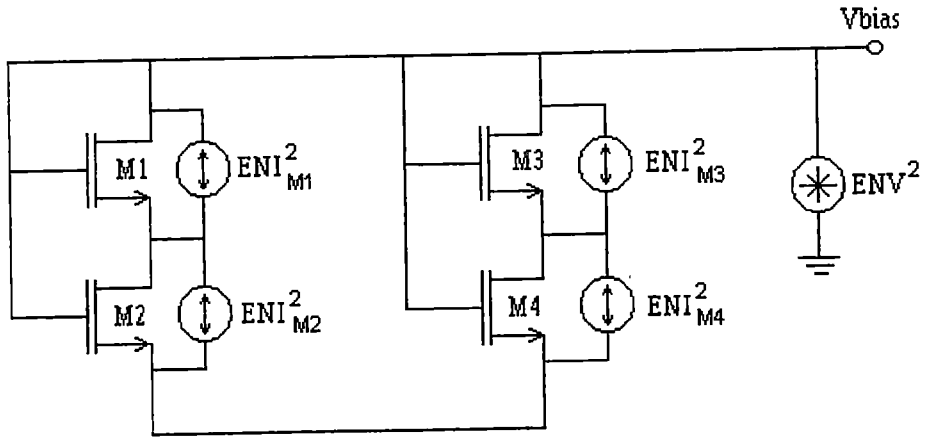

Figure B.3: Preamplifier bias circuit

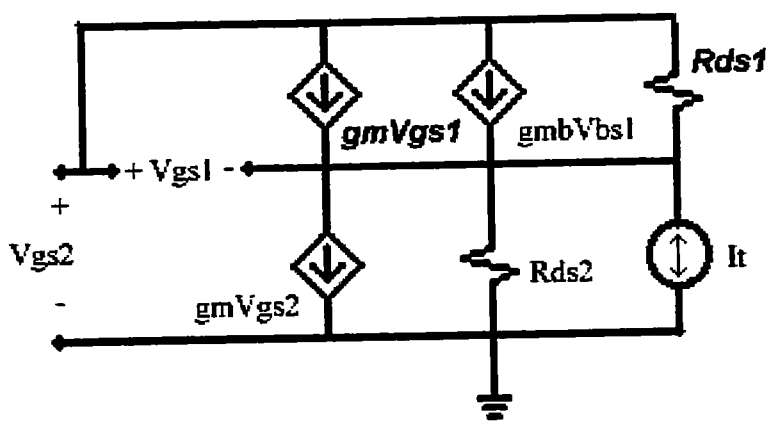

Figure B.4: Small-signal models for M1 and M2

Solving for:

$$\frac{Vgs2}{It} \tag{B.6}$$

$$It + gm1 \cdot Vgs1 + gmb1 \cdot Vbs1 + \left(\frac{Vgs2 - Vbs1}{Rds1}\right) = gm2 \cdot Vgs2 - \frac{Vbs1}{Rds2} \tag{B.7}$$

$$Vgs2 = Vgs1 - Vbs1 \tag{B.8}$$

$$gm1 \cdot Vgs1 + gmb1 \cdot Vbs1 + \frac{Vgs1}{Rds1} = 0 \tag{B.9}$$

$$gm2 \cdot Vgs2 - \frac{Vbs1}{Rds2} = It \tag{B.10}$$

$$\frac{Vgs2}{It} = \frac{1}{gm2 + gds2 \cdot \left[\left(\frac{gmb1}{gm1 + gds1}\right) + 1\right]^{-1}} \tag{B.11}$$

The transfer function for the noise of the top device is obtained simply by moving the test current to the appropriate location, and repeating the above process. Adding the complete bias circuit (M1-M4) has the result of putting a two in the denominator of Equation B.11.

VITA

Lemuel Herbert Thompson II was born in Dyersburg, Tennessee on July 17, 1972. He graduated from Dyersburg High School in 1990, and then attended The University of Tennessee at Knoxville where he was a member of the Tau Beta Pi national engineering honor society. He graduated with the Bachelor of Science in Electrical Engineering in December of 1997, and then began working toward the master's degree while working for the Oak Ridge National Laboratory's Instrumentation and Controls Division. He obtained the Master of Science in Electrical Engineering in August of 1999.