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Characterization of a mixed-signal ASIC Communicatons Signal Processor for cordless telephones

Carlyle L. Reynolds

To the Graduate Council:

I am submitting herewith a thesis written by Carlyle L. Reynolds entitled "Characterization of a mixed-signal ASIC Communicatons Signal Processor for cordless telephones." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

T. V. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

M. J. Roberts, Don Bouldin

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Accepted for the Council:

Associate Vice Chancellor and
Dean of The Graduate School

CHARACTERIZATION OF A MIXED – SIGNAL ASIC COMMUNICATONS SIGNAL PROCESSOR FOR CORDLESS TELEPHONES

A Thesis
Presented for the Master of Science
Degree
The University of Tennessee, Knoxville

Carlyle L. Reynolds
December 1999

DEDICATION

This thesis is dedicated to my wife,

Christi J. Reynolds,

who was patient and supporting

during the writing and throughout my graduate studies.

This thesis would have never been completed

without her encouragement.

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ABSTRACT

This thesis describes the measurement procedures employed to effectively characterize the Lucent Technologies Communications Signal Processor (CSP1009). The results of these measurements are presented and discussed. This study was conducted on the first prototype to be manufactured. The CSP1009 is the analog baseband integrated circuit chip in a three-chip system designed for use in 900 MHz cordless telephones. It was fabricated using a 0.3μm CMOS process. The CSP1009 contains several amplifiers including a programmable gain amplifier (PGA), a telephone line driver amplifier and a speaker driver amplifier. In addition, it contains a charge pump for use in a phase lock loop circuit, a bandgap reference, an analog to digital converter (ADC) and a digital to analog converter (DAC). The amplifiers were characterized by measuring three quantities: gain, power supply rejection ratio, and total harmonic distortion (THD). The output current of the charge pump was measured. The voltage of the bandgap reference was measured at different temperatures. The current consumption of the individual modules was also measured. All of these measurements were taken over process variations and over changes in the power supply voltage. The programmable gain amplifiers have gains ranging from 0dB to 44dB, PSRR of approximately 50dB, and THD less than 0.2%. The reference voltage of 1 VDC is derived from the bandgap voltage reference. The charge pump output current is programmable and ranges from 100μA to 1600μA. The total current consumption of the CSP1009, under loaded conditions, was approximately 7mA. Most of the modules on the first prototype of the CSP1009 performed adequately. However, a few anomalies were found. These include a

DAC offset, low charge pump current, PGA feed-through, and the frequency response of the double sampling circuit rolled off at a lower frequency than expected.

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LIST OF ABBREVIATIONS

AAF	Anti-Aliasing Filter
ADC	Analog to Digital Converter
AI#	Analog Input (# - port number)
AO4	General Purpose Output Amplifier
AP	Audio Precision
ASIC	Application Specific integrated Circuit
BFSK	Binary Frequency Shift Keying
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Analog to Digital Converter and Digital to Analog Converter
CPF	Charge Pump Final Current
CPI	Charge Pump Initial Current
CPOUT	Charge Pump Out
CSP	Communications Signal Processor
DAC	Digital to Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
IC	Integrated Circuit
JTAG	Joint Test Association Group
LNDV	Line Driver

MAN	Microphone Negative Input
MAP	Microphone Positive Input
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OSCIN	Oscillator In
PC	Personal Computer
PDCNT	Pulse Count
PGA	Programmable Gain Amplifier
PGMO	Programmable Gain Microphone Amplifier
PLL	Phase Lock Loop
PSIN	Pre-Scale In
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
RF	Radio Frequency
SIO	Serial Input/Output Port
SYNTHC	Synthesizer
TC	Temperature Coefficient
THD	Total Harmonic Distortion
VCO	Voltage Controlled Oscillator
VDC	Volts of Direct Current
VDDA	Analog Positive Power Supply Line
VDDL	Line Driver Positive Power Supply Line
VDDS	Speaker Amplifier Positive Power Supply Line

VREF	Voltage Reference
VSSA	Analog Negative Power Supply Line
VSSL	Line Driver Negative Power Supply Line
VSSS	Speaker Amplifier Negative Power Supply Line

Chapter 1 Introduction

1.1 Introduction

An overview of the Lucent Technologies Communications Signal Processor (CSP1009) and the system for which it was designed is discussed in this chapter. In addition, a brief history of the cordless telephone will be presented. This will include a discussion of the advantages and improvements associated with the 900 MHz-frequency range. It should be pointed out that due to the proprietary nature of the modules in the CSP1009, no detailed circuit diagrams are shown or analyzed in this thesis.

1.2 History of the Cordless Telephone

With the advent of the cordless telephone in the early 1980's, people could roam about their places of residence or business free of cords, all the while, having a conversation with a friend or client. This was viewed as being a major convenience. No longer were people restricted to sitting within a few feet of the telephone. However, as cordless telephones became more popular, the problems became more evident. When the first cordless telephone hit the market, the Federal Communication Commission (FCC) decided to use the 46 MHz band for transmission and the 49 MHz band for reception, relative to the base station [FCC1]. The operation within this band was limited to the use of ten channels or ten different frequencies and was later increased to 25.

There were several problems associated with a limited number of channels. Padgett (1984) outlines several of these problems as being. One problem was the possibility that two different users could be on the same frequency. This would lead to interference, with one user's conversation being audible on another user's line. In addition, the telephones were transmitting an analog signal, which made encryption of the transmission difficult and unpractical. Any instrument capable of receiving 46 MHz – 49 MHz and in close proximity of the transmitter could easily intercept the conversation. Digital transmission would easily facilitate encryption of the information. However, the bandwidth of the channels was restricted to 20 kHz and a high-rate digital transmission is not possible within this bandwidth. Finally, with the transmitted power restriction on this band, the telephones were only capable of transmitting short distances, depending on their surroundings. Obviously, with the increasing popularity of the cordless telephone, something had to change.

When the FCC opened the 902 MHz – 928 MHz band, they did a few things differently. First, they did not set channel bands within the frequency range. The entire band was open for use. Nor did they restrict the bandwidth used within this band; thus, enabling the use of digital transmission. In addition, the allowed transmission power was raised, increasing the effective communication distance. These guidelines provided much more versatility within the 900 MHz spectrum. It is now possible to search for a clear frequency band over a much greater frequency range, since there are no longer restrictions placed on the number of channels; thus, increasing the probability of having an uninterrupted conversation. It is also possible to encrypt the digital transmission,

which greatly increases privacy and security. Finally, and most important to the consumer, the increased transmission power greatly enlarges the effective communication distance, depending on surroundings.

1.3 The CSP1009 and Supporting Devices

Figure 1.1 shows the current version of the Lucent Technologies 900 MHz cordless telephone. If one were to go out to his/her favorite department store and buy a 900 MHz cordless telephone, he/she would find four or five major brands. In each of the different brands of telephones, three integrated circuit (IC) chips make up the system. This system is found in the base station and the handset. The three chips consist of a digital signal processor (DSP) chip, an analog baseband chip and a radio frequency (RF) chip. In each of the different brands of telephones, different brands of chips will be found. For instance, a particular telephone may contain an American Micro Devices (AMD) DSP, a Lucent Technologies analog chip and an Analog Devices RF chip. The manufacturer of the telephone would mix and match, with the major concern being cost. Lucent Technologies' plan was to develop a "three chip solution". That is to manufacture all three chips and sell them as a package at a cost less than the cost of mixing and matching. Lucent believed if this could be done, it would give them the majority of the 900 MHz cordless telephone market.

This thesis concentrates on the analog baseband chip (CSP1009). The measurements discussed in the following chapters were done on the first prototype that was fabricated. The characterization was done in June 1998 through August 1998. It

Figure 1.1: Lucent 9110, 900MHz Cordless Telephone

should be pointed out that revisions were made following this characterization and they are not discussed in this thesis.

The Lucent "three chip solution" is made up of the DSP (B900), the analog baseband chip (CSP1009) and the RF chip (W9009). "The CSP1009 is a mixed-signal ASIC (Application Specific Integrated Circuit)" [LUCENT1] realized in a 0.3µm CMOS (complementary metal oxide semiconductor) process. A CMOS process makes it possible to create an IC that contains both PMOS and NMOS transistors in a common substrate. CMOS technology was chosen for the CSP1009 to allow lower power supply voltages to be used. This reduces the power consumption of the chip, which is important with any system powered by a battery. The CSP1009 interfaces with the DSP through a serial interface port (SIO) that allows for access to the thirty 16-bit control registers. The CSP1009 interfaces with the RF chip through a radio control interface. The CSP1009

supports the W9009 with a frequency synthesizer, a binary frequency shift keying modulator (BFSK) and a BFSK correlation demodulator. It also contains an analog CODEC, which consists of an analog-to-digital converter (ADC) and digital-to-analog converter (DAC).

A block diagram of a basic cordless telephone handset and base station are shown in Figure 1.2 and Figure 1.3. These figures illustrate how the three-chip system operates in a cordless telephone. They also show graphically how the CSP1009 fits into the system. In the handset, some of the responsibilities of the CSP1009 include:

- Amplifying, digitizing and modulating (to the intermediate frequency – IF) the users voice from the microphone, in preparation for transmission by the W9009.
- Demodulation, digital-to-analog conversion and amplification of the received signal, which is routed to the speaker.
- Alerting the user of an incoming call.
- Digitizing and modulating signals from the B900, such as number tones from the keypad.
- Keeping the phase lock loop synchronized by generating current pulses that control the voltage controlled oscillator.

In the handset the responsibilities of the CSP1009 include:

- Coupling the ring detection signal to B900.
- Digitizing and modulating to IF signals from the B900, such as the command to "ring" the handset.

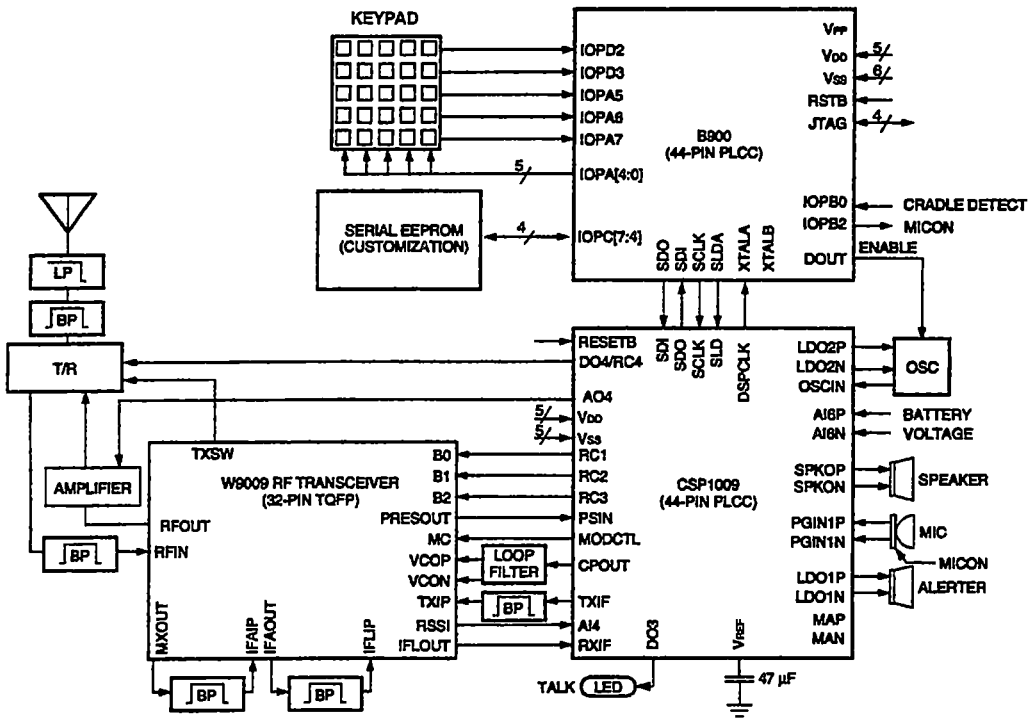


Figure 1.2: Block Diagram of a Basic Cordless Telephone Handset

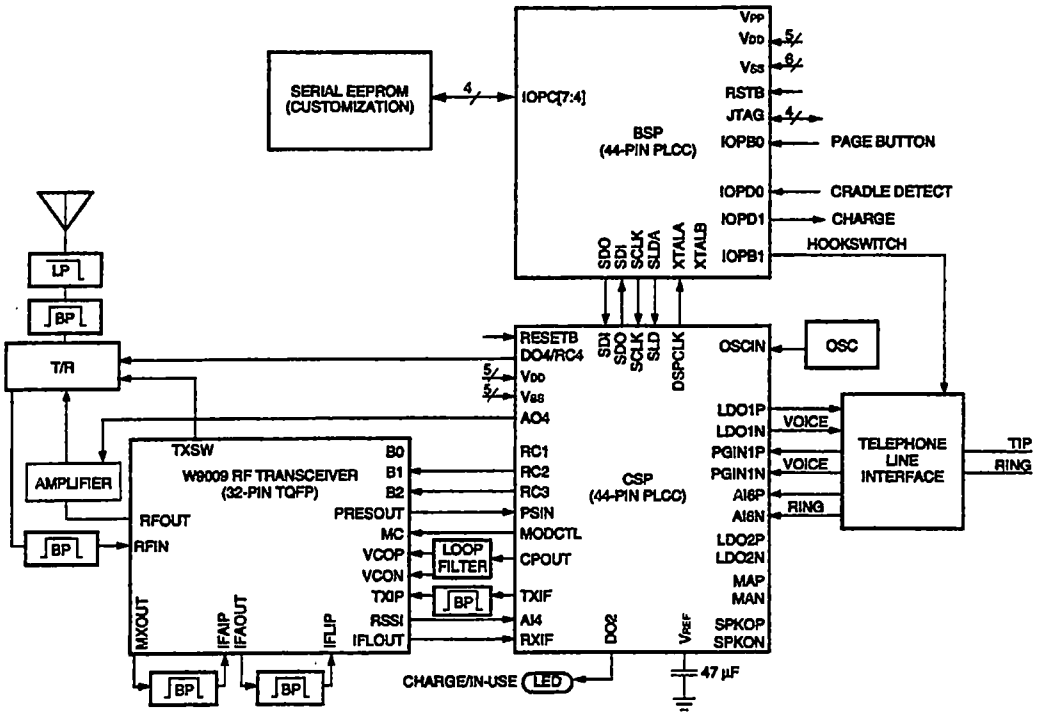


Figure 1.3: Block Diagram of a Basic Cordless Telephone Base Station

- Demodulation, digital-to-analog conversion and amplification of the local users voice, which is routed to the telephone line.
- Amplifying, digitizing and modulating to IF the received voice signal from the telephone line.
- Synchronizing the PLL as above.

Figure 1.4 shows simplified block diagram of the CSP1009. It has three front-end differential amplifiers consisting of two programmable gain amplifiers (PGA1 and PGA2), and one programmable microphone amplifier (PGMO). The CSP1009 has two analog differential inputs (AI6P, AI6N and AI7P, AI7N) and two single-ended inputs

(AI4 and AI5). It has three differential output drivers including two line drivers (LDO1 and LDO2), one programmable speaker amplifier (SPKR), and one single ended output amplifier (AO4). The ADC has the capability of placing digital words on to the SIO for the DSP or the RF chip. The DAC has the capability of taking digital words off the SIO from the DSP or the RF chip. The output of the DAC can be routed to any of the output amplifiers.

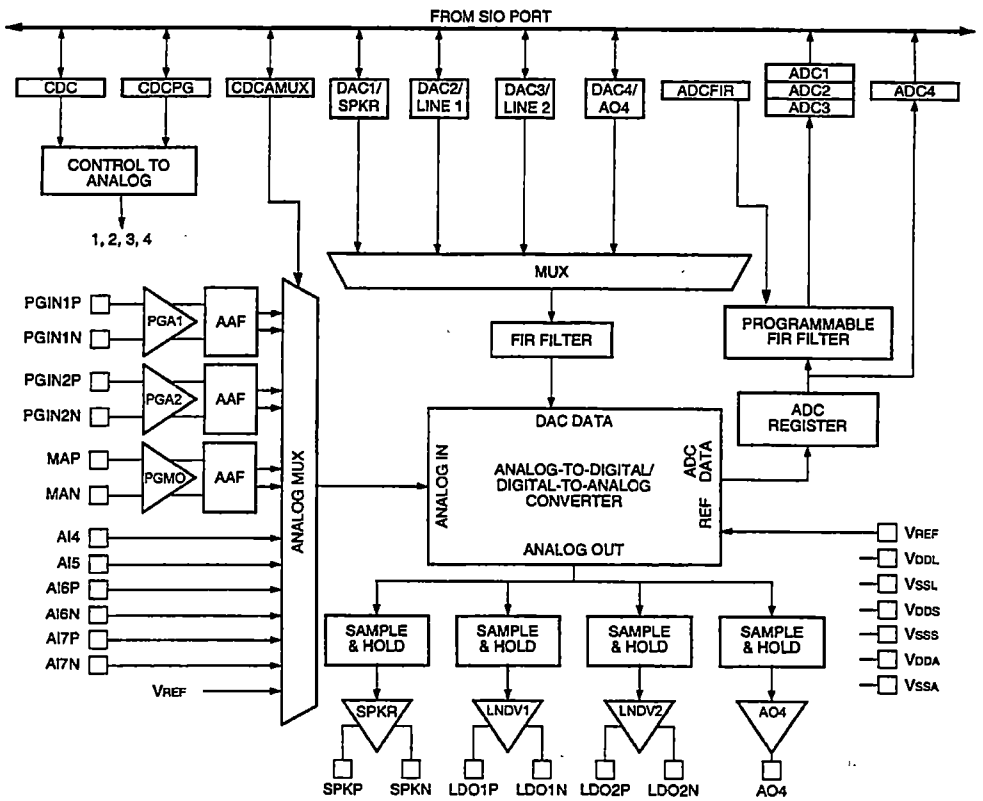


Figure 1.4: Simplified Block Diagram of the CSP1009

For the measurements in this thesis, the ADC and DAC are simply connected together. That is, the ADC does a conversion and the DAC converts it back. This is indicated in the figures with the ADC/DAC set into a gray box.

The CSP1009 is available in a 44-pin package and a 68-pin package. The 44-pin package supports a single line telephone. The 68-pin package supports a dual line telephone. Figure 1.4 shows the modules and pins available on the 68-pin device. On the 44-pin device, the following pins are not available: AI5, AI7P, AI7N, PGIN2P and PGIN2N. The measurements discussed in this thesis were all taken on the 44-pin device.

The chip accommodates three separate power supply connections. These include the SPKR amplifiers supply, VDDS and VSSS, the LNDV amplifiers supply, VDDL and VSSL, and the remainder of the analog circuitry supply, VDDA and VSSA. For these measurements VDDA, VDDS, and VDDL were in the range of 2.8 VDC to 3.7 VDC. VSSA, VSSS, and VSSL were all grounded.

This thesis will address the following issues in relation to the modules within the CSP1009; verify the functionality, test to ensure that all of the specifications are met, identify any problems with the device, and determine testing procedures to document those problems. In addition to these tasks, a characterization procedure will also be developed. This will be done in order to document the process, which in turn can be used as a testing guide for any similarly designed ASICs. In an effort to minimize measurement time and simplify the characterization process, an automated testing procedure will be developed.

Chapter 2 Theory of Operation of the CSP1009 and Tests Conducted

2.1 Introduction

This chapter will describe the modules within the CSP1009. The information will include the purpose of the module. This chapter also contains some basic information on the software programmability of the CSP1009, which includes discussion about the registers and what operations those registers control.

2.2 Programming the CSP1009

Many of the modules on the CSP1009 are software controllable. As far as the system is concerned, the B900 (DSP) communicates with the CSP1009 through a serial input/output interface (SIO). This interface uses four pins on the CSP1009. For the procedures discussed in this paper, the CSP1009 was connected to a personal computer (PC) through a Joint Test Association Group (JTAG) interface. A text file from the PC is compiled to digital signal processing (DSP) assembly language, then sent to the JTAG module via the serial port. The JTAG interface then downloads the assembled code to the CSP1009. The code is stored in 16 bit registers. The information in the registers controls certain operations of the CSP1009. The Lucent Technologies CSP1009 Data Sheet contains a complete discussion of the SIO and the registers. However, for this thesis, only a basic description of the software control will be presented.

A couple of the registers will be discussed to give the reader a feel for what the registers are and what they control. The two most used registers in this study are shown in Figure 2.1. The "CODEC CONTROL REGISTER" controls what modules on the CSP1009 are enabled/disabled. Table 2.1 gives the bit locations and defines the abbreviations used in Figure 2.1. The modules are enabled by writing a 1 to the appropriate bit location or disabled with a 0. The "CODEC GAIN REGISTER" controls the gains of the programmable gain amplifiers. The four bits for each amplifier allow 16 gain settings. The gain is set be writing the binary number that corresponds to the desired gain setting (shown in Chapter 3) to the appropriate location.

2.3 Processing Variations

There are approximately 10-15 processing steps involved in fabricating a CMOS IC. During these steps, a number of different procedures are carried out. These procedures include etching, diffusing and annealing. Each of these procedures is a carefully and precisely timed event. When fabricating a large number of these IC chips, the goal is to ensure that the operational characteristics of each of the chips are identical. The precise duplication of the procedures outlined above is necessary for this to occur. However, during the fabrication process, there exists a certain range of error. Therefore, the prototypes tested for this thesis were supplied in three process variations from the Lucent Technologies foundry. The process types were characterized as slow, nominal and fast. The slow and fast designators refer to the worst case variations at both ends of the process.

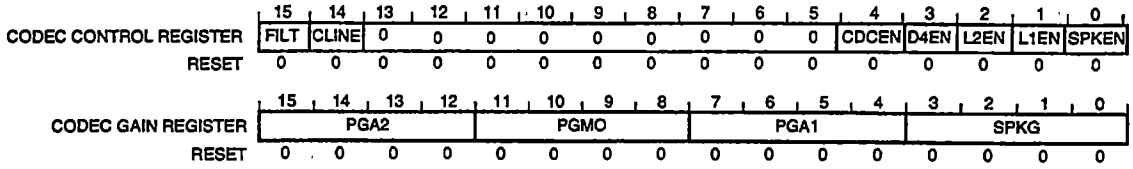


Figure 2.1: Two of the 16 Registers on the CSP1009

Table 2.1: Bit Locations and Descriptions for Figure 2.1

Bit Location	Abbreviation	Description
[15]	FILT	Filter – not used or discussed in this thesis
[14]	CLINE	Discussed Later in this chapter
[4]	CDCEN	ADC/DAC enable/disable
[3]	D4EN	AO4 amplifier enable/disable
[2]	L2EN	Line Driver 2 enable/disable
[1]	L1EN	Line Driver 1 enable/disable
[0]	SPKEN	Speaker driver enable/disable
[15-12]*	PGA2	Programmable gain amplifier (2) gain settings
[11-8]*	PGMO	Programmable gain microphone amplifier gain settings
[7-4]*	PGA1	Programmable gain amplifier (1) gain settings
[3-0]*	SPKG	Speaker amplifier gain settings

* CODEC gain register

The slow chip is fabricated by purposely delaying some or all of the procedures. In contrast to this, the fast chip is rushed through the fabrication procedures, thus, spending less time at some or all of the points during the process. The nominal chip proceeds through the process at the design rate of speed. Therefore, this chip has the greatest probability of being manufactured. The importance of producing these three types of IC chips is to give the circuit design engineer a better understanding of how the circuit behaves under these extreme conditions.

2.4 Double Sampling

The digital-to-analog converter (DAC) presents an analog signal to the output amplifiers. Preceding the output amplifiers (AO4, speaker and line driver), there is a double sampling network. The double sampling network gets its name from the fact that it effectively doubles the sampling rate. Figure 2.2 shows the double sampling network. The analog signal from the DAC is in the form of steps. An example of this signal is shown in Figure 2.3. This figure shows a 1 kHz sine wave sampled at 32 kHz. The double sampling network samples this analog signal and holds it for the output amplifiers. The two SAMPLEP switches allow the DAC output to be sampled at a rate of 16kHz or 32kHz depending on the selected mode. The two SAMPLEP switches operate on the same clock signal. Therefore, they open and close at the same time. The switches, $\phi 2$ and $\phi 3$ operate with clock signals that are out of phase with each other. This allows the network to smooth out the DAC signal. Therefore, the double sampling network is

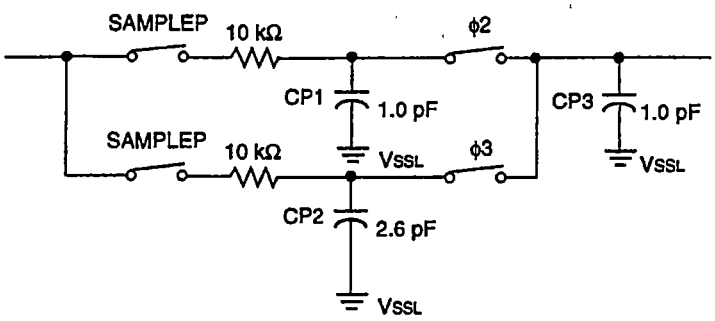


Figure 2.2: Double Sampling Network for the Output Amplifiers

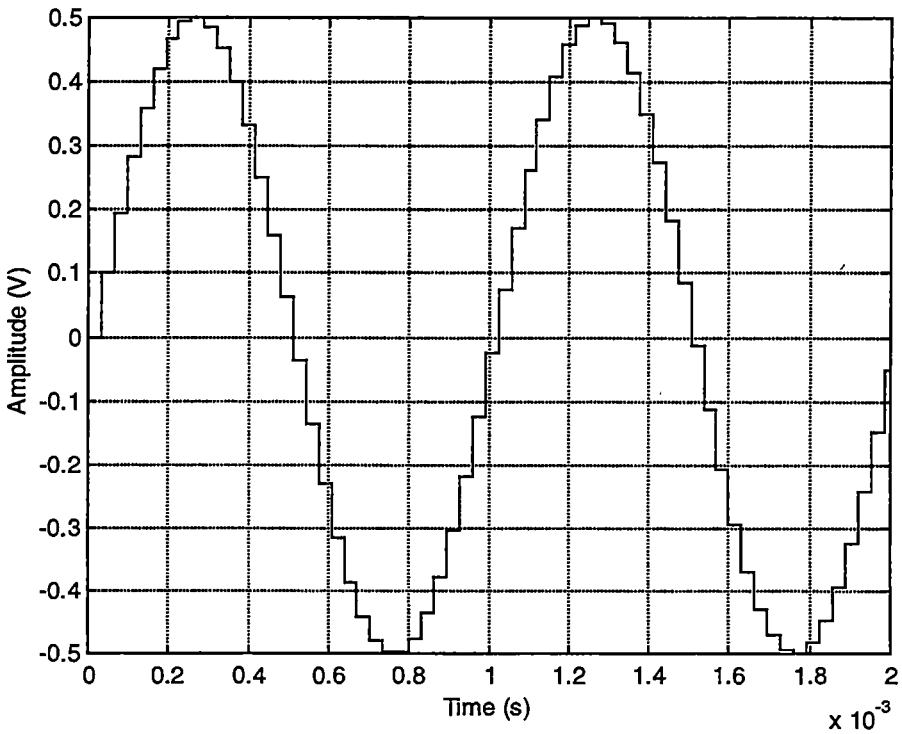


Figure 2.3: A 1kHz Sine Wave Sampled at 32kHz that is Representative of DAC Output

essentially a smoothing filter. To demonstrate this effect, Figure 2.4 shows the 1 kHz signal from Figure 2.2 sampled at 64 kHz.

2.5 AO4 Amplifier

The AO4 amplifier is a single-ended amplifier. It has no specific purpose and it was included only as a spare general-purpose amplifier. The input is connected to the DAC. The output of the AO4 amplifier is connected to pin AO4. The AO4 amplifier is displayed in Figure 2.5. The gain of the amplifier is set by feedback resistor Rf and resistor R1. The gain is calculated using

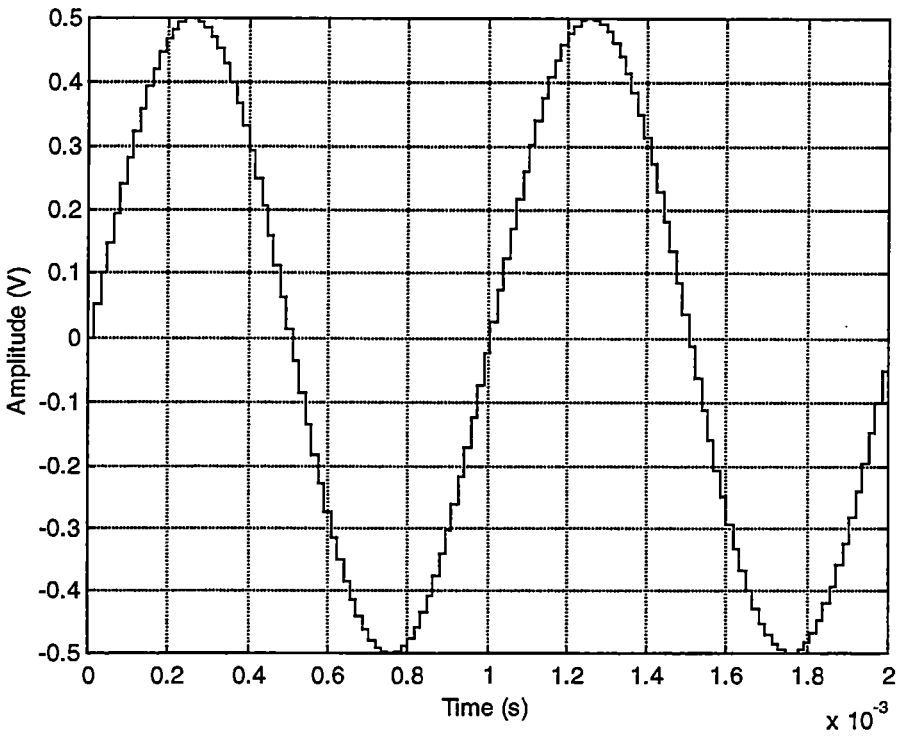


Figure 2.4: A 1kHz Sine Wave Sampled at 64kHz to show the Effects of Double Sampling

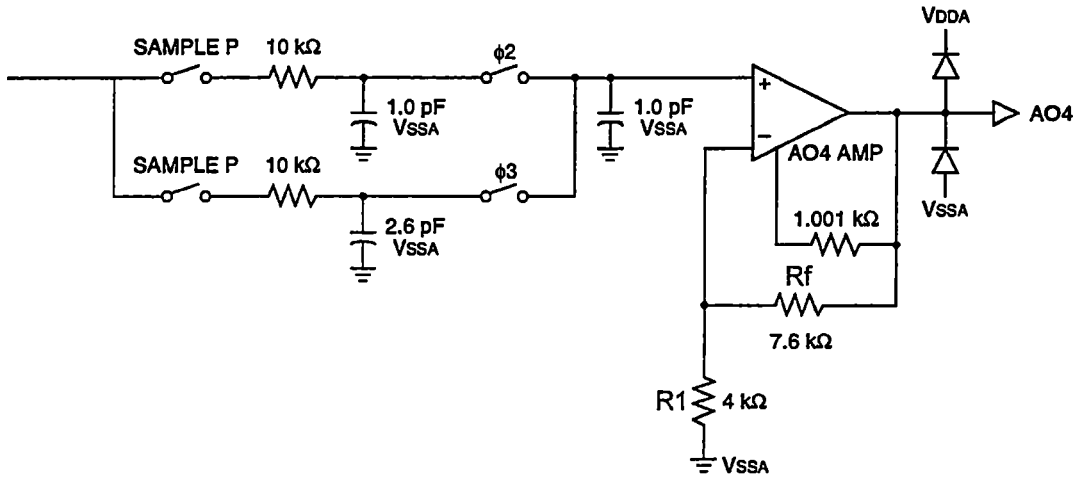


Figure 2.5: Simplified Block Diagram of the AO4 Amplifier

$$AO4\_Gain = 1 + \frac{Rf}{R1} = 1 + \frac{7.6k}{4.0k} = 2.9 = 9.25dB. \qquad (2.1)$$

The 1.001kΩ resistor shown in the figure is a compensation resistor. This resistor is used to improve the stability of the amplifier.

2.6 Bandgap Voltage Reference

A voltage reference is a DC voltage source that has a very low temperature coefficient. A bandgap voltage reference is a DC reference that is realized by "canceling the negative temperature dependence of a *pn* (diode) junction with a positive temperature dependence from a PTAT (proportional to absolute temperature) circuit" [JOHNS&MARTIN1]. A simplified block diagram is shown in Figure 2.6. The *pn* junction is the base-emitter voltage (V_{BE}) of the transistor connected as a diode. The V_{BE} voltage can be shown to have about a –2.0mV/°C temperature coefficient. The PTAT, or

thermal voltage (V_T) generator, can be designed to have a positive temperature coefficient. The magnitude of the positive temperature coefficient will depend on the actual design of the generator. Regardless of the magnitude, the voltage can be increased using some gain, *K*, to approximately +2mV/°C. This will effectively cancel out the negative temperature coefficient of the V_{BE} when the two voltages are summed together, thus, producing a voltage that is stable with respect to temperature. For silicon with a bandgap voltage of 1.206V, the reference voltage will be approximately 1.26V. The reader is encouraged to see Johns & Martin (1997) for a detailed analysis of this phenomenon. Figure 2.6 is shown in most of the literature. It gives the reader a general view of how the bandgap reference operates. However, the figure may give a distorted view of what the actual circuit might look like. The following discussion is presented to clarify this. It may or may not be a representation of the bandgap circuit used on the CSP1009.

Figure 2.7 shows a simplified circuit diagram of a bandgap reference. Brokaw (1974) presents this circuit and analysis. The amplifier with the feedback loop will hold the voltage, at the collectors of Q1 and Q2 equal. By sizing the emitter of Q_2 some x times larger than Q_1, a V_{BE} mismatch is introduced in the transistors. Since $R_1 = R_2$ the currents, I_{R1} and I_{R2} must be equal.

The circuit gives

$$V_{REF} = V_{BE2} + V_{R4}, \tag{2.2}$$

where

$$V_{R4} = I_{R4} \cdot R_4 = 2 \cdot I_{R3} \cdot R_4, \tag{2.3}$$

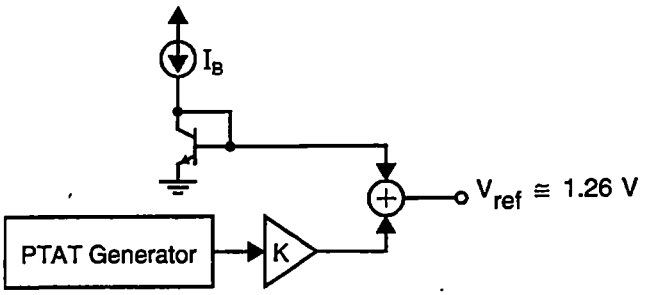


Figure 2.6: Simplified Block Diagram of a Bandgap Reference

since

$$I_{R4} = 2 \cdot I_{R3}. \tag{2.4}$$

Also

$$I_{R3} = \frac{V_{R3}}{R_3} = \frac{V_{BE2} - V_{BE1}}{R_3} = \frac{\Delta V_{BE}}{R_3}. \tag{2.5}$$

Substituting (2.5) into (2.3) gives

$$V_{R4} = \frac{2 \cdot \Delta V_{BE} \cdot R_4}{R_3}. \tag{2.6}$$

Substituting (2.6) into (2.2) gives

$$V_{REF} = V_{BE2} + \frac{2 \cdot R_4}{R_3} \cdot \Delta V_{BE}. \tag{2.7}$$

Johns & Martin show that the "difference of two base-emitter junctions (ΔV_{BE}) biased at fixed but different current densities" make up a PTAT generator.

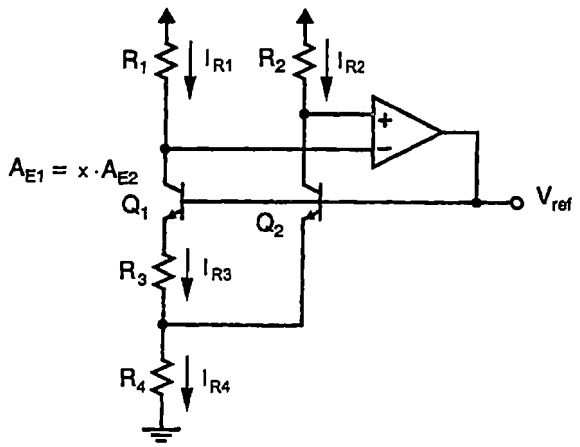


Figure 2.7: Simplified Circuit Diagram of a Bandgap Reference

Recognizing that

$$K = \frac{2 \cdot R_4}{R_3}, \tag{2.8}$$

it becomes clear that Equation 2.7 realizes the general function shown in Figure 2.5.

The bandgap reference measurements described in this thesis are actually for a voltage of approximately 1V. This voltage (VREF) is derived from the bandgap voltage of 1.26V.

2.7 Charge Pump

The charge pump in the CSP1009 is part of the phase lock loop (PLL) circuit. Figure 2.8 shows the modules of the PLL that are in the CSP1009. The external voltage controlled oscillator's (VCO) signal comes into the CSP1009 (PSIN) from the W9009 (RF chip) after being pre-scaled down in the W9009. The VCO signal goes through a

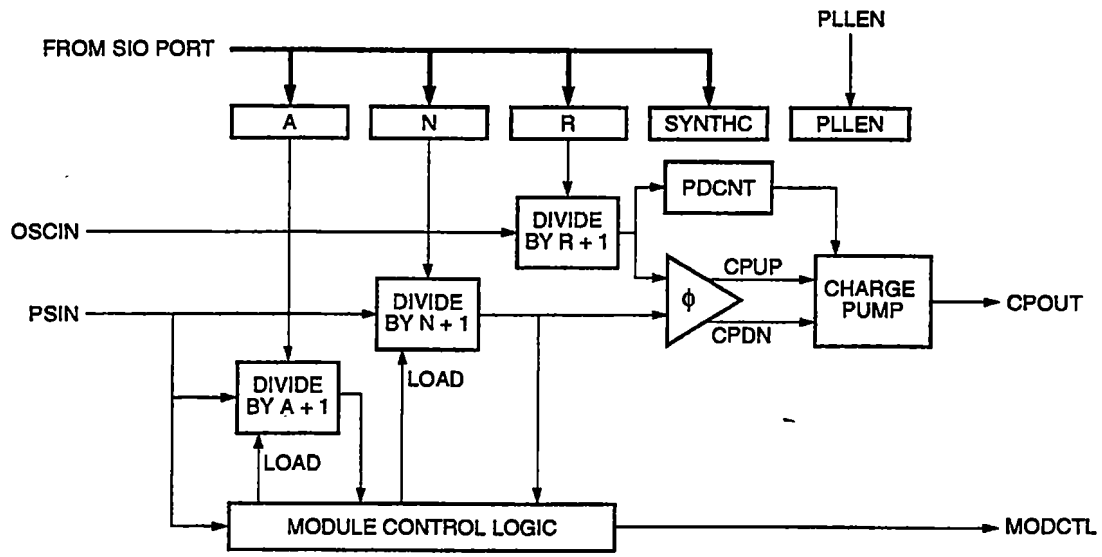


Figure 2.8: Simplified block diagram of the Charge Pump and Supporting Modules

divide-by-(N + 1) counter and is fed to the phase comparator. The external system clock (10.24 MHz) comes into the CSP1009 (OSCIN) and goes through a divide-by-(R + 1) counter before reaching the phase comparator. The phase comparator then issues a command to the charge pump. This command can be either pump up (CPUP) or pump down (CPDN) depending on the phase relationship of the two signals. The charge pump then adjusts its output accordingly. This output (CPOUT) is fed to the VCO through a loop filter to synchronize the VCO with the reference clock. The R and N values are set by the binary value of their respective registers. The charge pump is enabled and controlled by the synthesizer (SYNTHC) register. The entire PLL circuit is enabled/disabled by setting or clearing bit 11 of the control register.

2.8 Line Driver Amplifier

The line driver (LNDV) amplifier is a differential amplifier made up of two single-ended channels. It couples the user's voice to the telephone line via a line-matching transformer. It is capable of driving both a 1200Ω transformer with a differential output and a 600Ω transformer with a single-ended output. The amplifier has 2 gain settings, 6dB and 12dB. However, the 12dB gain is only possible with a power supply voltage above 3.3V. This insures no signal clipping. A simplified circuit diagram of the LNDV amplifier is shown in Figure 2.9.

The amplifier consists of two identical channels. For this reason, only one will be discussed. The gain is set by the feedback resistor, Rfa, and resistors R1a and R2a. The CLINE control bit makes the MOSFET appear as a short (with a small on resistance) or an open. When CLINE = 0, resistor R2a is in the circuit and the gain is

$$LNDV\_GAIN = 1 + \frac{Rfa}{R1a + R2a} = 1 + \frac{4.5k}{1.22k + 2.75k} = 2.13 = 6.58dB. \quad (2.9)$$

When CLINE = 1, resistor R2a is shorted out and the gain is (neglecting on resistance):

$$LNDV\_GAIN = 1 + \frac{Rfa}{R1a} = 1 + \frac{4.5k}{1.22k} = 4.68 = 13.42dB \quad (2.10)$$

2.9 Programmable Gain Amplifier

The programmable gain amplifier (PGA) is a differential front-end amplifier. Its main purpose is to maintain the signal level, at the input of the analog-to-digital converter (ADC), to approximately the full-scale value. Software monitors the voltage level

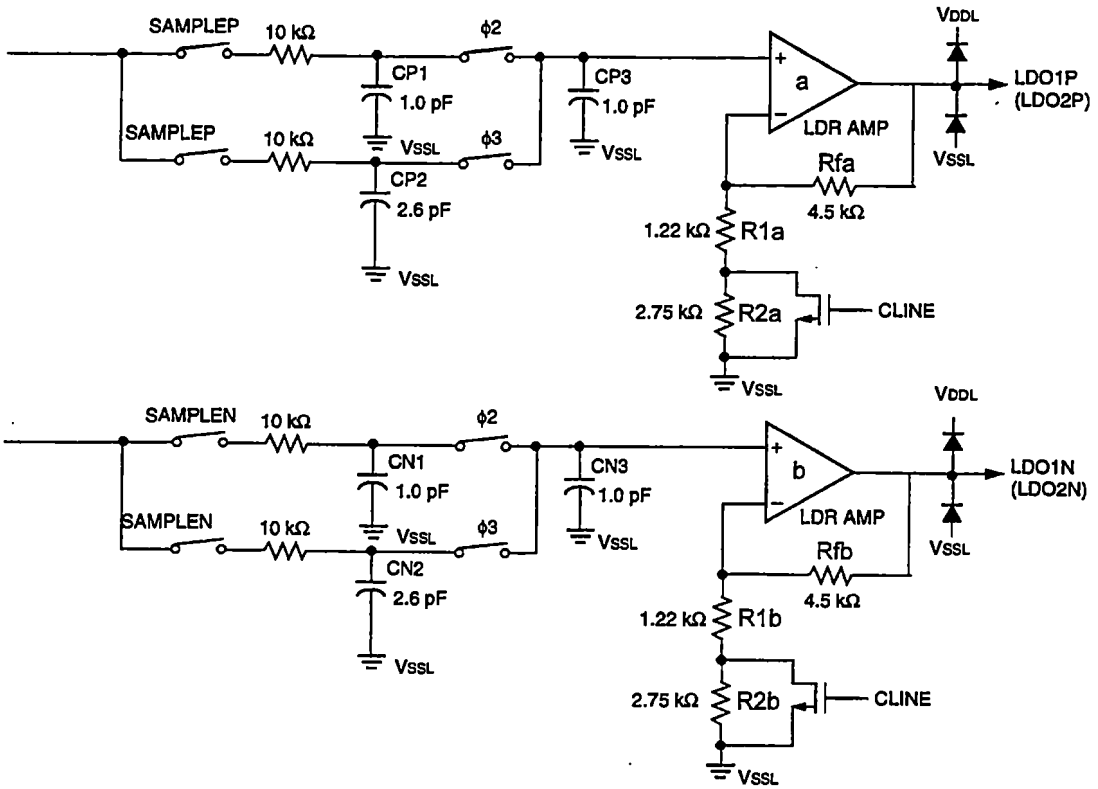


Figure 2.9: Simplified Block Diagram of Line Driver Amplifier

coming into the ADC and automatically adjusts the gain of the PGA to keep the signal level near the full-scale value. When the ADC sees a full scale input, the resolution of the ADC is maximized.

A simplified block diagram of the PGA is shown in Figure 2.10. The CSP1009 contains two identical PGAs, PGA1 and PGA2. For this reason, only PGA1 was characterized in this thesis. The inputs to the PGA are connected to the pins, PGIN1P and PGIN1N. The PGA receives the voice signal from the telephone line and couples it to the ADC through an anti-aliasing filter. The purpose of an anti-aliasing filter is to

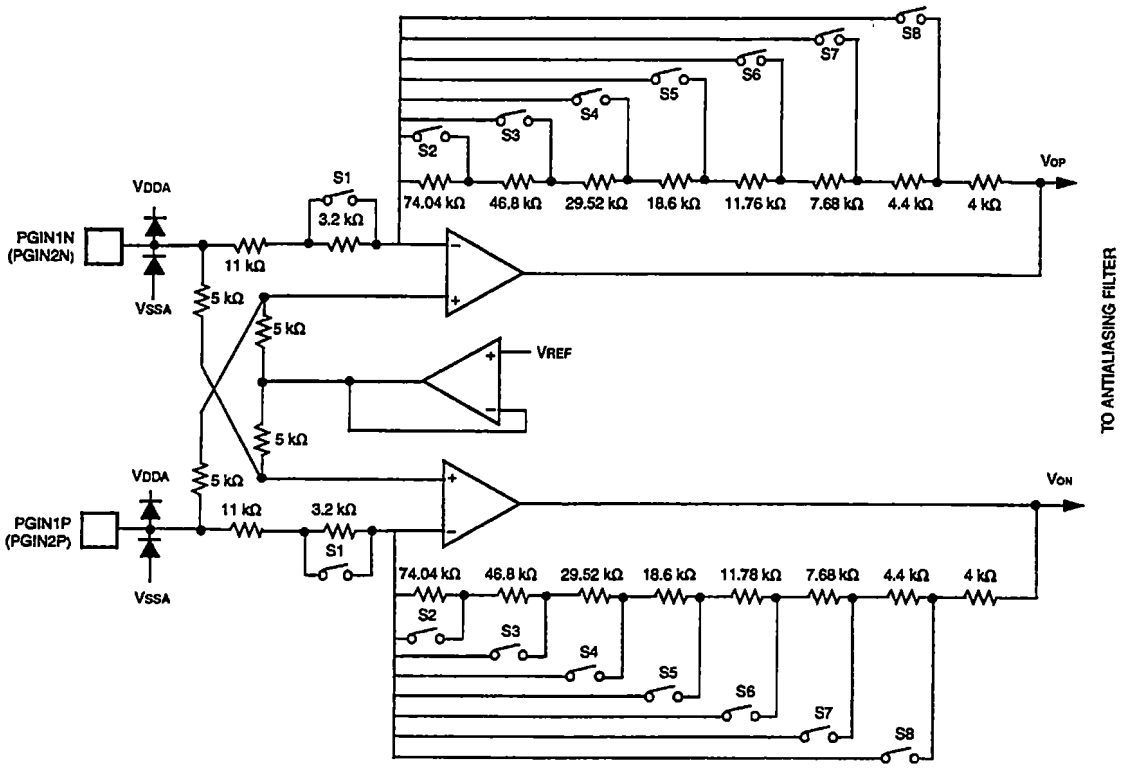


Figure 2.10: Simplified Block Diagram of Programmable Gain Amplifier

"limit the bandwidth of the analog signal to less than half the sampling frequency" [DATEL1]. This ensures a high enough sampling frequency to prevent an alias frequency from being recovered. The anti-aliasing filter is a low-pass filter with a 3dB frequency of 3.7 kHz. This attenuates the voltage of any frequencies outside of the voice band before entering the ADC. The voice band includes frequencies up to 4 kHz.

The amplifier is made up of two identical channels. Therefore, only one will be discussed. The channels are biased at the reference voltage (VREF). VREF is approximately 1VDC. The gain of the PGA is selected by setting switches S1 through S8 open or closed to achieve the desired gain. The switches are actually MOSFET devices.

Their gates are driven by a network of digital logic that has a 4 bit binary input. This binary input selects one of the 16 different gain levels. The gain of the PGA ranges from 0dB to 28dB in increments of 2dB. The binary selection is done by setting bits [7-4] of the CODEC control register.

2.10 Programmable Gain Microphone Amplifier

The programmable gain microphone amplifier (PGMO) is also a differential front-end amplifier. It is very similar to the PGA. Therefore, only the differences will be discussed in this section. The simplified block diagram of the PGMO is displayed in Figure 2.11. The PGMO amplifies and couples the user's voice to the ADC through the anti-aliasing filter. The inputs to the PGMO are the pins, MAP and MAN. The gain of the PGMO is programmed by setting bits [11-8] of the CODEC control register. The possible gains range from 16dB to 44dB in increments of 2dB.

2.11 Speaker Amplifier

The speaker (SPKR) amplifier is a differential output amplifier. It is similar to the LNDV amplifier. Figure 2.12 shows a simplified block diagram of the SPKR amplifier. The inputs of the SPKR amplifier are connected to the DAC. The programmable gain settings are from −14dB to 14dB in increments of 2dB. The gain is set using bits [3-0] of the CODEC control register. The outputs of the SPKR amplifier are connected to the pins, SPKP and SPKN.

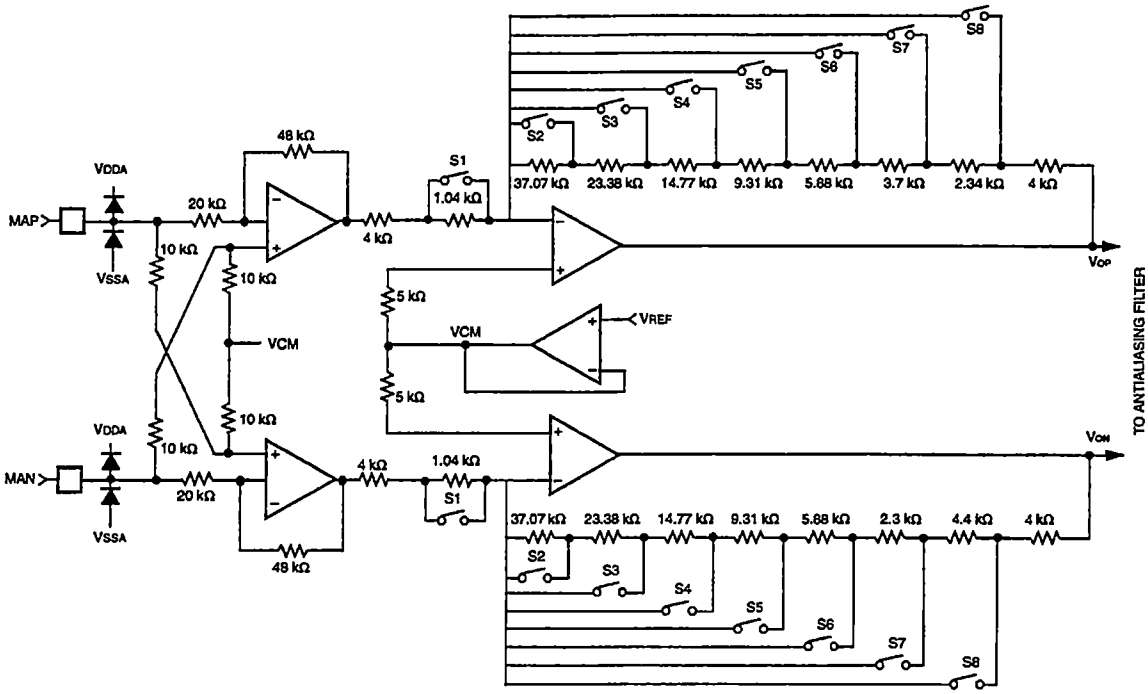


Figure 2.11: Simplified Block Diagram of Programmable Gain Microphone Amplifier

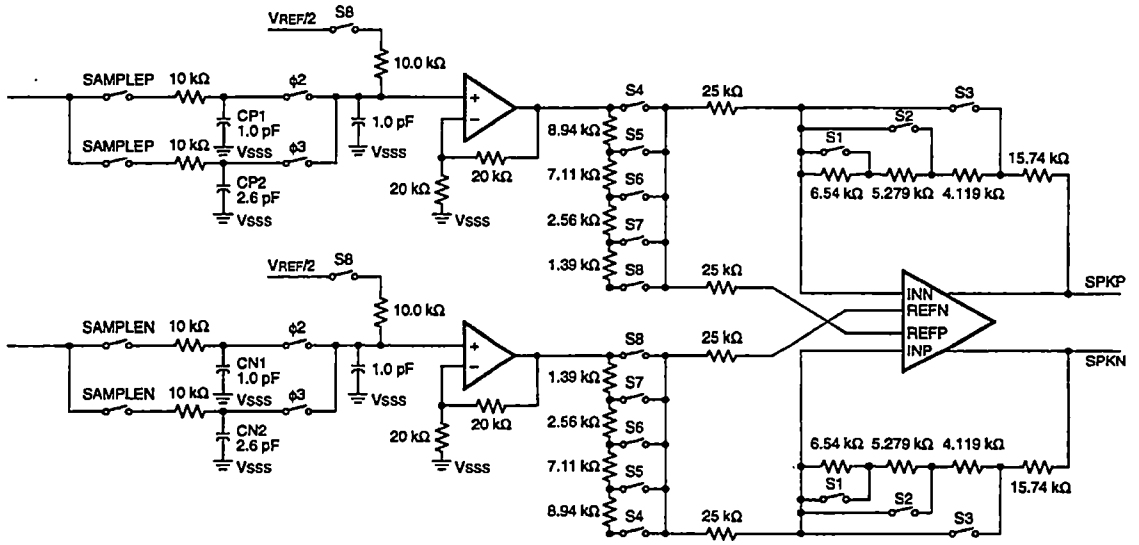


Figure 2.12: Simplified Block Diagram of the Speaker Amplifier

Chapter 3 Measurement Considerations and Procedures for the CSP1009

3.1 Introduction

This chapter describes in detail the methods used to accomplish the measurements and gather the data. In addition, the test equipment used in making the measurements will be described. The chapter is split into sections; each section pertains to a module on the CSP1009. Within the various sections, the different tests that were performed on the module are described. There are two major reasons for doing these measurements. First, the functionality of the modules had to be confirmed. Second, the modules were characterized by the data obtained from the measurements.

The characterization results allow the circuit designers to thoroughly check their modules and compare the actual performance with the design goals. This enables them to find anything that may have been overlooked, and better understand the effects of process variations; thus, producing information that is valuable when making future improvements.

The Lucent Technologies Systems Group in Allentown, Pennsylvania provided the test board for the measurements. The board was basically the circuit board used in the telephone handset with some modifications. The board contained a plug-in socket for the CSP1009 to allow for easy insertion and removal. A serial input/output interface was available to allow downloading of the control registers with a PC via a JTAG module. The Microelectronics Group Technician, Dale Muffley, did most of the modifications.

The modifications included separating the power supply lines for separate access. The reason for this will become clear later in this chapter. In addition, test pins were soldered to access points needed for a specific test.

3.2 Test Equipment Used

Audio Precision, System Two

The Audio Precision, System Two (AP) was used to generate all of the various input signals. The AP was also used to take the gain, power supply rejection ratio (PSRR), and total harmonic distortion (THD) data. The hardware interfaces with a PC. The AP has its own software and is only controlled using this software. The programming consists of selecting specific modules and linking them together to achieve the desired input and output display characteristics. The instrument can be used as a function generator, which is programmed to supply the desired input to one channel; then, data are read on another channel. The AP can be programmed to perform a fast Fourier transform (FFT) and plot the signal amplitude in decibels with respect to frequency. The AP also can be programmed to sweep a set of desired frequencies, while calculating the THD. The THD is then plotted with respect to frequency. The AP is a complete testing system and has the capability of operating over a frequency range of dc to 100kHz. For the measurements discussed in this paper, a frequency limit of 20kHz was imposed. The AP also allows an external DC voltage level to be modulated with a sinusoidal signal. This procedure was used in the PSRR measurements. For the

gain and PSRR measurements, an arbitrary waveform was used. This waveform consists of common frequencies below 20kHz. This will be described in detail later in this chapter. The AP's software used to accomplish the tasks performed in this chapter had been previously installed by the Microelectronics Group Circuit Designer, Kouros Azimi. However, some modifications were made to these programs to facilitate automated testing.

LeCroy Digital Oscilloscope

The LeCroy model LC574AL is 4-channel digital oscilloscope. It was used to capture the data taken for the charge pump. The scope contained a serial interface that allowed data to be pulled into the PC. It was also used for general signal measurement and monitoring.

Temptronic Temperature Control Machine

The Temptronic model TP04010A ThermoStream was used to control the package temperature of the chip during the bandgap reference measurements.

3.3 Important Notes

There are a few important notes that should be kept in mind when considering the measurements discussed in this chapter. They are as follows:

- All of the measurements were taken at room temperature (25°C), unless otherwise noted.
- Each of the modules discussed were tested on integrated circuits from three different processes, slow, nominal and fast.

- The outputs of the programmable gain amplifier (PGA) and programmable gain microphone amplifier (PGMO) cannot be accessed directly. Therefore, they were routed through the speaker (SPKR) amplifier, with the voltage gain set to 0dB. Thus, the voltage gain of the SPKR amplifier will not change the overall system gains. However, it does affect the PSRR and THD results for the PGA and PGMO.
- When tests were done with full-scale outputs, the output was first checked with an oscilloscope to insure no signal distortion. This was done prior to the data being recorded.
- The mention of sampling or no sampling refers to the double sampling modules in front of the output stages.

3.4 Arbitrary Waveform

The Microelectronic Group's Technician, Dale Muffley previously programmed the arbitrary waveform used in the measurements. The frequencies desired in the arbitrary waveform are placed into a spreadsheet file and the AP reads this file and creates the waveform. The AP gives all of the frequencies equal amplitudes and adds them together linearly. The composite signal is then scaled to the amplitude desired by the user. Table 3.1 shows the arbitrary waveform frequencies used in the gain and PSRR measurements. This waveform is shown in Figure 3.1.

Table 3.1: Arbitrary Waveform Frequencies Used in Gain and PSRR Measurements

Frequency (Hz)
20
50
100
200
500
1000
2000
3000
4000
5000
6500
8000
10000
12000
15000
20000

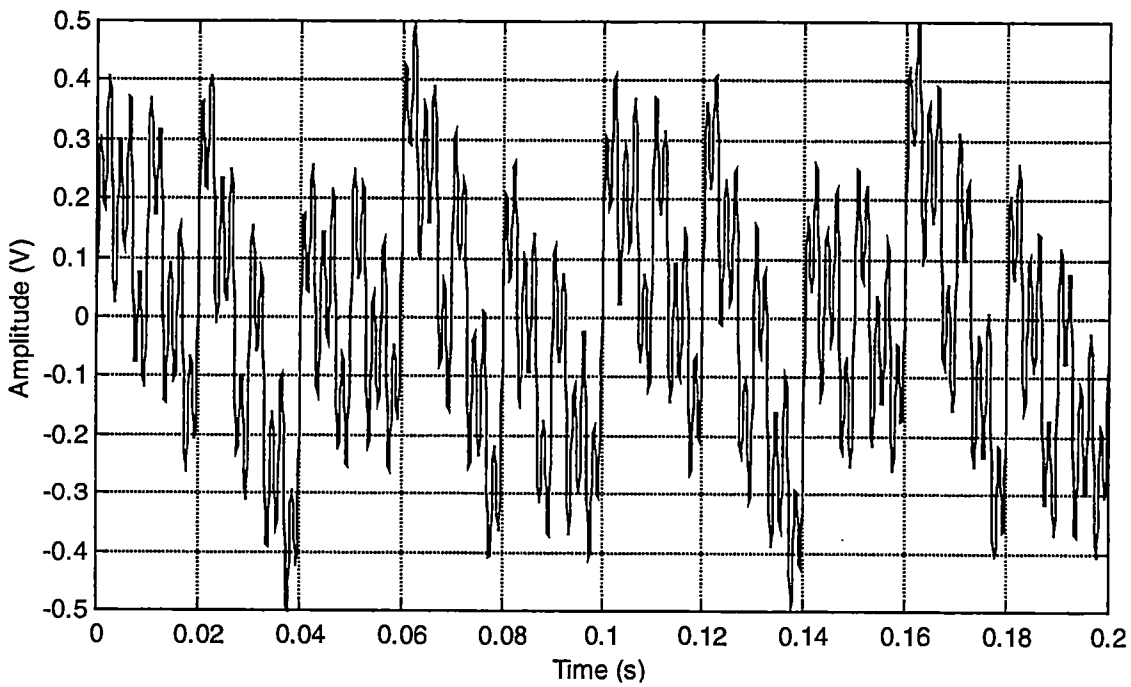


Figure 3.1: Two periods of the arbitrary waveform used in the gain and PSRR measurements.

Two periods of a 1Vpp waveform are shown. The amplitude shown is arbitrary; the amplitude changes from test to test.

The arbitrary waveform is used to eliminate the need of changing the input signal a number of times during the measurement process. This cuts down the testing time and simplifies the procedures. When the arbitrary waveform is used, the AP takes a measurement by tuning a bandpass filter to each one of the frequencies in the arbitrary waveform. At each of the frequencies, a measurement is taken. When measurements have been taken at all of the frequencies the AP compiles the data and plots a graph versus frequency. When "arbitrary waveform" is mentioned in this and following chapters it refers to the arbitrary waveform discussed in this section. The amplitude of the waveform changes from test to test, but the frequency components remain the same throughout.

3.5 Amplifier Measurements

Three measurements were taken to characterize the amplifiers. These measurements were voltage gain, power supply rejection ratio, and total harmonic distortion. This section provides a brief explanation of each of these measurements and explains why each is important.

3.5.1 Gain

The gain of an amplifier is essentially the whole purpose and definition of an amplifier. There are many types of gain. The important one for this paper is voltage gain. It is easily illustrated in the following equation in which the multiplying factor K represents the gain of the amplifier:

$$Output\_Voltage = K \times Input\_Voltage \tag{3.1}$$

To measure the gain the arbitrary waveform is applied to the inputs of the amplifier. A measurement of this input signal is taken with the AP. Next, a measurement at the output of the amplifier is taken. The voltage gain can then be calculated using the equation

$$\text{Gain} = \text{Measured Output Decibel Level} - \text{Measured Input Decibel Level}. \tag{3.2}$$

3.5.2 Power Supply Rejection Ratio

Noise can easily be introduced through the power supply lines. Some examples would be the 60 Hz hum from the ac line voltage or the noise from digital circuits that are attached to the same supply. In addition, the CSP1009 was designed for battery operation. The battery voltage can fluctuate from changing load conditions. The power supply rejection ratio (PSRR) is a measure of the amount of noise coupled from the power supply lines to the output of the amplifier. It is usually given in decibels (dB) form and is calculated using Equation 3.3.

$$PSRR = 20 \times \log_{10}\left(\frac{\text{signal amplitude on the power supply}}{\text{signal amplitude at the output}}\right) \tag{3.3}$$

The amplitude, or the peak-to-peak voltage, could be used in this equation. The following example clarifies this measurement. The power supply voltage is modulated

with a 0.5Vpp 1 kHz signal. At the output of the amplifier, the 1 kHz signal is measured to be 0.005Vpp. This results in a PSRR of 40dB.

The PSRR of the amplifiers was determined by modulating the power supply voltage with a 0.5Vpp arbitrary waveform for the differential case. The 0.5Vpp signal was used to obtain a large variation of the supply voltage. For example, at a supply voltage of 3.3V the voltage would actually be varying from 3.05V to 3.55V. A differential output will increase the PSRR. Since both channels of the amplifier are using the same supply causing the outputs to vary similarly. Therefore, looking at the outputs differentially the change is not observed. However, the single-ended output does not share this benefit since one end of the load is tied to ground. Therefore, a much smaller signal, a 0.1Vpp arbitrary waveform was used to modulate the power supply voltage in the single ended case. The PSRR of the amplifier was calculated using Equation 3.4.

PSRR = Measured Decibel Level of the Supply - Measured Output Decibel Level **(3.4)**

3.5.3 Total Harmonic Distortion

A harmonic frequency is a multiple of some fundamental frequency. For example, a 1kHz fundamental frequency has harmonics at 2kHz, 3kHz, 4kHz, ..., and all other integer multiples. "When a single-frequency signal is applied to the input of an amplifier, the output waveform may contain frequency components that include the fundamental and several harmonics" [PIERCE&PAULUS1]. These harmonics are generated from the nonlinear transfer characteristics of the active devices in the amplifier. Therefore, the THD can be interpreted as a measure of the amplifier's linearity. The

THD is the root-mean-squared (rms) value of the harmonics of some fundamental frequency given as a percentage of the rms value of the fundamental. The equation for THD is

$$THD = \frac{\sqrt{(2nd\_harmonic)^2 + (3rd\_harmonic)^2 + (4th\_harmonic)^2 + \cdots}}{\sqrt{(fundamental)^2}} \times 100 . \quad (3.5)$$

Some common values for the harmonics and fundamental are amplitude or peak-to-peak values. The important thing is to keep them consistent. For the purpose of this thesis, the THD calculation was limited to the fourth harmonic of the fundamental.

The THD of the amplifier was tested at various gain settings. To give the measurements a common reference point, an output signal amplitude was chosen. That is, every THD measurement was taken with the amplifier supplying the same output signal amplitude. Therefore, the input signal amplitude has to be changed when the gain is changed. A typical mid-scale output signal value of 0.5Vpp was used. Once the output signal is adjusted to 0.5Vpp the AP then scans through the test frequencies and automatically calculates the THD at each frequency. The AP calculates the THD out to the fourth harmonic.

Table 3.2 shows the test frequencies used for the fundamental frequencies in the THD measurements. The THD was measured over this range to cover the frequencies in the voice band.

Table 3.2: THD Test Frequencies

THD (Hz)
20
25
32
40
50
62
80
100
130
160
200
250
320
400
500
620
800
1000
1300
1600
2000
2500
3200
4000
5000

3.6 Automated Testing

Many of the measurements discussed in this chapter are repetitive. Because of this repetitiveness, an automated testing procedure was developed while taking these measurements to reduce the testing time. A basic overview with some specific points will be discussed in this section.

The software for the AP includes a Visual Basic editor. Visual Basic simplifies port access and communications from a PC to an external device via a serial interface. A Tektronix programmable power supply was procured. This allowed the power supply voltage to be changed using software. The AP is fully software programmable. The software was written so that it controlled every aspect of the measurement process. For example, a typical program would do the following: set the power supply to the desired voltage, download the chip settings to the CSP1009, take the necessary measurements, and export the data to a spreadsheet file. A very helpful instance was with the THD measurements. A loop was used in the software to set the output peak-to-peak voltage of the amplifier. This was done by automatically adjusting the input voltage until the output voltage was approximately 0.5Vpp. Then the desired data were taken. The Visual Basic programs written to take the measurements are shown in Appendix A.

3.7 Power Supply Voltages

The majority of the modules were tested with a power supply voltage in the range of 2.8V to 3.7V. The CSP1009 is rated for a power supply voltage range of 3.1V to

3.6V. The 2.8V tests were considered exploratory. In the future, on superceding IC chips, some of these modules on the CSP1009 will be required to operate with a power supply voltage of 2.8V. While testing this chip, it was desired to find out what modules may have to be redesigned and what modules would operate satisfactorily at this voltage.

3.8 AO4 Measurements

3.8.1 Gain

The circuits used to take the gain measurements of the AO4 amplifier are shown in Figures 3.2 and 3.3. Figure 3.2 shows the circuit without sampling. Figure 3.3 shows the circuit with sampling. The input used was a 1Vpp arbitrary waveform generated by the AP. The AO4 amplifier has only one gain setting and is a single-ended output amplifier. The desired gain of the AO4 was approximately 9dB. A 2.2kΩ resistor was placed between the AO4 pin and ground. The 2.2kΩ load is the typical load of the AO4. This load ensures that the maximum current drive of the amplifier is not exceeded. Measurements were taken at power supply voltages of 3.0V, 3.3V and 3.6V. The analog inputs, AI6P and AI6N are used for these tests. They were routed to the input of the AO4

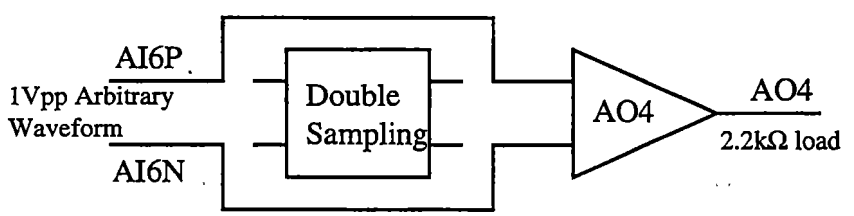


Figure 3.2: Circuit used for AO4 Gain Measurements (no sampling)

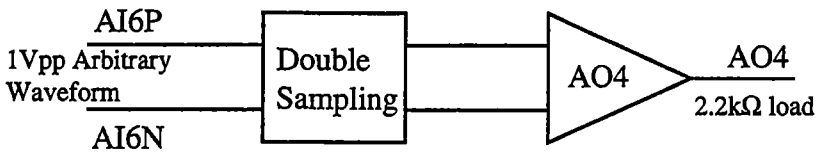


Figure 3.3: Circuit used for AO4 gain measurements (sampling)

amplifier. The gain of the amplifier was calculated using Equation 3.2.

3.9 Bandgap Voltage Reference Measurements

The two tests used to characterize the bandgap reference have some common points that will be discussed here. The temperature was controlled using the Temptronic machine. This machine has a nozzle attached to the end of an arm. This arm carries the temperature-controlled air and the nozzle fits down over the device under test. The temperature recorded was the temperature at the output of the nozzle, which would be the package temperature of the CSP1009. To insure proper chip temperature, the chip was allowed a five-minute soaking time before the voltage was recorded.

3.9.1 Reference Voltage vs. Temperature

The voltage reference (VREF) is derived from the bandgap voltage reference. This voltage is tied to the VREF pin and has a nominal value of approximately 1V. This test was accomplished by monitoring the VREF pin, as the temperature was varied from -20°C to 80°C in increments of 20°C. This temperature range was chosen to verify the operation from the extreme cold to the extreme hot temperature conditions that may be

encountered in the actual operation of the system. Data were taken at power supply voltages of 2.7V, 3.0V, 3.3V and 3.7V.

3.9.2 Reference Voltage vs. Supply Voltage at Temperatures of -20 °C and 0 °C

This test was accomplished by monitoring the VREF pin as the power supply voltage was varied from 3V down to 1V. This test was done at two temperatures, -20°C and 0°C. The -20°C temperature was chosen as a worst-case temperature for this test. This was considered the lowest temperature in which this system would be used. The 0°C temperature was chosen as a more realistic low temperature for the device. The reference voltage stayed relatively constant before sharply dropping off. The power supply voltage at which the bandgap reference drops out of regulation was the main interest of this test. To clarify this, a plot of the resulting data are shown in Figure 3.4 with the point of interest marked.

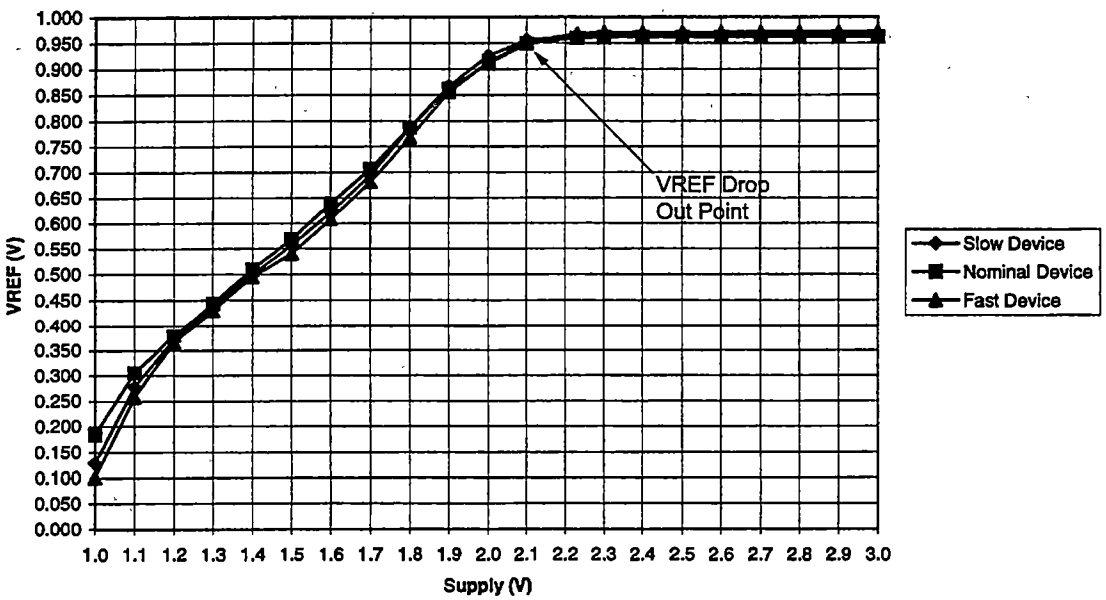


Figure 3.4: VREF vs. Power Supply Voltage with Drop Out Point Indicated

3.10 Charge Pump Measurements

3.10.1 Current Levels

In this test, the current levels of the charge pump were compared to the desired design values. To accomplish this test, the charge pump was placed into a test mode by the software. This caused the charge pump to ignore the output of the phase detector and simply source or sink the programmed current. The circuit used to measure the currents is shown in Figure 3.5.

The charge pump can be programmed for an initial current level (CPI), the number of reference clock periods to maintain this initial current (PDCNT), and a final current level (CPF). The PDCNT has a maximum setting of 5 bits (32 periods). The clock is derived from the divide-by-(R+1) counter. The programmable current values, for CPI and CPF, are shown in Table 3.3. Also shown are the binary settings for obtaining a specific amount of current. The desired amount of current for CPI is programmed by loading the binary number into bits [7–5] of the synthesizer control register. Loading bits [10–8] of this register sets the CPF current. Finally, loading bits [4–0] of this register sets PDCNT. Measurements were taken at power supply voltages of 2.8V and 3.3V.

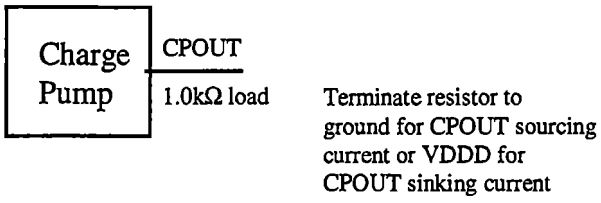


Figure 3.5: Charge Pump Test Setup

Table 3.3: Charge Pump Control with Currents

Binary Settings [2:0]	Current (μA)
000	175
001	250
010	350
011	500
100	700
101	1000
110	1400
111	2000

A 1kΩ resistor was placed at the charge pump output (CPOUT) and, depending on whether it was sourcing or sinking current, the resistor would be tied to ground or VDDD. The 1kΩ load was selected to give proper measurement resolution without creating a large voltage at the output of the charge pump. The charge pump current ranged from 100μA to 2000μA. Therefore, the voltage across the 1kΩ resistor would range from 0.1V to 2V. The sourcing or sinking modes were selected by setting bit [14]

(CPOL) to a 1 for sourcing, or to a 0 for sinking. The charge pump's current can be calculated by measuring the voltage across the 1kΩ resistor.

3.11 Current Consumption Measurements

The individual blocks on the chip were tested for worst-case current consumption. The speaker and line drivers have separate power supplies, VDDS and VDDL, which were monitored for the current measurements. The PGA, PGMO, and the analog to digital (ADC) and digital to analog (DAC) converters (together they are referred to as the CODEC) use the VDDA supply. This supply was also monitored during the current measurements. Since the value of the largest amount of current supplied to the CSP1009 was desired, the front-end amplifiers (PGA and PGMO) were set to their maximum gains. The input signal was set to ensure that the CODEC saw a full scale input. However, the gains of the output amplifiers (SPKR and LNDRV) were set to drive the maximum signal without noticeable distortion. The routing was set to emulate normal operation. If someone were talking on the telephone, the "receive path" is the signal flow from the telephone line to his/her ear. The "transmit path" is the signal flow from the mouthpiece to the telephone line. Figure 3.6 shows the circuit used to determine the current consumption of the PGA and the SPKR. Figure 3.7 shows the circuit used to determine the current consumption of the PGMO, LDRV1, and LDRV2. Finally, Figure 3.8 shows the circuit used to determine the current consumption of the AO4 amplifier. Some of the currents could not be measured directly. These had to be calculated knowing the current consumed by another block that was operating at the same time.

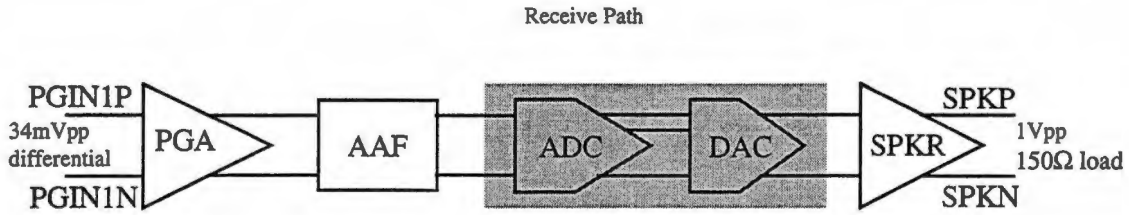


Figure 3.6: Circuit used to determine current consumption of PGA and SPKDRV

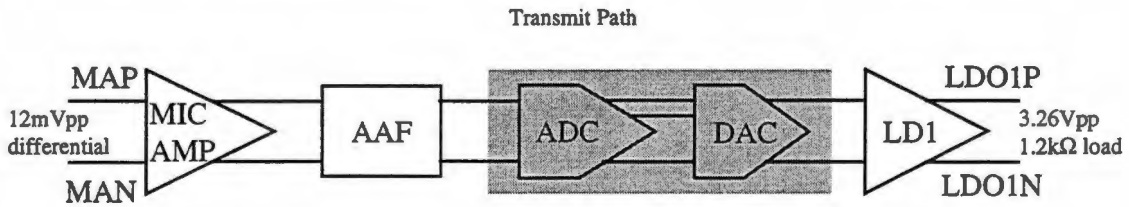


Figure 3.7: Circuit used to determine current consumption of PGMO, LNDRV1 and LNDRV2

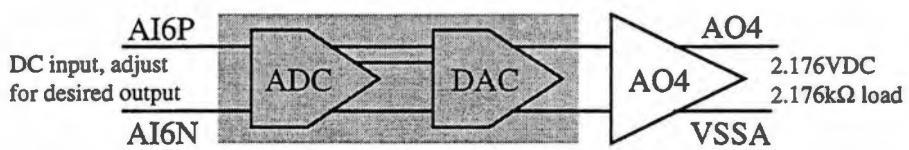


Figure 3.8: Circuit used to determine current consumption of AO4

3.12 Programmable Gain Amplifiers

The remainder of this chapter pertains to the four programmable gain amplifiers that were tested. For each amplifier, three attributes were characterized: gain, PSRR, and THD. Many of the circuit setup issues are the same for all three of the measurements.

Therefore, the first paragraph in each section will contain the common points. The subsections will contain points that are specific to that particular test.

3.13 Line Driver Amplifier Measurements

The gain, PSRR, and THD, of the Line Driver Amplifier (LDRV) were measured with differential and single ended outputs. The CSP1009 contains two identical line drivers, but only LDRV1 was tested. LNDV1 will be referred to as LDRV in this thesis. The measurements were done on all three-device types: fast, nominal and slow. The LNDVamplifier has 2 gain settings, 6dB and 12dB. The gains were selected by setting the CLINE bit to either 0 or 1. The CLINE bit is bit number 14 in the CODEC control register. The measurements include both gain settings, CLINE = 0 and CLINE = 1. The circuit used to conduct the measurements on the amplifier with a differential output is shown in Figure 3.9. The circuit used for the single-ended output measurements is shown in Figure 3.10. The 1200Ω and 600Ω loads shown in these circuits represent the actual loads seen by the amplifier when connected to the line matching transformer. The figures show the circuits with no sampling but measurements were done for the sampling case as well.

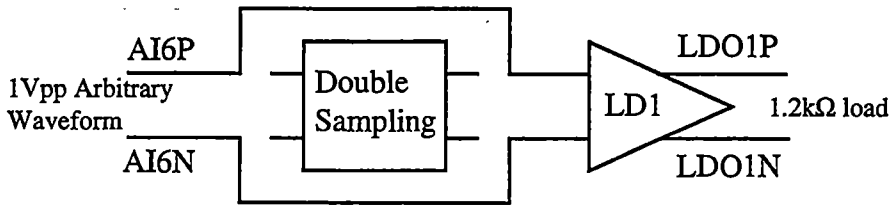


Figure 3.9: Circuit used for LDRV Measurements (no sampling)

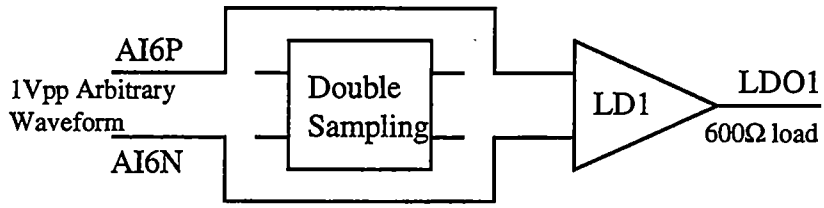


Figure 3.10: Circuit used for LDRV, Single Ended Measurements (no sampling)

3.13.1 Gain

The gain was measured at power supply voltages of 3.0V, 3.3V, and 3.6V for the differential case. The gain, for the single-ended case, was measured at the 3.3V supply voltage only. The single-ended case was tested at only one supply voltage because if the differential gains were correct then single-ended gains would also be correct. The one trial was done to verify and document this fact. The input (AI6P and AI6N) was a 1Vpp arbitrary waveform superimposed on a 0.5VDC level for biasing. The gain of the amplifier was calculated using Equation 3.2 in the Amplifier Measurement section.

3.13.2 PSRR

The PSRR of the LNDV was measured at power supply voltages of 2.8V and 3.3V for both the differential and single-ended configurations. The input (AI6P and AI6N) was connected to a 0.5VDC level for biasing. The PSRR was determined by modulating the power supply voltage with a 0.5Vpp arbitrary waveform for the differential case. For the single ended case, a 0.1Vpp arbitrary waveform was used to modulate the power supply voltage. The PSRR of the amplifier was calculated using Equation 3.4.

3.13.3 THD

The THD of the LNDV was measured at power supply voltages of 2.8V and 3.3V for both the differential and single-ended configurations. The input (AI6P and AI6N) was a sinusoid superimposed on a 0.5VDC level for biasing.

3.14 Programmable Gain Amplifier Measurements

The CSP1009 contains two identical programmable gain amplifiers, but only PGA1 was tested. PGA1 it will be referred to as PGA in this thesis. Since the outputs of the PGA cannot be accessed, it was routed through the speaker amplifier. The gain of the speaker amplifier was set to 0dB with a differential output configuration. Figure 3.11 shows the circuit used to gather the data for the amplifier. The input (PGIN1P and PGIN1N) of the amplifier must be biased with a voltage equal to VREF or approximately 1V. Therefore, each of the inputs discussed is superimposed onto a 1VDC level. The

figure shows the circuits with no sampling, but measurements were done for the sampling case as well.

3.14.1 Gain

The gain was measured at power supply voltages of 3.0V, 3.3V, and 3.6V. The gain of the PGA was measured at all possible programmed levels. The possible gain settings range from 0dB to 28dB in increments of 2dB, as shown in Table 3.4.

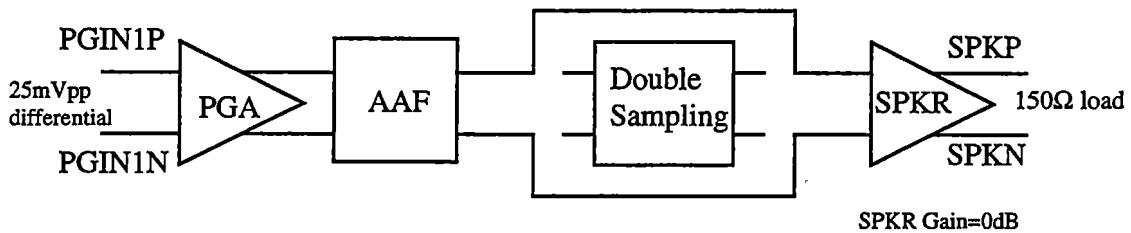


Figure 3.11: Circuit used for PGA Measurements

Table 3.4: Programmable Gain Amplifier Control Settings with Gain

Binary Settings [3:0]	Gain (dB)
0000	Off
0001	0
0010	2
0011	4
0100	6
0101	8
0110	10
0111	12
1000	14
1001	16

1010	18
1011	20
1100	22
1101	24
1110	26
1111	28

Also shown are the binary settings for obtaining a specific gain. The gain was programmed by loading the binary number into bits [7–4] of the CODEC control register. The input (PGIN1P and PGIN1N) was a 25mVpp arbitrary waveform. The amplitude of this signal was chosen to allow all of the gain settings to be tested without distorting (clipping) the output waveform. The gain of the amplifier was calculated using Equation 3.2 in the Amplifier Measurements section.

3.14.2 PSRR

Initially, the PSRR of the PGA was to be measured at power supply voltages of 2.8V and 3.3V. However, the results appeared erroneous at lower power supply voltages (2.7V to 3.0V). This error is discussed in Chapter 4. For these measurements, the power supply voltage for the slow and fast devices were raised to 3.1V and 3.0V for the nominal device. The PSRR was measured at three gain levels for completeness, 0dB, 14dB, and 28dB. The input (PGIN1P and PGIN1N) was only connected to a 1VDC level for biasing purposes. The PSRR was found by modulating the power supply voltage with a 0.5Vpp arbitrary waveform. The PSRR of the amplifier was calculated using Equation 3.4 in the Amplifier Measurements section.

3.14.3 THD

The THD was measured at power supply voltages of 2.8V and 3.3V and at three gain settings for completeness, 0dB, 14dB and 28dB. The input (PGIN1P and PGIN1N) was a sinusoidal signal generated by the AP.

3.15 Programmable Gain Microphone Amplifier Measurements

Since the output of the PGMO cannot be accessed directly, it was routed through the speaker amplifier. The gain of the speaker amplifier was set to 0dB and the output configuration was differential. Figure 3.12 shows the circuit used to take the measurements of the amplifier. It shows the circuits with no sampling but measurements were done for the sampling case as well. The inputs of the PGMO are ac coupled using a capacitor and therefore do not require a biasing voltage.

3.15.1 Gain

The gain was measured at power supply voltages of 3.0V, 3.3V, and 3.6V. The gain of the PGMO was measured at all possible programmed levels. The possible gain settings were from 16dB to 44dB in increments of 2dB, as shown in Table 3.5. Also shown are the binary settings for obtaining a specific gain.

Loading the binary number into bits [11-8] of the CODEC control register programmed the gain. The input (MAP and MAN) was a 6mVpp arbitrary waveform. A 6mVpp signal was used to allow all of the gain settings to be tested without distorting the

output waveform. The gain of the amplifier was calculated using Equation 3.2 in the Amplifier Measurements section.

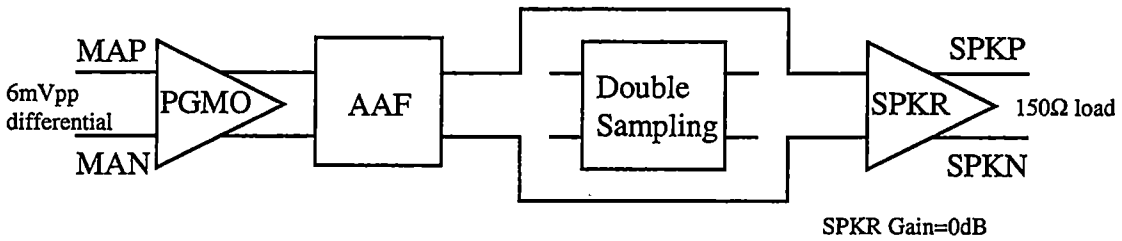


Figure 3.12: Circuit used for PGMO measurements

Table 3.5: Programmable Microphone Amplifier Control with Gain

Binary Settings [3:0]	Gain (dB)
0000	Off
0001	16
0010	18
0011	20
0100	22
0101	24
0110	26
0111	28
1000	30
1001	32
1010	34
1011	36

1100	38
1101	40
1110	42
1111	44

3.15.2 PSRR

Initially the PSRR of the PGA was to be measured at power supply voltages of 2.8V and 3.3V. However, the results appeared erroneous at lower power supply voltages (2.7V to 3.0V). This error is discussed in chapter 4. For these measurements, the power supply voltage for the slow and fast devices was raised to 3.1V and to 3.0V for the nominal device. The input (MAP and MAN) was left open. The PSRR was measured at three gain levels for completeness. These levels were 16dB, 30dB, and 44dB.

3.15.3 THD

The THD was measured at power supply voltages of 2.8V and 3.3V. The THD was measured at three gain settings for completeness, 16dB, 30dB, and 44dB. The input (MAP and MAN) was a sinusoidal signal generated by the AP.

3.16 Speaker Amplifier Measurements

The gain, PSRR, and THD, of the speaker amplifier (SPKR) were measured with differential and single-ended outputs. The circuit used to take the measurements on the

amplifier with a differential output is shown in Figure 3.13. The circuit used for the single-ended output measurements is shown in Figure 3.14.

3.16.1 Gain

The gain was measured at all possible programmed levels. It was also tested with two types of outputs, differential and single-ended. The gain settings for the differential output (without sampling case) range from -14dB to 14dB in increments of 2dB, as shown in Table 3.6. Also shown are the binary settings for obtaining a specific gain. The gain was programmed by loading the binary number into bits [3–0] of the CODEC control register. The differential output (with sampling case) was only tested at a power supply voltage of 3.3V with gain settings of –14dB, -8dB, 0dB, 8dB, and 14dB. The gain settings for the single-ended output (without sampling case) are from -20dB to 8dB in increments of 2dB. This is also shown in Table 3.6. The single ended output (with sampling case) was only tested at a power supply voltage of 3.3V with gain settings of -20dB, -10dB, 0dB, 2dB, and 8dB.

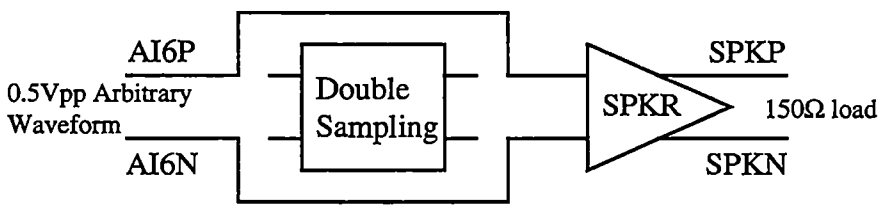


Figure 3.13: Circuit used for SPKR Measurements with Differential Outputs (no sampling)

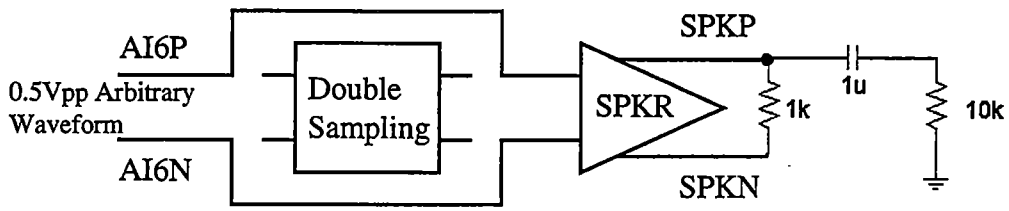


Figure 3.14: Circuit used for SPKR, Single Ended Measurements (no sampling)

Table 3.6: Programmable Speaker Amplifier Control with Gain

Binary Settings [3:0]	Differential Gain (dB)	Single Ended Gain (dB)
0000	Off	Off
0001	-14	-20
0010	-12	-18
0011	-10	-16
0100	-8	-14
0101	-6	-12
0110	-4	-10
0111	-2	-8
1000	0	-6
1001	2	-4
1010	4	-2
1011	6	0
1100	8	2
1101	10	4
1110	12	6
1111	14	8

3.16.2 PSRR

Initially the PSRR of the SPKR amplifier was to be measured at power supply voltages of 2.8V and 3.3V. However, the results appeared erroneous at lower power supply voltages (2.7V to 3.0V). This error is discussed in chapter 4. For these measurements, the power supply voltage for the slow and fast devices was raised to 3.1V for the differential case and 3.0V for the single-ended case. The PSRR was measured, for the differential output case, at gain settings of –14dB, 0dB, and 14dB. For the single-ended output case, the PSRR was measured at gains of –20dB, -6dB and 8dB. Both cases were also tested with the amplifier off, which indicates the path is open in front of the amplifier. The input (AI6P and AI6N) was connected to a 0.5VDC level for biasing purposes.

3.16.3 THD

The THD was measured at power supply voltages of 2.8V and 3.3V. The THD was measured at 2 gain settings, 8dB and 14dB for both the differential and single-ended output configurations. The input (AI6P and AI6N) was a sinusoidal signal, generated by the AP and superimposed on a 0.5VDC level for biasing

Chapter 4 Experimental Results

4.1 Introduction

This chapter contains a summary of the results from the measurements described in Chapter 3. The results are presented in table format and are accompanied by a brief description. They summarize the actual graphical data displayed in the Appendices. The results are classified into the three device types, slow, nominal and fast. Therefore, process variations are easily identified. Keep in mind, the measurements were done at different power supply voltages so that the values indicated in the results reflect those different voltages.

Some important notes about the PSRR measurements should be pointed out before proceeding. As noted in chapter 3, the PSRR measurements gave erroneous results at power supply voltages below 3.1V in some cases. Figure 4.1 illustrates this error. The "28dB of gain w/o sampling" case is approximately 20dB higher than the others and changes very little with frequency. Figure 4.2 shows the results for the same device where the only change is the increased supply voltage to 3.3V. Here the "28dB of gain w/o sampling" case is consistent with the others. It turns out that the 0.5Vpp signal used to modulate the supply voltage for the differential case, which was thought to be appropriate, was too large. This was especially true at the lower power supply voltages. A 0.1Vpp signal would have been more realistic.

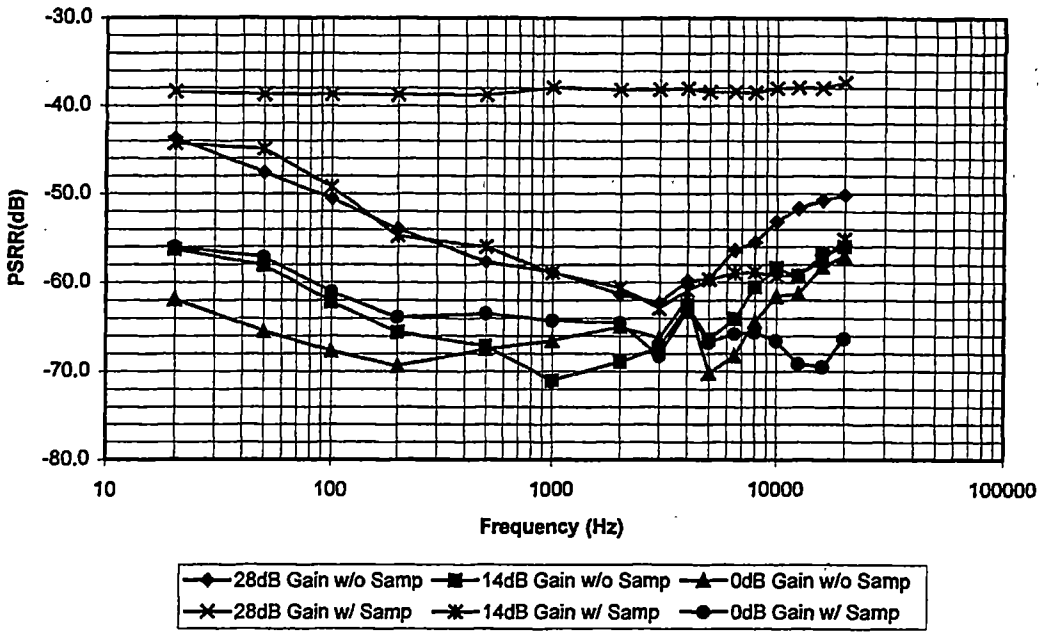


Figure 4.1: PSRR Showing Erroneous Data for PGA with 3.1V Supply

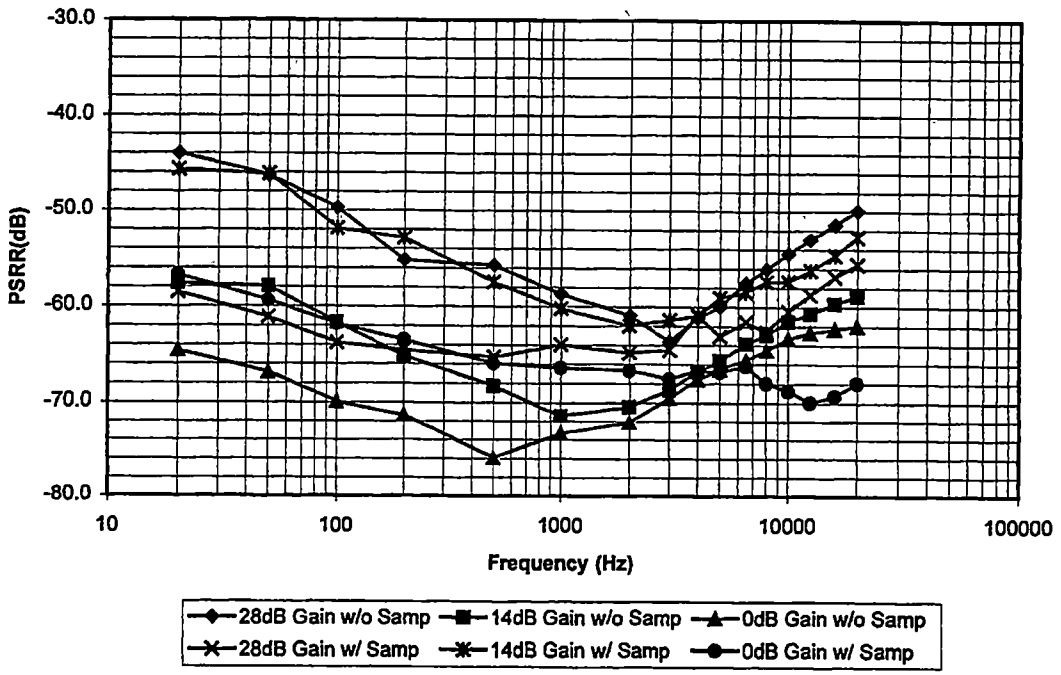


Figure 4.2: PSRR Showing Expected Data for the Same Device as in Figure 4.1 with 3.3V Supply

It was determined during the measurement process that enough of the PSRR data were legitimate to sufficiently characterize the device. Most of the actual PSRR data shown in the Appendix are what one would expect for this device. The expected values for these amplifiers come from past chips that contained the same or similar amplifiers. A small percentage of the results have the same or a similar problem as discussed above. These results were considered errors and were ignored. Most importantly, the error was not due to the CSP1009. It was an error in the measurement procedures.

4.2 AO4 Measurements

4.2.1 Gain

The results of the gain measurements for the AO4 amplifier are shown in Table 4.1. The results shown in the table reflect the minimum and maximum gains from the actual data shown in Appendix B. These extreme values occurred over the power supply changes. The gain values are taken at a mid-band frequency of 1kHz.

Table 4.1: AO4 Gain Measurement Results

	Measured Gain at 1kHz (dB)	
Type of Device	**Minimum**	**Maximum**
Slow	2.0	2.4
Nominal	2.0	2.6
Fast	2.1	2.5

4.3 Bandgap Reference Measurements

4.3.1 Reference Voltage vs. Temperature

Table 4.2 shows the results of the VREF voltage measurements as the temperature was varied from –20°C to 80°C in increments of 20°C. These results show the minimum and maximum voltages, over the entire temperature range and over power supply changes. These results are taken from the actual data shown in Appendix C.

4.3.2 Reference Voltage vs. Supply Voltage at -20 °C and 0 °C

Table 4.3 illustrates the results of the VREF voltage measurements as the temperature was kept constant at –20°C and the power supply voltage is varied from 3V down to 1V. Of particular interest in this test was the power supply voltage value at which the VREF voltage falls out of regulation. The results show the minimum and maximum voltages over changes in the supply voltage, before the drop off. The actual data are shown in Appendix B.

The same test was conducted with the temperature held constant at 0°C. The results are shown in Table 4.4. Also shown in Table 4.3 and Table 4.4 is the power supply voltage at which the VREF voltage drops off.

Table 4.2: VREF Voltage vs. Temperature Measurement Results

Type of Device	VREF (V) Over Temperature Range (-20°C to 80°C)	
	Minimum	Maximum
Slow	0.953	0.969
Nominal	0.947	0.966
Fast	0.958	0.975

Table 4.3: VREF Voltage vs. Supply Voltage Results at -20°C

Type of Device	VREF (V) Over Supply Voltage Range (3V down to 1V)		Supply Voltage at VREF Drop Off (V)
	Minimum	Maximum	
Slow	0.965	0.968	2.1
Nominal	0.964	0.965	2.1
Fast	0.973	0.974	2.1

Table 4.4: VREF Voltage vs. Supply Voltage Results at 0°C

Type of Device	VREF (V) Over Supply Voltage Range (3V down to 1V)		Supply Voltage at VREF Drop Off (V)
	Min	Max	
Slow	0.964	0.966	2.1
Nominal	0.964	0.965	2.1
Fast	0.973	0.974	2.1

4.4 Charge Pump Measurements

4.4.1 Current Levels

Table 4.5 shows the measured charge pump current levels when sourcing current. The results from when the charge pump is sinking current are displayed in Table 4.6. The "Programmed Current" was the amount of current expected. The results show the minimum and maximum current over changes in the power supply voltage. The data are taken from the actual results shown in Appendix D.

The data plots in Appendix D show other information, which is explained as follows. The charge pump can be programmed in the following manner; an initial current level (CPI), the number of system clock pulses for this initial current (PDCNT), and a final current level (CPF).

Table 4.5: Charge Pump Current Level when Sourcing Current

Programmed Current (μA)	Measured Current (μA)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
175	111	174	126	158	111	174
250	174	221	173	205	190	237
350	237	300	268	284	237	316
500	347	410	347	410	379	442
700	521	584	537	584	537	600
1000	742	805	742	804	805	868
1400	1073	1137	1105	1167	1121	1184
2000	1500	1610	1515	1594	1626	1720

Table 4.6: Charge Pump Current Level when Sinking Current

Programmed Current (μA)	Measured Current (μA)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
175	128	176	128	160	128	176
250	176	239	176	239	191	255
350	255	318	255	318	270	333
500	365	428	365	428	397	460
700	554	618	554	602	554	633
1000	775	839	775	823	823	902
1400	1123	1202	1138	1186	1138	1186
2000	1549	1675	1549	1628	1643	1675

The data plots show all of the possible current levels, most of which have CPI = CPF. However, two trials show CPI ≠ CPF with PDCNT set to maximum (32 periods) and 16 periods of the reference clock. These two trials were done to show how the charge pump operates normally and to verify this operational characteristic.

4.5 Current Consumption Measurements

Table 4.7 shows the current consumed by the individual modules while operating at the specified conditions. The table shows the minimum and maximum current over changes in the power supply voltage. These data are taken from the actual detailed results shown in Appendix E.

Two things should be noted about Table 4.7. First, for the slow and fast devices the LDRV1, LDRV2 and AO4 current measurements were done with the ADC and DAC (CODEC) operating but bypassed. The CODEC was found to cause distortion of the output waveform when the power supply voltage is below 3.0V for the fast device and below 2.9V for the slow device. Therefore, it was left operating, consuming power, but it was bypassed. That is, the signals were not being processed by the CODEC. Second, the last row of the table, "Channel Current", is a worst case total current during normal operation of the transmit and receive paths. It is the summation of CODEC, PGA, PGMO, LDRV1, and SPKR currents.

4.6 Programmable Gain Amplifiers

The remainder of this chapter pertains to the four programmable amplifiers. The results displayed for each of the amplifiers is from the three tests conducted: gain, PSRR, and THD. The tables showing the results of a specific test (gain, PSRR or THD), for all of the amplifiers have similar characteristics. The similar characteristics will be pointed out in this section. Any points that are particular to a specific amplifier will be presented in the sections that follow.

Table 4.7: Individual Block Current Consumption

Active Block	Measured Current (mA)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
CODEC (Analog ON)	1.19	1.23	1.22	1.26	1.28	1.31
PGA and AAF (28dB Gain)	0.60	0.63	0.59	0.60	0.64	0.68
PGMO and AAF (44dB Gain)	0.77	0.79	0.75	0.78	0.81	0.86
LNDRV1 (5.4dB Gain)	1.57	1.59	1.27	1.28	1.57	1.59
LNDRV2 (5.4 dB Gain)	1.58	1.60	1.35	1.36	1.56	1.57
SPKR (2dB)	2.93	3.26	3.04	3.06	3.06	3.18
AO4 (loaded – 1mA)	0.97	1.00	1.65	1.66	1.62	1.64
Total Current	9.61	10.10	9.87	10.00	10.54	10.83
Channel Current	7.06	7.50	6.87	6.98	7.36	7.62

The tables in the following sections reflect the minimum and maximum values of the gain, PSRR, and THD over changes in the power supply voltage. The gain values recorded in the tables are taken at a mid-band frequency of 1kHz. The "Programmed Gain" column indicates the gain settings and/or the expected gain at which the amplifiers were set during that particular test.

The PSRR results were obtained over a frequency range of 20Hz to 20kHz. The desired PSRR was specified at 50dB or greater at 0dB gain, for the differential configuration. For the single-ended configuration, the PSRR was specified at 25dB or greater.

The THD results are over a frequency range of 20Hz to 4kHz. The desired THD was specified at 0.03% for both configurations. This specification is valid when the output double sampling is disabled. The output sampling contributes to the THD. Therefore, the measurement would not be a true reflection of the amplifier with this sampling employed.

4.7 Line Driver Amplifier Measurements

The actual data for the line driver are displayed in Appendix F. Results from both output configurations, differential and single-ended, are illustrated.

4.7.1 Gain

The results of the LNDV amplifier's gain measurements are shown in Table 4.8.

4.7.2 PSRR

The results of the LNDV amplifier's PSRR measurements are displayed in Table 4.9.

4.7.3 THD

Table 4.10 illustrates the results of the LNDV amplifier's THD measurements. The maximum values indicated are with the output sampling turned on, see the results in Appendix E.

Table 4.8: Comparison of LNDRV Programmed Gain and Measured Gain

Programmed Gain (dB)	Measured Gain at 1kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
Differential						
CLINE = 0 (6dB)	5.2	5.4	5.2	5.5	5.3	5.5
CLINE = 1 (12dB)	10.3	10.5	10.2	10.5	10.2	10.4
Single Ended						
CLINE = 0 (0dB)	-0.8	-0.1	-0.8	0.1	-0.8	0.0
CLINE = 1 (6dB)	3.7	3.9	3.6	3.8	3.6	4.0

Table 4.9: Results of LNDRV PSRR Measurements

Programmed Gain (dB)	Measured PSRR up to 20kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
Differential						
CLINE = 0 (6dB)	53.1	76.1	50.7	76.7	51.1	74.7
CLINE = 1 (12dB)	47.4	66.7	47.2	64.7	47.7	64.5
Single Ended						
CLINE = 0 (0dB)	31.2	49.1	30.4	59.1	26.4	50.5
CLINE = 1 (6dB)	23.6	35.6	24.9	58.8	24.2	35.4

Table 4.10: Results of LNDRV THD Measurements

Programmed Gain (dB)	Measured THD up to a 4kHz Fundamental(%)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
Differential						
CLINE = 0 (6dB)	0.03	1.5	0.03	1.5	0.04	1.5
CLINE = 1 (12dB)	0.05	1.5	0.05	1.5	0.07	1.5
Single Ended						
CLINE = 0 (0dB)	0.3	1.6	0.15	1.6	0.2	1.6
CLINE = 1 (6dB)	0.5	1.9	0.26	1.8	0.4	1.8

4.8 Programmable Gain Amplifier Measurements

The actual data for the programmable gain amplifier are displayed in Appendix G.

4.8.1 Gain

The results of the PGA amplifier's gain measurements are shown in Table 4.11.

4.8.2 PSRR

The results of the PGA amplifier's PSRR measurements are shown in Table 4.12.

4.8.3 THD

The results of the PGA amplifier's THD measurements are shown in Table 4.13.

Table 4.11: Comparison of PGA Programmed Gain and Measured Gain

Programmed Gain (dB)	Measured Gain at 1kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
0	-0.7	-0.3	-0.7	-0.2	-0.7	-0.5
2	2.3	*	2.3	*	2.1	*
4	3.3	3.6	3.3	3.7	3.2	3.5
6	6.3	*	6.4	*	6.1	*
8	7.9	*	8.0	*	7.7	*
10	10.2	*	10.3	*	9.9	10.0
12	11.6	12.0	11.6	12.1	11.5	11.7
14	14.0	14.1	14.2	*	13.8	13.9
16	15.9	*	16.1	*	15.7	*
18	18.0	*	18.1	*	17.8	*
20	19.7	20.0	19.6	20.1	19.5	19.8
22	22.0	*	22.1	*	21.8	*
24	23.9	24.0	24.1	*	23.7	23.8
26	25.9	26.0	26.1	*	25.7	25.8
28	27.7	27.9	27.7	28.1	27.5	27.8

* Indicates that the value is the same as the "Min" value.

Table 4.12: Results of the PGA PSRR Measurements

Programmed Gain (dB)	Measured PSRR up to 20kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
0	56.0	75.9	48.6	77.5	54.2	72.1
14	44.3	71.4	35.3	70.6	46.7	70.9
28	43.7	65.3	44.3	71.4	56.0	75.9

Table 4.13: Results of the PGA THD Measurements

Programmed Gain (dB)	Measured THD up to a 4kHz Fundamental (%)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
0	0.03	0.04	0.03	0.04	0.03	0.04
14	0.04	0.05	0.04	0.06	0.04	0.06
28	0.12	0.19	0.13	0.22	0.11	0.20

4.9 Programmable Gain Microphone Amplifier Measurements

The actual data for the programmable gain microphone is displayed in Appendix H.

4.9.1 Gain

Table 4.14 displays the results of the PGMO amplifier's gain measurements.

4.9.2 PSRR

The results of the PGMO amplifier's PSRR measurements are shown in Table 4.15.

4.9.3 THD

Table 4.16 shows the results of the PGMO amplifier's THD measurements.

Table 4.14: Comparison of PGMO Programmed Gain and Measured Gain

Programmed Gain (dB)	Measured Gain at 1kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
16	16.0	16.1	15.9	16.2	15.8	16.1
18	18.2	*	18.1	18.2	18.1	18.2
20	20.0	20.1	19.9	20.1	19.8	20.0
22	22.2	*	22.0	22.2	22.1	*
24	24.0	*	23.8	24.0	23.9	24.0
26	26.2	*	25.8	26.1	26.1	*
28	27.9	28.0	27.8	28.0	27.7	28.0
30	30.1	30.2	30.1	*	30.0	*
32	32.0	*	32.0	*	31.9	*
34	34.1	*	34.0	34.1	34.0	*
36	35.8	36.0	35.7	36.0	35.7	35.9
38	38.1	*	38.0	38.1	38.0	*
40	40.0	*	39.9	40.0	39.8	39.9
42	42.2	*	42.1	42.2	42.0	42.1
44	43.8	44.1	43.7	44.1	43.7	44.0

* Indicates that the value is the same as the "Min" value.

Table 4.15: Results of PGMO PSRR Measurements

Programmed Gain (dB)	Measured PSRR up to 20kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
16	53.5	78.8	52.7	77.9	51.0	72.0
30	41.9	73.6	41.1	65.9	40.1	70.8
44	28.6	62.0	27.6	47.8	28.0	69.3

Table 4.16: Results of PGMO THD Measurements

Programmed Gain (dB)	Measured THD up to a 4kHz Fundamental (%)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
16	0.04	0.06	0.05	0.07	0.04	0.06
30	0.14	0.20	0.17	0.27	0.15	0.24
44	0.70	1.0	0.80	1.24	0.73	1.13

4.10 Speaker Amplifier Measurements

The actual data for the speaker amplifier is shown in Appendix I.

4.10.1 Gain

Table 4.17 indicates the results of the SPKR amplifier's gain measurements with a differential output configuration. Table 4.18 shows the results of the SPKR amplifier's gain measurements with a single-ended output configuration.

4.10.2 PSRR

The results of the SPKR amplifier's PSRR measurements are shown in Table 4.19.

4.10.3 THD

The results of the SPKR amplifier's THD measurements are displayed in Table 4.20. The maximum values shown are with the output double sampling turned on.

Table 4.17: Comparison of SPKR Programmed Gain and Measured Gain (differential output)

Programmed Gain (dB)	Measured Gain at 1kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
-14	-14.1	-13.7	-14.1	-13.9	-14.0	-13.8
-12	-11.7	*	-11.8	*	-11.8	*
-10	-9.7	*	-9.9	-9.8	-9.8	*
-8	-8.1	-7.9	-7.9	*	-8.1	-7.9
-6	-5.9	*	-5.9	*	-5.9	*
-4	-3.9	*	-3.8	*	-3.9	-3.8
-2	-1.9	*	-1.8	-1.9	-1.9	*
0	-0.1	0.1	0.2	*	-0.1	0.1
2	2.1	*	2.2	*	2.1	*
4	4.1	4.2	4.2	*	4.1	*
6	6.1	*	6.2	*	6.1	*
8	7.9	8.2	8.0	8.2	7.9	8.2
10	10.2	*	10.2	*	10.1	10.2
12	12.2	12.3	12.2	12.3	12.2	*
14	13.9	14.3	14.0	14.2	14.0	14.2

* Indicates that the value is the same as the "Min" value.

Table 4.18: Comparison of SPKR Programmed Gain and Measured Gain (single ended output)

Programmed Gain (dB)	Measured Gain at 1kHz (dB)					
	Slow		Nominal		Fast	
	w/o Samp.	w/ Samp.	w/o Samp.	w/ Samp.	w/o Samp.	w/ Samp.
-20	-19.8	-20.0	-19.9	-20.1	-19.8	-20.0
-18	-17.7	N/A	-17.9	N/A	-17.7	N/A
-16	-15.7	N/A	-15.9	N/A	-15.8	N/A
-14	-13.9	N/A	-13.9	N/A	-13.9	N/A
-12	-11.9	N/A	-11.9	N/A	-11.9	N/A
-10	-9.9	-10.1	-9.9	-10.1	-9.8	-10.0
-8	7.9	N/A	7.9	N/A	7.8	N/A
-6	-5.9	N/A	-5.9	N/A	-5.9	N/A
-4	-3.9	-4.1	-3.9	-4.1	-3.9	-4.1
-2	-1.9	N/A	-1.8	N/A	-1.8	N/A
0	0.1	N/A	0.1	N/A	0.1	N/A
2	2.2	2.0	2.2	2.0	2.2	2.0
4	4.2	N/A	4.2	N/A	4.2	N/A
6	6.3	N/A	6.2	N/A	6.3	N/A
8	8.3	8.0	8.2	8.0	8.3	8.0

N/A indicates that gain setting was not tested.

Table 4.19: Results of SPKR PSRR Measurements

Programmed Gain (dB)	Measured PSRR up to 20kHz (dB)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
Differential						
Off	57.9	82.0	51.1	74.9	58.2	73.0
-14	58.9	81.0	52.2	73.7	58.3	71.2
0	58.0	79.3	48.2	71.7	57.6	71.6
14	47.8	69.1	39.1	67.5	47.7	66.5
Single Ended						
Off	28.8	59.5	27.8	58.2	29.5	58.0
-20	27.9	57.9	27.0	59.9	28.7	58.2
-6	28.7	58.8	27.8	58.8	29.5	57.7
8	25.7	50.6	24.8	52.9	26.5	51.1

Table 4.20: Results of the SPKR THD Measurements

Programmed Gain (dB)	Measured THD up to a 4kHz Fundamental (%)					
	Slow		Nominal		Fast	
	Min	Max	Min	Max	Min	Max
Differential						
8	0.02	1.5	0.02	1.5	0.02	1.5
14	0.06	1.5	0.07	1.5	0.06	1.5
Single Ended						
8	0.1	1.5	0.11	1.5	0.1	1.5
14	0.13	1.5	0.16	1.5	0.11	1.5

Chapter 5 Interpretation of the Results and Conclusions

5.1 Introduction

In this chapter, the results will be discussed and any errors that were found during the measurement process will be noted. In addition, problems with the CSP1009 that were found during the characterization process will be discussed. Finally, some recommendations and conclusions will be offered.

5.2 AO4 Results

The gain of the AO4 was measured to be in the range of 2dB - 3dB. The desired value of this gain was approximately 9.2dB. This is a major difference and needs to be discussed. The following illustration is given to explain this problem. However, the signals shown are not the actual signals used in the measurements. Figure 5.1 shows the circuit setup to measure the gain of the AO4 amplifier. The inputs, AI6P and AI6N were driven differentially. The output was single-ended. The inputs are shown in Figure 5.2 (a) and (b). The figure displays the signals applied to AI6P and AI6N. The actual differential input is shown in Figure 5.3 along with the single-ended output of the amplifier.

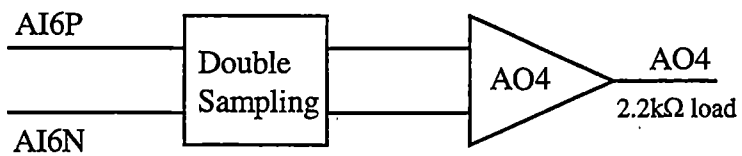


Figure 5.1: Circuit used to take AO4 Gain Measurements

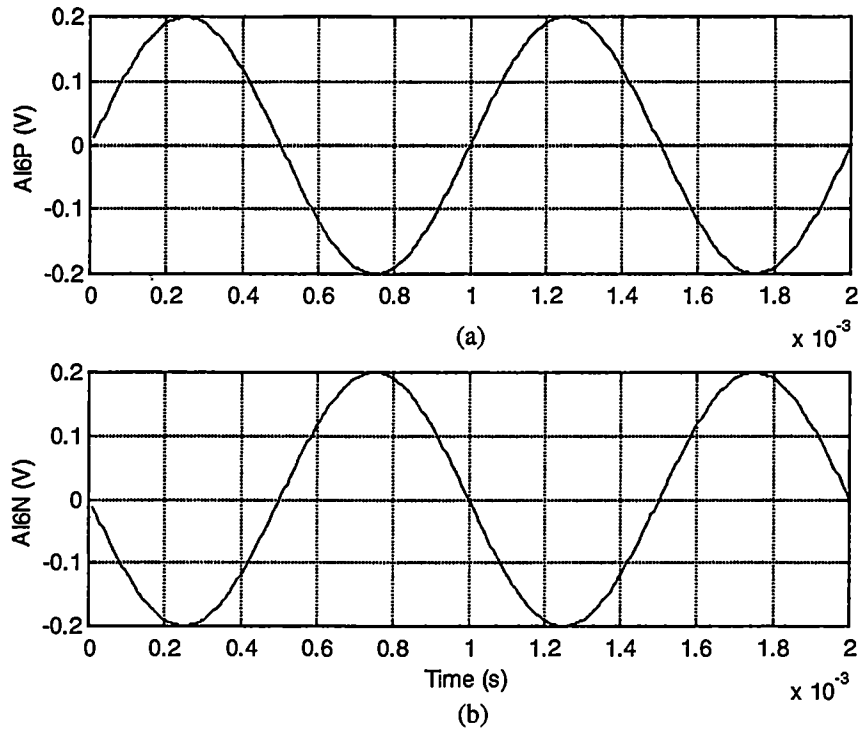


Figure 5.2: Each Leg of the Differential Input Applied to AI6P (a) and AI6N (b)

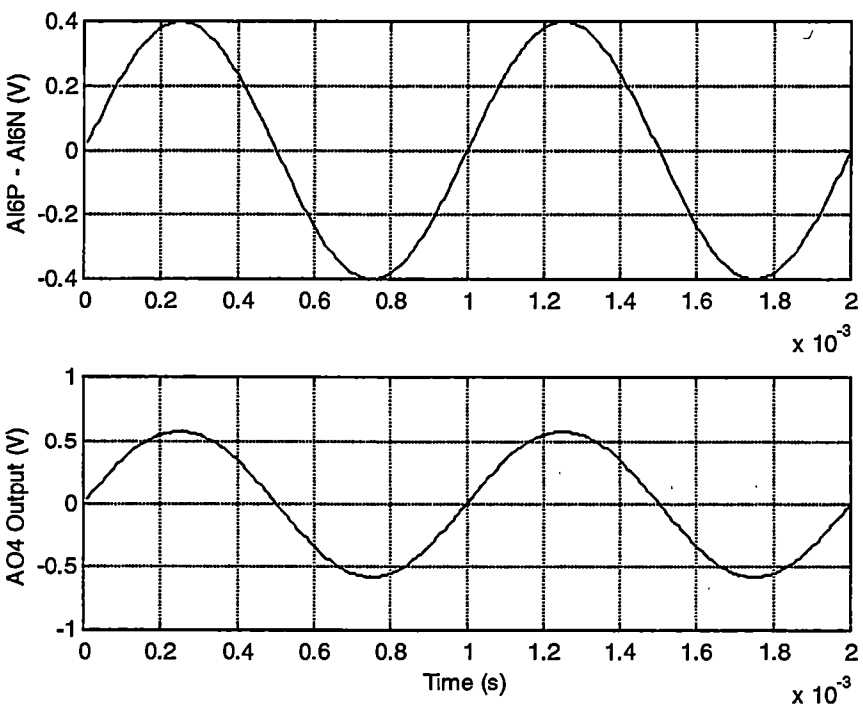


Figure 5.3: The Differential Input and the Single-Ended Output of the AO4 Amplifier

Referring to the AO4 amplifiers simplified circuit diagram shown in Figure 5.4; the output was found and plotted using the following equation:

$$AO4\_Output = Vin * \left(1 + \frac{Rf}{R1}\right) = 0.4Vpp * \left(1 + \frac{7.6k}{4k}\right) = 1.16Vpp \quad (5.1)$$

where

$$\left(1 + \frac{7.6k}{4k}\right) = 2.9\,{}^{V}\!/_{V}, \quad (5.2)$$

is the non-inverting voltage gain of the amplifier. Equation 5.1 is calculated using Vin=0.4Vpp, which is ½ of the differential input shown previously or the single-ended input. This gain can then be converted to dB, which is approximately 9.25dB. However, if the differential-in, single-ended-out voltage gain is calculated using Equation 5.2 it is one half the gain calculated in 5.2 or 6dB less.

$$\frac{Vo}{Vin_{diff}} = \frac{1.16Vpp}{0.8Vpp} = 1.45\,{}^{V}\!/_{V} = 3.2dB \quad (5.3)$$

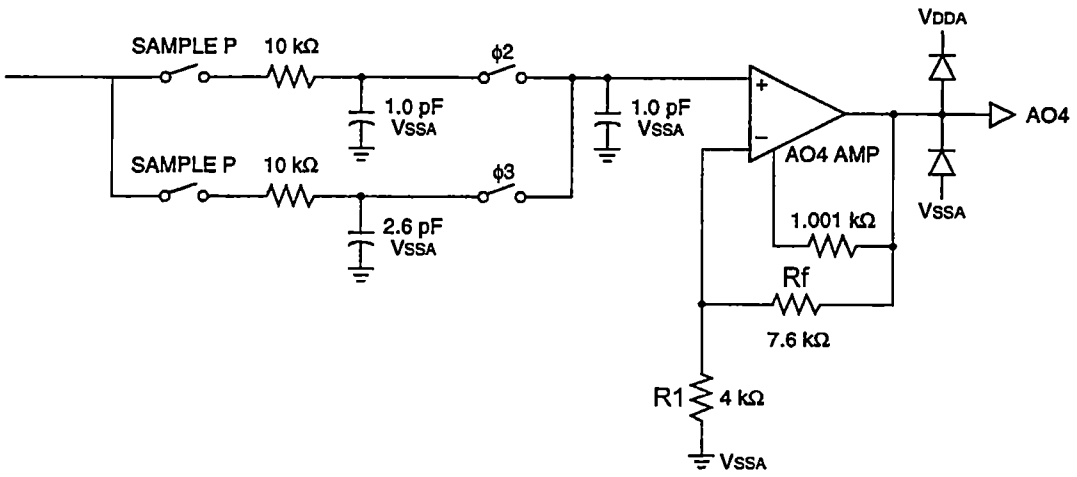


Figure 5.4: Simplified Block Diagram of the AO4 Amplifier

This example illustrates the fact that the differential-in, single-ended-out gain will be 6dB less than the single-ended-in, single-ended-out gain. This assumes the amplitude of the differential input is twice the amplitude of the single-ended input. This applies to all of the output amplifiers, AO4, SPKR and LNDV when measurements were done with single-ended outputs.

The gain of the AO4 amplifier was found to range from 2.0dB to 2.6dB. After taking into account the 6dB difference, the gain is approximately 10% less than the specified gain. However, this is sufficient since the amplifier is a general-purpose amplifier and this small discrepancy does not affect any operational detail.

5.3 Bandgap Reference

The voltage reference, VREF changed, at most, 2% over the temperature range. This says that the reference has a temperature coefficient (TC) of

$$TC = \frac{dV}{dT} = \frac{0.965V - 0.948V}{80^\circ C - (-20^\circ C)} = \frac{0.017}{100} = 0.17\,{}^{mV}/_{^\circ C}. \qquad (5.4)$$

This TC was adequate for this system. However, the voltage was designed to be 1V and turned out to be approximately 3% lower. Small errors in VREF are expected in the first prototype and can be corrected on later revisions.

The voltage reference was also tested to find the power supply voltage at which the reference drops out of regulation. This voltage was found to be approximately 2.1V. That is much less than the minimum power supply voltage of 3.0V and therefore adequate.

5.4 Charge Pump

The measured charge pump currents were approximately 25% lower than the desired values. This, however, was not a problem. The charge pump supplies current to a loop filter, which creates a voltage at the input of the VCO. The amount of current the charge pump can source or sink is set by software. Therefore, the important thing is that the magnitudes of the different current levels are known. This is important to the software engineer who is responsible for the setup of this module. They must know how they are affecting the VCO with a certain programmed amount of current. Figure 5.5 shows a portion of the charge pump results. The figure shows the actual magnitudes of each of the programmed levels. In addition, it shows that different levels can be programmed. The text in the figure shows what values were programmed.

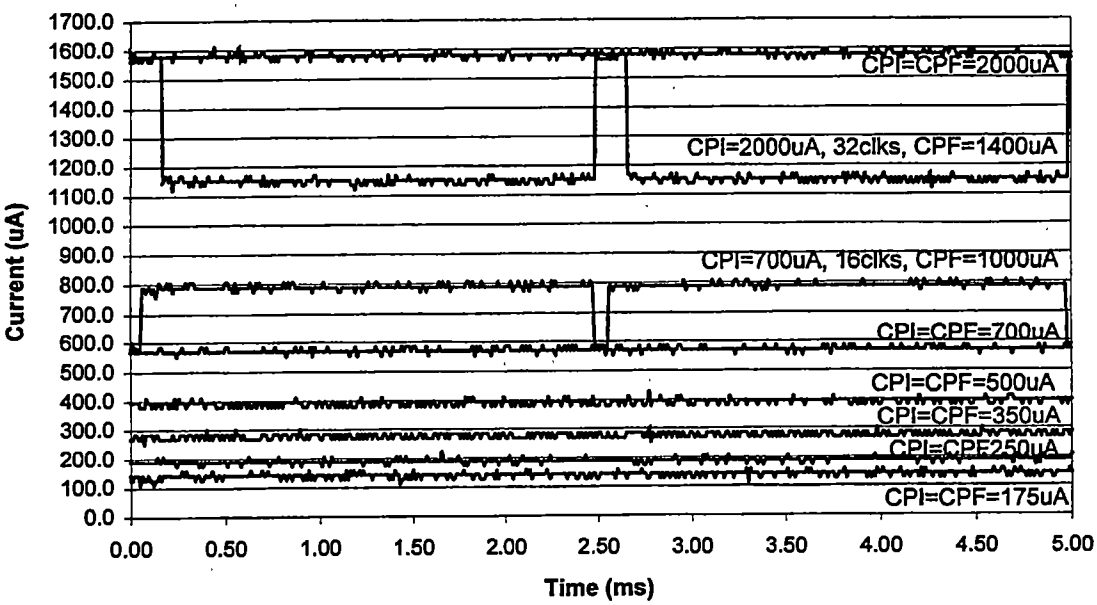


Figure 5.5: Results from the Charge Pump Sourcing Current Measurements

5.5 Current Consumption

Since the system the CSP1009 is designed for is powered by a battery, the current required by the chip is critical. The life of the battery is one of the major advertising issues for cordless telephones. Therefore, it was desired to monitor the current of the individual blocks and ultimately obtain a value for the maximum current (worst case) for the entire chip. The "Channel Current", from Table 4.7 reflects this value. It was approximately 7mA. A target value of 7mA was set for the chip. This target value is derived from past IC chips with similar characteristics. It is desired to have a maximum current measurement no greater than that of past systems.

5.6 Programmable Gain Amplifiers

The programmable amplifiers, LNDV, PGA, PGMO and SPKR all performed adequately, with the one exception being the gain of the LNDV amplifier, which will be discussed. They met all of the specifications set forth for gain, THD and PSRR. However, a few anomalies were found while characterizing these amplifiers. These anomalies will be discussed in the following sub-sections.

5.6.1 LNDV Gain

The line driver gain results were lower than expected. For the differential case, the gains were about 15% lower than expected. The single-ended results were about 35% lower than expected.

5.6.2 DAC Offset

While checking the maximum signal swing at the output of the LNDV amplifier it was noticed that the top of the output sinusoid clipped before the bottom, indicating some offset. Further investigation showed that the positive output of the LNDV, LNDOP clipped before the negative output, LNDON. The test setup is shown in Figure 5.6. The nominal device was used at a power supply voltage of 3.6V. The gain was set at the maximum, 10dB – 11dB. The inputs, AI6P and AI6N were left open and therefore the two outputs should be setting at an equal DC voltage. However, the outputs had a ΔV of +0.27VDC. To verify this, the SPKR amplifier was set to approximately the same gain as the LNDV of 10dB. This test circuit is shown in Figure 5.7. The offset observed there was +0.25VDC. The common factor in these two test setups was the CODEC. Other devices were tested to throw out the possibility of a bad device. The ΔV changed over the different process types, but was significant for all of the devices.

The next step was to bypass the CODEC and retest. With the CODEC bypassed, the outputs were approximately equal. With a sinusoid input, the top and bottom of the waveform clipped at nearly the same voltage.

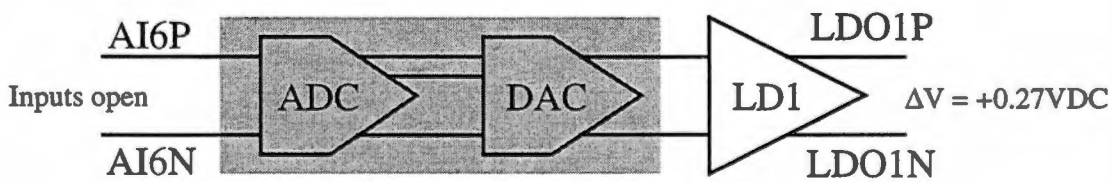


Figure 5.6: LNDV Setup During investigation of Offset

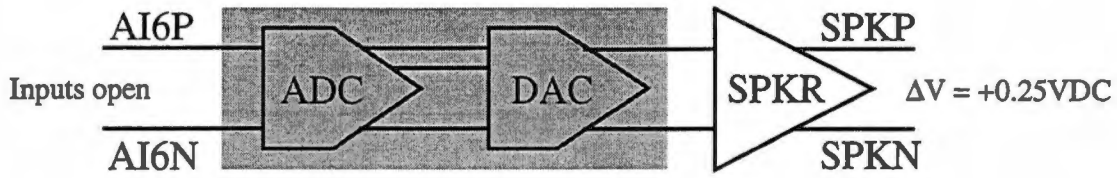


Figure 5.7: SPKR Setup during Investigation of Offset

This procedure indicated that the CODEC indeed had an offset. The course of action is not known, however the problem was being addressed.

5.6.3 PGA Feed-Through

All of the amplifiers in the CSP1009 have the capability of being disabled. This is accomplished by removing the power from the amplifier. While testing the "off" condition of the input amplifiers, PGA and PGMO, it was noticed that a signal was still getting through to the output of the LNDV and SPKR amplifiers. The current drawn from the analog supply was first monitored to verify that the amplifier was indeed powered down. The circuit was then examined to find what might be happening. Looking back at Figure 2.5 or Figure 2.6 one can see that even with the amplifiers powered down, a resistive path still exists from the input pins to the anti-aliasing filter. This path allowed the input of the PGA to be coupled to the output of the LNDV. This problem could easily be corrected by placing a MOSFET switch in the signal path of each channel.

5.6.4 Double Sampling Roll Off

The output amplifiers, AO4, LNDV and SPKR all have a double sampling network that smoothes out the output of the DAC before amplification. The network is shown is Figure 2.1. Upon completion of the SPKR amplifier characterization, it was noticed that the roll-off of the sampling network was actually in the voice band. Figure 5.6 shows the programmable gains of the SPKR amplifier without the double sampling employed. In addition, it shows the bandwidth of the amplifier is much greater than 20kHz, since no roll-off is seen. Figure 5.7 shows the some of the programmable gains, of the SPKR amplifier, with the double sampling employed. This figure shows the –3dB frequency of the sampling roll-off to be approximately 4kHz. This was viewed as a problem because it was rolling off in the voice band. Therefore, it was attenuating the upper frequencies of the voice band.

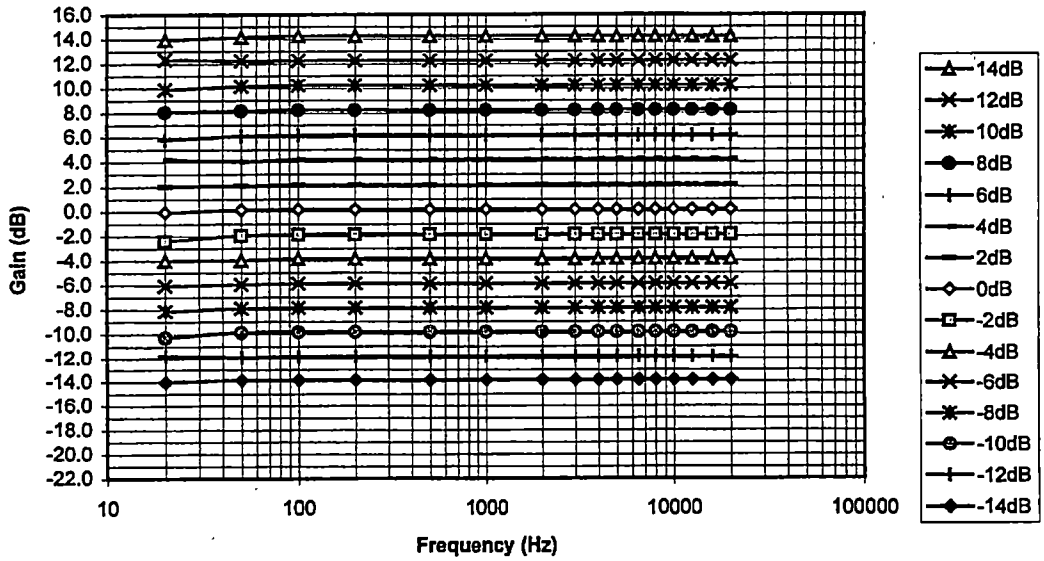


Figure 5.8: Speaker Amplifier Gain without Double Sampling Employed

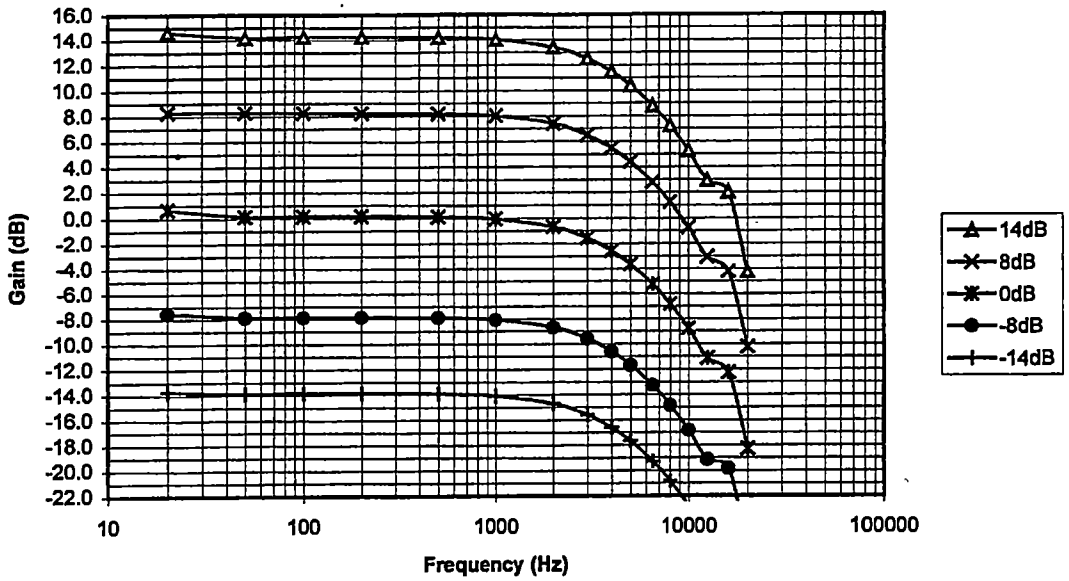


Figure 5.9: Speaker Amplifier with Double Sampling Employed

A solution for this problem was applied to a few of the prototypes. The "Silicon Surgery" Group at Lucent Technologies etched the top off some of the devices and modified the double sampling network. Figure 5.8 shows the SPKR amplifier gain with and without the "new" double sampling network employed. It shows the –3dB frequency has been pushed out to approximately 10kHz, thus outside of the voice band.

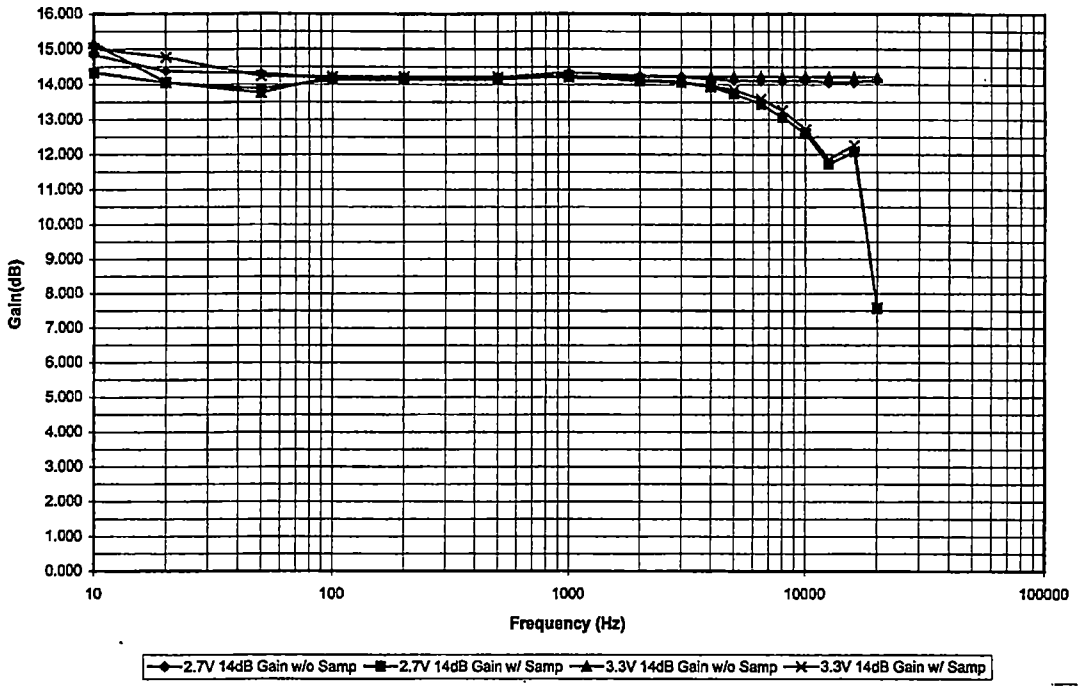


Figure 5.10: Speaker Amplifier Gain after Revision to Push Out Double Sampling Roll-off

5.7 Conclusions

The CSP1009 as a whole operated well, considering these measurements were done on the first prototype. Every module operated as it was intended to and most met specifications. The defects found were significant and should be addressed. However, none of the defects were operationally debilitating.

The measurement process was comprehensive and thorough. However, the PSRR measurements could be improved. PSRR measurements turned out to be quite difficult. This was due to the fact that the individual stages of the amplifier react differently to the power supply changes. In addition, PSRR was not well represented in the literature. This

leads to difficulty in interpreting the results. So, the Microelectronics Group at Lucent Technologies uses the PSRR results of past chips as a standard by which to compare the newer chips. If the results are comparable, they are considered viable.

When the PSRR tests began on this device, the appropriate amplitude of the modulating signal was uncertain. The amplitudes suggested really had no basis. The 0.5Vpp signal was eventually chosen in order to decrease the PSRR to a value where it could be measured. The noise floor of this device was approximately –75dB (with the CODEC operating). Therefore, the PSRR could not be measured using a modulating signal with an amplitude much less than 0.5Vpp. The signal at the output of the amplifier was lower than the noise floor. Therefore, a PSRR value could not be measured. It became obvious that this amplitude was too large because the supply voltage varied a great amount. However, the majority of the problems occurred when the supply voltage was less than 3.0V. For a supply voltage of 3.0V, the supply is actually 2.75V – 3.25V, well out of the range for the design of this device.

Another issue with the PSRR measurement was the use of the arbitrary waveform. The arbitrary waveform is characteristically much different from a pure, single frequency sine wave. It is suggested, from this experience, that the power supply voltage be modulated with a single frequency sine wave instead of the arbitrary waveform when taking PSRR measurements. The sine wave is a much more realistic power supply variance than the arbitrary waveform. That is, in reality the supply voltage will not encounter variances similar to the arbitrary waveform.

This thesis addressed the following issues in relation to the modules within the CSP1009; verified the functionality, tested to ensure that all of the specifications were met, identified the problems with the device, and determined a testing procedure to document the problems. In addition to these tasks, a characterization procedure was also developed. This was done in order to document the process. In an effort to minimize measurement time and simplify the characterization process, an automated testing procedure was also developed.

REFERENCES

Chapter 1

[FCC1] Federal Communications Commission, Title 47, Chapter I, Part 15, Subpart C, Section 15.233

J. E. Padgett, "Cordless Telephones: Present and Future", Proceedings of the National Electronics Conf., v 38 1984, Published by Professional Education Int. Inc., pp.151-156

[LUCENT1] Lucent Technologies Inc., "CSP1009 Communications Signal Processor (CSP)", April 1999

Lucent Technologies Inc., "Lucent Technologies Everest™ 900 MHz ISM Frequency-Hopping Spread Spectrum (FH/SS) Cordless Basic Phone Solution", January 1999

Chapter 2

[JOHNS&MARTIN1] D. A. Johns and K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997, pp. 353-359

Lucent Technologies Inc., "CSP1009 Communications Signal Processor (CSP)", April 1999

[DATEL1] DATEL, Data Acquisition and Conversion Handbook, Datel Eighth Printing, March 1987

A. P. Brokaw, "A Simple Three-Terminal IC Bandgap Reference", IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, Dec. 1974, pp. 388-393

Chapter 3

[PIERCE&PAULUS1] J. F. Pierce and T. J. Paulus, Applied Electronics, Bell & Howell Co., 1972, pp. 602

APPENDICES

APPENDIX A

AUDIO PRECISION VISUAL BASIC PROGRAMS

Speaker Gain Measurement Routine:

```
Sub Main

        ap_file_directory = "C:\files\Modified Devices"                    'Change directory for
different tests
        dsp_file_directory = "C:\ltdsp\r6_6_3\uhura\ai6tos~1"                    'Change
directory for different tests
        ascii_data_directory = "C:\files\Modified Devices\data"
        counter = 1

        ChDir ap_file_directory
        open_test = GetFilePath$("", "*.at2", "", "Select the file to copy AP settings from")
        AP.File.OpenTest(open_test)              'Change filename for different tests
        Call Setup_panels
        Call Setup_com_port
        Call Setup_PS

loop1:
        ChDir dsp_file_directory
        Select Case counter
                Case 1
                        Call Set_PS_2_7
                        Call PS_Output_on
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_f")
                        Wait 7
                Case 2
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_f")
                        Wait 7
                Case 3
                        Call Set_PS_3_3
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_f")
                        Wait 7
                Case 4
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_f")
                        Wait 7
                Case Else
                        MsgBox ("Invalid Case in Select", 0, "Error")
                        End
        End Select

        If counter = 1 Then
                MsgBox ("Connect AP's Probes to Input, AI6.  Click 'OK' when ready.", 0, "Yo!")
                AP.Sweep.Start
                MsgBox ("Connect AP's Probes to Output of SPKR.  Click 'OK' when ready.", 0,
"Yo!")
                End If

        AP.Sweep.Start

        If counter = 4 Then
```

```
            ChDir ap_file_directory
            new_test = GetFilePath$("", "*.at2", "", "Enter the NEW AP filename", 3)
            AP.File.SaveTestAs (new_test)
            ChDir ascii_data_directory
            new_data = GetFilePath$("", "*.adx", "", "Enter the NEW ASCII Data filename", 3)
            AP.File.ExportASCIIData(new_data)
            Call PS_Output_off
            End
        End If

        counter = counter + 1
        GoTo loop1


End Sub

Sub Setup_panels

        AP.Application.NewData
        AP.Application.Page = 1
        AP.Anlr.FuncFilterLP = 0
        AP.Application.Page = 2

End Sub                                 'Setup_panels

Sub Setup_com_port
        AP.CommA.CommPort = 1       'Select Comm Port
        AP.CommA.Settings = "9600,N,8,2"      'Set Comm Port settings baud rate ect.
        AP.CommA.RTSEnable = False
        AP.CommA.Handshaking = 0
        AP.CommA.OutBufferSize = 50 'Set Output buffer size
        AP.CommA.InBufferSize = 50            'Set Input buffer size

End Sub                                 'Setup_com_port

Sub Setup_PS
        AP.CommA.PortOpen = True              'Open Comm Port 1
        AP.CommA.Output = "SYST:REM"          'Send data
        AP.CommA.Output = Chr$(10)            'Send CR
        AP.CommA.Output = "*RST;*CLS"         'Send data
        AP.CommA.Output = Chr$(10)            'Send CR
        AP.CommA.PortOpen = False   'Close Comm Port
End Sub                         'Setup_PS

Sub Set_PS_2_7
        AP.CommA.PortOpen = True              'Open Comm Port 1
        AP.CommA.Output = "VOLT 2.7"          'Send data
        AP.CommA.Output = Chr$(10)            'Send CR
        AP.CommA.Output = "CURR 0.1"          'Send data
        AP.CommA.Output = Chr$(10)            'Send CR
        AP.CommA.PortOpen = False   'Close Comm Port
        Call PS_Beep
        Wait 2
```

```
        End Sub                         'Set_PS_2_7

Sub Set_PS_3_3
        AP.CommA.PortOpen = True        'Open Comm Port 1
        AP.CommA.Output = "VOLT 3.3"    'Send data
        AP.CommA.Output = Chr$(10)      'Send CR
        AP.CommA.Output = "CURR 0.1"    'Send data
        AP.CommA.Output = Chr$(10)      'Send CR
        AP.CommA.PortOpen = False   'Close Comm Port
        Call PS_Beep
        Wait 2                                          'Wait 2 seconds
End Sub                         'Set_PS_3_3

Sub PS_Beep
        AP.CommA.PortOpen = True        'Open Comm Port 1
        AP.CommA.Output = "SYST:BEEP"   'Send data
        AP.CommA.Output = Chr$(10)      'Send CR
        AP.CommA.PortOpen = False   'Close Comm Port
        Wait 2                                          'Wait 2 seconds
End Sub                         'PS_Beep

Sub PS_Output_on
        AP.CommA.PortOpen = True        'Open Comm Port 1
        AP.CommA.Output = "OUTP ON"             'Send data
        AP.CommA.Output = Chr$(10)      'Send CR
        AP.CommA.PortOpen = False   'Close Comm Port
        Wait 2
End Sub                         'PS_Output_on

Sub PS_Output_off
        AP.CommA.PortOpen = True        'Open Comm Port 1
        AP.CommA.Output = "OUTP OFF"            'Send data
        AP.CommA.Output = Chr$(10)      'Send CR
        AP.CommA.PortOpen = False   'Close Comm Port
End Sub                         'PS_Output_off
```

Speaker PSRR Measurement Routine:

```
Sub Main

        ap_file_directory = "C:\files\PSRR Measurements\SPKR"                    'Change
directory for different tests
        dsp_file_directory = "C:\ltdsp\r6_6_3\uhura\ai6tos~1"                    'Change
directory for different tests
        ascii_data_directory = "C:\files\PSRR Measurements\SPKR\data"
        counter = 1

        ChDir ap_file_directory
        open_test = GetFilePath$("", "*.at2", "", "Select the file to copy AP settings from")
        AP.File.OpenTest(open_test)              'Change filename for different tests
        Call Setup_panels

loop1:
        ChDir dsp_file_directory
        Select Case counter
                Case 1
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_f")
                        Wait 8
                Case 2
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_8")
                        Wait 6
                Case 3
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_1")
                        Wait 6
                Case 4
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_0")
                        Wait 6
                Case 5
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_f")
                        Wait 8
                Case 6
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_8")
                        Wait 6
                Case 7
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_1")
                        Wait 6
                Case 8
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_0")
                        Wait 6
                Case Else
                        MsgBox ("Invalid Case in Select", 0, "Error")
                        End
        End Select

        If counter = 1 Then
                MsgBox ("Connect AP's Probes to Supply Voltage.  Click 'OK' when ready.", 0,
"Yo!")
                AP.Sweep.Start
```

```
            MsgBox ("Connect AP's Probes to Output.  Click 'OK' when ready.", 0, "Yo!")
            End If

        AP.Sweep.Start

        If counter = 8 Then

            Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_8")
            Wait 6
            AP.Application.Page = 1
            AP.Gen.Output = False
            AP.Application.Page = 2
            AP.Sweep.Start
            AP.Gen.Output = True

            ChDir ap_file_directory
            new_test = GetFilePath$("", "*.at2", "", "Enter the NEW AP filename", 3)
            AP.File.SaveTestAs (new_test)
            ChDir ascii_data_directory
            new_data = GetFilePath$("", "*.adx", "", "Enter the NEW ASCII Data filename", 3)
            AP.File.ExportASCIIData(new_data)
            End
        End If

        counter = counter + 1
        GoTo loop1


End Sub

Sub Setup_panels

        'AP.Application.PanelOpen apbPanelDataEditor
        'AP.Application.PanelClose apbPanelDataEditor
        AP.Application.NewData
        AP.Application.Page = 1
        AP.Anlr.FuncFilterLP = 0
        AP.Application.Page = 2

End Sub                                 'Setup_panels
```

Speaker THD Measurement Routine:

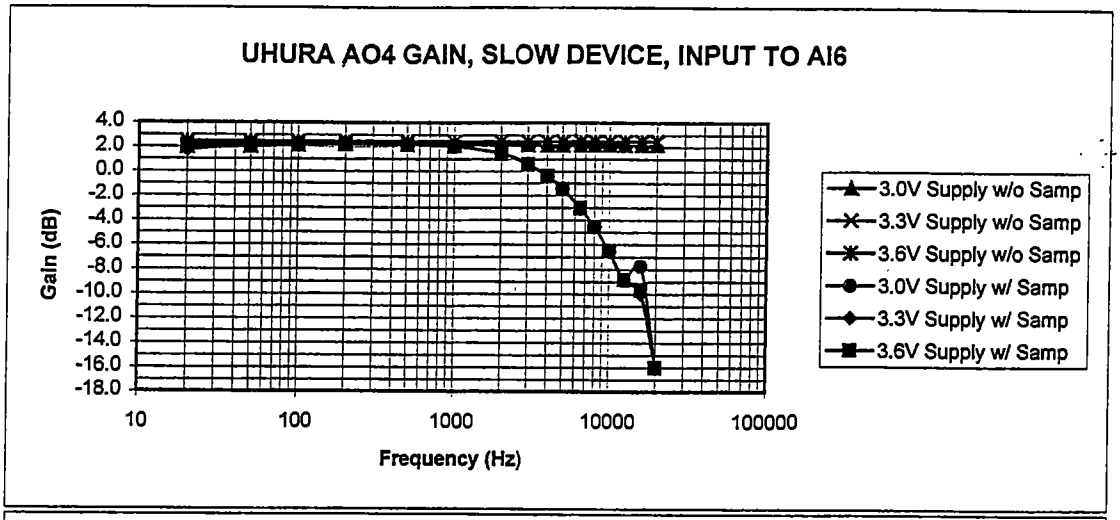
```
Sub Main

        ap_file_directory = "C:\files\THD Measurements"                    'Change directory for
different tests
        dsp_file_directory = "C:\ltdsp\r6_6_3\uhura\ai6tos~1"                    'Change
directory for different tests
        ascii_data_directory = "C:\files\THD Measurements"
        counter = 1

        ChDir ap_file_directory
        open_test = GetFilePath$("UHURA","at2","","Select the file to copy AP settings from",0)
        AP.File.OpenTest(open_test)              'Change filename for different tests.
        Call Setup_panels

loop1:
        ChDir dsp_file_directory
        Select Case counter
                Case 1
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_f")
                        Wait 8
                Case 2
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spk_8")
                        Wait 6
                Case 3
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_f")
                        Wait 8
                Case 4
                        Shell("C:\ltdsp\r6_6_3\uhura\ai6tos~1\runt.bat a6spks_8")
                        Wait 6
                Case Else
                        MsgBox ("Invalid Case in Select", 0, "Error")
                        End
        End Select

        If counter = 1 Then
                MsgBox ("Connect AP's Probes to Output.  Click 'OK' when ready.", 0, "Yo!")
        End If

        Call Desired_Output
        output_rms_ck = AP.Anlr.ChALevelRdg("V")                    'Getting measured RMS
- Confirmation
        output_pkpk_ck = output_rms_ck * 2 * (2 ^ 0.5)          'Converting RMS to pkpk -
Confirmation

        If output_pkpk_ck > 0.510 Or output_pkpk_ck < 0.490 Then
                'Comparing to desired
                Call Desired_Output
        End If
```

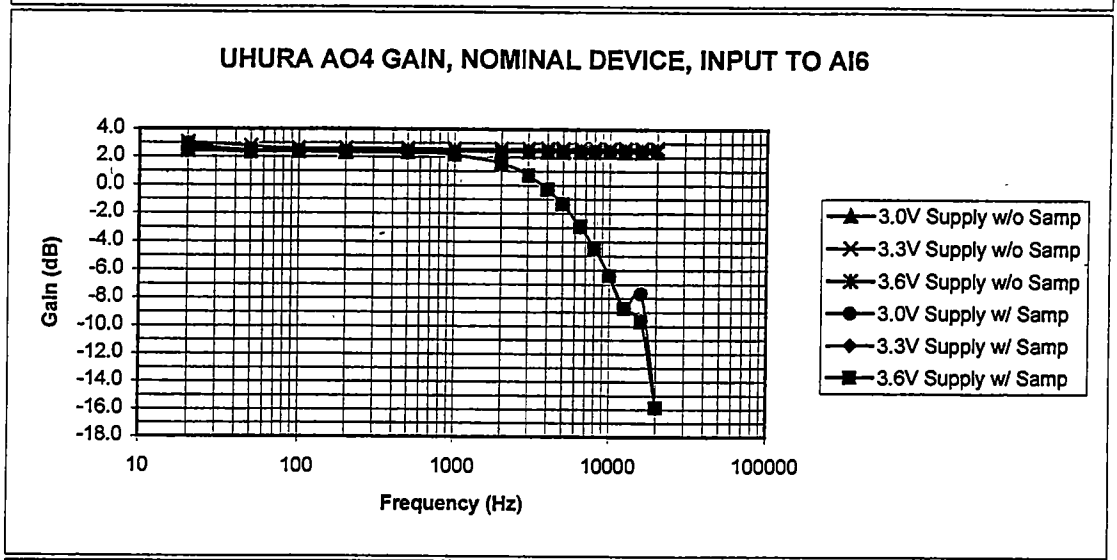
```
        AP.Sweep.Start

        If counter = 4 Then
                ChDir ap_file_directory
                new_test = GetFilePath$("UHURA","at2","","Enter the NEW AP filename", 3)
                AP.File.SaveTestAs (new_test)
                ChDir ascii_data_directory
                new_data = GetFilePath$("UHURA","adx","","Enter the NEW ASCII Data
filename", 3)
                AP.File.ExportASCIIData(new_data)
                End
        End If

        counter = counter + 1
        GoTo loop1


End Sub

Sub Setup_panels

        AP.Application.NewData
        AP.Application.Page = 1
        AP.Anlr.FuncFilterLP = 0
        AP.Application.Page = 2

End Sub                                 'Setup_panels

Sub Desired_Output

                g = 0
                term = 0
                AP.Application.Page = 1
                AP.Gen.Output = True

                While g = 0
                        output_rms = AP.Anlr.ChALevelRdg("V")                   'Getting
measured RMS
                        output_pkpk = output_rms * 2 * (2 ^ 0.5)        'Converting RMS to
pkpk
                        input_pkpk = AP.Gen.ChAAmpl("Vpp")                      'Getting
generators amplitude setting
                        gain = output_pkpk / input_pkpk
        'Calculate the gain
                        initial_pkpk = 0.5 / gain                               'Find
the approximate needed input knowing gain
                        AP.Gen.ChAAmpl("Vpp") = initial_pkpk            'Set input to
calculated value
                        input_pkpk = AP.Gen.ChAAmpl("Vpp")                      'Getting
generators new amplitude setting

                        If output_pkpk > 0.510 Then
        'Comparing to desired
```

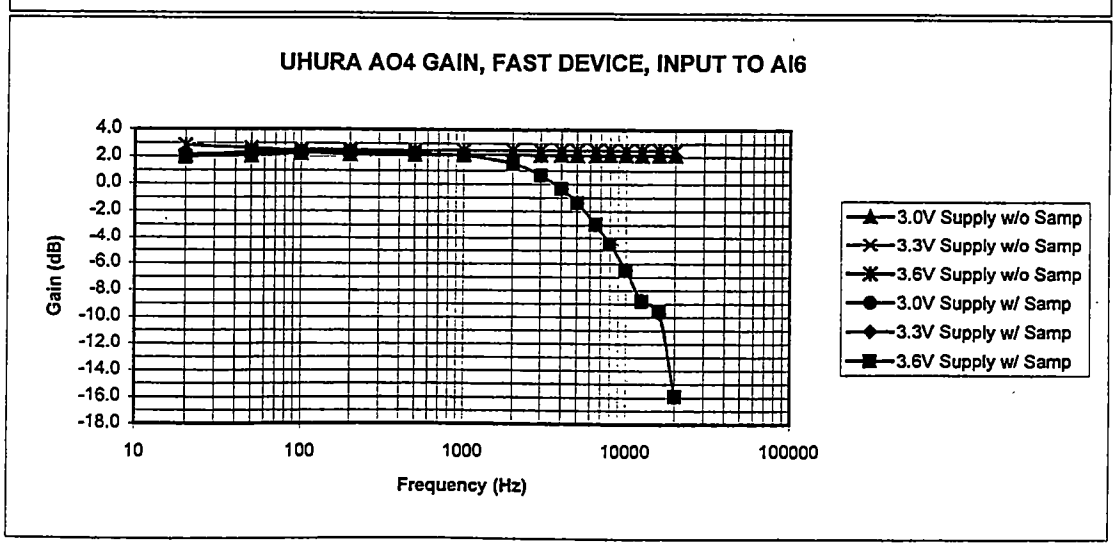
```
                    AP.Gen.ChAAmpl("Vpp") = input_pkpk - 0.001    'Decrementing
generators output
                ElseIf output_pkpk < 0.490 Then
                    AP.Gen.ChAAmpl("Vpp") = input_pkpk + 0.001    'Incrementing
generators output
                Else
                    g = 1
            'Setting Flag to continue
                End If

                If input_pkpk > 3.0 Or input_pkpk < 0.001 Then   'Watch for overflow -
chip not operating
                    MsgBox ("Output could not be set to 0.5Vpp.  Program will
terminate. Check device.", 0, "Error")
                    g = 1
                    End
                End If

            Wend
        AP.Application.Page = 2

End Sub                         'Desired_Output
```

APPENDIX B

AO4 DATA


UHURA AO4 GAIN, SLOW DEVICE, INPUT TO AI6
Gain (dB)
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
10
100
1000
10000
100000
Frequency (Hz)
3.0V Supply w/o Samp
3.3V Supply w/o Samp
3.6V Supply w/o Samp
3.0V Supply w/ Samp
3.3V Supply w/ Samp
3.6V Supply w/ Samp


UHURA AO4 GAIN, NOMINAL DEVICE, INPUT TO AI6
Gain (dB)
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
10
100
1000
10000
100000
Frequency (Hz)
3.0V Supply w/o Samp
3.3V Supply w/o Samp
3.6V Supply w/o Samp
3.0V Supply w/ Samp
3.3V Supply w/ Samp
3.6V Supply w/ Samp


UHURA AO4 GAIN, FAST DEVICE, INPUT TO AI6
Gain (dB)
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
10
100
1000
10000
100000
Frequency (Hz)
3.0V Supply w/o Samp
3.3V Supply w/o Samp
3.6V Supply w/o Samp
3.0V Supply w/ Samp
3.3V Supply w/ Samp
3.6V Supply w/ Samp

APPENDIX C

BANDGAP REFERENCE DATA

UHURA VREF MEASUREMENTS VARYING THE TEMPERATURE AT DIFFERENT SUPPLY VOLTAGES

Slow Device

	Supply			
Temp	2.7V	3.0V	3.3v	3.7V
-20.0	0.968	0.968	0.969	0.969
0.0	0.966	0.966	0.967	0.967
20.0	0.963	0.964	0.964	0.964
40.0	0.960	0.961	0.961	0.961
60	0.957	0.957	0.957	0.958
80	0.953	0.953	0.953	0.954

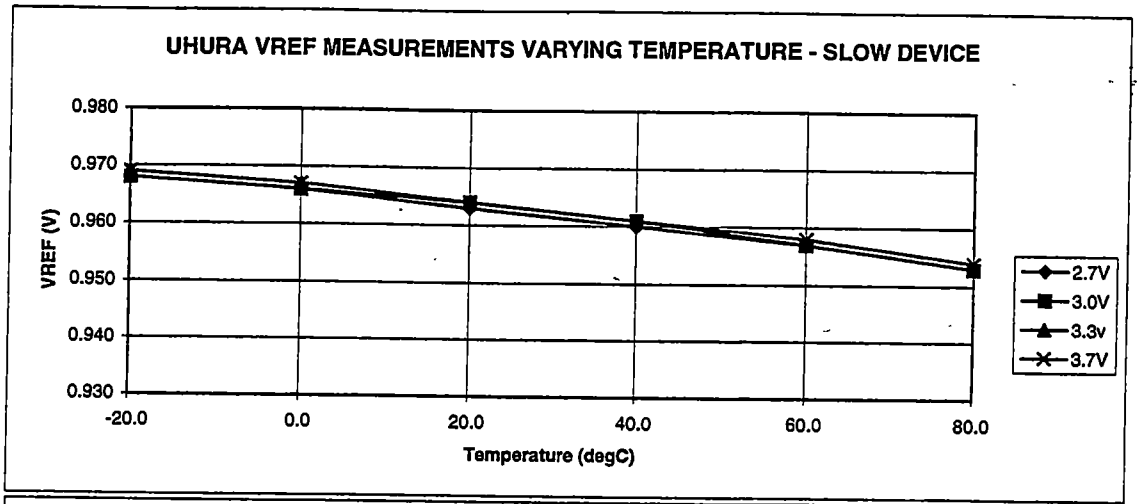
Nominal Device

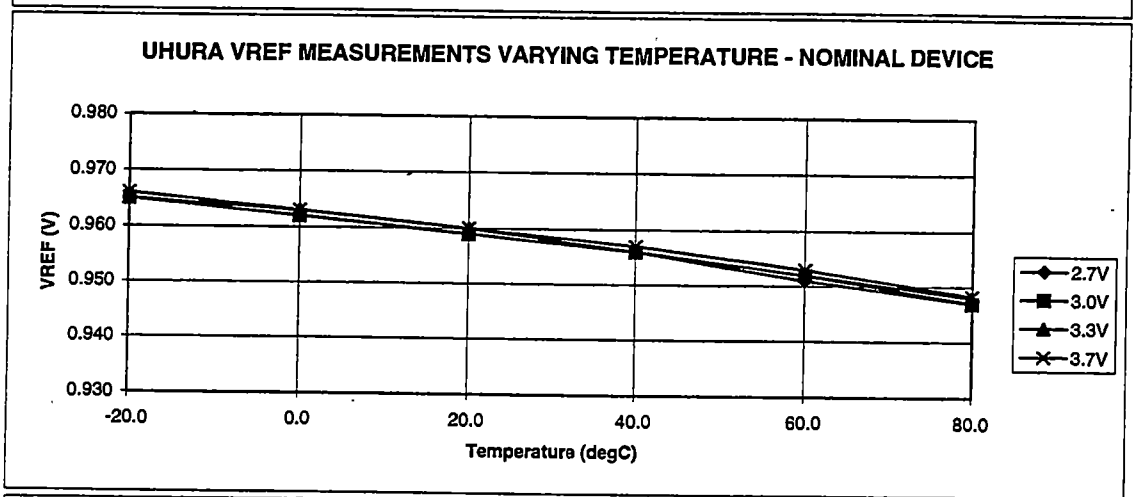
	Supply			
Temp	2.7V	3.0V	3.3V	3.7V
-20.0	0.965	0.965	0.965	0.966
0.0	0.962	0.962	0.963	0.963
20.0	0.959	0.959	0.960	0.960
40.0	0.956	0.956	0.956	0.957
60	0.951	0.952	0.952	0.953
80	0.947	0.947	0.948	0.9483

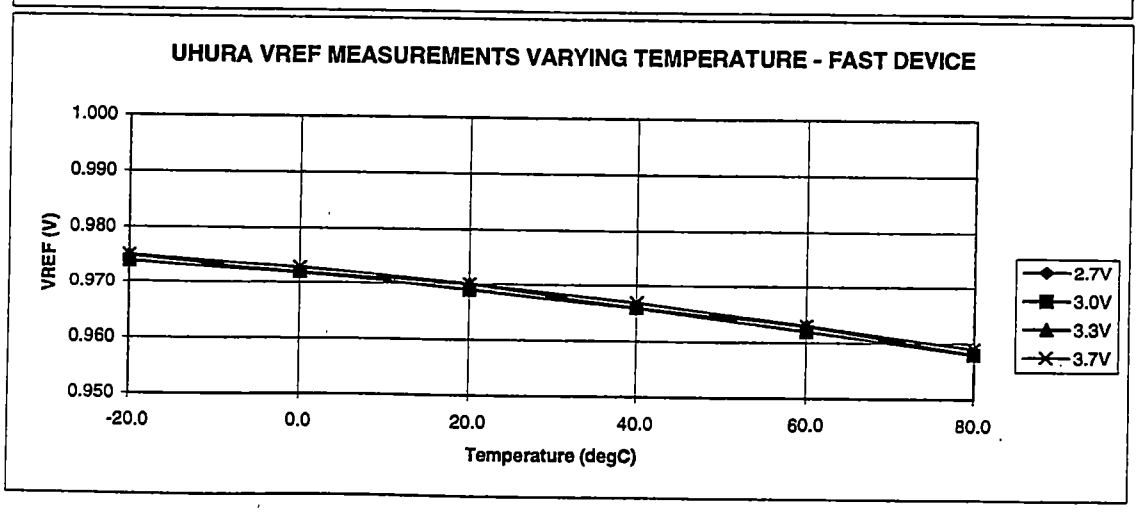
Fast Device

	Supply			
Temp	2.7V	3.0V	3.3V	3.7V
-20.0	0.974	0.974	0.975	0.975
0.0	0.972	0.972	0.972	0.973
20.0	0.969	0.969	0.970	0.970
40.0	0.966	0.966	0.966	0.967
60	0.962	0.962	0.963	0.963
80.0	0.958	0.958	0.958	0.959

UHURA VREF MEASUREMENTS VARYING THE TEMPERATURE AT DIFFERENT SUPPLY VOLTAGES







UHURA VREF MEASUREMENTS VARYING THE SUPPLY VOLTAGE AT 0 and -20 degC

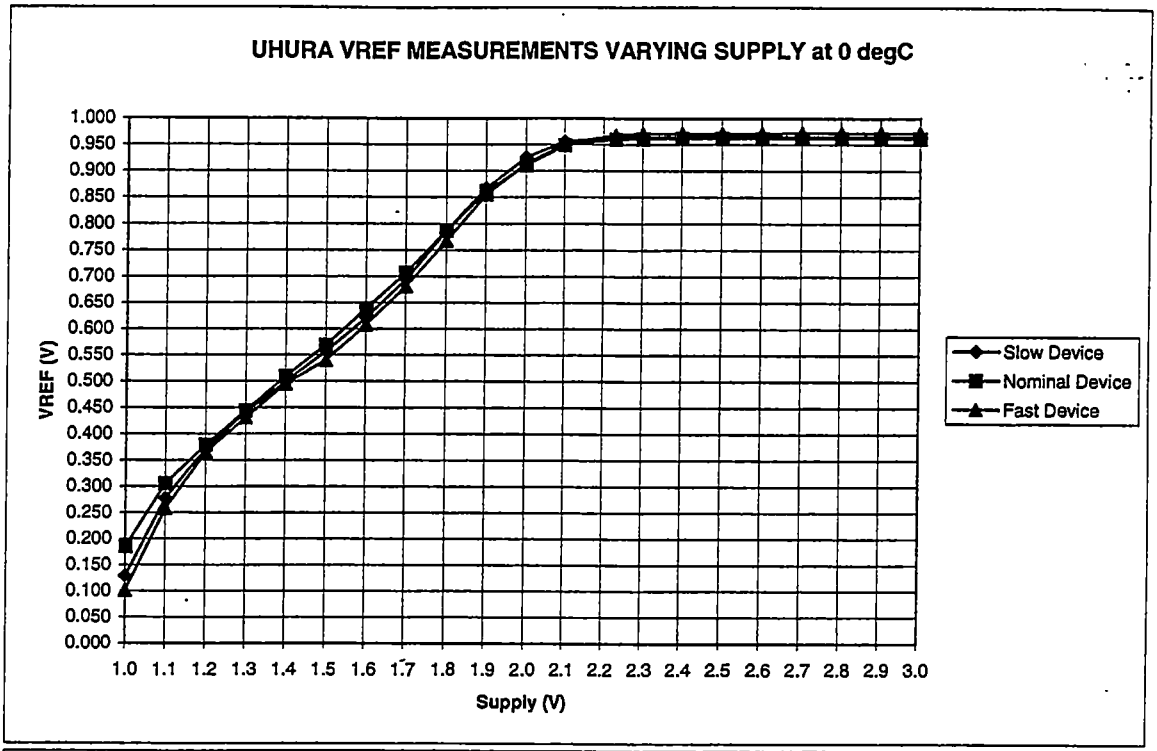
Temp: 0 degC

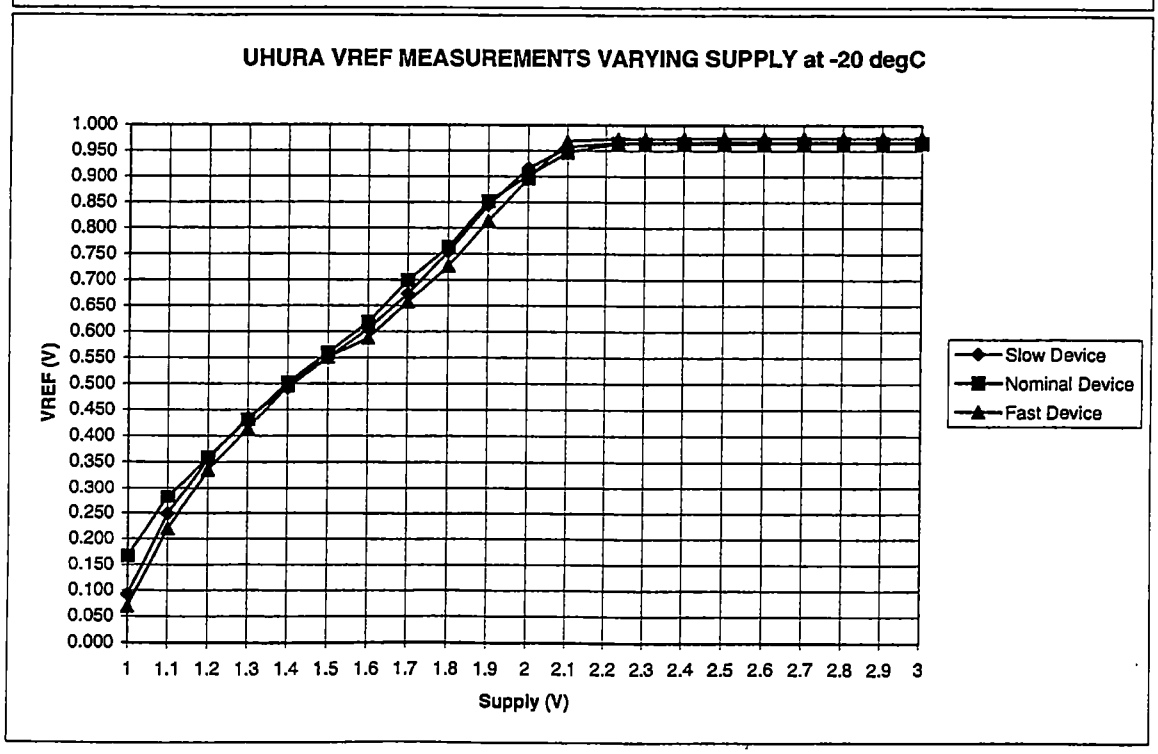
Supply	Slow Device	Nominal Device	Fast Device
1.0	0.129	0.185	0.101
1.1	0.278	0.306	0.258
1.2	0.372	0.379	0.366
1.3	0.441	0.444	0.431
1.4	0.499	0.509	0.495
1.5	0.557	0.569	0.540
1.6	0.621	0.639	0.608
1.7	0.694	0.707	0.681
1.8	0.787	0.787	0.767
1.9	0.867	0.862	0.856
2.0	0.926	0.911	0.914
2.1	0.956	0.949	0.952
2.2	0.964	0.960	0.968
2.3	0.965	0.961	0.971
2.4	0.965	0.962	0.971
2.5	0.966	0.962	0.971
2.6	0.966	0.962	0.971
2.7	0.966	0.962	0.972
2.8	0.966	0.962	0.972
2.9	0.966	0.962	0.972
3.0	0.966	0.962	0.972

Temp: -20 degC

Supply	Slow Device	Nominal Device	Fast Device
1.0	0.092	0.167	0.069
1.1	0.249	0.283	0.220
1.2	0.357	0.359	0.336
1.3	0.435	0.432	0.414
1.4	0.492	0.502	0.496
1.5	0.550	0.559	0.551
1.6	0.605	0.618	0.587
1.7	0.673	0.699	0.657
1.8	0.754	0.763	0.726
1.9	0.844	0.852	0.813
2.0	0.916	0.902	0.896
2.1	0.957	0.947	0.969
2.2	0.965	0.964	0.973
2.3	0.967	0.964	0.973
2.4	0.967	0.964	0.973
2.5	0.968	0.964	0.974
2.6	0.968	0.964	0.974
2.7	0.968	0.965	0.974
2.8	0.968	0.965	0.974
2.9	0.968	0.965	0.974
3.0	0.968	0.965	0.974

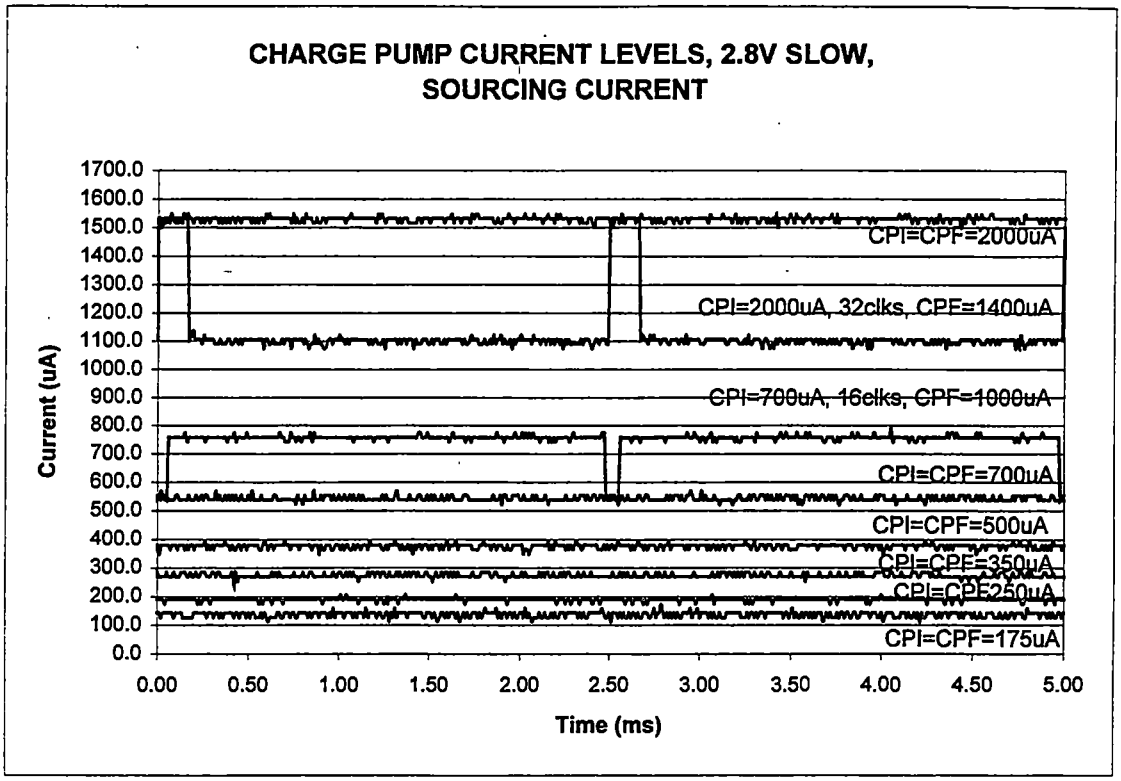
UHURA VREF MEASUREMENTS VARYING THE SUPPLY VOLTAGE AT 0 and -20 degC

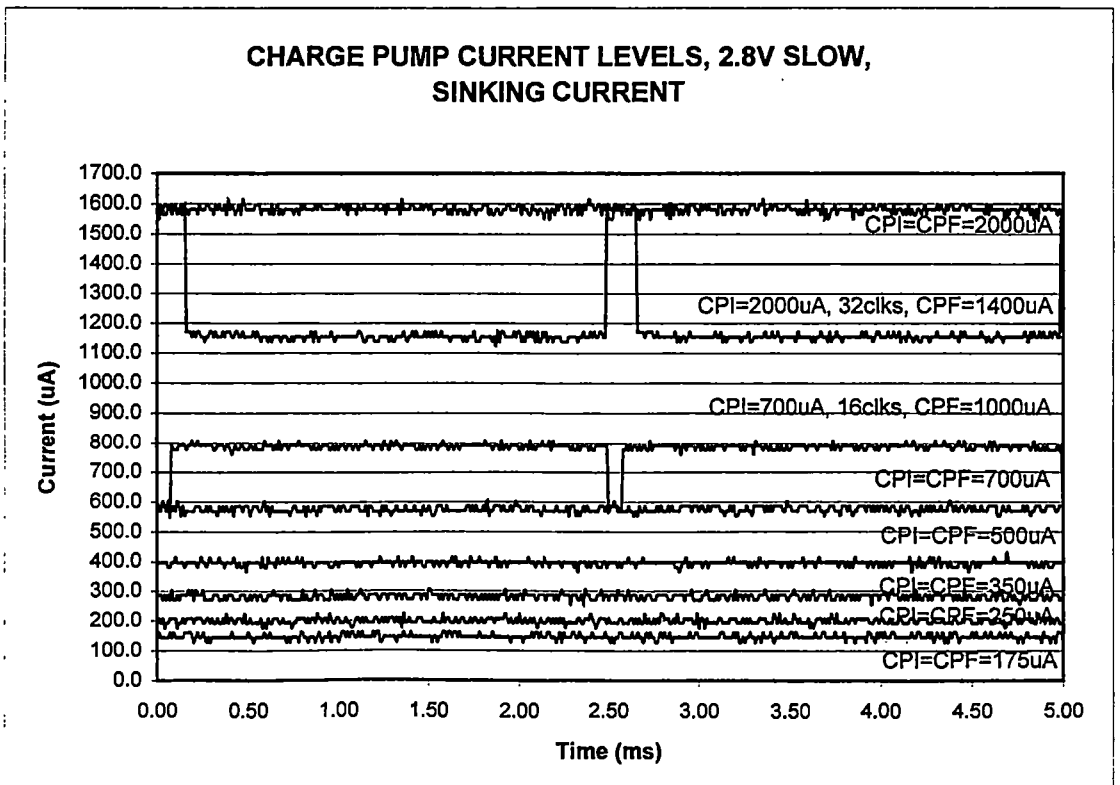


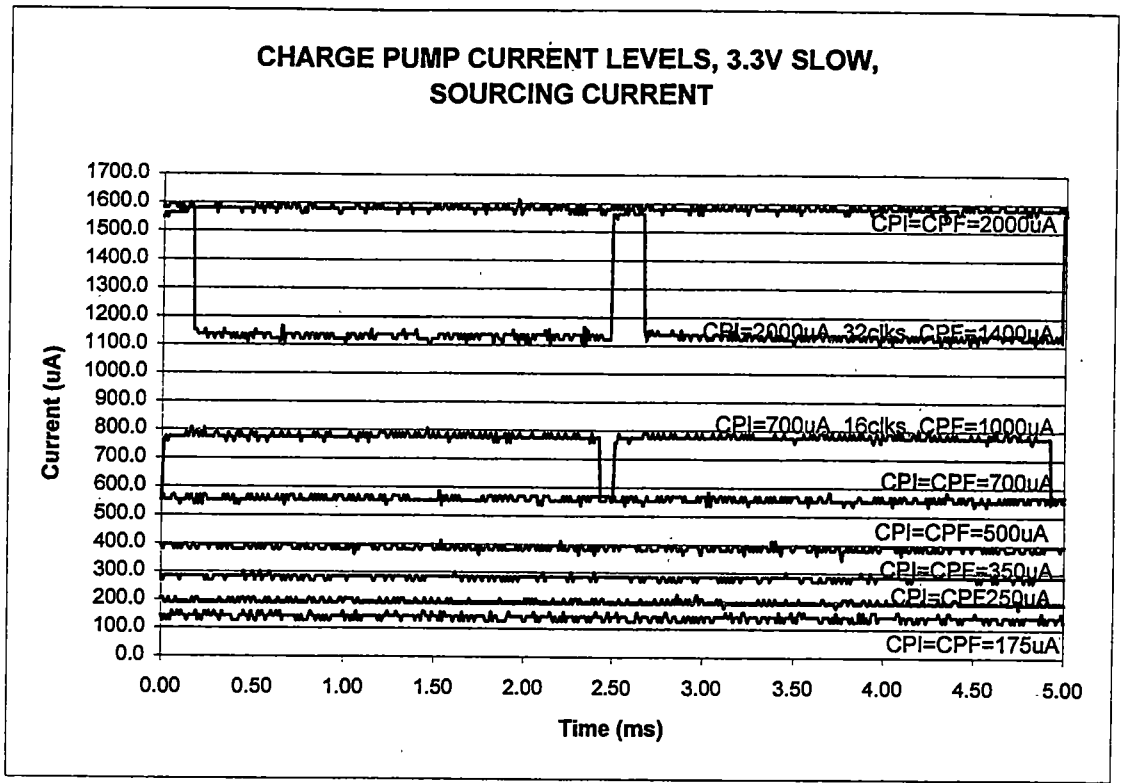


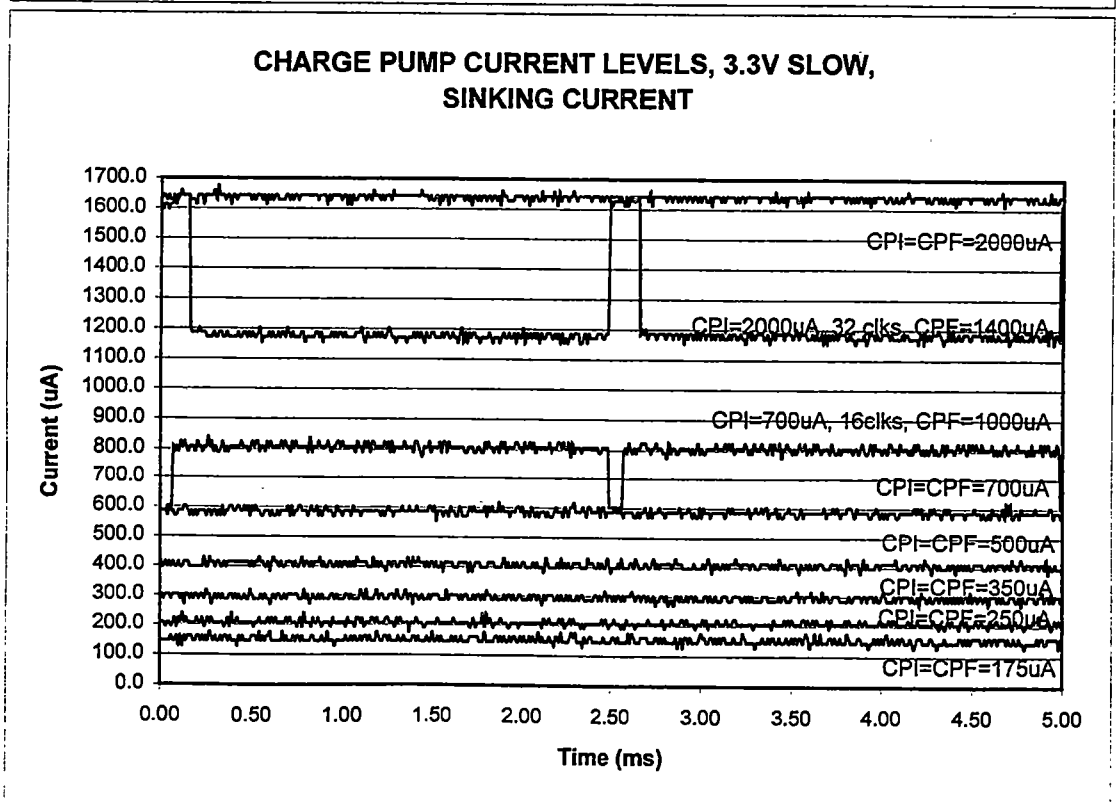
APPENDIX D

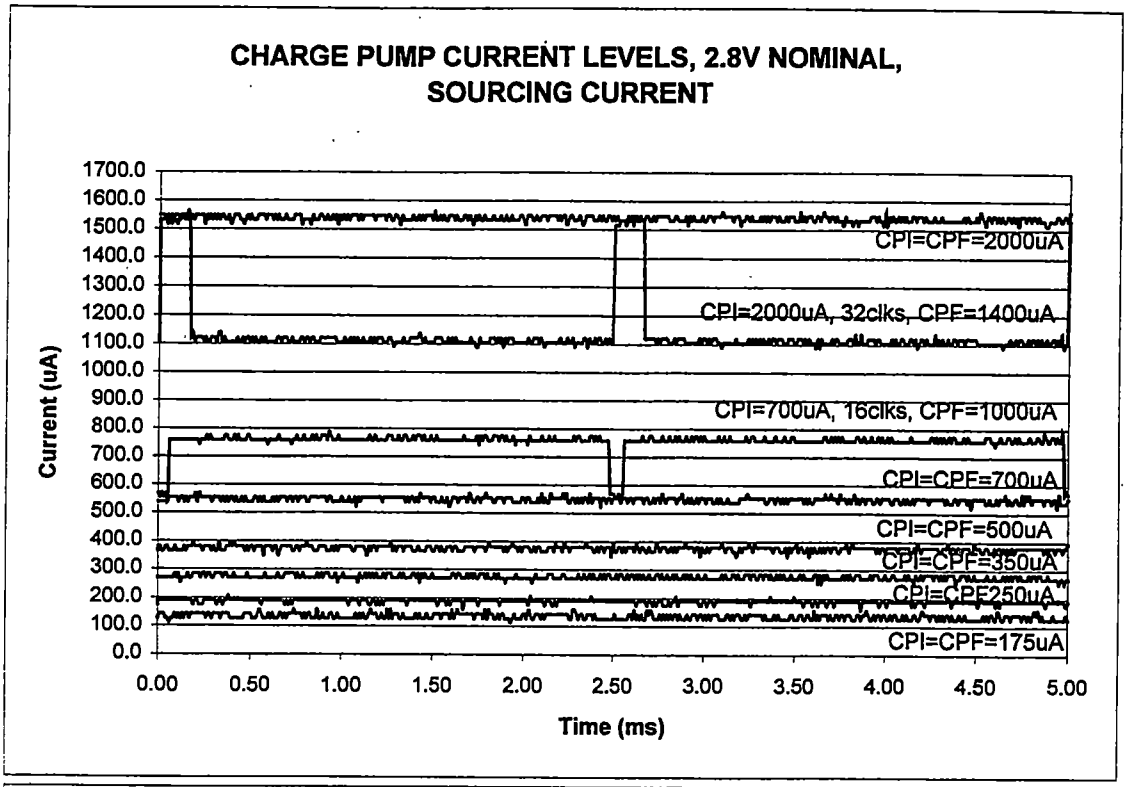
CHARGE PUMP DATA

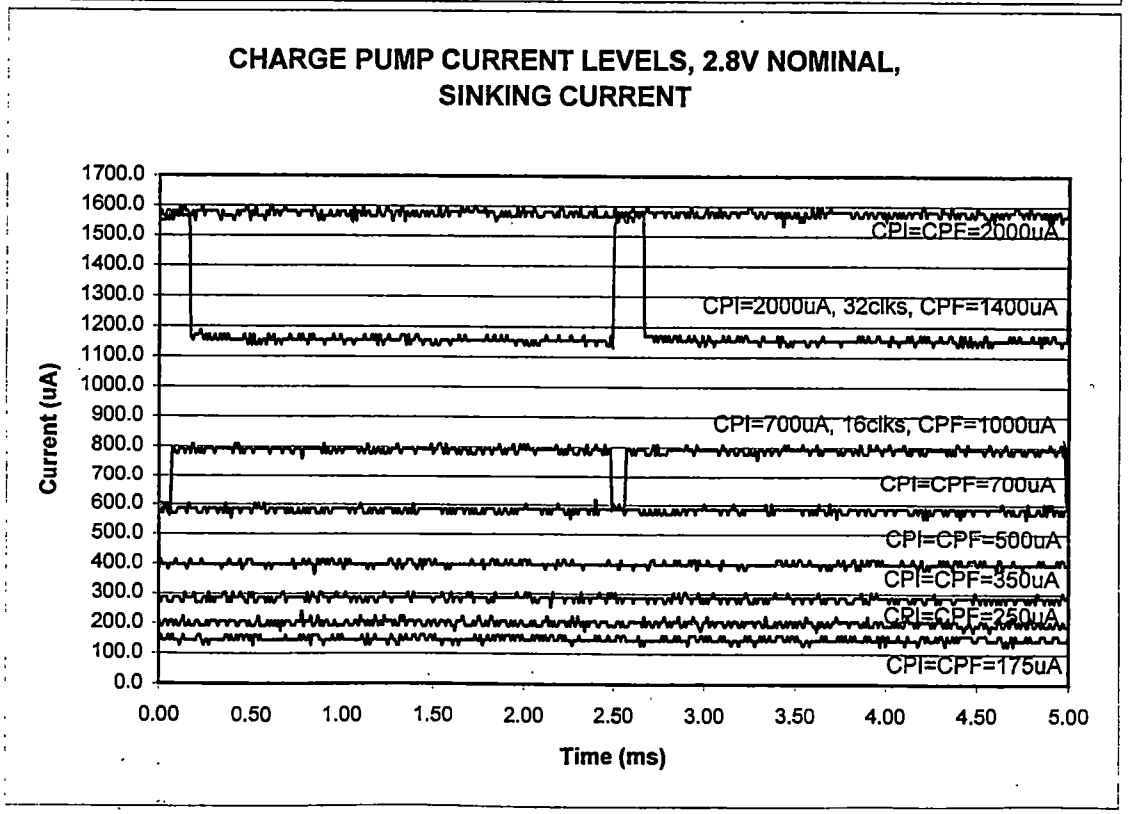

CHARGE PUMP CURRENT LEVELS, 2.8V SLOW,
SOURCING CURRENT
Current (uA)
1700.0
1600.0
1500.0
1400.0
1300.0
1200.0
1100.0
1000.0
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
CPI=CPF=2000uA
CPI=2000uA, 32clks, CPF=1400uA
CPI=700uA, 16clks, CPF=1000uA
CPI=CPF=700uA
CPI=CPF=500uA
CPI=CPF=350uA
CPI=CPF250uA
CPI=CPF=175uA
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
Time (ms)


CHARGE PUMP CURRENT LEVELS, 2.8V SLOW,
SINKING CURRENT
Current (uA)
1700.0
1600.0
1500.0
1400.0
1300.0
1200.0
1100.0
1000.0
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
CPI=CPF=2000uA
CPI=2000uA, 32clks, CPF=1400uA
CPI=700uA, 16clks, CPF=1000uA
CPI=CPF=700uA
CPI=CPF=500uA
CPI=CPF=350uA
CPI=CPF=250uA
CPI=CPF=175uA
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
Time (ms)

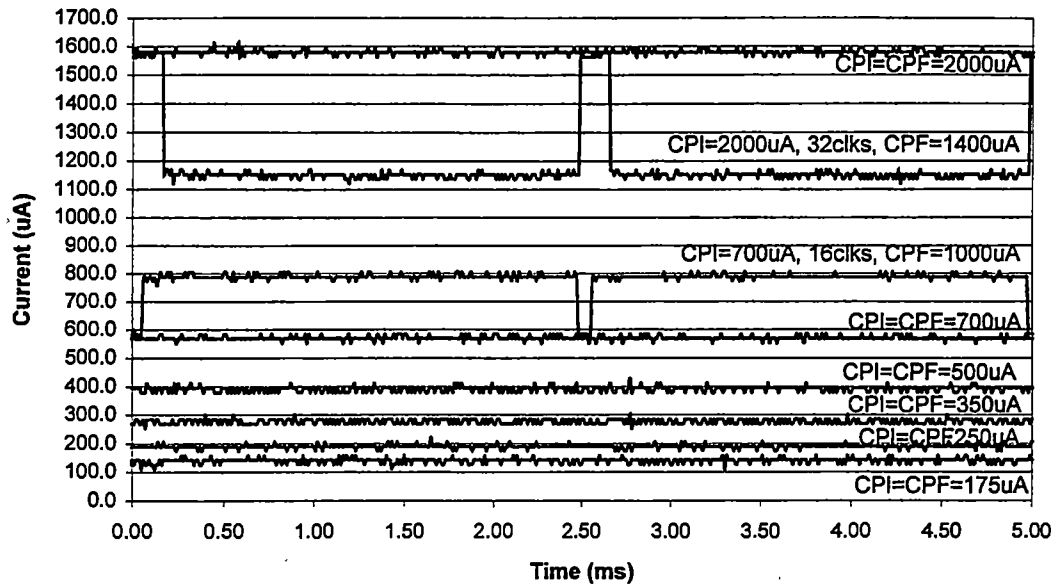

CHARGE PUMP CURRENT LEVELS, 3.3V SLOW, SOURCING CURRENT
Current (uA)
Time (ms)
CPI=CPF=2000uA
CPI=2000uA, 32clks, CPF=1400uA
CPI=700uA, 16clks, CPF=1000uA
CPI=CPF=700uA
CPI=CPF=500uA
CPI=CPF=350uA
CPI=CPF250uA
CPI=CPF=175uA


CHARGE PUMP CURRENT LEVELS, 3.3V SLOW, SINKING CURRENT
Current (uA)
Time (ms)
CPI=CPF=2000uA
CPI=2000uA, 32 clks, CPF=1400uA
CPI=700uA, 16clks, CPF=1000uA
CPI=CPF=700uA
CPI=CPF=500uA
CPI=CPF=350uA
CPI=CPF=250uA
CPI=CPF=175uA

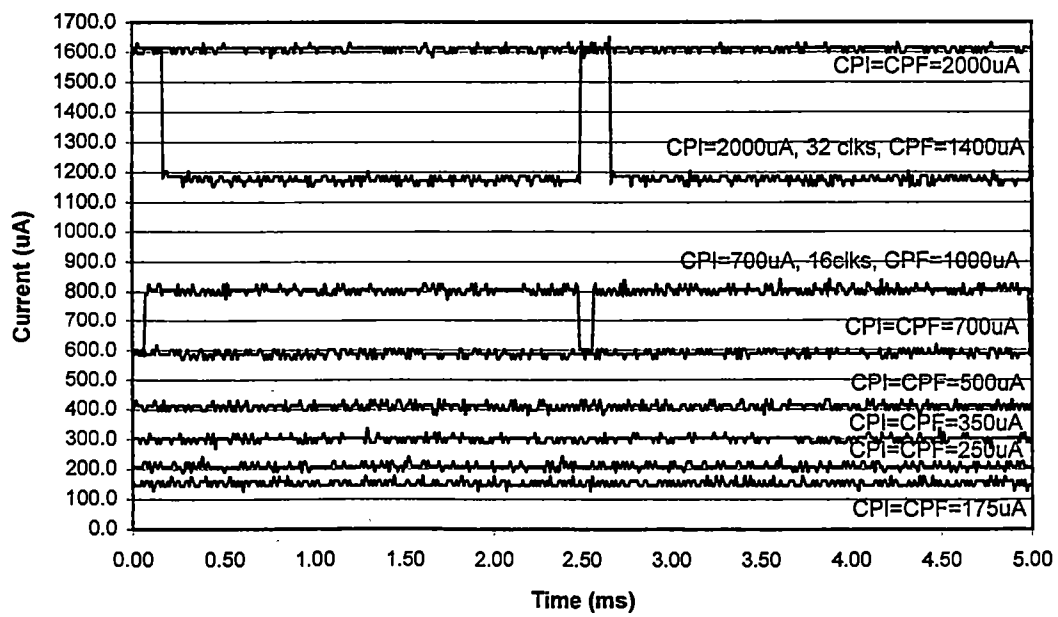

CHARGE PUMP CURRENT LEVELS, 2.8V NOMINAL,
SOURCING CURRENT
Current (uA)
1700.0
1600.0
1500.0
1400.0
1300.0
1200.0
1100.0
1000.0
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
CPI=CPF=2000uA
CPI=2000uA, 32clks, CPF=1400uA
CPI=700uA, 16clks, CPF=1000uA
CPI=CPF=700uA
CPI=CPF=500uA
CPI=CPF=350uA
CPI=CPF=250uA
CPI=CPF=175uA
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
Time (ms)


CHARGE PUMP CURRENT LEVELS, 2.8V NOMINAL,
SINKING CURRENT
Current (uA)
1700.0
1600.0
1500.0
1400.0
1300.0
1200.0
1100.0
1000.0
900.0
800.0
700.0
600.0
500.0
400.0
300.0
200.0
100.0
0.0
CPI=CPF=2000uA
CPI=2000uA, 32clks, CPF=1400uA
CPI=700uA, 16clks, CPF=1000uA
CPI=CPF=700uA
CPI=CPF=500uA
CPI=CPF=350uA
CPI=CPF=250uA
CPI=CPF=175uA
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
Time (ms)

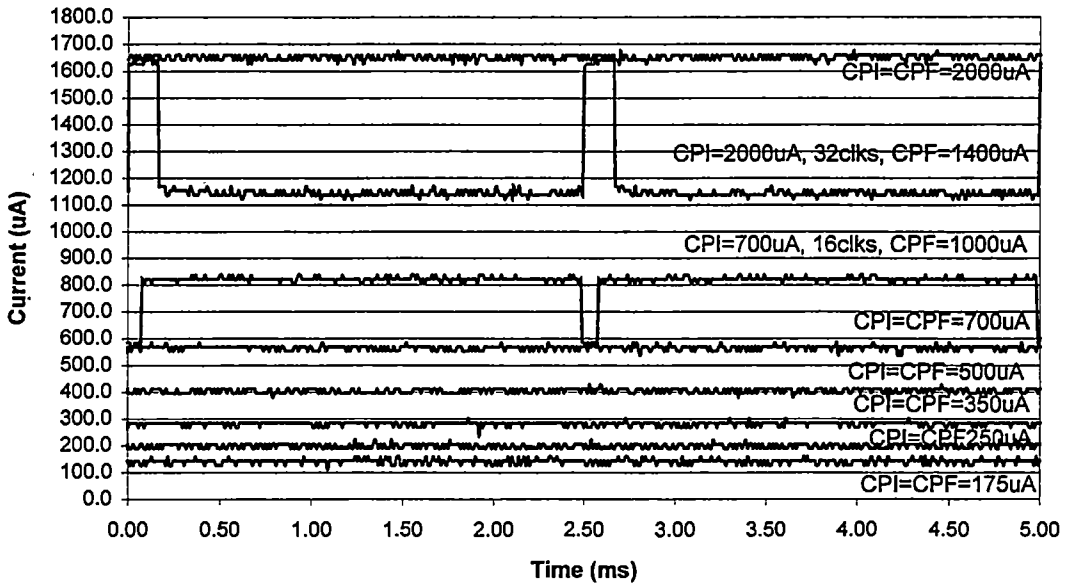
CHARGE PUMP CURRENT LEVELS, 3.3V NOMINAL, SOURCING CURRENT



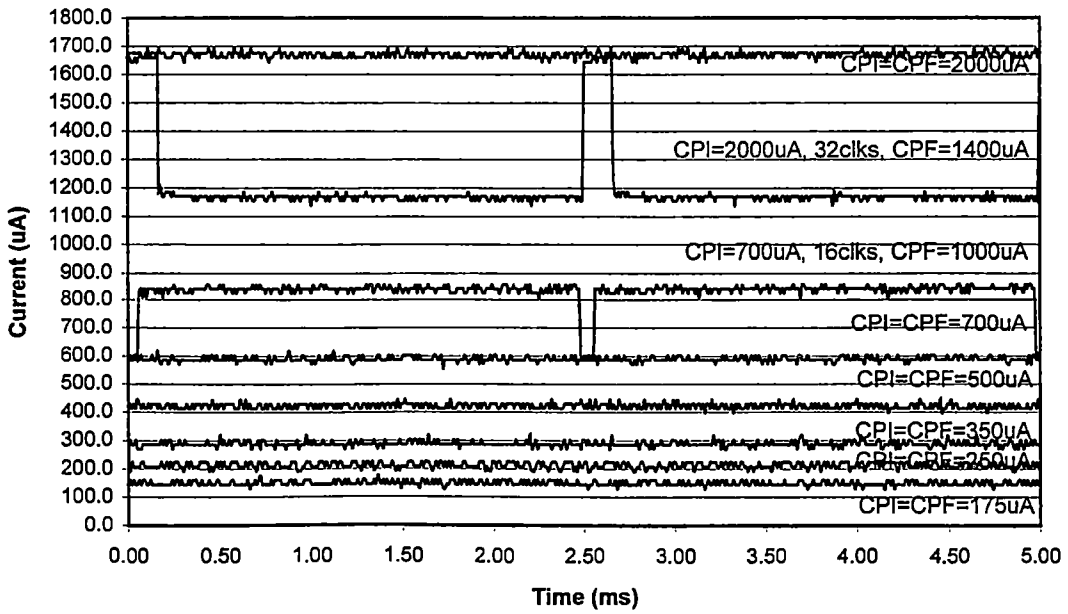
CHARGE PUMP CURRENT LEVELS, 3.3V NOMINAL, SINKING CURRENT



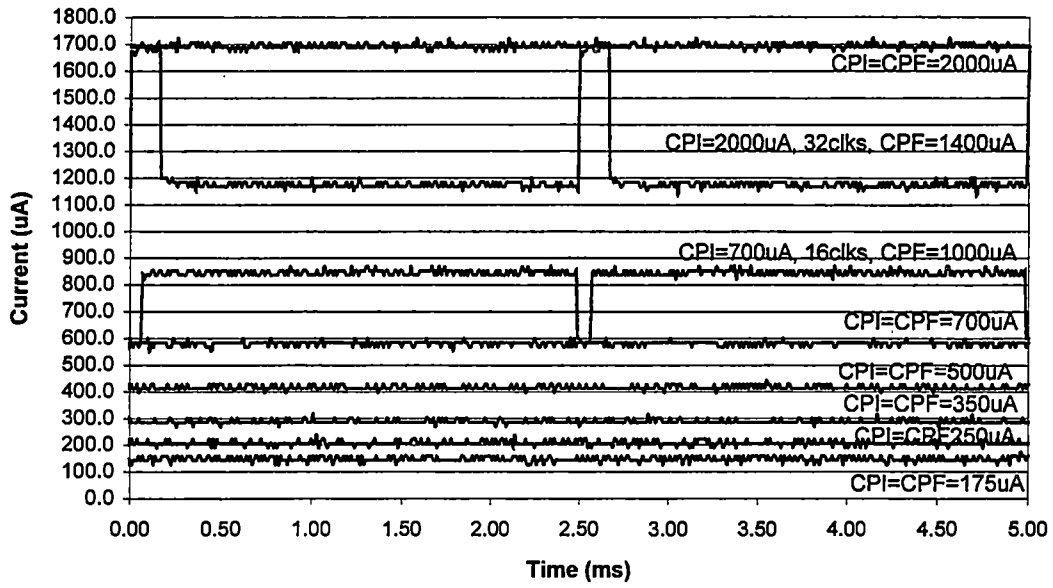
CHARGE PUMP CURRENT LEVELS, 2.8V FAST, SOURCING CURRENT



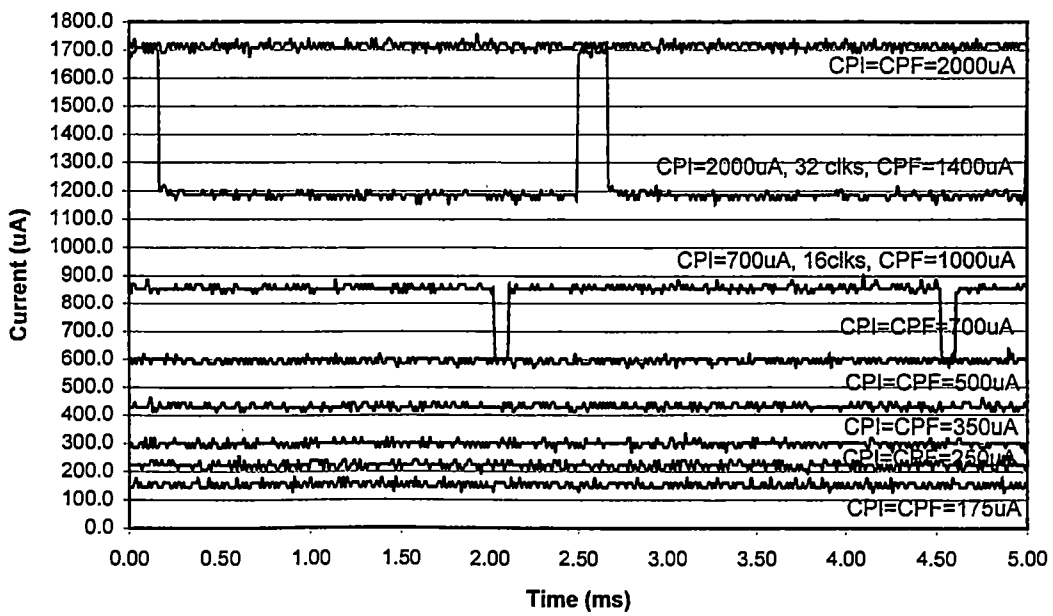
CHARGE PUMP CURRENT LEVELS, 2.8V FAST, SINKING CURRENT



CHARGE PUMP CURRENT LEVELS, 3.3V FAST, SOURCING CURRENT



CHARGE PUMP CURRENT LEVELS, 3.3V FAST, SINKING CURRENT



APPENDIX E

CURRENT CONSUMPTION DATA

Table 1: CSP1009, Slow Device, Analog Block Current Consumption

Active Block	Current (mA) Supply = 3.3V	Current (mA) Supply = 3.0V	Current (mA) Supply = 2.7 V
CODEC (Analog ON)	1.23	1.21	1.19
PGA (28dB Gain)	0.63	0.62	0.60
PGMO (44db Gain)	0.79	0.78	0.77
LNDRV1 (5.4dB Gain)	1.59 (1)	1.59 (1)	1.57 (1)
LNDRV2 (5.4dB Gain)	1.60 (1)	1.59 (1)	1.58 (1)
SPKRDRV (2dB)	2.93	2.98	3.26
AO4 (loaded - 1mA)	1.00 (1)	0.98 (1)	0.97 (1)
Total	9.90	9.75	9.94
Total (2)	7.17	7.18	7.39

Table 2: CSP1009, Nominal Device, Analog Block Current Consumption

Active Block	Current (mA) Supply = 3.3V	Current (mA) Supply = 3.0V	Current (mA) Supply = 2.7 V
CODEC (Analog ON)	1.26	1.24	1.22
PGA (28dB Gain)	0.60	0.60	0.59
PGMO (44db Gain)	0.78	0.78	0.75
LNDRV1 (5.4dB Gain)	1.28	1.28	1.27
LNDRV2 (5.4dB Gain)	1.36	1.36	1.35
SPKRDRV (2dB)	3.06	3.04	3.04
AO4 (loaded - 1mA)	1.66	1.65	1.65
Total	10.145	10.15	10.21
Total (2)	6.98	6.94	6.87

Table 3: CSP1009, Fast Device, Analog Block Current Consumption

Active Block	Current (mA) Supply = 3.3V	Current (mA) Supply = 3.0V	Current (mA) Supply = 2.7 V
CODEC (Analog ON)	1.31	1.30	1.28
PGA (28dB Gain)	0.68	0.66	0.64
PGMO (44db Gain)	0.86	0.84	0.81
LNDRV1 (5.4dB Gain)	1.59 (1)	1.58 (1)	1.57 (1)
LNDRV2 (5.4dB Gain)	1.57 (1)	1.57 (1)	1.56 (1)
SPKRDRV (2dB)	3.06	3.18	3.08
AO4 (loaded - 1mA)	1.64 (1)	1.62 (1)	1.62 (1)
Total	11.03	10.89	10.58
Total (2)	7.50	7.56	7.38

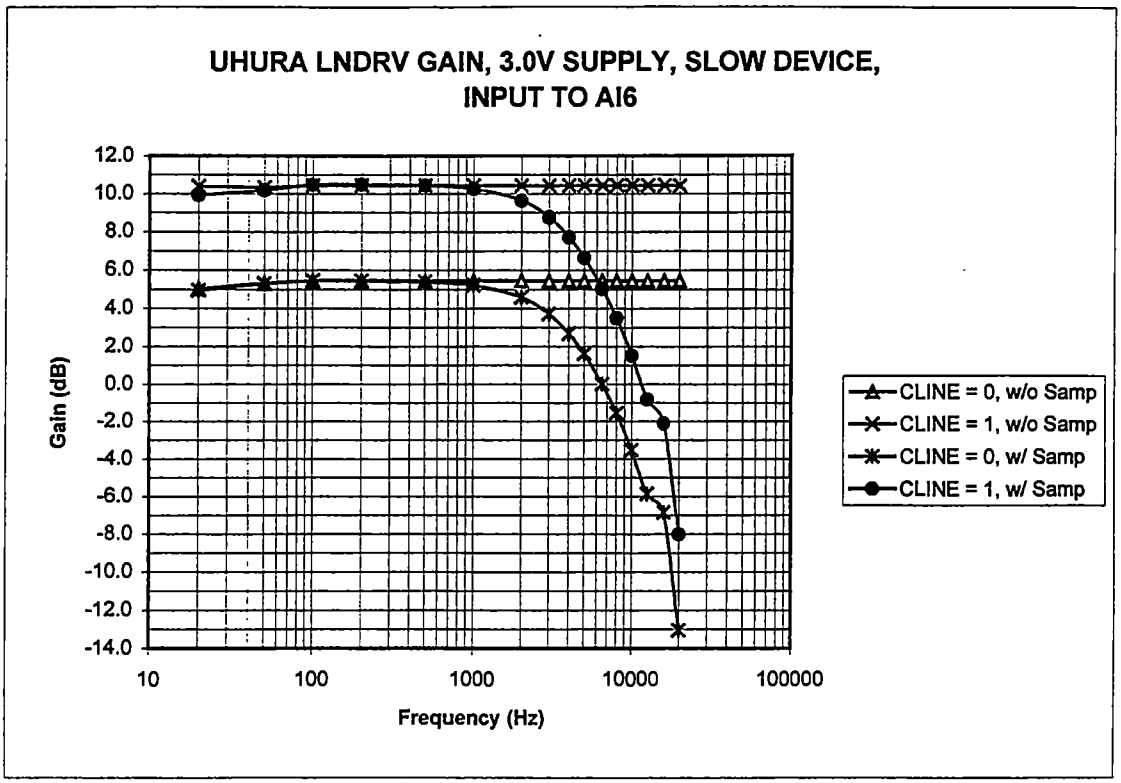
Notes:

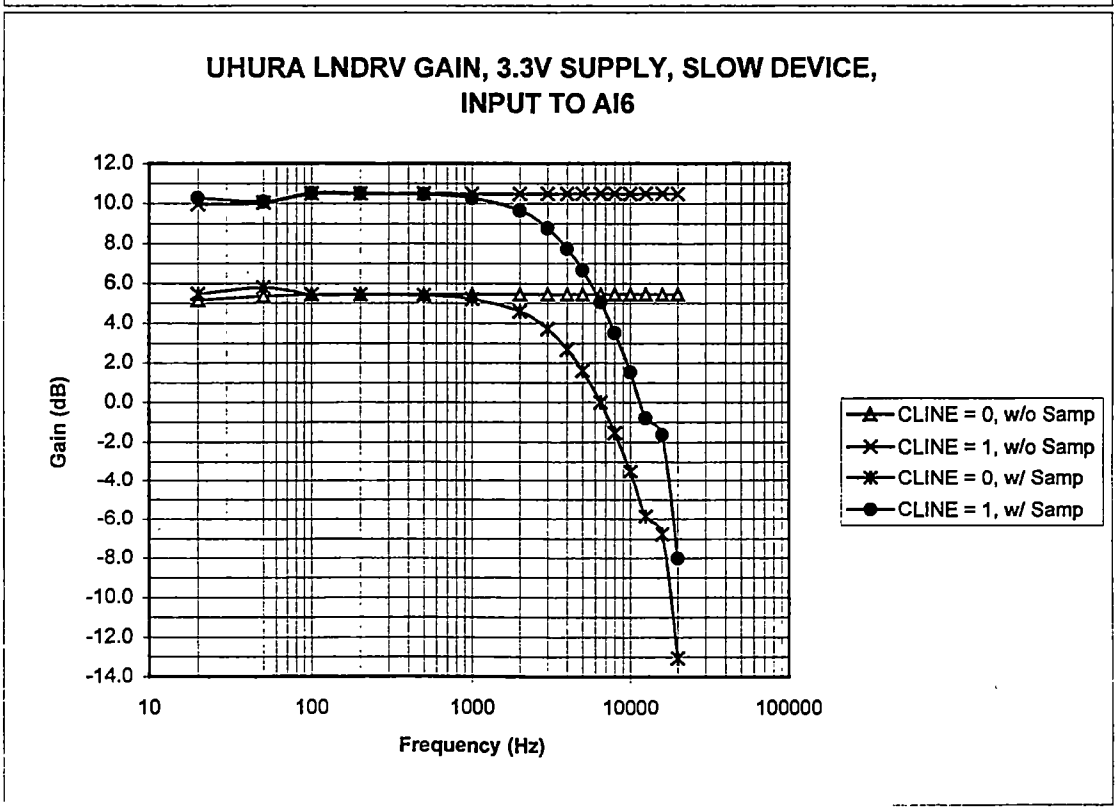
1) For these measurements the CODEC was ON but bypassed due distortion of the output waveform when the supply voltage is below 3.0V for the fast device and 2.9V for the slow device.
2) This is a worst case total during normal operation of the channels. It is the summation of CODEC, PGA, PGMO, LNDRV1, & SPKRDRV currents.
3) All measurements were taken at 25° C.

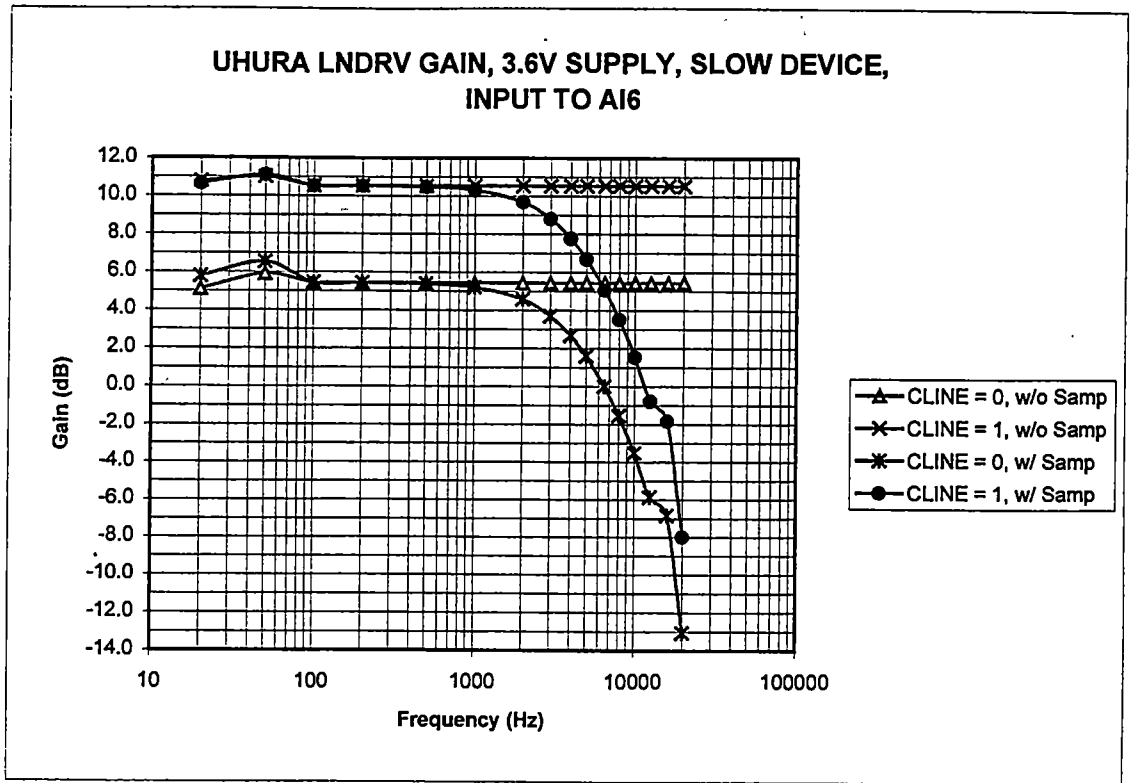
APPENDIX F

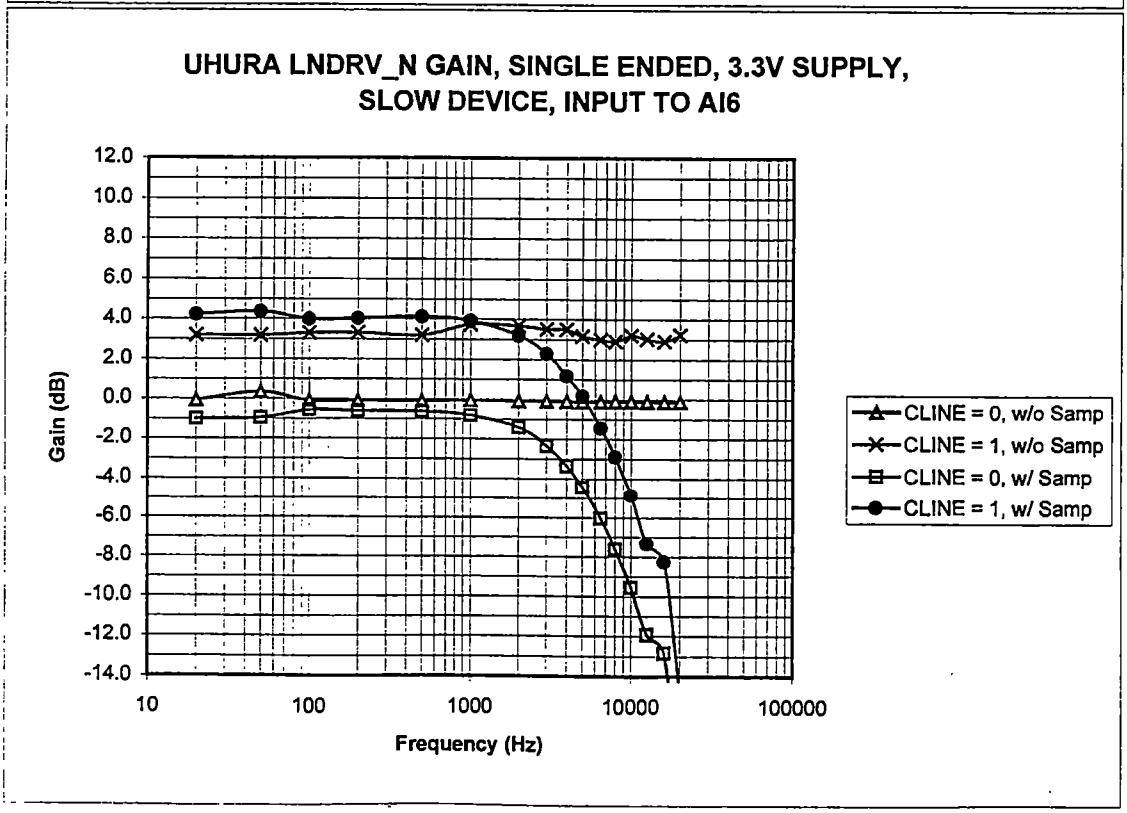
LINE DRIVER AMPLIFIER DATA

LINE DRIVER GAIN DATA

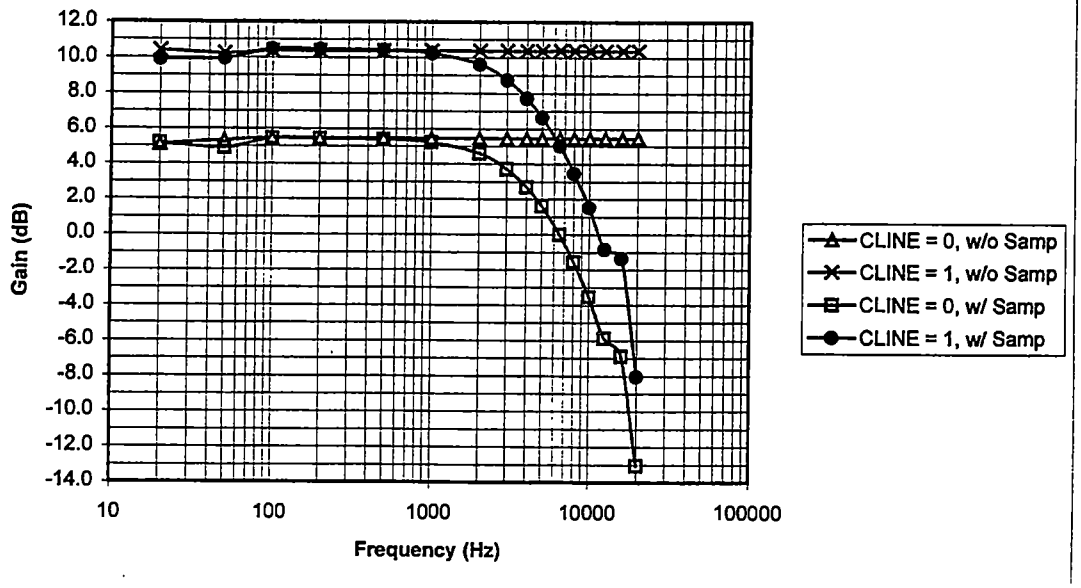

UHURA LNDRV GAIN, 3.0V SUPPLY, SLOW DEVICE,
INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp


UHURA LNDRV GAIN, 3.3V SUPPLY, SLOW DEVICE,
INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

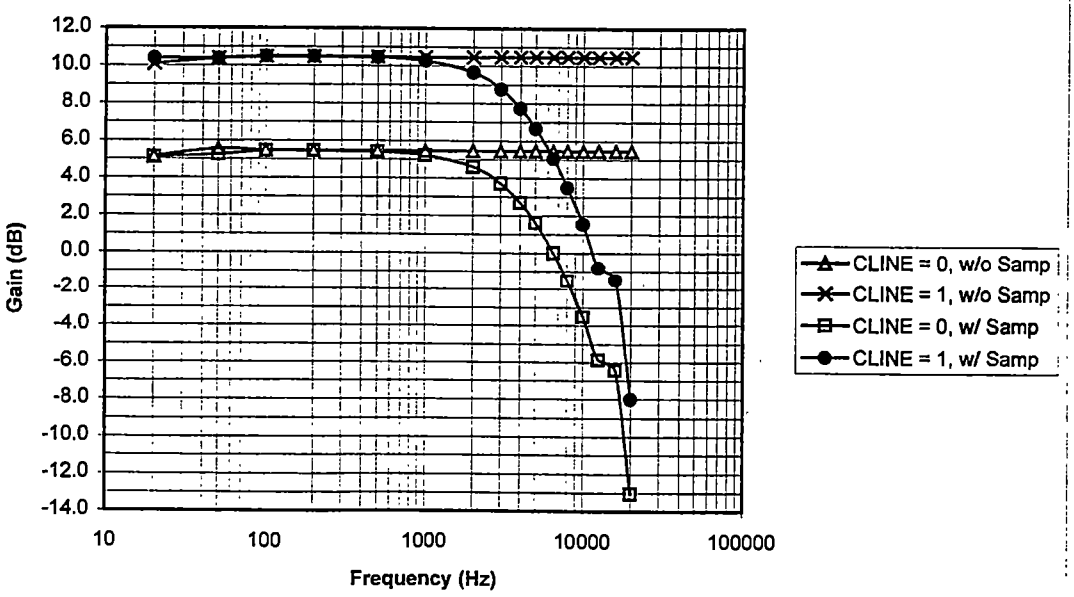

UHURA LNDRV GAIN, 3.6V SUPPLY, SLOW DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

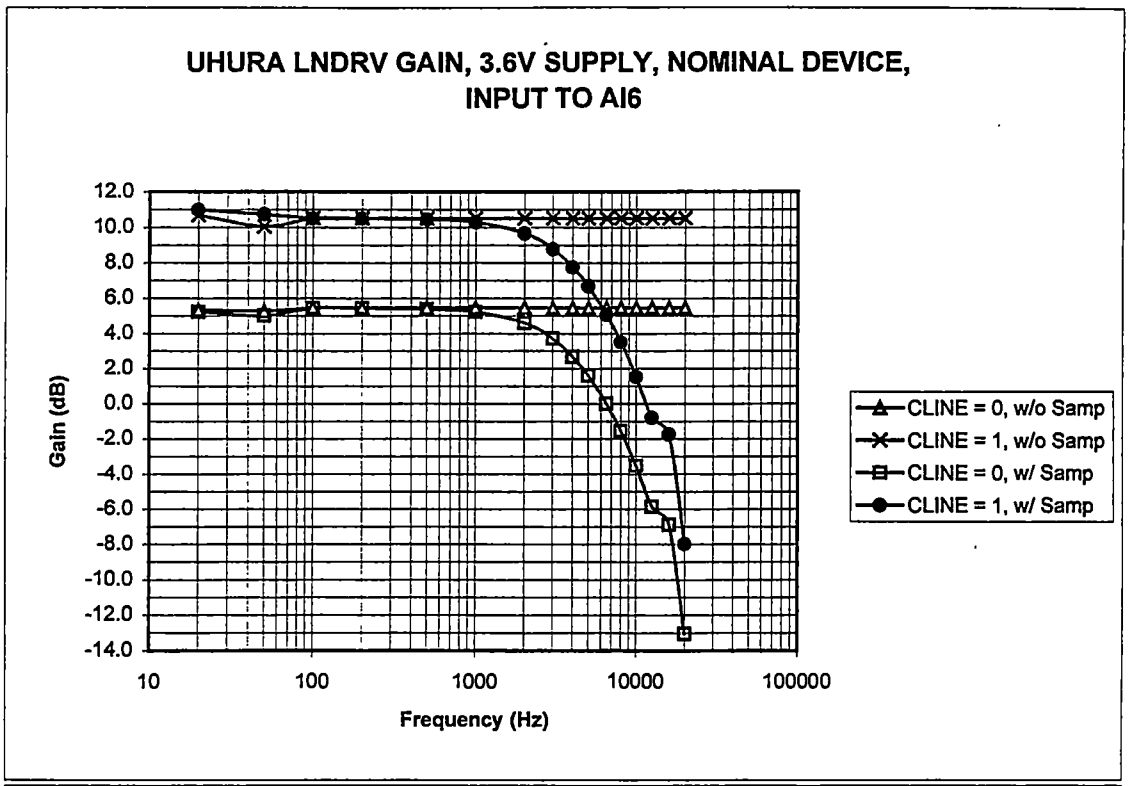

UHURA LNDRV_N GAIN, SINGLE ENDED, 3.3V SUPPLY, SLOW DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

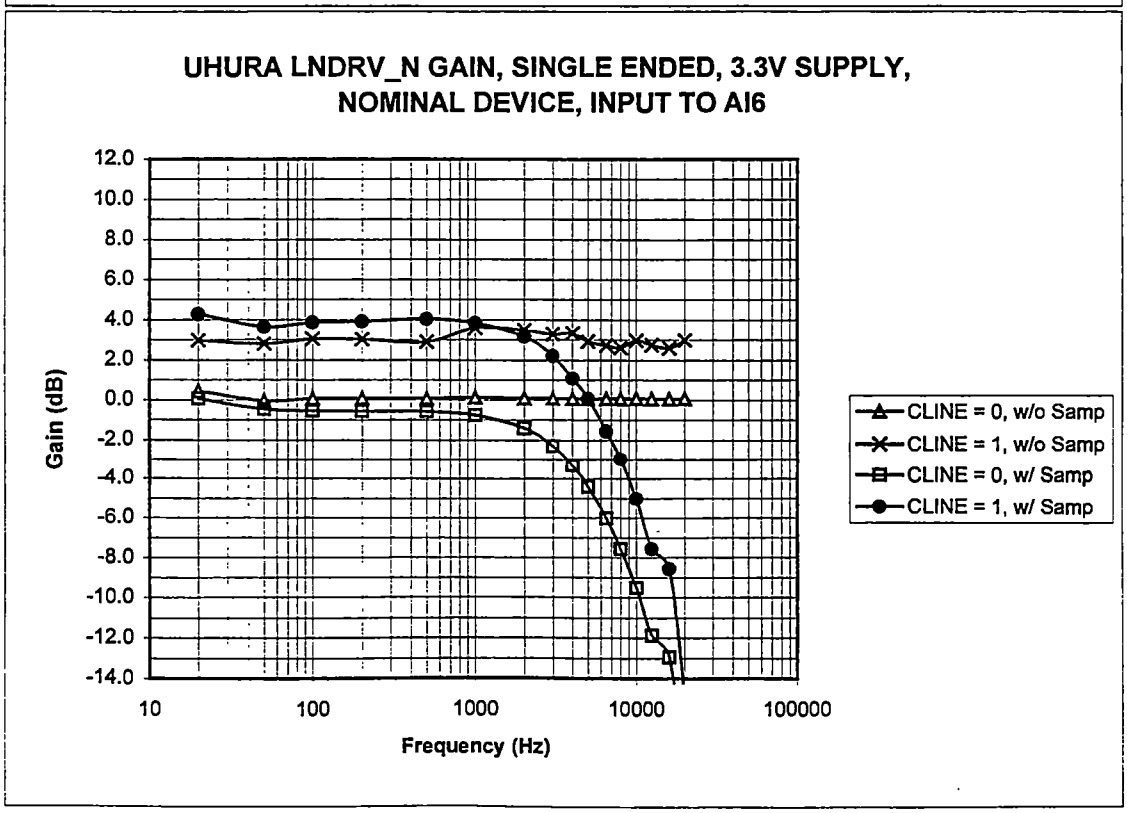
UHURA LNDRV GAIN, 3.0V SUPPLY, NOMINAL DEVICE, INPUT TO AI6

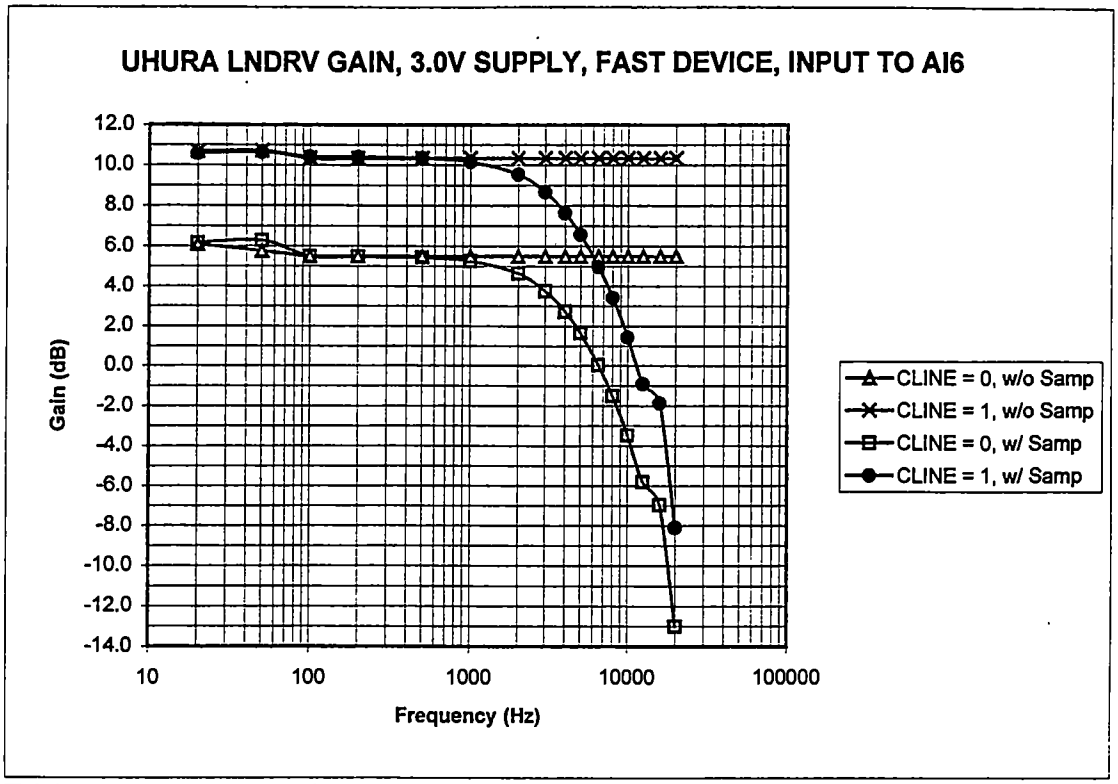


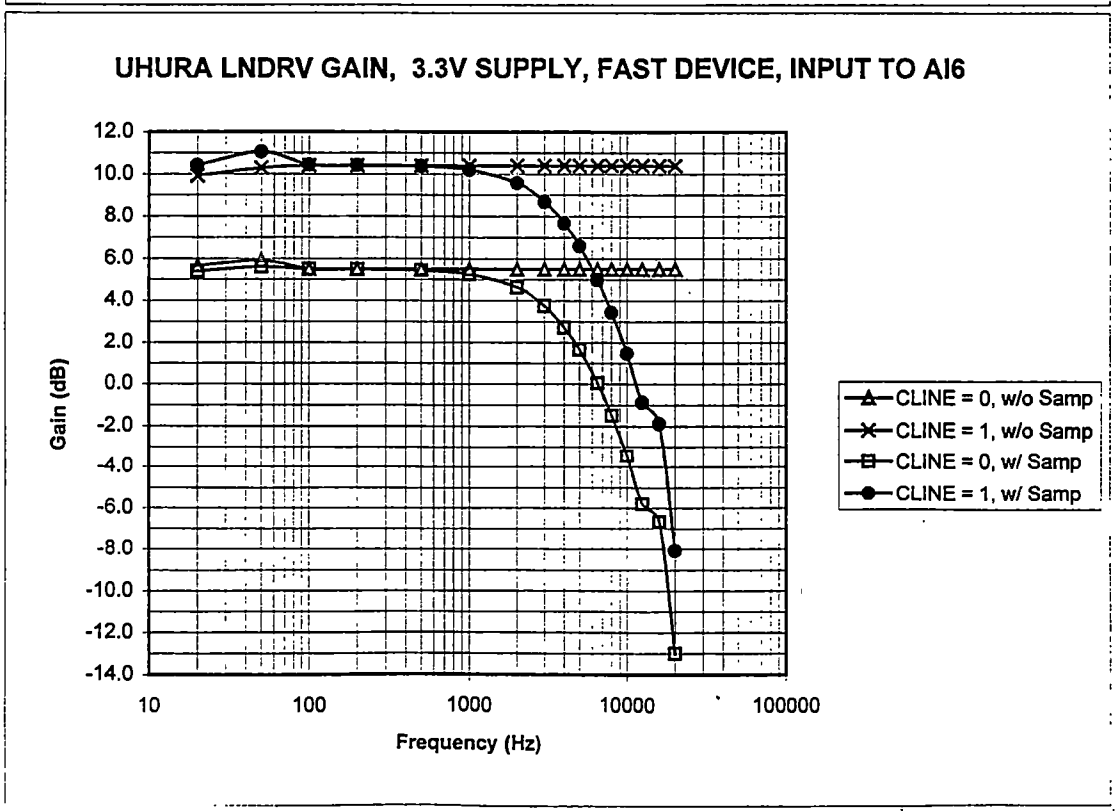
UHURA LNDRV GAIN, 3.3V SUPPLY, NOMINAL DEVICE, INPUT TO AI6

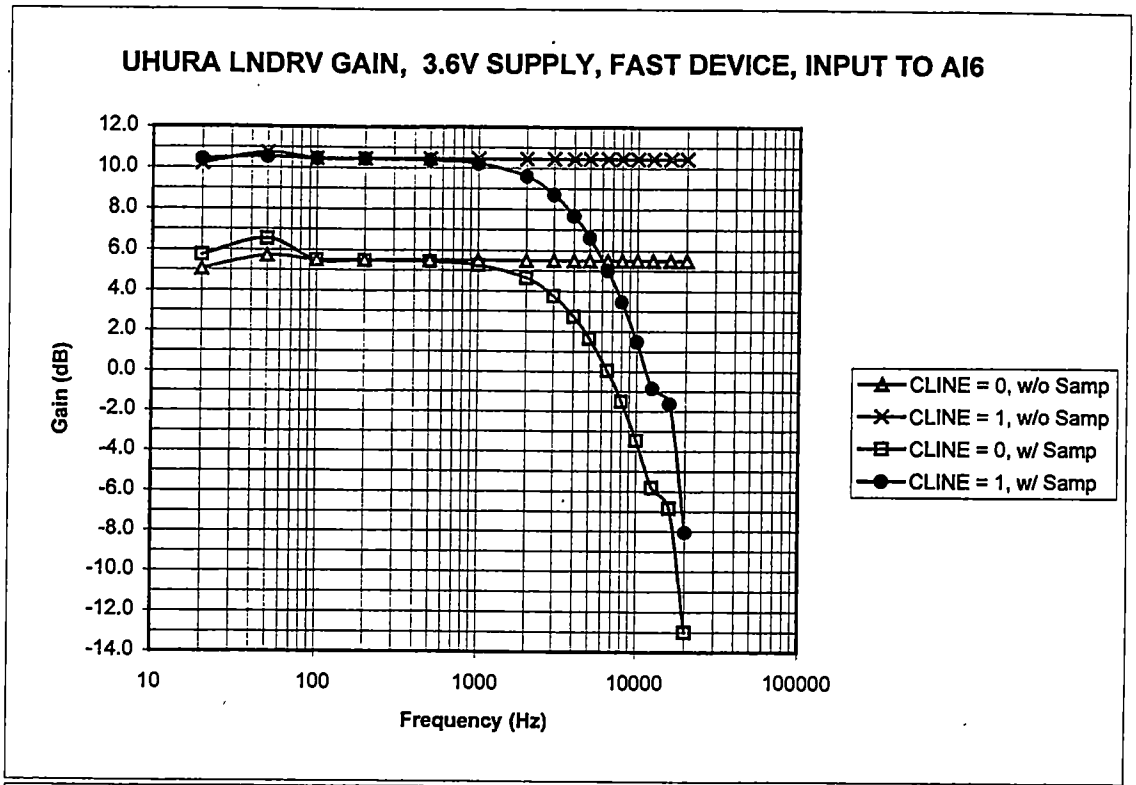


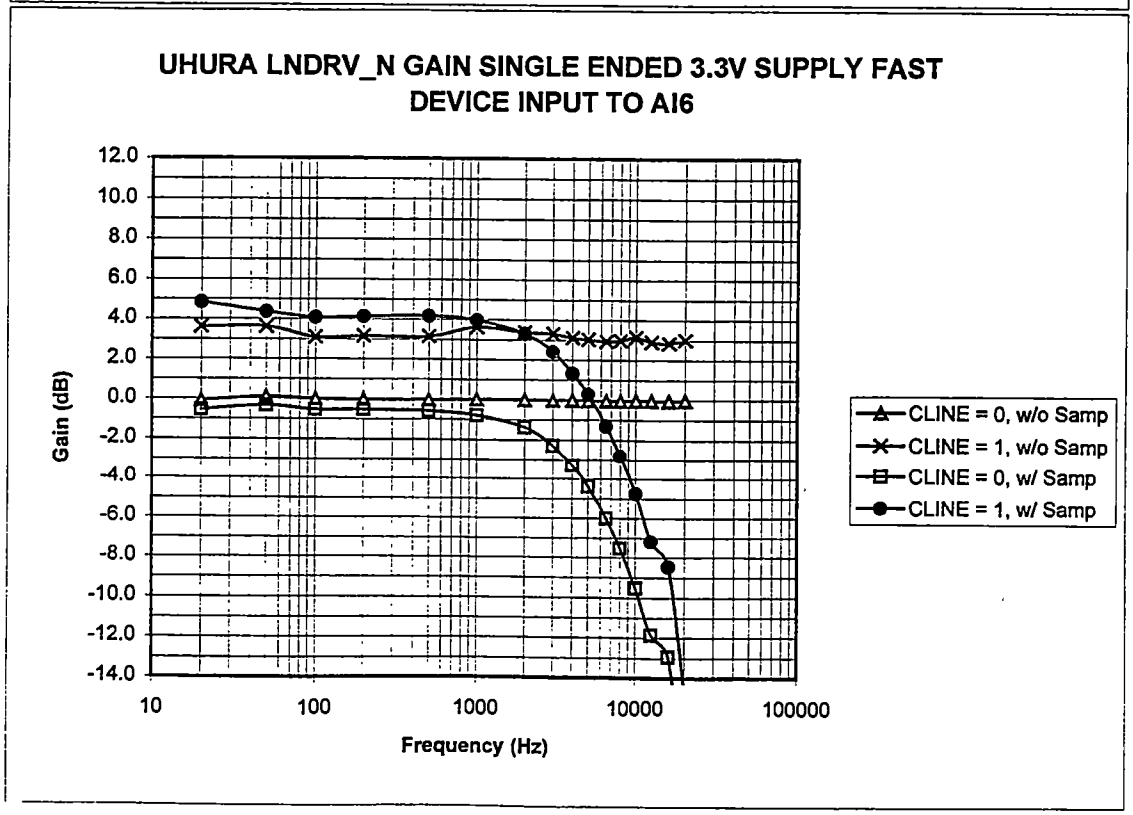

UHURA LNDRV GAIN, 3.6V SUPPLY, NOMINAL DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp


UHURA LNDRV_N GAIN, SINGLE ENDED, 3.3V SUPPLY, NOMINAL DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

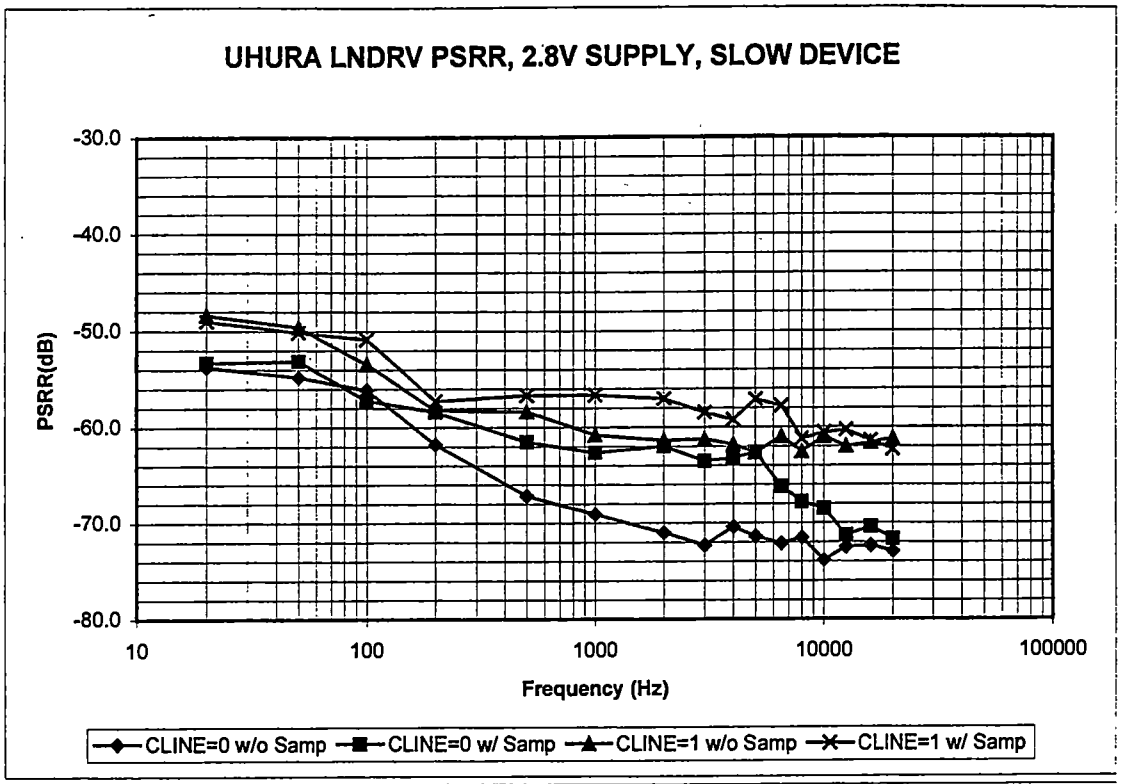

UHURA LNDRV GAIN, 3.0V SUPPLY, FAST DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

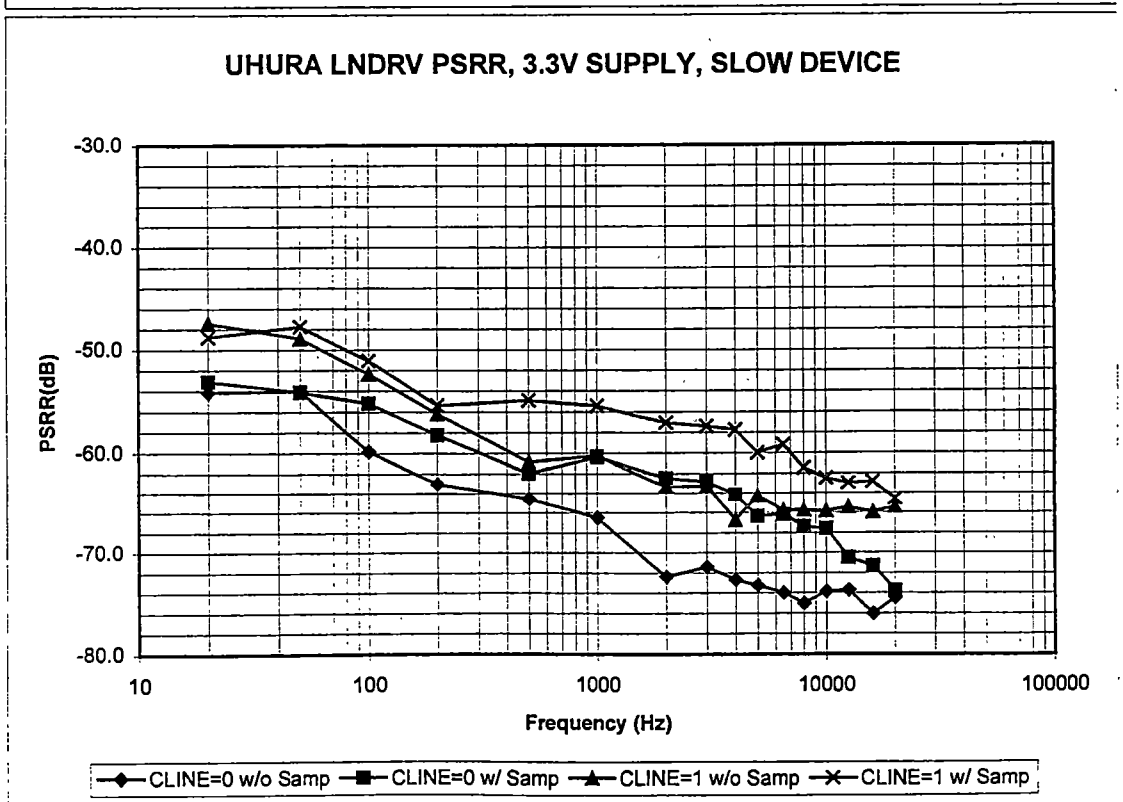

UHURA LNDRV GAIN, 3.3V SUPPLY, FAST DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

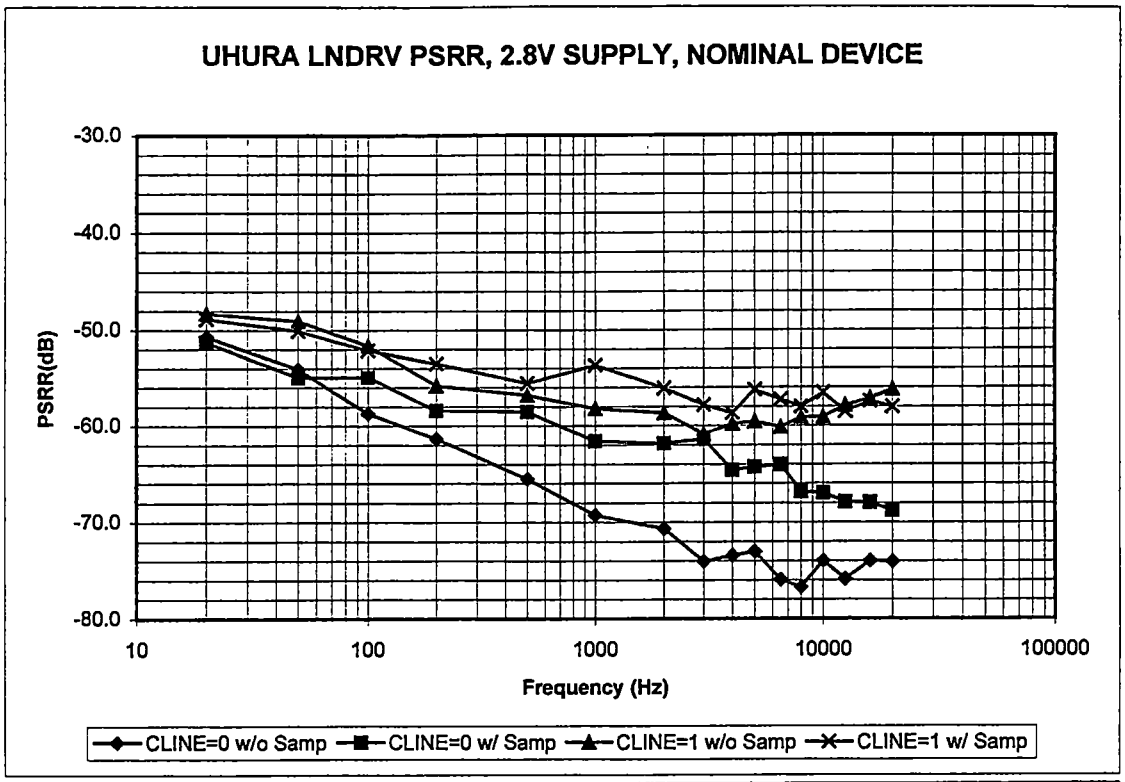

UHURA LNDRV GAIN, 3.6V SUPPLY, FAST DEVICE, INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

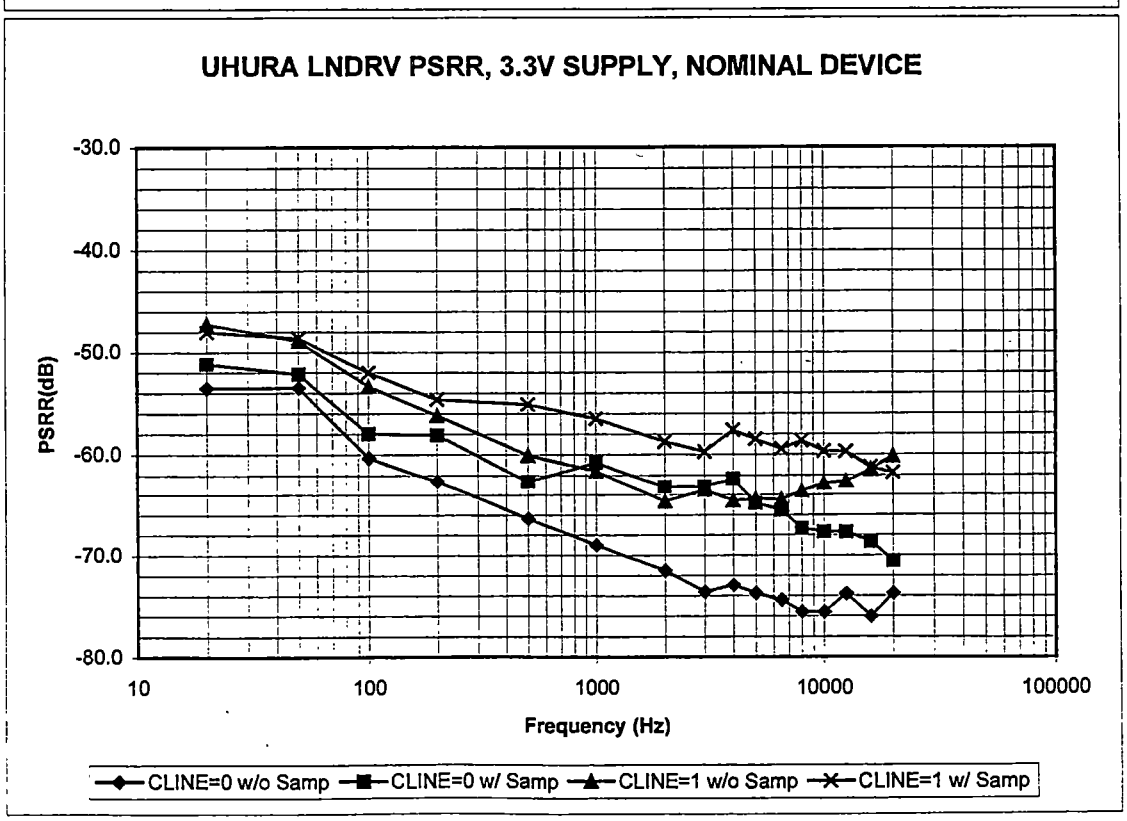

UHURA LNDRV_N GAIN SINGLE ENDED 3.3V SUPPLY FAST DEVICE INPUT TO AI6
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE = 0, w/o Samp
CLINE = 1, w/o Samp
CLINE = 0, w/ Samp
CLINE = 1, w/ Samp

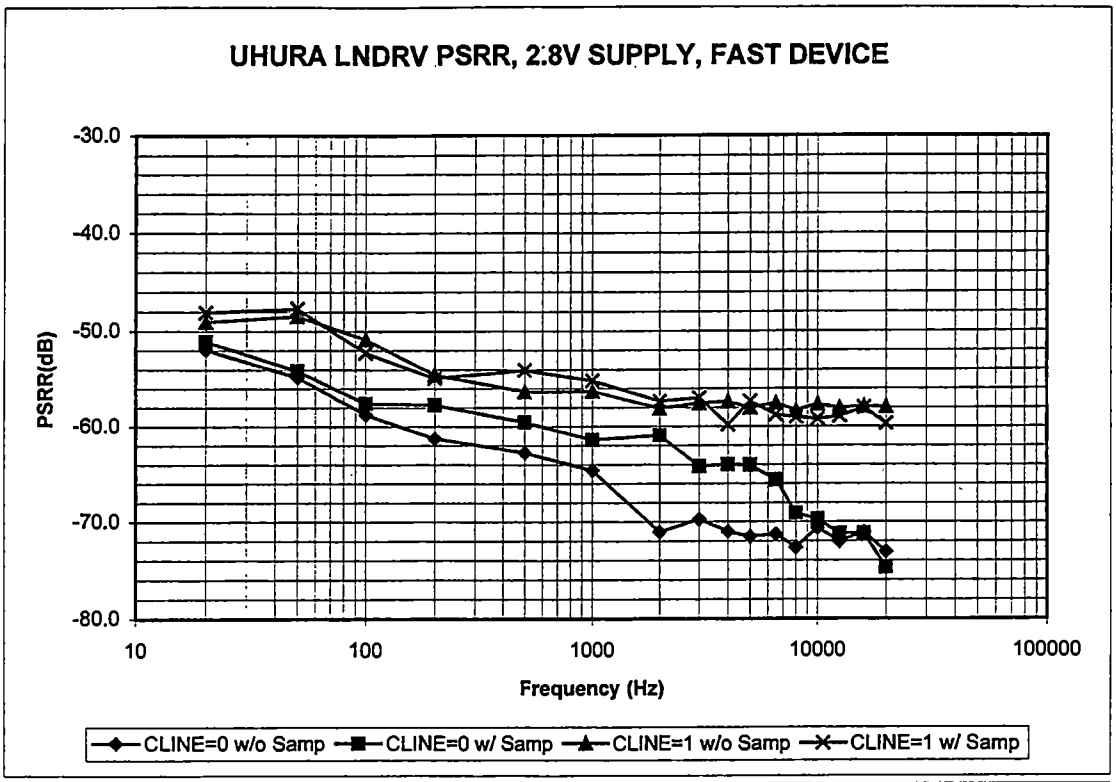
LINE DRIVER PSRR DATA

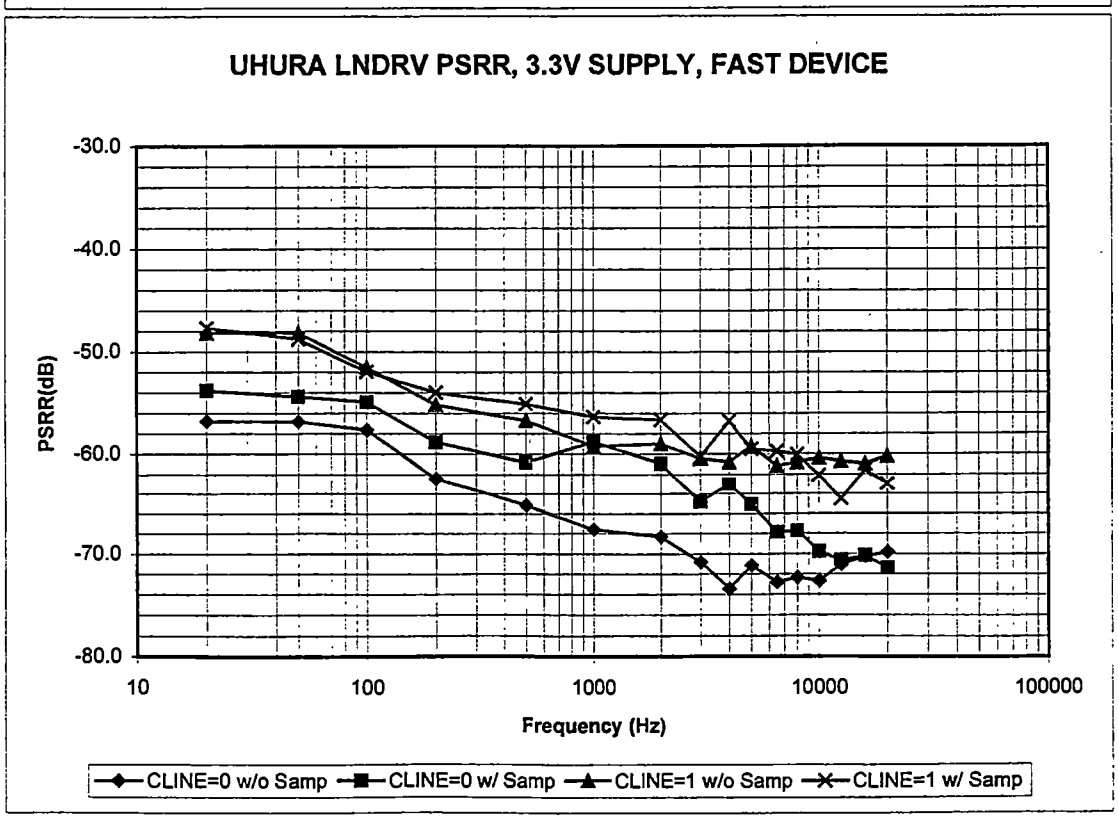

UHURA LNDRV PSRR, 2.8V SUPPLY, SLOW DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

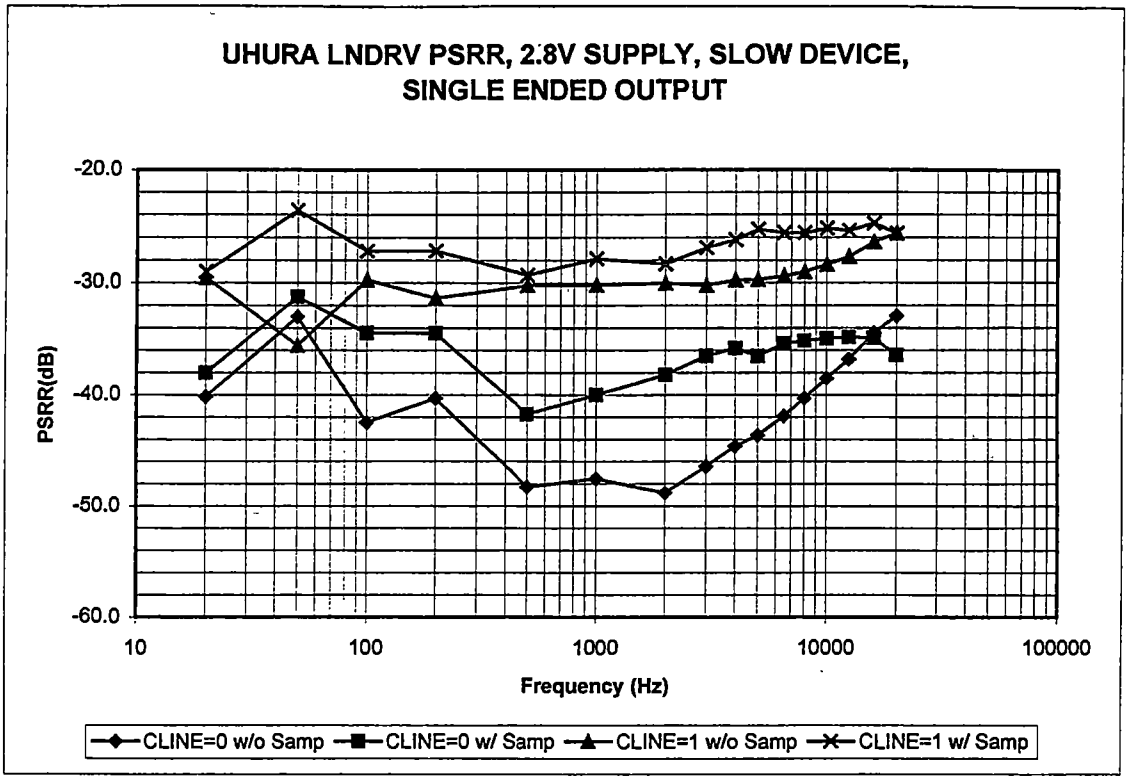

UHURA LNDRV PSRR, 3.3V SUPPLY, SLOW DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

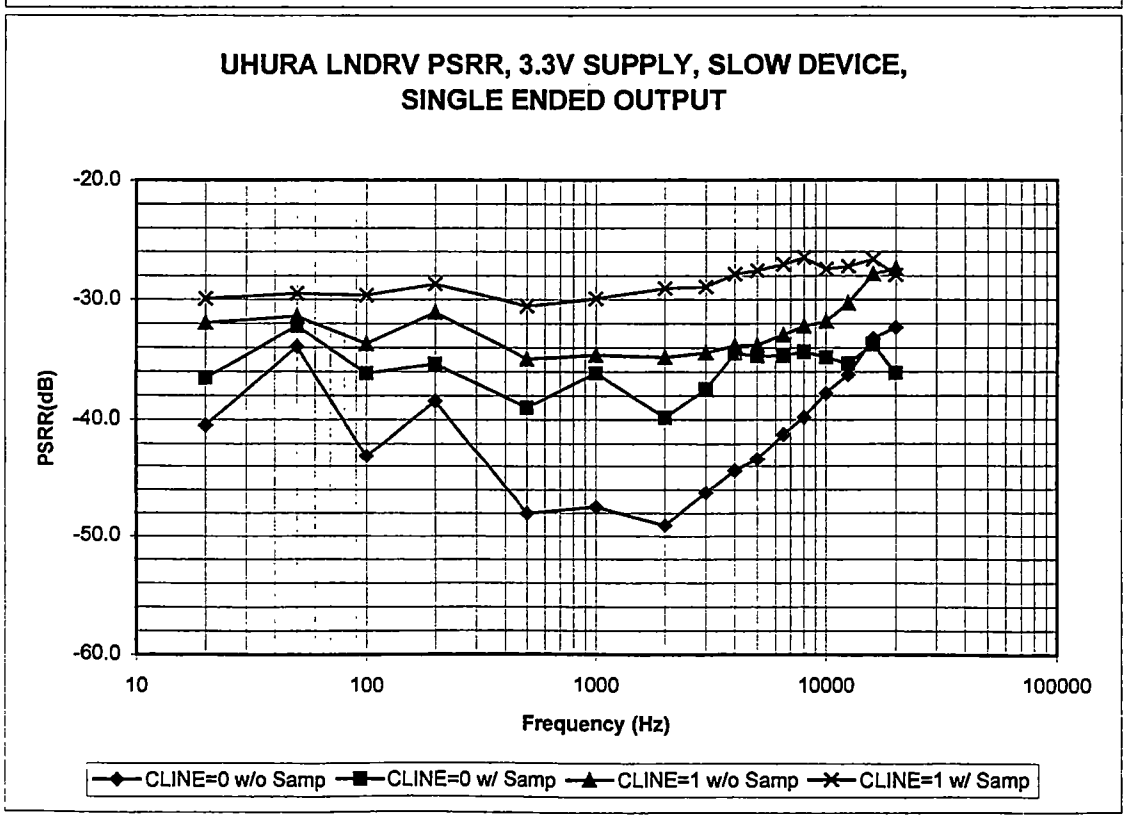

UHURA LNDRV PSRR, 2.8V SUPPLY, NOMINAL DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

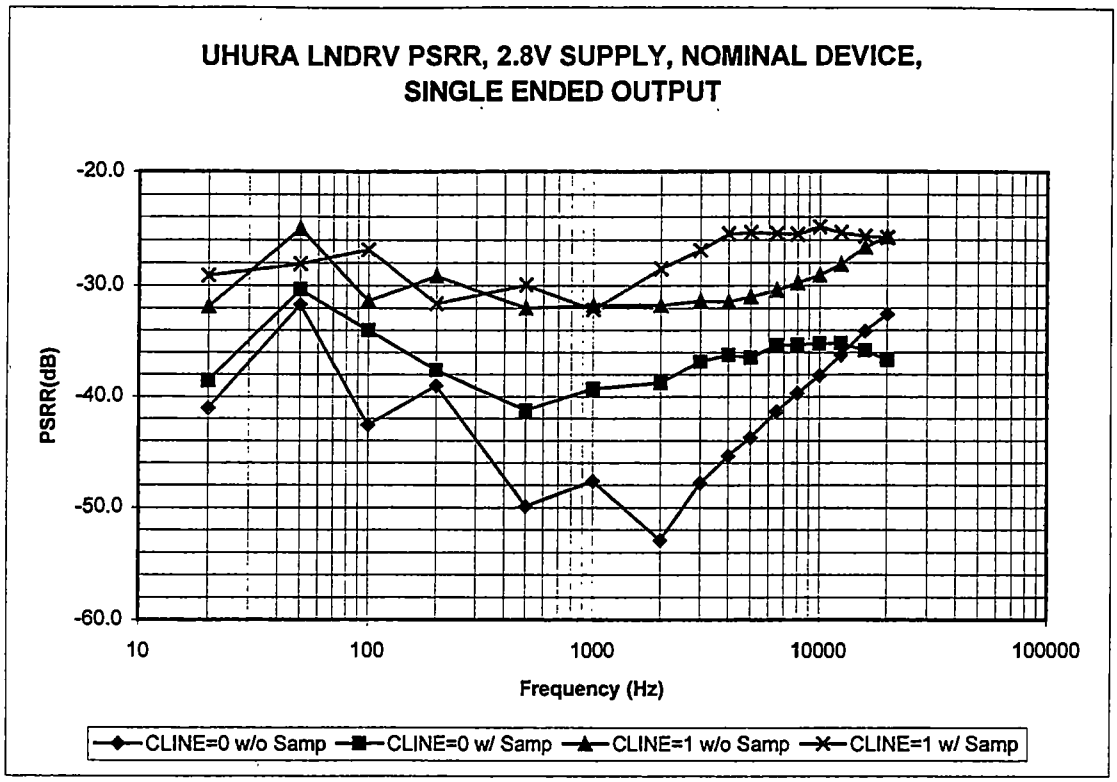

UHURA LNDRV PSRR, 3.3V SUPPLY, NOMINAL DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

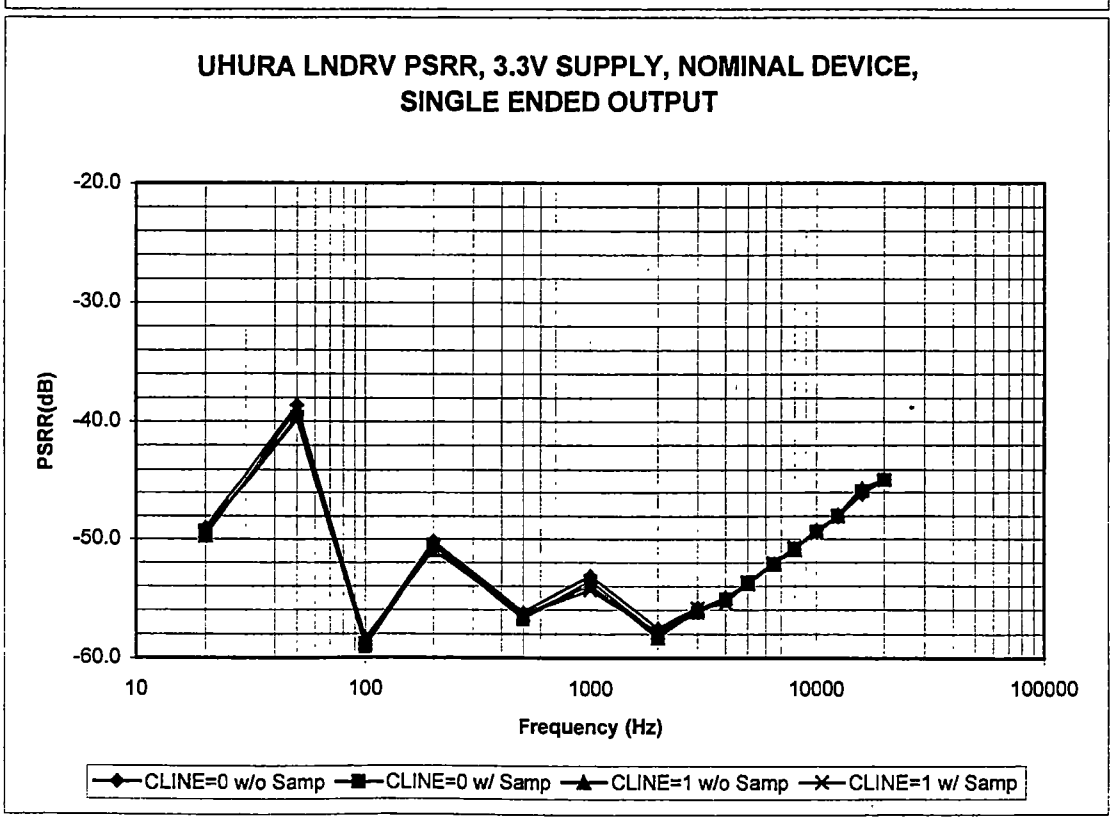

UHURA LNDRV PSRR, 2.8V SUPPLY, FAST DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

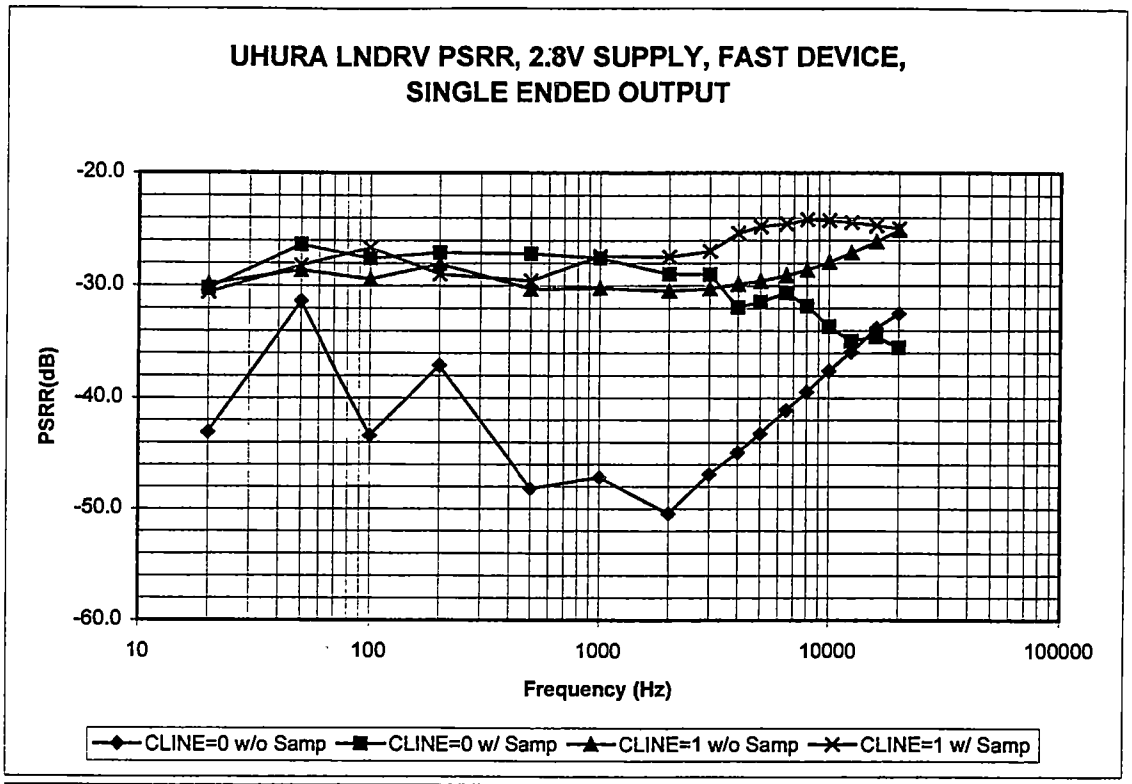

UHURA LNDRV PSRR, 3.3V SUPPLY, FAST DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

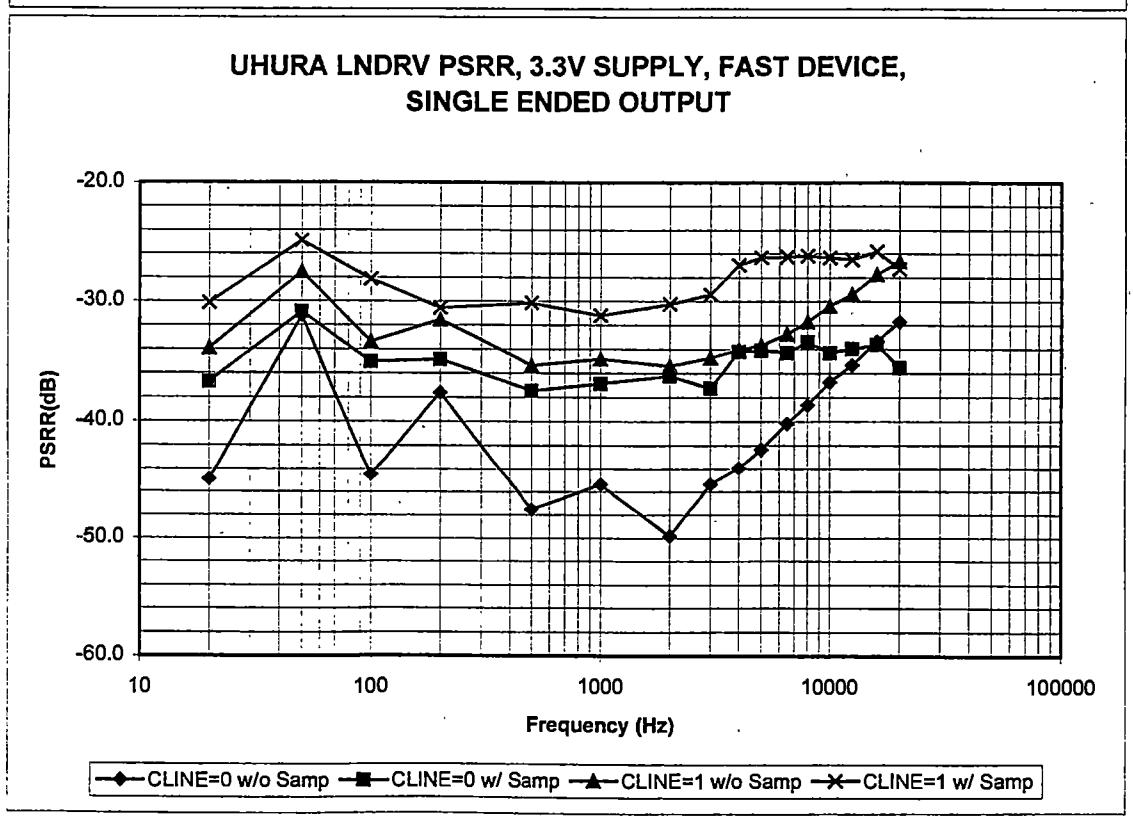

UHURA LNDRV PSRR, 2.8V SUPPLY, SLOW DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp


UHURA LNDRV PSRR, 3.3V SUPPLY, SLOW DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

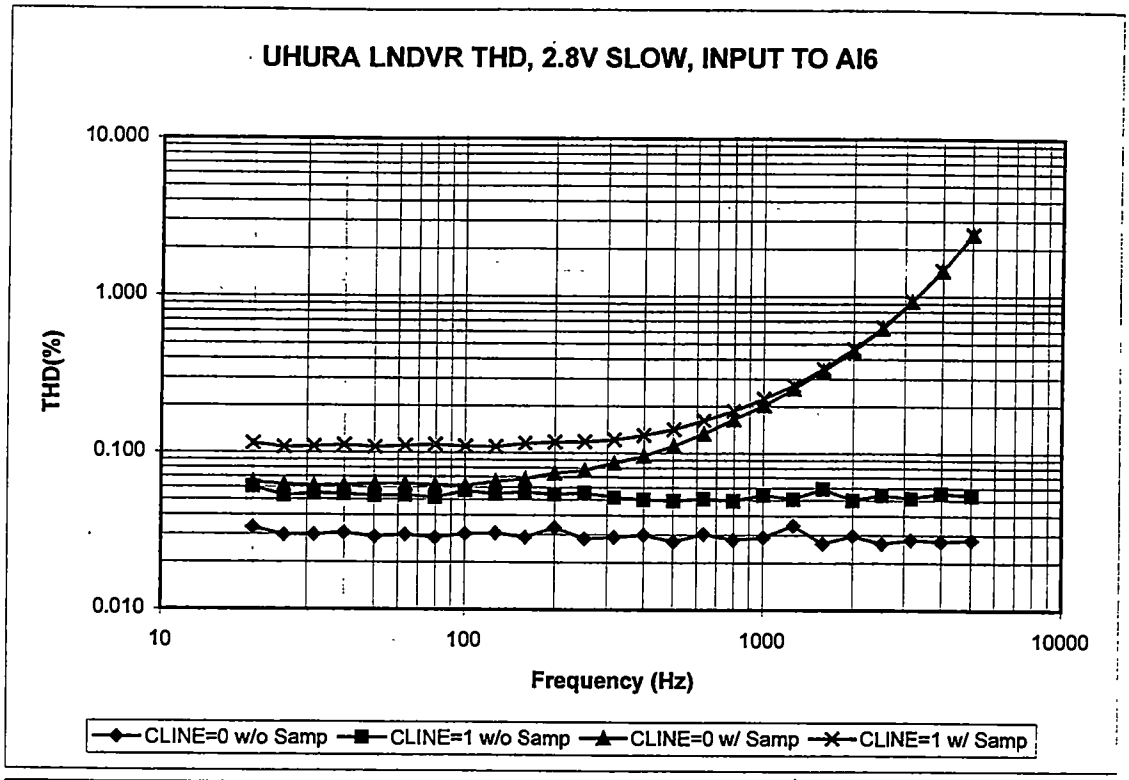

UHURA LNDRV PSRR, 2.8V SUPPLY, NOMINAL DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

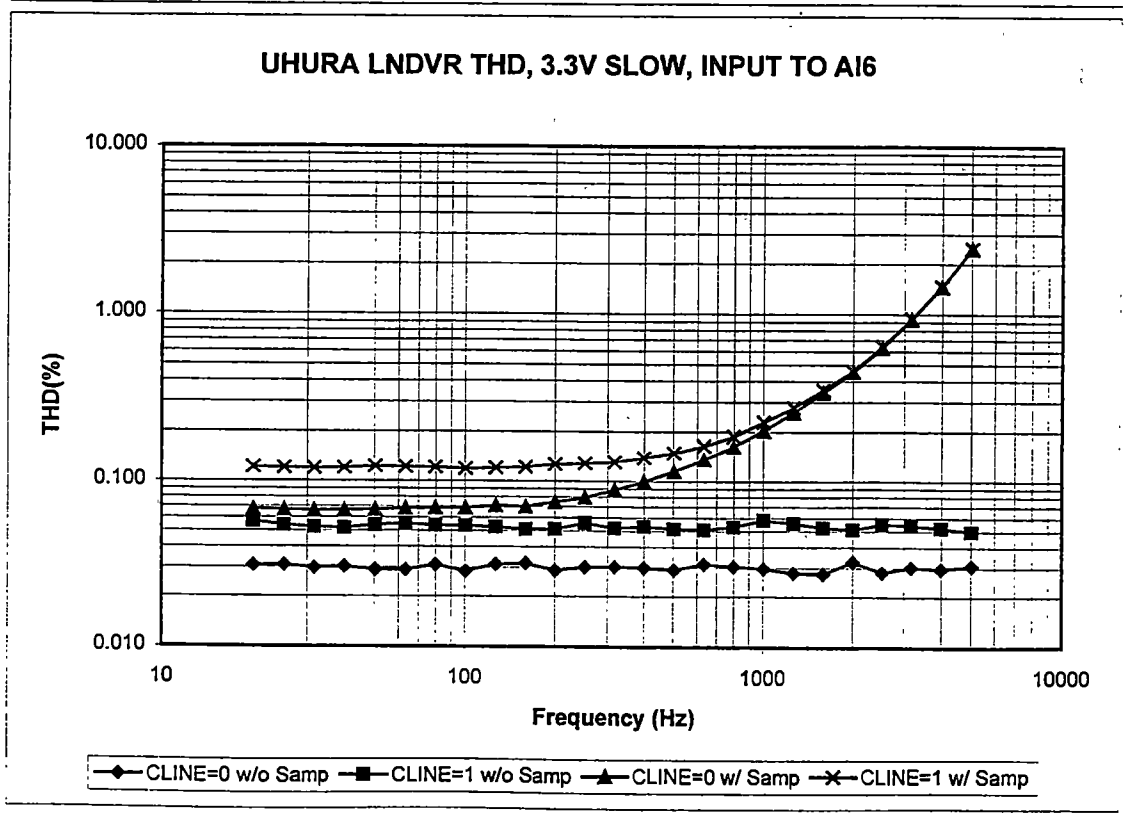

UHURA LNDRV PSRR, 3.3V SUPPLY, NOMINAL DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

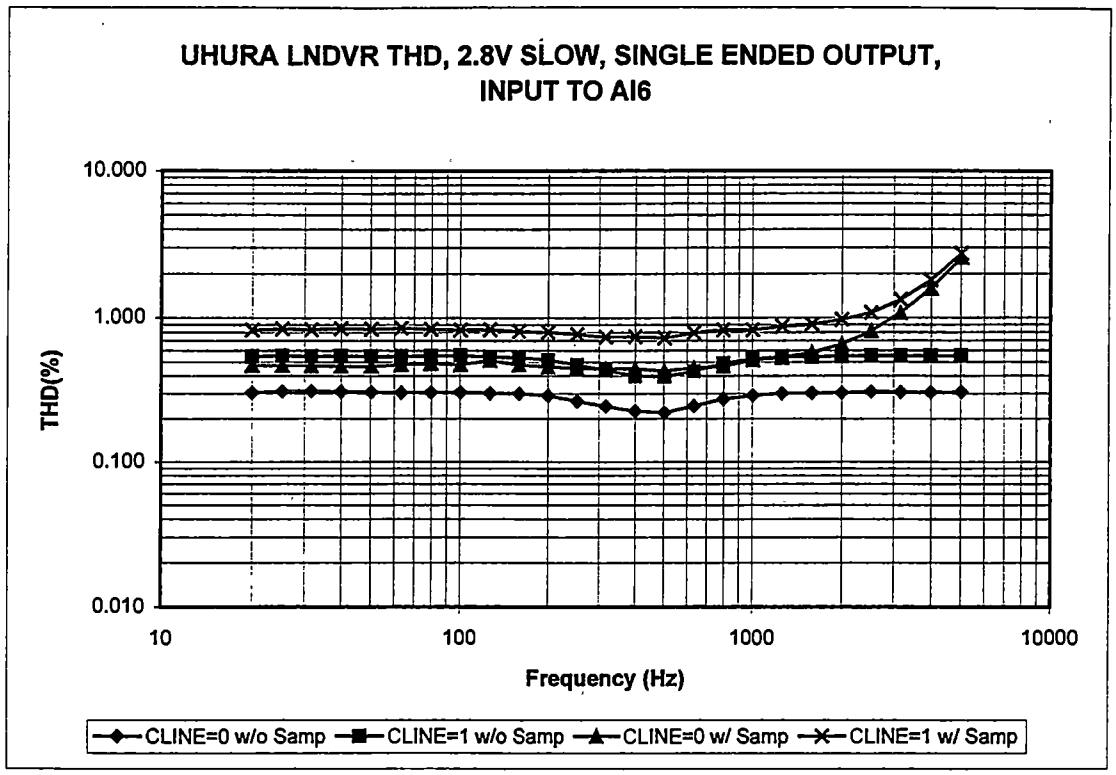

UHURA LNDRV PSRR, 2.8V SUPPLY, FAST DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

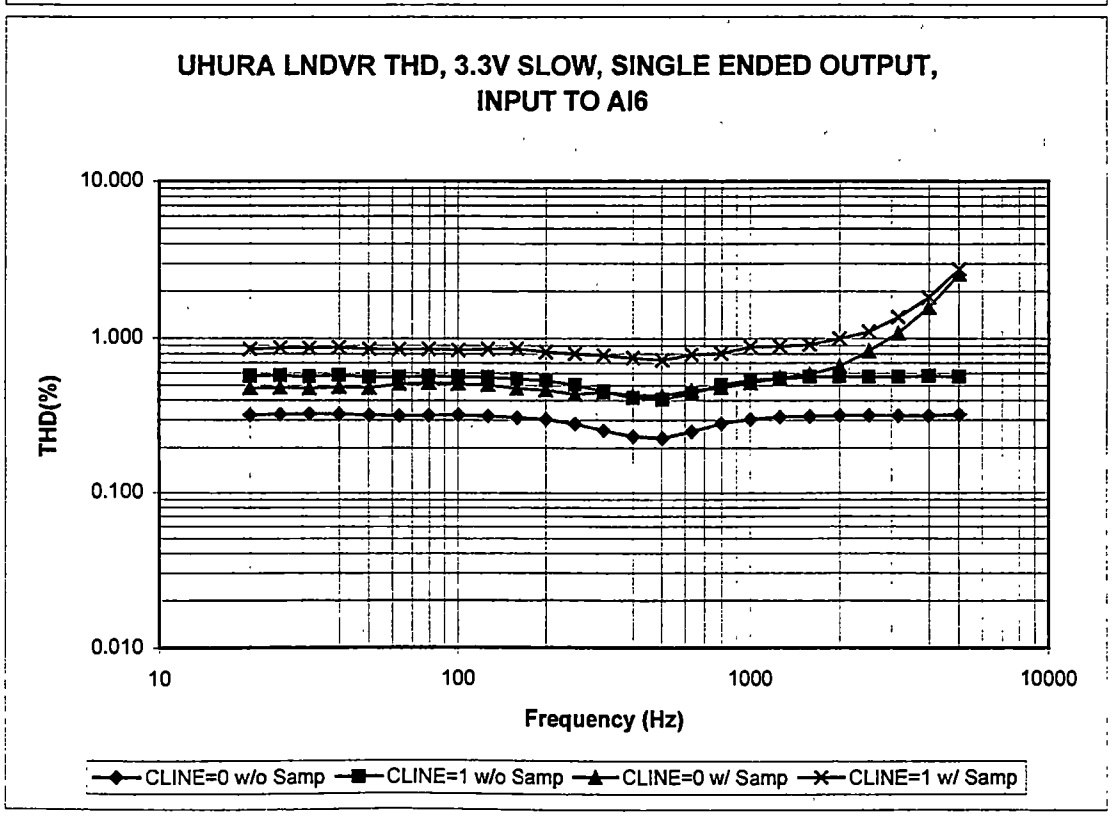

UHURA LNDRV PSRR, 3.3V SUPPLY, FAST DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/o Samp
CLINE=1 w/ Samp

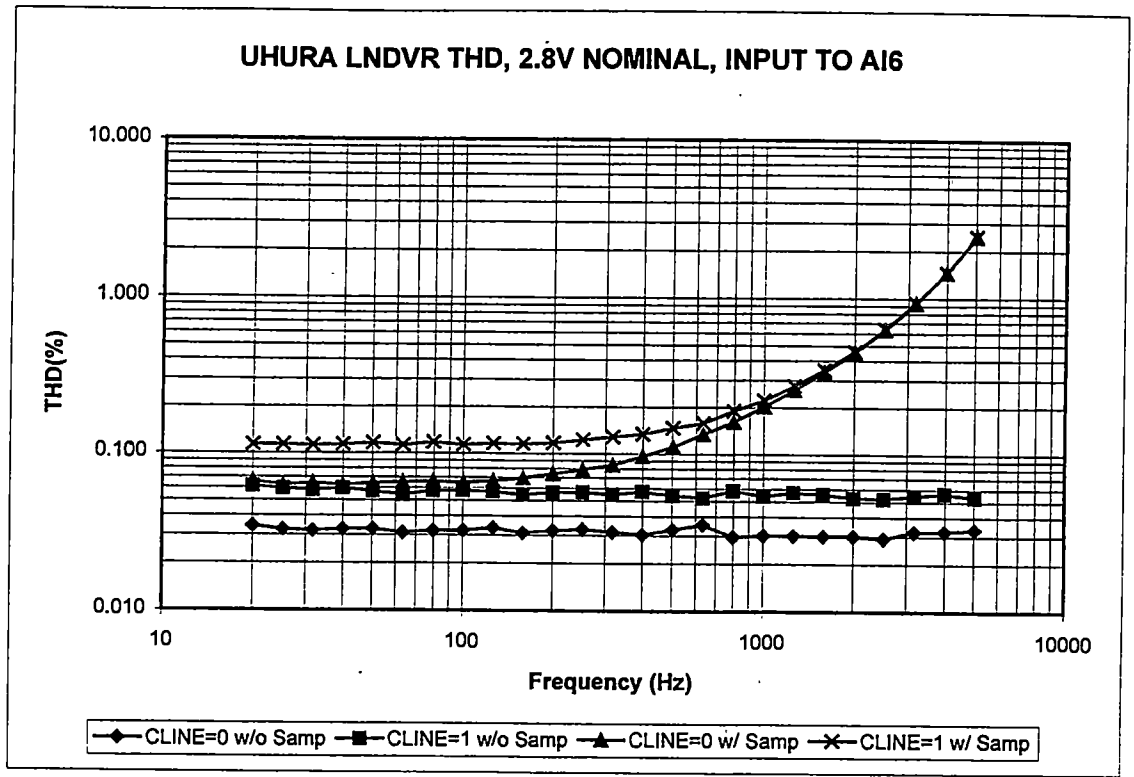
LINE DRIVER THD DATA

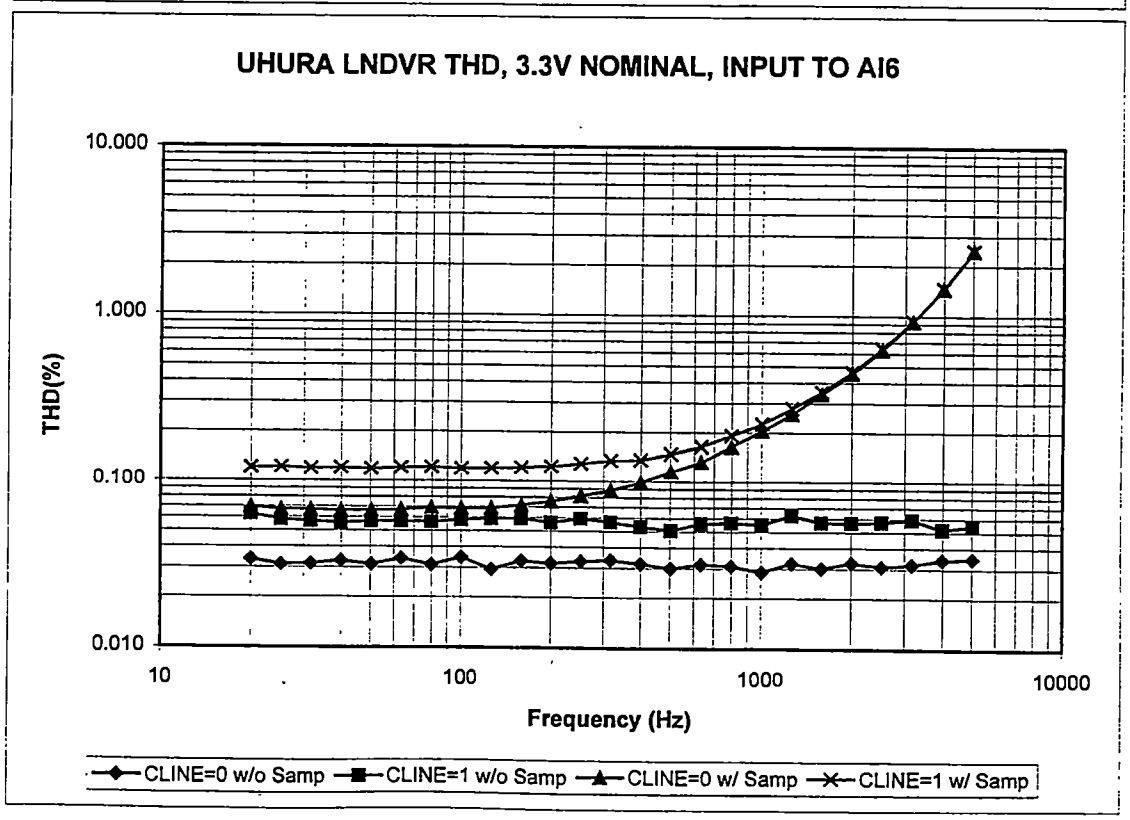

UHURA LNDVR THD, 2.8V SLOW, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

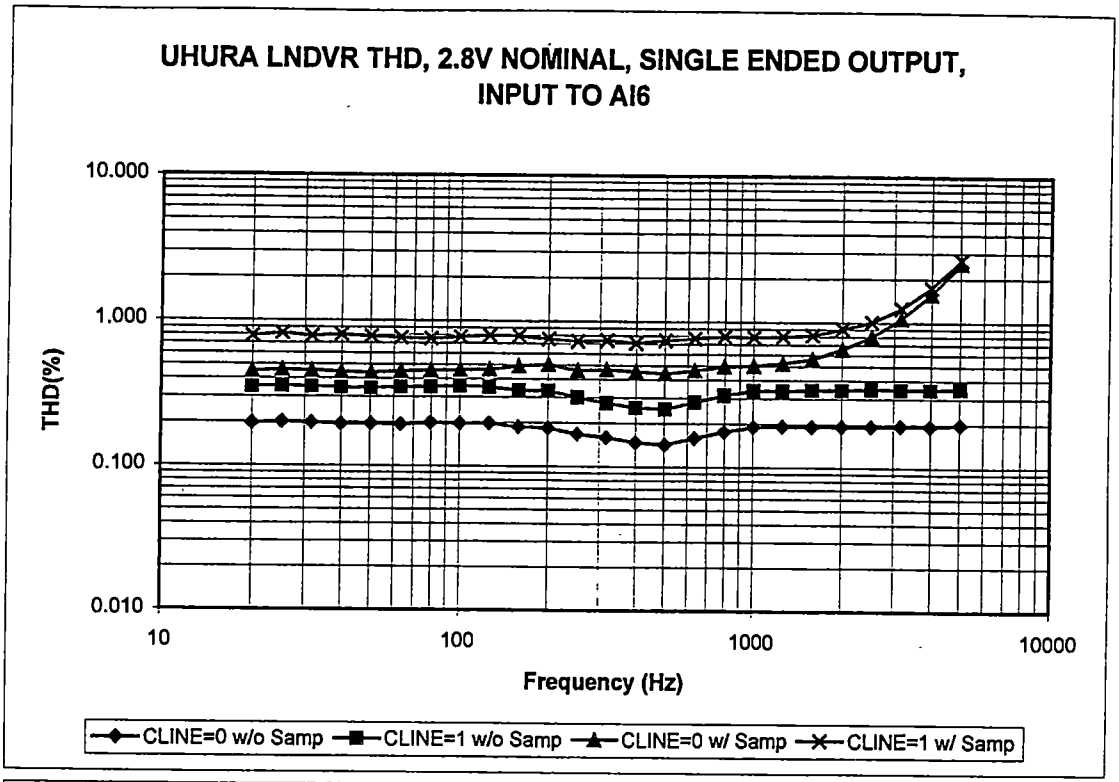

UHURA LNDVR THD, 3.3V SLOW, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

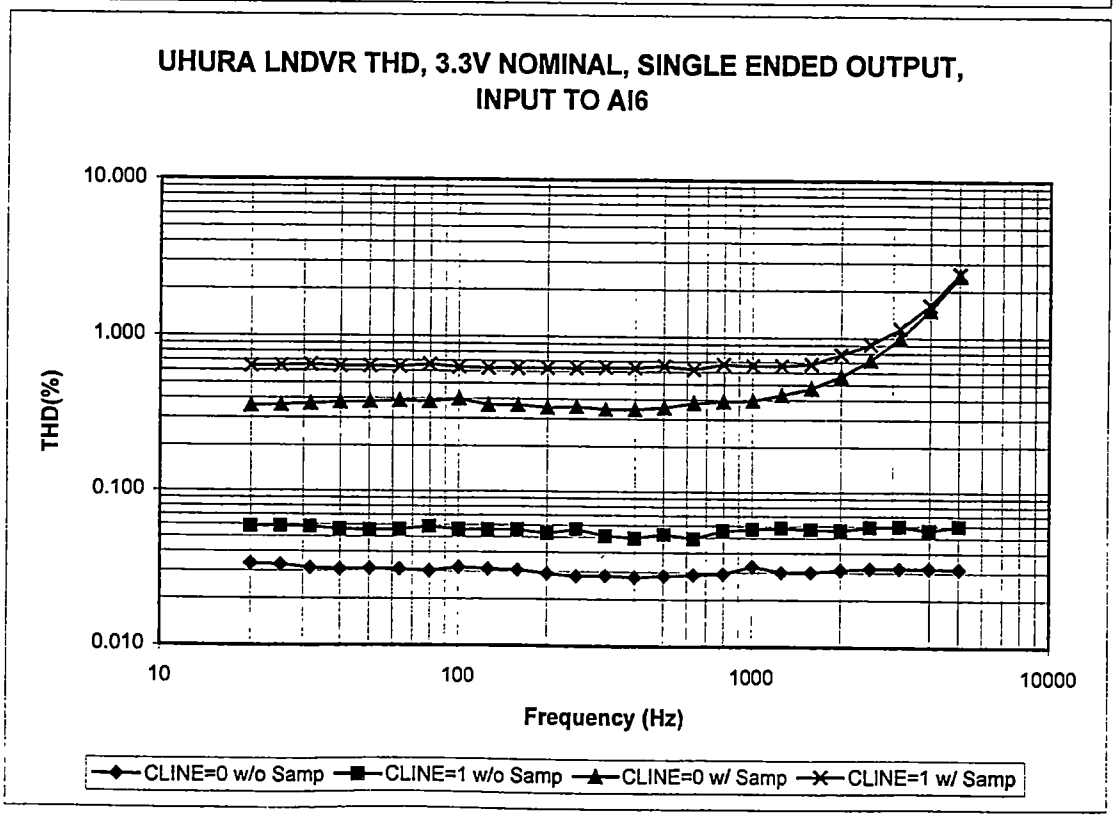

UHURA LNDVR THD, 2.8V SLOW, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

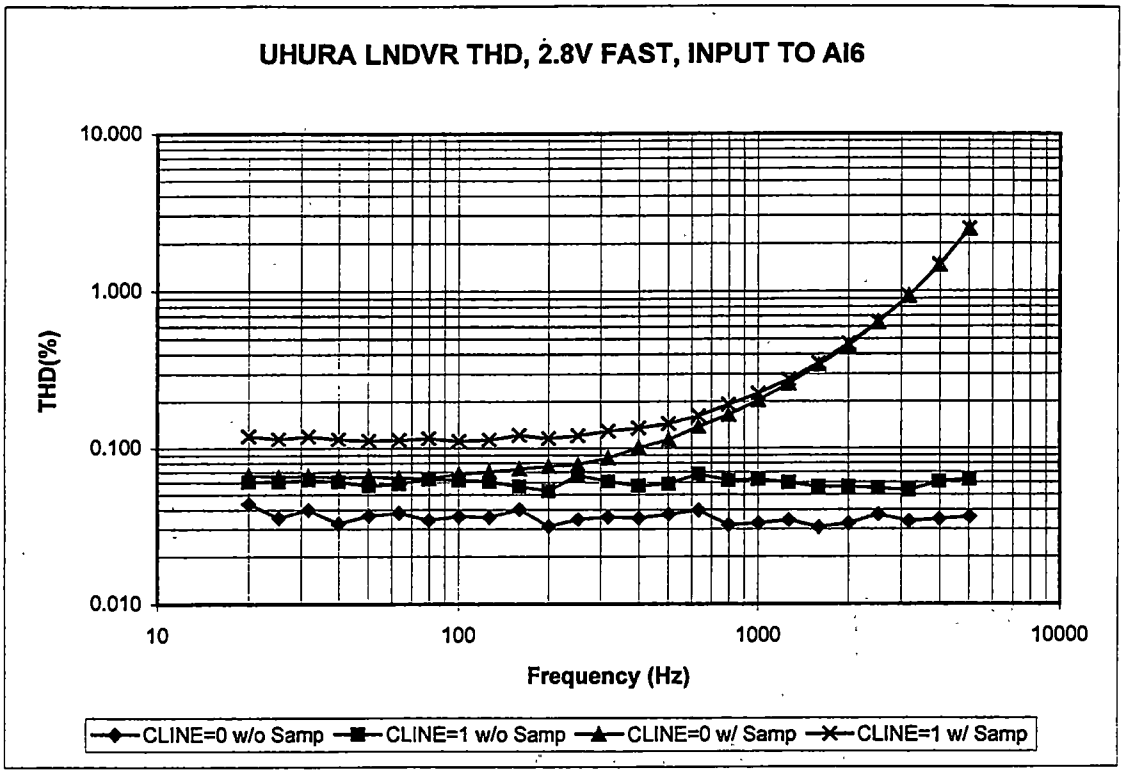

UHURA LNDVR THD, 3.3V SLOW, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

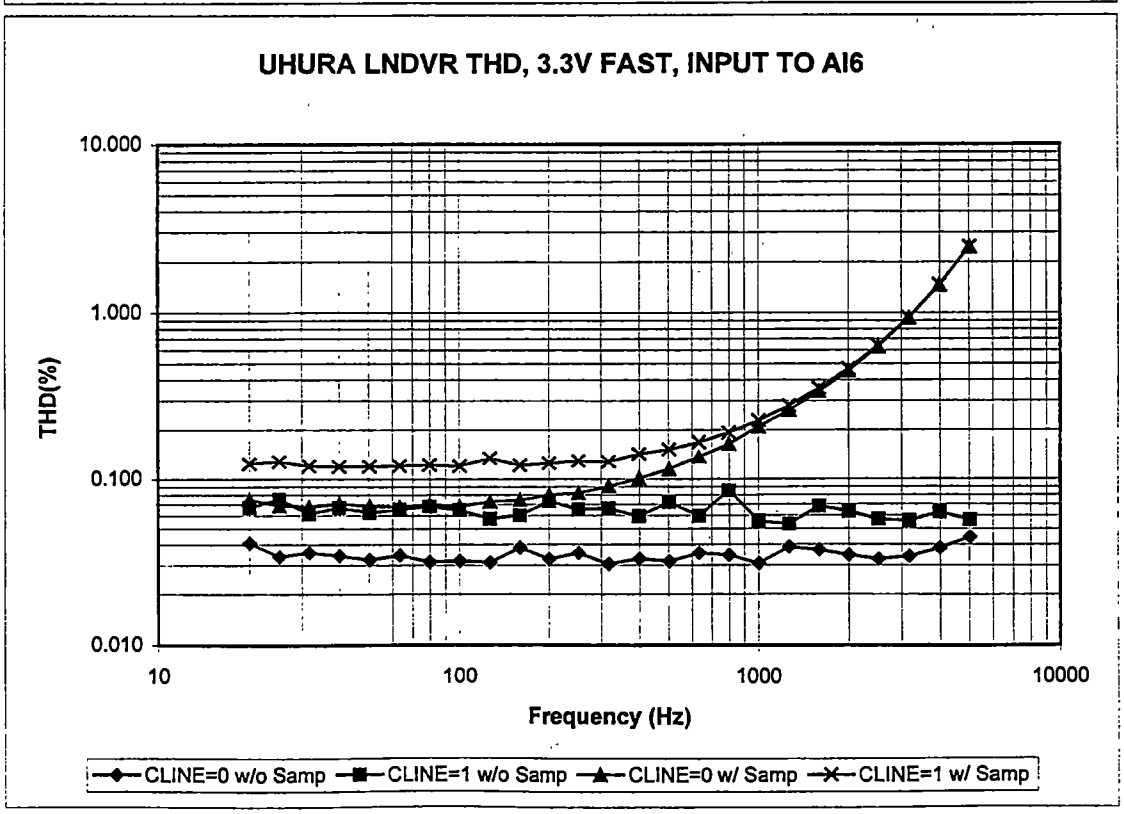

UHURA LNDVR THD, 2.8V NOMINAL, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

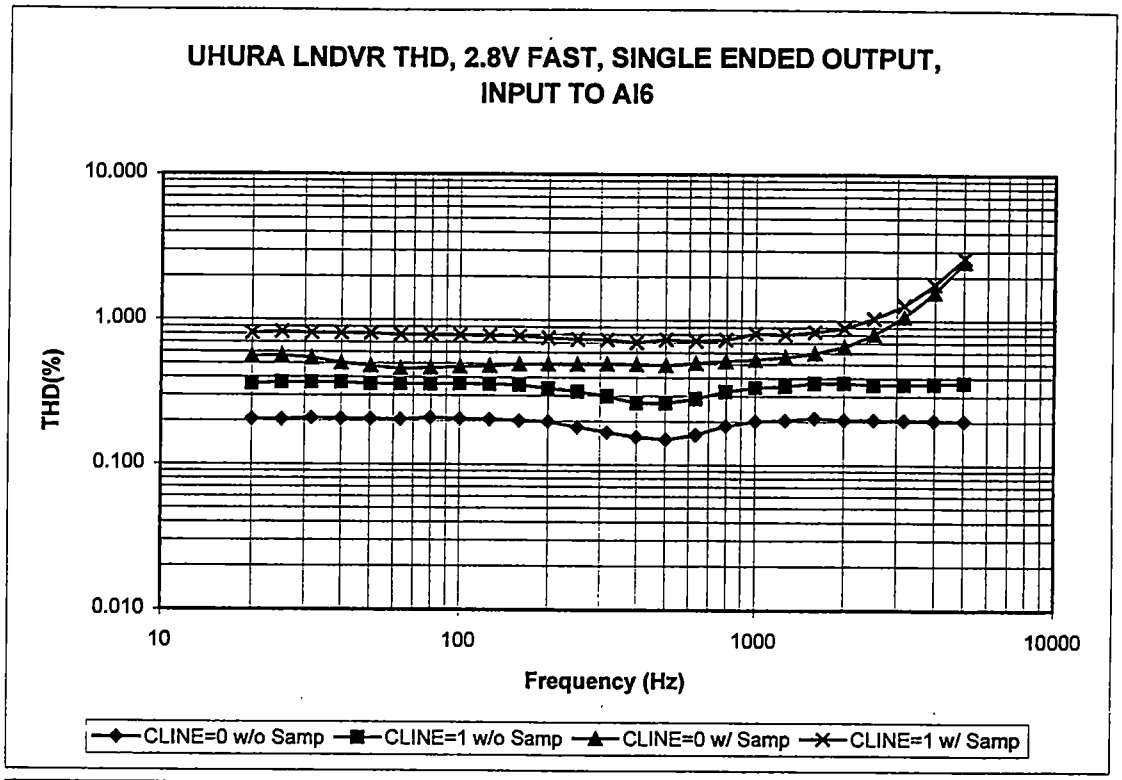

UHURA LNDVR THD, 3.3V NOMINAL, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

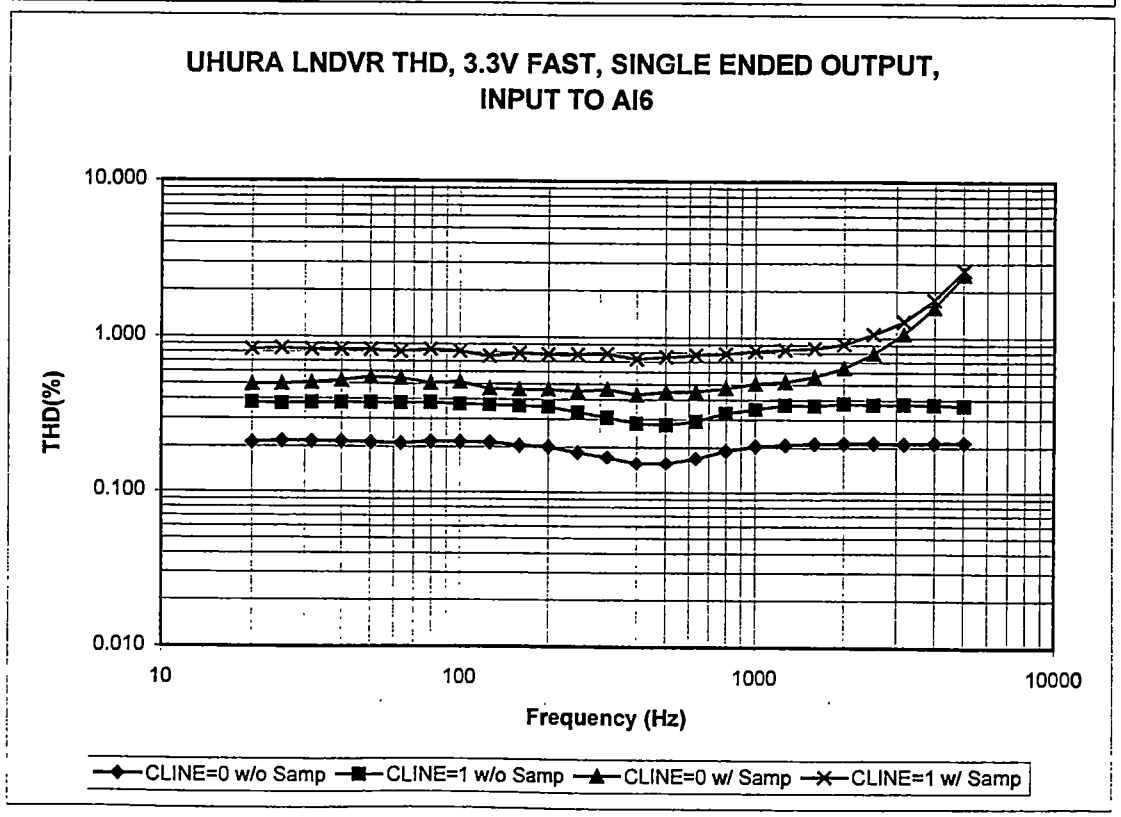

UHURA LNDVR THD, 2.8V NOMINAL, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp


UHURA LNDVR THD, 3.3V NOMINAL, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp


UHURA LNDVR THD, 2.8V FAST, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

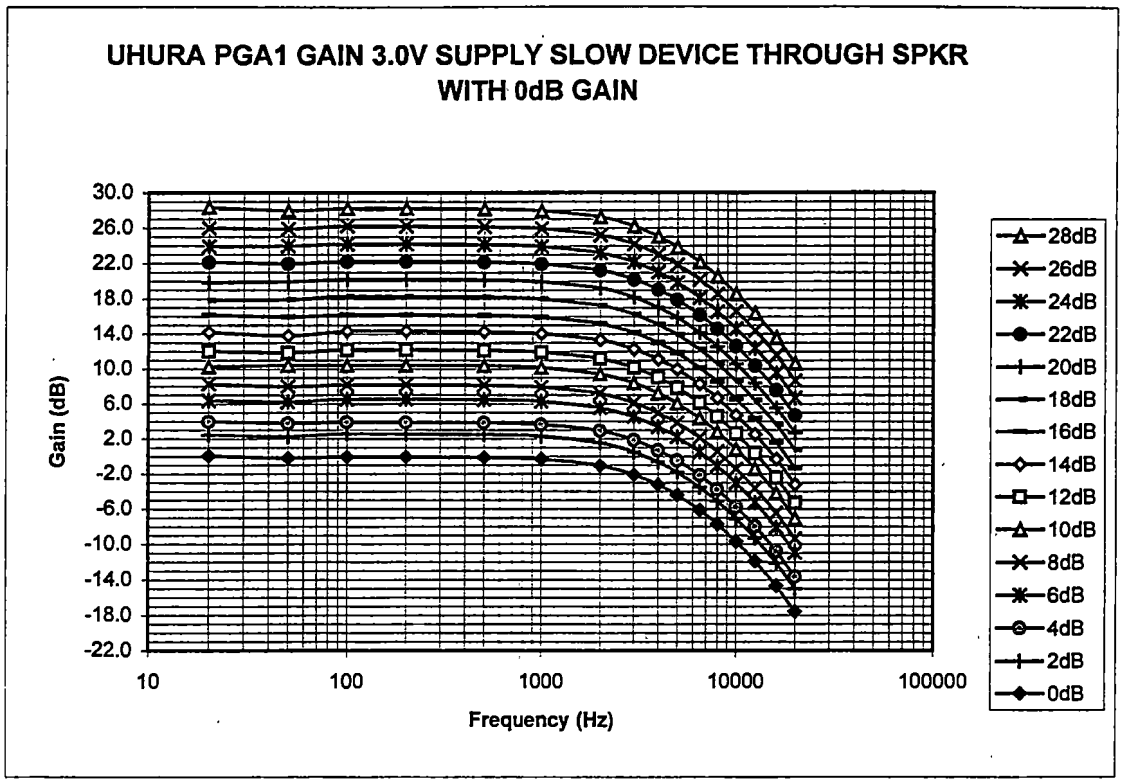

UHURA LNDVR THD, 3.3V FAST, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

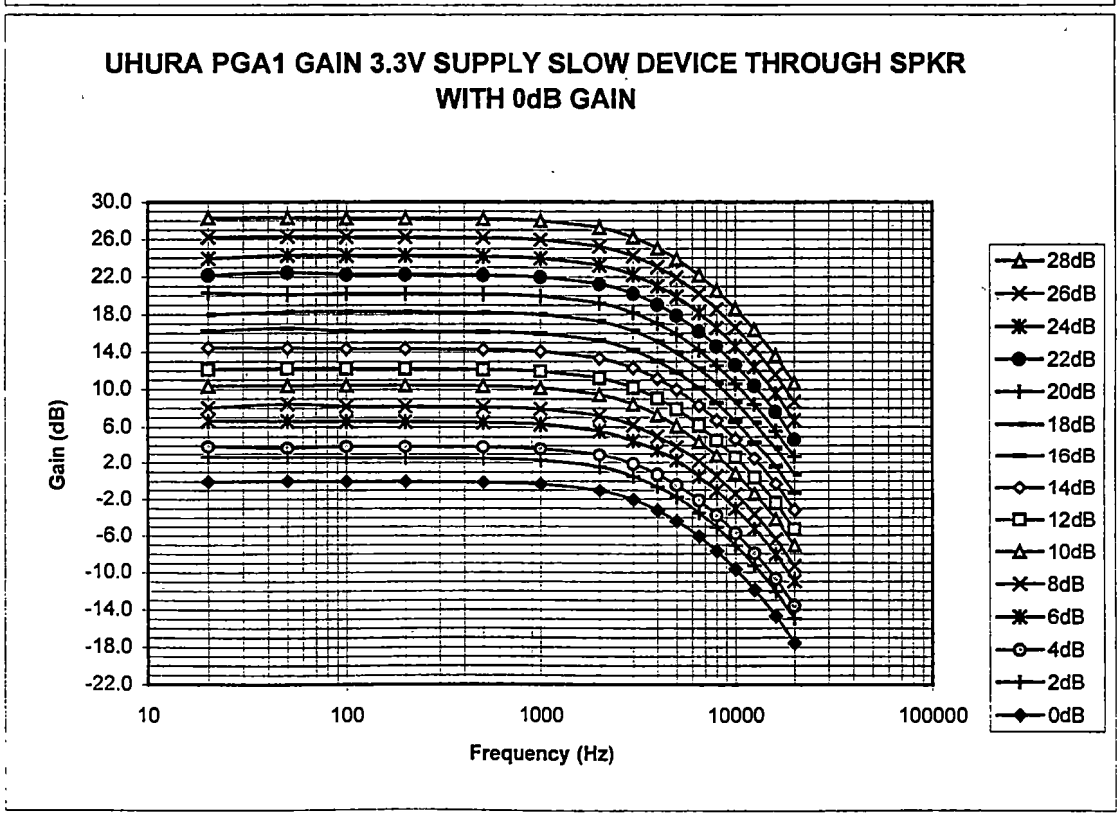

UHURA LNDVR THD, 2.8V FAST, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

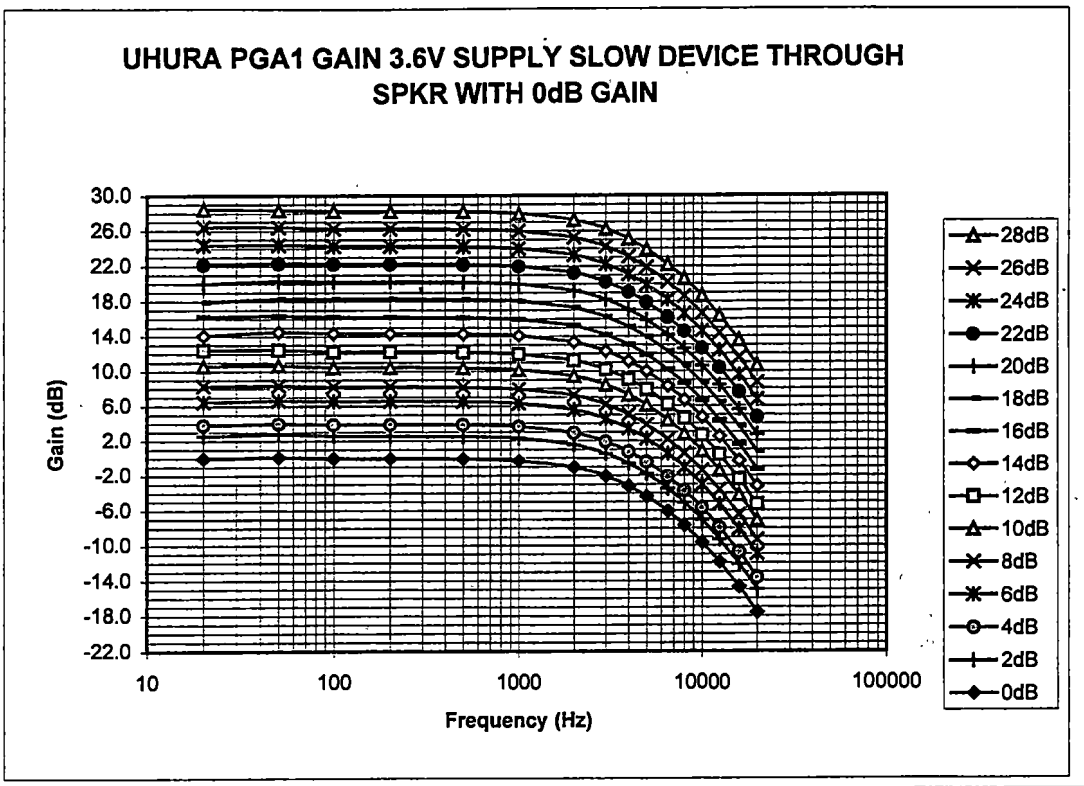

UHURA LNDVR THD, 3.3V FAST, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
CLINE=0 w/o Samp
CLINE=1 w/o Samp
CLINE=0 w/ Samp
CLINE=1 w/ Samp

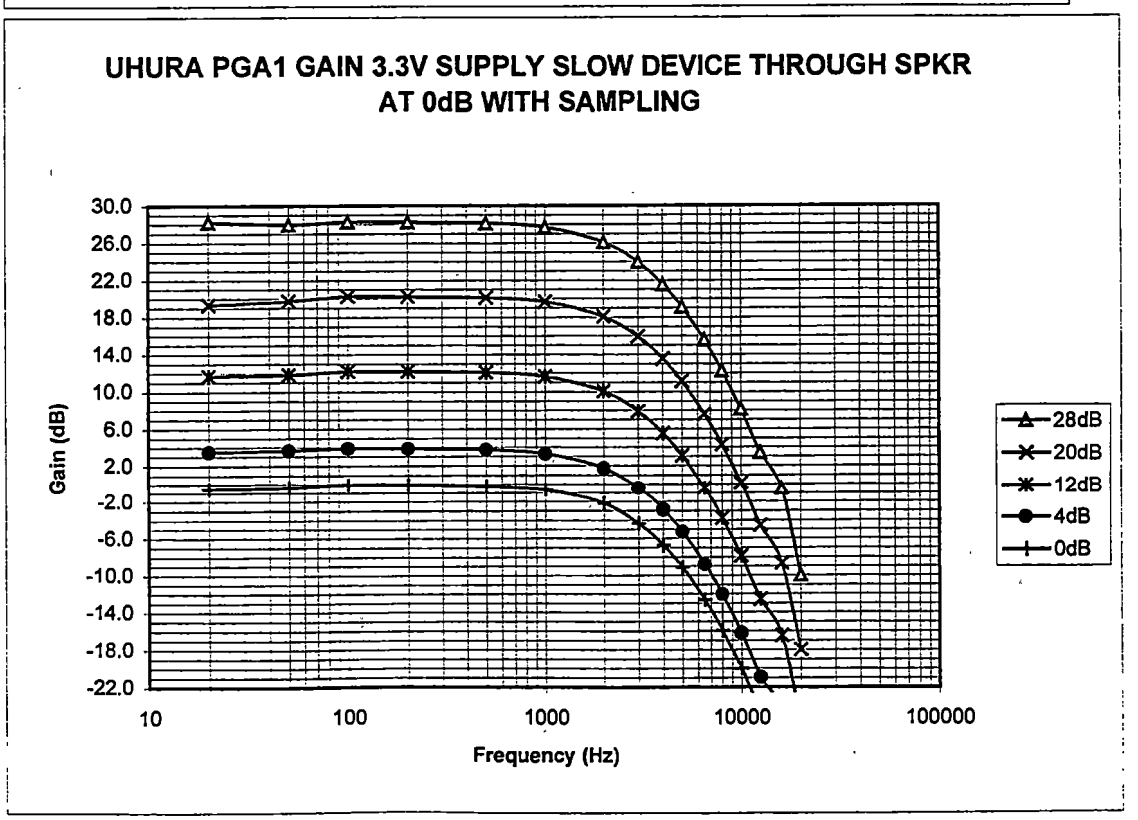
APPENDIX G

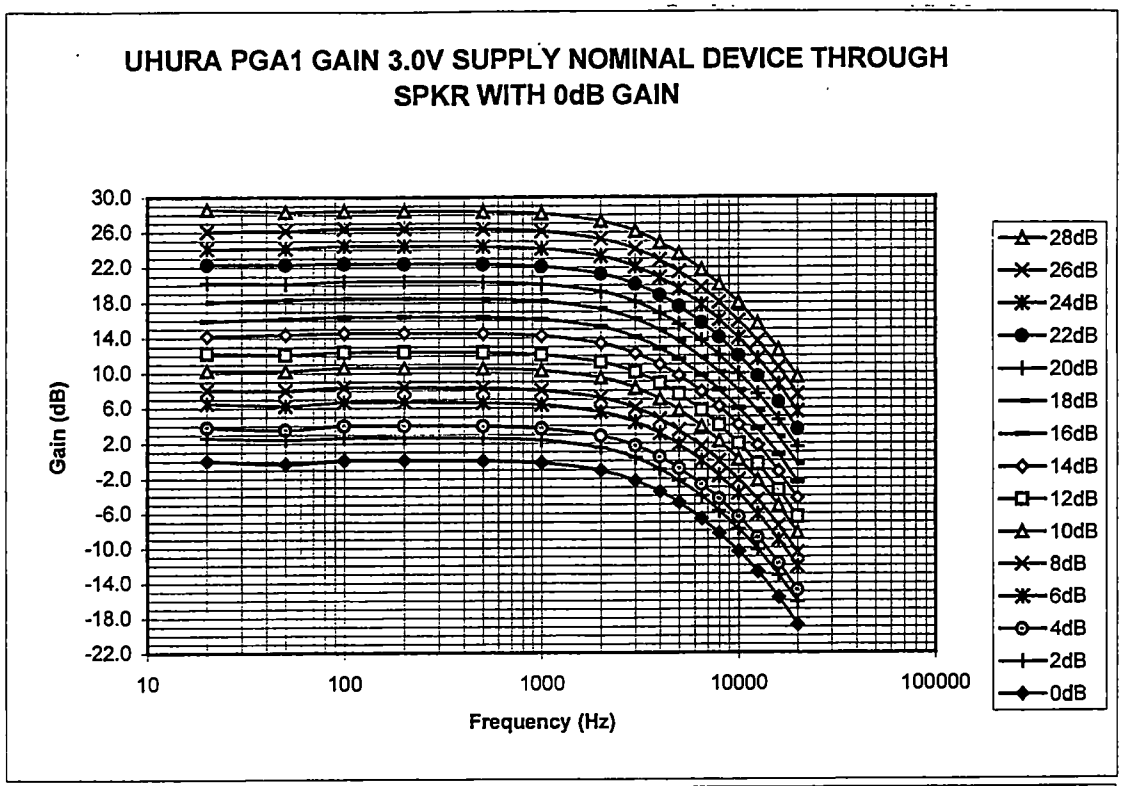
PROGRAMMABLE GAIN AMPLIFIER DATA

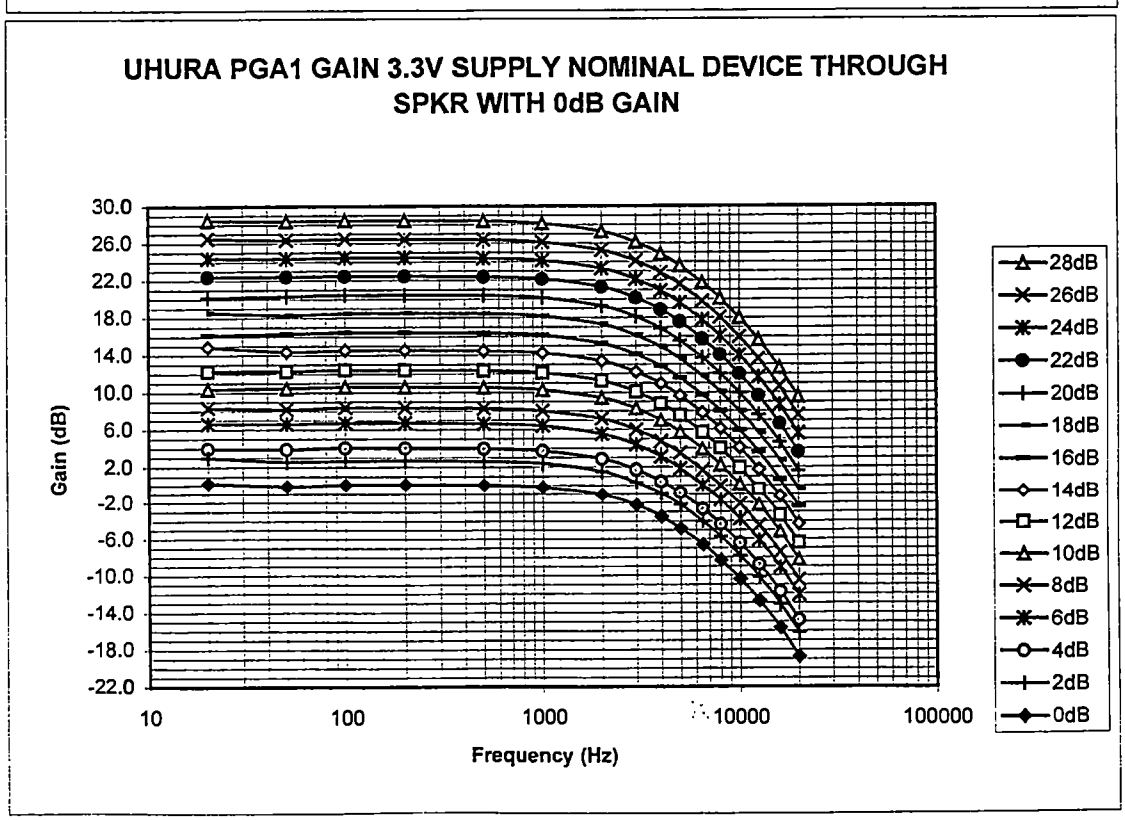

UHURA PGA1 GAIN 3.0V SUPPLY SLOW DEVICE THROUGH SPKR WITH 0dB GAIN
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB


UHURA PGA1 GAIN 3.3V SUPPLY SLOW DEVICE THROUGH SPKR WITH 0dB GAIN
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB

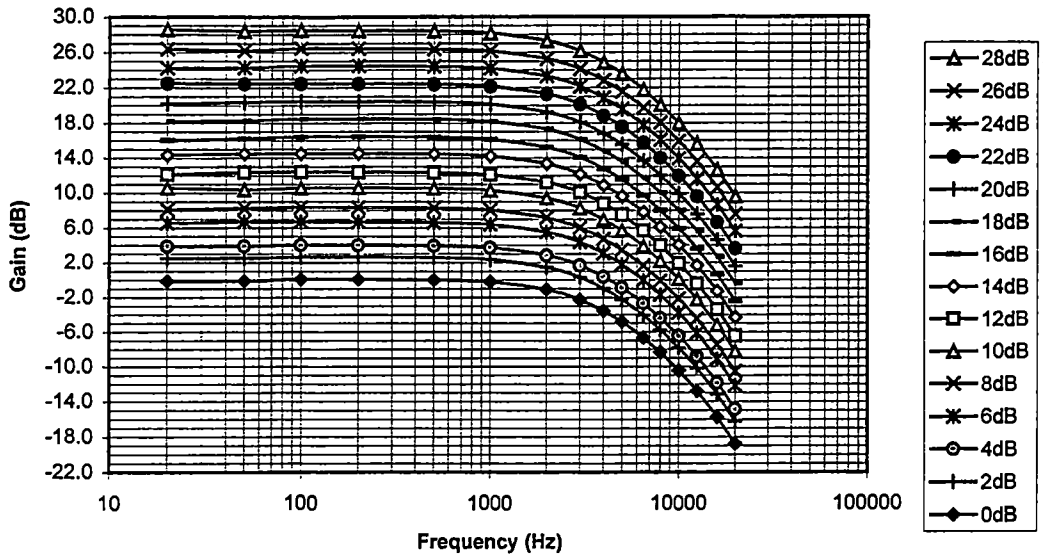

UHURA PGA1 GAIN 3.6V SUPPLY SLOW DEVICE THROUGH SPKR WITH 0dB GAIN
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB


UHURA PGA1 GAIN 3.3V SUPPLY SLOW DEVICE THROUGH SPKR AT 0dB WITH SAMPLING
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB
20dB
12dB
4dB
0dB

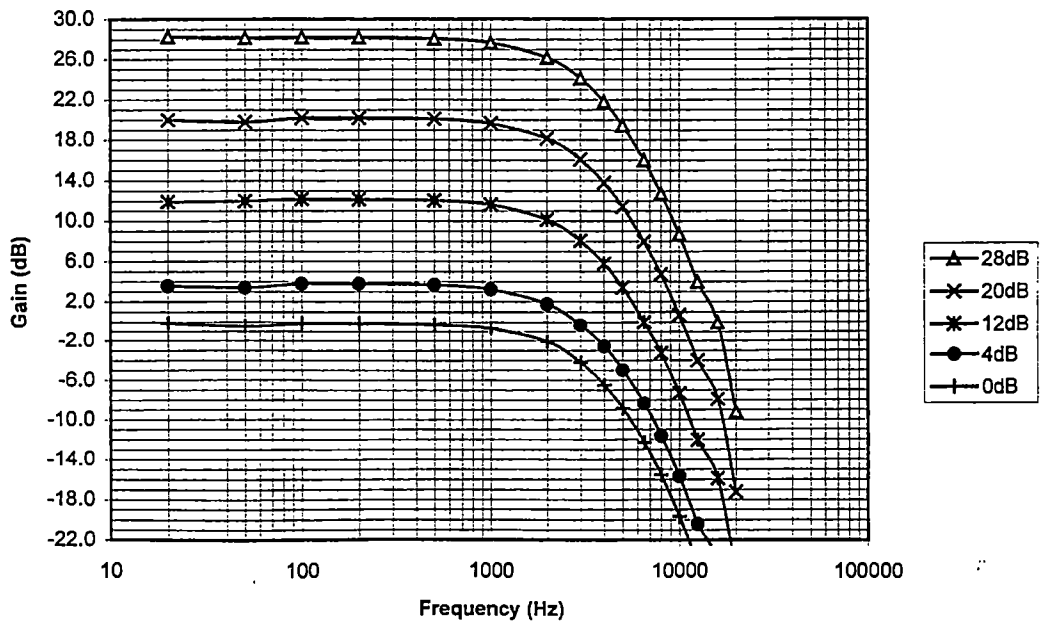

UHURA PGA1 GAIN 3.0V SUPPLY NOMINAL DEVICE THROUGH SPKR WITH 0dB GAIN
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB

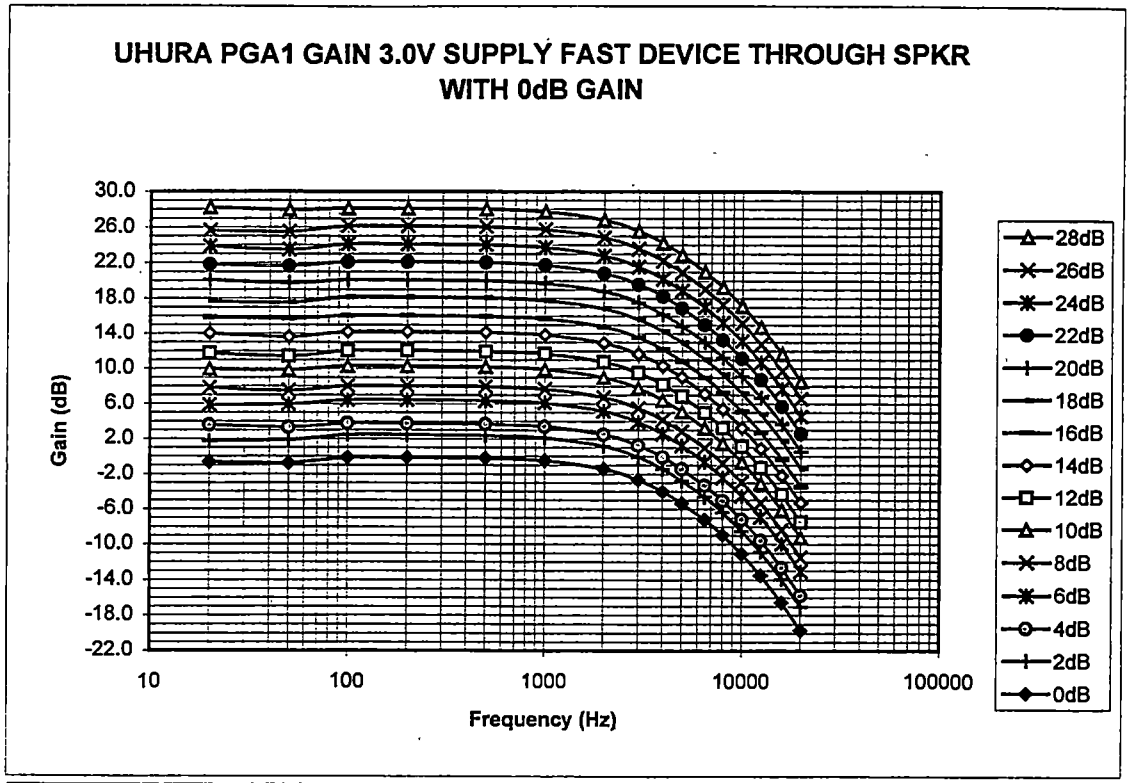

UHURA PGA1 GAIN 3.3V SUPPLY NOMINAL DEVICE THROUGH SPKR WITH 0dB GAIN
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
Gain (dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB

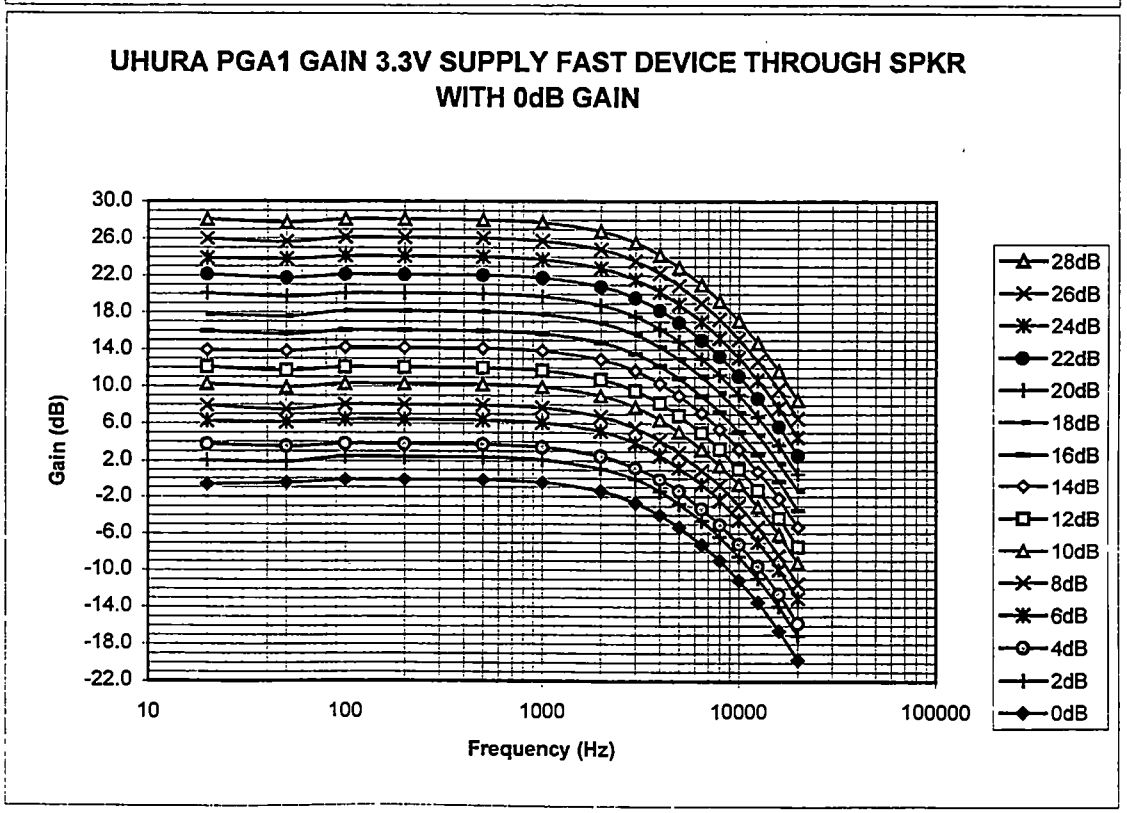
UHURA PGA1 GAIN 3.6V SUPPLY NOMINAL DEVICE THROUGH SPKR WITH 0dB GAIN



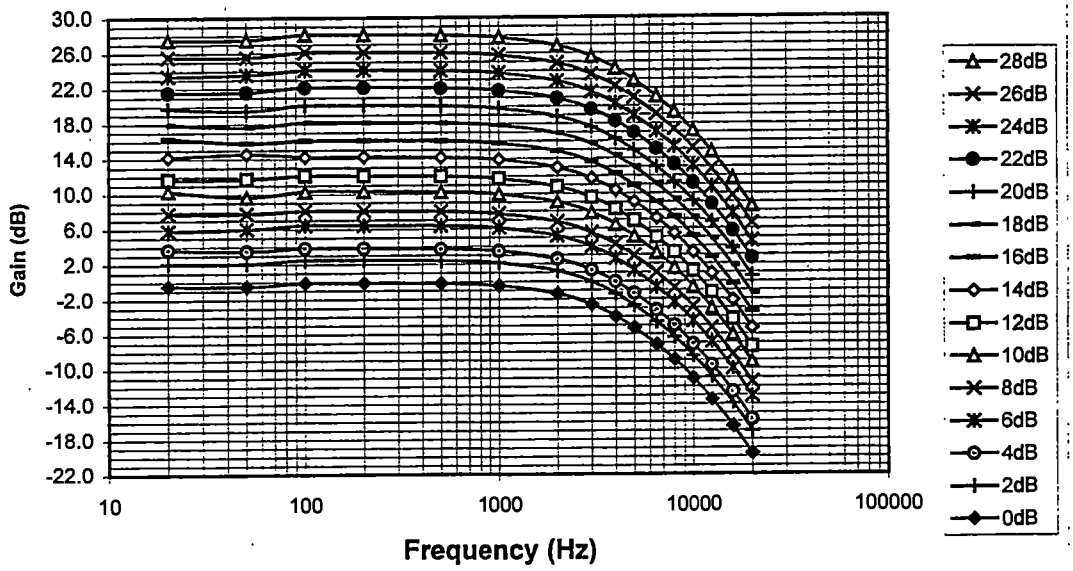
UHURA PGA1 GAIN 3.3V SUPPLY NOMINAL DEVICE THROUGH SPKR AT 0dB WITH SAMPLING



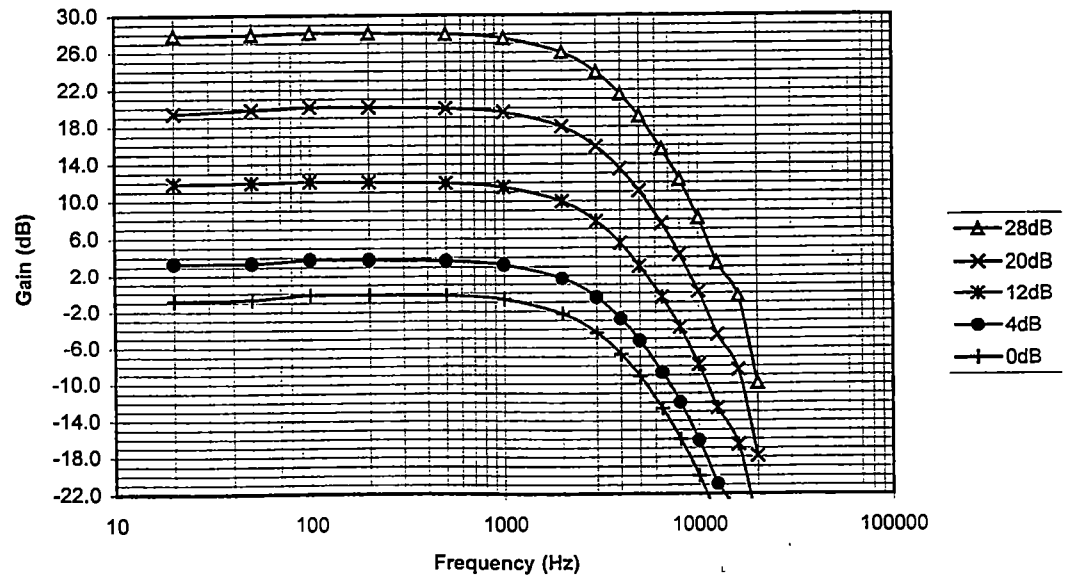

UHURA PGA1 GAIN 3.0V SUPPLY FAST DEVICE THROUGH SPKR
WITH 0dB GAIN
Gain (dB)
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB


UHURA PGA1 GAIN 3.3V SUPPLY FAST DEVICE THROUGH SPKR
WITH 0dB GAIN
Gain (dB)
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
-10.0
-14.0
-18.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
28dB
26dB
24dB
22dB
20dB
18dB
16dB
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB

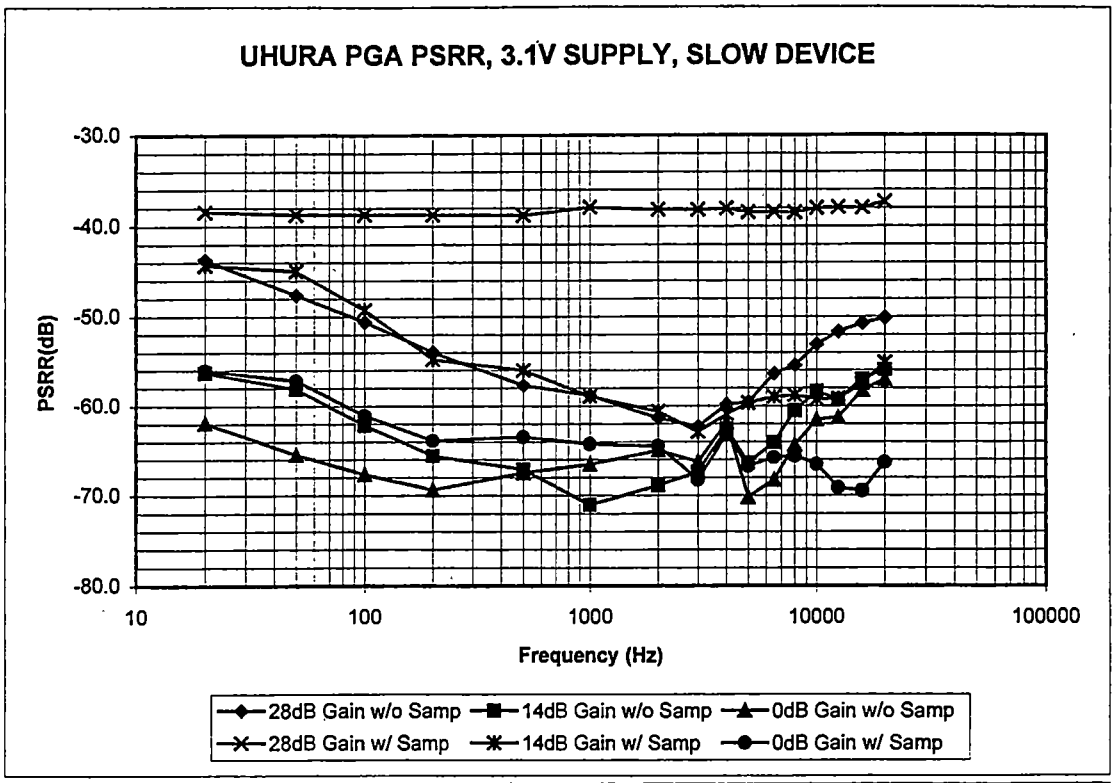
UHURA PGA1 GAIN 3.6V SUPPLY FAST DEVICE THROUGH SPKR WITH 0dB GAIN

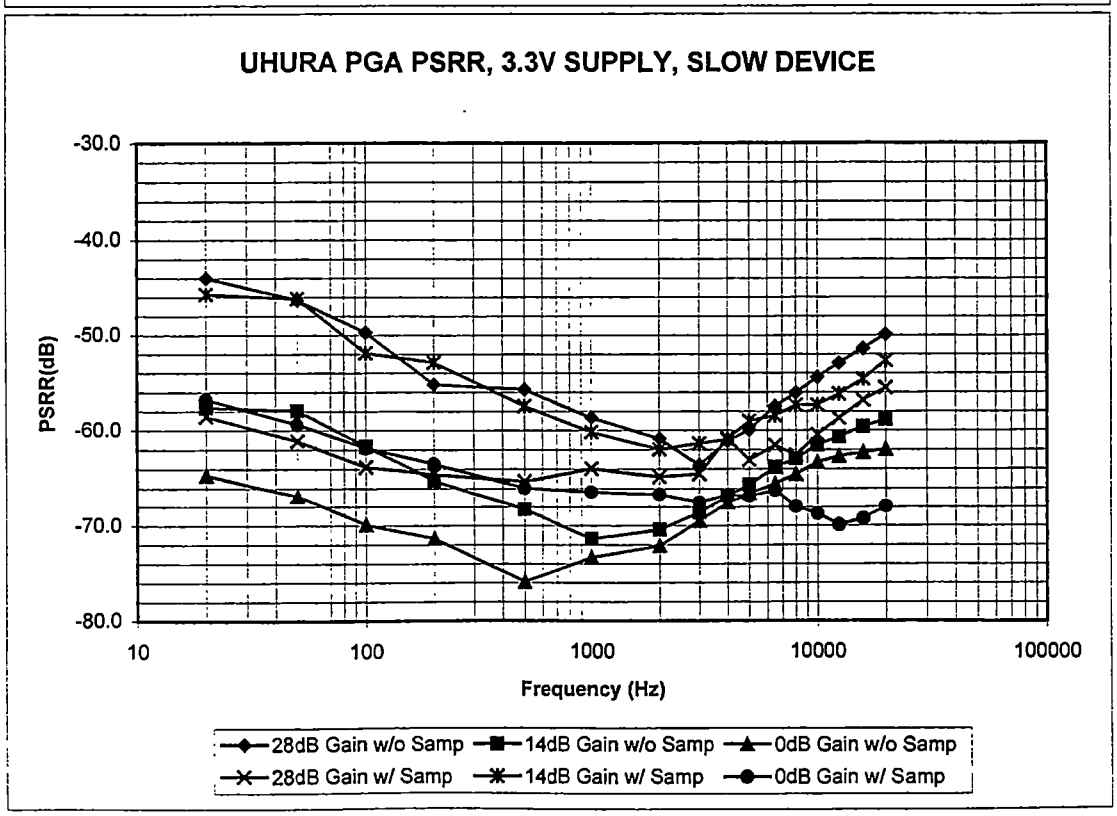


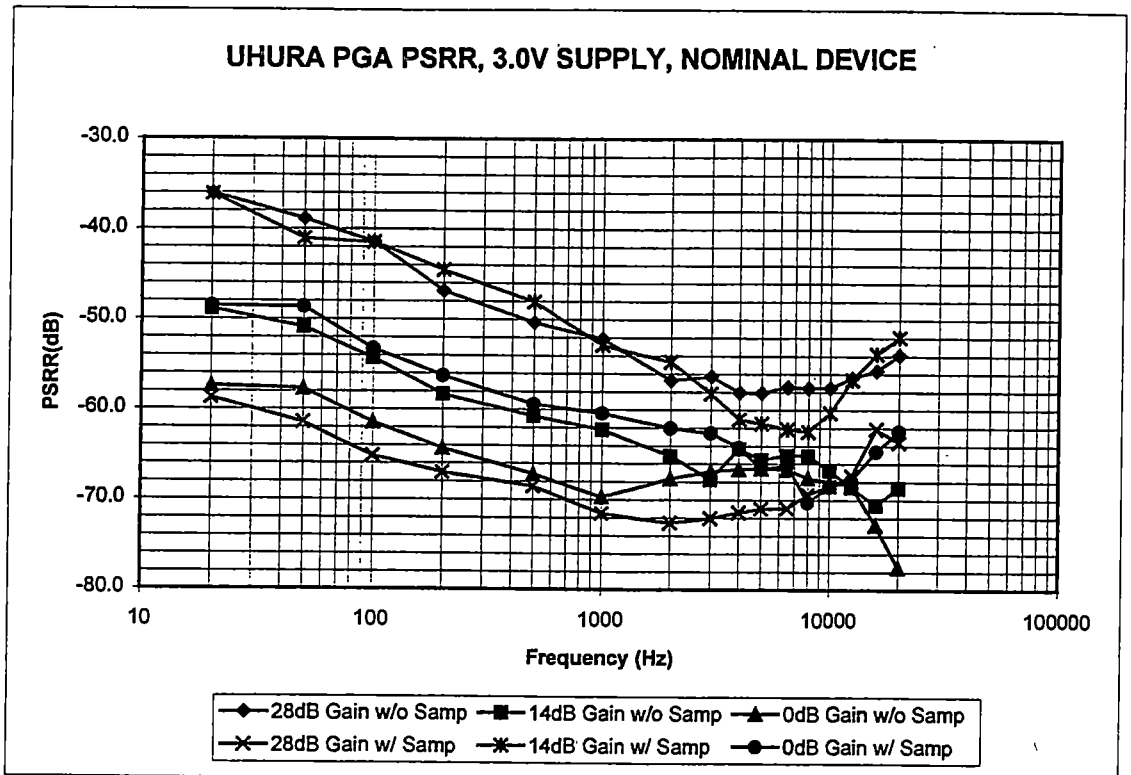
UHURA PGA1 GAIN 3.3V SUPPLY FAST DEVICE THROUGH SPKR AT 0dB WITH SAMPLING

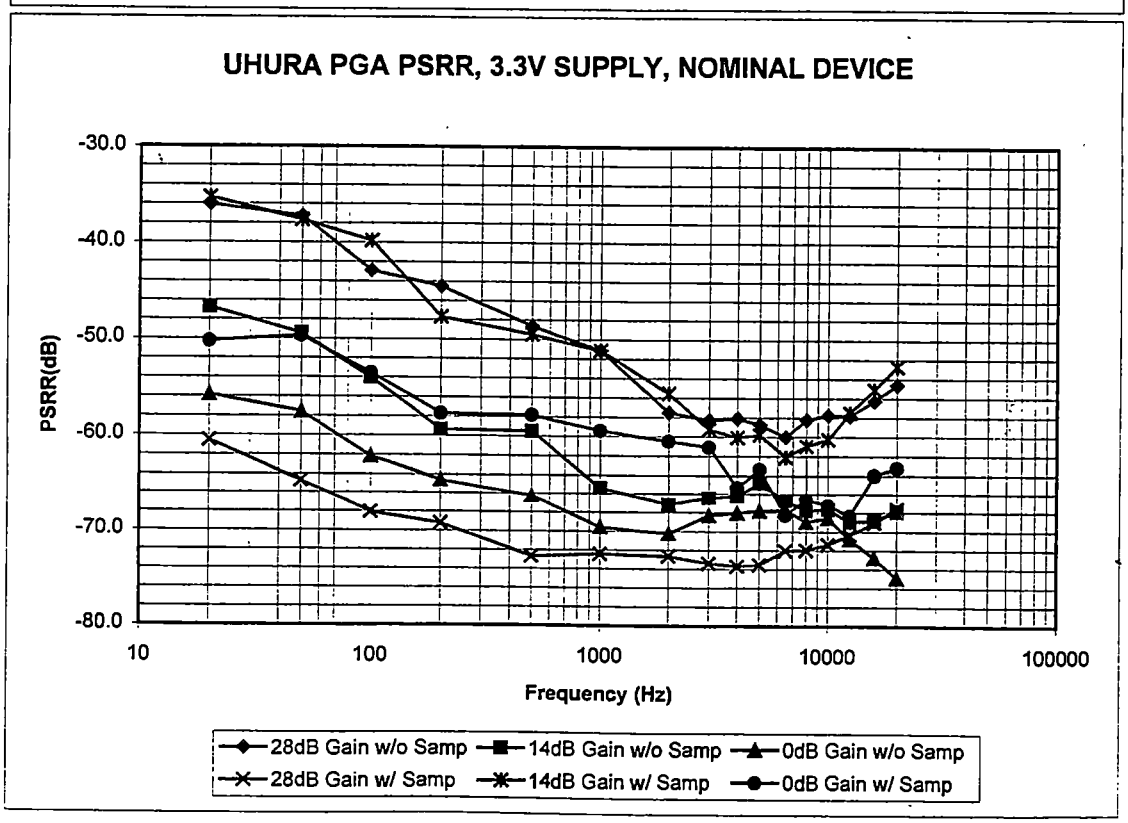


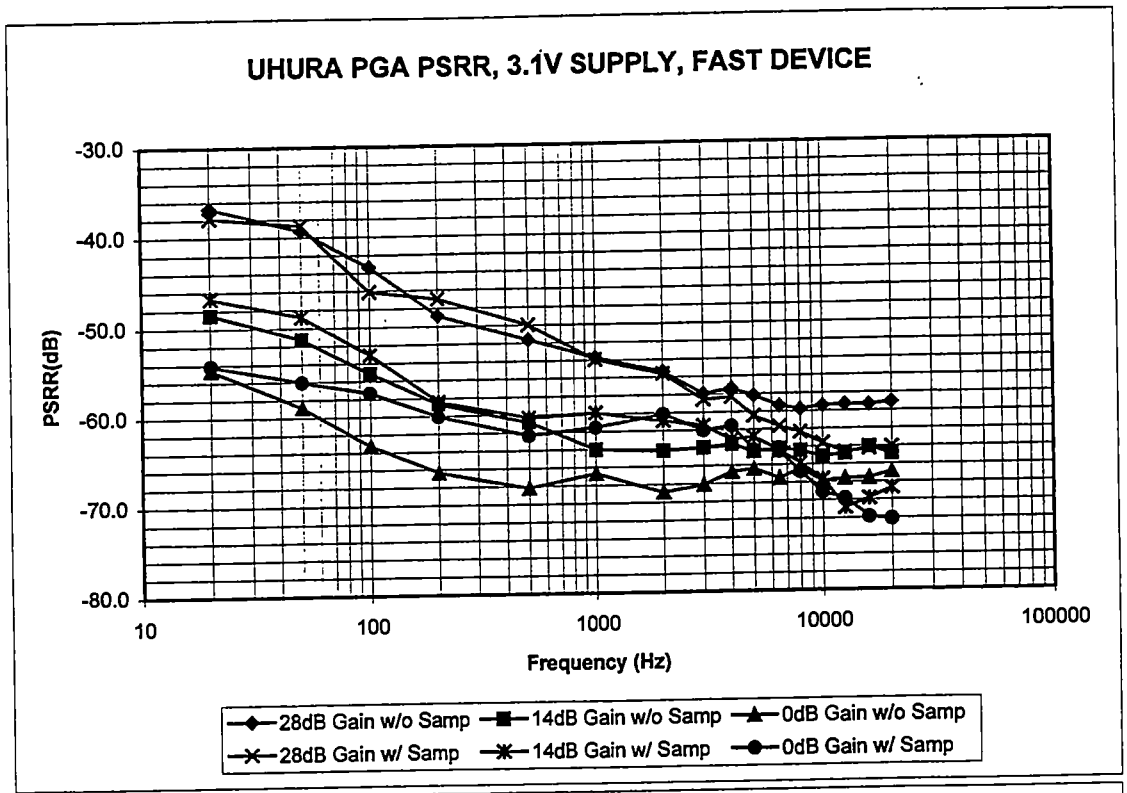
PROGRAMMABLE GAIN AMPLIFIER PSRR DATA

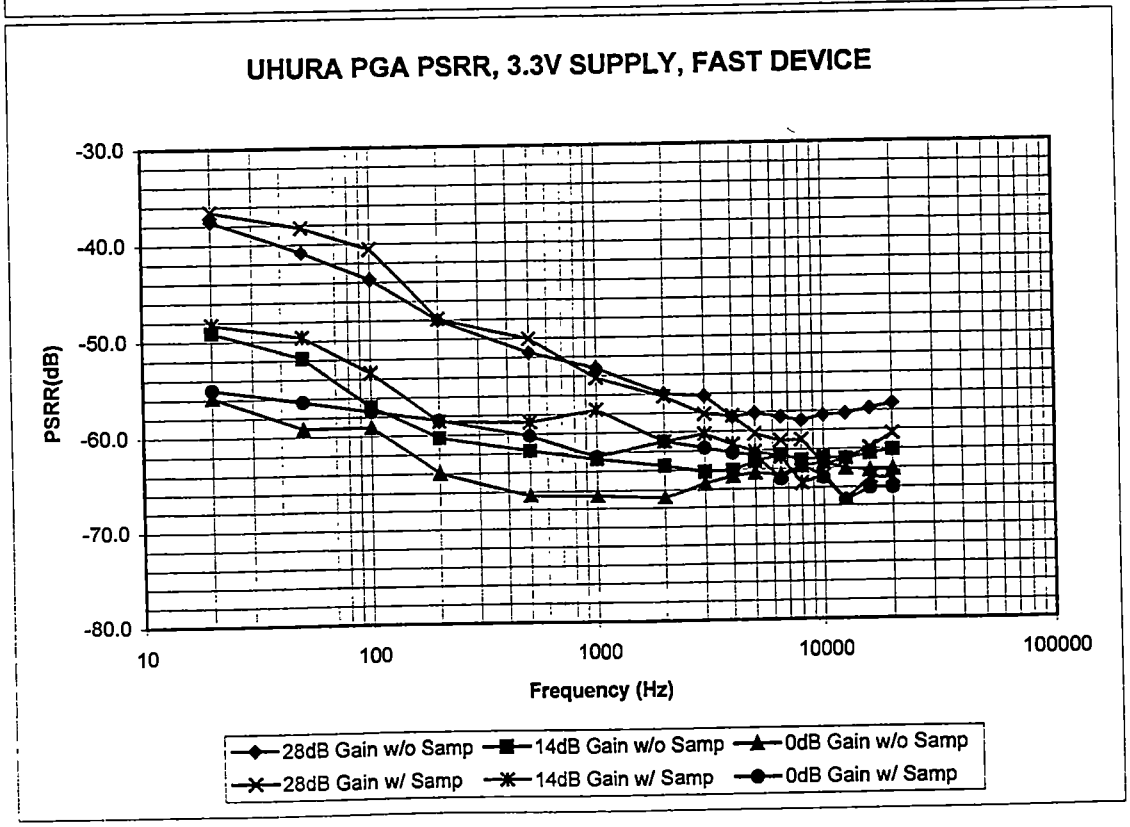

UHURA PGA PSRR, 3.1V SUPPLY, SLOW DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp


UHURA PGA PSRR, 3.3V SUPPLY, SLOW DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

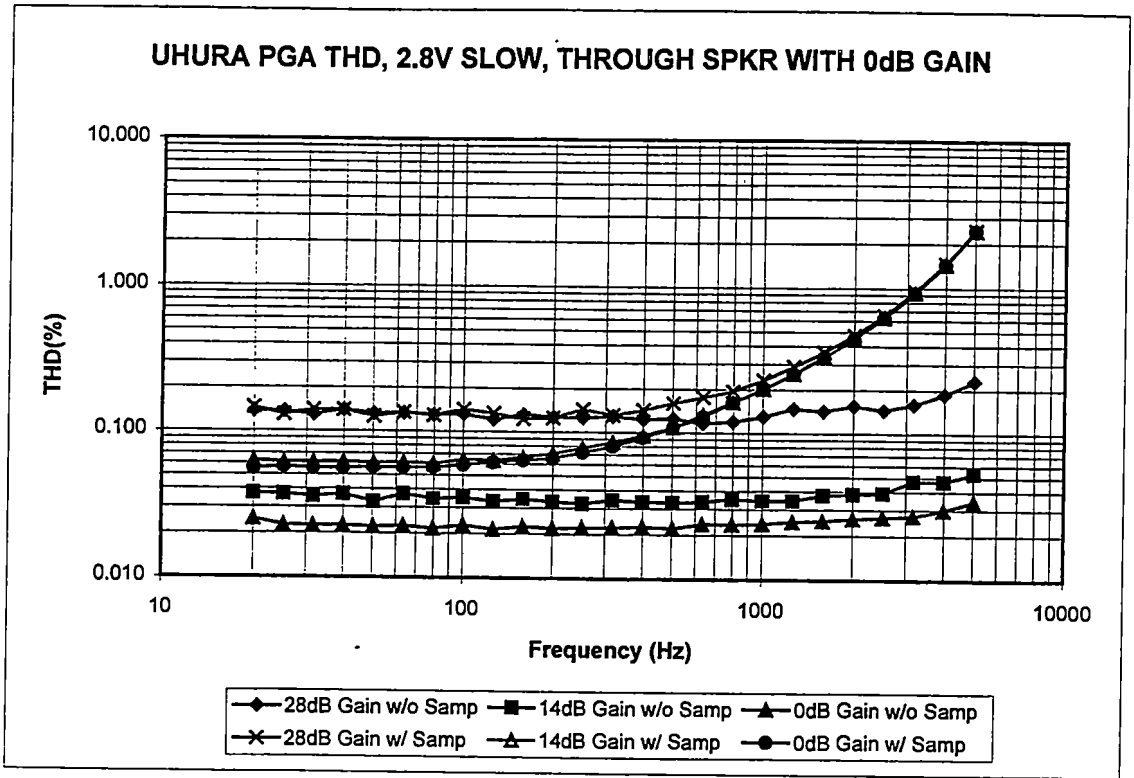

UHURA PGA PSRR, 3.0V SUPPLY, NOMINAL DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

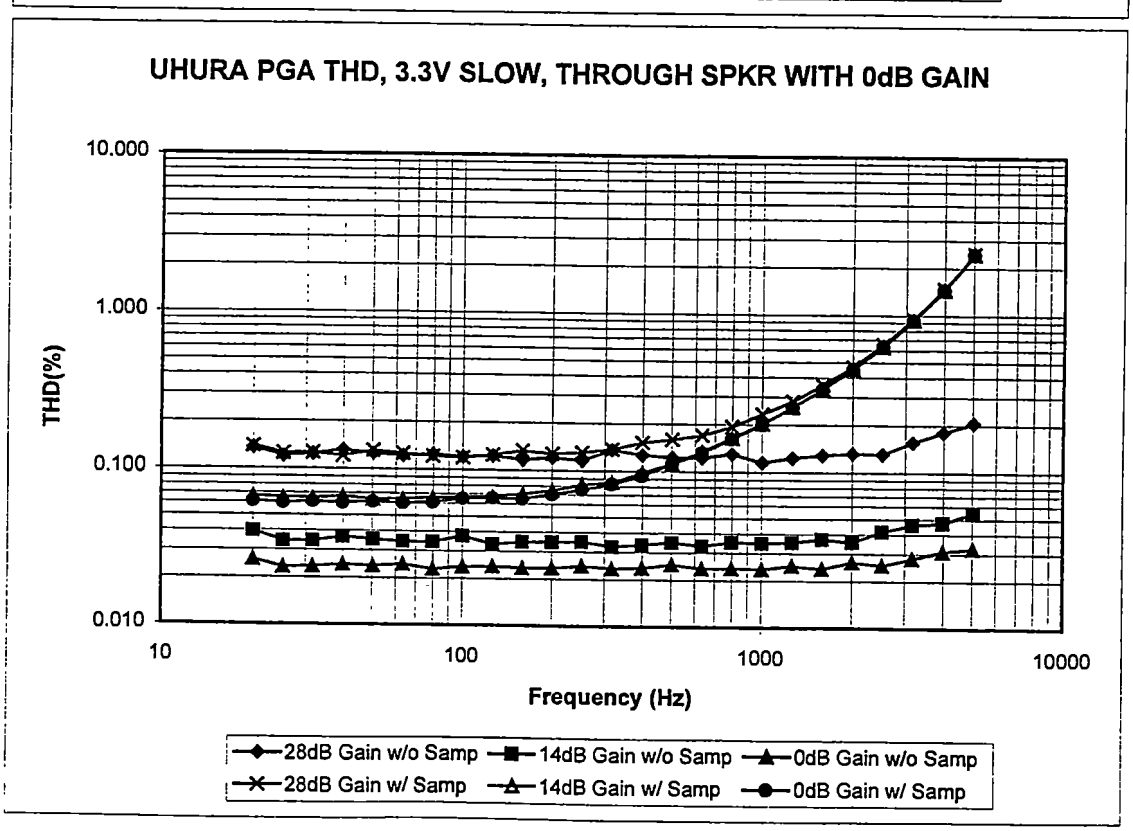

UHURA PGA PSRR, 3.3V SUPPLY, NOMINAL DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

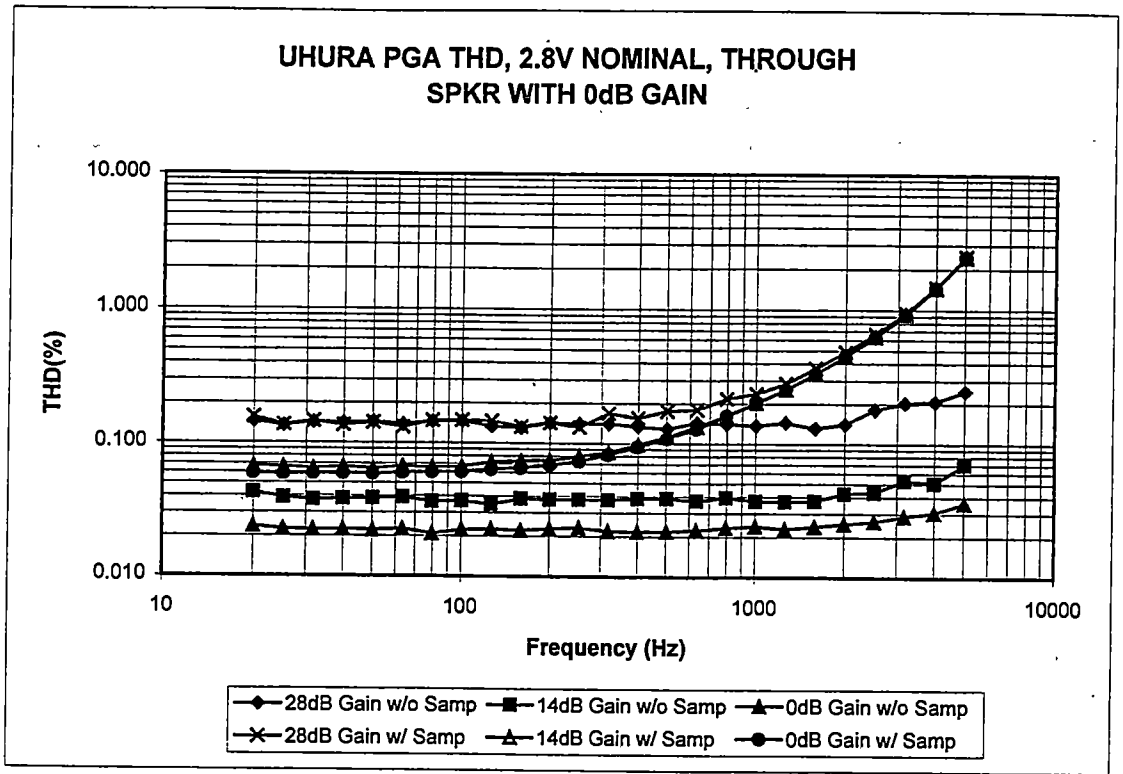

UHURA PGA PSRR, 3.1V SUPPLY, FAST DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

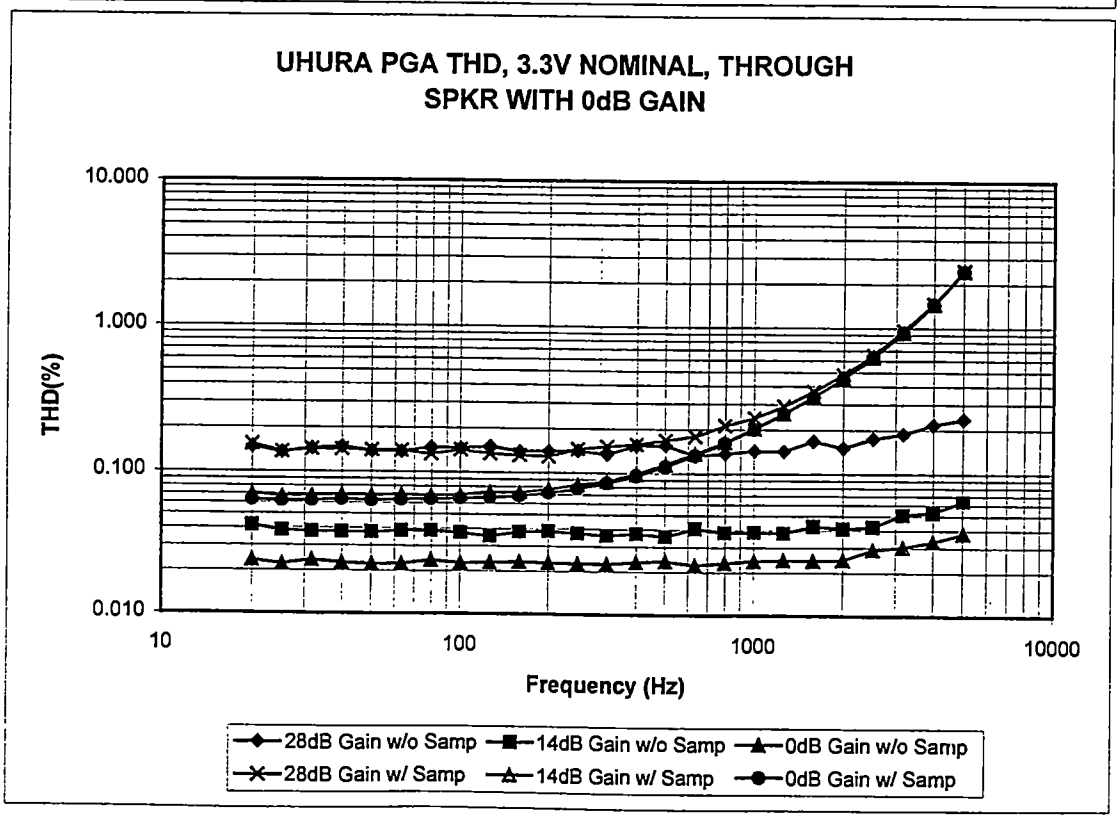

UHURA PGA PSRR, 3.3V SUPPLY, FAST DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

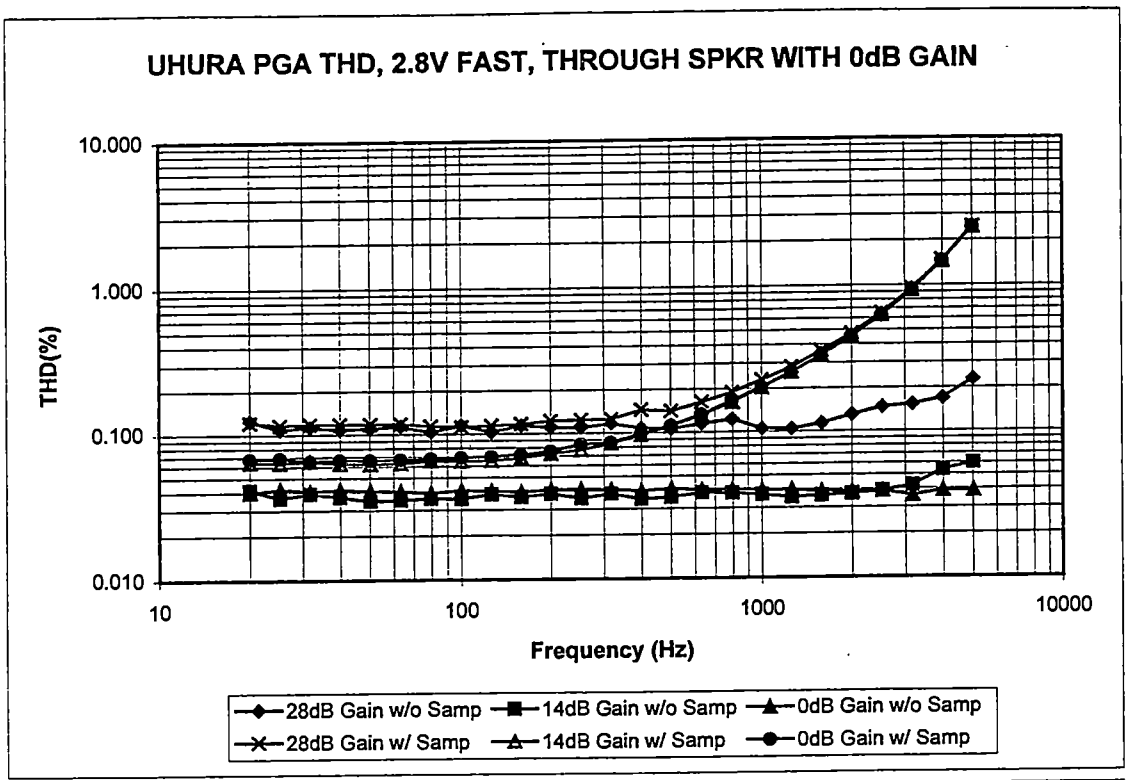
PROGRAMMABLE GAIN AMPLIFIER THD DATA

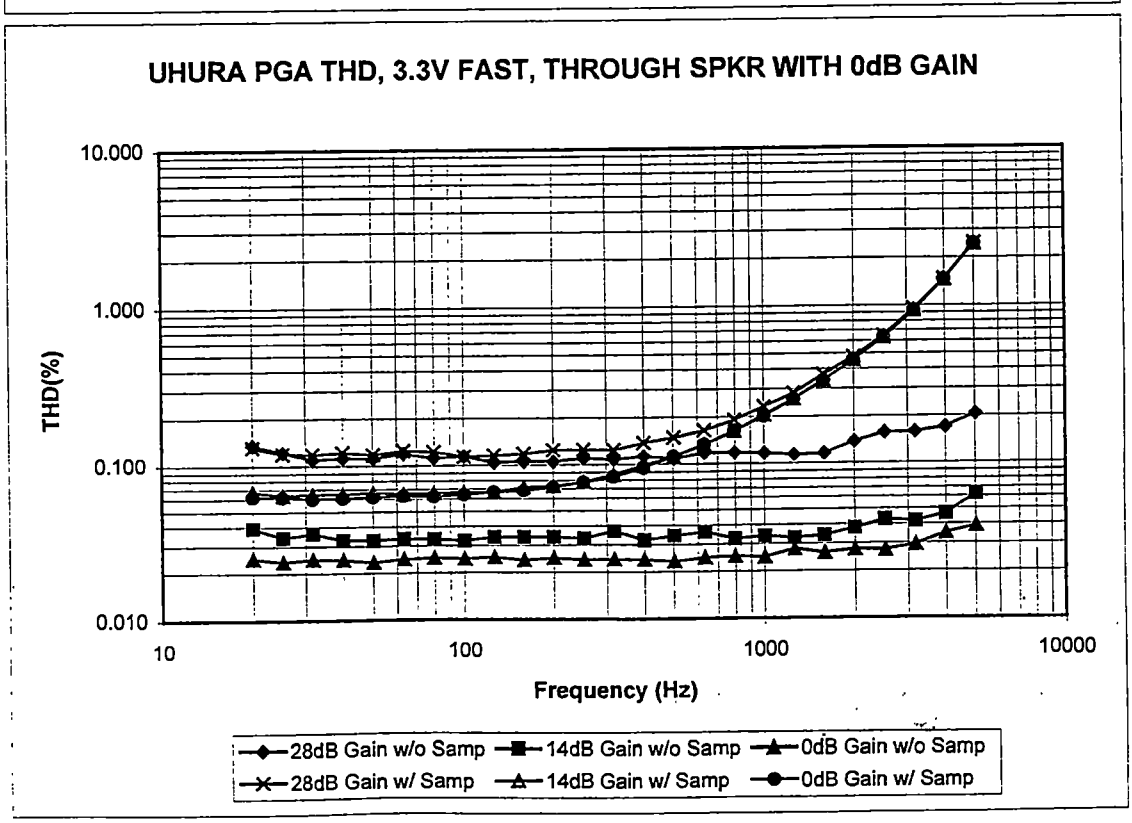

UHURA PGA THD, 2.8V SLOW, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp


UHURA PGA THD, 3.3V SLOW, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp


UHURA PGA THD, 2.8V NOMINAL, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp


UHURA PGA THD, 3.3V NOMINAL, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp


UHURA PGA THD, 2.8V FAST, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

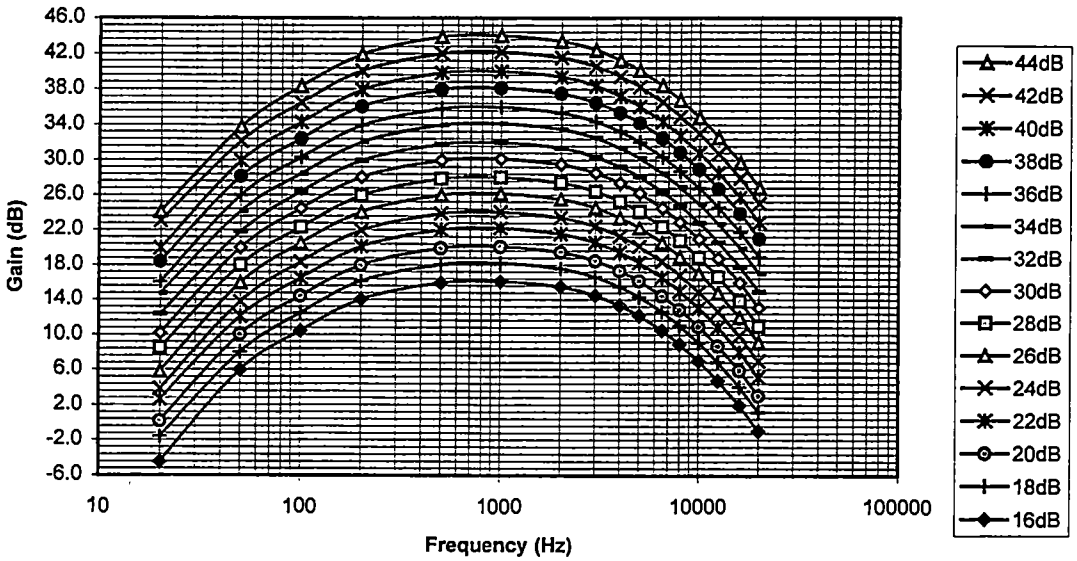

UHURA PGA THD, 3.3V FAST, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
28dB Gain w/o Samp
14dB Gain w/o Samp
0dB Gain w/o Samp
28dB Gain w/ Samp
14dB Gain w/ Samp
0dB Gain w/ Samp

APPENDIX H

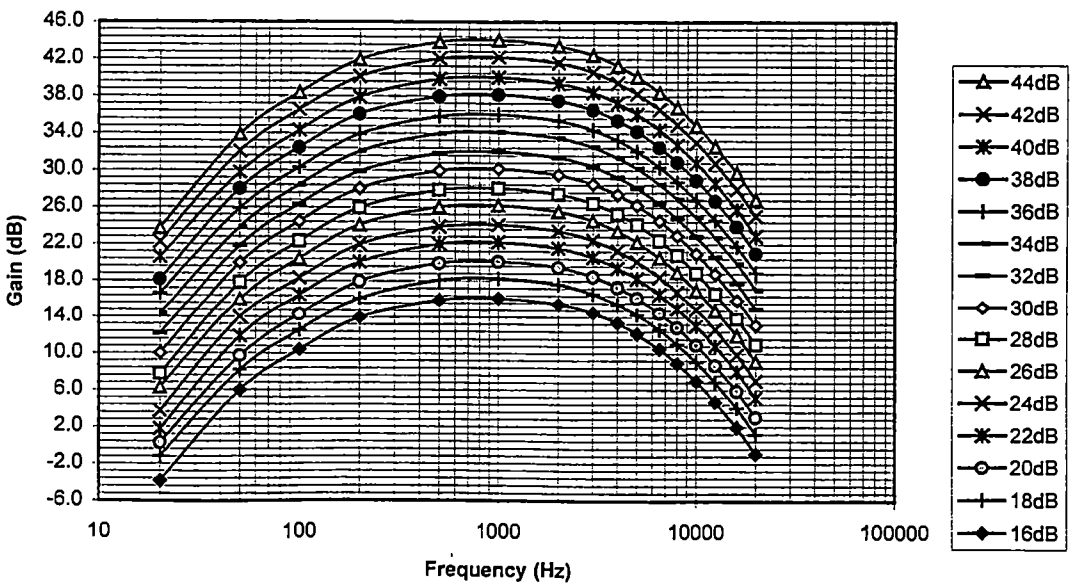
PROGRAMMABLE GAIN MICROPHONE AMPLIFIER DATA

PROGRAMMABLE GAIN MICROPHONE AMPLIFIER GAIN DATA

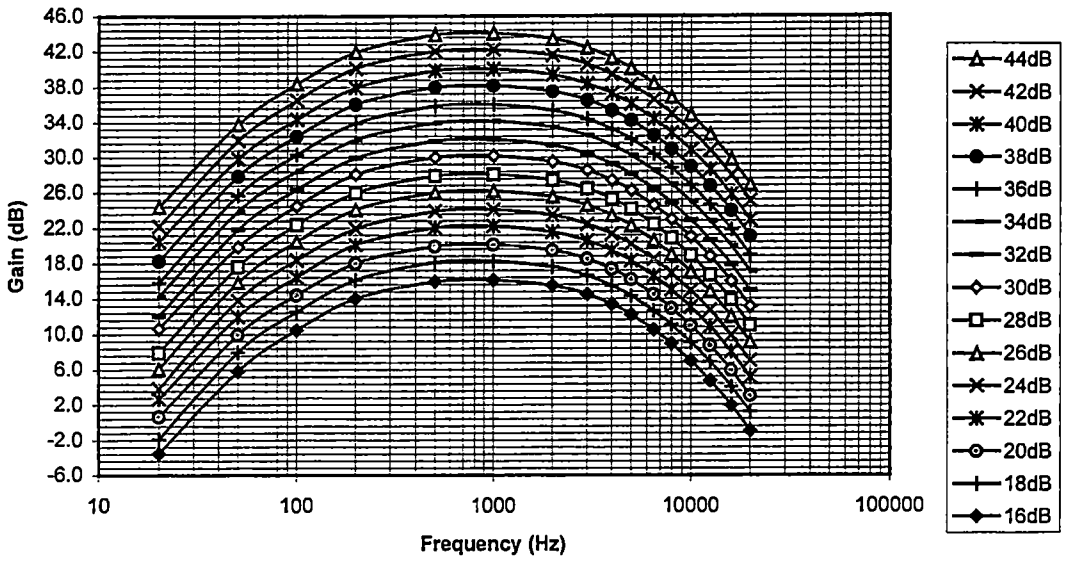
UHURA PGMO GAIN 3.0V SUPPLY SLOW DEVICE THROUGH SPKR WITH 0dB GAIN



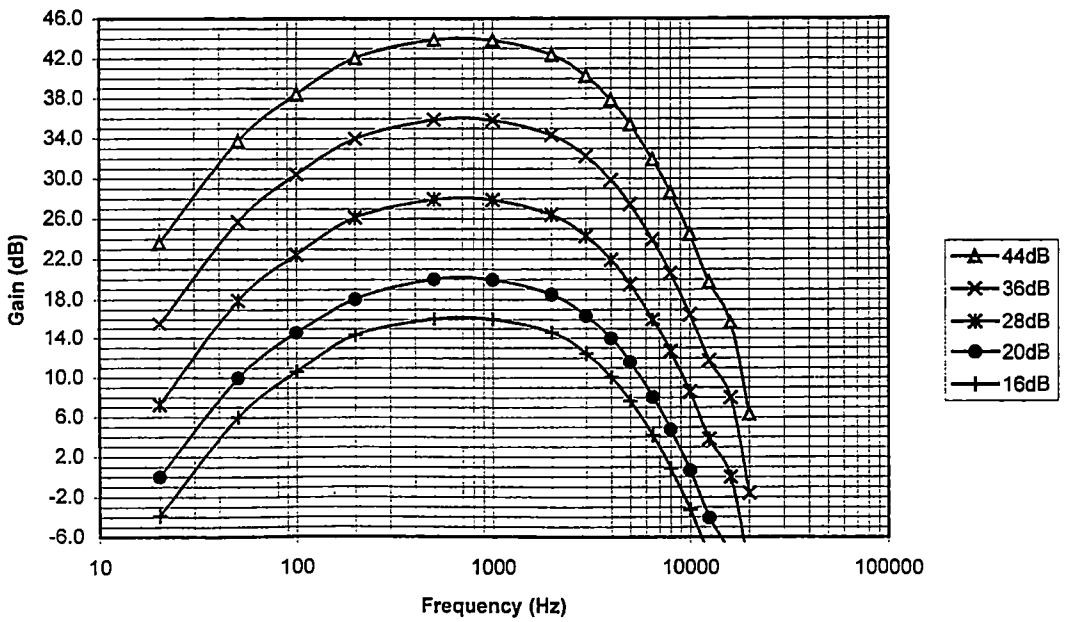
UHURA PGMO GAIN 3.3V SUPPLY SLOW DEVICE THROUGH SPKR WITH 0dB GAIN



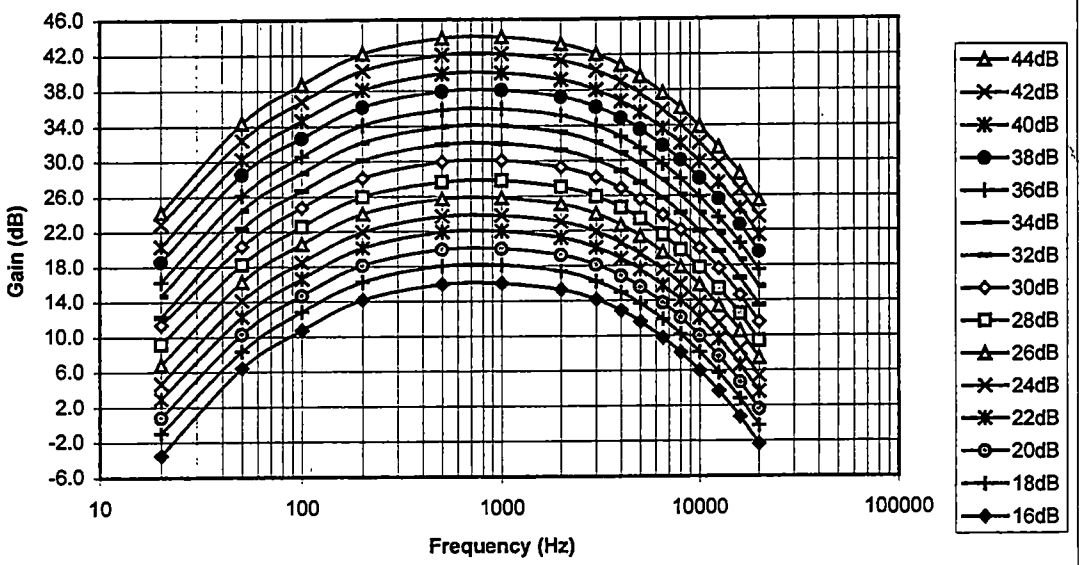
UHURA PGMO GAIN 3.6V SUPPLY SLOW DEVICE THROUGH SPKR WITH 0dB GAIN



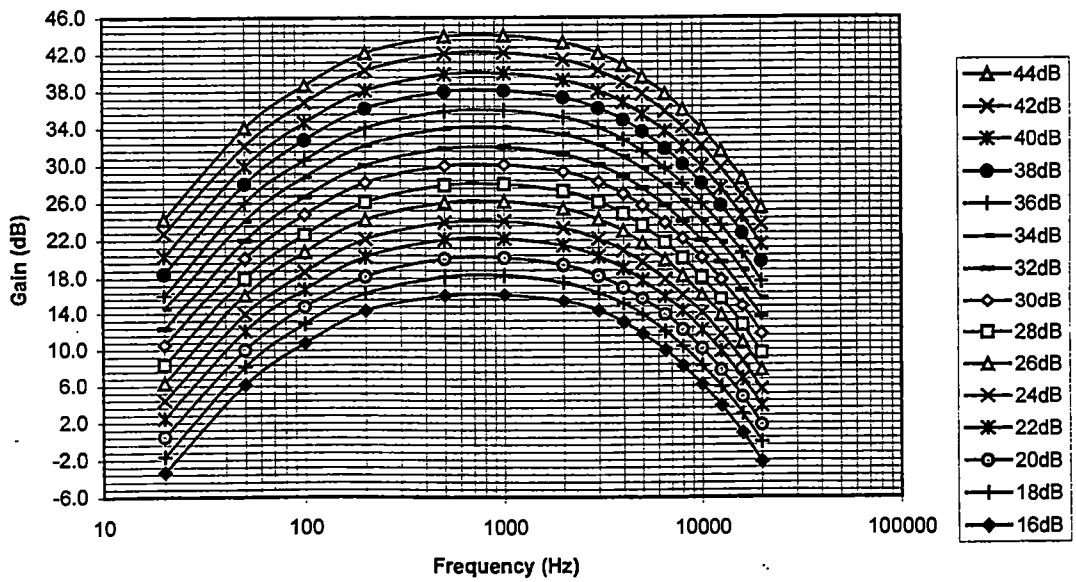
UHURA PGMO GAIN 3.3V SUPPLY SLOW DEVICE THROUGH SPKR AT 0dB WITH SAMPLING



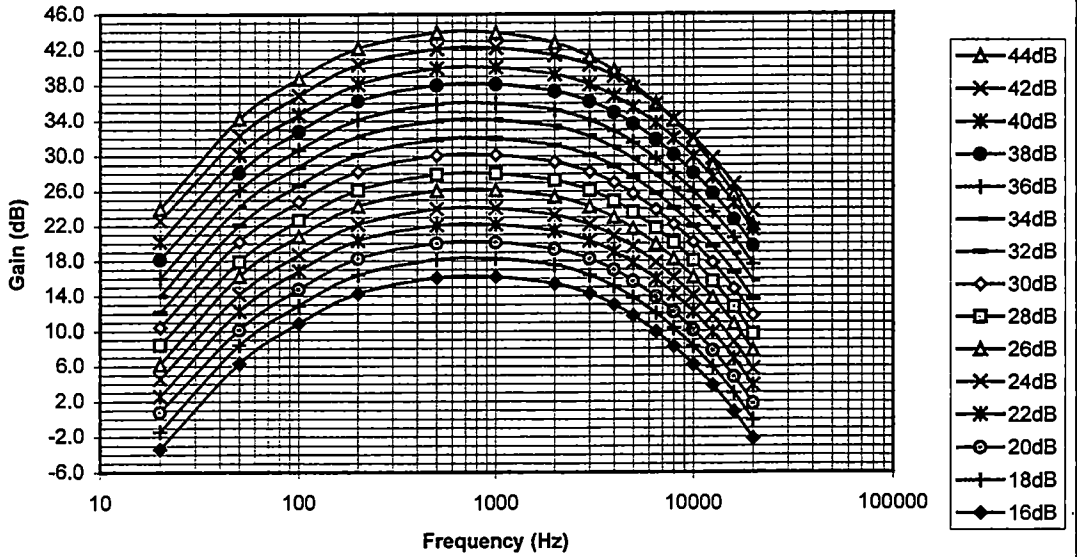
UHURA PGMO GAIN 3.0V SUPPLY NOMINAL DEVICE THROUGH SPKR WITH 0dB GAIN



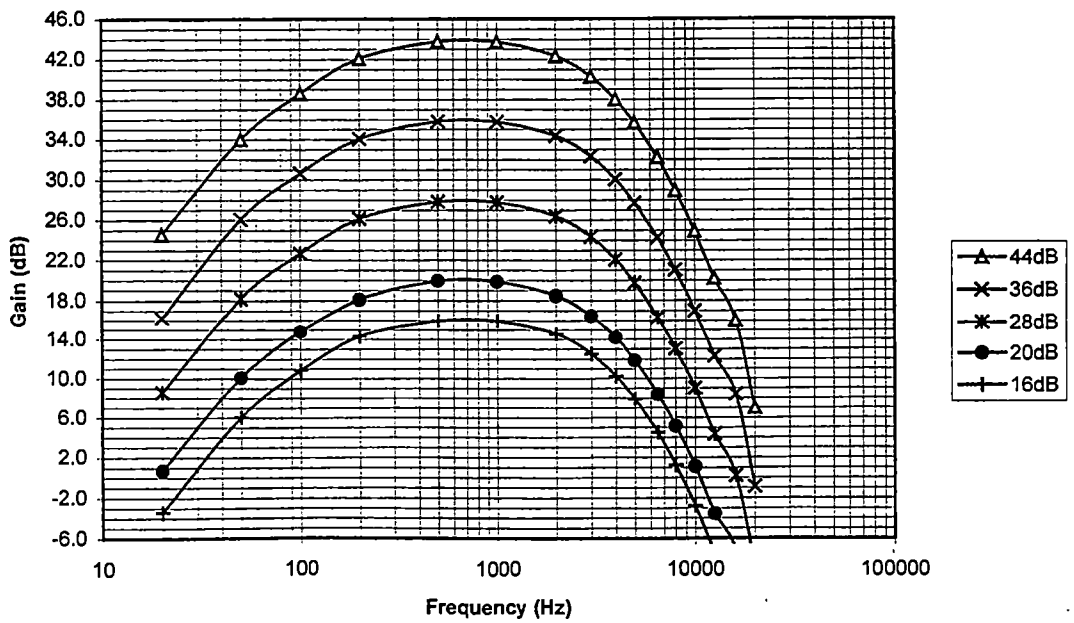
UHURA PGMO GAIN 3.3V SUPPLY NOMINAL DEVICE THROUGH SPKR WITH 0dB GAIN



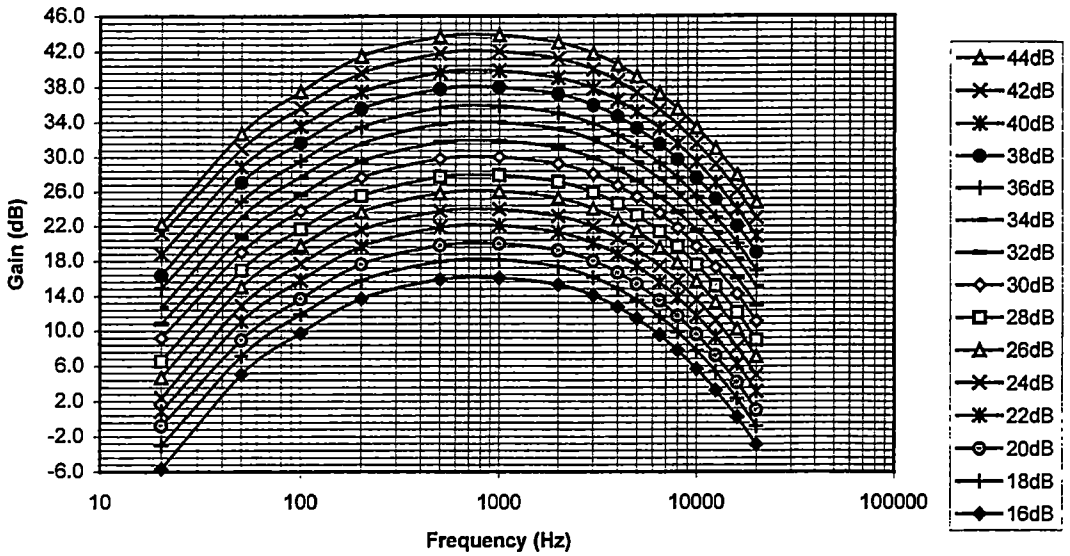
UHURA PGMO GAIN 3.6V SUPPLY NOMINAL DEVICE THROUGH SPKR WITH 0dB GAIN



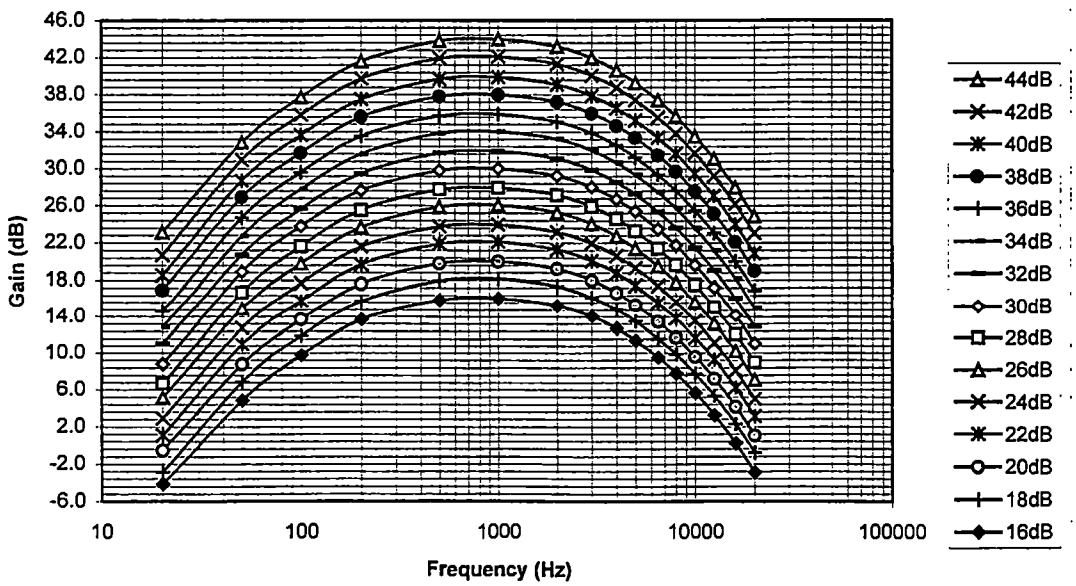
UHURA PGMO GAIN 3.3V SUPPLY NOMINAL DEVICE THROUGH SPKR AT 0dB WITH SAMPLING

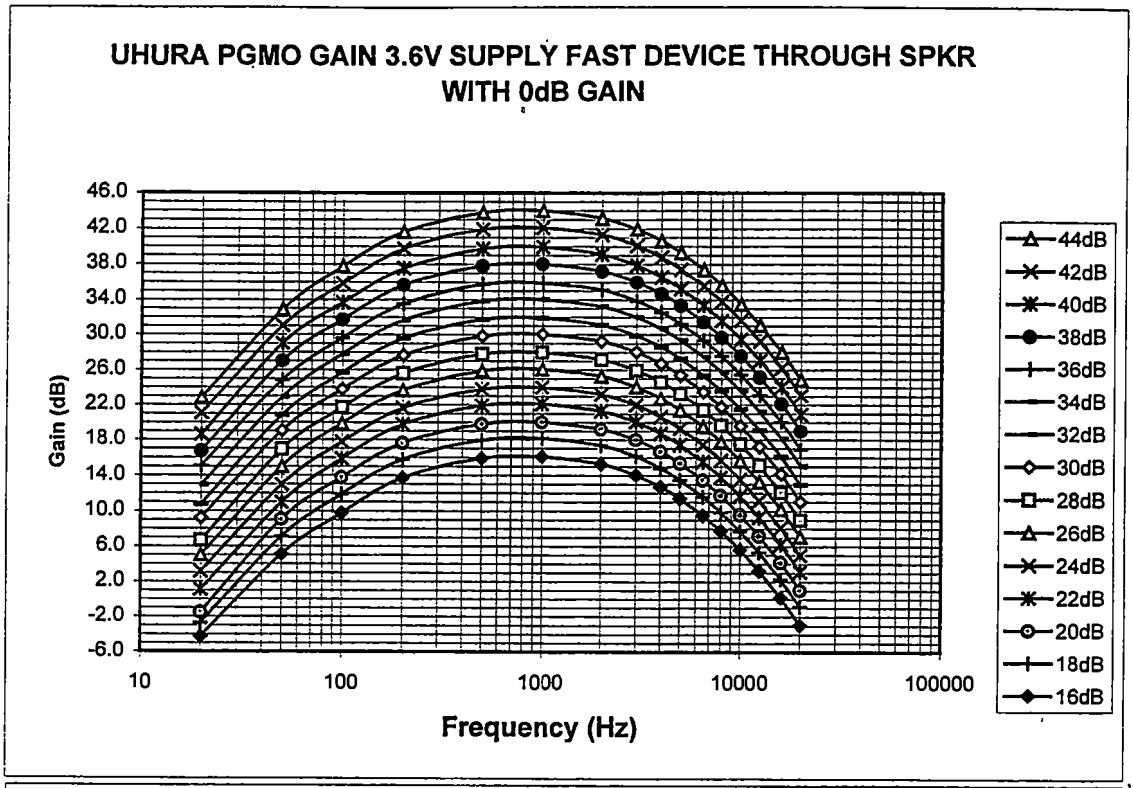


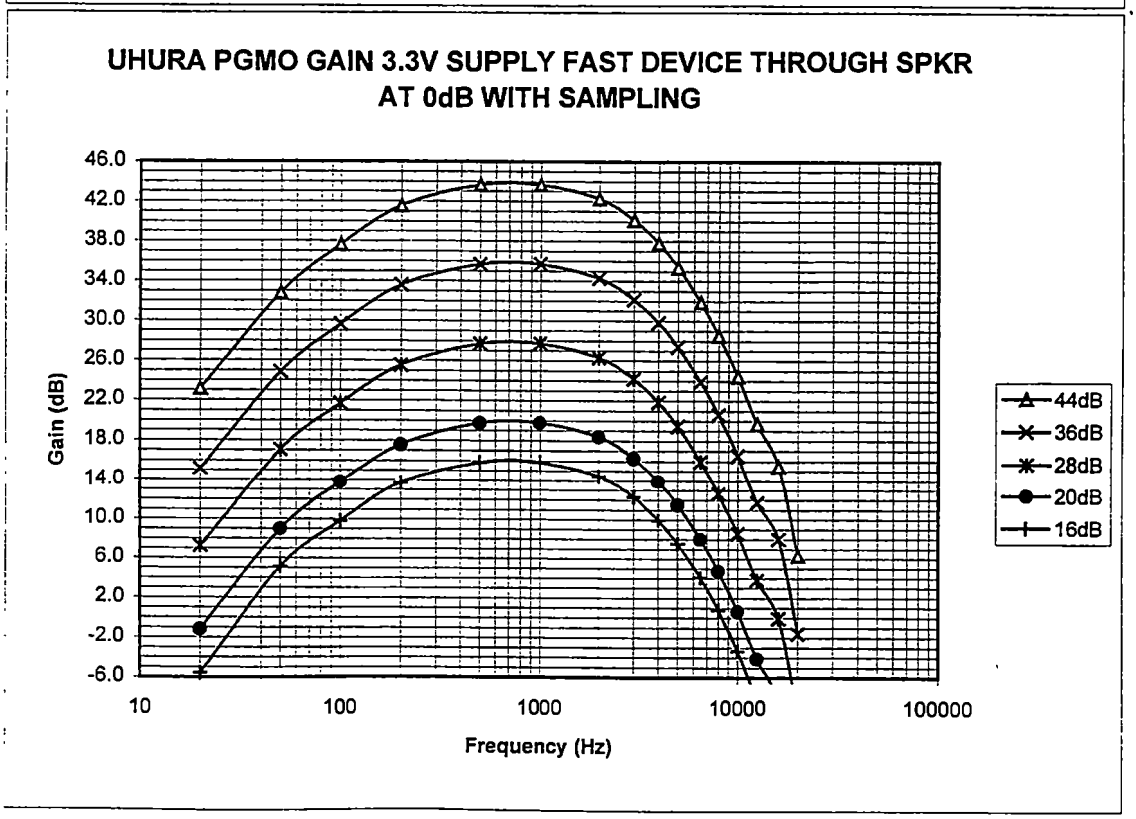
UHURA PGMO GAIN 3.0V SUPPLY FAST DEVICE THROUGH SPKR WITH 0dB GAIN



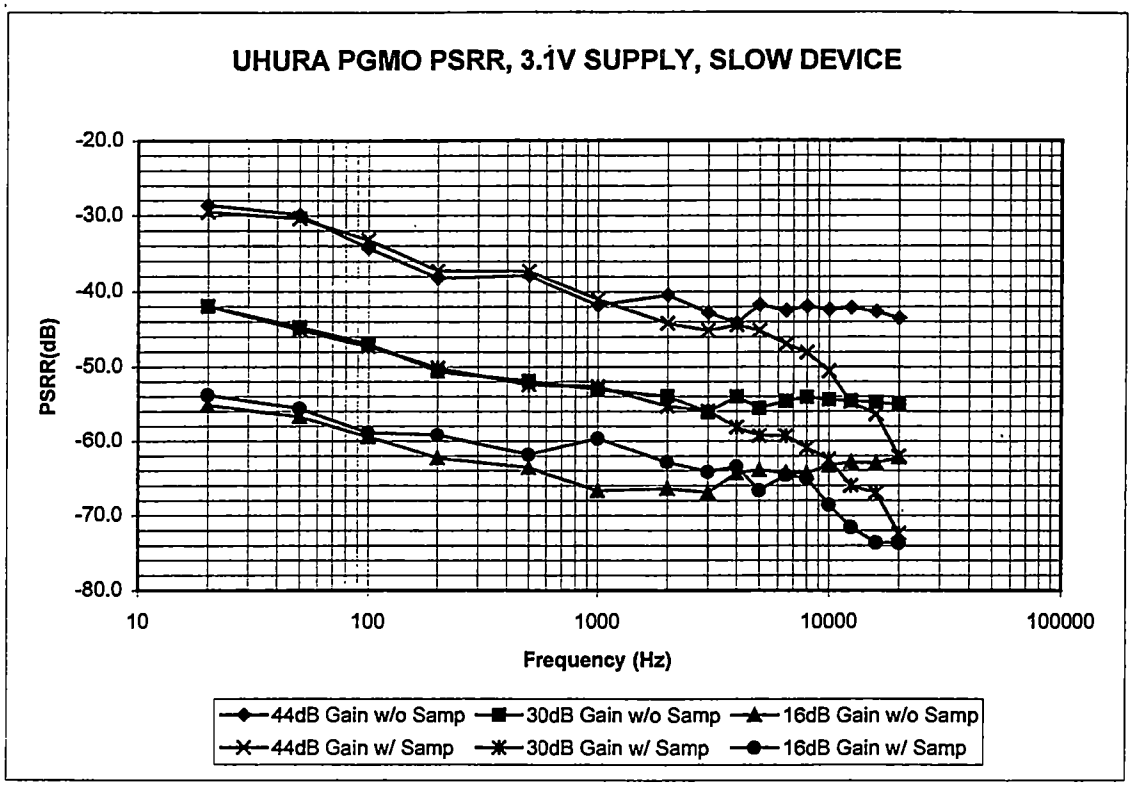
UHURA PGMO GAIN 3.3V SUPPLY FAST DEVICE THROUGH SPKR WITH 0dB GAIN

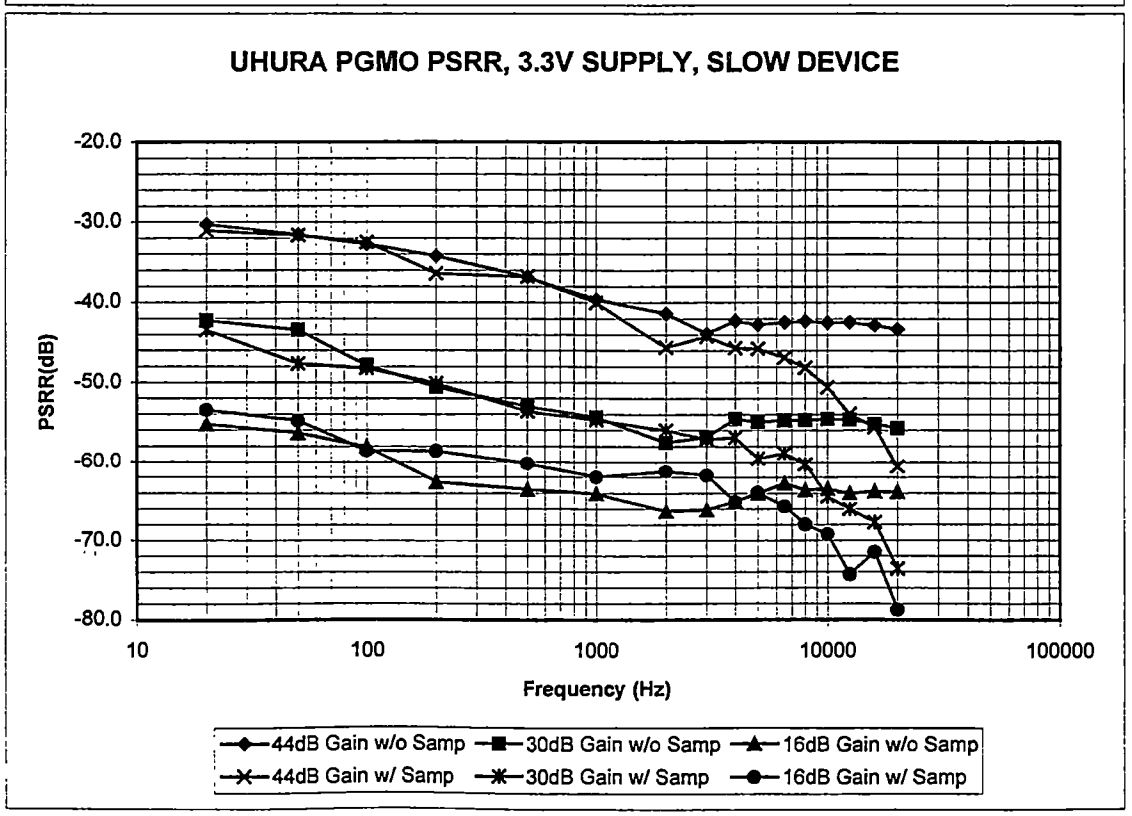


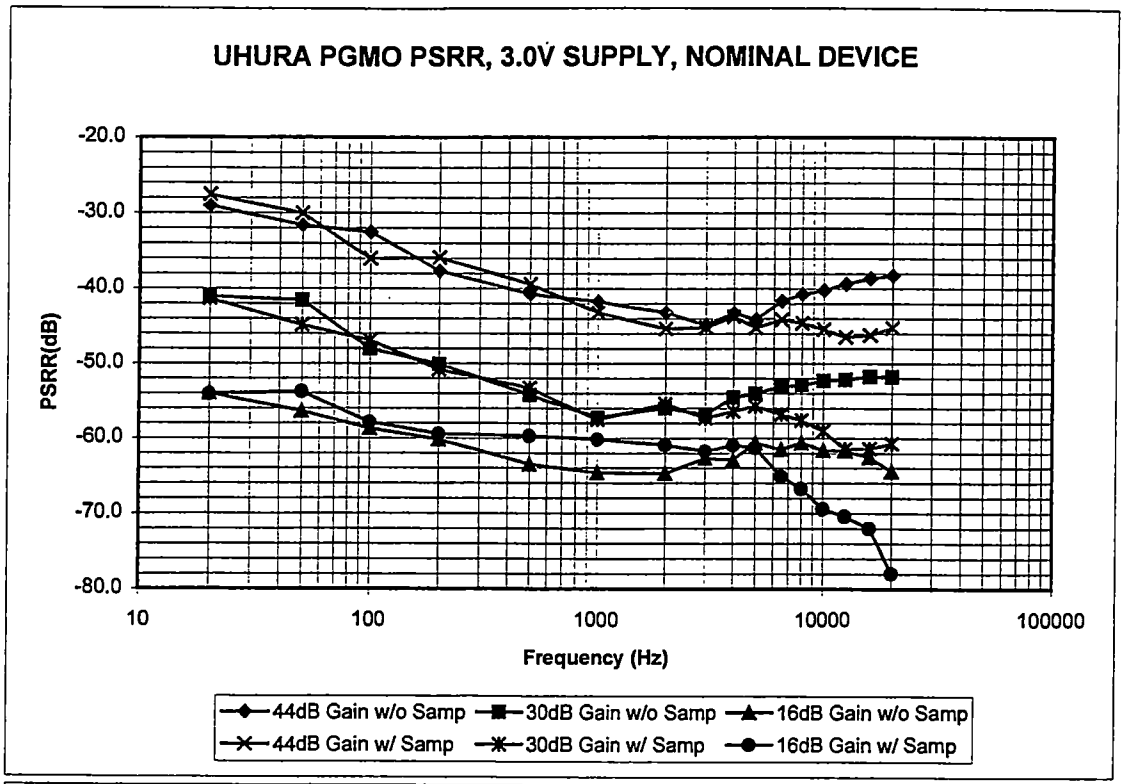

UHURA PGMO GAIN 3.6V SUPPLY FAST DEVICE THROUGH SPKR
WITH 0dB GAIN
Gain (dB)
46.0
42.0
38.0
34.0
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
10
100
1000
10000
100000
Frequency (Hz)
44dB
42dB
40dB
38dB
36dB
34dB
32dB
30dB
28dB
26dB
24dB
22dB
20dB
18dB
16dB

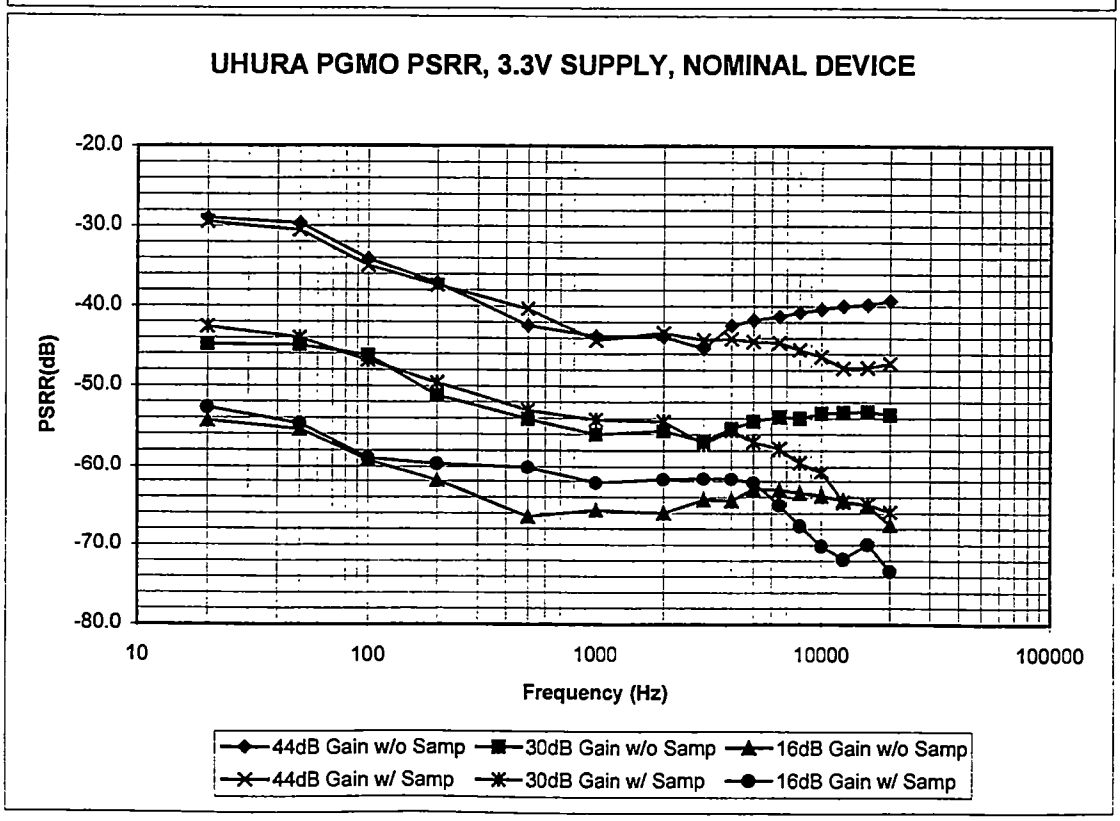

UHURA PGMO GAIN 3.3V SUPPLY FAST DEVICE THROUGH SPKR
AT 0dB WITH SAMPLING
Gain (dB)
46.0
42.0
38.0
34.0
30.0
26.0
22.0
18.0
14.0
10.0
6.0
2.0
-2.0
-6.0
10
100
1000
10000
100000
Frequency (Hz)
44dB
36dB
28dB
20dB
16dB

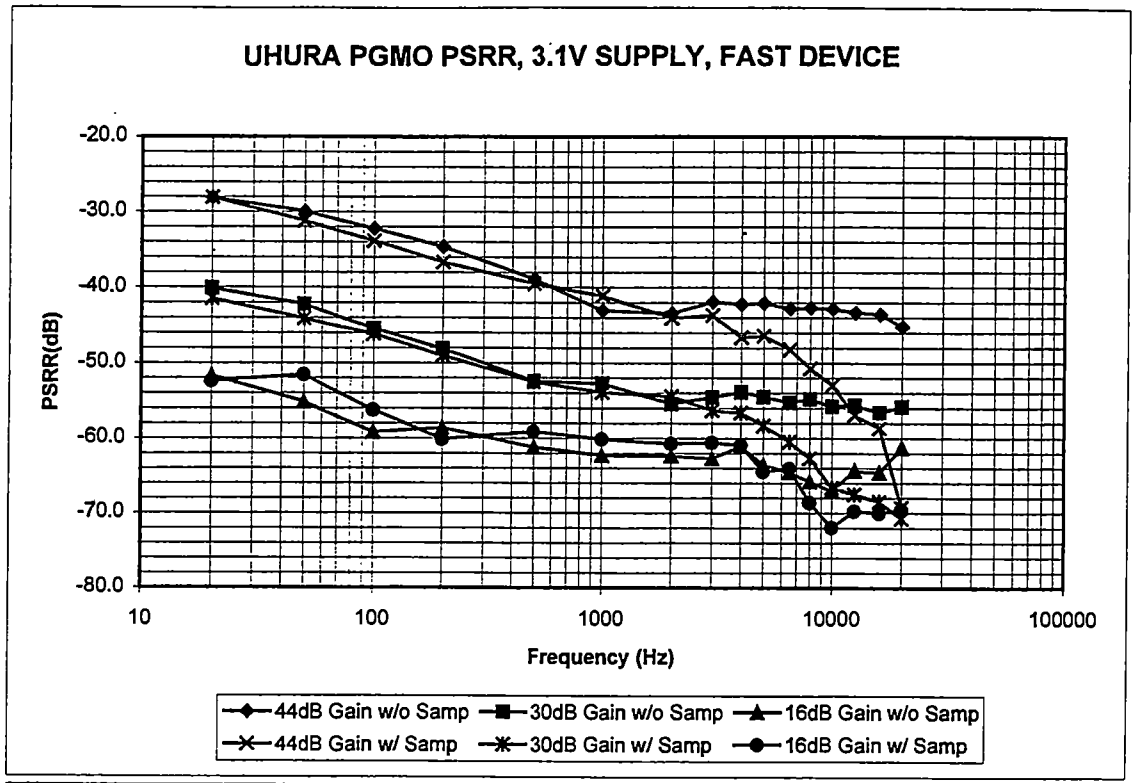
PROGRAMMABLE GAIN MICROPHONE AMPLIFIER PSRR DATA

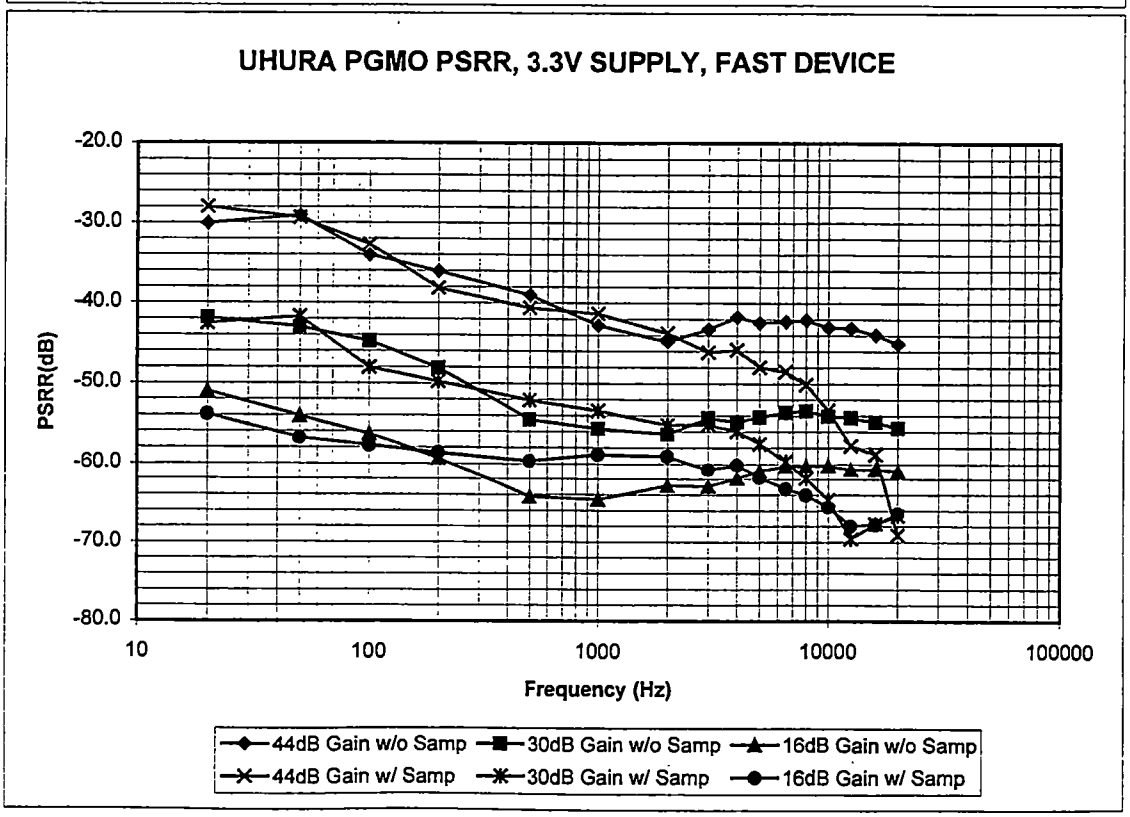

UHURA PGMO PSRR, 3.1V SUPPLY, SLOW DEVICE
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp


UHURA PGMO PSRR, 3.3V SUPPLY, SLOW DEVICE
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

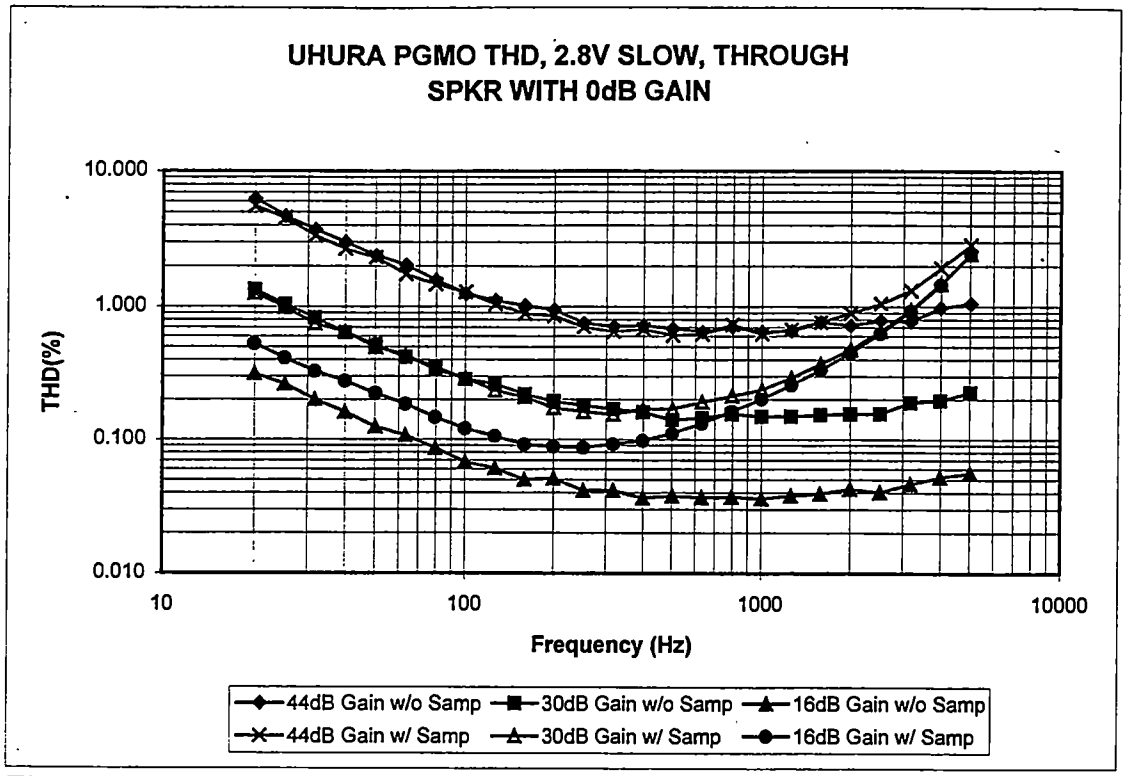

UHURA PGMO PSRR, 3.0V SUPPLY, NOMINAL DEVICE
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

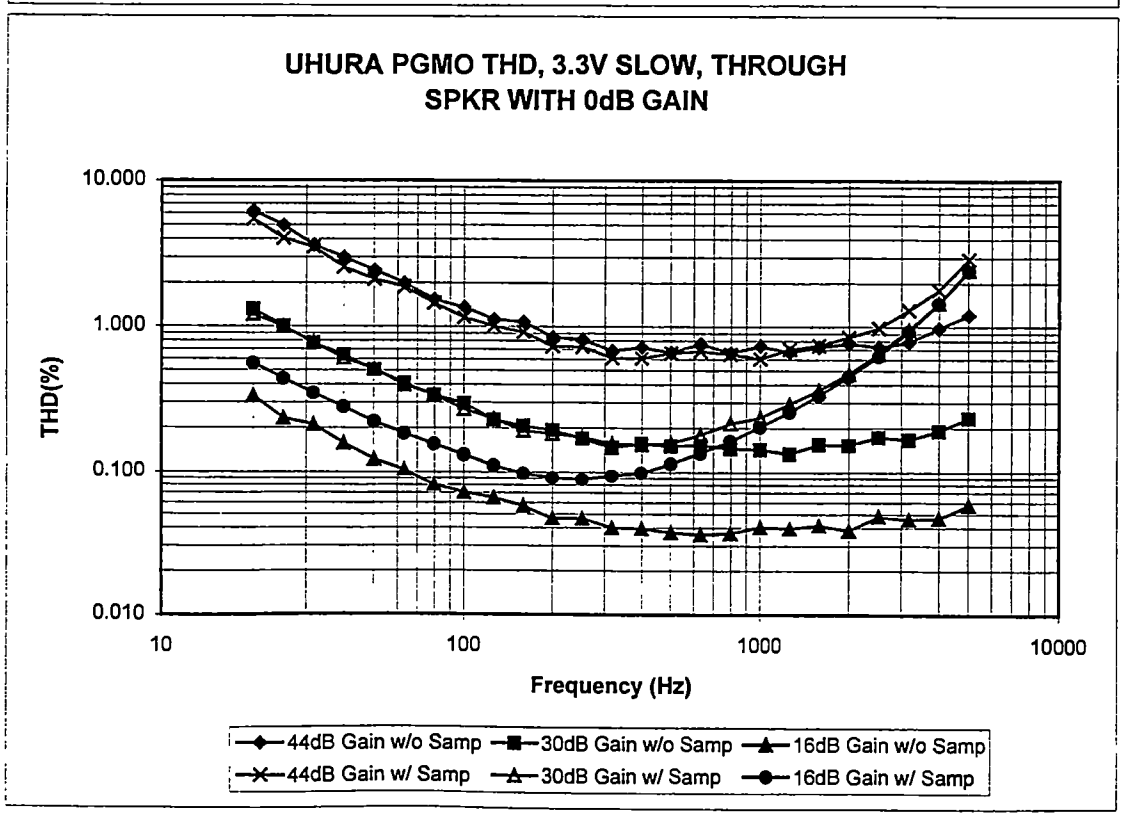

UHURA PGMO PSRR, 3.3V SUPPLY, NOMINAL DEVICE
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

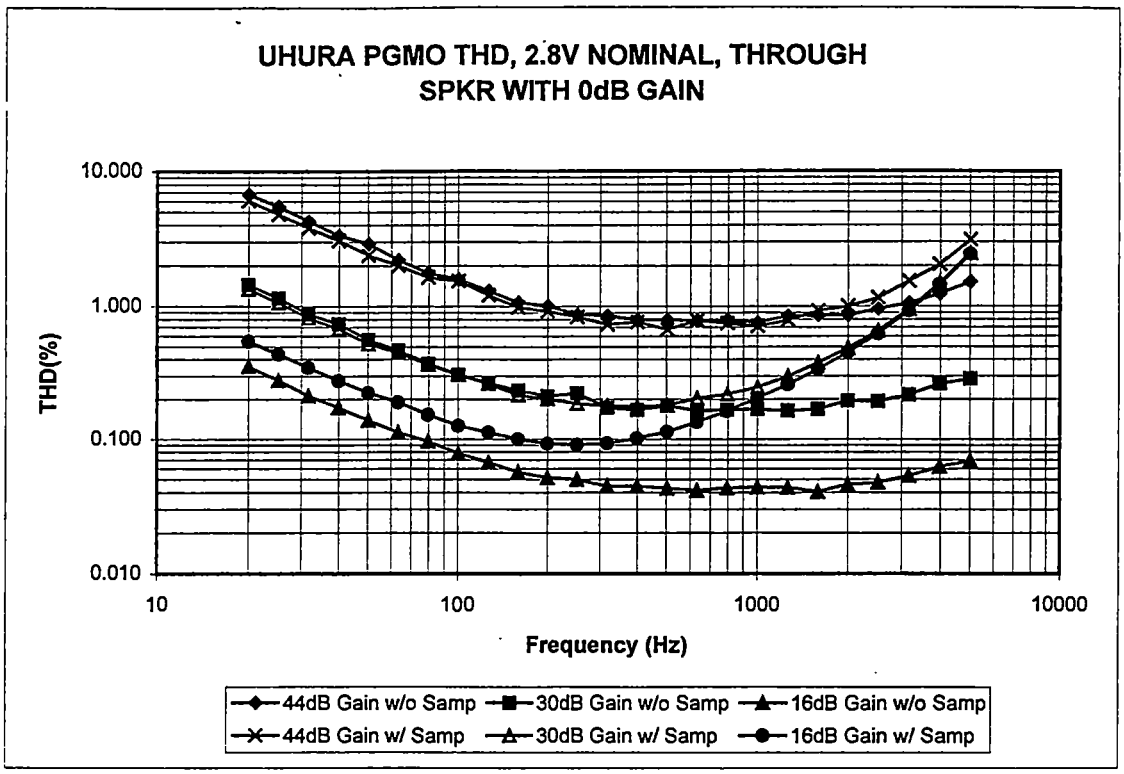

UHURA PGMO PSRR, 3.1V SUPPLY, FAST DEVICE
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

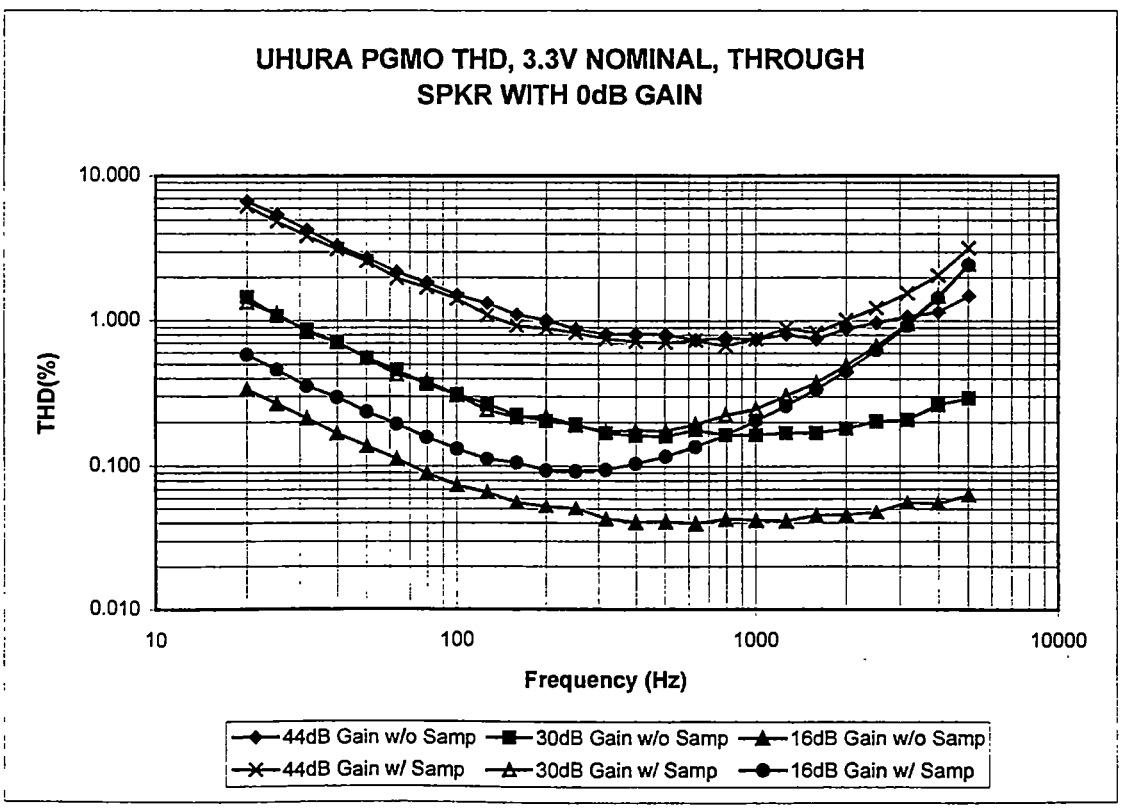

UHURA PGMO PSRR, 3.3V SUPPLY, FAST DEVICE
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

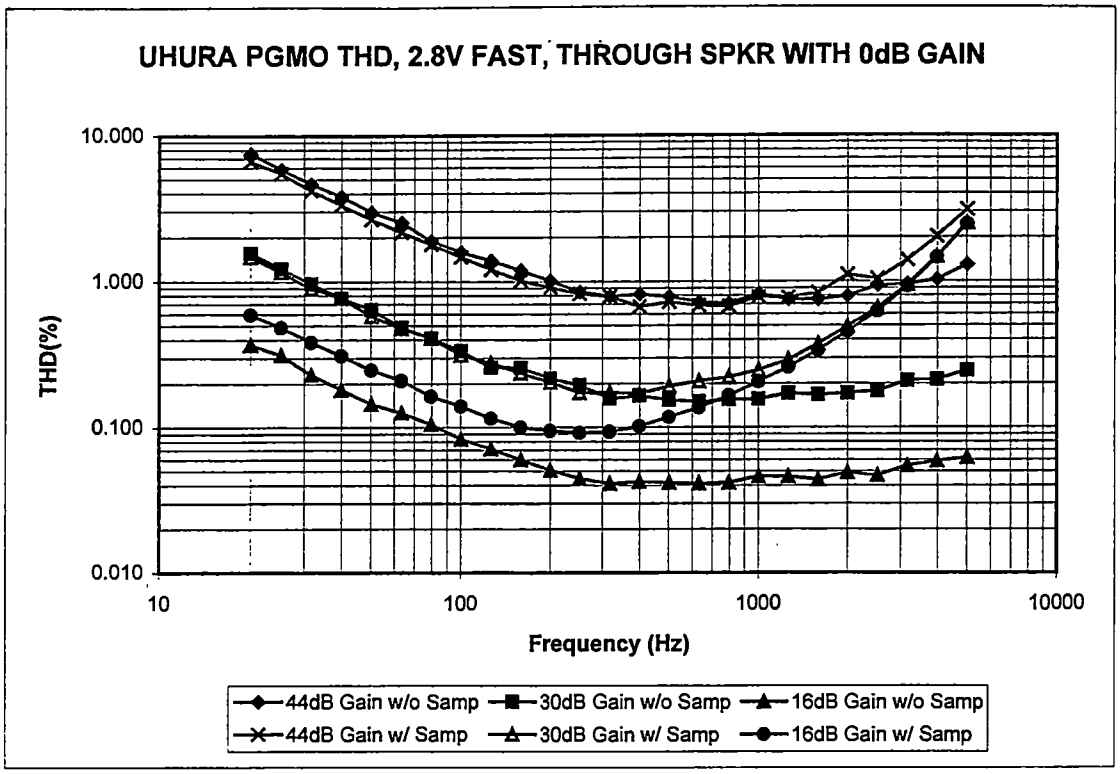
PROGRAMMABLE GAIN MICROPHONE AMPLIFIER THD DATA

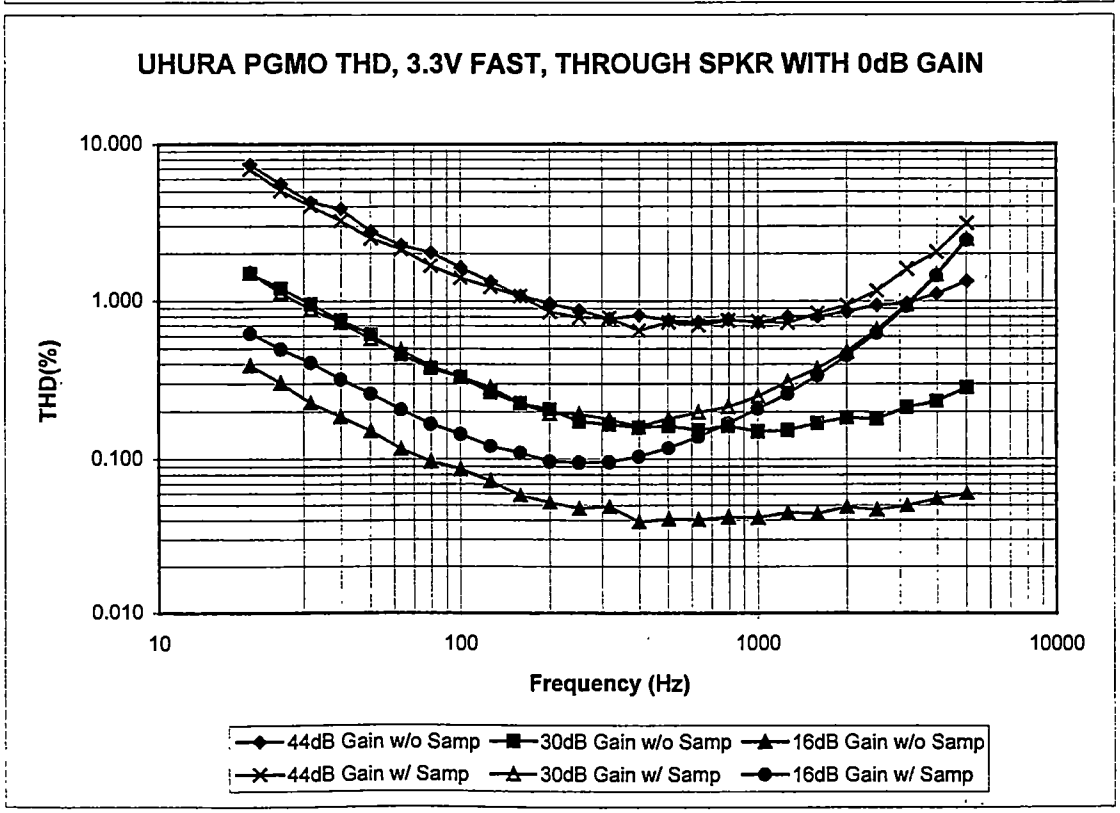

UHURA PGMO THD, 2.8V SLOW, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp


UHURA PGMO THD, 3.3V SLOW, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp


UHURA PGMO THD, 2.8V NOMINAL, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp


UHURA PGMO THD, 3.3V NOMINAL, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp


UHURA PGMO THD, 2.8V FAST, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

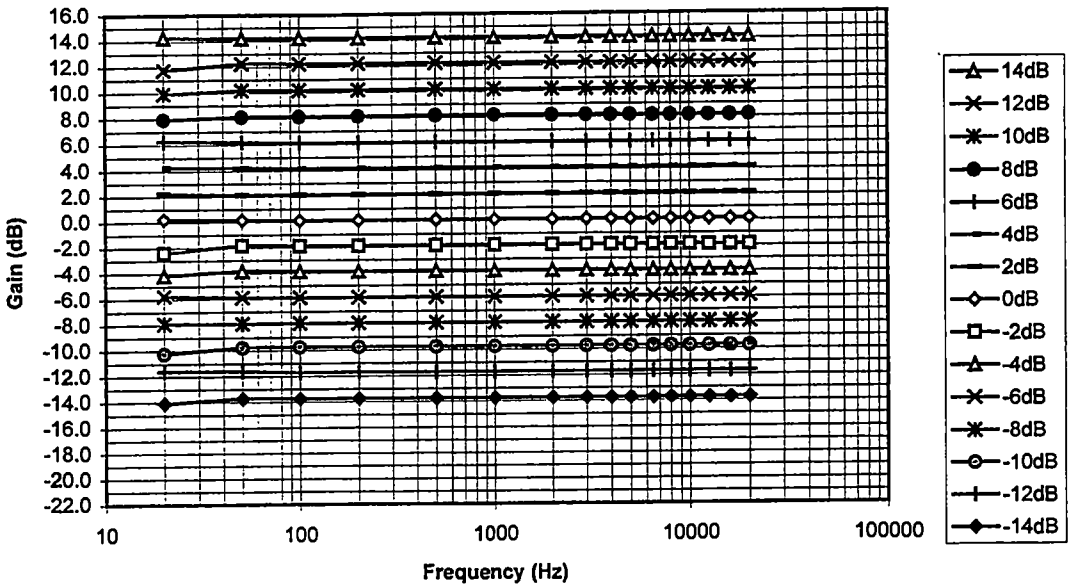

UHURA PGMO THD, 3.3V FAST, THROUGH SPKR WITH 0dB GAIN
10.000
1.000
0.100
0.010
THD(%)
10
100
1000
10000
Frequency (Hz)
44dB Gain w/o Samp
30dB Gain w/o Samp
16dB Gain w/o Samp
44dB Gain w/ Samp
30dB Gain w/ Samp
16dB Gain w/ Samp

APPENDIX I

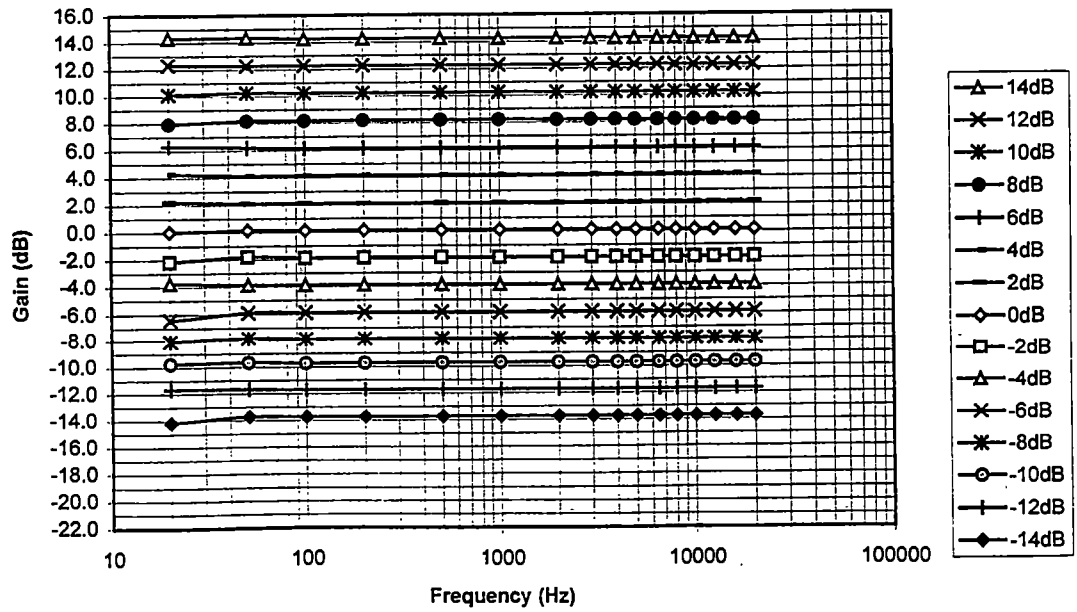
SPEAKER AMPLIFIER DATA

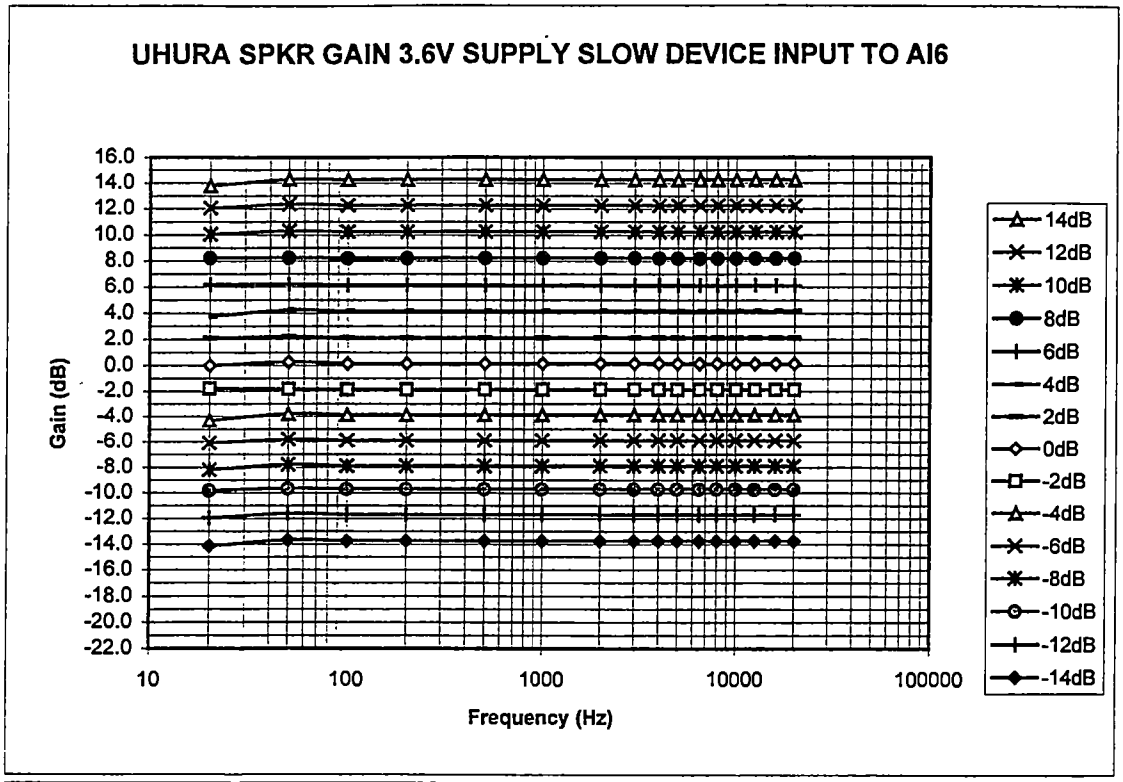
SPEAKER AMPLIFIER GAIN DATA

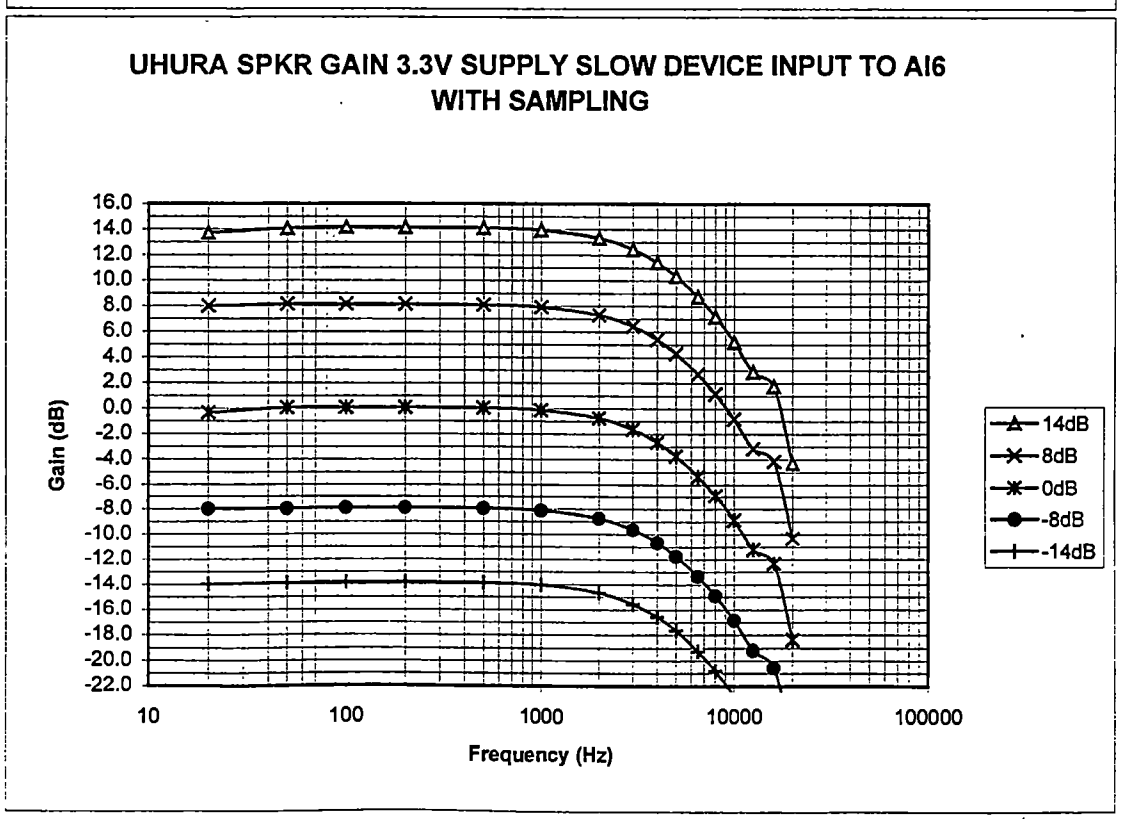
UHURA SPKR GAIN, 3.0V SUPPLY, SLOW DEVICE, INPUT TO AI6



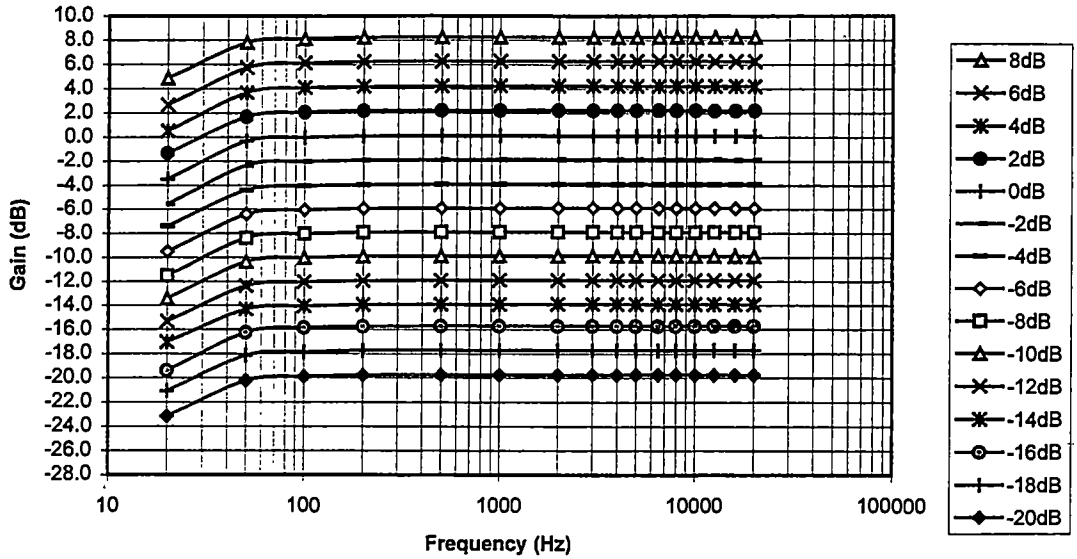
UHURA SPKR GAIN, 3.3V SUPPLY, SLOW DEVICE, INPUT TO AI6



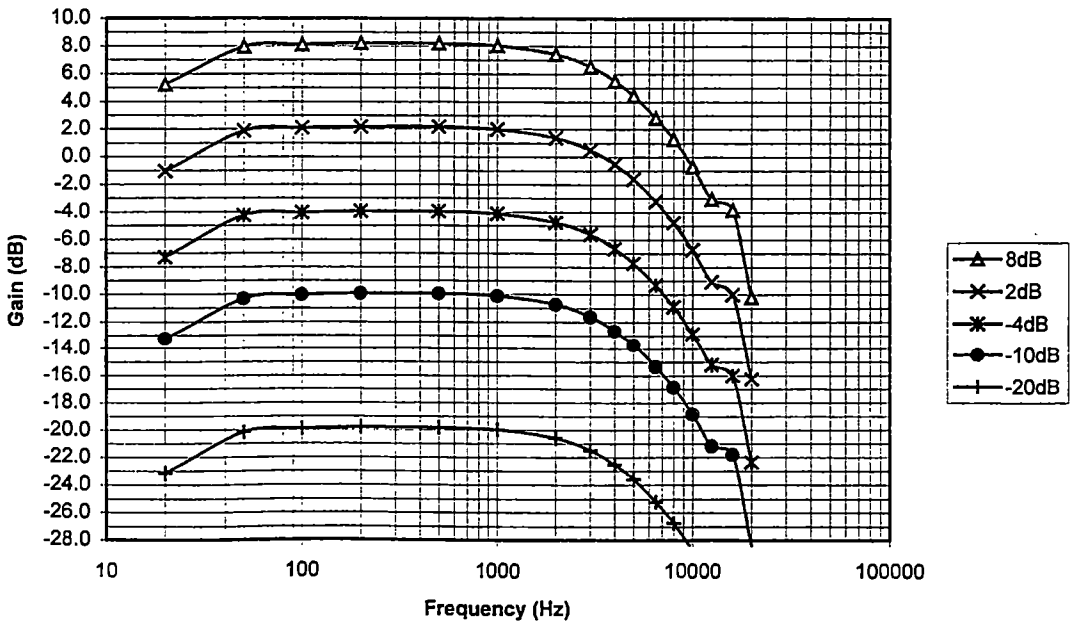

UHURA SPKR GAIN 3.6V SUPPLY SLOW DEVICE INPUT TO AI6
Gain (dB)
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB
-2dB
-4dB
-6dB
-8dB
-10dB
-12dB
-14dB


UHURA SPKR GAIN 3.3V SUPPLY SLOW DEVICE INPUT TO AI6
WITH SAMPLING
Gain (dB)
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
14dB
8dB
0dB
-8dB
-14dB

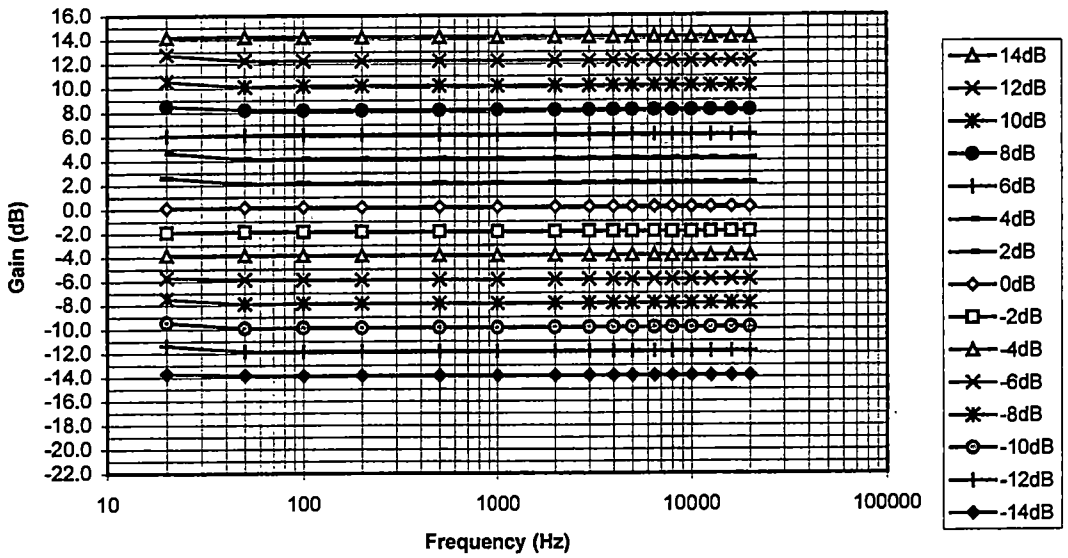
UHURA SPKR GAIN, SINGLE ENDED, 3.3V SUPPLY, SLOW DEVICE, INPUT TO AI6



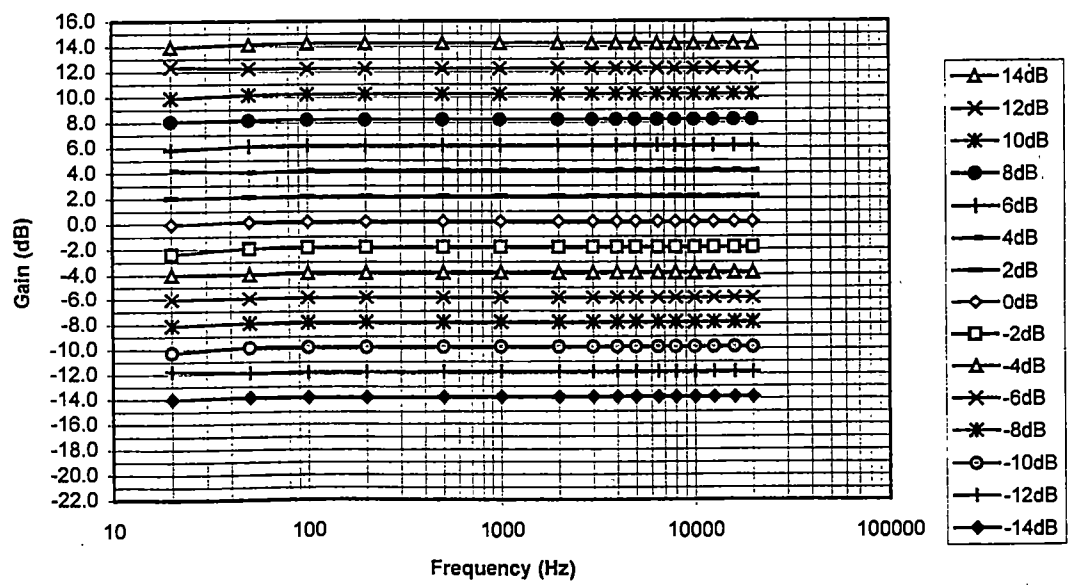
UHURA SPKR GAIN, SINGLE ENDED, 3.3V SUPPLY, SLOW DEVICE, INPUT TO AI6, WITH SAMPLING



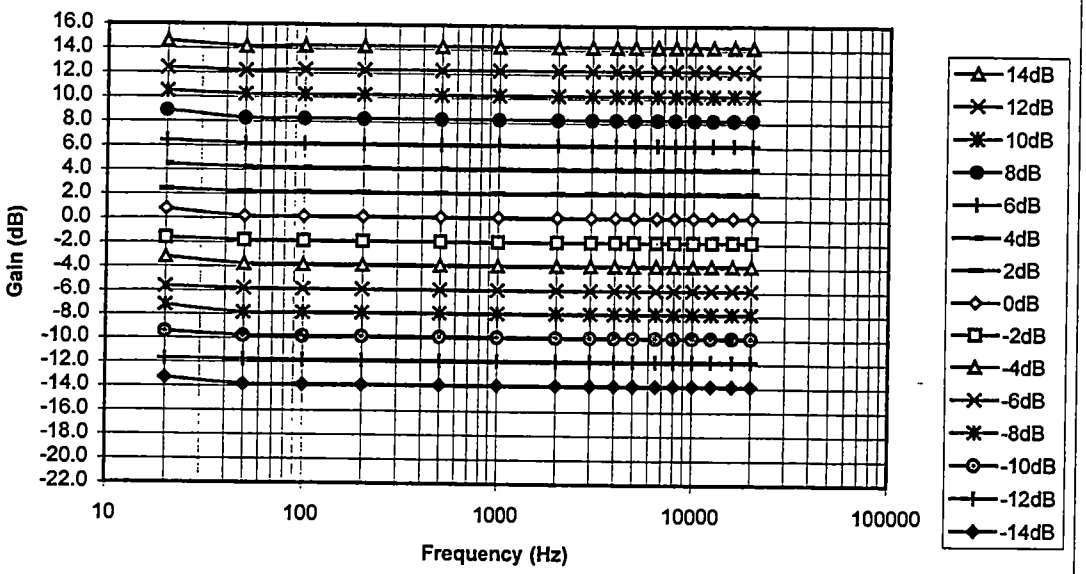
UHURA SPKR GAIN, 3.0V SUPPLY, NOMINAL DEVICE, INPUT TO AI6



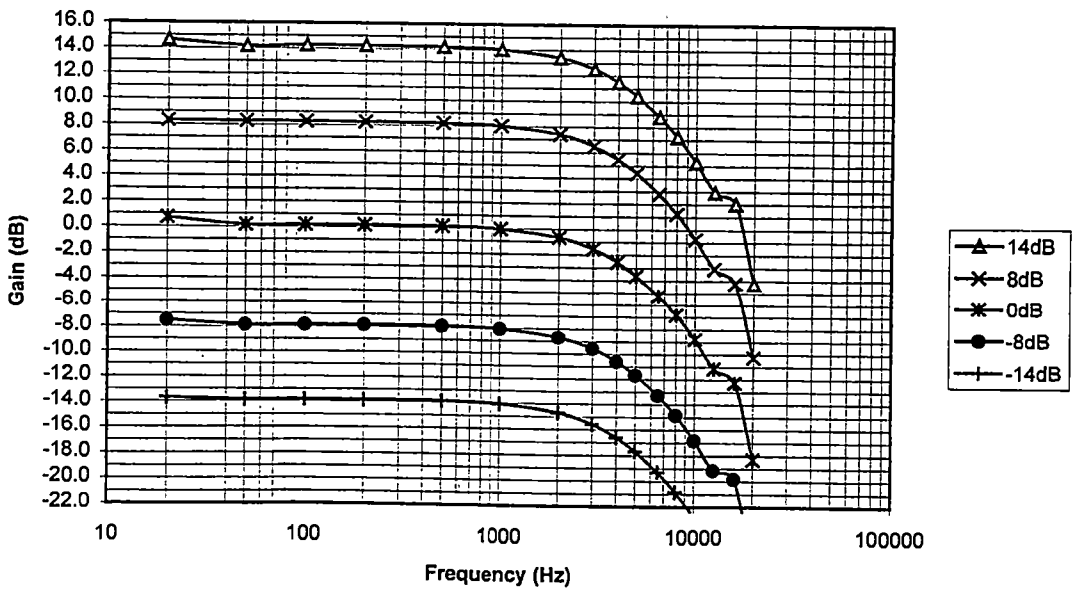
UHURA SPKR GAIN, 3.3V SUPPLY, NOMINAL DEVICE, INPUT TO AI6



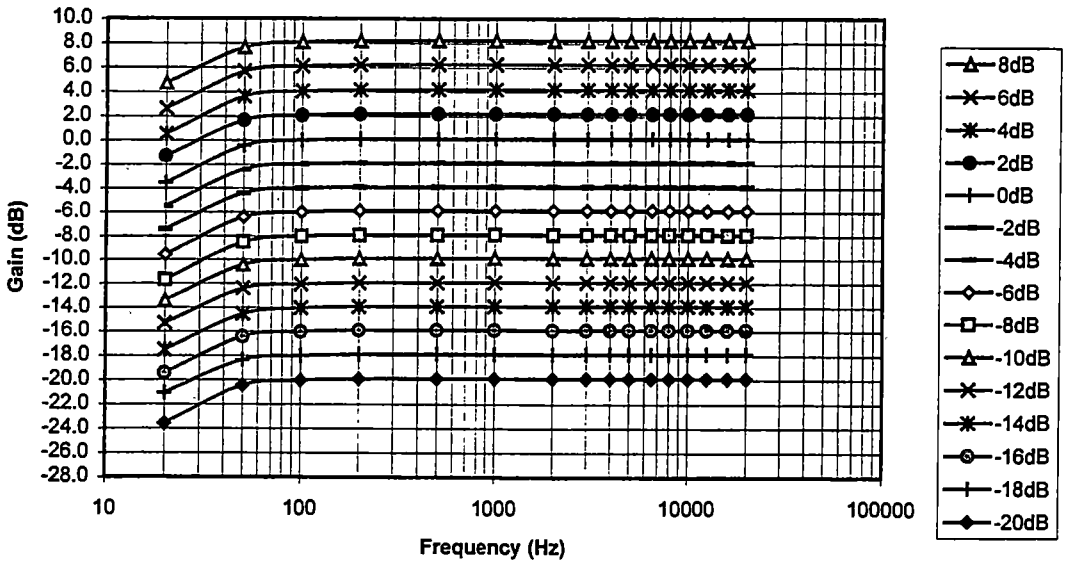
UHURA SPKR GAIN, 3.6V SUPPLY, NOMINAL DEVICE, INPUT TO AI6



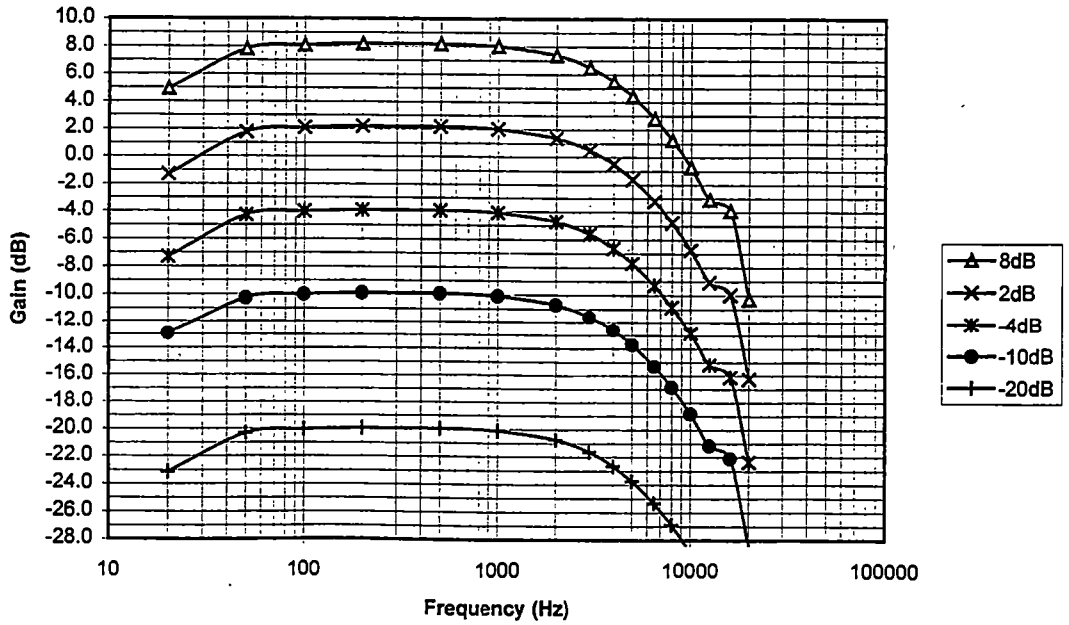
UHURA SPKR GAIN, 3.3V SUPPLY, NOMINAL DEVICE, INPUT TO AI6, WITH SAMPLING

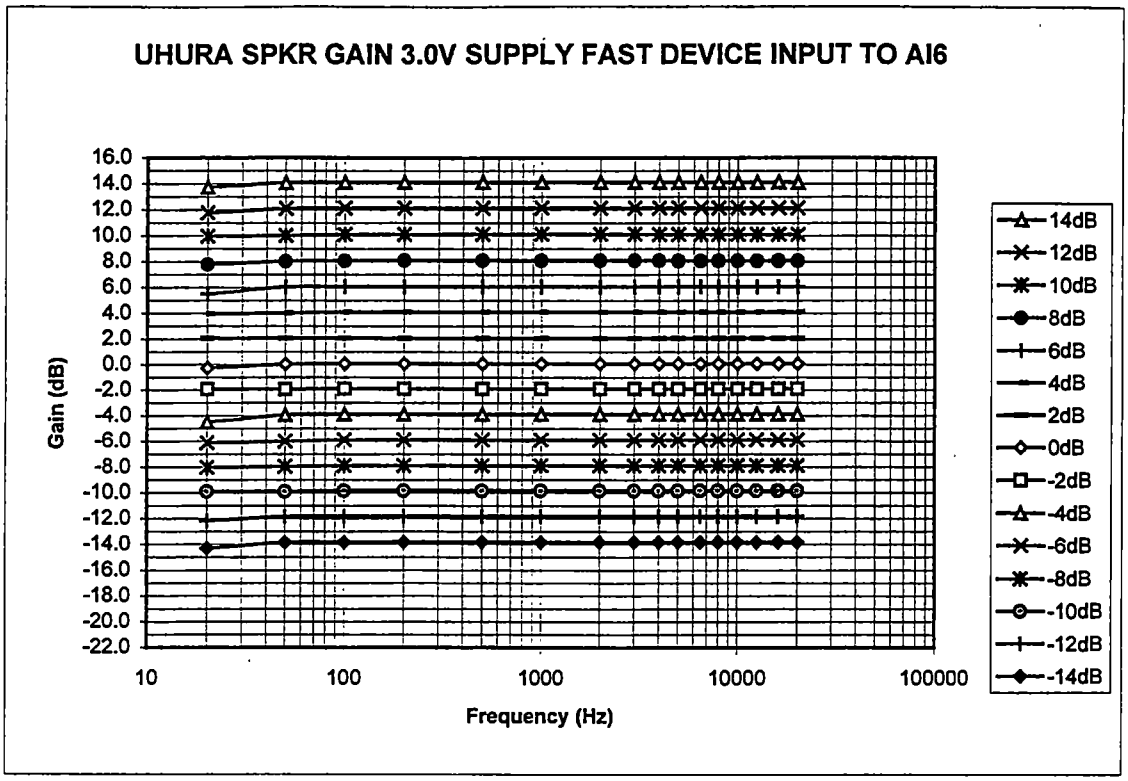


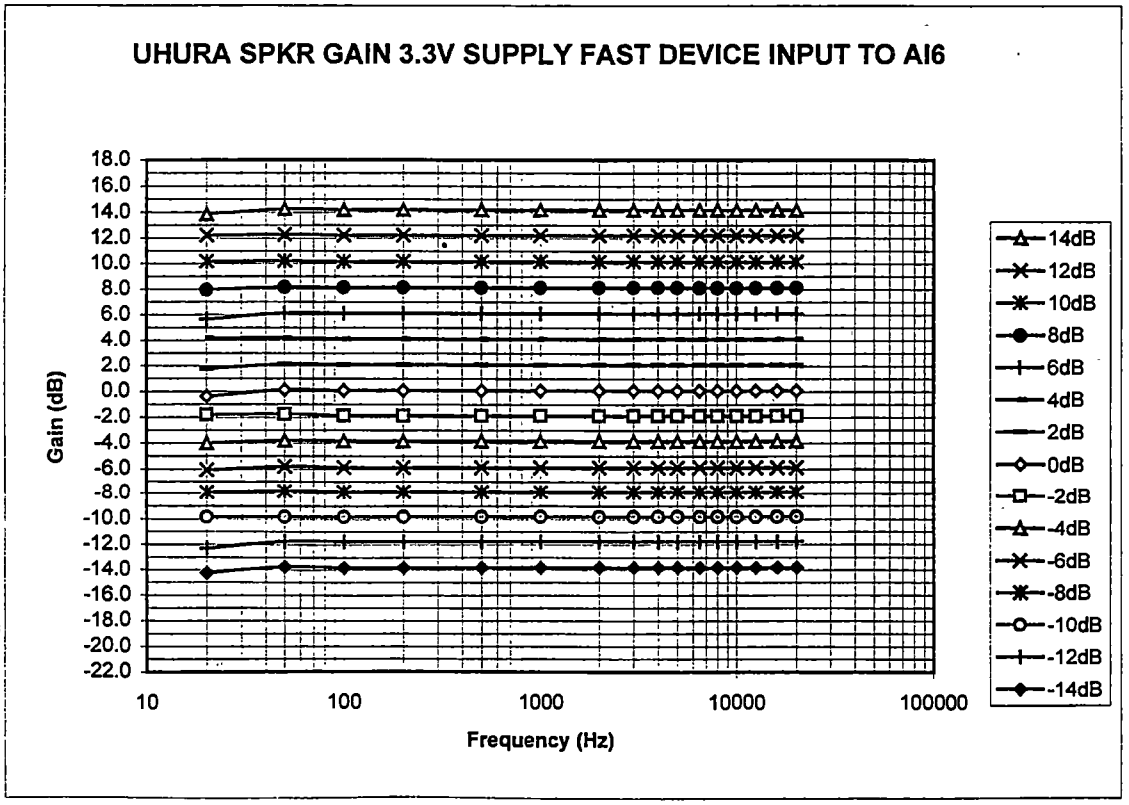
UHURA SPKR GAIN, SINGLE ENDED, 3.3V SUPPLY, NOMINAL DEVICE, INPUT TO AI6

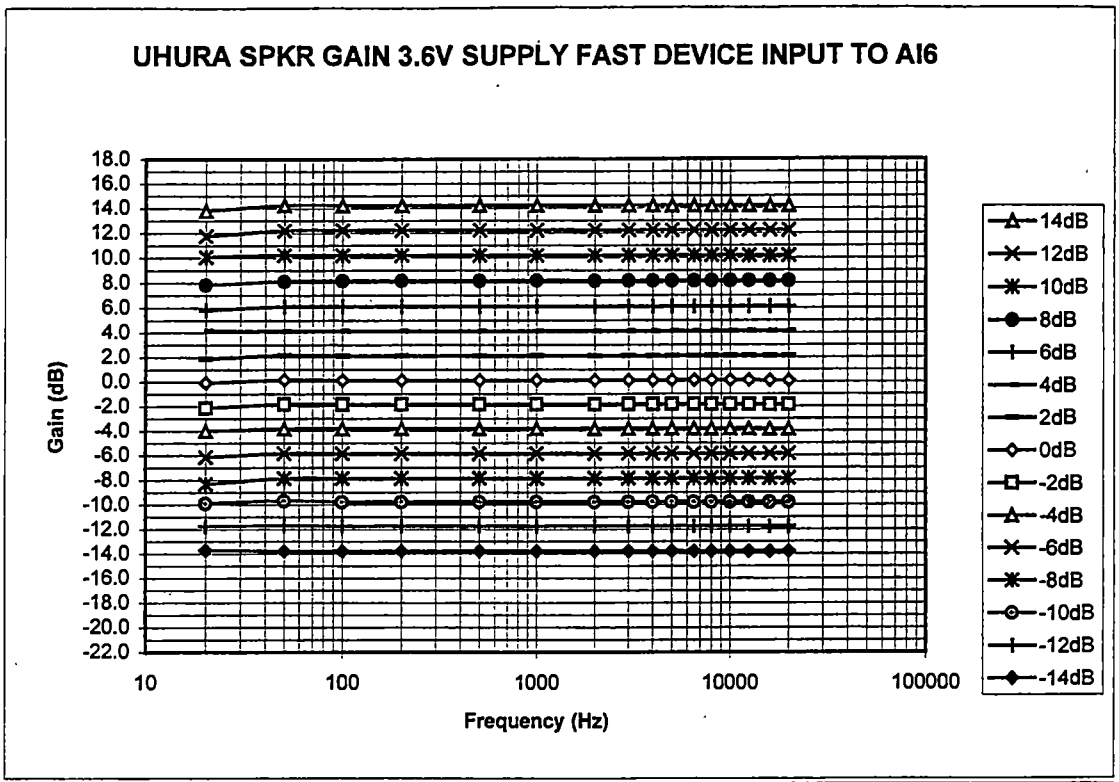


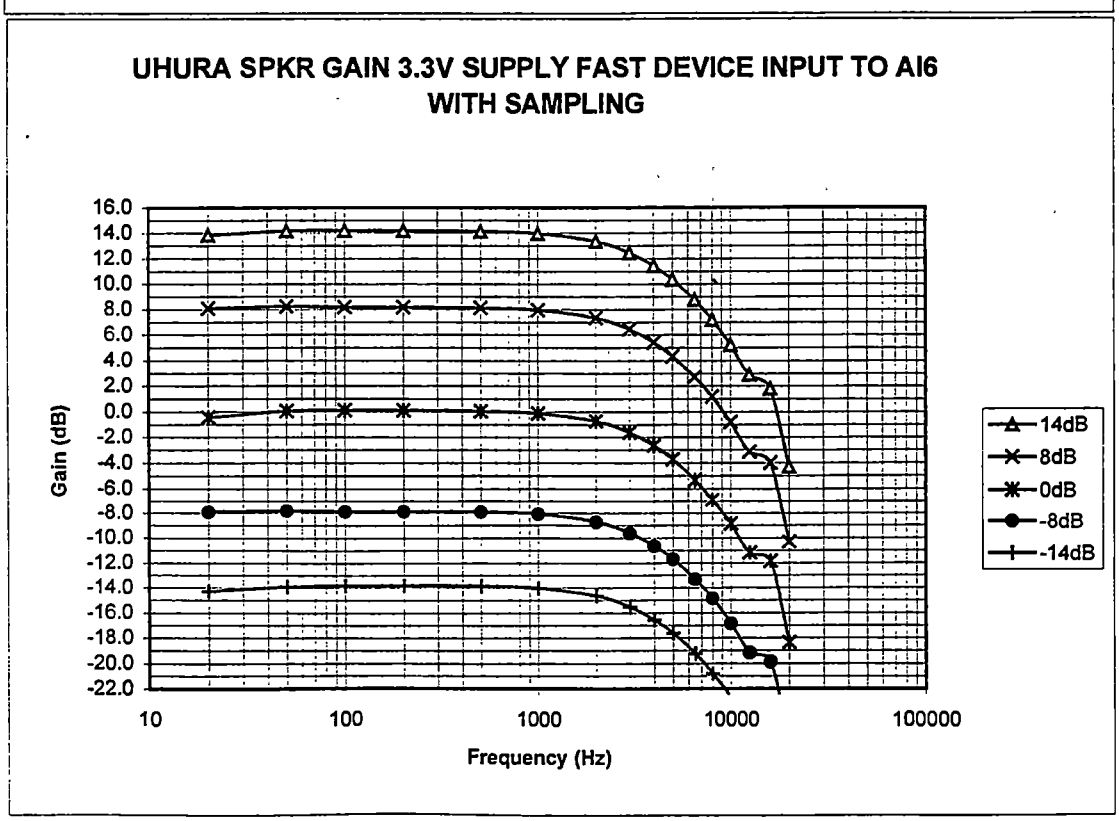
UHURA SPKR GAIN, SINGLE ENDED, 3.3V SUPPLY, NOMINAL DEVICE, INPUT TO AI6, WITH SAMPLING

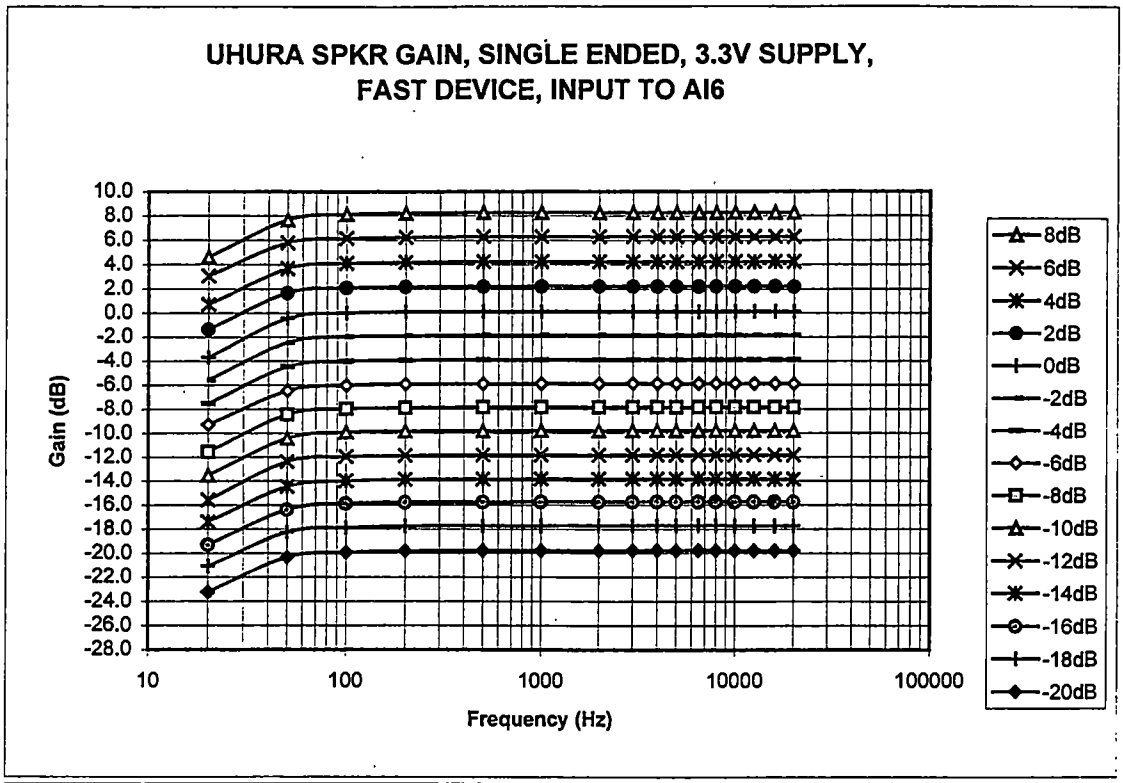


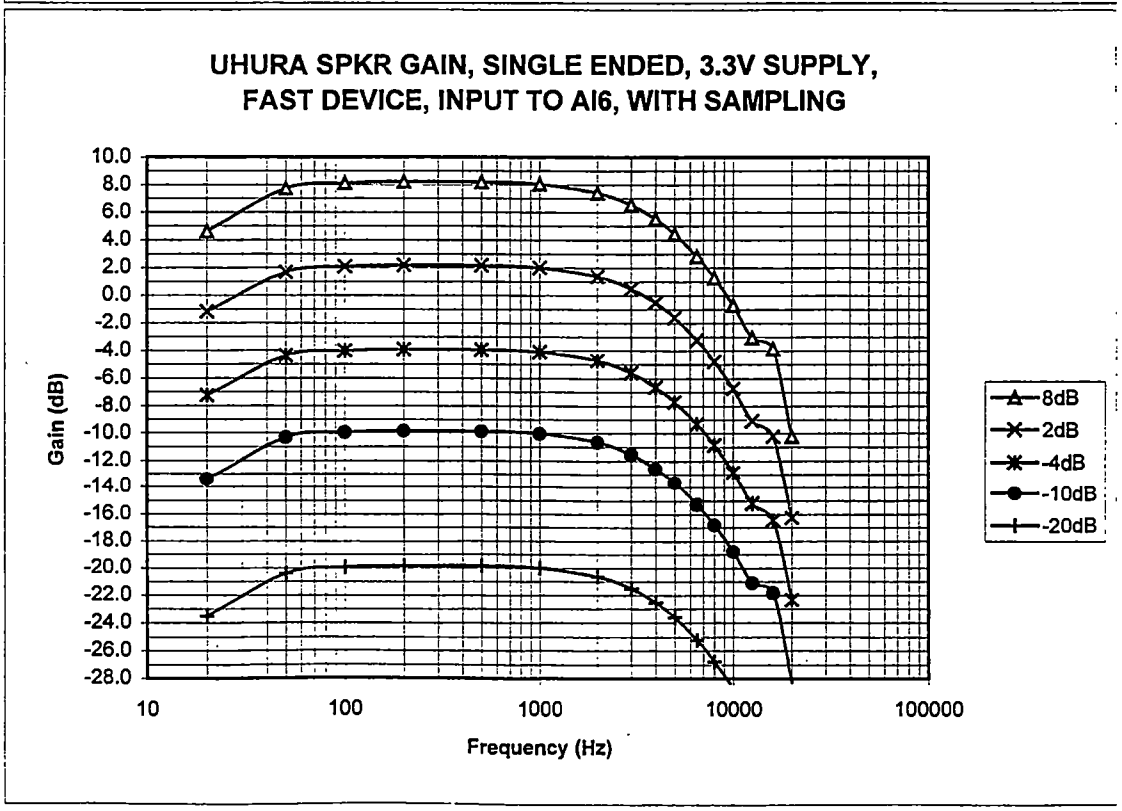

UHURA SPKR GAIN 3.0V SUPPLY FAST DEVICE INPUT TO AI6
Gain (dB)
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB
-2dB
-4dB
-6dB
-8dB
-10dB
-12dB
-14dB

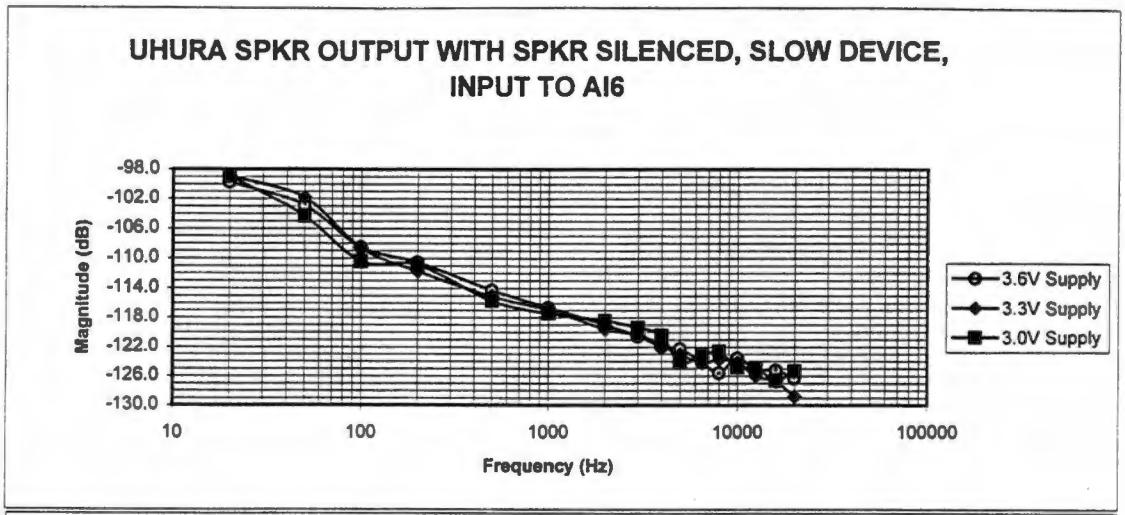

UHURA SPKR GAIN 3.3V SUPPLY FAST DEVICE INPUT TO AI6
Gain (dB)
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB
-2dB
-4dB
-6dB
-8dB
-10dB
-12dB
-14dB

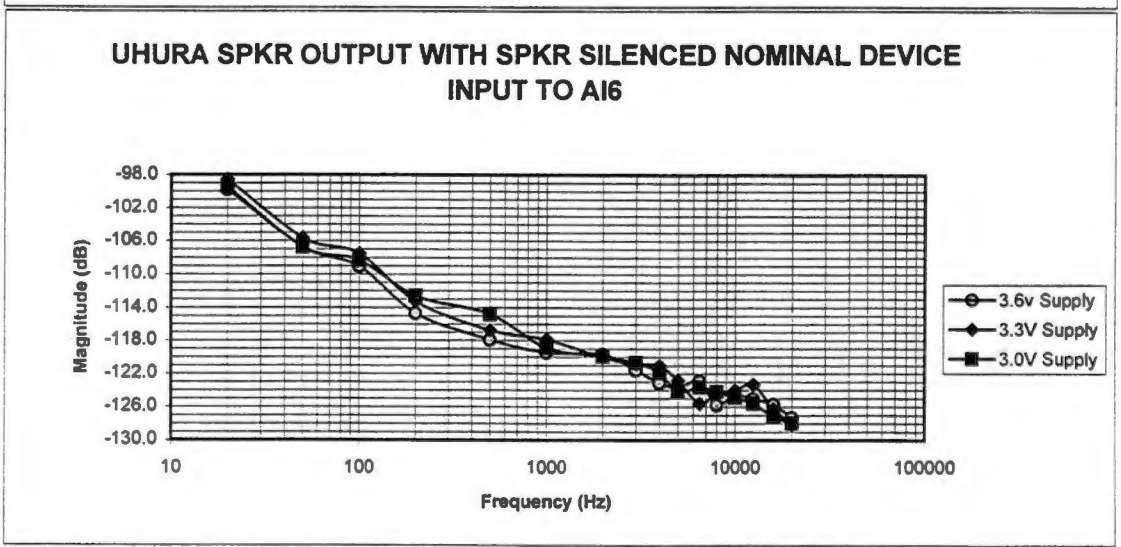

UHURA SPKR GAIN 3.6V SUPPLY FAST DEVICE INPUT TO AI6
Gain (dB)
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
14dB
12dB
10dB
8dB
6dB
4dB
2dB
0dB
-2dB
-4dB
-6dB
-8dB
-10dB
-12dB
-14dB

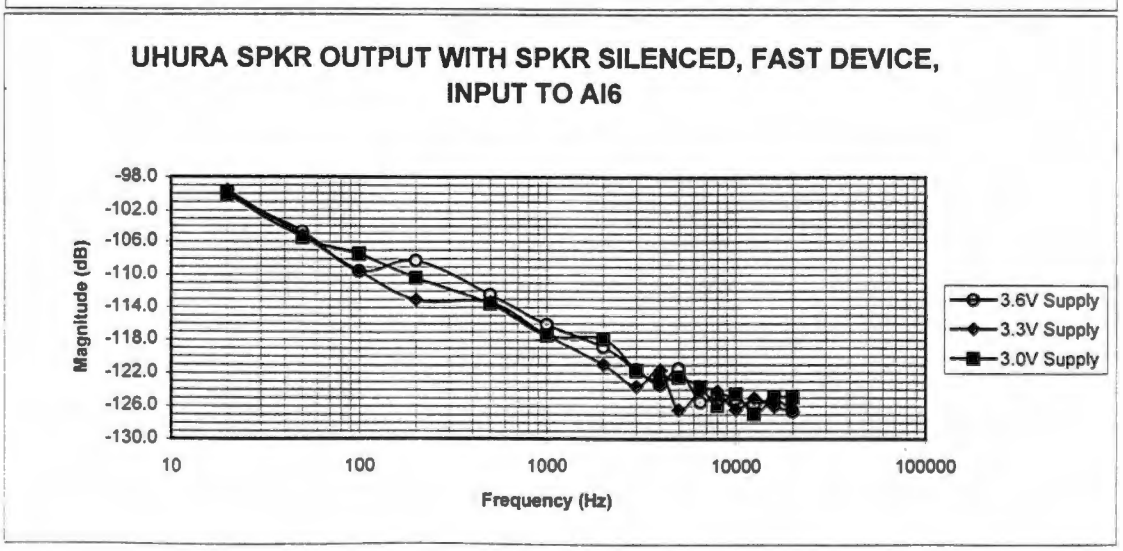

UHURA SPKR GAIN 3.3V SUPPLY FAST DEVICE INPUT TO AI6
WITH SAMPLING
Gain (dB)
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
10
100
1000
10000
100000
Frequency (Hz)
14dB
8dB
0dB
-8dB
-14dB


UHURA SPKR GAIN, SINGLE ENDED, 3.3V SUPPLY,
FAST DEVICE, INPUT TO AI6
Gain (dB)
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
-24.0
-26.0
-28.0
10
100
1000
10000
100000
Frequency (Hz)
8dB
6dB
4dB
2dB
0dB
-2dB
-4dB
-6dB
-8dB
-10dB
-12dB
-14dB
-16dB
-18dB
-20dB

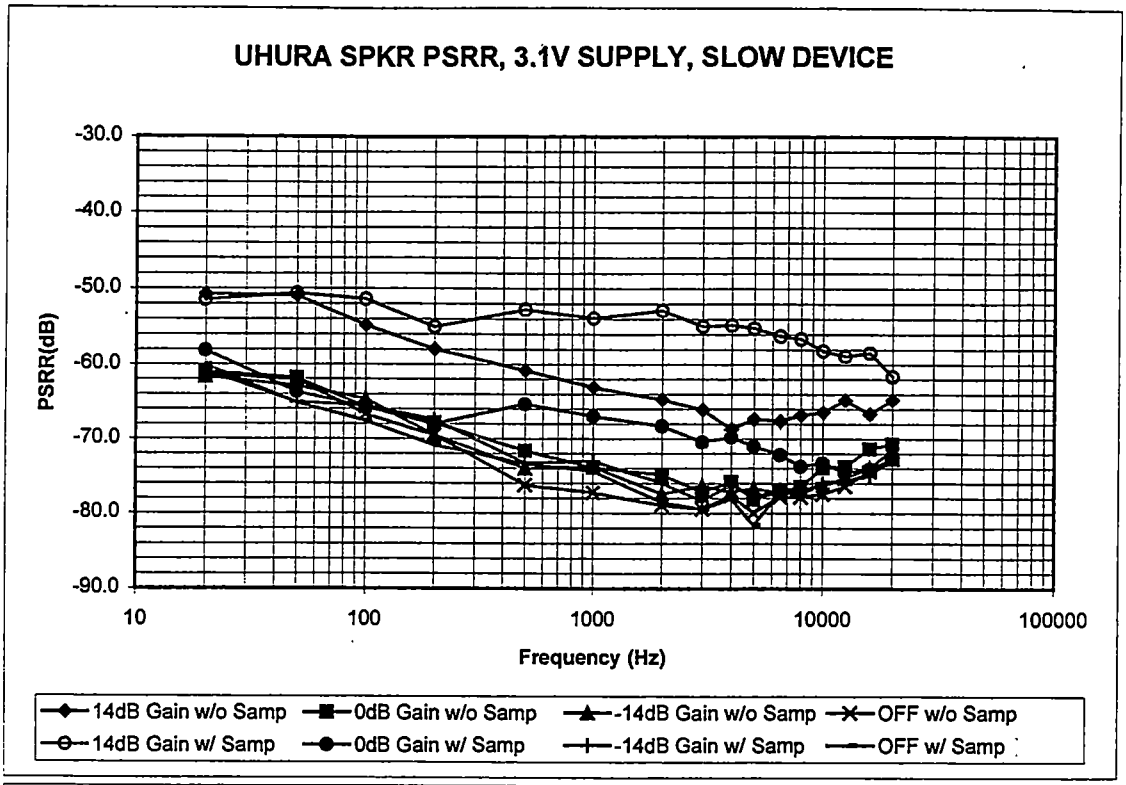

UHURA SPKR GAIN, SINGLE ENDED, 3.3V SUPPLY,
FAST DEVICE, INPUT TO AI6, WITH SAMPLING
Gain (dB)
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
-22.0
-24.0
-26.0
-28.0
10
100
1000
10000
100000
Frequency (Hz)
8dB
2dB
-4dB
-10dB
-20dB

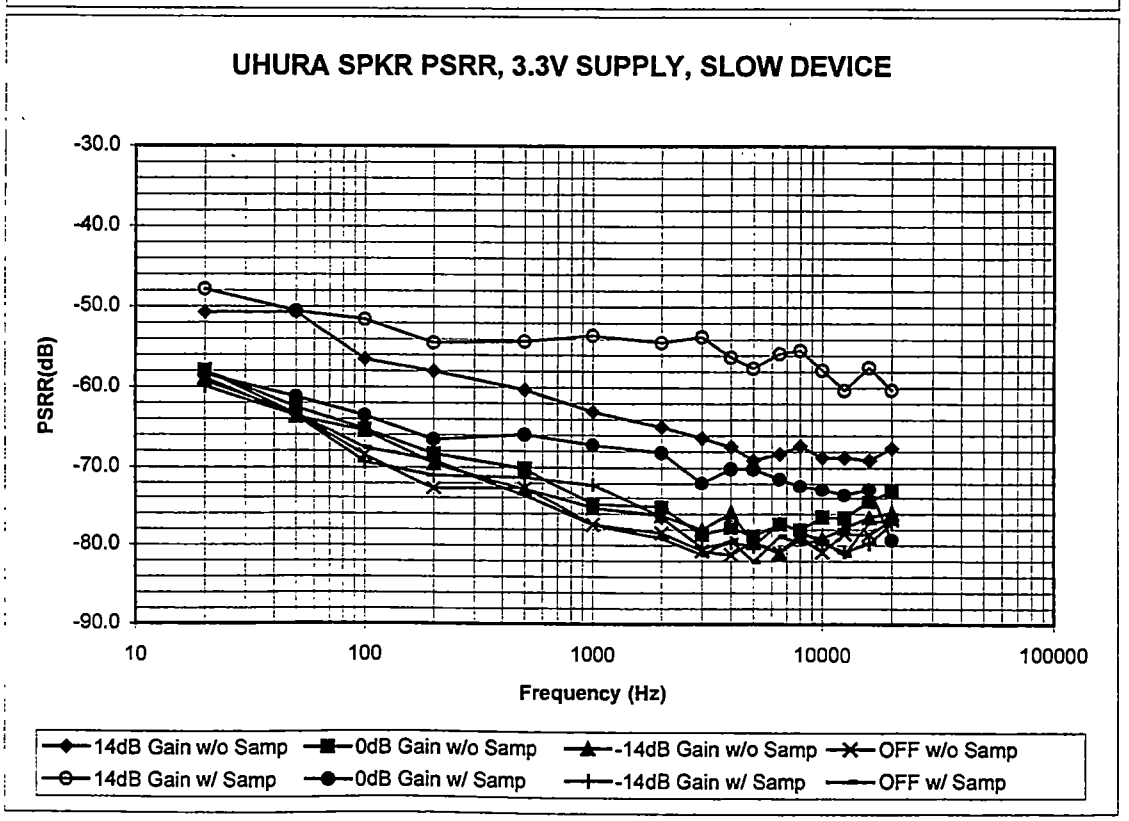

UHURA SPKR OUTPUT WITH SPKR SILENCED, SLOW DEVICE, INPUT TO AI6
-98.0
-102.0
-106.0
-110.0
-114.0
-118.0
-122.0
-126.0
-130.0
Magnitude (dB)
10
100
1000
10000
100000
Frequency (Hz)
3.6V Supply
3.3V Supply
3.0V Supply

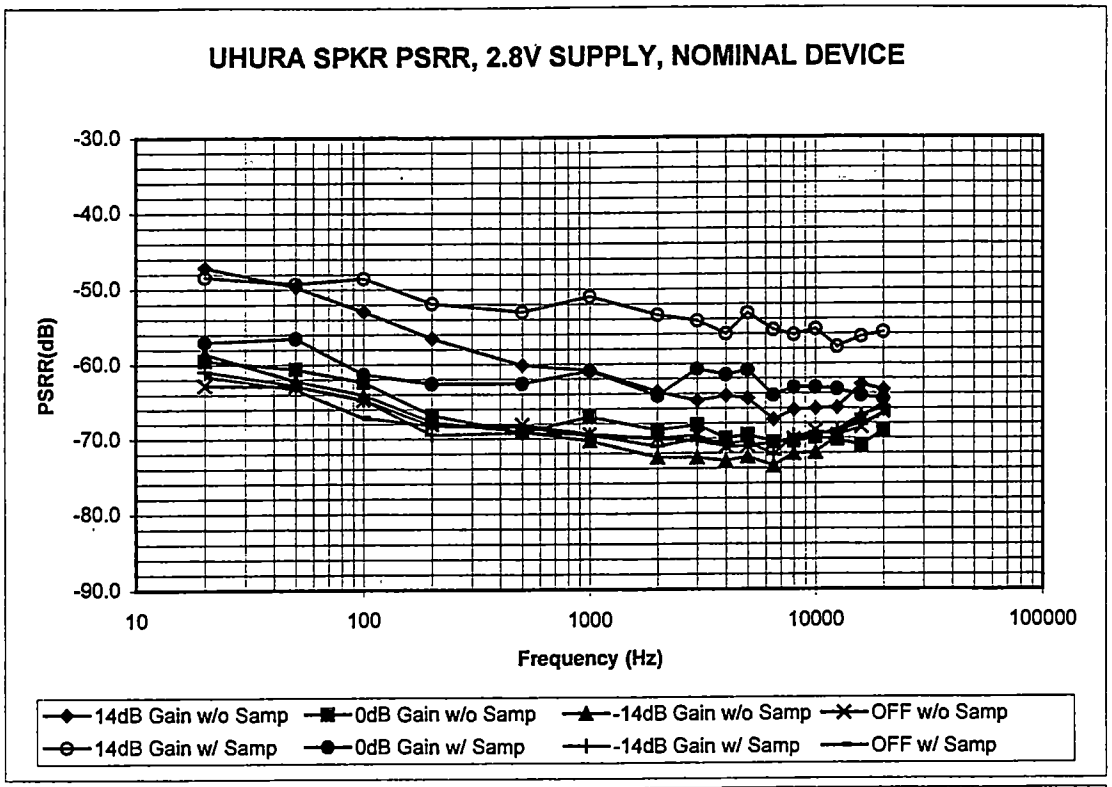

UHURA SPKR OUTPUT WITH SPKR SILENCED NOMINAL DEVICE INPUT TO AI6
-98.0
-102.0
-106.0
-110.0
-114.0
-118.0
-122.0
-126.0
-130.0
Magnitude (dB)
10
100
1000
10000
100000
Frequency (Hz)
3.6v Supply
3.3V Supply
3.0V Supply

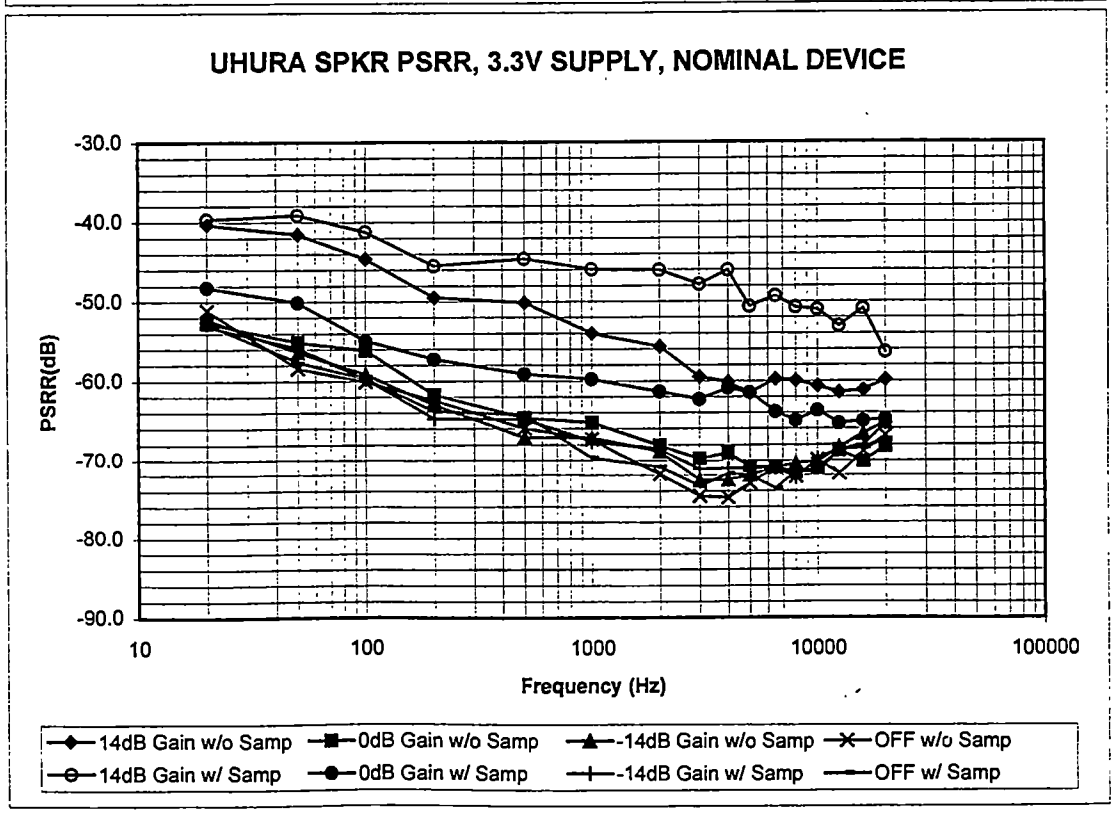

UHURA SPKR OUTPUT WITH SPKR SILENCED, FAST DEVICE, INPUT TO AI6
-98.0
-102.0
-106.0
-110.0
-114.0
-118.0
-122.0
-126.0
-130.0
Magnitude (dB)
10
100
1000
10000
100000
Frequency (Hz)
3.6V Supply
3.3V Supply
3.0V Supply

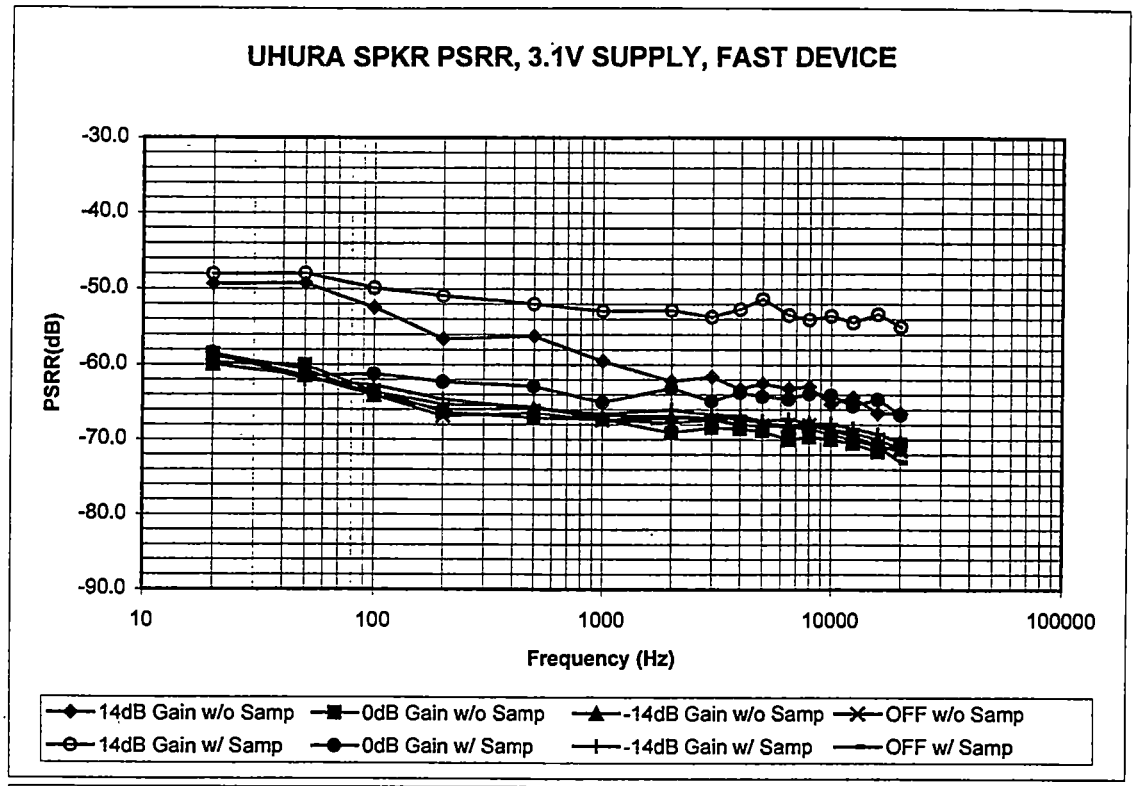
SPEAKER AMPLIFIER PSRR DATA

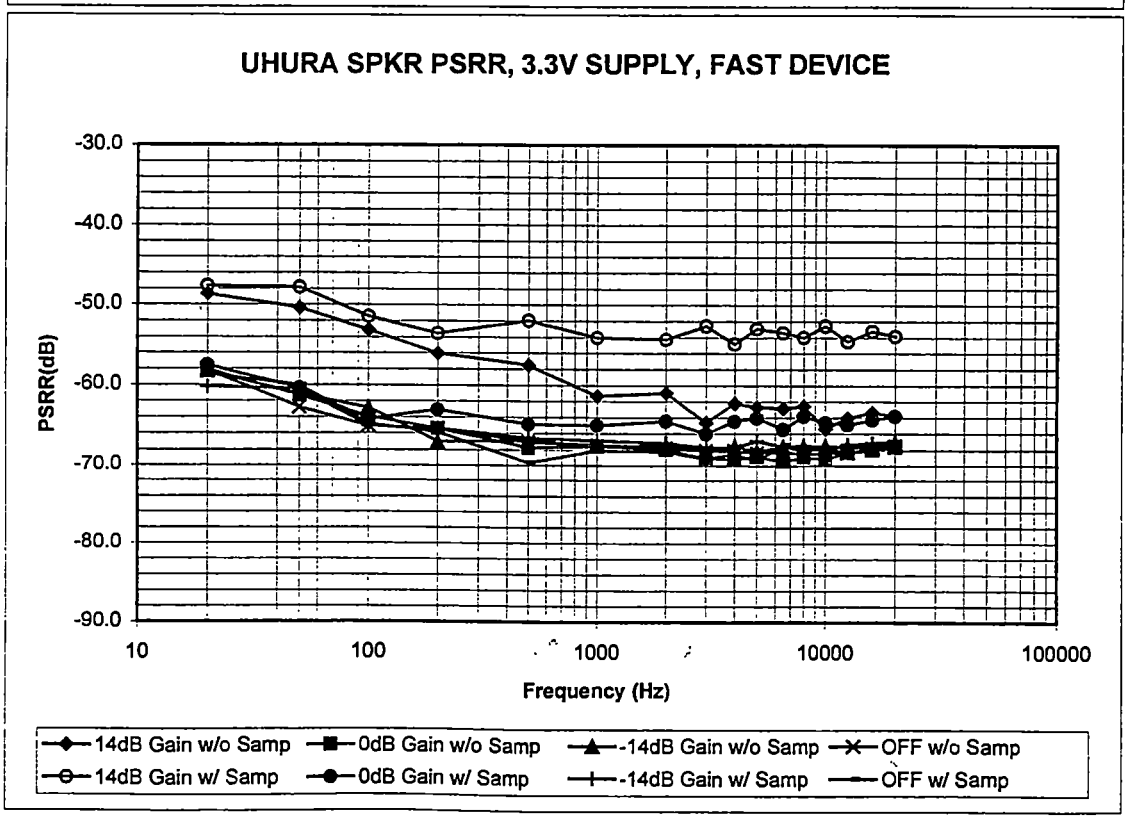

UHURA SPKR PSRR, 3.1V SUPPLY, SLOW DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
14dB Gain w/o Samp
0dB Gain w/o Samp
-14dB Gain w/o Samp
OFF w/o Samp
14dB Gain w/ Samp
0dB Gain w/ Samp
-14dB Gain w/ Samp
OFF w/ Samp

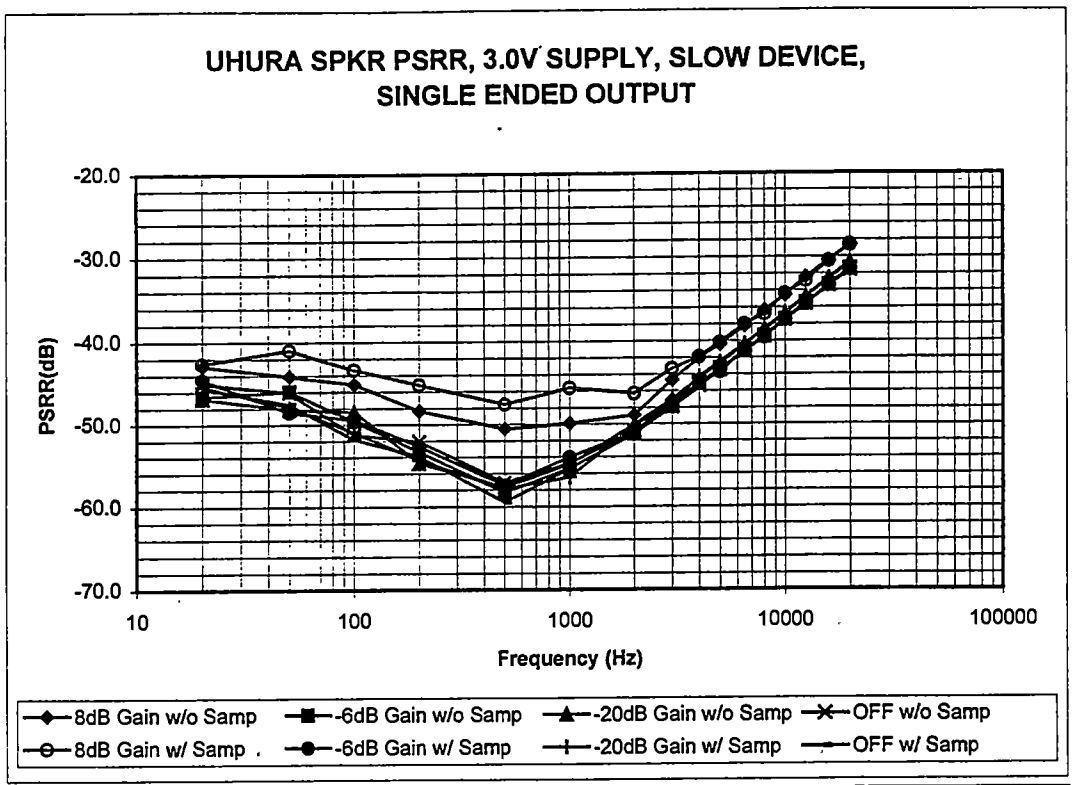

UHURA SPKR PSRR, 3.3V SUPPLY, SLOW DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
14dB Gain w/o Samp
0dB Gain w/o Samp
-14dB Gain w/o Samp
OFF w/o Samp
14dB Gain w/ Samp
0dB Gain w/ Samp
-14dB Gain w/ Samp
OFF w/ Samp

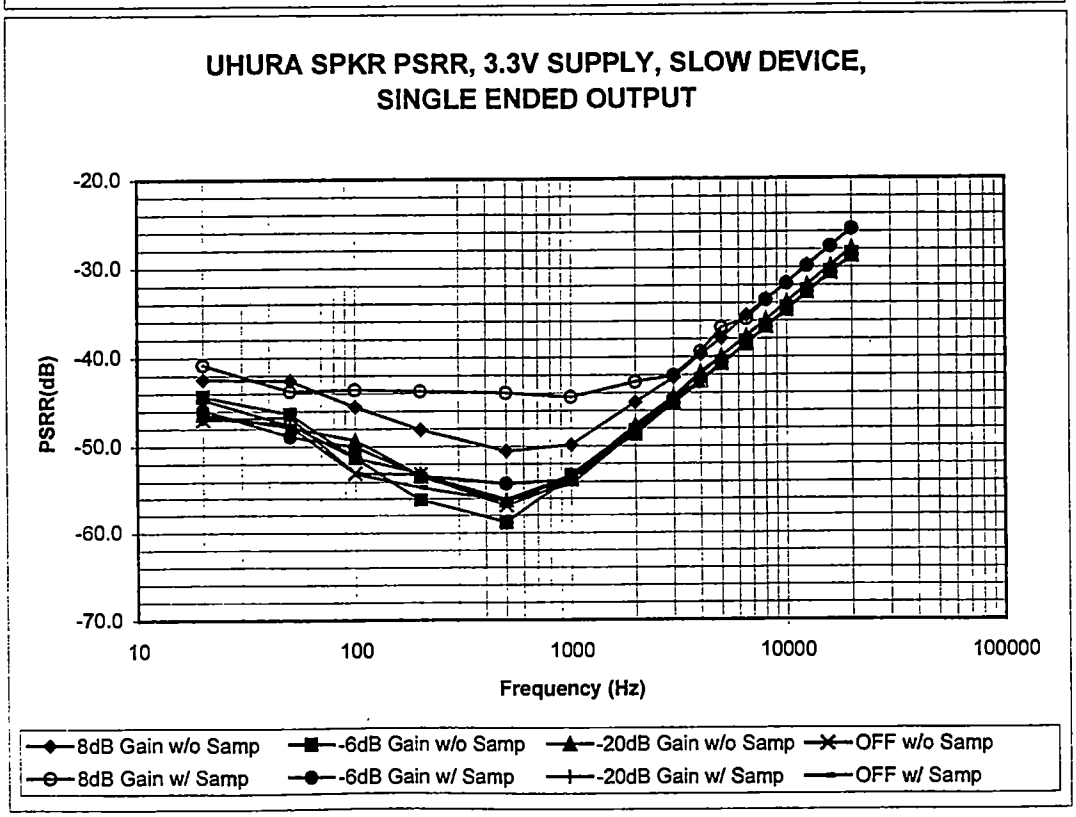

UHURA SPKR PSRR, 2.8V SUPPLY, NOMINAL DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
14dB Gain w/o Samp
0dB Gain w/o Samp
-14dB Gain w/o Samp
OFF w/o Samp
14dB Gain w/ Samp
0dB Gain w/ Samp
-14dB Gain w/ Samp
OFF w/ Samp

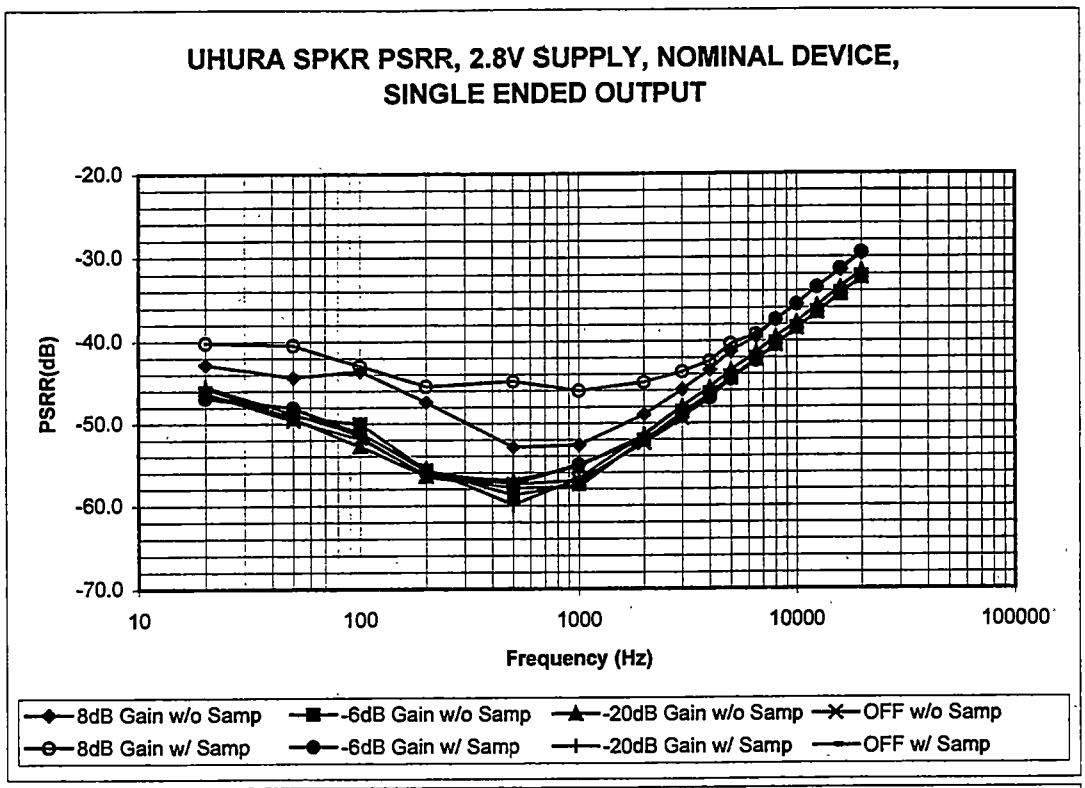

UHURA SPKR PSRR, 3.3V SUPPLY, NOMINAL DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
14dB Gain w/o Samp
0dB Gain w/o Samp
-14dB Gain w/o Samp
OFF w/o Samp
14dB Gain w/ Samp
0dB Gain w/ Samp
-14dB Gain w/ Samp
OFF w/ Samp

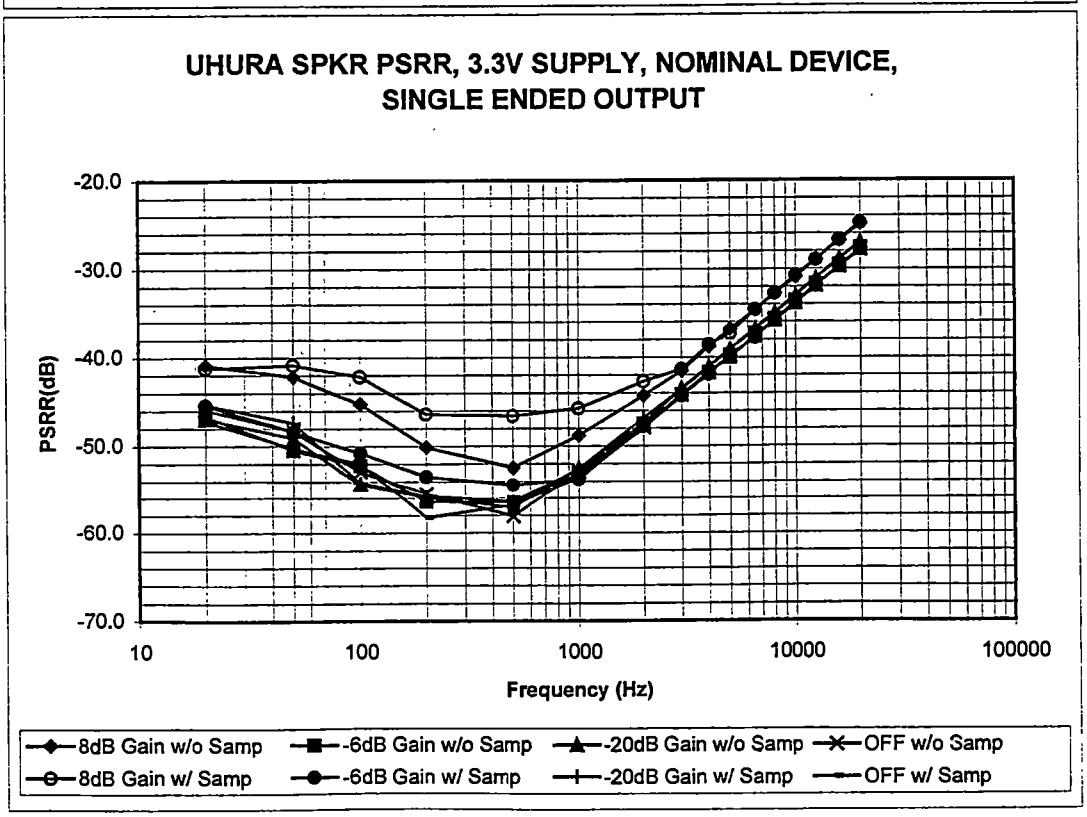

UHURA SPKR PSRR, 3.1V SUPPLY, FAST DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
14dB Gain w/o Samp
0dB Gain w/o Samp
-14dB Gain w/o Samp
OFF w/o Samp
14dB Gain w/ Samp
0dB Gain w/ Samp
-14dB Gain w/ Samp
OFF w/ Samp


UHURA SPKR PSRR, 3.3V SUPPLY, FAST DEVICE
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
14dB Gain w/o Samp
0dB Gain w/o Samp
-14dB Gain w/o Samp
OFF w/o Samp
14dB Gain w/ Samp
0dB Gain w/ Samp
-14dB Gain w/ Samp
OFF w/ Samp

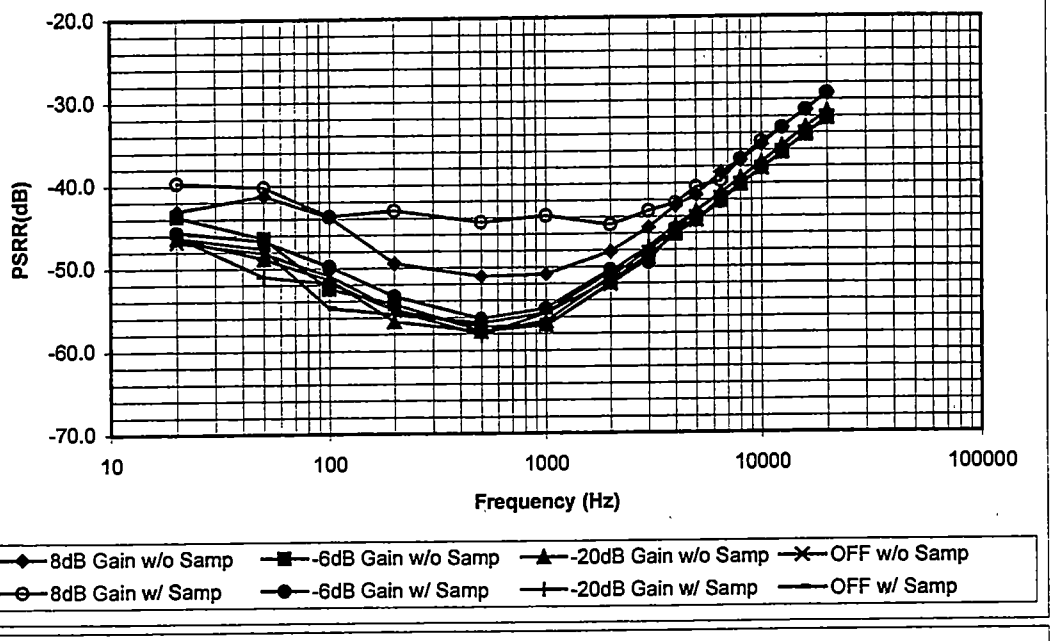

UHURA SPKR PSRR, 3.0V SUPPLY, SLOW DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
8dB Gain w/o Samp
-6dB Gain w/o Samp
-20dB Gain w/o Samp
OFF w/o Samp
8dB Gain w/ Samp
-6dB Gain w/ Samp
-20dB Gain w/ Samp
OFF w/ Samp


UHURA SPKR PSRR, 3.3V SUPPLY, SLOW DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
8dB Gain w/o Samp
-6dB Gain w/o Samp
-20dB Gain w/o Samp
OFF w/o Samp
8dB Gain w/ Samp
-6dB Gain w/ Samp
-20dB Gain w/ Samp
OFF w/ Samp

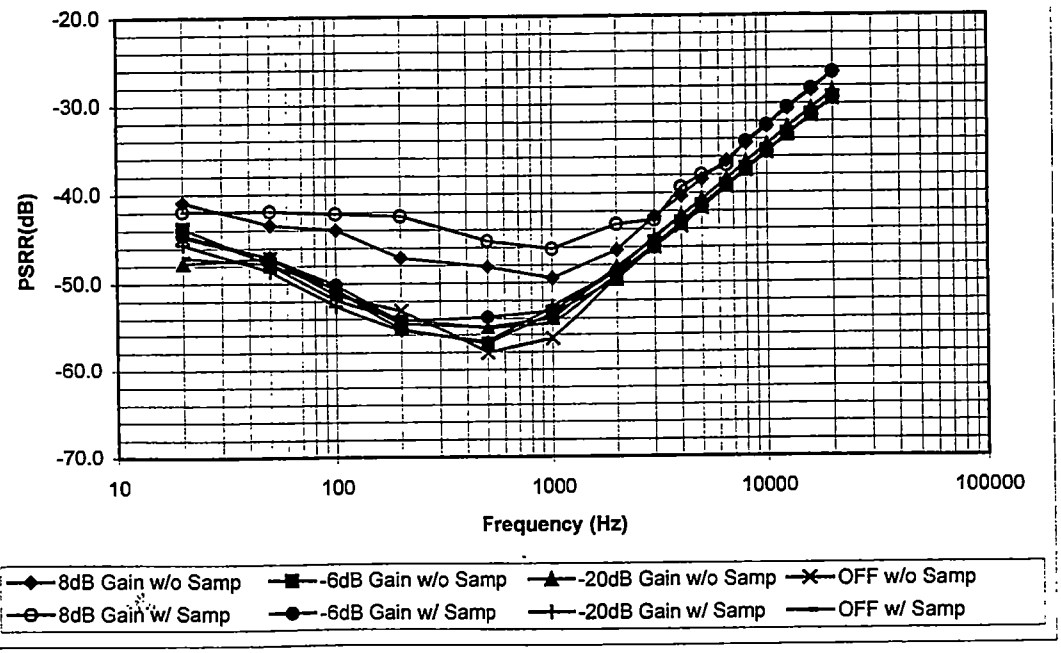

UHURA SPKR PSRR, 2.8V SUPPLY, NOMINAL DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
8dB Gain w/o Samp
-6dB Gain w/o Samp
-20dB Gain w/o Samp
OFF w/o Samp
8dB Gain w/ Samp
-6dB Gain w/ Samp
-20dB Gain w/ Samp
OFF w/ Samp


UHURA SPKR PSRR, 3.3V SUPPLY, NOMINAL DEVICE,
SINGLE ENDED OUTPUT
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
PSRR(dB)
10
100
1000
10000
100000
Frequency (Hz)
8dB Gain w/o Samp
-6dB Gain w/o Samp
-20dB Gain w/o Samp
OFF w/o Samp
8dB Gain w/ Samp
-6dB Gain w/ Samp
-20dB Gain w/ Samp
OFF w/ Samp

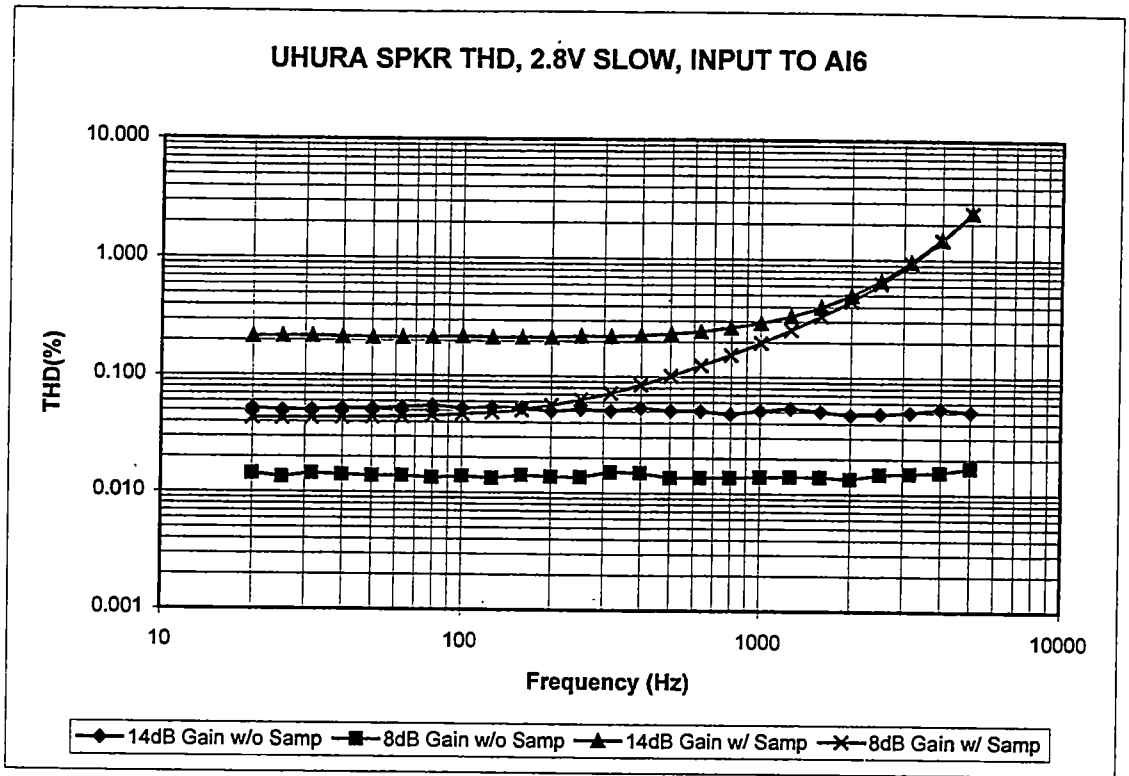
UHURA SPKR PSRR, 3.0V SUPPLY, FAST DEVICE, SINGLE ENDED OUTPUT

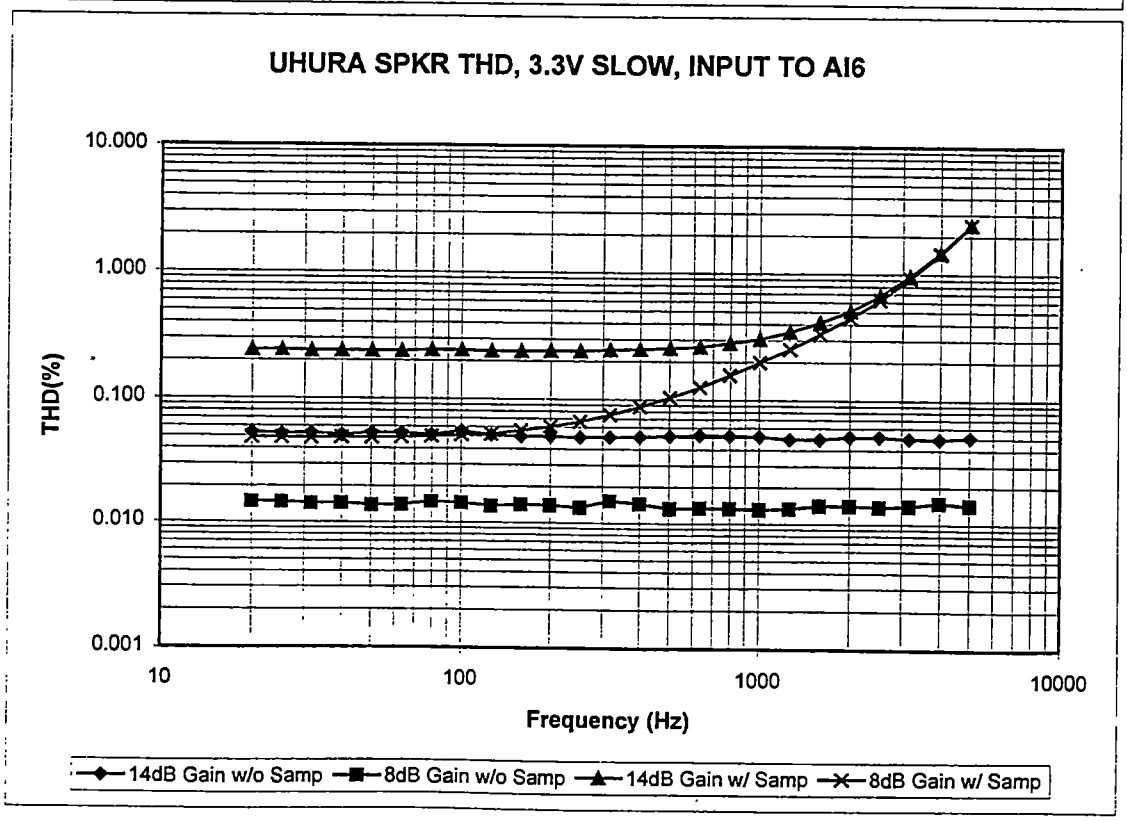


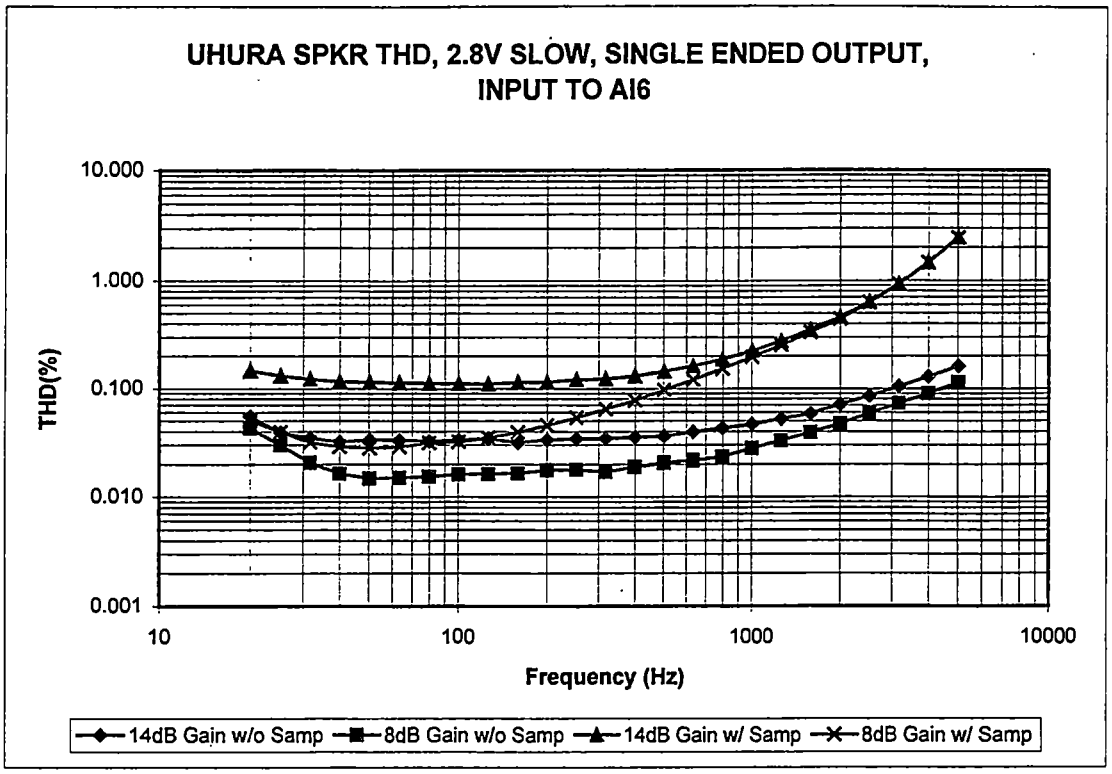
UHURA SPKR PSRR, 3.3V SUPPLY, FAST DEVICE, SINGLE ENDED OUTPUT

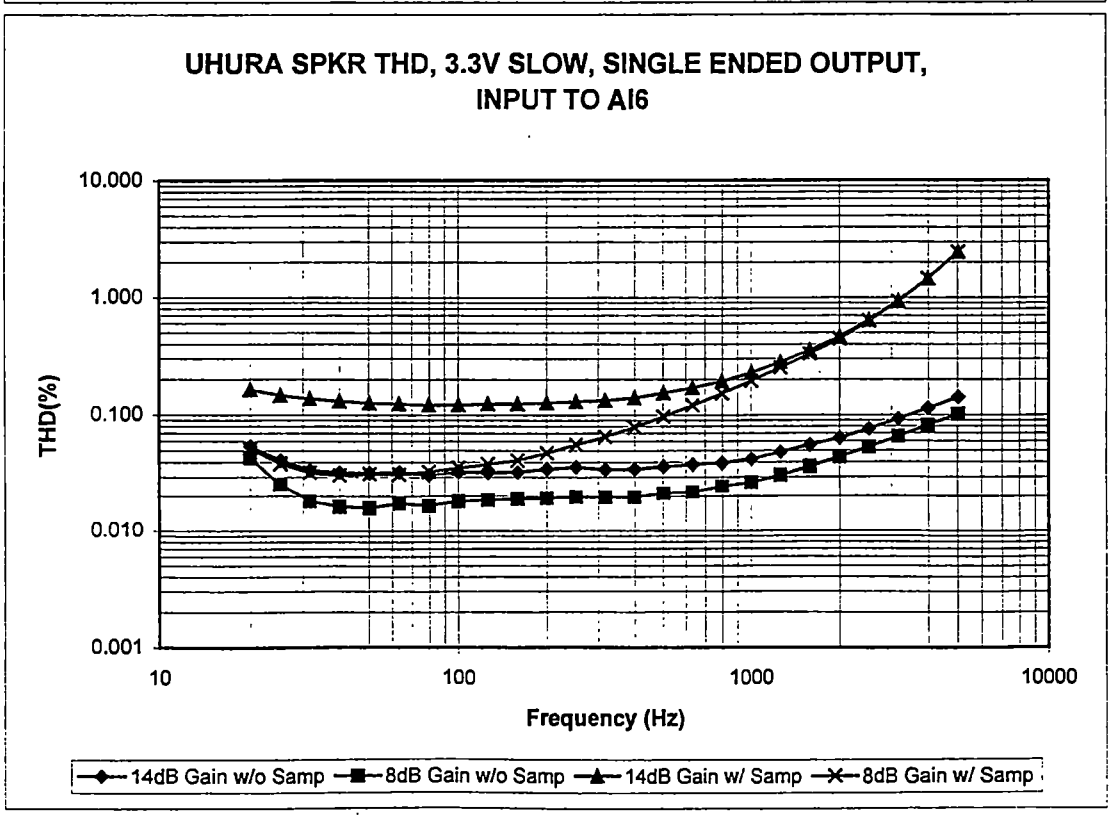


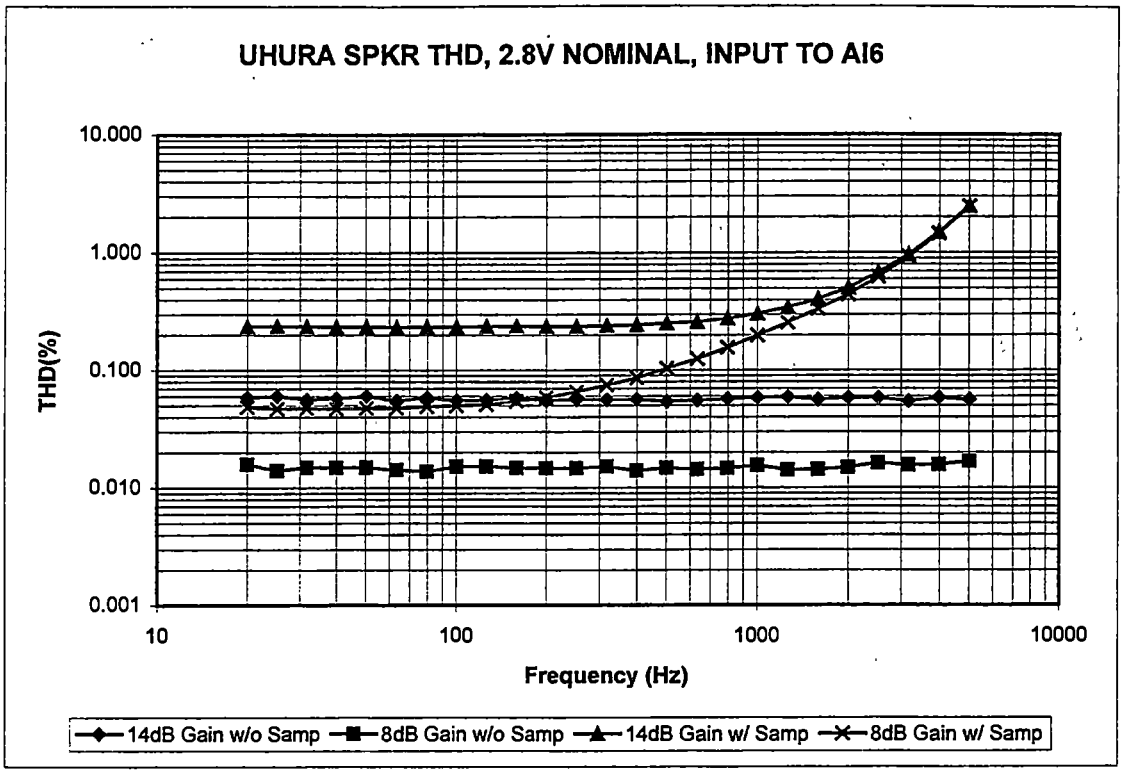
SPEAKER AMPLIFIER THD DATA

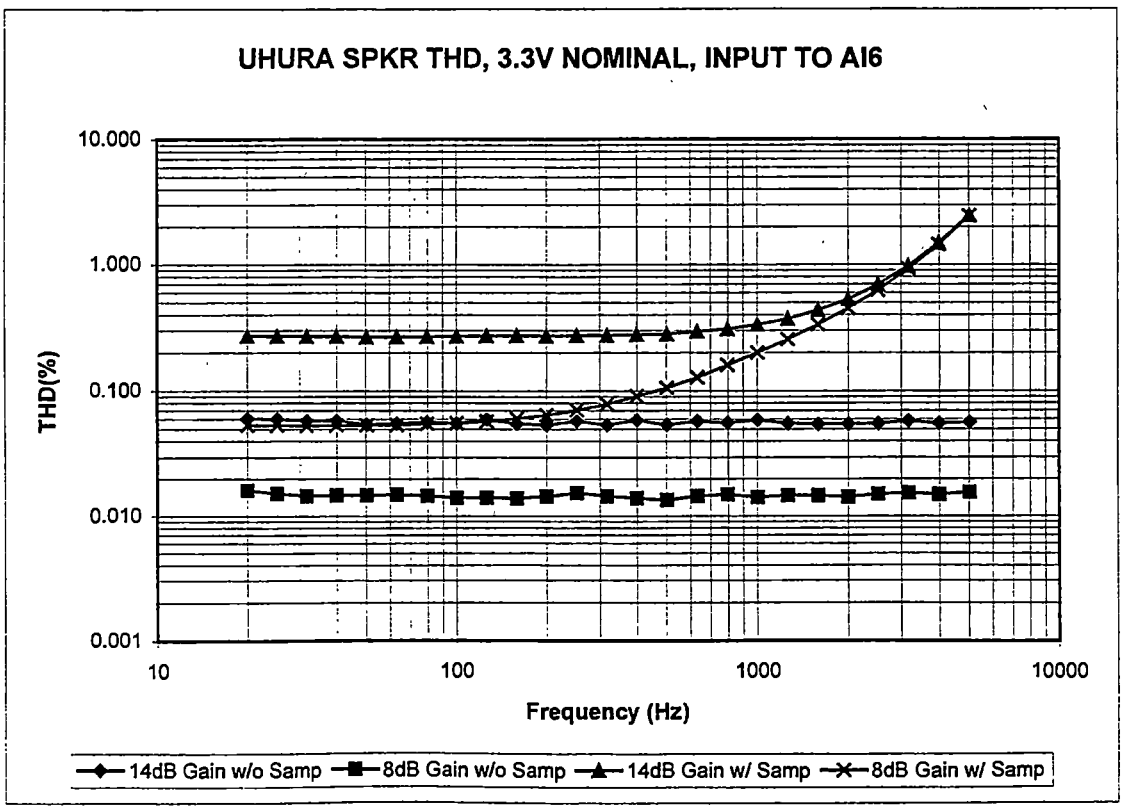

UHURA SPKR THD, 2.8V SLOW, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

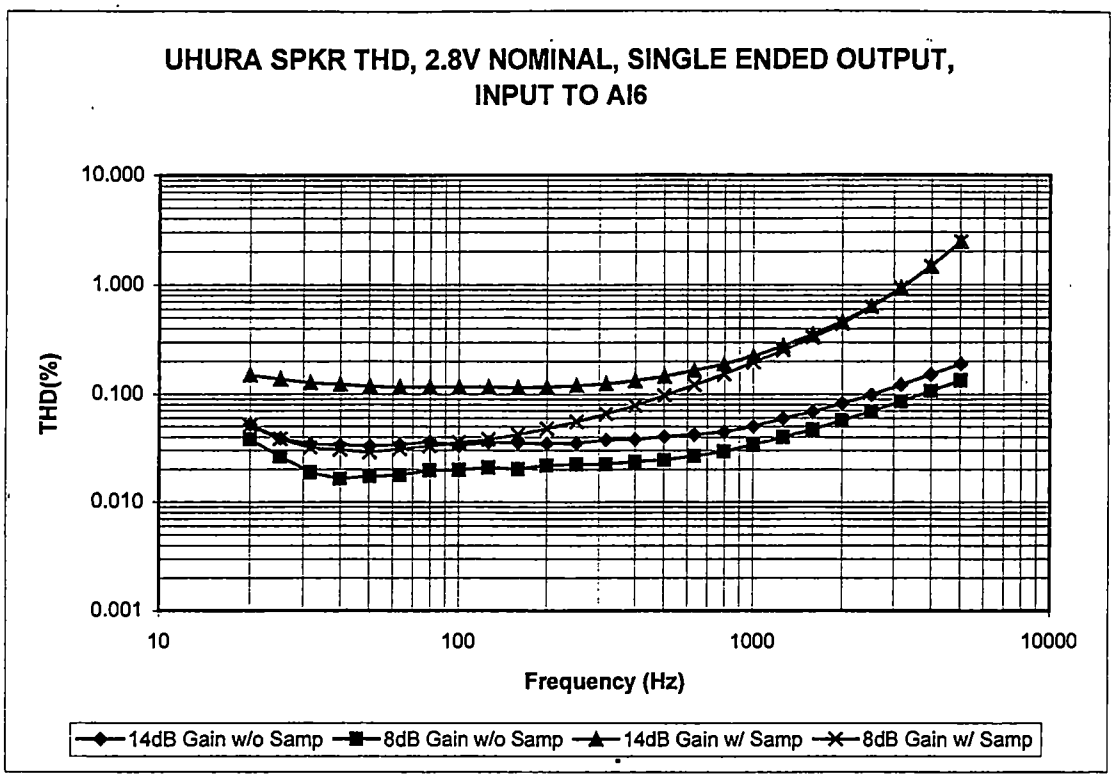

UHURA SPKR THD, 3.3V SLOW, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

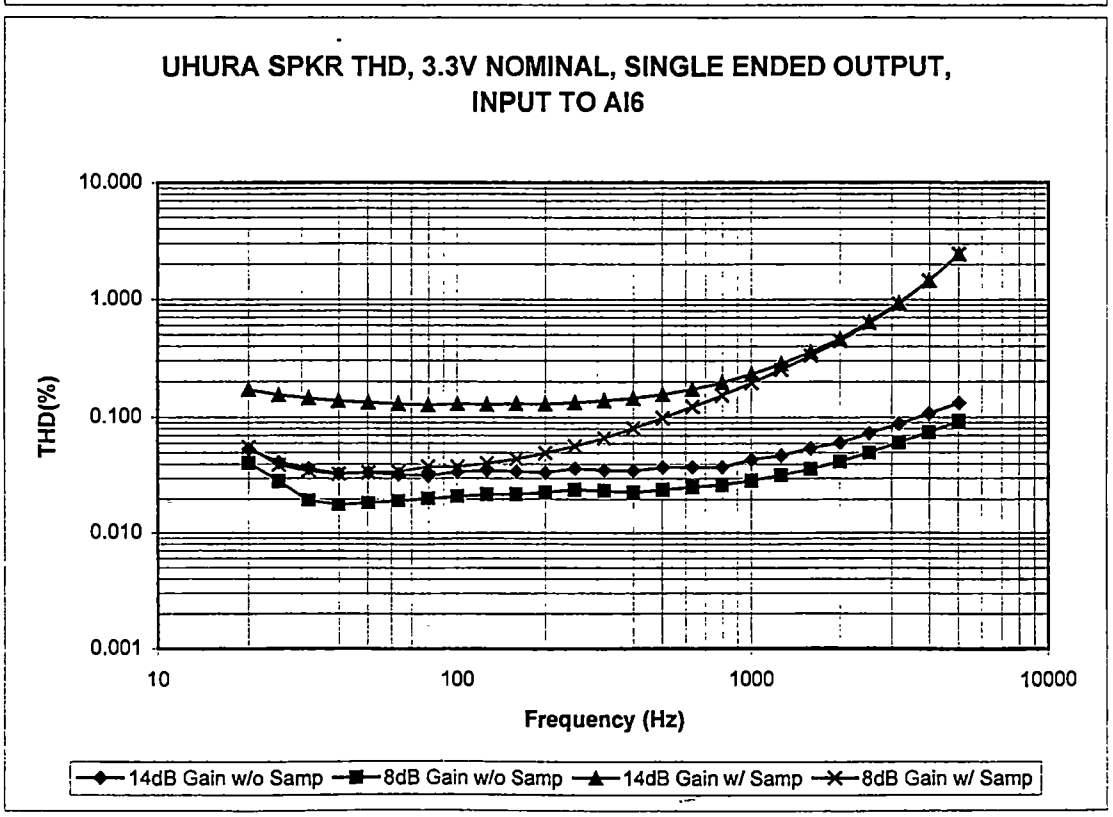

UHURA SPKR THD, 2.8V SLOW, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

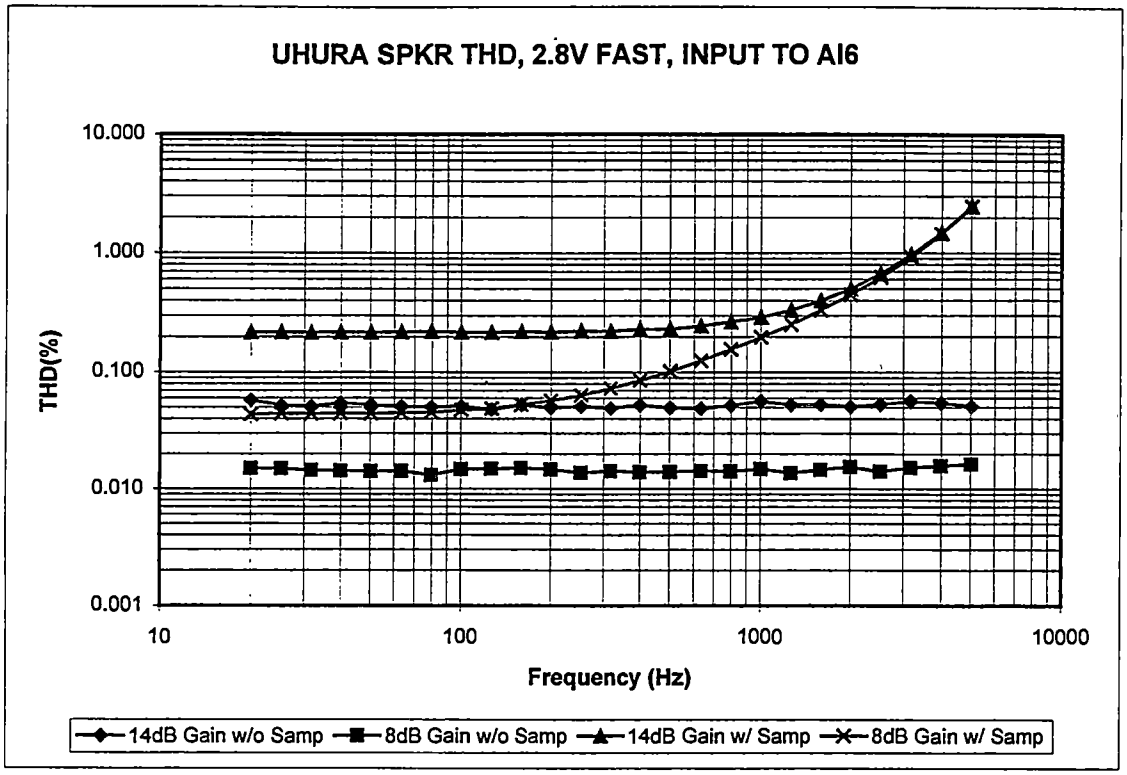

UHURA SPKR THD, 3.3V SLOW, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

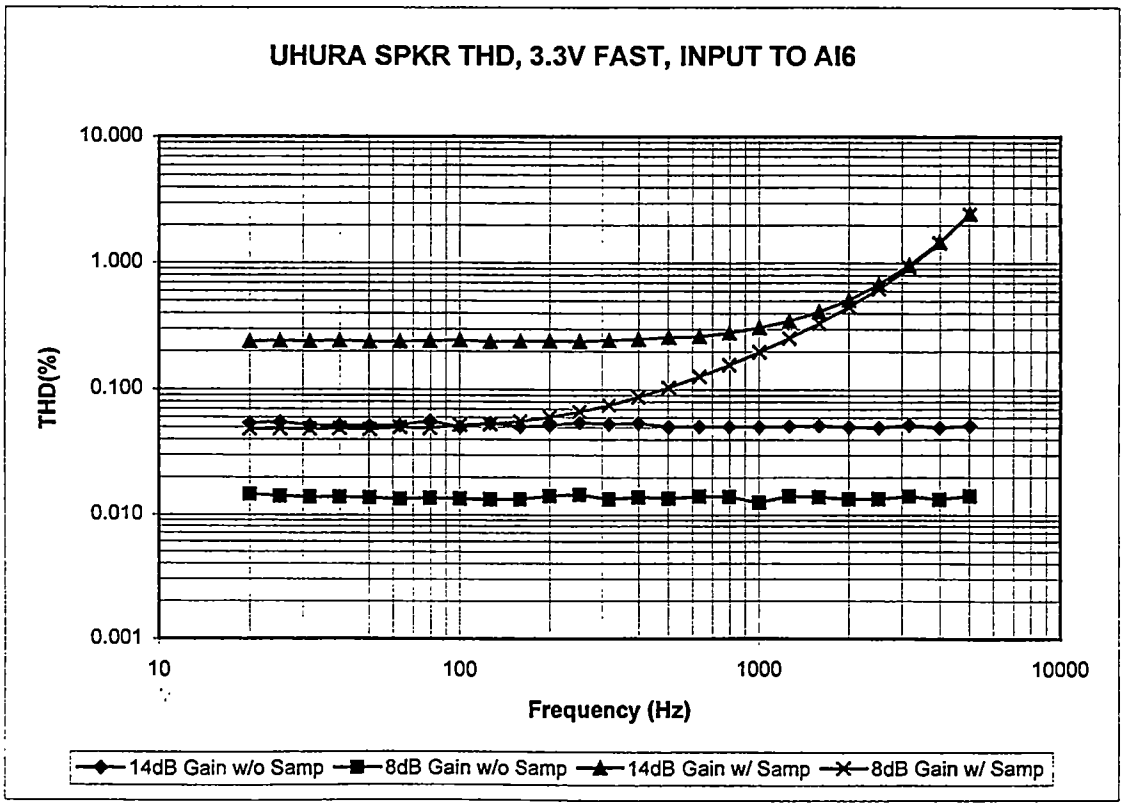

UHURA SPKR THD, 2.8V NOMINAL, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

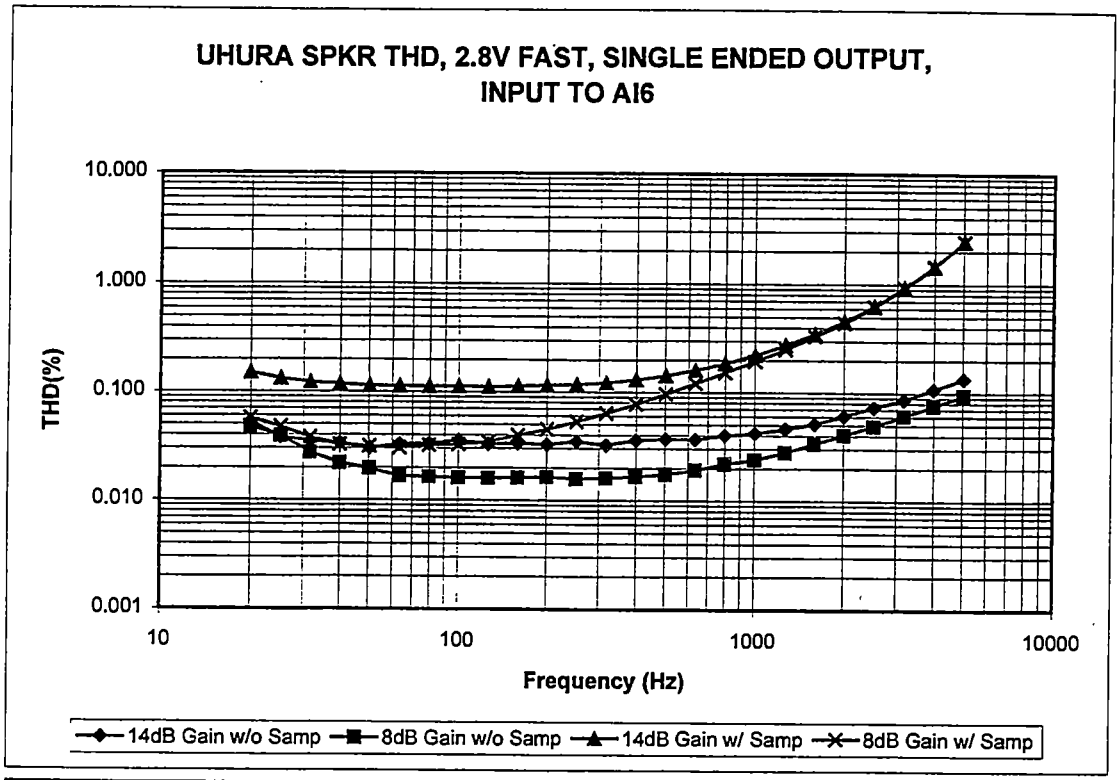

UHURA SPKR THD, 3.3V NOMINAL, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

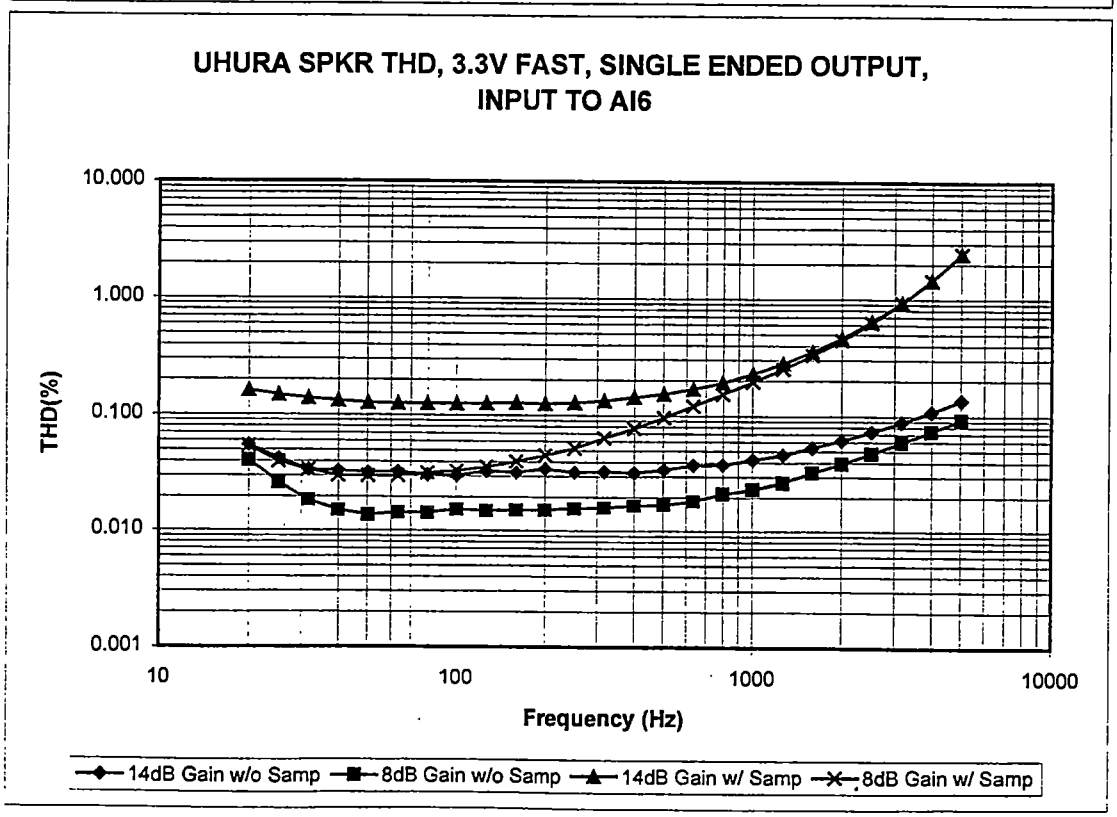

UHURA SPKR THD, 2.8V NOMINAL, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp


UHURA SPKR THD, 3.3V NOMINAL, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp


UHURA SPKR THD, 2.8V FAST, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp


UHURA SPKR THD, 3.3V FAST, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp


UHURA SPKR THD, 2.8V FAST, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp


UHURA SPKR THD, 3.3V FAST, SINGLE ENDED OUTPUT, INPUT TO AI6
10.000
1.000
0.100
0.010
0.001
THD(%)
10
100
1000
10000
Frequency (Hz)
14dB Gain w/o Samp
8dB Gain w/o Samp
14dB Gain w/ Samp
8dB Gain w/ Samp

VITA

Carlyle L. Reynolds was born in Harrison Valley, Pennsylvania on November 20, 1970. He attended Northern Potter High School where he graduated with honors. Upon finishing high school in 1988 he entered the Air Force. He was stationed at Mather AFB in Sacramento, California where he served as an electronics technician. He was responsible for security systems on the base. In addition, his duties included maintaining the ground-to-air communications systems and the radar system used by air traffic control. He was honorably discharged from the Air Force in 1992. At that time, he moved to Knoxville, Tennessee where he worked as a security alarm technician before starting college. In 1993 he enrolled at the University of Tennessee. He graduated with his Bachelors of Science degree with a major in electrical engineering in 1997 and immediately started his graduate work. With the benefit of a graduate teaching assistant position extended to him by the Electrical Engineering department, he was able to obtain his Masters degree in that discipline in December of 1999.