5-1999

Development of a 916 MHz RF transmitter in 0.5-[mu]m [i.e. micrometer] CMOS

Ryan Erik Lind

To the Graduate Council:

I am submitting herewith a thesis written by Ryan Erik Lind entitled "Development of a 916 MHz RF transmitter in 0.5-[mu]m [i.e. micrometer] CMOS." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this thesis and recommend its acceptance:

T. V. Blalock, Charles L. Britton, Jr.

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Development of a 916 MHz RF Transmitter in 0.5-μm CMOS

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Ryan Erik Lind

May 1999

Dedicated to my loving wife and son,

Meredith and Isaiah, who have patiently

supported me in school and in life and to my

Lord and Savior Jesus Christ from whom come

all the blessings in this life and the one to come.

Acknowledgments

I have many people to thank who have aided me in the preparation of this thesis. First and foremost I would like to thank M. Nance Ericson for providing the necessary funding and resources to do this project. Thanks for letting me do the fun stuff Nance. I would also like to thank Mike Emery whose guidance and instruction helped educate me in the method and madness of the RF hardware design world. Dr. Steve Smith and Mike Moore have also increased my understanding of communication systems in addition to providing a good laugh on more than one occasion. Special thanks to Dr. James Rochelle who has showed endless patience helping me refine this thesis from some very rough drafts. I would like to thank Dr. Chuck Britton who has always been glad to help answer any questions I have had. I would like to thank all the friends I have made while getting my graduate degree for their support and good. To Rob Jones, Michael Vann, Shane Frank and Chris Moscone I offer thanks. Best of luck guys. To Dr. Mike Simpson I extend my thanks for starting and maintaining (with a high degree of excellence) the joint program. I must also thank my wife, Meredith, for her patience and selflessness in allowing me to get my masters degree. Thank you for your encouragement, support and confidence in me.

Above all, I thank the Lord God Almighty who has revealed Himself to me by His Holy Spirit, has atoned for my sin through the cross and has robed me in the perfect righteousness of Christ saving me from His wrath. *Sola Scriptura. Sola Gratia. Solo Christo. Sola Fide. Soli Deo Gloria.*

Abstract

This thesis is a study in the design and implementation of a 916 MHz RF transmitter in 0.5-μm CMOS technology. The transmitter is designed to be used in a biologically implantable, physiological measurement system for the mouse population in the Functional Genomics Laboratory at Oak Ridge National Laboratory (ORNL).

The transmitter system is first presented from a high level where issues such as modulation scheme and system architecture are discussed. A detailed analysis then proceeds for each of the transmitter's components. These include a micro-power frequency reference, a phase locked loop (PLL) and an RF mixer. Each transmitter component has a chapter discussing the design, implementation and simulation of the circuit or circuits used to meet the design requirements. Finally, the test results for each of the components is given as well as the performance of the transmitter as a complete system.

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Chapter 1

A 916 MHz RF Transmitter in 0.5-um CMOS

The application of wireless communications to micro-sensor technology has increased significantly as information rates and the number of items being monitored have increased. This is due to the added complexity and inherent cost to systems making use of large amounts of cable for communication purposes. There are also a large number of applications where having a cable link to the measurement system is inappropriate such as biological applications where internal measurements are required or long distance communications where excessively long cables are necessary. For biological monitoring using implanted sensors and systems, wireless technology provides a viable approach for instrument control and data collection with minimal specimen impairment. Wireless communications therefore offer an elegant and practical solution to high density information systems. The focus of this thesis is to design and implement a CMOS compatible wireless transmitter for an implantable biological monitoring system. A CMOS implementation is desirable due to its low cost and high level of integration allowing the transmitter and the required measurement electronics to be comprised of a single ASIC (Application Specific Integrated Circuit). This thesis begins by discussing

the transmitter from the system level and then focuses on the individual circuits of which the system is comprised.

1.1 System Overview

In support of the ongoing genomics research at the Oak Ridge National Laboratory, an automated implantable monitoring system is under development that will measure heart rate, temperature, and activity of mice under study. The research goal is to quickly identify abnormal specimens and determine the gene or genes responsible. With a facility housing approximately 90,000 specimens, automation is key to effective and cost efficient identification of abnormal specimens, which typically exist as only 0.3% of the mouse colony population [1].

In order to allow long term monitoring without inducing physiological effects, the system must be highly miniaturized, wireless, and powered using inductive methods. These requirements necessitate the use of low-power monolithically integrated RF electronics. This thesis focuses on the analysis and design of a CMOS RF transmitter optimized for this challenging application.

The implantable unit consists of four main blocks: the front end electronics which performs the physiological measurements, the system controller, the RF transmitter and the inductive power coupling system. The front end electronics condition and digitize the sensor outputs. The sensors consist of an optical emitter/detector pair for pulse rate measurement, an accelerometer for activity monitoring, and an integrated thermometer for temperature measurement. The system controller is responsible for packeting the

digitized data from the front end sensors and forming a serial data stream which is spread and sent to the RF transmitter. The system controller also coordinates the operation of the front end and RF transmitter. The RF transmitter modulates the data using a 916 MHz carrier and transmits it with the required amount of signal power. This frequency is in the Industrial Scientific and Medical (ISM) Band, designated as a low power spread spectrum band which lends itself to this application. The inductive power coupling system provides power to the entire unit. Power is inductively coupled to avoid the use of a battery which would limit the implant's lifetime. A block diagram of the implantable system is shown in Figure 1.1 [1].

Now that the implantable system has been discussed, attention will be focused on the RF transmitter sub-system which is the subject of this thesis. The remainder of this chapter details the general transmitter requirements for this application and gives a broad overview of the transmitter system.

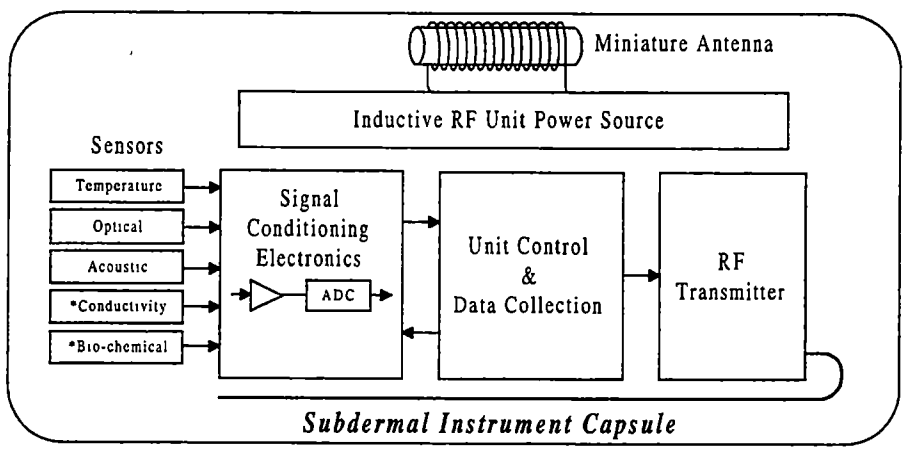


Figure 1.1 - Implantable Monitoring Unit Diagram

1.2 General Implantable Transmitter Requirements

As wireless systems have become increasingly popular so has the need for low-power circuit design. This increased need for power efficiency is especially important for wireless systems used in stand alone applications such as the implantable which is remotely powered using inductive power coupling methods. In this system, low power consumption is necessary due to restrictions in the allowable magnetic field strength in the presence of biological specimens. As a result there is a limited amount of power available to the implantable system which must be shared by all of the system's electronics. Therefore, efforts must be made to optimize the transmitter's electronics for low power operation wherever possible. Initial measurements indicate that the available power is insufficient to continuously power the transmitter system. As a result the transmitter will only be powered when data is ready for transmission which is approximately 10% of the time. Thus the transmitter must have the ability to be enabled when needed and disabled when not transmitting. Figure 1.2 demonstrates the power management scheme implemented.

Non-invasive monitoring of biological specimens implies a high degree of system integration to reduce the size of the implantable. This requires the designer to minimize the use of off-chip components and to maximize efficiency in the use of chip area. The restriction of off-chip components is especially difficult in the RF transmitter as many RF topologies make use of inductors and large capacitors which cannot be successfully implemented using a standard CMOS process. The transmitter system has been implemented using the HP 0.5μm CMOS process due to the high level of system

integration capability, low power and the relatively low cost associated with a standard CMOS process.

1.3 Communication Signal Requirements

The communications signal scheme should provide good transmission power efficiency, robust data spectrum against atmospheric or man made noise and minimal system complexity (reduction of hardware). The data to be transmitted is the digitized results from the front end electronics measurement circuitry. Digital data transmission was chosen due to its inherent robustness with a penalty in transmission bandwidth [2].

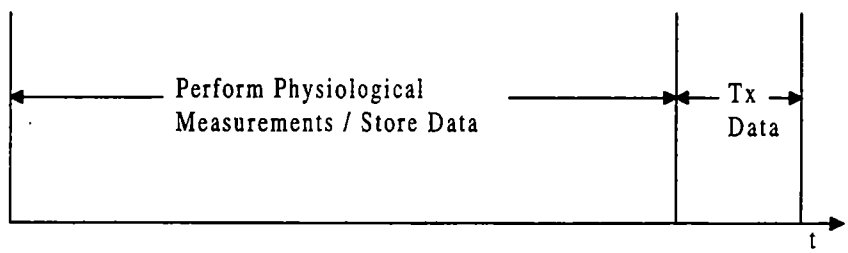


Figure 1.2 - Operational Cycle of Implantable

The carrier frequency is chosen to be 916 MHz because it falls within the ISM band and is realizable using CMOS technology. Another ISM band that is more universally accepted is located at 2.4 GHz however use of CMOS circuits at this frequency is not practical for presently available processes.

Perhaps the best known of all modulation schemes is AM. Amplitude modulation is accomplished by multiplying the message signal directly with the carrier frequency.

AM is the simplest of all modulation schemes but its transmission power efficiency suffers due to wasted power associated with the transmission of an extra sideband and the carrier frequency. These inefficiencies can be avoided using suppressed carrier single sideband AM (SCSSB) which transmits only one sideband of the message signal at the cost of increased system complexity at the receiver [3].

Frequency modulation (FM) is the most popular modulation scheme for analog signals where hi-fidelity is required such as music. This particular modulation method spreads the message out in the frequency domain for transmission. This spreading helps make FM more immune to transmission noise in the frequency domain. Also because the receiver is sensitive to the frequency of the incoming signal and not the amplitude, the demodulated signal will have a much higher fidelity when compared to an AM scheme due to the effects of additive noise on a received signal's amplitude [3].

Sending digital data to an FM system results in another type of modulation called frequency shift keying (FSK) [4]. The transmitter outputs only two frequencies based on the input digital signal. One of the drawbacks to an FSK system is the lack of interference immunity which results from an output spectrum that has the form of an impulse at each of the two transmitted frequencies. Any interference at these frequencies can result in lost data at the receiver.

Binary phase shift keying (BPSK) is one of the most popular methods for modulating digital data because of its simplicity in implementation and good transmission efficiency. In BPSK systems the carrier frequency output is phase shifted 180° each time

the input digital data changes state [4]. Due to the good performance and implementability, BPSK is the chosen method of modulation for this transmitter system.

Now that the method of modulation has been discussed, attention can be given to specifics of the digital communications format selected for this application. The implantable's communications system requires multiple access capabilities in addition to immunity from spectral interference. Both requirements are met using a spread spectrum communications scheme.

Spread spectrum systems are becoming an increasingly popular method of digital data transmission. The objective of a spread spectrum system is to spread the transmitted message out in the frequency domain. This results in a more robust communications link against many types of noise that can commonly degrade system performance. This is especially critical when digital data is being transmitted due to the fact that lost bits can be catastrophic to the received signal message. Spread spectrum transmission schemes also offer advantages in the area of error detection and correction by the receiver [5].

Two common methods of frequency spreading are frequency hopping spread spectrum (FHSS) and direct sequence spread spectrum (DSSS). FHSS systems modulate the digital data with a carrier frequency which is changing at some pre-defined rate [5]. This type of system requires a precise variable frequency oscillator which can be quite complex to implement. DSSS performs the spreading operation digitally before the data gets to the transmitter. One common way of spreading the digital message is to exclusive-or each message bit with an n-ary pseudo-random (PN) bit generator (Figure 1.3). Therefore for each bit of message data there are n number of bits transmitted

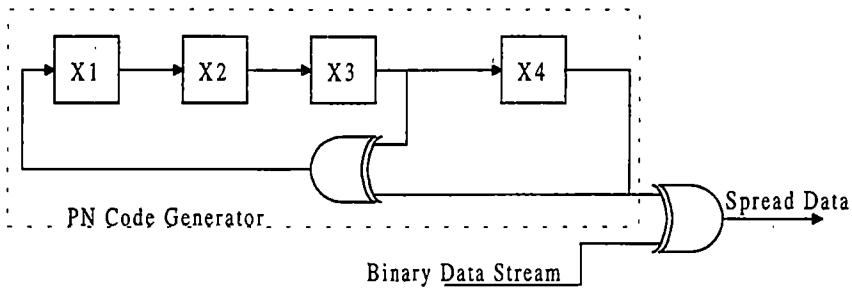


Figure 1.3 - Digital Data Spreading System

depending on the length of the PN code. The larger n is, the more the data is spread [5]. A DSSS system is desirable for this application because the digital spreading can be done easily in CMOS. Multiple access capabilities are also realized by giving each transmitter a different uncorrelated PN code [5]. This allows the receiver to pick one transmitter's output from all the others by looking for the correct PN code [5]. The result of a DSSS system is the spread data spectrum as shown in Figure 1.4 [5]. The baseband signal at the left is spread to result in the wideband signal to the right. The spectral noise spike shows the improved immunity of a spread spectrum system. The main lobe of the baseband signal is almost entirely covered by the spectral noise while the spread message spectrum is only slightly affected by the noise.

This resulting spread data stream is BPSK modulated to the desired carrier frequency to achieve the modulated message signal. The advantages in noise immunity and multiple access capabilities of a spread spectrum system make it ideal for the biological monitoring system [5].

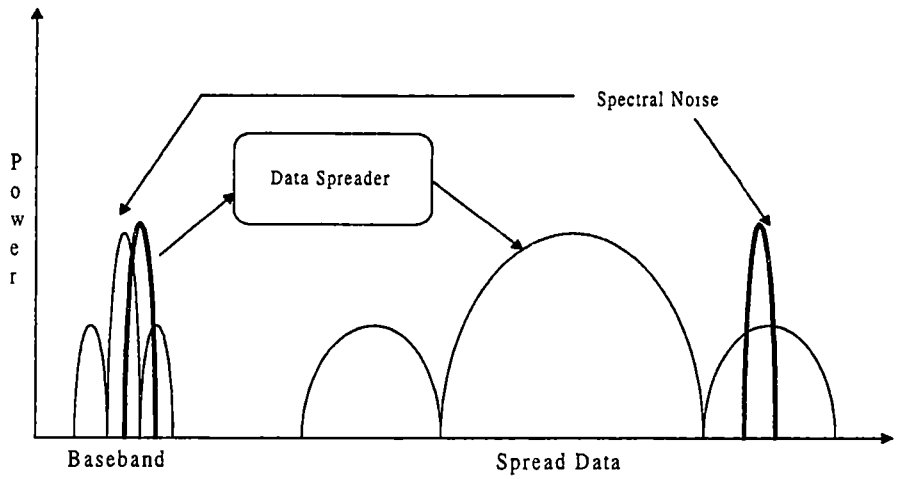


Figure 1.4 - Spectral Diagram of a Spread Spectrum System

1.4 Transmission System Overview

The transmission system used in this application is shown in Figure 1.5. The transmitter system is comprised of four main blocks. A precision frequency reference, phase locked loop, mixer (analog multiplier) and the necessary bias control circuitry. The precision frequency reference is multiplied by the phase locked loop to the 916 MHz carrier frequency (ISM band). The mixer then modulates the spread data with the carrier frequency and the resulting output signal is transmitted via the RF antenna. The bias control circuitry provides the necessary current biasing for all the analog parts of the system as well as the ability to power down the system while not transmitting.

1.4.1 Micro-Power Frequency Reference

The use of a micro-power frequency reference is essential to the transmitter for providing a highly stable frequency reference for the PLL to multiply. If the frequency reference drifts over time the receiver will be unable to maintain lock with the modulated

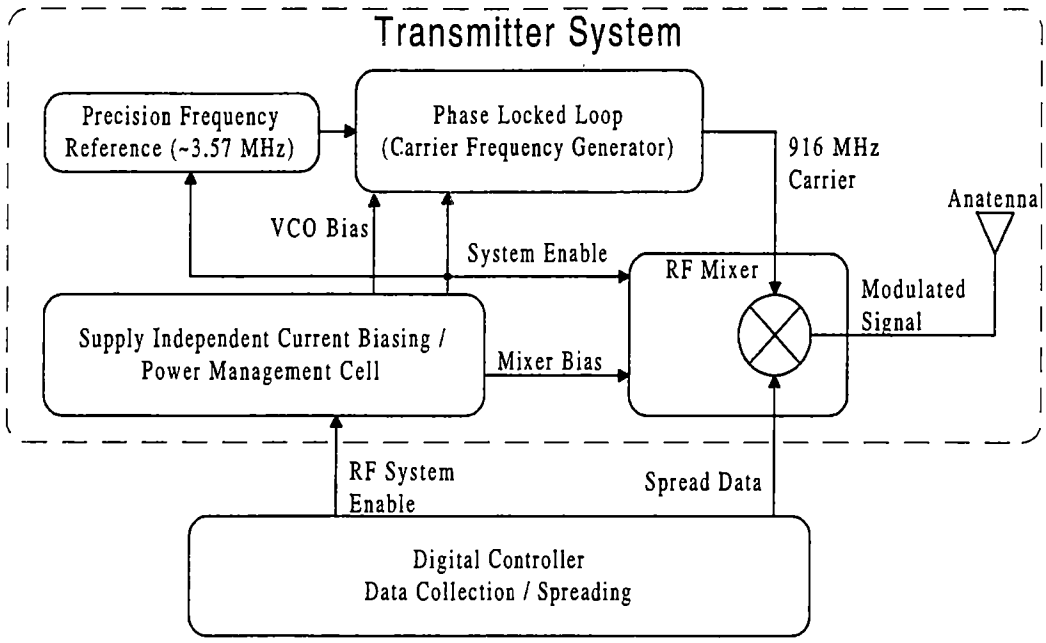


Figure 1.5 - System Block Diagram

message and the communications link will fail. Thus a case could be made that this is the most important building block of the RF transmitter. Chapter 2 contains a detailed analysis of the micro-power frequency reference.

1.4.2 Phase Locked Loop

The PLL is a negative feedback loop that outputs a frequency that is a pre-defined multiple of the frequency reference [6]. A basic block diagram of the PLL is shown in Figure 1.6. The circuit operates by dividing the output frequency by a multiplication factor and then comparing this signal to that of the frequency reference using the phase frequency detector. The phase frequency detector output is then filtered to produce an error signal that in turn adjusts the output frequency of the phase locked loop. The output should therefore be as stable as the reference to which it is compared.

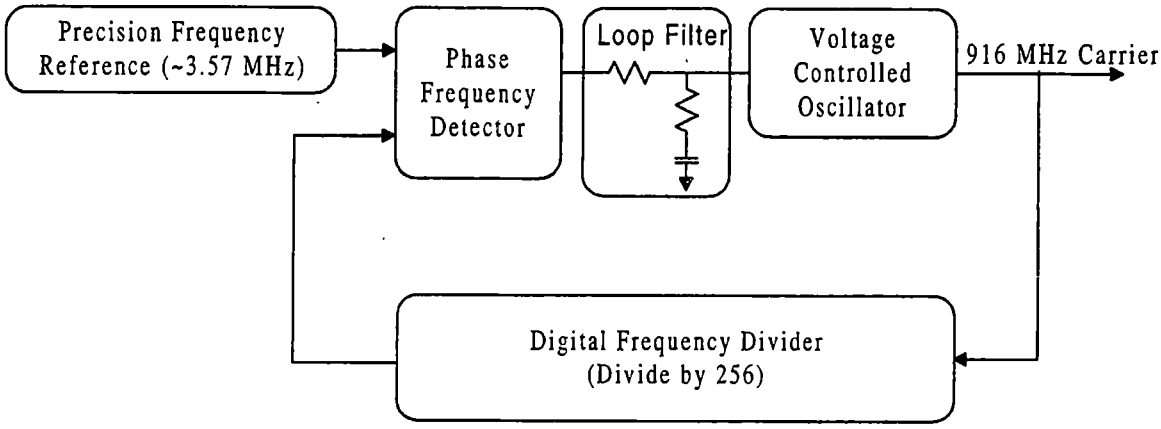


Figure 1.6 - Phase Locked Loop Block Diagram

Chapter 3 contains a detailed analysis of the PLL as a system as well as the circuits of which it is comprised.

1.4.3 Mixer

The function of the mixer is to modulate the message signal to the desired carrier frequency. This is accomplished by multiplying the message by the carrier frequency. When transmitting a digital signal, the modulated waveform appears as the carrier frequency signal which is phase shifted by 180 degrees each time the message signal changes state. This method of modulation is binary phase shift keying (BPSK) and is discussed in Section 1.3. Chapter 4 discusses the design and implementation of a CMOS mixer.

1.4.4 Bias Control

The bias control circuitry primarily provides the necessary dc bias for all the analog circuitry and also permits the powering down of the RF system while not in use.

The latter is necessary to reduce the average operating power of the implantable unit. Providing a consistent bias point for the system is further complicated by the inability of the inductive power to supply enough instantaneous power for the RF electronics while enabled [1]. Therefore the voltage across the power supply capacitor will droop during the transmitting portion of operation. This necessitates a biasing scheme that is relatively independent of supply voltage fluctuations. Figure 1.7 shows the expected supply voltage during the operation of the transmitter. The latter half of Chapter 4 discusses several potential design solutions to achieve supply independent current biasing.

1.5 Thesis Organization

Chapters two through four discuss in detail the individual circuits which comprise the RF transmitter system. Chapter five details the test results of each individual cell and the transmitter as a system. Chapter six discusses areas for improvement and future work

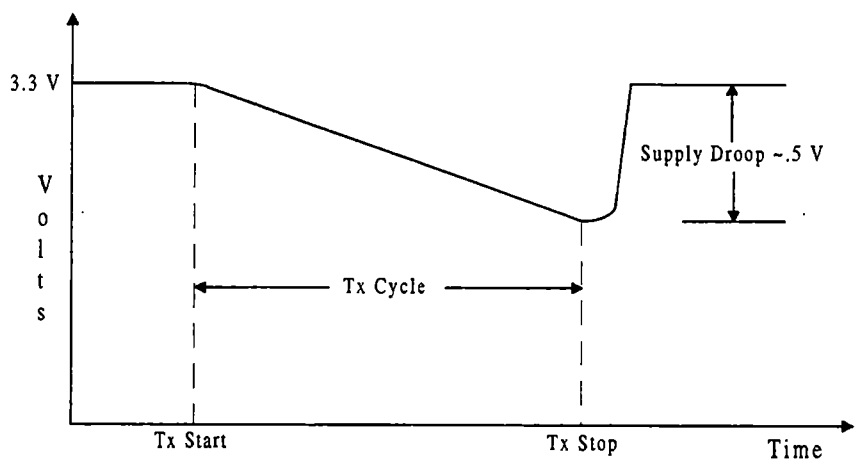


Figure 1.7 - Supply Voltage Fluctuations

related to the project. Appendix 1 contains process parameters for three individual runs of the HP 0.5-μm process in addition to the models used by the simulator. All circuit simulation files are contained in Appendix 2. All simulations are performed using HSPICE simulation software and MetaWaves waveform display viewer [7].

1.6 Related Work

Biologically implantable systems are moving to the forefront of bio-engineering technology. Two companies in particular, DSI (Data Sciences Incorporated) and Mini-Mitter, are producing implantable units which monitor physiological parameters in animals. These manufactured implantables are designed to be implanted into the animals peritoneal cavity whereas the mouse project implantable is designed to be sub-dermal and thus less intrusive. The DSI and Mini-Mitter implantables also use AM for their communications scheme as opposed to spread spectrum techniques.

Although work has been done in the area of implantables, there is much room for improvement. This project seeks to take implantables to a higher level of integration to reduce physical size and also to take advantage of superior communications schemes to achieve a more robust communications link.

Chapter 2

Precision Low Power Frequency Reference

A precision frequency reference is an important building block of any communications system. While their role in clocking the digital circuitry is apparent, the stability with which they drive the PLL is paramount. Any drift in reference frequency will be multiplied by the PLL's closed loop gain at the output which will degrade the receivers ability to lock on the transmitted data signal. The necessity for stability coupled with the ever present demand for low power and a high level of integration points to a CMOS implementation of a crystal oscillator. This application requires a 3.5796 MHz oscillator to achieve a PLL output frequency of 916 MHz.

2.1 Background

Oscillator topologies in use today can generally be placed into one of two categories. The first category is the classic RLC tank circuit with positive feedback. The Colpitts oscillator shown in Figure 2.1 is a classic example of this variety of oscillator [8]. Two drawbacks of this type of oscillator are the number of required external components and the fluctuation in frequency caused by component drift with temperature.

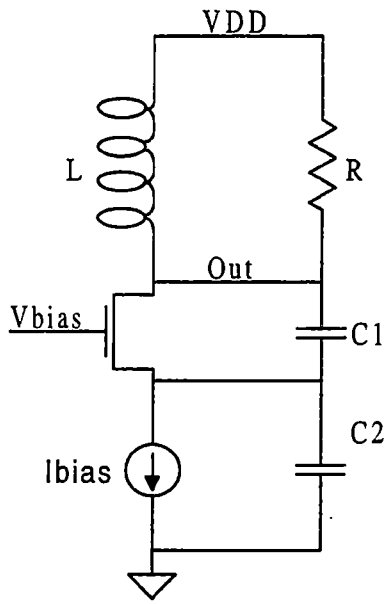


Figure 2.1 - Colpitts Oscillator

The second major category of oscillators incorporates a logic inverter with some type of tuned feedback network. This is a widely used topology because it is easy to implement monolithically with a minimum of required external components. An example which uses a simple RC feedback network is shown in Figure 2.2 [9]. In this example the frequency of oscillation is controlled by adjusting the resistor and capacitor. The advantages of this type of network are its relatively compact topology, its ease of implementation using a standard CMOS process and its ability to operate at low current levels if the capacitor is small. The most notable disadvantage of this particular design is the precision of the passive elements as well as process variations which all contribute to changes in frequency stability and repeatability from circuit to circuit. Conceivably if only a few are needed, each can be calibrated and trimmed to give the correct frequency output at a specified temperature.

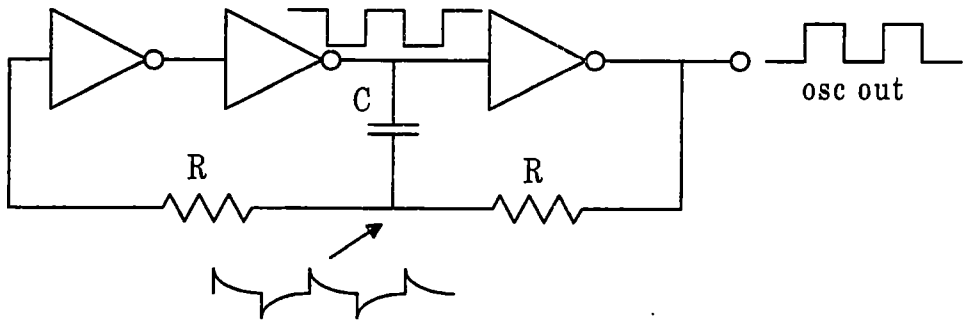


Figure 2.2 - Gated RC Oscillator

This, however, does not solve the problem of frequency drift resulting from the temperature variations of the resistors and capacitor. Therefore, this implementation is unsuitable because any drift in frequency by the reference results in large frequency shifts at the PLL output.

The problems associated with the previous circuit are greatly diminished through the use of a quartz crystal in the feedback path instead of resistors and capacitors. A quartz crystal provides a highly stable tuned network. The use of a quartz crystal is desirable whenever precision (+/- 50 PPM typical tolerance) and temperature stability (+/- 50 PPM, -10° C < T < 70° C) are required. The electrical model for a quartz crystal is shown in Figure 2.3 [8]. Cs and Ls represent the mechanical storage elements, Co models the capacitance associated with the packaging and leads and Rs models the losses inherent to the crystal. The values shown are for an ECS Inc. crystal whose resonant frequency is the required 3.5796 MHz [10].

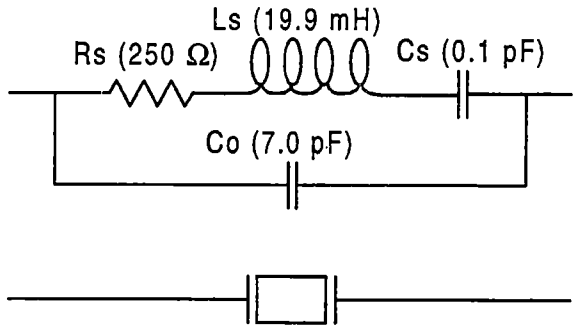


Figure 2.3 - Quartz Crystal Electrical Model

A frequency reference circuit which implements a crystal in the feedback path is shown in Figure 2.4 [11]. The feedback resistor 'Rf' is required to set DC bias voltages and the capacitors 'Cg' and 'Cd' assure that the conditions for resonance are satisfied. This particular implementation has many advantages over the previously discussed designs. These are a high degree of frequency stability, low number of external components, efficient use of silicon, and low power dissipation. This oscillator therefore meets all the necessary requirements for the mouse biological monitoring system.

The actual circuit used is shown in Figure 2.5. The inverter has been replaced by a NAND gate to provide the ability to disable the oscillator when it is not needed. The output has an inverter to provide shaping of the signal as well as good drive capability. Now that the oscillator's topology has been determined, the designer must perform an analysis on the oscillator system to ensure sufficient conditions for the buildup of oscillations. Another critical performance parameter for this system is to develop an expression for the oscillator's operating power. Once both of these analyses have been

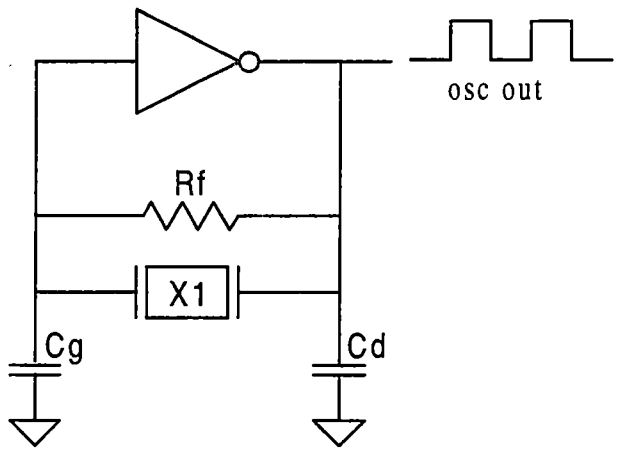


Figure 2.4 - Gated Crystal Oscillator

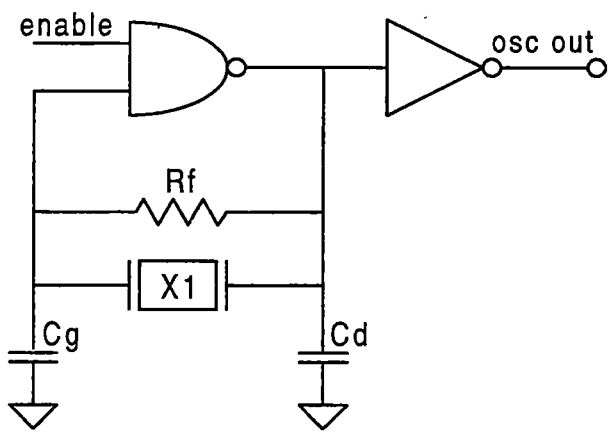


Figure 2.5 - Micro-Power Frequency Reference

performed, the designer can choose appropriate component values and device sizes for the NAND gate and inverter shown in Figure 2.5.

2.2 Required Conditions for Oscillation

In order to determine the necessary conditions for oscillation, the circuit is represented as a negative impedance loop (Figure 2.6) [11]. 'Zc' represents the impedance of the crystal and 'Za', the amplifier impedance, represents the impedance of the NAND gate, 'Cg', and 'Cd' of Figure 2.5. The necessary conditions for oscillation are given by the following [11]:

$$Za + Zc = 0\,, \qquad Eq.\ 2.1$$

$$\mathrm{Re}(Za + Zc) \leq 0 \ and \qquad Eq.\ 2.2$$

$$\mathrm{Im}(Za + Zc) = 0\,. \qquad Eq.\ 2.3$$

In simple terms, this states that the real part of the cumulative impedance of the crystal and the amplifier must be equal to or less than zero, and the imaginary portion of the impedance must sum to zero at the desired frequency of oscillation.

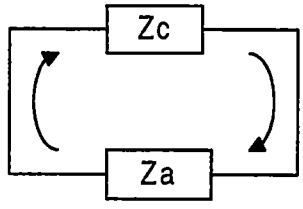


Figure 2.6 - Negative Impedance Loop

In order to proceed with the negative impedance analysis, one must first determine the complex impedance of the crystal and amplifier respectively. The impedance of the crystal using the equivalent circuit in Figure 2.3 is found to be

$$Zc = \left[\frac{1}{Rs + j(\omega \cdot Ls - \frac{1}{\omega \cdot Cs})} + j(\omega \cdot Co) \right]^{-1} . \qquad Eq.\ 2.4$$

At resonant frequency the real impedance of the crystal is approximately 'Rs' (Figure 2.3) and the imaginary component is zero. Determining the impedance of the amplifier (amplifier refers to the NAND gate, 'Cg', and 'Cd') requires a transistor level diagram of a NAND gate shown in Figure 2.7.

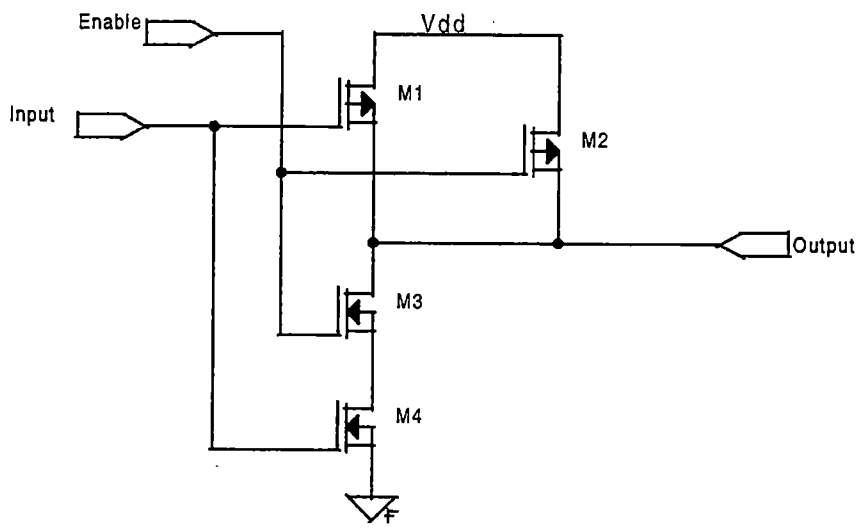


Figure 2.7 - CMOS NAND Gate

The 'Enable' input is tied to 'Vdd' for this analysis and as a result the channel resistance of 'M3' is considered to be very small and the channel resistance of 'M2' is assumed to be very large. The impedance of the amplifier is found using a simplified equivalent circuit for the amplifier as shown in Figure 2.8 [12]. This equivalent circuit assumes the channel impedance of 'M1' and 'M4' to be large compared to the impedance of 'Cd' at the frequency of operation and parasitic capacitance's are assumed to be small compared to 'Cg' and 'Cd'. In Figure 2.8 'gm' represents the combined transconductance of 'M1' and 'M4'. By applying a test voltage Vx and monitoring the return current Ix, the impedance is the ratio of Vx to Ix as shown below (C = Cg = Cd):

$$-\frac{Ix}{s \cdot Cg} gm + s \cdot (-\frac{Ix}{s \cdot Cg} + Vx) \cdot Cd = Ix , \qquad Eq. \quad 2.5$$

$$Za = \frac{Vx}{Ix} = \frac{gm}{s^2 \cdot Cg \cdot Cd} + \frac{1}{s \cdot Cg} + \frac{1}{s \cdot Cd} , \qquad Eq. 2.6$$

and

$$Za = -\frac{gm}{\omega^2 \cdot C^2} - j(\frac{2}{\omega \cdot C}) . \qquad Eq. 2.7$$

The first term in equation 2.7 is the real part of the amplifier impedance and the second term is the imaginary part of the amplifier impedance. Thus the amplifier exhibits a negative real impedance which is required because the real part of the crystal impedance at resonance is positive and approximately equal to 'Rs' [11].

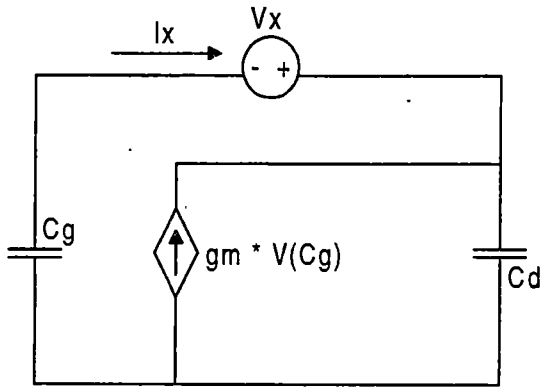


Figure 2.8 - Simplified Amplifier Circuit

From the condition required by equation 2.2, one can derive an expression for the necessary transconductance of the amplifier in order to ensure oscillations (Equations 2.9 and 2.10) [11]. To ensure robust oscillations, the value of transconductance is usually from five to ten times this value calculated using Equation 2.9:

$$\frac{gm}{\omega^2 \cdot C^2} \geq Rs, \qquad Eq.\ 2.8$$

$$gm \geq \omega^2 \cdot C^2 \cdot Rs \approx 41 \frac{\mu A}{Volt} \quad (C = 18\ pF). \qquad Eq.\ 2.9$$

Now that an expression for the minimum required transconductance has been derived, the transconductance of the amplifier circuit must be quantified. The total transconductance is found by constructing a small signal equivalent circuit of the NAND

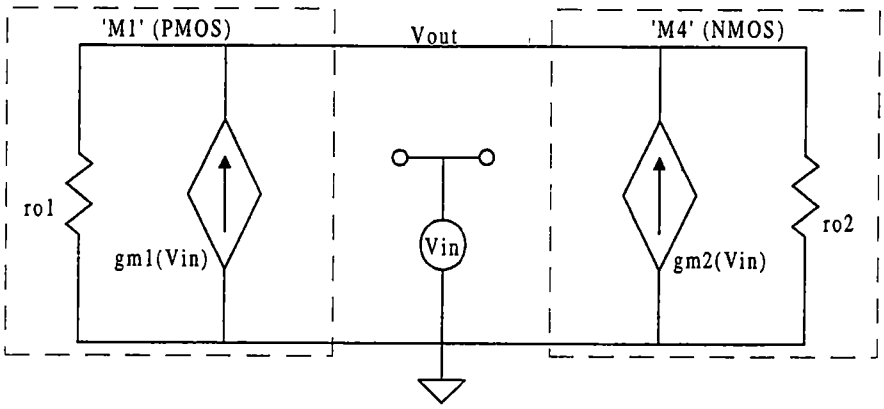


Figure 2.9 - NAND Gate Small Signal Equivalent Circuit

gate shown in Figure 2.7. Figure 2.9 is the small signal equivalent circuit assuming 'Enable' is tied to 'Vdd' and thus neglects the effects of 'M2' and 'M3'. The small signal equivalent circuit shows that the total transconductance of the NAND gate is the sum of the transconductance of 'M1' and 'M4' [13]. Using the saturation region model the transconductance of 'M1' and 'M4' can be expressed as (neglecting channel length modulation effects) [14]

$$gm_{1,4} = \sqrt{2 \cdot K_{P,N} \cdot \left(\frac{W}{L}\right)_{1,4} \cdot I_D} \,. \qquad Eq.\ 2.10$$

The total tranconductance is expressed as

$$gm_{Total} = \sqrt{2 \cdot K_P \cdot \left(\frac{W}{L}\right)_1 \cdot I_{D1}} + \sqrt{2 \cdot K_N \cdot \left(\frac{W}{L}\right)_4 \cdot I_{D4}} \,. \qquad Eq.\ 2.11$$

In order to solve for the total transconductance, the width and length of each device in addition to the drain current must be known. The width and length of the devices should be chosen to achieve the necessary transconductance and minimize the required chip area. The drain current in both transistors can be solved for iteratively using the saturation region model for drain current in a MOS device (neglecting channel length modulation) [13] to yield

$$I_{D1} = \frac{K_P}{2} \cdot \left(\frac{W}{L}\right)_1 \cdot \left(V_{DD} - V_{IN} - |V_{TP}|\right)^2 , \qquad Eq.\ 2.12$$

and

$$I_{D4} = \frac{K_N}{2} \cdot \left(\frac{W}{L}\right)_4 \cdot \left(V_{IN} - V_{SS} - V_{TN}\right)^2 . \qquad Eq.\ 2.13$$

V_{IN} is the input gate voltage of 'M1' and 'M4'. V_{TP} and V_{TN} are the threshold voltages of the PMOS and NMOS devices respectively. By iteratively adjusting V_{IN} until I_{D1} and I_{D4} are equal the designer is able to calculate the drain current in the devices. For a width to length ratio of 7.0 for 'M1' and 2.5 for 'M2" and using the process parameters given in Appendix 1, the drain current is found to be 67 μA and the resulting total transconductance is 322 μA per volt (equation 2.11). This is 7.8 times the minimum required transconductance found using equation 2.9 which will allow for robust operation. The final oscillator circuit is shown in Figure 2.10.

Now that all the necessary circuit parameters have been given, the required conditions for oscillation shown in equations 2.1 - 2.3 can be verified. Figure 2.11 and 2.12 are plots of the total real and imaginary impedance of the oscillator.

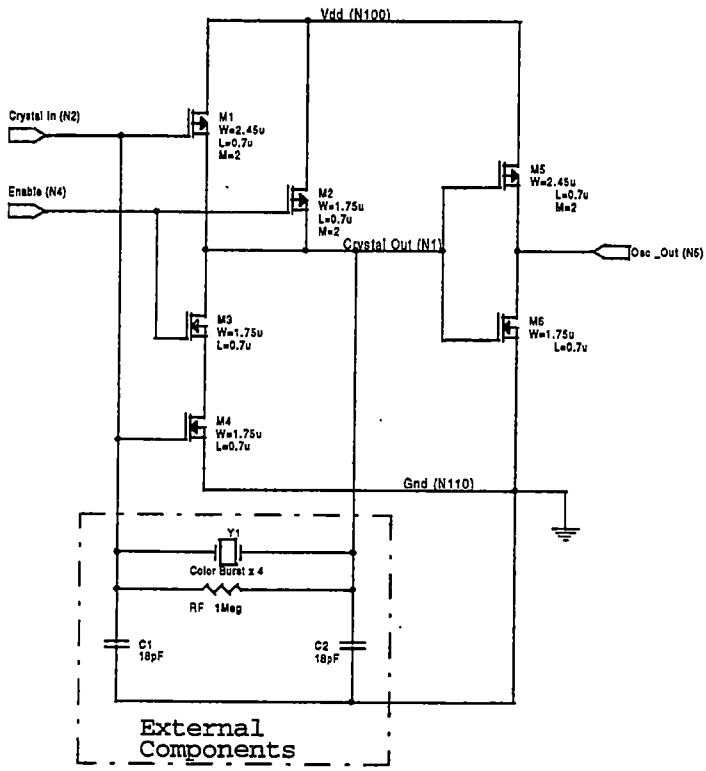


Figure 2.10 - Local Oscillator Schematic

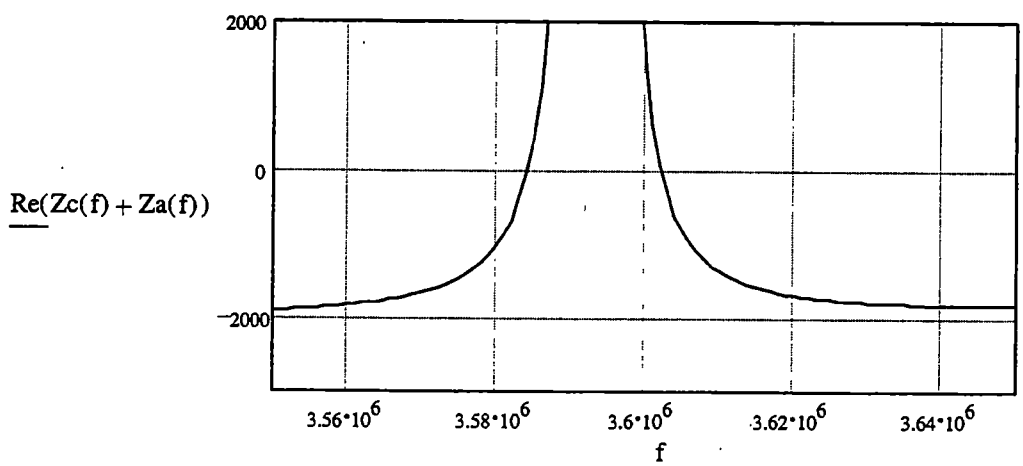


Figure 2.11 - Total Real Impedance of the Oscillator

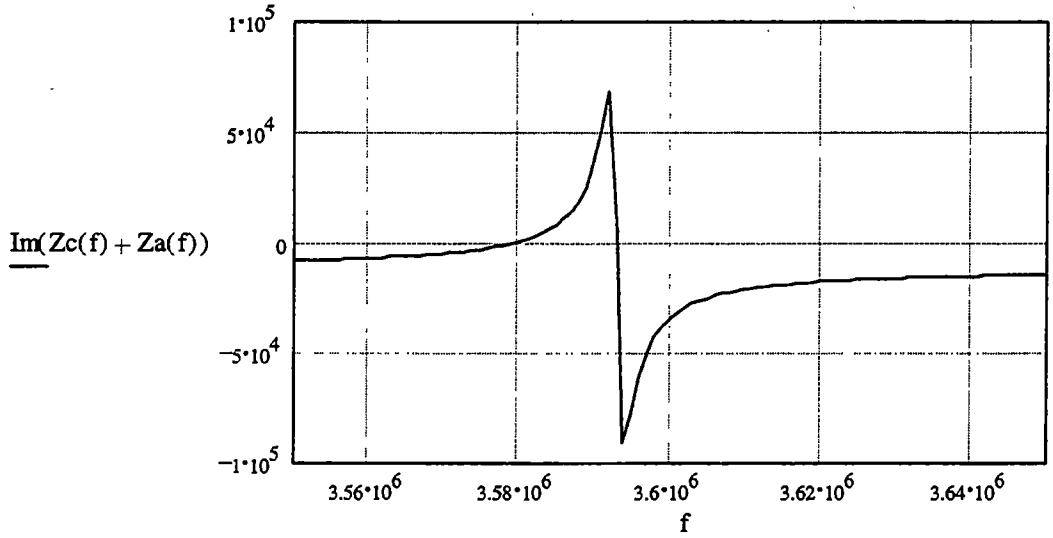


Figure 2.12 - Total Imaginary Impedance of the Oscillator

These figures show that the real component of the oscillator's impedance is less than zero at the first frequency where the total imaginary impedance is equal to zero. Thus the conditions set by equations 2.2 and 2.3 have been satisfied. The location of the first zero imaginary impedance point is the frequency of oscillation and is approximately 3.579 MHz which is the desired reference frequency. This indicates that the oscillator circuit shown in Figure 2.10 meets the necessary criterion to guarantee the buildup of oscillations.

2.3 Estimated Power Consumption

Developing an exact expression for power consumption for this type of circuit is not a trivial task due to its non-linear switching operation. To simplify the analysis an assumption is made that the majority of the power is consumed in the charging and

discharging of the capacitor 'Cd' which is located at the output of the NAND gate ('Cg' is assumed to have minimal effect because it is buffered through the crystal which exhibits an inductive reactance at the frequency of oscillation). This assumption also neglects the finite switching time of transistors 'M1' and 'M2'. Stray capacitance at the output of the buffer inverter is neglected in the analysis because it is much smaller than 'Cd'. Considering only the effects of 'Cd' the circuit model for determining the average power consumption is shown in Figure 2.13. The 'R' represents the finite channel resistance of the 'M4' (see Figure 2.10) when the NAND gate input is low. The expression for current from the power supply when the switch is closed has the form [15]

$$i(t) = \left(\frac{Vdd}{R}\right) \cdot e^{-\frac{t}{RCg}} . \qquad Eq.\ 2.14$$

The total energy supplied by the battery is defined as

$$e = \int_0^\infty Vdd \cdot i(t)\, dt = Vdd^2 \cdot C . \qquad Eq.\ 2.15$$

The average power consumed by the circuit is the total energy divided by the period of the oscillations and is expressed by (for rail to rail switching)

$$P_{AVG} = Cg \cdot Vdd^2 \cdot f . \qquad Eq.\ 2.16$$

For a 'Cg' of 18 pF the estimated average power consumption is approximately 700 μW or 212 μA average current. This is acceptable for this application. The operating power can be reduced by lowering 'Cg'; however, this also has an effect on the output frequency

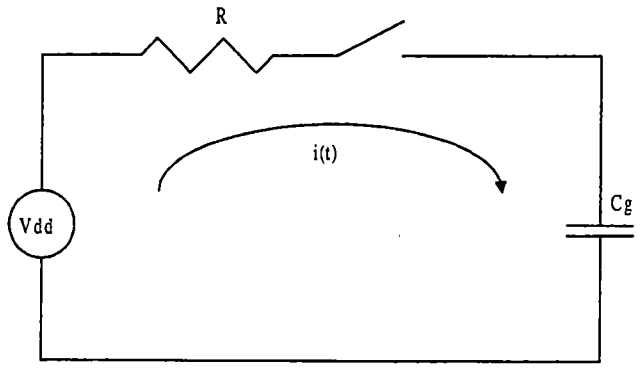


Figure 2.13 - Average Power Dissipation Circuit Model

of the oscillator due to a change in the imaginary impedance component of the amplifier (see Equation 2.7). Now that the appropriate device sizing and component values are known, the circuit shown in Figure 2.10 can be simulated to verify functionality and a reasonable operating power.

2.4 Oscillator Simulation Results

The circuit was laid out in the HP 0.5μm process and extracted to a circuit simulation file. The crystal model used in the simulations is shown in Figure 2.3. All circuit simulation list files are in Appendix 2.

Oscillator simulations were performed with the enable signal set low initially and switched high after 10 μsec and run long enough for the oscillations to reach steady state (~600 μsec). The results of the simulation indicate that the oscillator meets the requisite conditions to ensure the buildup of oscillations. Figure 2.14 shows the output of the buffer inverter for the full length of the simulation.

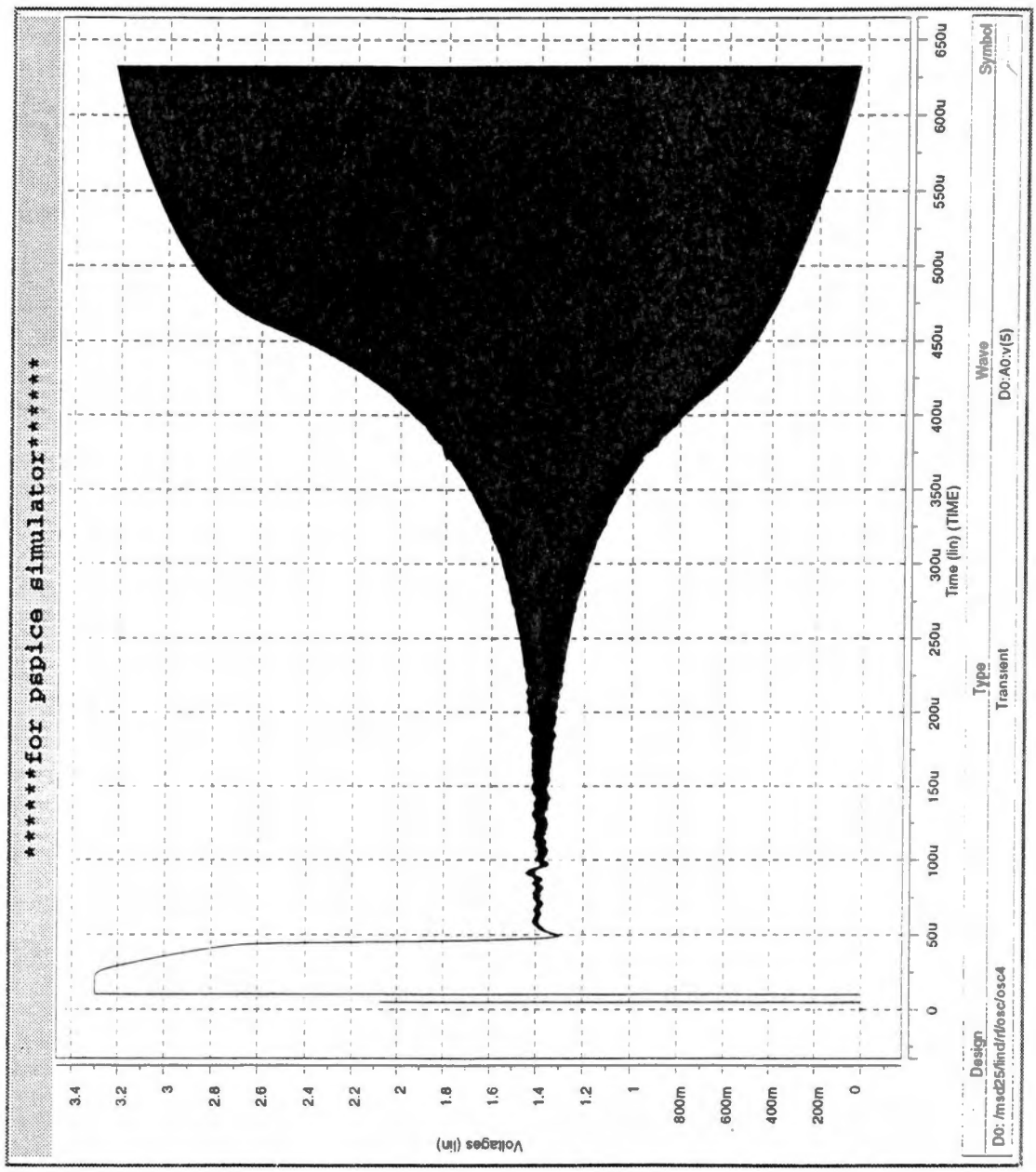


Figure 2.14 - Full Run Time Simulation

The frequency of operation can be determined by zooming in on one cycle of the simulation (after steady state) and measuring the period of the output waveform. Using Figure 2.15 the simulated output frequency is 3.57845 MHz which corresponds well to that estimated in Figure 2.12.

The average power dissipated per cycle can be estimated by performing a graphical integration of the supply current and dividing it by the period of the output. The average current times the supply voltage is the average operating power. The simulated average power consumption is approximately 480 μW which is 220 μW less than predicted by equation 2.16. Thus, the equation for average power consumption is pessimistic. This is attributed to the fact that the impedance of the crystal and 'Cg' were not taken into account, but instead only 'Cd' was accounted for. This indicates that the combination of the crystal and 'Cg' in parallel with 'Cd' actually act to lower the capacitive reactance at the output of the NAND gate. Equation 2.16 is useful to get a "ball park" figure for the operating power, but is not very precise.

2.5 Conclusions

A low-power crystal oscillator circuit has been designed and implemented for use as a reference in the transmitter system. Hand calculations and simulation results indicate that the oscillator is fully functional. Table 2.1 is a listing of the oscillator's performance parameters. The oscillator consumes 441.5 μm^2 of chip area.

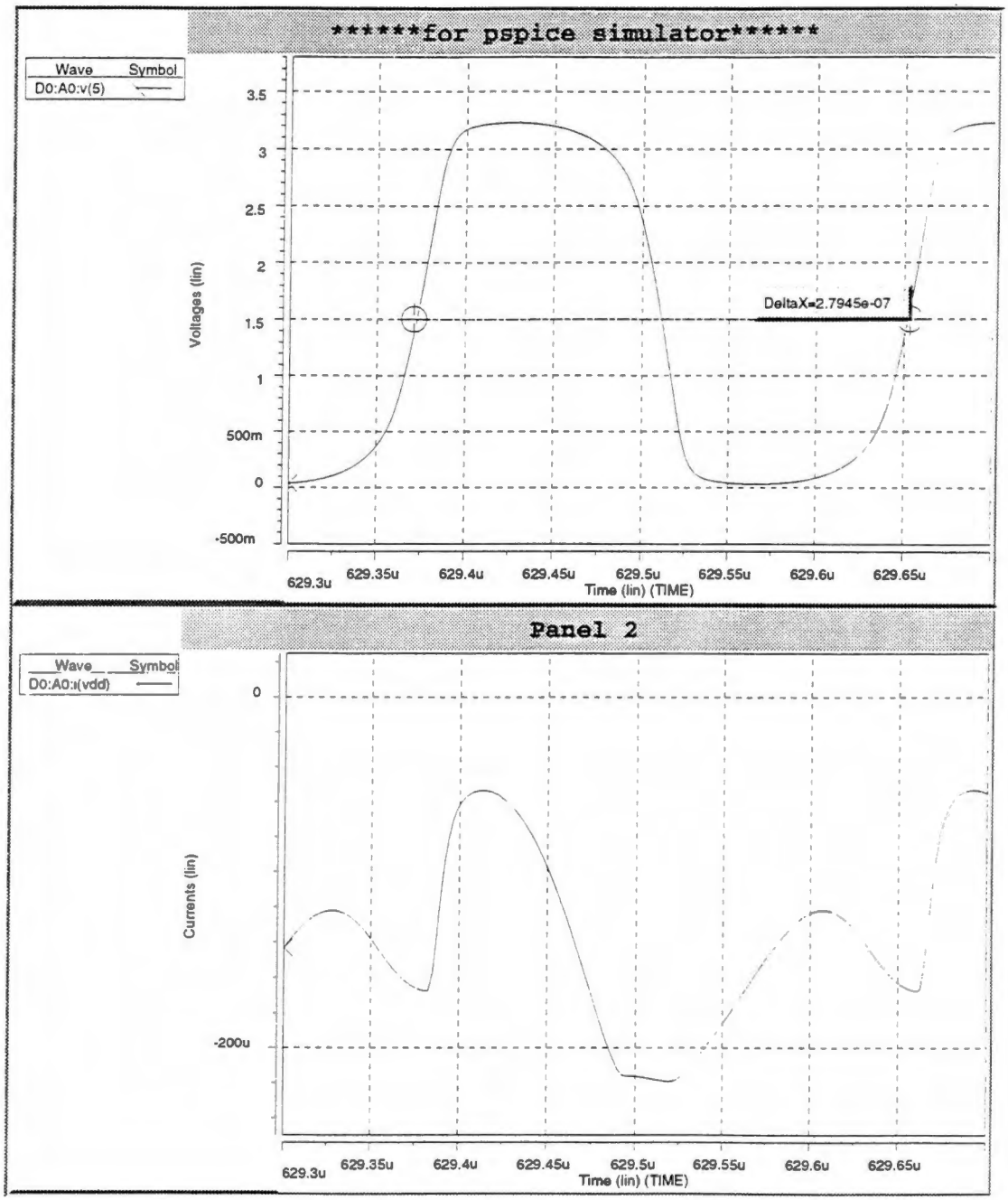


Figure 2.15 - Frequency / Power Measurement

Table 2.1 - Oscillator Performance Summary

Performance Parameter	**Value**
Frequency of Oscillation	3.5796 MHz
Simulated Operating Power (Vdd = 3.3 V)	480 μW

Chapter 3

Phase Locked Loop Design and Analysis

This chapter discusses the design, implementation, analysis and testing of the phase locked loop. The phase locked loop (PLL) used in the RF transmitter for the implantable unit is considered to be the classical digital phase locked loop topology because the divider and phase detector are fully digital [6]. This topology was chosen because it lends itself quite readily for implementation in a CMOS process. The phase locked loop is required to create the 916 MHz RF carrier signal which is modulated by the baseband digital signal through the mixer. This is accomplished by multiplying the 3.5796 MHz frequency reference by 256, which is the gain of this PLL, to achieve the 916 MHz carrier frequency. The need for a frequency multiplier arises from the fact that there are no precision crystals available at this high frequency.

3.1 PLL System Overview

The system diagram for the PLL is shown in Figure 3.1. The voltage controlled oscillator (VCO) output is divided by 256 and then compared to the precision frequency reference using a digital phase frequency detector (PFD). The output of the phase

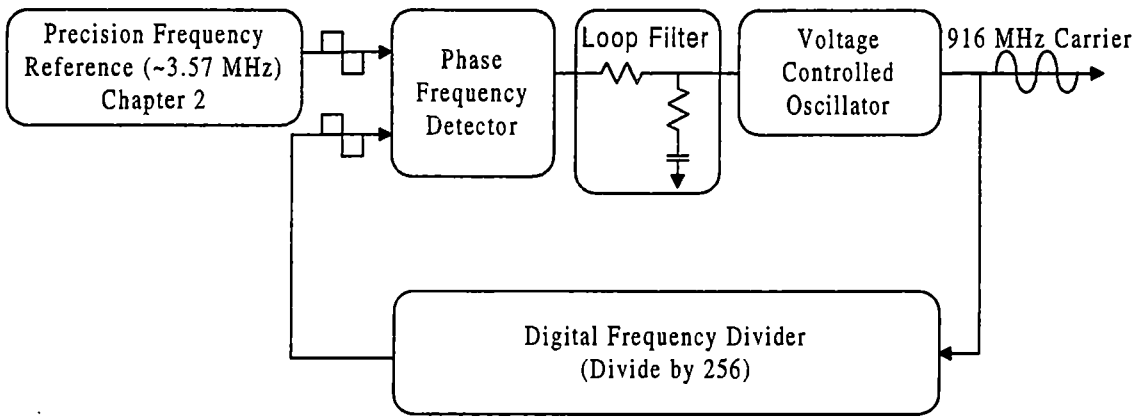


Figure 3.1 - PLL System Diagram

detector is then fed through the loop filter which provides a low frequency error signal. This error signal modulates the output frequency of the voltage controlled oscillator (VCO). Thus the PLL forms a negative feedback loop. Feedback ensures that the output frequency remains stable and phase locked with the input reference frequency. The frequency reference and feedback system can be eliminated by simply biasing the inputs of the voltage controlled oscillator (VCO) at the proper DC bias point. This is not practical however because small fluctuations in the bias at the input of the VCO over time will result in large fluctuations in the carrier frequency. Maintaining a stable carrier frequency is required for the receiver to maintain a lock on the incoming data signal. If the carrier frequency is unstable, there will be no communication between the implantible and the receiver.

3.2 PLL Performance Analysis

By performing a complete system analysis, the designer can understand which system parameters have an effect on important issues such as loop stability, lock in time, and phase noise. Before continuing the system analysis, these performance parameters must first be defined.

3.2.1 PLL Performance Parameters

Loop stability is paramount for any type of feedback system and is usually defined in terms of phase margin. Phase margin is a measure of the total phase delay incurred from the system input to the output of the feedback network. Low phase margin results in marginal stability. In terms of the PLL, low phase margin can cause the PLL's output frequency to lose lock which is unacceptable for this application.

Lock-in time is defined as the time required for the output to achieve the desired frequency at start-up [6]. For this system, a reasonable startup time is required because the transmitter is not operated continuously. For this PLL system, the lock-in time is a function of the loop filter critical frequencies as well as the gain of the phase detector and VCO as will be shown in section 3.6.

Phase noise is related to random fluctuations in the PLL output frequency [16]. This appears as a broadening of the spectral peak of the PLL's output. Excessive phase noise can greatly impair the receiver's ability to lock on the incoming RF signal. The local oscillator, loop filter and VCO all contribute to the system's total phase noise. Any phase noise present in the local oscillator is multiplied by the PLL gain (256) at the output. The local oscillator's contributions can be minimized by using a low phase noise

oscillator and a reasonably low value for the PLL closed loop gain (if the closed loop gain is too low the system's phase margin can suffer due to a large loop gain). Noise present at the loop filter's output is multiplied by the VCO's gain at the PLL output. Also noise sources within the VCO contribute to the PLL's output phase noise. Contributions from the loop filter can be reduced by using small resistance values for the loop filter and minimizing the VCO's gain. Reducing the VCO phase noise contribution requires reducing the VCO circuit noise.

3.2.2 PLL System Analysis

An analytic system evaluation requires determining the transfer functions for each of the components in the phase locked loop. Once the individual transfer functions (gains) have been formalized, the elements can be combined together and the system analyzed using classical control systems analysis [16]. Figure 3.2 is a simplified model of the PLL system for understanding of the loop analysis [6]. In this equivalent circuit the summing node and 'Kd' block represent the phase detector transfer function. The 'Kf' represents the loop filter, the 'Ko' and integrator block represent the VCO transfer functions. The feedback block 'N' represents the divider transfer function.

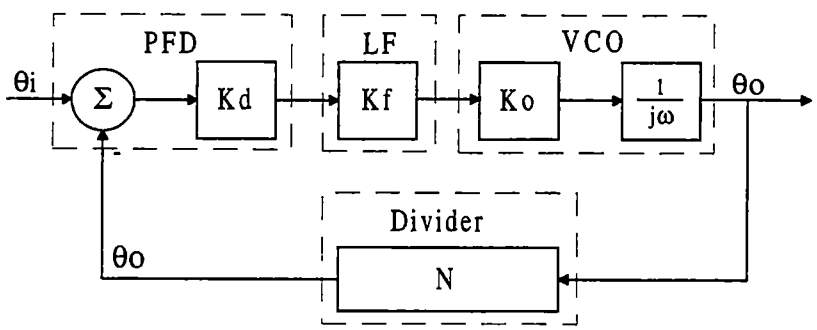


Figure 3.2 - PLL Loop Analysis Model

3.2.3 PFD Loop Transfer Function

The phase frequency detector (PFD) transfer function is defined to be

$$K_d \equiv \frac{dVout}{d\theta_e} = \frac{Vdd}{4\pi}\left(\frac{volt}{rad}\right), \qquad Eq.\ 3.1$$

where *dVout* is the change in output voltage per difference in input phase, $d\theta_e$, between the reference and divider signals [6]. *Vdd* is the power supply voltage.

Simply stated, the PFD transfer function is the change in output voltage of the PFD as a result of the difference between the phase of the incoming reference signal and that of the divided output signal from the VCO. The phase error detection range is 4π because a phase frequency detector is used as opposed to a simple exclusive-or phase detector. This means that the detector can discriminate differences in phase between -2π and 2π. The available output voltage range is determined by the type of circuit used and will be shown later in this chapter to be the supply voltage (see section 3.5).

3.2.4 VCO Transfer Function

The transfer function for the VCO has both a frequency and phase component which must be addressed separately [17]. The frequency sensitivity of the VCO transfer function is defined to be

$$K_o \equiv \frac{\Delta\omega_{out}}{\Delta V_{in}}\left(\frac{rad/\sec}{volt}\right). \qquad Eq.\ 3.2$$

The term in the numerator is the available output frequency range of the VCO which is also termed it's tuning range. The denominator is the range of input voltage required to achieve the full tuning range of the VCO. A narrow tuning range reduces the gain of the

VCO and improves the loop stability in addition to reducing the VCO's contribution to the PLL's overall phase noise. Noise present at the output of the loop filter is multiplied by the VCO's gain. A tuning range of 100 MHz centered about the 916 MHz carrier frequency is nominally chosen for this application.

The output component of the VCO due to phase is represented by Equation 3.3:

$$\theta_{out} \equiv \int \omega_{out}\, dt\, (rad)\,. \qquad Eq.\ 3.3$$

The first derivative of phase with respect to time is frequency [17]. In the frequency domain an integral is represented by

$$\int dt \Leftrightarrow \frac{1}{s}\, (rad)\,. \qquad Eq.\ 3.4$$

This results in an inherent PLL system phase shift of -90° which imposes restraints on system stability.

3.2.5 Loop Filter Transfer Function

The transfer function of the loop filter depends entirely upon the topology that is incorporated. For this PLL system, a lag-lead filter was incorporated in the design for its simplicity and loop compensation characteristics. Compensation is achieved by introducing a pole and also a zero which is needed because of the -90° phase shift imposed by the VCO. A simple low pass filter is not used because it contributes only a pole to the system. The actual loop filter circuit is shown in Figure 3.15. The loop filter transfer function is defined to be [16]:

$$K_f \equiv \frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}\left(\frac{volt}{volt}\right), \qquad Eq.\ 3.5$$

where $\tau_1 = R_1 C\,, \quad \tau_2 = R_2 C\,.$

The time constants , τ_1 and τ_2, of the loop filter have a direct effect on the PLL's stability and lock-in time [6].

3.2.6 Divider Transfer Function

The divider transfer function is defined to be [16]

$$N \equiv 256\left(\frac{\frac{rad}{\sec}}{\frac{rad}{\sec}}\right). \qquad Eq.\ 3.6$$

The divider transfer function is the PLL's ideal closed loop gain. A division factor of 256 is chosen as a trade off between system stability and output phase noise. A large division factor lowers the system loop gain which improves system stability, however any phase noise present in the local oscillator is multiplied by PLL gain.

3.2.7 PLL Loop Analysis

Expressions for the overall loop gain of the system and the closed loop system response can now be found. These are needed to determine what changes can be made to improve the systems performance.

The loop gain is found by breaking the loop (at any place) and applying an appropriate signal and measuring the return signal. This is accomplished by multiplying the system's individual transfer functions together (carefully keeping track of the units). The loop gain for this system is shown in Equation 3.8 [16]. Analysis of the loop gain frequency response is needed to determine the overall stability of the system.

$$T(s) = -K_d\left(\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}\right)\left(\frac{K_o}{s}\right)\left(\frac{1}{N}\right). \qquad Eq.\ 3.7$$

The overall closed loop gain of the phase locked loop is found by taking the product of the ideal closed loop gain and the ratio of the loop gain divided by 1 minus the loop gain. Equation 3.8 is the expression for the closed loop gain of this system [16]:

$$A_{CL}(s) = N\cdot\left(\frac{-T(s)}{1-T(s)}\right). \qquad Eq.\ 3.8$$

Equation 3.8 is equivalent to [18]

$$A_{CL}(s) = N\cdot\left(\frac{\left(\frac{K_oK_d}{N}\right)\left(\frac{1+s\tau_2}{\tau_1+\tau_2}\right)}{s^2+\left(\frac{1+\frac{K_oK_d}{N}\tau}{\tau_1+\tau_2\ \ _2}\right)s+\frac{\frac{K_oK_d}{N}}{\tau_1+\tau_2}}\right). \qquad Eq.\ 3.9$$

The denominator in Equation 3.9 can be written in the normalized form,

$$s^2+2\zeta\omega_n s+\omega_n{}^2, \qquad Eq.\ 3.10$$

where $$\omega_n = \sqrt{\frac{K_o K_d}{N(\tau_1 + \tau_2)}}, \quad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{N}{K_o K_d}\right).$$

The natural frequency of the PLL, ω_n, is the system's correction bandwidth [18]. The PLL can track any phase or frequency changes which occur from zero frequency to ω_n. For this application, ω_n is chosen to be 1% of the reference (35.796 kHz) to provide sufficient filtering of the reference frequency at the output of the PLL. The damping factor, ζ, is a measure of the system's transient response to a change in input reference frequency. A ζ value of 0.707 provides a critically damped transient response. The lock-in time of the PLL is directly related to the natural frequency and is defined to be [18]

$$T_L \approx \frac{2\pi}{\omega_n}. \qquad Eq.\ 3.11$$

At start-up, when the PLL is not locked, Equation 3.11 indicates the output of the PFD and the loop filter perform a damped oscillation at approximately ω_n and that lock is achieved within one cycle of this oscillation (not accounting for VCO oscillation build-up). For a natural frequency of 35.769 KHz the approximate lock-in time is 28 μs which is acceptable for this application. The individual circuit blocks and associated transfer functions must be quantified before Equations 3.7 - 3.11 can be applied further.

3.3 Voltage Controlled Oscillator (VCO) Design

The VCO is comprised of an oscillator circuit and an oscillator biasing circuit. Each is presented separately, and then analyzed together as a system.

3.3.1 Oscillator

The VCO, as described previously, is a circuit which converts an input voltage to an output frequency. It can thus be categorized as a voltage to frequency converter. A common CMOS implementation of a voltage to frequency converter (which excludes the use of inductors or large capacitors) is a starved inverter ring oscillator.

The basic circuit for a starved inverter is shown in Figure 3.3. The starved inverter's input to output delay (the time required for 'Vout' to reach steady state after a state change of 'Vin') can be altered by varying the bias voltage , 'Vbias', at the gate of M2. Changing 'Vbias' modulates the channel current supplied by 'M2' which alters the charging rate of 'Cnode'. 'Cnode' refers to the parasitic capacitance associated with the output node.

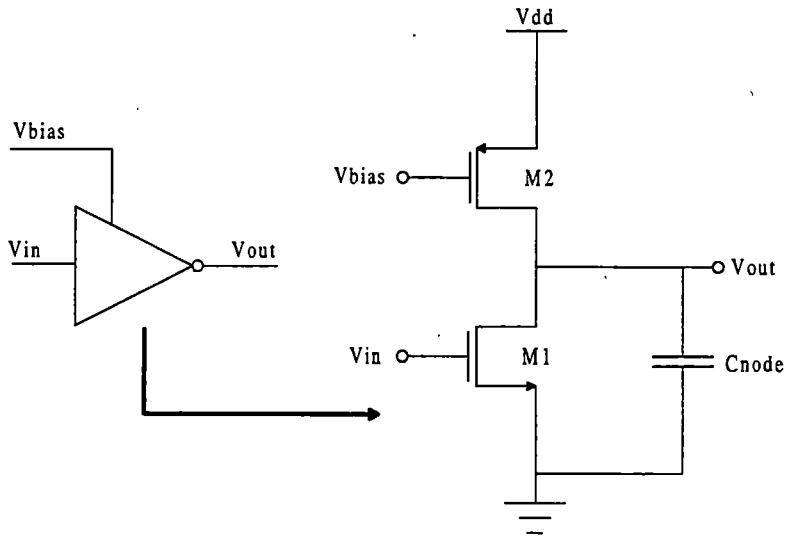


Figure 3.3 - Starved Inverter

A ring oscillator is formed by connecting an odd number of three or more inverters from output to input with output of the last stage connected to the input of the first stage. To achieve the required 916 MHz carrier frequency, the implantable transmitter uses two starved inverters with a CMOS inverter as the output stage to comprise a three stage ring oscillator. The complete schematic of the ring oscillator circuit is shown in Figure 3.4. In addition to the ring oscillator, transistors 'M7 - M10' are necessary to sufficiently drive the digital divider and mixer.

The relationship between the output frequency and 'Vbias' is now developed by making the following assumptions: 'M1' and 'M3' are ideal current sources, 'M2' and 'M4' behave as ideal switches (zero on-resistance) and the CMOS inverter ('M5' and 'M6') introduces no time delay from input to output.

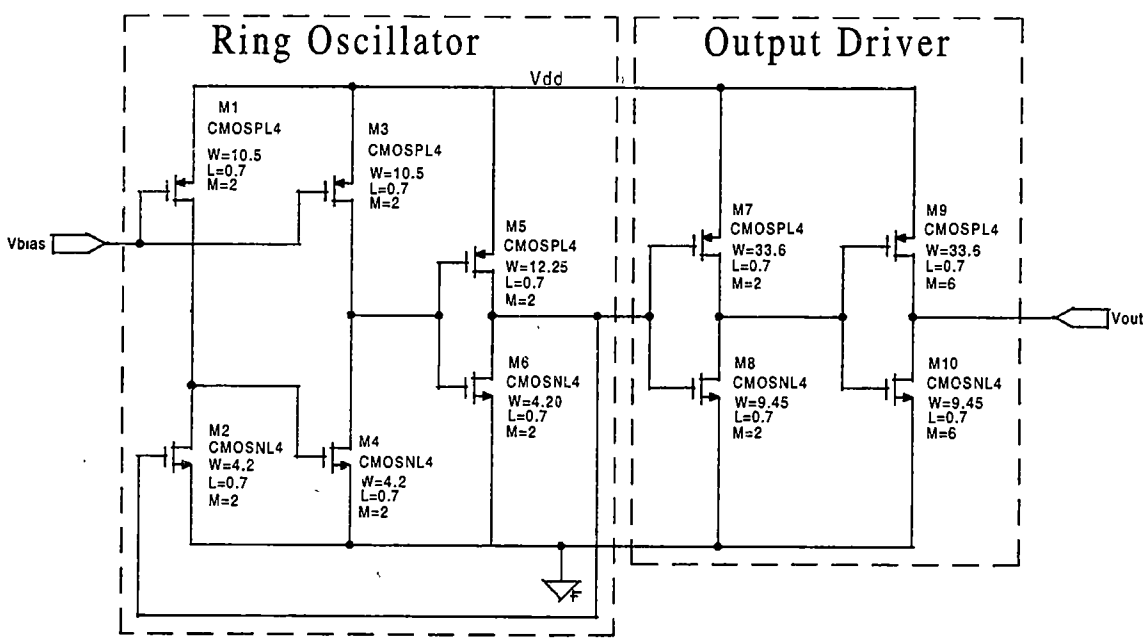


Figure 3.4 - Starved Inverter Ring Oscillator

Figure 3.5 shows the equivalent circuit for the analysis and the corresponding waveforms at each node. The period of the output is equivalent to twice the time required for the voltage at node cs1 to reach the switching threshold of the following stage. As the current in 'M1' and 'M3' becomes larger, the charging time at nodes cs1 and cs2 decreases and the output frequency increases. The analysis is simplified by assuming that 'M1' and 'M3' are operating in the saturation region which is correct for a certain range of 'Vbias' voltages. The low range of 'Vbias' is required to keep these devices form operating in the ohmic region and is determined by the relationship [14]

$$V_{SD}(sat) \geq V_{SG} - |V_{TP}| . \qquad Eq.\ 3.12$$

Assuming that the switching threshold of the following stage is half the supply voltage, the minimum value of 'Vbias' is 0.76 volts. The upper range of Vbias is 2.41 volts and is required to keep 'M1' and 'M3' in strong inversion.

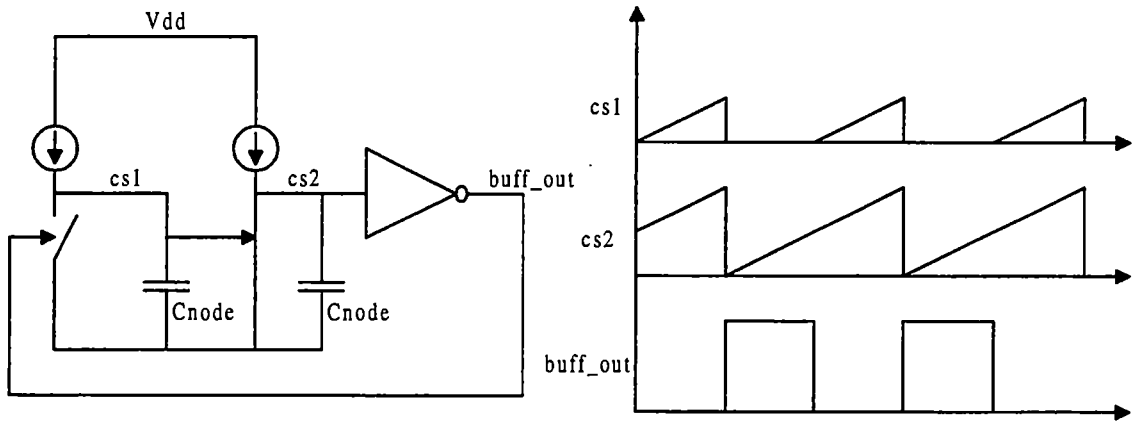


Figure 3.5 - Ring Oscillator Analysis Model

Therefore, given the aforementioned constraints, the frequency output as a result of bias voltage is derived as follows:

The charging rate of the nodal capacitance takes the form

$$\frac{\Delta V}{\Delta t} = \frac{I}{C_{NODE}}. \qquad Eq.\ 3.13$$

Rearranging this equation to determine the charging time yields

$$\Delta t = \frac{C_{NODE}}{I}\Delta V. \qquad Eq.\ 3.14$$

The output frequency of the oscillator is approximately the time required for two transitions and is expressed as

$$f_{out} = \frac{1}{2\Delta t} = \frac{I}{2 \cdot C_{NODE} \cdot \Delta V}. \qquad Eq.\ 3.15$$

The current I is the drain current of the PMOS device and is shown to be (neglecting channel length modulation effects) [14]

$$I = I_D = \frac{K_P}{2}\left(\frac{W}{L}\right)_P \left(V_{SG} - |V_{TP}|\right)^2. \qquad Eq.\ 3.16$$

The resulting output frequency is now given as

$$f_{out} = \frac{\frac{K_P}{2}\left(\frac{W}{L}\right)_P \left(V_{SG} - |V_{TP}|\right)^2}{2 \cdot C_{NODE} \cdot \Delta V}, \qquad Eq.\ 3.17$$

where, $V_{SG} = V_{DD} - V_{bias}$, *Eq.* 3.18

and, $\Delta V = Switching\ Threshold = \frac{Vdd}{2}$. *Eq.* 3.19

The expression for the output frequency with respect to 'Vbias' is

$$f_{out}(V_{bias}) = \frac{\frac{K_P}{2}\left(\frac{W}{L}\right)_P \left(V_{DD} - V_{bias} - |V_{TP}|\right)^2}{C_{NODE} \cdot V_{DD}}. \qquad Eq.\ 3.20$$

Therefore the output frequency depends approximately on the square of the 'Vbias'. However, the relationship can be linearized over a narrow tuning range (small range of output frequency). Using Equation 3.20 the range for Vbias required for a tuning range of 100 MHz, centered about the 916 MHz carrier frequency, is approximately 1.905 < 'Vbias' < 1.932 (using the circuit in Figure 3.4 and the process parameters in Appendix 1, Cnode = 30 fF).

Simulations performed on the circuit of Figure 3.4 indicate that the simplified model used to develop Equation 3.20 is not valid at 916 MHz (see Appendix 2 for list files). Figure 3.6 shows the simulated waveforms present at nodes cs1, cs2 and buff_out of Figure 3.5. These indicate that the delay due to the output CMOS buffer and the discharging time required for 'Cnode' are not negligible. The simulated range of 'Vbias' required to achieve a 100 MHz tuning range about the carrier frequency is 1.38 < 'Vbias' <1.524. This is significantly different from that predicted by Equation 3.20. As a result, Equation 3.20 is only valid for lower frequencies.

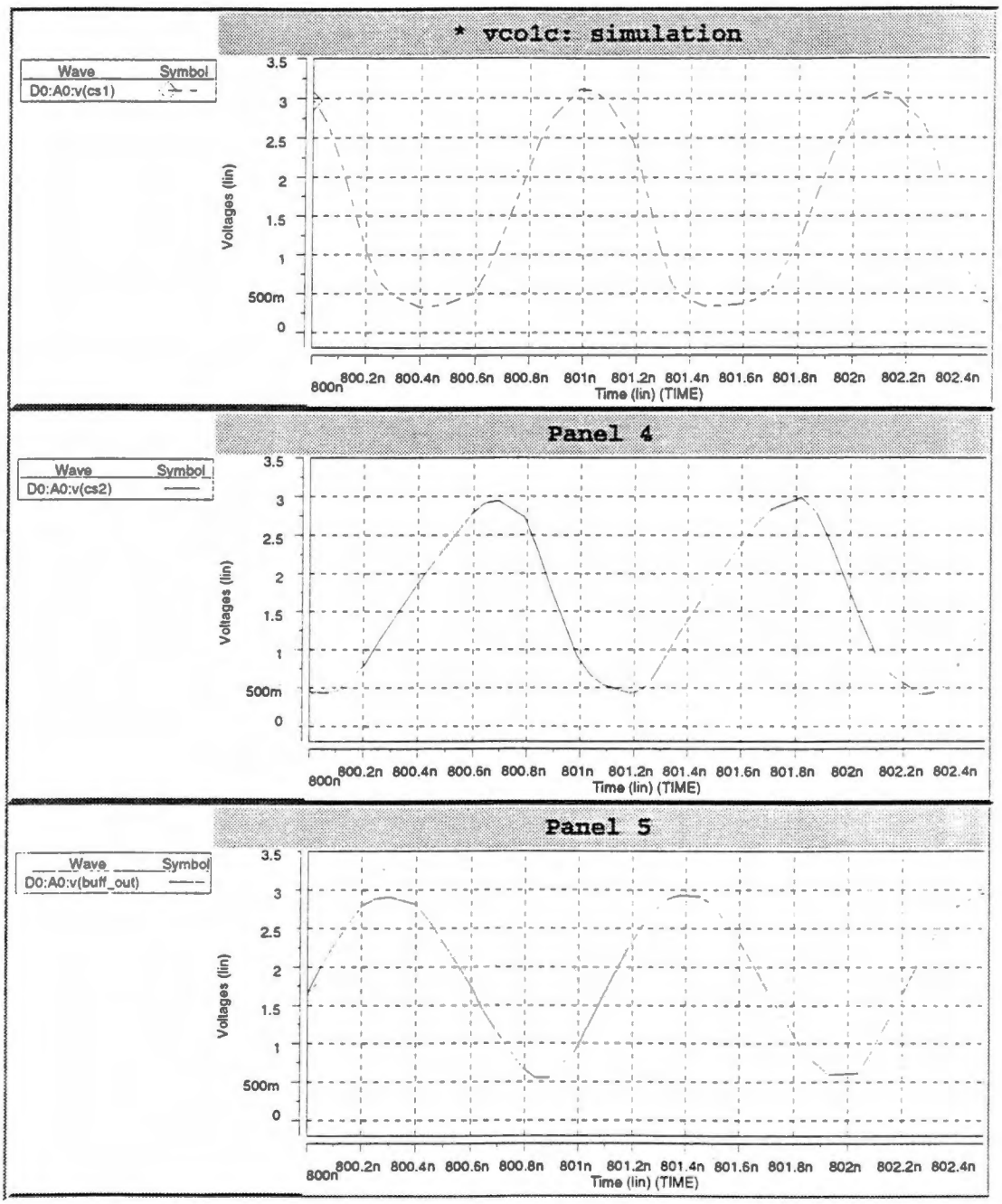


Figure 3.6 - Simulated Ring Oscillator Waveforms

3.3.2 Voltage Controlled Biasing

A biasing circuit was designed to control the gate bias voltage of the PMOS devices in the ring oscillator as a function of the loop filter output voltage. From the point of view of a control system, the circuit measures the difference between the loop filter output voltage and some known reference voltage and adjusts the oscillator bias to achieve the desired 916 MHz carrier frequency. In addition to providing dynamic control of the VCO output frequency, the biasing circuitry also provides a means of adjusting the overall tuning range of the oscillator.

One of the classic analog circuits which provides a difference measurement between two voltages is a differential pair. A differential pair varies the drain current in each transistor as a function of the voltage difference between the gates. This dynamic control of channel current can be used to establish the tuning range of the oscillator by mirroring the current from one side of the differential pair to an output stage which performs a current to voltage transformation.

The bias control should also provide some means of offsetting this tuning range so the center of the tuning range is set at 916 MHz . This achieves a balanced tuning range about the carrier frequency. The circuit in Figure 3.7 satisfies these requirements.

The circuit operates in the following manner. The frequency offset is controlled by the current through 'Roffset'. This provides a constant current source which is relatively unaffected by the current in 'M2'. The tuning range is controlled by adjusting 'Rtune' which limits the available current in the differential pair. The offset current and

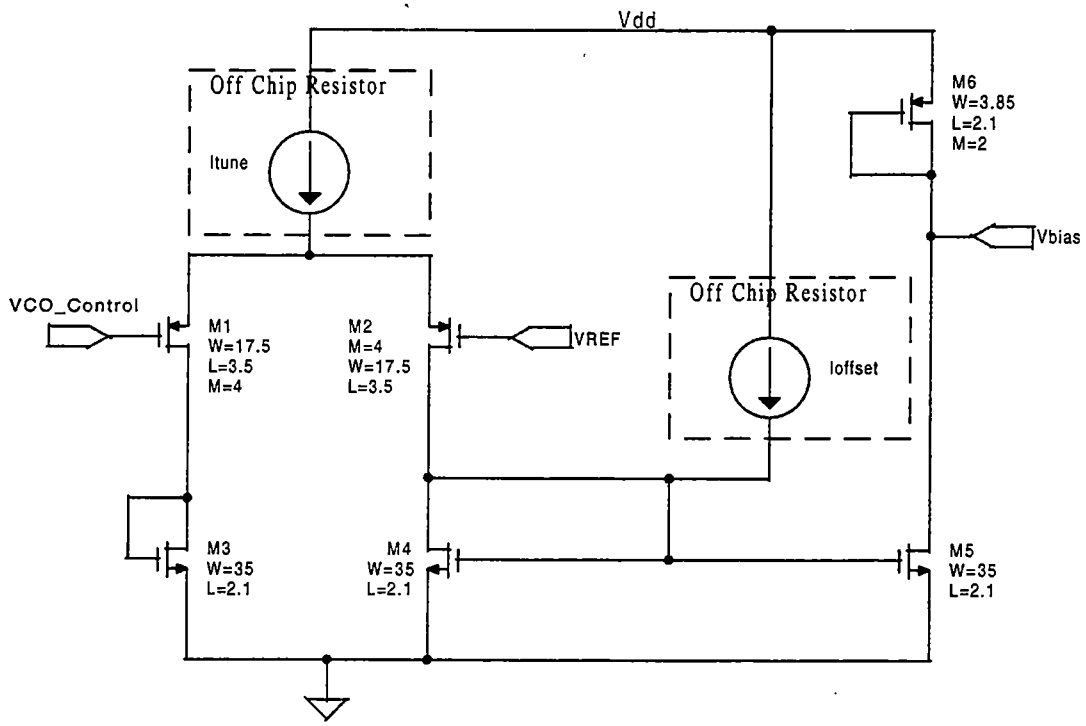


Figure 3.7 - Ring Oscillator Biasing Circuit

the current in 'M2' are summed together in 'M4'. This current is then mirrored to 'M5' which controls the current in 'M6'. This current is converted to a voltage at the gate of 'M6' which provides the bias voltage to the ring oscillator.

Now that the bias circuit topology has been developed, the transfer function from the 'VCO Control' input to the 'Vbias' output is developed. To derive this expression, the large signal behavior of the differential pair will be used to form the complete expression. The current in 'M2' is shown to be [19]

$$I_{D2} = \frac{I_{TUNE}}{2}\left(1 - \sqrt{\left(\frac{\beta_{1,2} \cdot V_{id}^{\,2}}{I_{TUNE}} - \frac{\beta_{1,2}^{\,2} \cdot V_{id}^{\,4}}{4 \cdot I_{TUNE}}\right)}\right), \qquad Eq.\ 3.21$$

where $$V_{id} = V_{VCO\_CONTROL} - V_{VREF}, \qquad Eq.\ 3.22$$

and, $$\beta_i = K_P \cdot \left(\frac{W}{L}\right)_i . \qquad Eq.\ 3.23$$

The current in 'M6' is the mirrored sum of the current in 'M2' and the offset current

$$I_{D6} = \left(\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}\right) \cdot \left(I_{OFFSET} + I_{D2}\right). \qquad Eq.\ 3.24$$

The resulting output bias voltage is shown to be (neglecting channel length modulation)

$$V_{bias} = V_{dd} - \left(\sqrt{\frac{2 \cdot I_{D6}}{\beta_6}} + |V_{TP}|\right). \qquad Eq.\ 3.25$$

Note that Equation 3.21 is bound by the condition

$$V_{id} \leq \sqrt{\frac{2 \cdot I_{TUNE}}{\beta_{1,2}}} . \qquad Eq.\ 3.26$$

Using Equations 3.21 - 3.25 and the transistor sizes shown in Figure 3.6 (process parameters in Appendix 1), a plot of 'Vbias' vs. differential input voltage is shown in Figure 3.8. 'Itune' and 'Ioffset' are 13 μA and 36 μA respectively. Figure 3.7 indicates that these current levels provide the necessary range of 'Vbias' (1.38 < 'Vbias' <1.524) to achieve the desired tuning range of the ring oscillator (100 MHz).

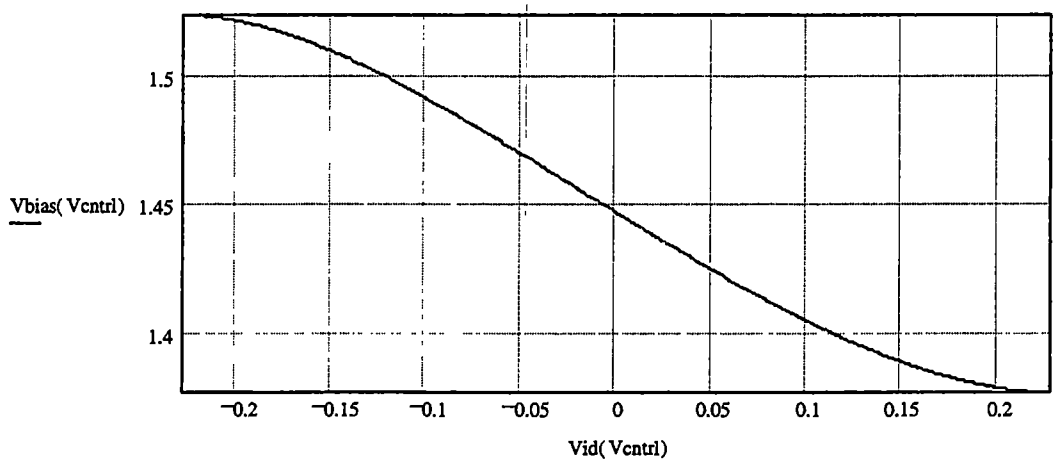


Figure 3.8 - Vbias vs. Vin (differential)

Simulations of the VCO bias control circuit indicate that the actual current levels for 'Itune' and 'Ioffset', to achieve a 100 MHz tuning range, are 17.3 μA and 42.3 μA respectively (see Appendix 2). These current levels are produced using a 634 KΩ resistor for 'Itune' and a 53.6 KΩ resistor for 'Ioffset' (standard 1% resistor values). These bias levels provide a 'Vbias' range of 1.37 volts to 1.52 volts. Figure 3.9 shows the simulated range of 'Vbias' vs. 'VCO_Control'. 'Vbias' is approximately linear over a range of 1.38 to 1.51 volts which corresponds to a 'VCO_Control' range of 0.4 volts (1.45 to 1.85 volts). The 'VCO_Control' range is equivalent to the ΔV_{in} term in Equation 3.2.

An important consideration of the VCO bias circuitry is the amount of delay from the 'VCO_Control' node to the 'Vbias' node which controls the frequency of oscillation. The time constant of the VCO is represented by τ_{VCO} and is particularly important when considering its effect on the loop gain of the system. Recall that the phase component of the VCO output signal introduces an immediate negative 90° phase shift to the system.

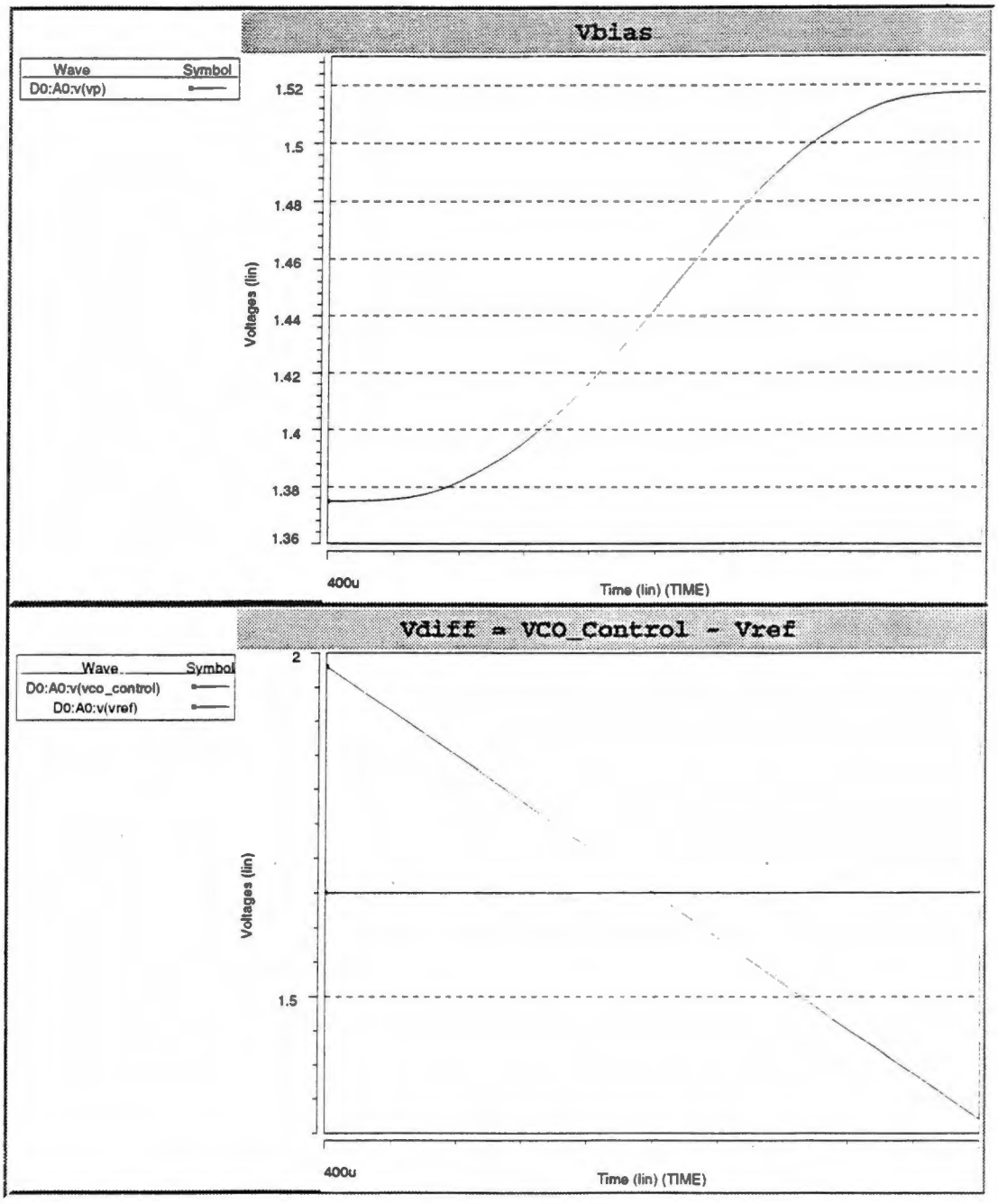


Figure 3.9 - 'Vbias' vs. 'VCO_Control'

Therefore, if τ_{VCO} becomes too large, it will degrade the phase margin of the system and could lead to a condition of instability. Care must be taken then to minimize the delay introduced by the biasing circuitry.

An estimate of τ_{VCO} is obtained by finding the time constant at each node in the signal path of the biasing circuitry and then summing together each of these time constants (using the circuit in Figure 3.7, 'Ibias' = 17.3 μA, 'Ioffset' = 42.3 μA). All capacitance values are from the VCO bias simulation list files found in Appendix 2.

Input Stage:

$$\tau_{in} = (R_{LF}) \cdot \left(C_{GS1} + C_{DS1} \left(1 + \frac{gm_1}{gm_3} \right) \right) \qquad Eq.\ 3.27$$

Second Stage:

$$\tau_2 = \left(R_{OFFSET} \left\| \left(\frac{1}{gm_4} \right) \right. \right) \cdot \left(C_{DG2} + C_{GS4} + C_{GS5} + C_{GD5} \left(1 + \frac{gm_5}{gm_6} \right) \right) \qquad Eq.\ 3.28$$

Output Stage:

$$\tau_{out} = \left(r_{o5} \left\| \frac{1}{gm_6} \right. \right) \cdot (C_{GD5} + C_{GS6} + C_{OSC}) \qquad Eq.\ 3.29$$

Bias Circuit Signal Path Delay:

$$\tau_{VCO} = \sum \tau \equiv (\tau_{in} + \tau_2 + \tau_{out}) \qquad Eq.\ 3.30$$

The total time constant is calculated to be 36 ns ('Itune' = 17.3 μA, 'Ioffset' = 42.3 μA) which is equivalent to 4.3 MHz high frequency roll off. The pole introduced by the

biasing circuitry is far enough away from the loop bandwidth so as not to interfere with the PLL' stability.

3.3.3 Complete VCO Circuit

The complete VCO circuit as implemented is shown in Figure 3.10. Transistors 'MSB1-4' provide the ability to disable the VCO when the transmitter is not used. The resistors which provide the bias currents, 'Itune' and 'Ioffset', are off-chip to provide the ability to adjust these values in the event that the simulated values are not accurate. The large resistance values required would also consume a large amount of chip area. The input differential pair comprised of 'M5' and 'M6' is laid out in a common centroid configuration to minimize the effect of process variation on the chip. The total area of the VCO is 49,098 μm^2. All the power supply traces are very wide to reduce parasitic resistance and inductance effects.

3.3.4 VCO Simulation Results

The VCO circuit of Figure 3.10 is now simulated to determine the operating power and the tuning range. Simulations are performed on the extracted circuit layout (Appendix 2) with bias resistor values of 634 KΩ for 'Itune' and 53.6 KΩ for 'Ioffset'. The reference voltage, 'VREF', at the gate of 'M6' is 1.65 volts. A 0.5 pF capacitor is added to the VCO output in the simulation file to verify the VCO's ability to drive the mixer and the divider.

Simulating the power dissipation of the VCO is accomplished by holding the 'VCO_Control' node at 1.65 volts and running the simulation long enough to achieve a steady output frequency (1 μsec in this case). The output frequency for this simulation is

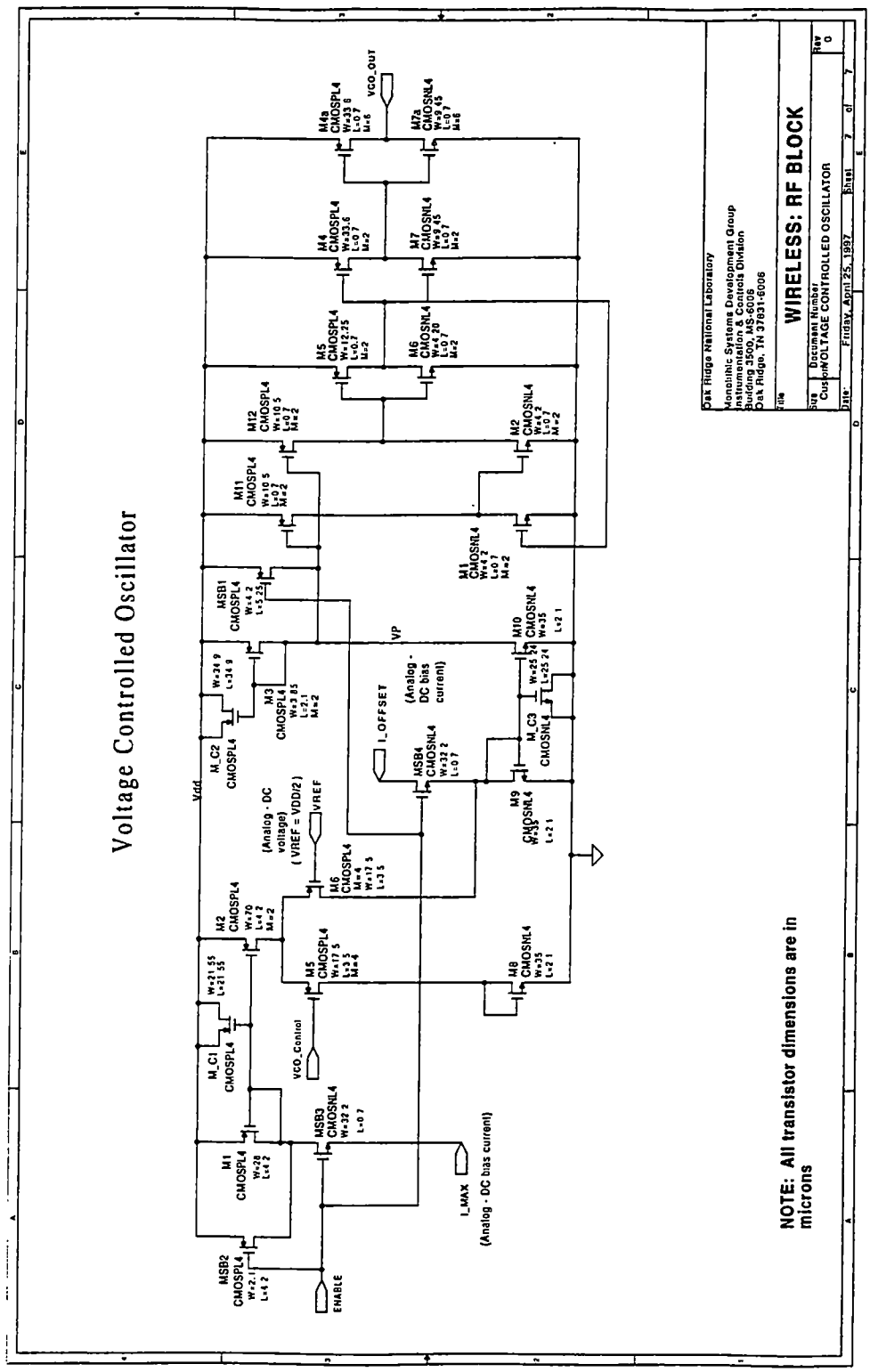


Figure 3.10 - Complete VCO Schematic

913 MHz which is very close to the desired carrier frequency. Therefore, the power measurement should hold for a 916 MHz output. Figure 3.11 shows the VCO output and supply current for one cycle. The average power dissipated is approximately 28 mW (~8.5 mA average current).

The tuning range is determined by running simulations with the 'VCO_Control' voltage at 1.45 and 1.85 volts (required range for 'Vbias' to be linear) respectively and measuring the resultant output frequency. Figure 3.12 shows the tuning range simulation results. The output frequency is found by measuring the average period over ten cycles and taking the inverse. The lower and upper frequency limits are 875 MHz and 966 MHz respectively. This provides a tuning range of 91 MHz over a 0.4 volt 'VCO_Control' input voltage range. The gain of the VCO, K_0, can now be quantified using the tuning range simulation results. For tuning range of 91 MHz and a linear input voltage range of 0.4 volts the resulting gain is shown to be (using Equation 3.2),

$$K_0 = \left(\frac{2\pi \cdot 91 \cdot 10^6 \cdot \frac{rad}{\sec}}{0.4 \cdot volt} \right) \cdot \left(\frac{1}{s} \right). \qquad Eq.\ 3.31$$

3.4 Frequency Divider

The output of the VCO must be divided by 256 to compare the output frequency to the 3.5796 MHz reference. The division operation is accomplished using an eight stage digital divider. The divider is comprised of eight D-flip flops with the output of each stage connected to the clock line of the subsequent stage and having the inverted output from each stage wired back to it's data input line.

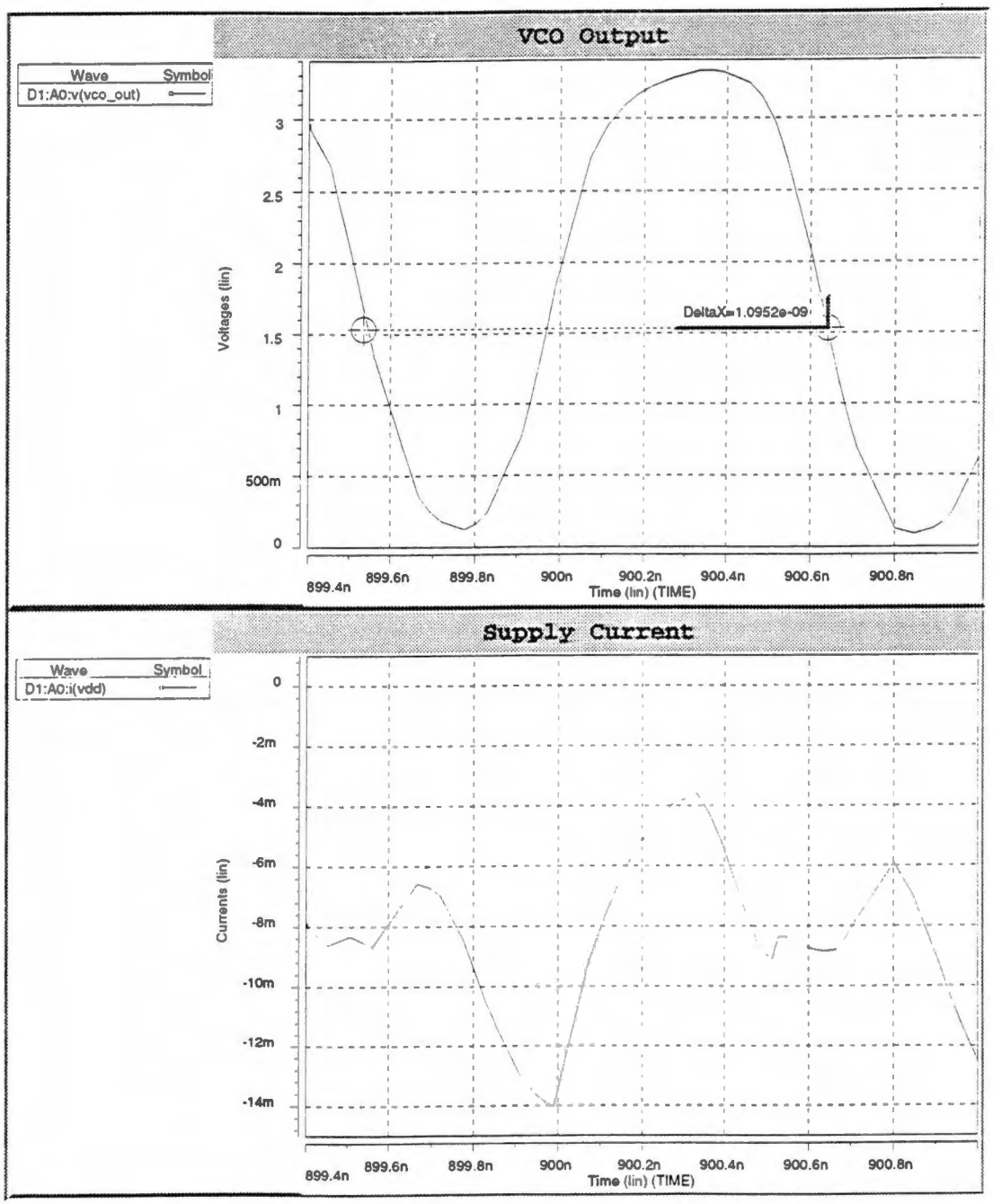


Figure 3.11 - Output Frequency and Supply Current

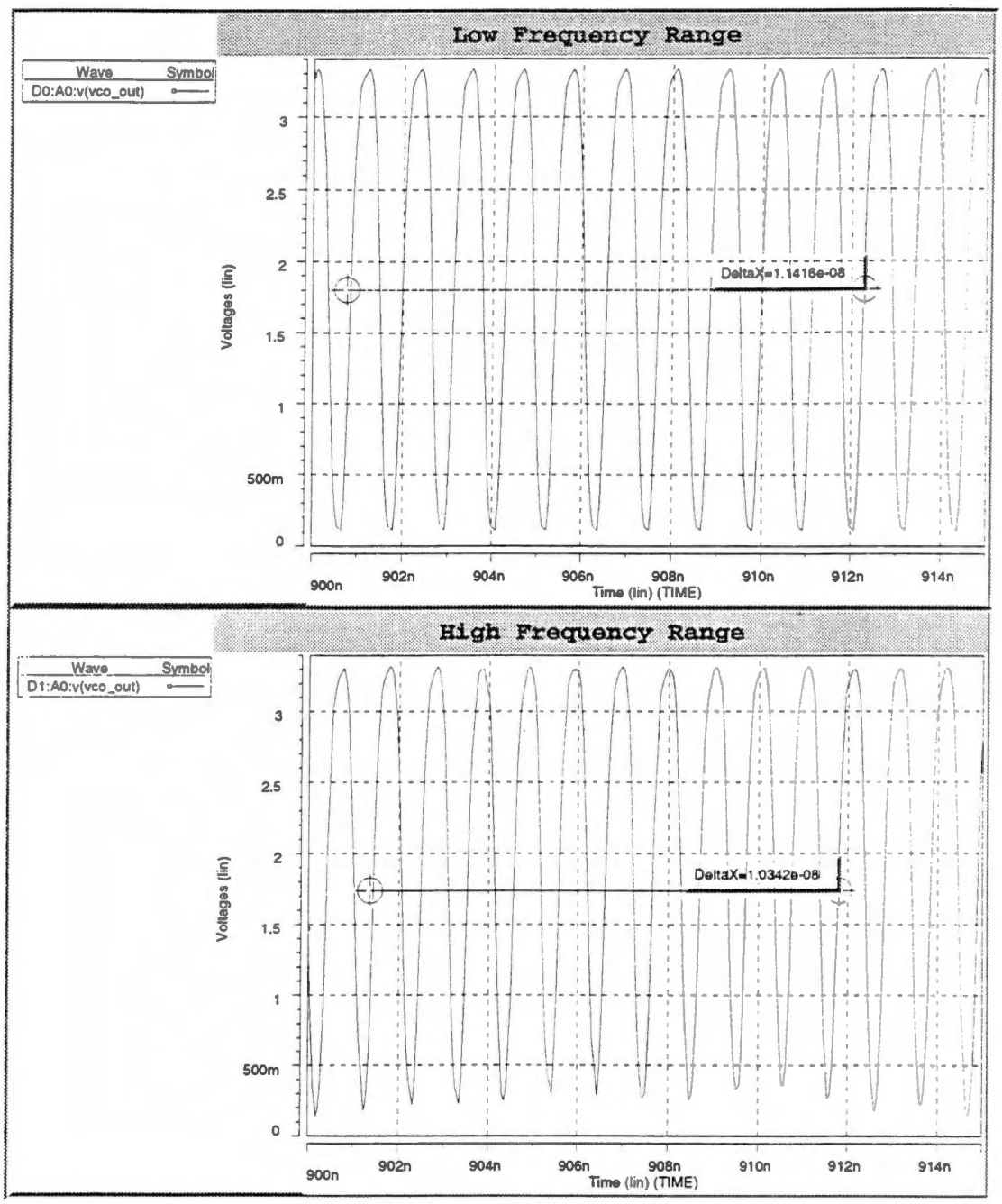


Figure 3.12 - VCO Tuning Range Simulation

The clock line of the first stage is connected to the output of the VCO. Figure 3.13 shows the schematic for the divider which is used. The flip-flops used are the DFRF311 (CMOS) and the DNRF312 (NMOS) which are part of the standard cell library from the Institute for Technology Development [20]. Each flip-flop divides its clocking frequency by two. A digital divider is implemented because of relative simplicity and robust operation compared to other types of divider topologies such as the use of analog multipliers. A digital implementation also lends itself well to a CMOS process. There is one problem associated with this topology however. The flip-flop clocked by the VCO runs at 916 MHz which exceeds by nearly 300 MHz the frequency at which the standard cell CMOS flip-flop can operate in the HP 0.5u process.

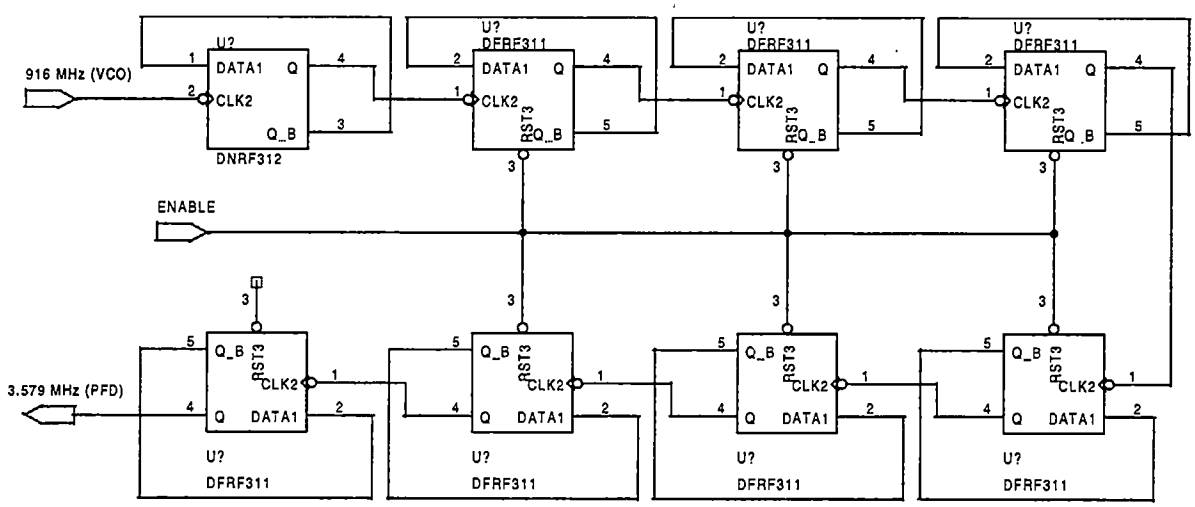


Figure 3.13 - Digital Divide by 256 Circuit

Efforts were made to stretch the cell in both height and width in an effort to increase the bandwidth but the highest functional frequency achieved in the simulations was about 800 MHz. The solution to this problem is to use an NMOS flip-flop (DNRF312) for the first divider stage. An NMOS flip-flop differs form a CMOS flip-flop in that the gate voltage of the PMOS transistors are biased at a constant voltage. Resultantly, the PMOS devices are always in an 'on' state. This significantly speeds up the maximum clocking rate of the flip-flop. The drawback to this solution is the high operating power that is associated with using NMOS logic [15]. When the NMOS device (in a particular stage) is turned on, the PMOS device acts as a current source to ground and thus dissipates much more power than CMOS logic. The average simulated power dissipation for the NMOS flip-flop running at 916 MHz is approximately 18.15 mW. Due to time constraints on the project, the NMOS flip-flop was used for the first divider stage in spite of the excessive power dissipation. Future efforts should be directed toward developing a high speed custom CMOS flip flop for use in future PLL applications.

3.5 Digital Phase Frequency Detector

The phase frequency detector (PFD) compares the digital divider's output phase and frequency to that of the frequency reference [16]. The output of the phase detector is the PLL error signal that is filtered, via the loop filter, the output of which controls the VCO input. Thus the phase detector output controls the VCO's output frequency. The phase detector circuit is shown in Figure 3.14 [6]. The phase detector functions as follows. The frequency divider output and frequency reference each clock a flip-flop.

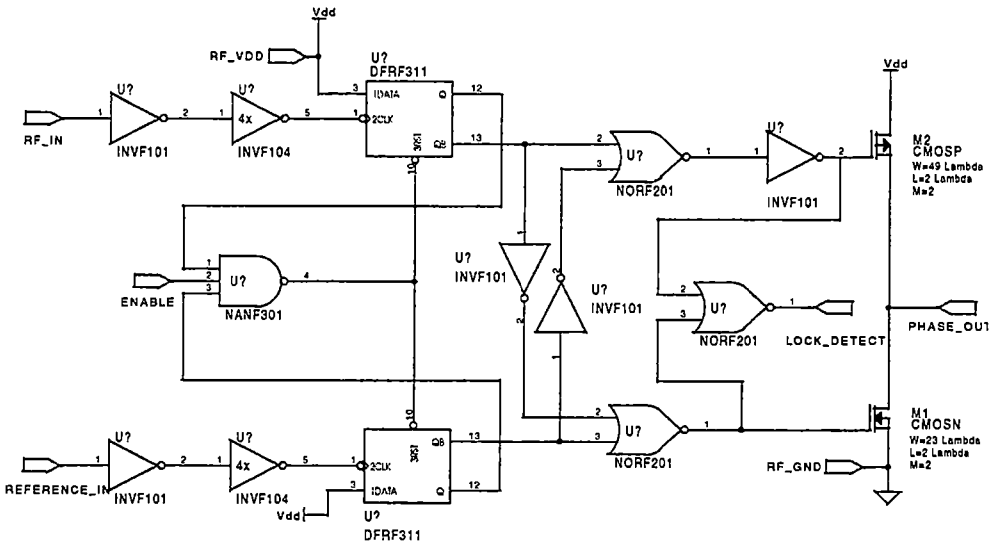


Figure 3.14 - Digital Phase Detector

If the clocking occurs simultaneously, both output transistors remain in a high impedance state which indicates a loop locked condition and can be monitored at the 'LOCK_DETECT' output. If one of the edges occurs before the other, one of the transistors will be in a low impedance state until the other edge is clocked. The result is a change in the output voltage for a period of time that is equal to the phase difference of the two clocking signals. This type of phase detector locks the PLL output phase to that of the frequency reference [6]. The output voltage range is set by the supply voltage since it is a tri-state output. The phase aligning operation of this circuit results in a phase detecting range of -2π to 2π. The plot of average output voltage versus input phase difference in Figure 3.15 shows graphically the PFD's transfer function which is given in Equation 3.1.

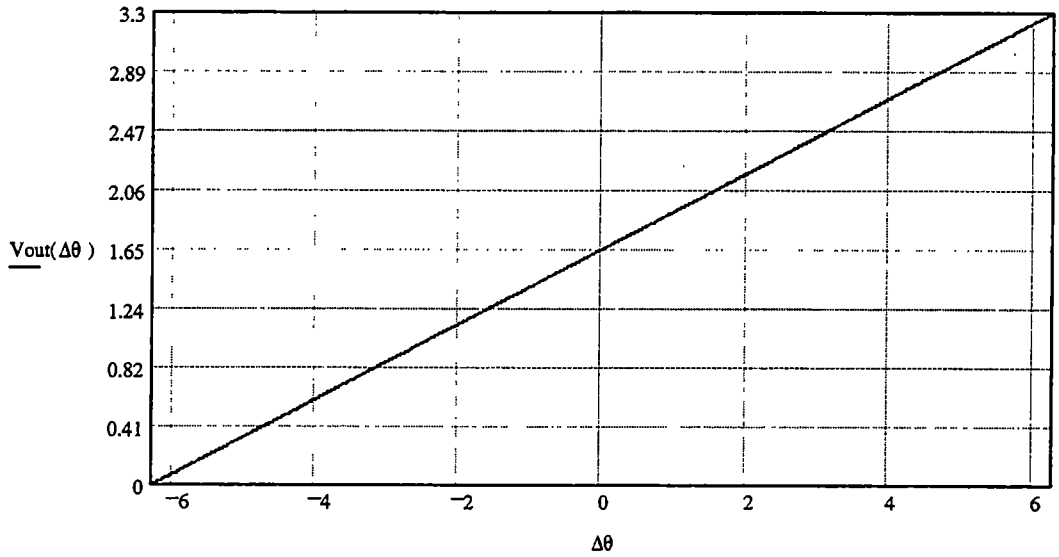


Figure 3.15 - PFD Output Voltage vs. Input Phase Difference

3.6 Loop Filter

The loop filter reduces the bandwidth of the phase detector output correction signal before it modulates the VCO [16]. For this system, the loop filter is a lag-lead low pass filter as shown in Figure 3.16. The filter's critical frequencies are determined by the PLL natural frequency (ω_n), damping factor (ζ), and the gain functions of the VCO, PFD and divider as shown in Equation 3.10. For a natural frequency of 35.79 KHz (1% of the reference) and a ζ of 0.707 (critically damped), τ_2 is found to be (using the quantified values for VCO, PFD and divider gain),

$$\tau_2 = R_2 C = \frac{2\zeta}{\omega_n} - \frac{N}{K_o K_d} = 5.6\ \mu\text{sec}. \qquad Eq.\ 3.32$$

The value for τ_1 is shown to be

$$\tau_1 = R_1 C = \frac{K_o K_d}{N \cdot \omega_n^{\,2}} - \tau_2 = 23.4\ \mu\text{sec}. \qquad Eq.\ 3.33$$

For a filter capacitor value of 0.0001 μF this results in values for R_1 and R_2 of 237 KΩ and 56.2 KΩ respectively (using 1% resistor sizes). The loop filter is implemented off-chip to allow flexibility in adjusting the time constants and because of the excessive chip area required by a 100 pF capacitor.

The quantified loop filter transfer function is

$$K_f \equiv \frac{1 + s(5.6\ \mu\text{sec})}{1 + s(29\ \mu\text{sec})} \left(\frac{volt}{volt}\right). \qquad Eq.\ 3.34$$

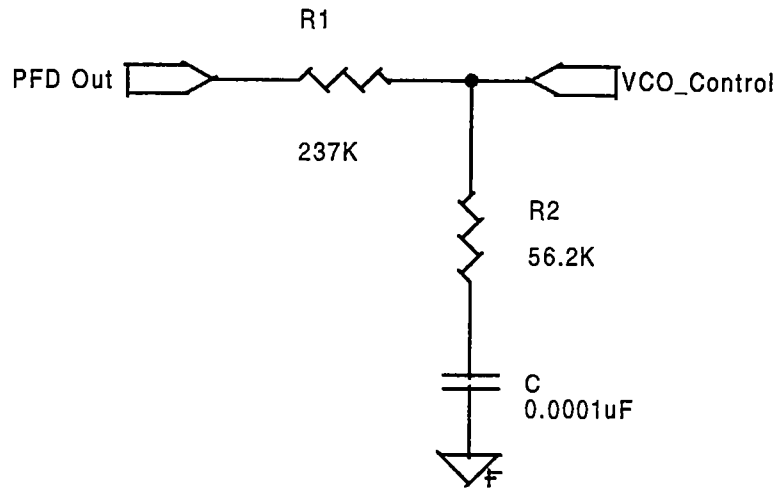


Figure 3.16 - Lag-Lead Loop Filter

3.7 Complete PLL Design

Table 3.1 gives a complete listing of the transfer functions for each component of the PLL. Using these transfer functions, the loop analysis can be performed using Equation 3.7. The resultant magnitude and phase plots are shown in Figure 3.17 and indicate a phase margin of 50° which provides a good margin of stability. The loop filter pole (5.5 KHz) causes the loop gain phase to shift downward but is compensated by the loop filter zero (28.4 kHz).

The closed loop gain vs. frequency is found using Equation 3.8. Figure 3.18 shows the closed loop gain with respect to frequency. The closed loop gain begins to drop off at the PLL natural frequency, ω_n (35.796 KHz). This implies that the PLL can track any phase or frequency modulation of the reference from a range of zero to ω_n which is referred to as the correction bandwidth.

Table 3.1 - PLL Component Transfer Functions

Component	Transfer Function
Voltage Controlled Oscillator	$K_0 = \left(\frac{2\pi \cdot 91 \cdot 10^6 \cdot \frac{rad}{\sec}}{0.4 \cdot volt}\right) \cdot \left(\frac{1}{s}\right)$
Phase Detector	$K_d = \frac{Vdd}{4\pi}\left(\frac{volt}{rad}\right)$
Loop Filter	$K_f \equiv \frac{1+s(5.6\ \mu\sec)}{1+s(29\ \mu\sec)}\left(\frac{volt}{volt}\right)$
Divider	$N \equiv 256$

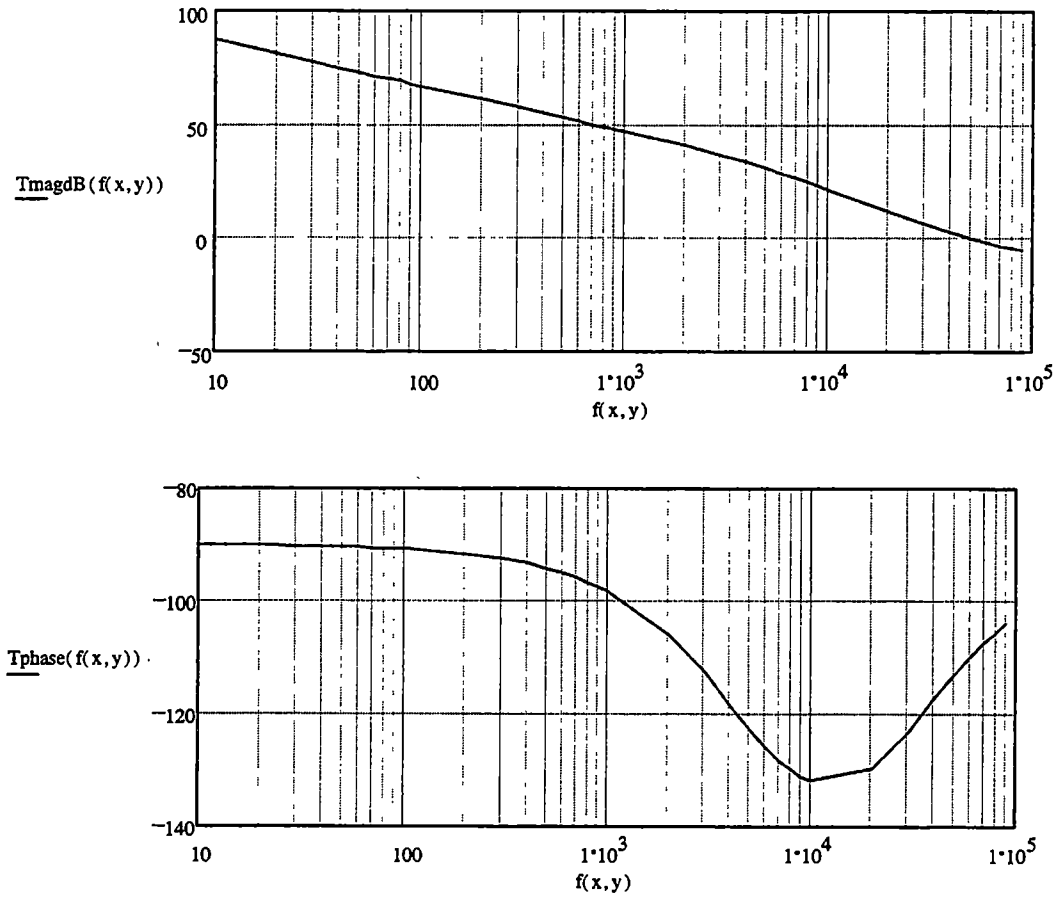


Figure 3.17 - PLL Loop Magnitude and Phase vs. Frequency

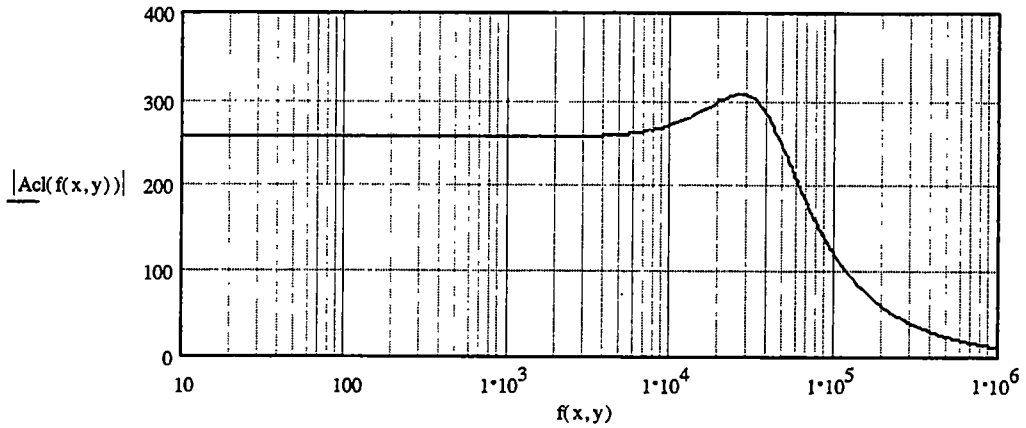


Figure 3.18 - Closed Loop Gain vs. Frequency

3.8 PLL Simulation Results

Simulating a PLL is quite difficult because the necessary lock-in time for the PLL is extremely large compared to the output frequency of 916 MHz. A complete simulation of the PLL from power-up to lock requires a great deal of simulation time and large amount of hardware resources. However, a complete PLL simulation is not required to verify functionality. Instead the PLL is simulated to verify the proper error correcting tendencies. Breaking the PLL at the output of the loop filter and applying a DC voltage at the 'VCO_Control' input, such that the VCO output frequency is above or below 916 MHz, shows the designer if the correction signal (loop filter output) is modulating the 'VCO_Control' input properly. For a VCO output frequency that is higher than 916 MHz the loop filter output should move in a negative voltage direction ,which acts to lower the VCO output frequency, and vice versa. Simulation hardware requirements are further reduced by dividing the VCO output frequency at the extremes of the tuning range (875 MHz and 966 MHz) by 256, and directly inputting these divided frequencies into the

phase detector. Thus the VCO and the divider are not used in the simulation which greatly speeds up processing time. Figure 3.19 shows the loop filter output for both a higher and lower (than carrier frequency) divided VCO output frequency. The input frequency to the phase detector is 3.418 MHz for the low frequency case and 3.773 MHz for the high frequency case. For the lower than reference input frequency the loop filter output is moving higher in voltage which acts to speed up the output frequency of the VCO. For the higher than reference input the loop filter is moving downward in voltage which slows the VCO's output frequency. This indicates that the PLL is correcting for the output frequency properly.

To determine the PLL operating power without running a full lock-in simulation, the loop can be broken and the VCO biased to achieve an output frequency of approximately 916 MHz. This allows the PLL to immediately operate near the desired output frequency and should provide a reasonable operating power measurement. Figure 3.20 shows the power supply current when 'VCO_Control' is 1.65 volts (913 MHz VCO output frequency). The average current is approximately 14 mA which corresponds to a PLL operating power of 46.2 mW.

3.8 Conclusions

A complete PLL system has been designed and implemented using the HP 0.5μ process. Table 3.2 is summary of the PLL's performance parameters. The required layout area for the PLL is approximately 111,887 μm^2. The loop analysis indicates a PLL phase margin of 50° and a correction bandwidth of approximately 35.796 KHz.

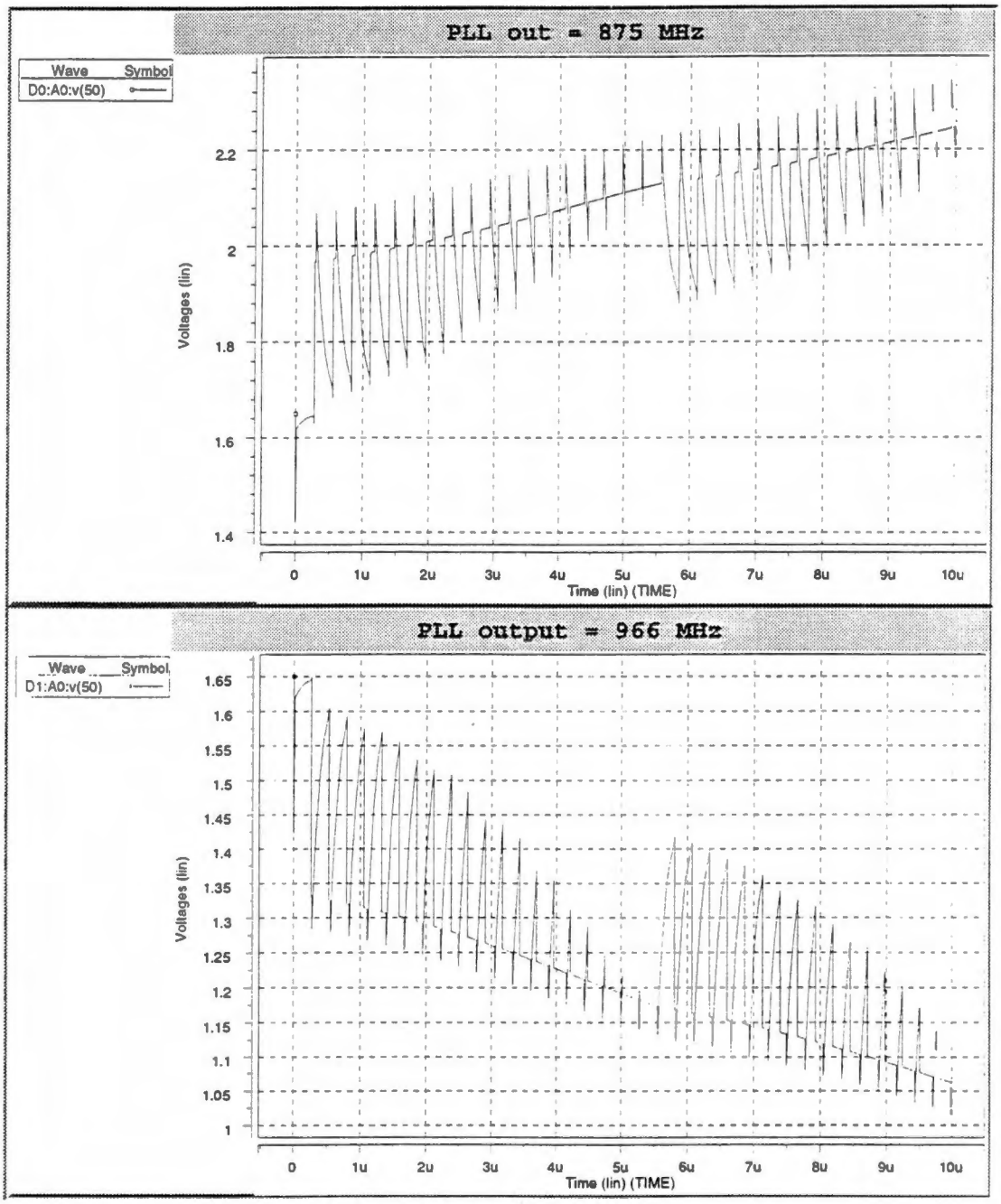


Figure 3.19 - Correction Ability Simulation Results

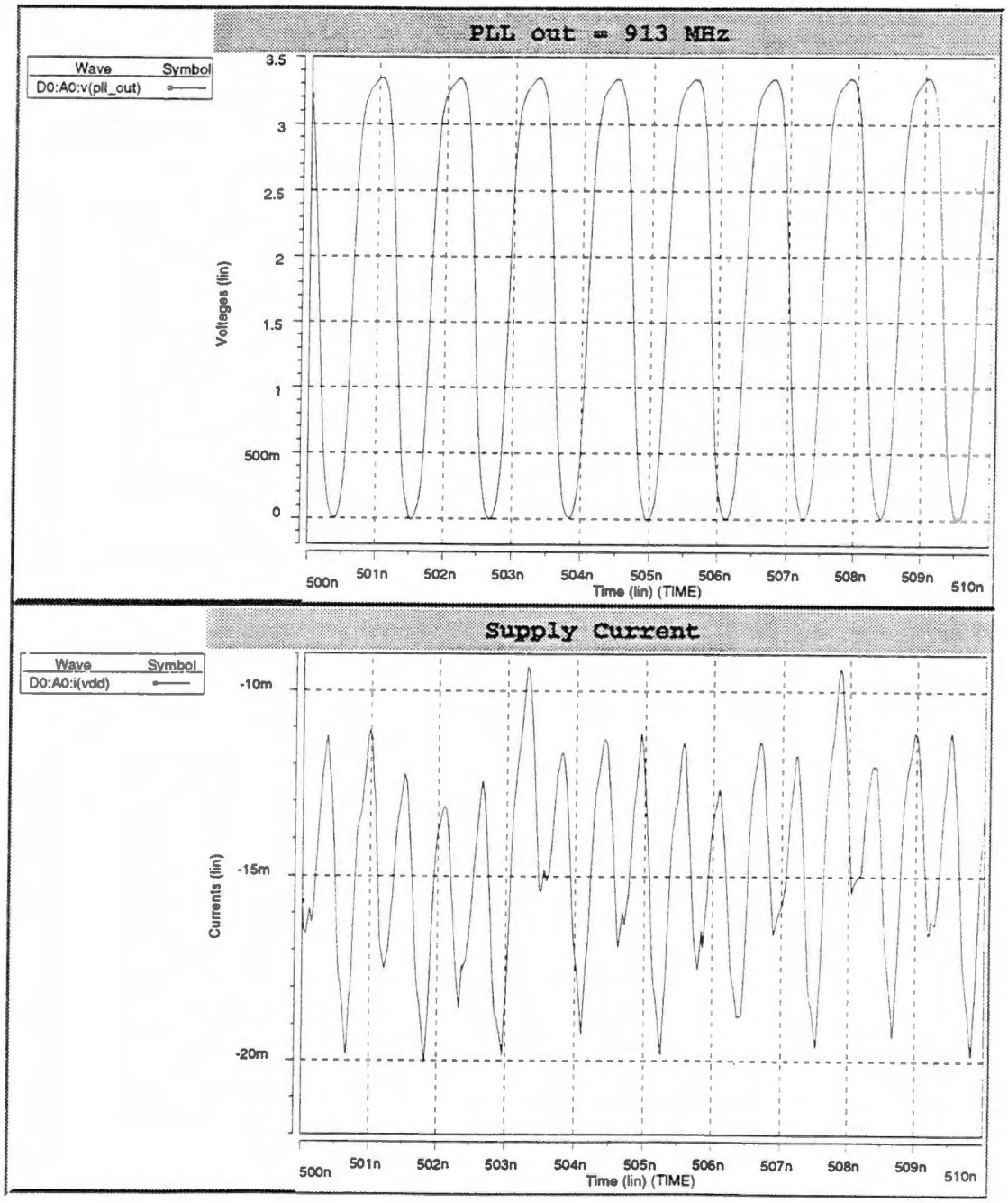


Figure 3.20 - PLL Operating Power

Table 3.2 - PLL Performance Parameter Summary

Parameter	Value
Tuning Range	91 MHz
Lock-in Time	28 μsec
Correction Bandwidth	35.796 KHz
Operating Power (Vdd 3.3 volts)	46.2 mW

PLL simulation results indicate that the PLL is fully functional. The PLL is designed to provide the ability to adjust the tuning range and loop filter critical frequencies if necessary.

Chapter 4

CMOS RF Mixer and Biasing Circuit Design

Mixers are an important component of any wireless communications system. Mixers are used in RF applications to modulate the message signal to the desired carrier frequency, usually much higher than the baseband signal. This modulation to a higher frequency is necessary because of transmission bandwidth restrictions and also for increased range and performance (higher frequencies generally propagate better than lower frequencies through air) [21]. Mixing two signals is synonymous with the multiplication of two signals, thus a mixer is often referred to as a multiplier. Multipliers can be implemented in both analog or digital circuits. At a carrier frequency of 916 MHz, an analog multiplier is often the mixer of choice. Analog multipliers typically have a small number of transistors and can operate at high frequencies if designed properly.

In addition to the mixer, this particular transmitter system requires stable current biasing to maintain optimum performance. This is usually accomplished with a simple current mirror configuration. However, the RF transmitter block is operating on a steadily drooping power supply which mandates a more complex biasing structure that is independent of the supply voltage.

4.1 Mixer Overview

Usually, the output of an analog multiplier circuit is the product of two input signals times some constant. Ideally the mixer output will take the form:

$$Vout = \alpha \cdot V_1 \cdot V_2 , \qquad Eq.\ 4.1$$

where α represents a constant in the multiplication and is controlled by the individual circuit parameters. In RF communications systems, the message signal is multiplied by a (usually) much higher carrier frequency. This process is also termed modulation (mixers are also called modulators). As a result of this modulation process, the message is moved outward in the frequency domain to a higher frequency more suitable for transmission [21]. The frequency shifting property of mixing is better understood when one considers that multiplication in the time domain is analogous to convolution in the frequency domain (see Equation 4.2).

$$Vout(t) = V_1(t) \cdot V_2(t) \quad \Leftrightarrow \quad Vout(j\omega) = V_1(j\omega) * V_2(j\omega) . \qquad Eq\ 4.2$$

Thus, the multiplication of two pure sinusoids produces a result having both the sum and difference frequencies present (see Equation 4.3) [22]. This result can be derived using Euler's identities or by performing convolution in the frequency domain.

$$A_1 \cdot Cos(\omega_1 t) \bullet A_2 \cdot Cos(\omega_2 t) = \left(\frac{A_1 \cdot A_2}{2}\right) \cdot \left(Cos(\omega_1 + \omega_2)t + Cos(\omega_1 - \omega_2)t\right) . \qquad Eq\ 4.3$$

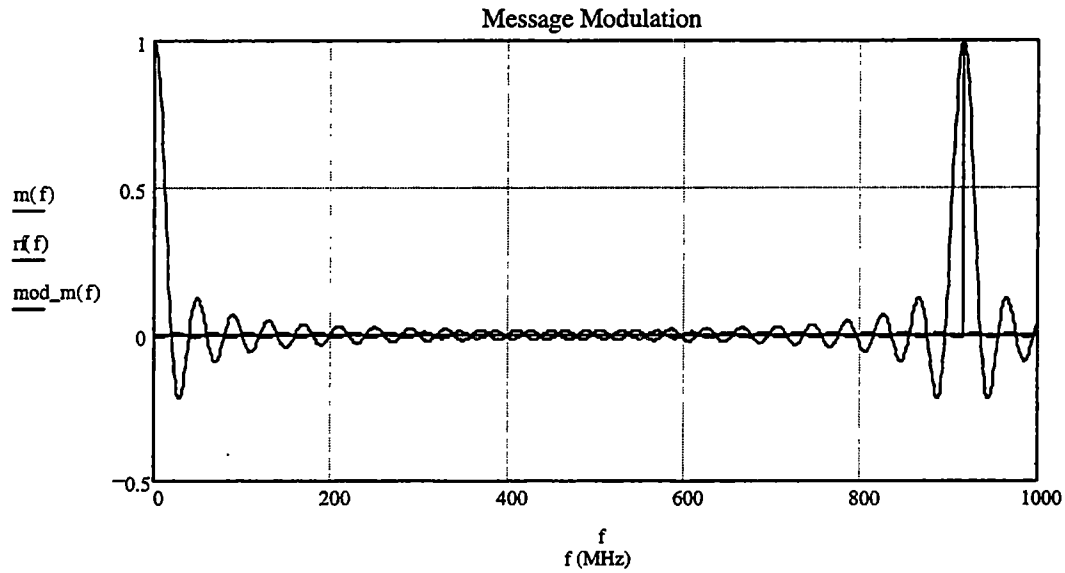


Figure 4.1 - Modulated Spread Data

Similarly, if one multiplies a message signal by the desired carrier frequency (sinusoidal) the message is shifted in the frequency domain as shown in Figure 4.1. Figure 4.1 shows a baseband message signal (represented by a sinc function, m(f)) centered about the origin and a carrier frequency (rf(f)) that is represented by an impulse function located at 916 MHz [2]. Applying Equation 4.2 results in a scaled version of the message signal being centered about the carrier frequency (mod_m(f)).

4.2 Available CMOS Mixer Topologies

Many different analog mixer architectures are available to the designer [23]. Two broad classifications of analog mixers are the single and double balanced mixer. This refers to the mixer's ability to suppress the RF carrier component at the output. The

single balanced mixer provides no carrier suppression while the double-balanced provides almost complete RF carrier rejection at the output [23]. Complete carrier rejection is desirable to maximize the transmitters output efficiency. This is because the carrier frequency contains no useful information to the receiver. Therefore, the double-balanced architecture is employed for this system.

Double-balanced mixers can be implemented using passive or active circuit architectures. Passive topologies include diode mixers and passive CMOS mixers (Figure 4.2) [23]. Although the passive CMOS switching mixer of Figure 4.2 exhibits acceptable performance, a lossy passive network is undesirable for this application because the mixer drives the antenna directly (as opposed to following the mixer with a linear power amplifier) and must therefore be capable of sourcing power to the antenna. The mixer therefore must be an active configuration capable of driving the antenna directly such as the Gilbert-type double-balanced mixer.

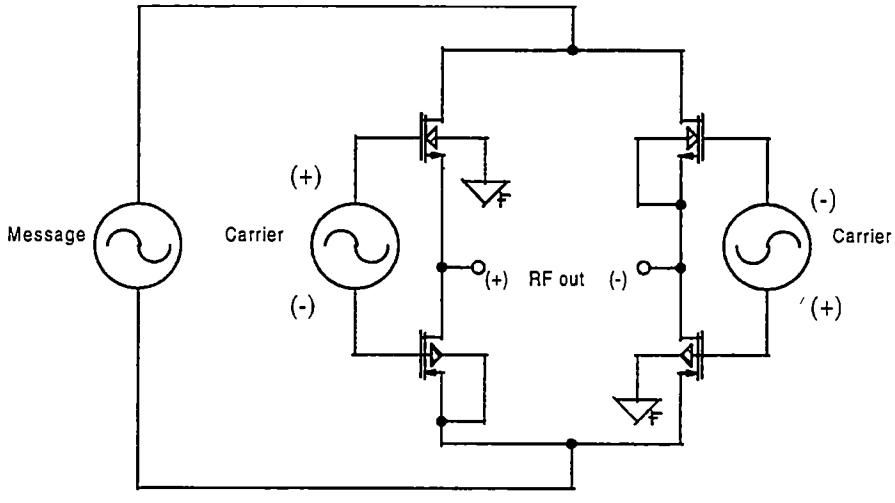


Figure 4.2 - Passive CMOS Mixer

Before examining in detail the operation of the Gilbert Cell mixer, a review of the fundamental design concepts of active CMOS mixers is beneficial.

4.2.1 Basic Active CMOS Mixer

A simplified model of an active CMOS mixer is shown in Figure 4.3 [23]. Here the digital message signal modulates the gate of 'M1' causing the current in the differential pair to be turned on (Message = 3.3 V) or turn off (Message = 0 V). The output current 'Iout' can therefore be represented as

$$I_{out} = \mathrm{sgn}\left(\omega_{Message}t\right)\cdot\left(I_{Carrier}\cdot\cos(\omega_{Carrier}t)\right). \qquad Eq.\ 4.4$$

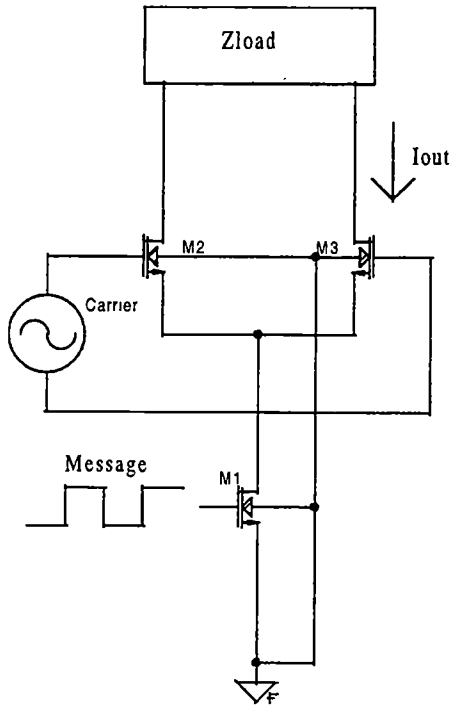


Figure 4.3 - Active CMOS Mixer

As a result the carrier is modulated by a square wave determined by the digital message signal. The output for this type of mixer is a carrier frequency that is keyed on and off. The modulated signal appears as FSK (Frequency Shift Keying) with two distinct output frequencies (916 MHz and 0 Hz). Removal of the square wave harmonics (odd harmonics: 3, 5, 7 ..) associated with this type of modulated waveform can be accomplished using a double-balanced mixer architecture as shown in the following section [23].

4.2.2 CMOS Double Balanced Multiplier (Gilbert Cell)

The Gilbert-type double-balanced mixer is comprised of two single-balanced mixers whose message signal is connected in parallel and carrier frequency signal is anti-parallel [23]. The anti-parallel nature of the carrier is what suppresses its presence from the output. The CMOS Gilbert mixer topology used in this transmitter is shown in Figure 4.4. The mixer functions in the following manner. The differential pair formed by 'M1' and 'M2' is driven by the spread digital data. Because the digital data signal swing is large, one of the transistors ('M1' or 'M2') is turned on and the other is turned off. The current in these transistors ('M1' and 'M2') is mirrored to the differential pairs comprised of transistors 'M7 - M9' and 'M8 - M10' which are driven by the RF carrier signal. As a result of the on-off switching of 'M1' and 'M2' one of the differential pairs driven by the carrier is turned on and the other is turned off. When the digital data changes state, the carrier driven differential pair that was on is now turned off and the differential pair that was off is now on. Because the output of these two differential pairs are connected in an anti-parallel fashion, the output signal changes phase by 180°.

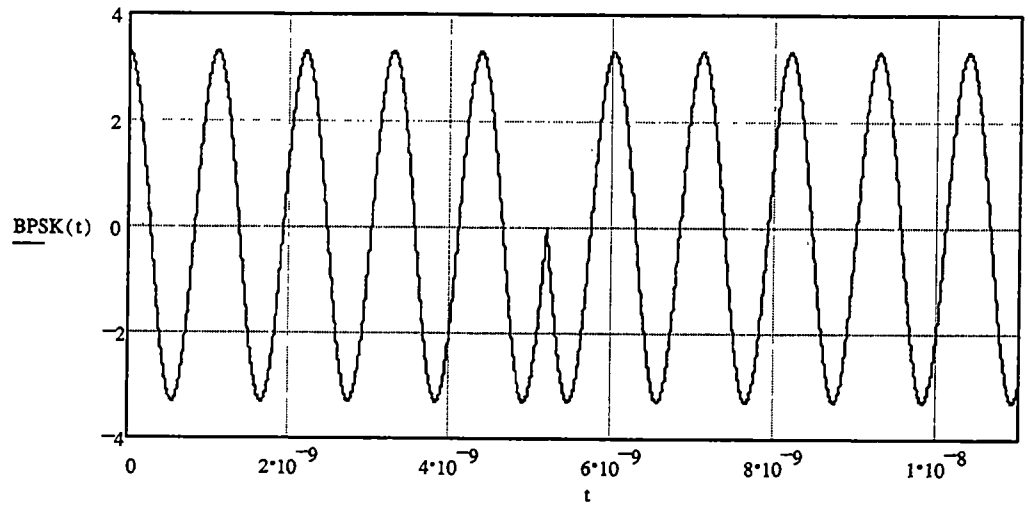
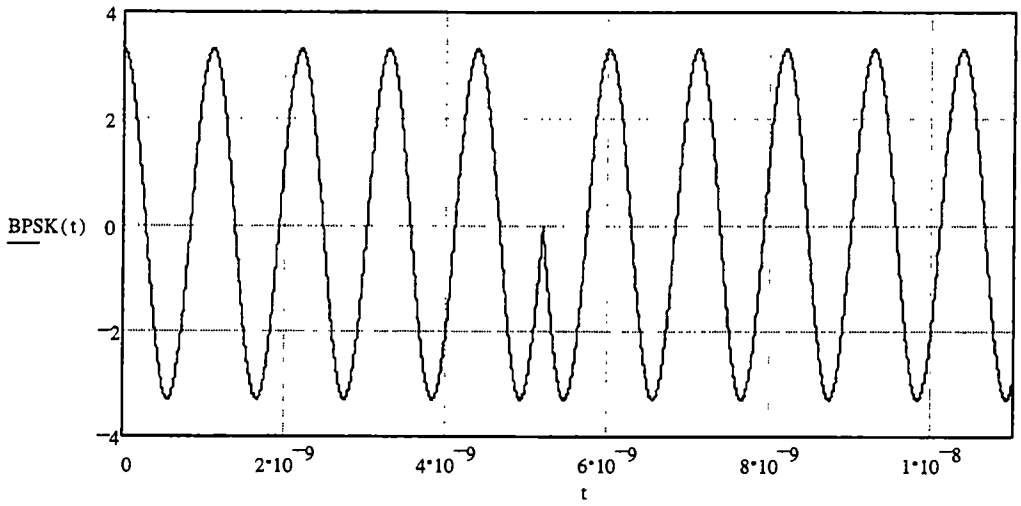


Figure 4.5 - Ideal BPSK Output From Mixer

necessary to provide enabling and disabling capabilities. The device sizes shown are the actual sizes used in the circuit layout.

4.3.1 Design Considerations / Analysis

Since this mixer is used as a BPSK modulator, a small signal analytic expression for the two inputs (carrier and message) to output is unnecessary. Instead, the output of the mixer is represented ideally as the carrier frequency multiplied by a digital data signal with amplitude of +/- 1 times a constant attenuation factor determined by circuit parameters. Another design consideration for this mixer is the time required for a complete phase shift of the output carrier signal upon a change in state of the digital input signal. This response time is a result of the time required for a change in digital input state at the gates of 'M1' and 'M2' to result in a change in the carrier signal's phase at the



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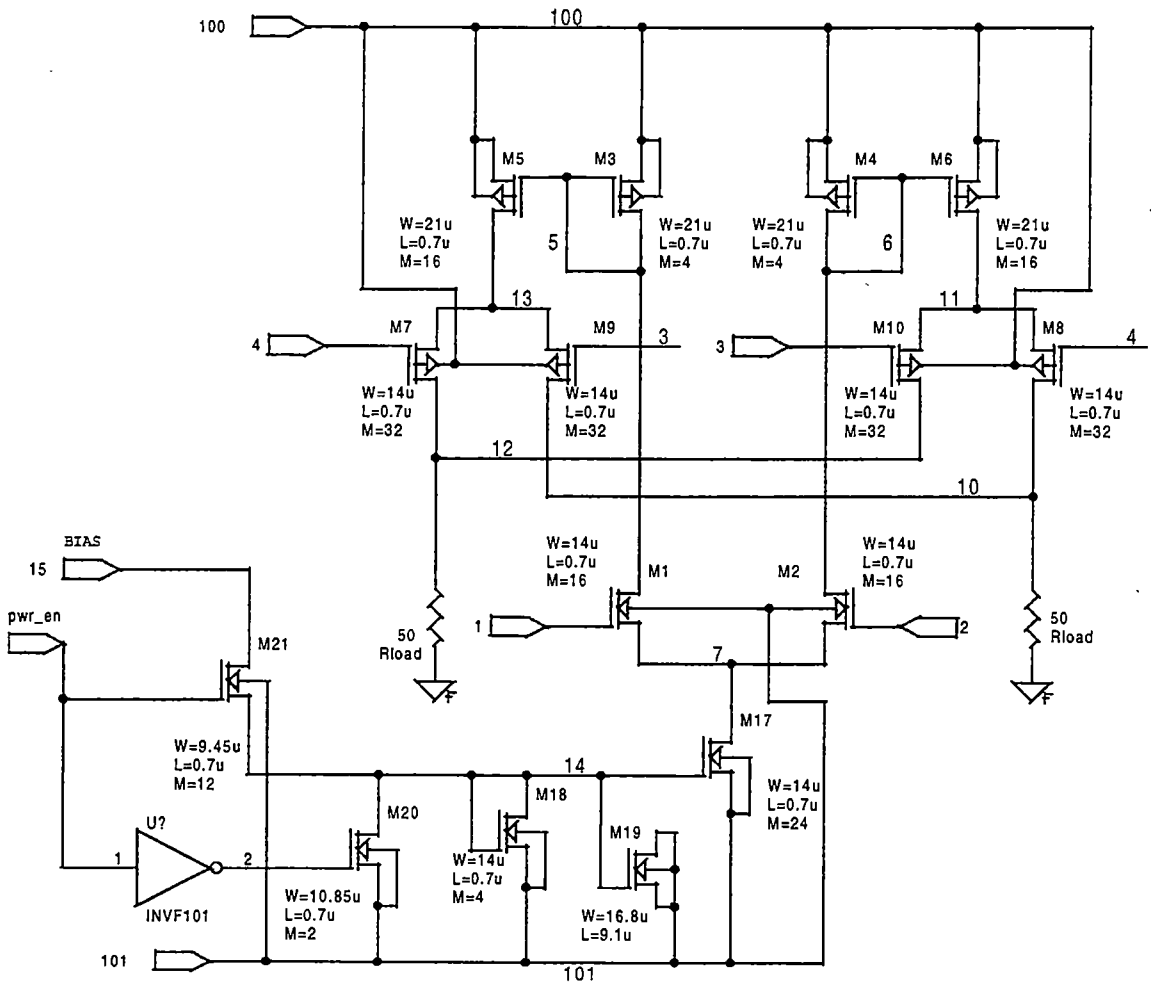

Figure 4.6 - Transmitter System Mixer Schematic

output. As a result, the designer must analyze the mixer to find the total signal path delay (digital input to carrier output) to ensure sufficient phase response time for this application. The maximum allowable phase shift settling time is determined by the receiver and is estimated to be 10 % of the maximum digital data rate (894.9 kHz) which corresponds to 110 nsec. Because of the large signal non-linear switching nature of the mixer a small signal approach yields a highly approximate representation of the time required for a complete phase shift and thus, the phase shift settling time is determined from circuit simulations.

4.3.2 Mixer Simulation Results

When simulating the mixer for this application, consideration must be given to how the carrier signal inputs are driven. A differential signal is achieved for the digital data input pair ('M1' and 'M2') by placing an inverter between the gates (see Figure 4.4). Differential drive for the 916 MHz carrier frequency inputs ('M7'-'M9' and 'M8'-'M10') however, presents significant design challenges. The carrier frequency signal is generated by the PLL and is inherently single ended. To further complicate matters, the output of the PLL cannot be simply inverted using a digital gate to achieve differential drive because the inverter delay is significant compared to the period of the 916 MHz carrier signal. One solution has one side of the 916 MHz input pair tied to the VCO output and the other side tied to a voltage that is the DC average of the carrier signal. Another carrier driving implementation uses a phase splitting circuit (see Figure 4.7) whose outputs are ideally 180° out of phase with one another [25]. The phase splitting circuit adds complexity to the system but offers performance advantages by providing a more

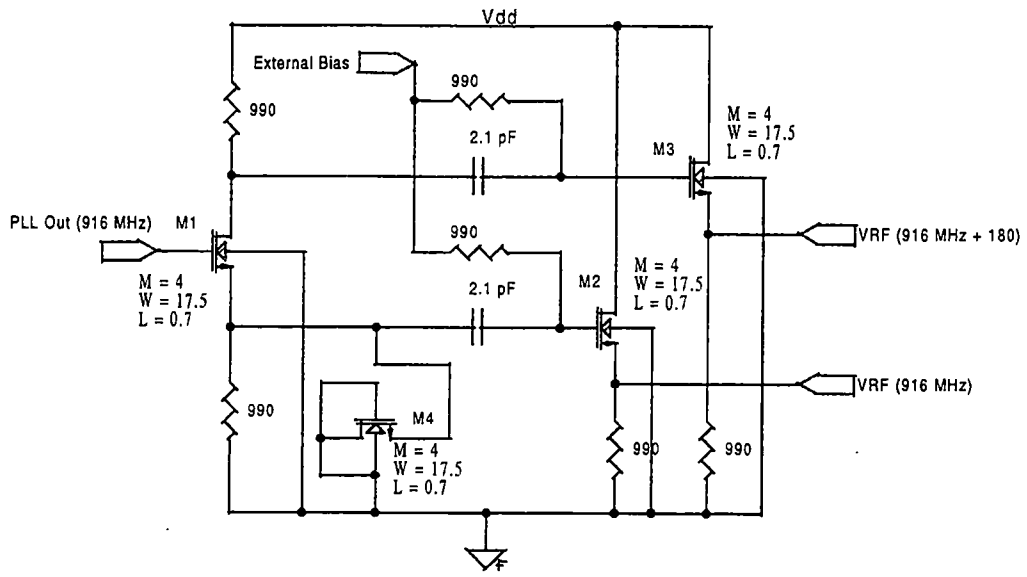

Figure 4.7 - Phase Splitting Network

balanced drive of the carrier frequency inputs. The phase splitting network of Figure 4.7 only works if the 3-dB frequencies of each output transfer function are well above the carrier frequency. Both approaches are implemented on the chip by having two complete transmitter systems, one with a direct single-ended drive from the VCO and another incorporating the phase splitting network

The mixer shown in Figure 4.6 is simulated with each type of carrier frequency driving network. All simulation list files are shown in Appendix 2. For the single-ended drive simulation, the output driver of the VCO is used to drive node 4 while node 3 is tied to 1.65 volts. The single-ended driving configuration required a bias current in 'M18' of 1 mA to achieve a satisfactory output signal. Lower bias currents resulted in poor phase alignment at both outputs of the mixer (nodes 10 and 12). Ideally nodes 10 and 12 should

be 180° out of phase with each other, but at low bias currents (less than 1 mA) the outputs were approximately 90° out of phase. Figure 4.8 shows the mixer output (nodes 10 and 12 in Figure 4.6) for the single ended drive configuration before and after a change in data state. The mixer output nodes are still only 135° out of phase which is undesirable. This is likely due to finite switching time of the carrier input differential pairs ('M7', 'M9' and 'M8', 'M10') at 916 MHz. Figure 4.8 also reveals an amplitude imbalance at nodes 10 and 12, however this is canceled out when the output is taken differentially as for this application. Figure 4.9 shows the response time of the single-ended drive configuration after a change in input digital data. The settling time for the output is approximately 2.5 nsec which is more than sufficient. Unfortunately the phase imbalance was discovered after the chip had been fabricated. Resultantly, the modulated signal at the output of the mixer is anticipated to have mediocre performance.

To simulate the differential drive network, the VCO output buffer is used to drive the phase-splitting network of Figure 4.7. This helps to achieve accurate loading at the mixer's carrier frequency inputs. The bias current in 'M18' is 100 μA for the differentially driven configuration. Figure 4.10 shows the mixer's output (nodes 10 and 12) before and after a change in digital input states. The differential drive network provides good phase balance at the output at the cost of a smaller signal swing (200 mV vs. 1 V). The reduction in signal level is primarily a result of the decreased current bias level in addition to the attenuation of the VCO output incurred by the phase-splitting network. A reduction in signal swing is inconsequential (within reason) for this application because the transmission distance is small (8 ft.).

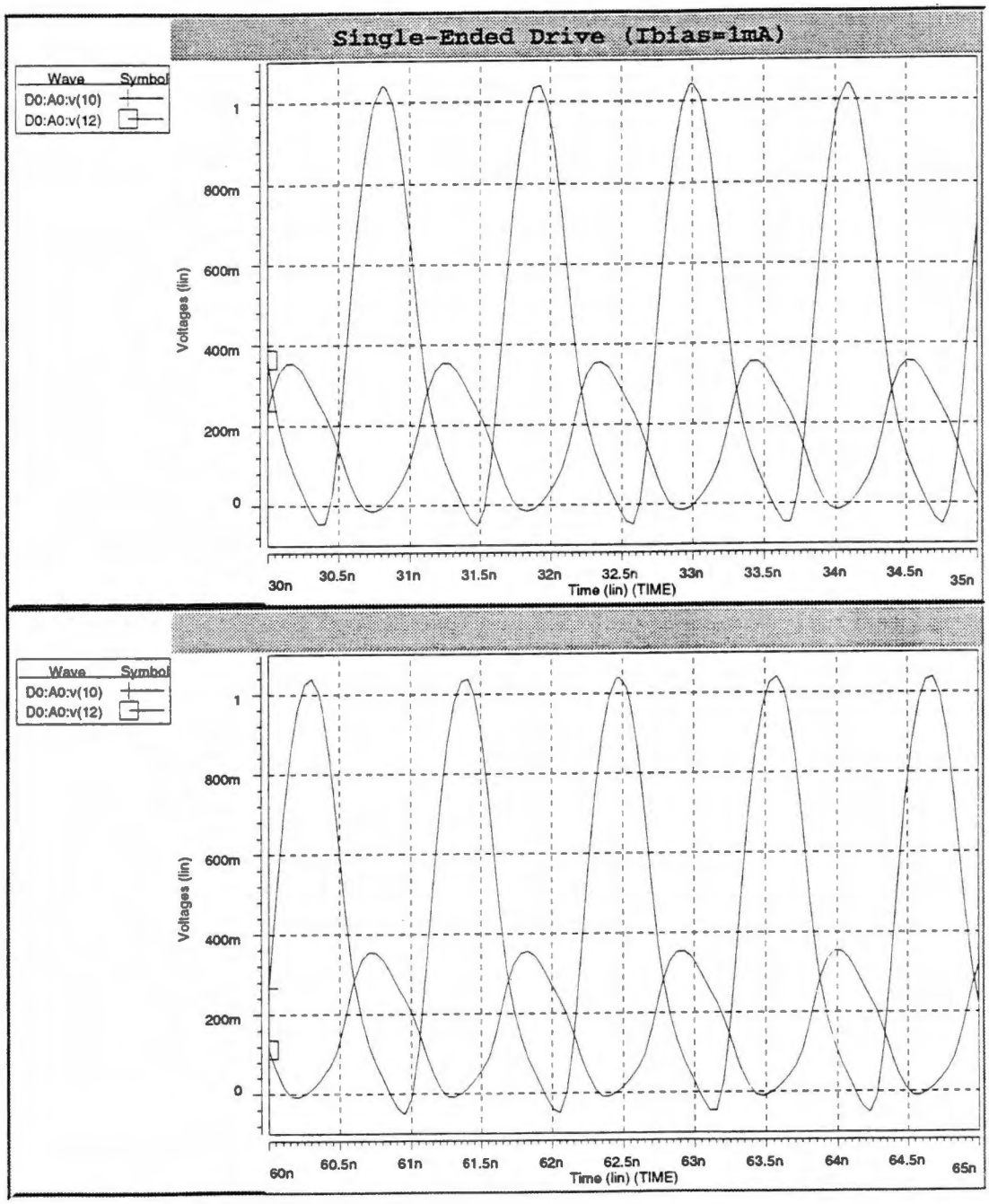

Figure 4.8 - Single-Ended Drive Simulation Results

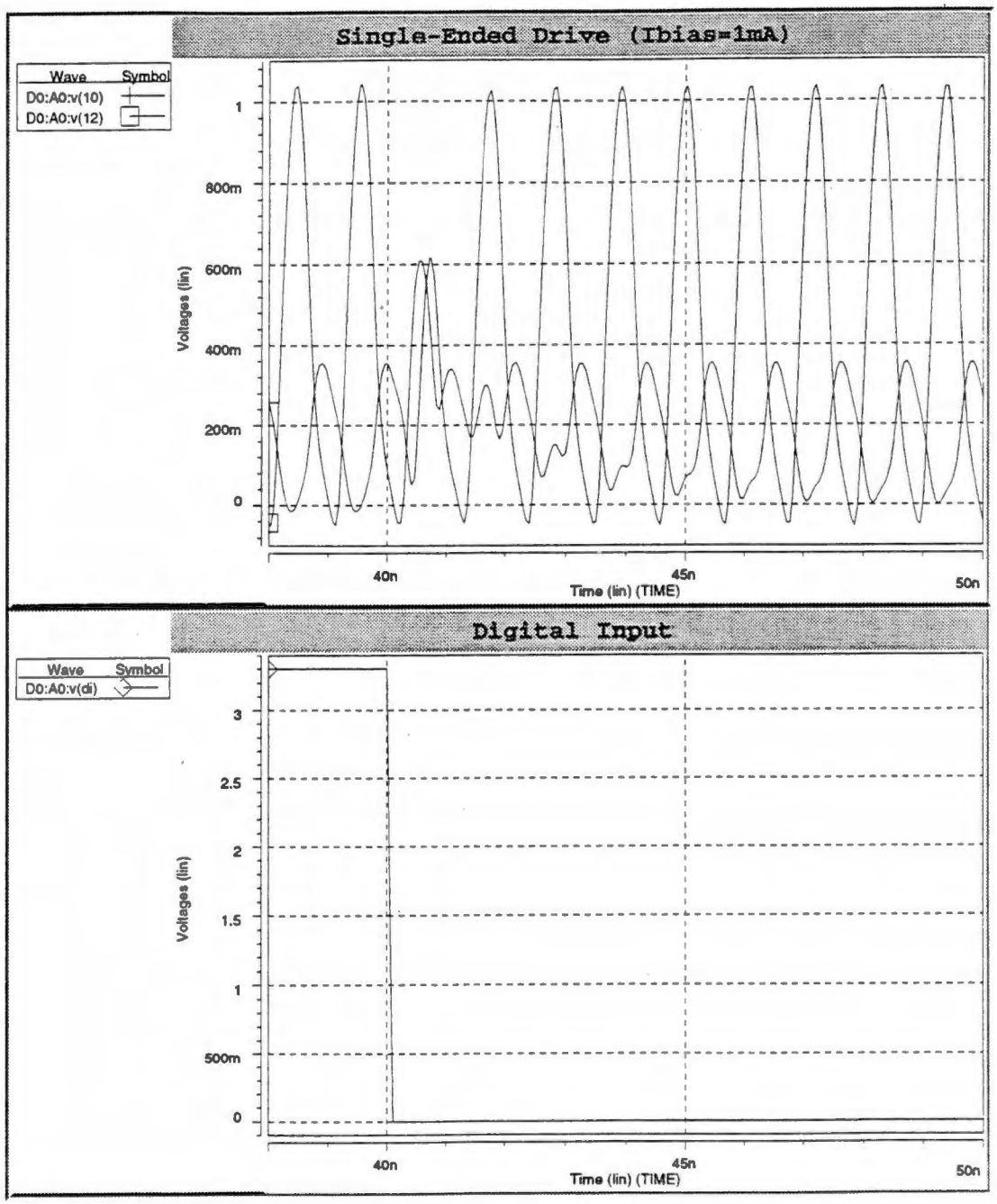

Figure 4.9 - Single-Ended Drive Output Response Time

In contrast, the reduction in bias current allowed by the differential driving network results in greatly reduced power consumption by the mixer which is very desirable for this application. Figure 4.11 shows the mixer output response time for a change in digital input state to be 2.5 nsec which is similar to that of the single-ended driving configuration.

Table 4.1 is a summary of mixer performance for each type of driving network. The differential driving network appears to be the most favorable for the application. Both implementations have been incorporated on a single chip to characterize the performance of each. The differential drive simulations rely heavily on the process models used by the simulator. If these models are inaccurate at high frequency (as previous projects have indicated), the actual performance of the differential drive configuration could suffer significantly.

Table 4.1 - Mixer Performance Summary

Performance Parameter	Single-Ended Drive	Differential Drive
Output Power (50 Ω load)	10 dBm	-3.9 dBm
Bias Current	1 mA	100 μA
Power Consumption	96.5 mW	37.7 mW
Output Settling Time	2.5 nsec	2.5 nsec

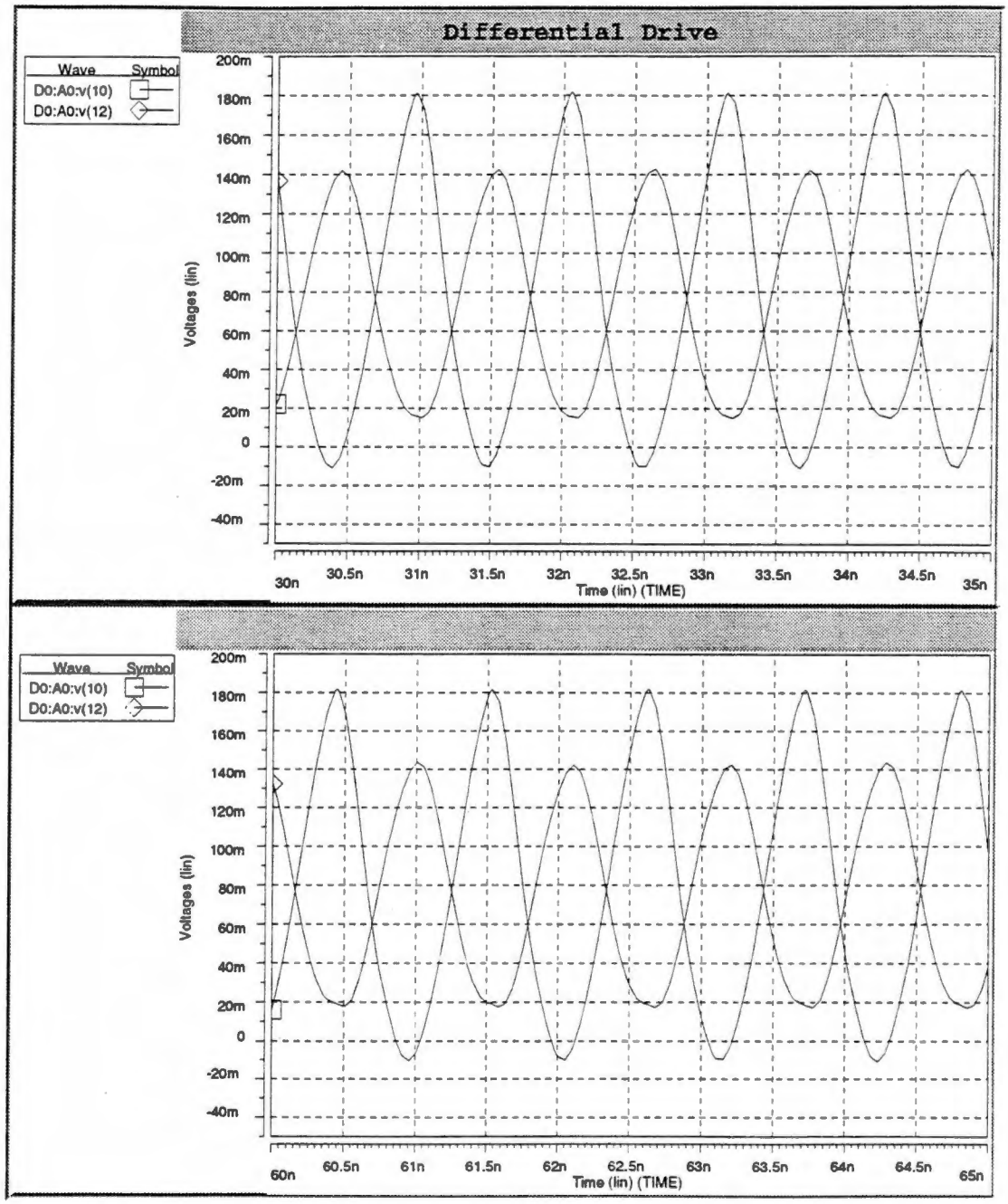

Figure 4.10 - Differential Drive Simulation Results

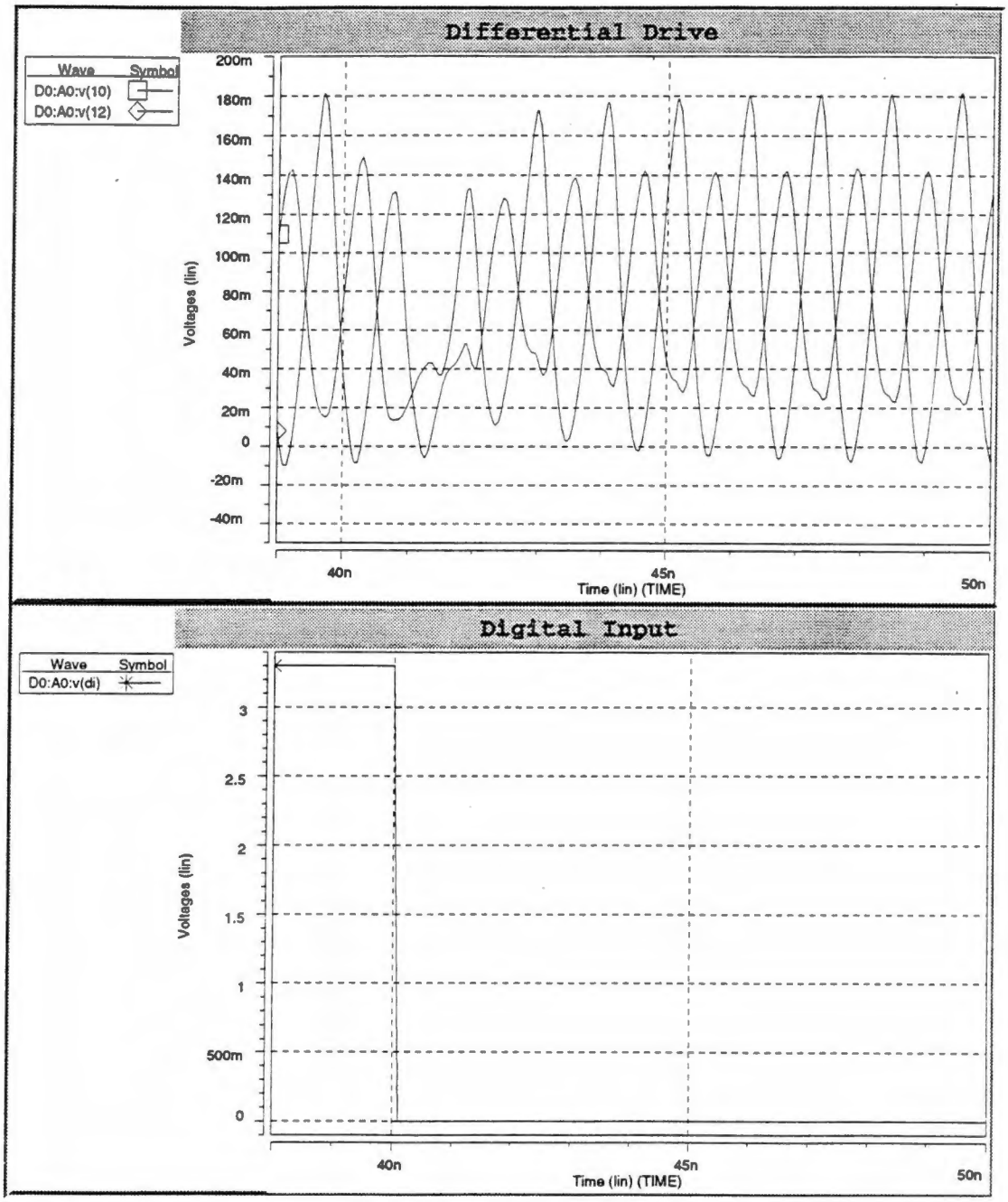

Figure 4.11 - Differential Drive Output Response Time

4.4 Supply Independent Current Biasing Cell

The last circuit in the RF transmitter system to be discussed is the supply independent current bias cell. This circuit is not implemented in this chip run but will be included in the next design cycle. The necessity of supply independent biasing for this application arises from the fact that the inductive power coupling to the chip cannot instantaneously supply the required power for transmission [1]. This results in a continuous decrease of the power supply while the transmitter is running. Without power supply rejection, the mixer and VCO circuit performance could suffer from variations in their respective bias points. This type of dynamic variation in bias should be avoided as much as possible.

4.5 Differing Topologies for Bias Regulation

There are many different methods of providing power supply independent biasing. One of the most common methods uses a bandgap voltage reference and other circuitry that uses the reference to supply a desired voltage or current output reference. Another less common independent bias reference method uses a self biasing feedback loop. Each of these methods has associated strengths and weaknesses. Bandgap references typically require more circuitry than do the self biasing networks. This can lead to decreased voltage compliance which is a disadvantage for designs where the power supply is sagging. The self biasing network is actually quite simple in its operation, but does require some extra startup circuitry as will be shown later.

4.5.1 Bandgap Reference

Bandgap references are a commonly used method of providing a reliable voltage reference. A bandgap reference is created by summing together a base-emitter junction voltage and a PTAT (proportional to absolute temperature voltage) [26]. Using this method, a voltage reference which is to a first order independent of temperature or bias voltage can be constructed. A typical CMOS implementation of a bandgap circuit is shown in Figure 4.12 [27]. The bandgap circuit works as follows. Transistors 'M1', 'M2' and 'M3' form a current mirror configuration which causes the current in 'Q2' to be N plus 1 times the current in 'Q1'. The current in 'I' is found by summing the base-emitter voltage of 'Q1' and the voltage across 'R1' and equating this to the base-emitter

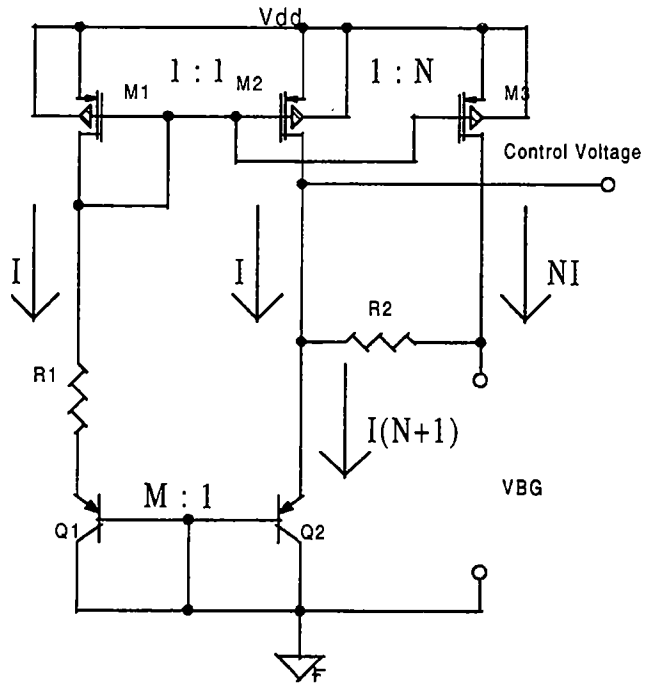

Figure 4.12 - CMOS Compatible Bandgap Reference

voltage of 'Q2'. It is important to note that the emitter voltage of 'Q2' ('Control Voltage') is controlled by a circuit (see reference for details) which keeps the drain voltage of 'M1' and 'M2' equal. 'I' is found to be

$$I = \frac{V_{BE2} - V_{BE1}}{R1} = \frac{1}{R!} \cdot \ln\left[M(N+1)\right] \cdot V_t , \qquad Eq.\ 4.5$$

where

$$V_t = \frac{KT}{q} \approx 26.mV \left(T = 300\ K^o\right). \qquad Eq.\ 4.6$$

The resultant output voltage, 'VBG', is determined by summing the base-emitter voltage of 'Q2' and the voltage across 'R2' and is shown to be [27]

$$VBG = V_{BE2} + N\frac{R2}{R1} \cdot \ln\left[M(N+1)\right] \cdot V_t . \qquad Eq.\ 4.7$$

Equation 4.7 satisfies the requirements for a bandgap circuit. 'Q2' provides the base-emitter junction voltage and the current in 'M3' multiplied by 'R2' provides the PTAT voltage. The base-emitter junction of 'Q2' has a temperature coefficient of -2.2 mV/°C (at 25 °C). A 'VBG" temperature coefficient of approximately zero (at 25 °C) is obtained by setting the values of 'R1', 'R2', 'M' and 'N' such that the second term in Equation 4.7 has a temperature coefficient of approximately +2.2 mV/°C [27]. In addition to temperature compensation Equation 4.7 also indicates that 'VBG' is independent of the supply voltage.

The mixer and VCO require current biasing which is achieved by adding circuitry to the bandgap reference like that shown in Figure 4.13. In this circuit the bandgap reference is buffered using an op-amp whose output voltage controls the current flowing

in 'Rbias'. This current is mirrored form 'M1' to 'M2' which sets the current in 'M3'. Bias currents are obtained by mirroring the gate voltage of 'M1' or 'M2' to the bias transistors of the mixer and VCO. Two disadvantages of using this type of circuit are the increased complexity due to the addition of the op-amp and reduced compliance voltage as a result of the voltage drop across 'Rbias' and the required gate-source voltage of 'M1'. A reduction in compliance voltage is extremely costly for this application because the supply voltage is continuously dropping.

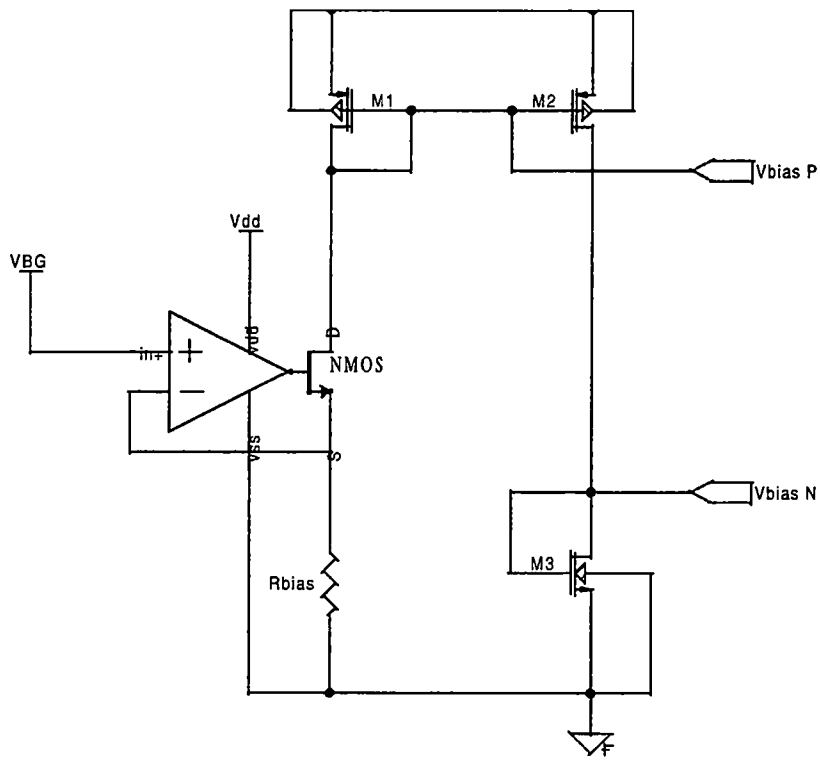

Figure 4.13 - Band Gap Output Current Biasing Scheme

4.5.2 Self-Biasing Feedback Loop

The self-biasing feedback circuit shown in Figure 4.14 shares some similarities with the bandgap circuit of Figure 4.12 [26]. Transistors 'M2' and 'M3' cause the current in each side of the circuit to be the same nominally. This acts as the feedback mechanism. The gate-source voltage of 'M1' sets the voltage across 'R1' which also controls the current. These conditions yield two separate expressions for the current through each side of the circuit. The current mirror gives the expression

$$I_3 = I_2 \,. \qquad Eq.\ 4.8$$

Assuming strong inversion the relationship between the gate-source voltage of 'M1' and the current through 'R1' yields the expression

$$I_3 = \frac{V_{GS1}}{R_1} = \frac{\left(\sqrt{\frac{2 \cdot I_2 \cdot L_1}{K_N \cdot W_1}} + V_{tN}\right)}{R_1}. \qquad Eq.\ 4.9$$

The bias point of the circuit is obtained by plotting Equations 4.13 and 4.14 on the same graph for a range of I_2 values. The intersection point of the two curves is the steady state bias current of the circuit. Using the transistor sizing shown in Figure 4.14 and a value for 'R1' of 88.7 KΩ, Figure 4.15 shows a resulting bias current of 10 μA (see Appendix 1 for transistor parameters). Bias currents for the VCO and mixer are obtained by mirroring the gate voltage of 'M3' or 'M4' depending on the current configuration.

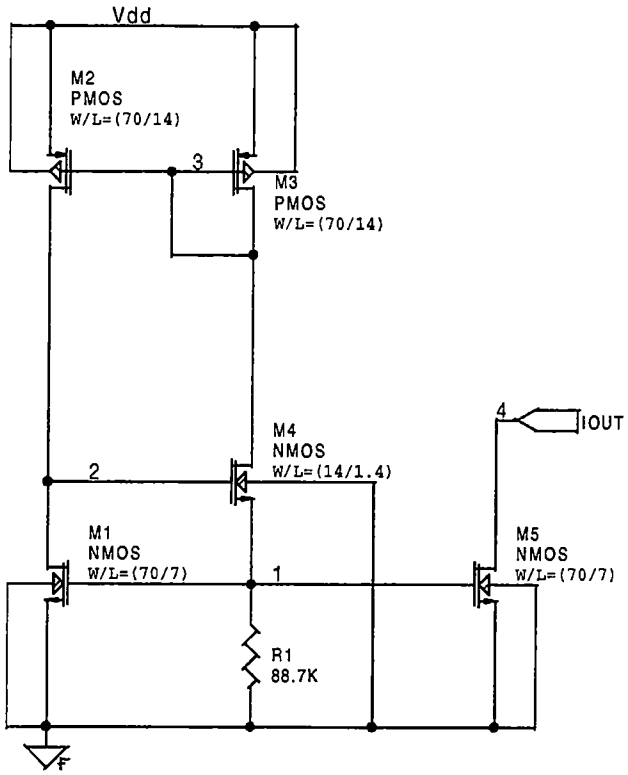

Figure 4.14 - Self-Biasing Feedback Circuit

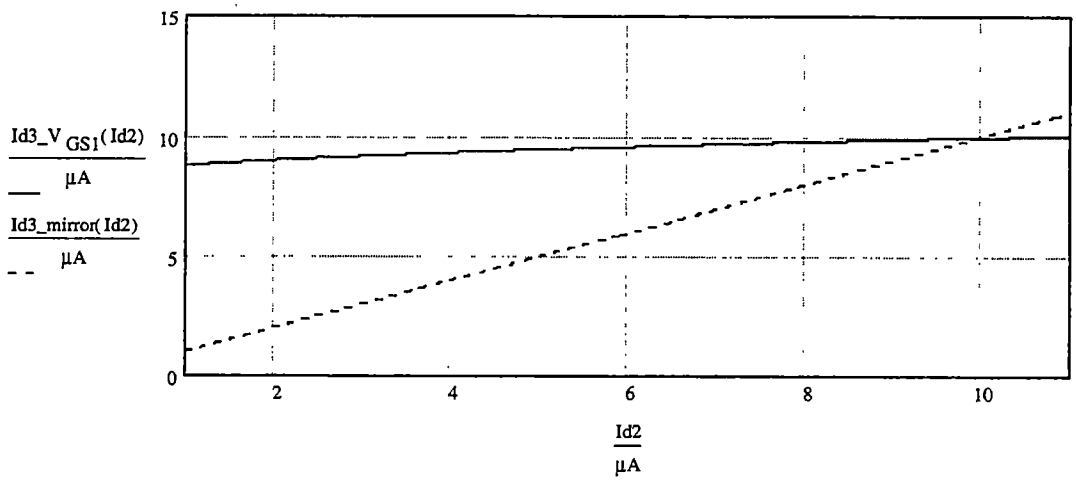

Figure 4.15 - Bias Point Determination Plot

There are actually two values of bias current which the circuit of Figure 4.14 . The first potential operating point is the desired bias current determined by Equations 4.13 and 4.14. The second undesirable operating point is zero quiescent current [26]. This mandates the need for some additional startup circuitry that will ensure that the circuit is not allowed to operate in a zero current mode. One particular startup circuit for this type of bias scheme is shown in Figure 4.16.

When the circuit of Figure 4.16 is initially powered up or reset, the PMOS device 'M6' is turned on and the voltage at the resistive divider is chosen to give the approximate voltage needed at node '2' for proper operation. After some time, determined by the charging rate of 'C1' through 'R4', the voltage at node 6 is sufficient to turn off 'M6' (assumes 'Vdd' to comes up faster than 'R4'-'C1' time constant). The resulting voltage at node 5 is close to zero if 'R2' and 'R3' are small compared to the off resistance of 'M6'. This reverse biases the diode so that the startup circuit has no effect on the bias circuit after the correct bias point has been reached. The diode for this circuit is comprised of a P-type diffusion in an N-type well. This actually results in a parasitic PNP BJT (Bipolar Junction Transistor) with the collector tied to ground. This is not an ideal configuration because node 2 is driven by the base of a transistor but should work at low current levels. Once 'M6' is turned off, the transistor has a virtual short from base to emitter and will not dissipate any appreciable current. This circuit is not yet fabricated, therefore the functionality of the startup circuit in Figure 4.16 is yet to be established.

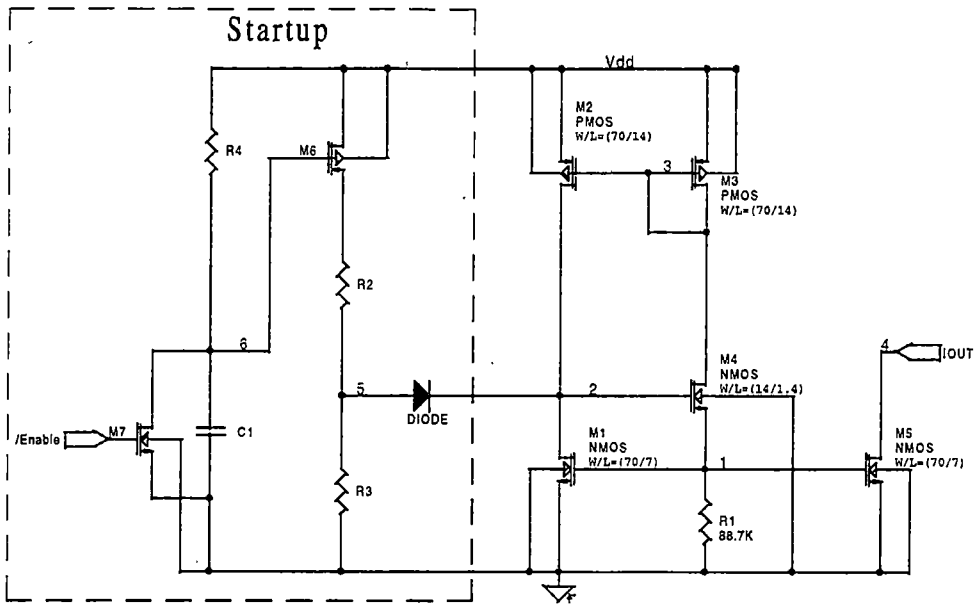

Figure 4.16 - Bias Control Startup Circuit

4.6 Simulation Results / Performance

Simulations of the bias circuit in Figure 4.14 are performed using an 'R1' value of 88.7 KΩ. To determine the bias circuit's independence from fluctuations in the supply voltage ('Vdd'), the simulations ramped the supply voltage from 3.3 volts to 2.3 volts (Appendix 2). The resulting change in the channel current of 'M5' represents the circuits supply voltage independence. The simulation results shown in Figure 4.17 indicate the bias current changes only 0.55 μA (11.525 μA to 10.95 μA) for a 0.86 volt change in supply voltage. This is equivalent to a 4.77% error in output current over a supply voltage range of 3.3 to 2.44 volts. The current drops off drastically as the supply voltage drops below 2.44 volts because there is no longer sufficient voltage to bias the gate to

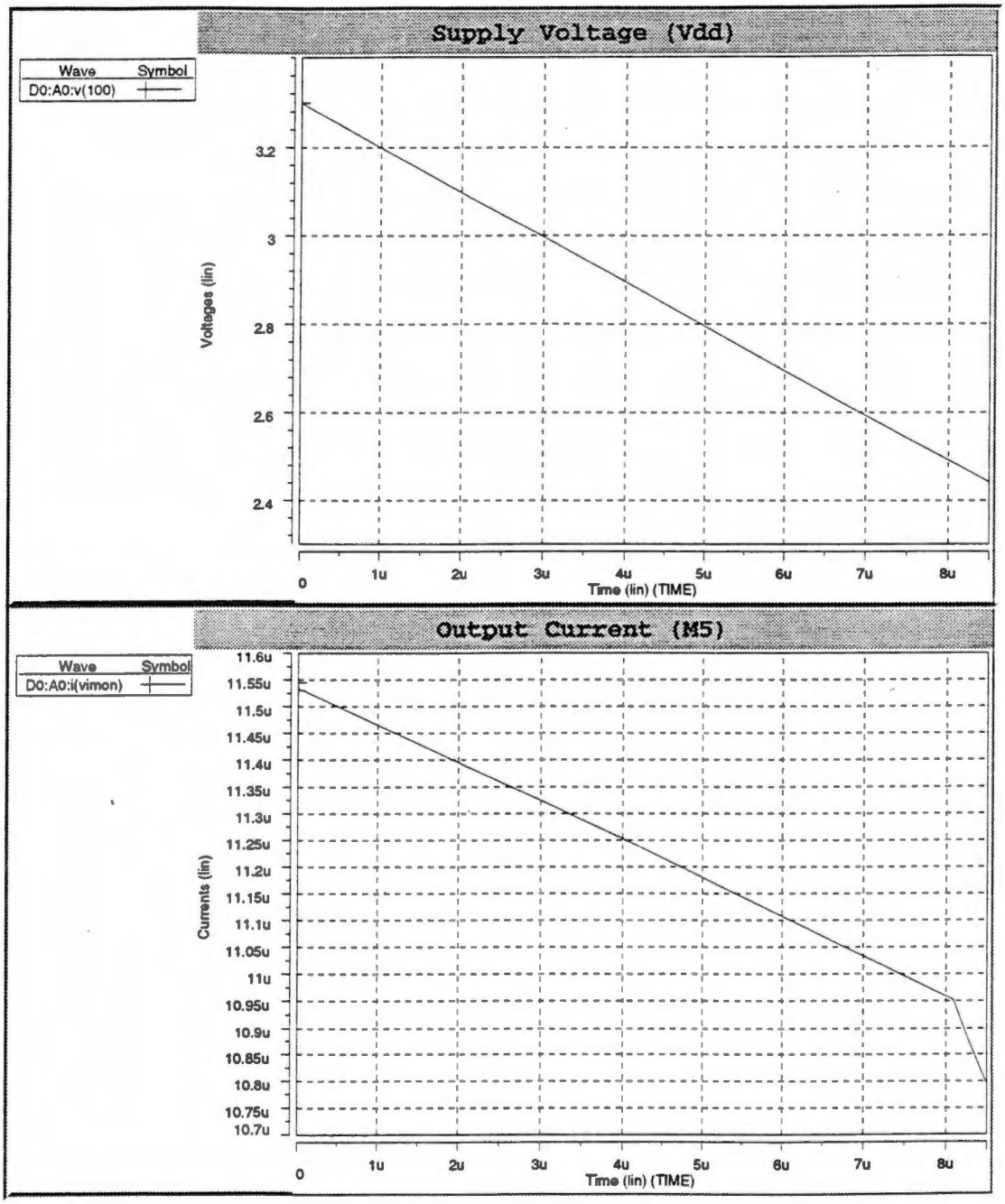

Figure 4.17 - Supply Independent Bias Circuit Simulation Results

source voltage of 'M3' and 'M1' in addition to the V_{Dsat} voltage of 'M4'. The resulting minimum operational supply voltage is 2.44 V.

4.7 Conclusions

A CMOS mixer has been designed and implemented using the HP 0.5μ process. Two different driving configurations for the 916 MHz carrier frequency input are implemented on chip. Simulation results indicate that the differential driving network of Figure 4.7 yield better performance than does the single-ended driving network. The mixer uses 45,330 μm^2 of chip area.

A supply independent current biasing scheme was designed and simulated based on the available process models. Initial simulations indicate that the achieved power supply rejection is acceptable. This bias network will be incorporated in the next design cycle.

Chapter 5

Transmitter System Evaluation

A 916 MHz CMOS RF transmitter has been designed, laid out and fabricated in the HP 0.5μm process. This chapter details the experimental results from the chip testing. The chip has two complete, nearly identical, transmitters. The difference being one has a single-ended mixer drive and the other uses a phase splitting network (shown in Figure 4.7) to drive the mixer carrier frequency inputs. The chip, named moustx1, is intended for testing and characterization purposes. Resultantly, testing is focused on determining each transmitter's functionality and potential methods of improving performance in the next design cycle. Characterization of each individual block within the transmitter system is performed wherever possible, and then the entire transmitter is tested as a system.

5.1 Test Setup and Measurement Techniques

Circuit testing at high frequencies is quite challenging, requiring special equipment and a properly designed test fixture to be performed accurately. The test board constructed for this chip is shown in Figure 5.1. Care was taken to avoid noise coupling

between traces and to provide sufficient power supply filtering. All power supply traces going to the chip were filtered with a ferrite bead in series and a capacitor shunt to ground to minimize noise coupling into the supply rails. Fifty ohm stripline traces were implemented at the mixer outputs to provide impedance matching to the mixer output load resistors which are 49.9 Ω. The chip itself is packaged in a 44-pin J-lead package. The test board provides the capability of attaching an antenna across the mixer's differential output in addition to extra solder pads for impedance matching components required by the antenna. Because the matching network for the antenna was unavailable at the time of testing, the transmitter's output was AC coupled to the spectrum analyzer for analysis.

All low frequency measurements (below 200 MHz) were performed using a Hewlett Packard 5385a frequency counter for precise measurements and a Tektronix TDS 360 digitizing oscilloscope for waveform analysis. High frequency signals (916 MHz) were measured using a Tektronix 494P programmable spectrum analyzer (for frequency domain analysis) and a Tektronix 7104 1 GHz analog oscilloscope (waveform display). The spectrum analyzer was used to measure the spectral content of the transmitter output, while the 1 GHz oscilloscope allowed the designer to look at the output and diagnose problems from a time domain perspective. A Hewlett Packard 899441A vector signal analyzer was used to receive and demodulate the transmitter's output signal. The vector signal analyzer provided a complete system test from input data to demodulated output data. Robust, correct data demodulation by the vector signal analyzer verifies the transmitter's functionality as a system.

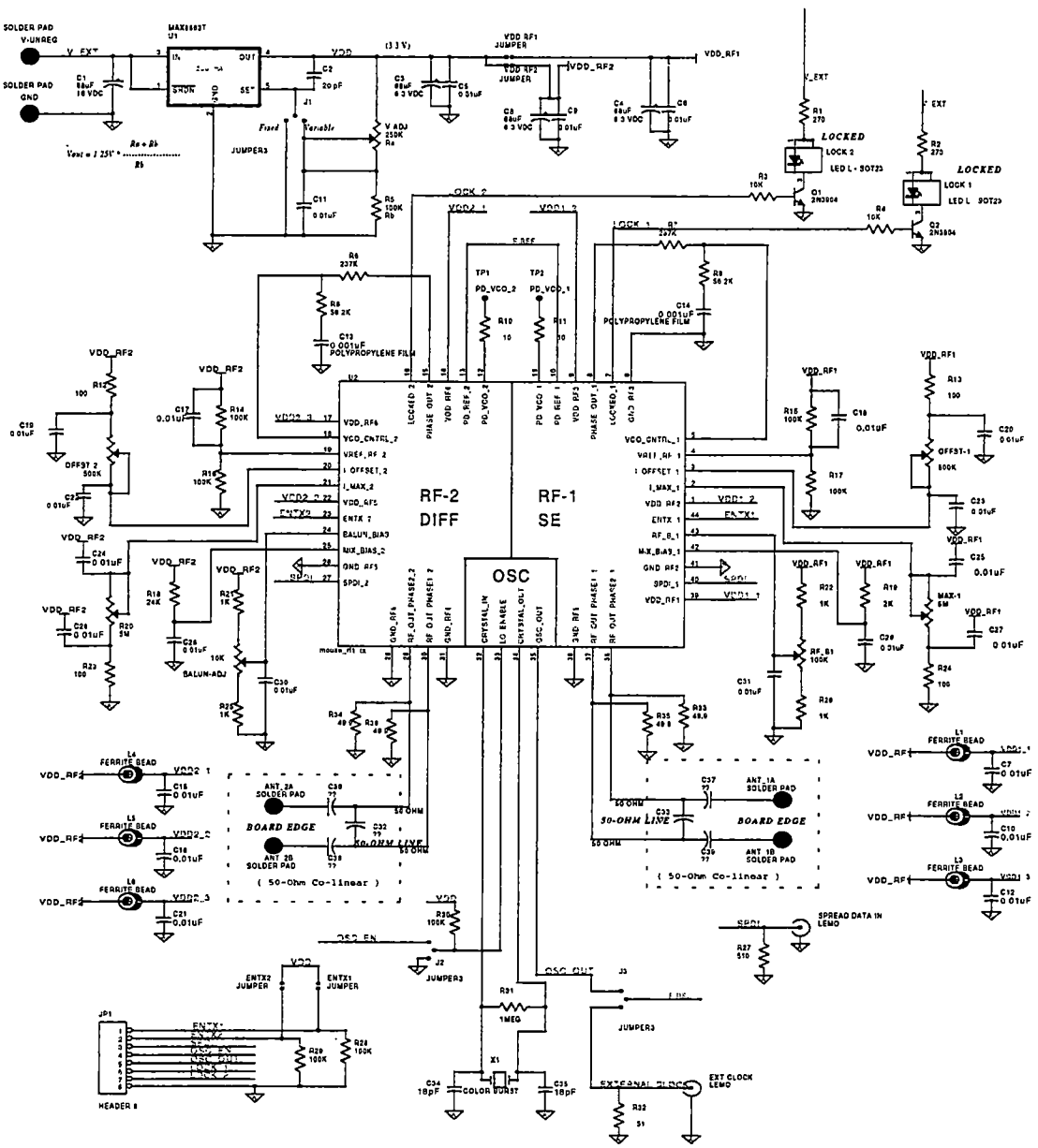

Figure 5.1 - Mousetx1 Test PCB Layout

5.2 Individual Circuit Testing

Testing and characterization of each circuit within the transmitter system was conducted wherever possible. Because some circuit nodes are inaccessible, full testing of every circuit was not possible.

5.2.1 Precision Frequency Reference

Testing the frequency reference presented in Chapter 2 required measurement of the output frequency, the output frequency stability and the average power dissipation. The oscillator's steady-state output frequency (pin 35) was measured (using a frequency counter) to be 3.579615 MHz which corresponds well to the calculated frequency found in Chapter 2 (3.579 MHz). The oscillator's short term frequency stability was measured by integrating the output of the transmitter (pins 37 and 38) with no data modulation (using a spectrum analyzer) over a specified time period and determining the width of the spectral peak. The integration was accomplished using the "max/hold" function of the spectrum analyzer which stores the maximum spectral energy content at each frequency location. Figure 2.2 shows the measured drift in carrier frequency over an approximately 10 minute period (after the circuit had time to warm up). This drifting of the PLL output frequency is the direct result of drift in the frequency reference. The frequency reference drift was obtained by dividing the width of the transmitter's spectral output by the PLL's gain (256) and then dividing this by the time of integration which yields a frequency drift rate of approximately 4.7 Hz/hr. The drift in reference frequency is mostly due to fluctuations in ambient temperature which affect crystal parameters in the oscillator and not because of fluctuations in circuit parameters. Because the implantable unit is inside

the body of a mouse, the circuit temperature will remain fairly constant and the drift rate will actually be lower than this test indicated. The average power dissipated by the oscillator was measured to be 719.4 μW (218 μA) which is higher than the simulated power dissipation found in Chapter 2 (480 μW or 145 μA average current). This discrepancy is due to the additional power required to drive the digital output pad and the additional capacitance introduced by the package and PCB test board. Using Equation 2.16 and assuming a total package and PCB board capacitance of approximately 5 pF the additional average power consumption due to the digital output driver is approximately 194 μW (59 μA). This result added to the simulated power found in Chapter 2 is 674 μW which corresponds well to the measured value. Table 5.1 is a summary of the local oscillator's measurement results.

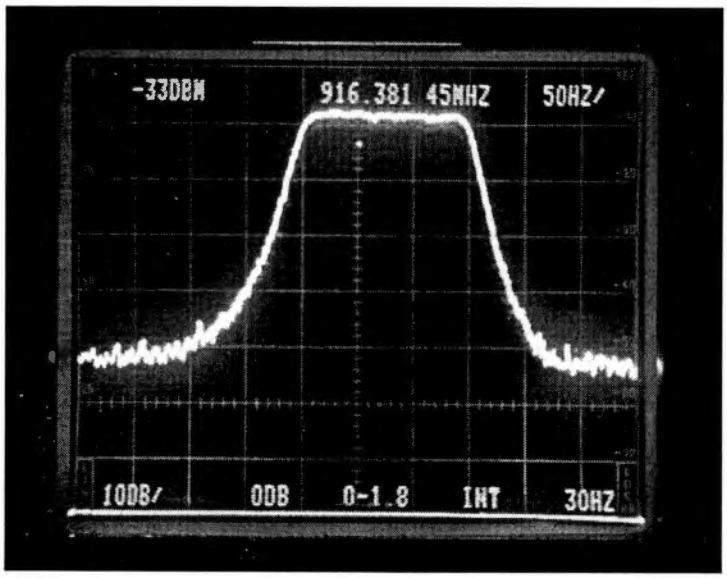

Figure 5.2 - Transmitter Output Drift - (Horizontal Axis is 50 Hz per Division, Measurement Time is 10 Minutes)

Table 5.1 - Frequency Reference Measurement Results

Performance Parameter	Value
Output Frequency	3.579615 MHz
Operating Power	719.4 μW

5.2.2 Voltage Controlled Oscillator

Before the VCO was characterized the resistors which control the tuning range (MAX-1) and offset frequency (OFFST-1) were adjusted to achieve a 100 MHz tuning range centered about the 916 MHz carrier frequency. The VCO's tuning range was obtained by inserting a DC voltage at the VCO control input (pins 5 and 18) and measuring the output frequency of the divider (pins 11 and 12) as the DC control voltage is varied from 0.0 to 3.3 volts. The VCO output frequency was obtained by reading the output from the divider and multiplying this number by 256. Using the simulation results of Chapter 3, the initial values for the tuning range and offset frequency bias resistors were initially adjusted (using trimmable-potentiometers) to 634 KΩ and 53.6 KΩ respectively. These bias resistor values resulted in an output frequency range of 732 MHz to over 1.87 GHz. Resultantly, the bias resistor values were adjusted until the desired tuning range was achieved. The actual resistor values required for the tuning range and frequency offset resistors became 2.24 MΩ and 362 KΩ respectively. The resulting output frequency versus input control voltage is shown in Figure 5.3. The resulting VCO gain is 100 MHz / 0.3 V compared to 91 MHz / 0.4 V found from the simulation results in Chapter 3 (Table 3.1).

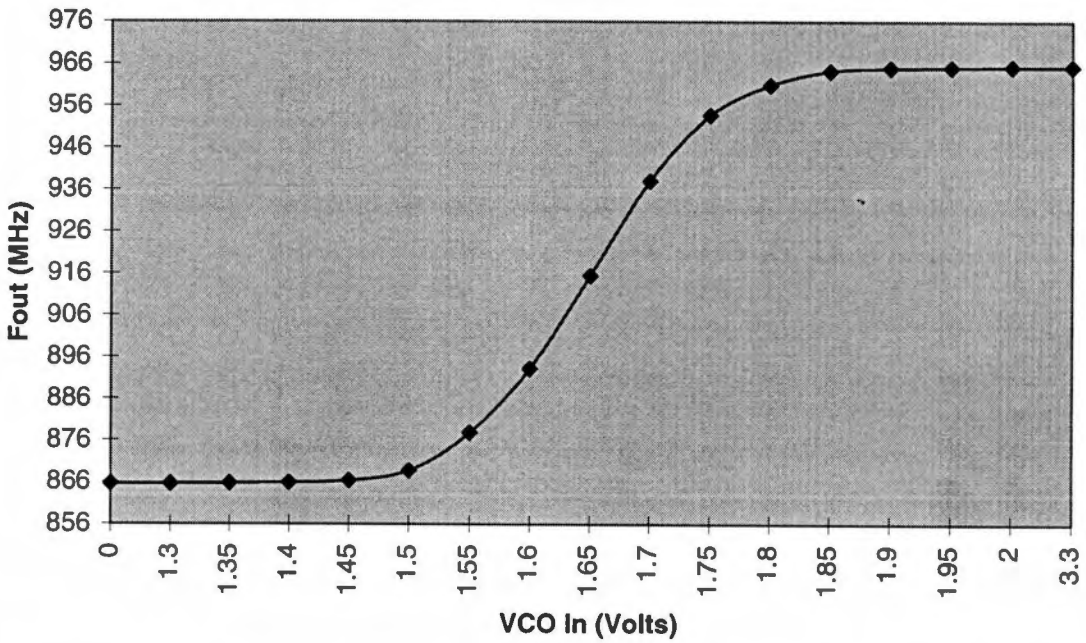

Figure 5.3 - VCO Output Characteristic

5.2.3 PLL

The PLL was tested as a stand-alone system by measuring the output frequency of the divider which should match that of the frequency reference if the PLL is functioning properly. Using the loop filter component values (R7, R9 and C14) calculated in Chapter 3, the PLL's output frequency was stable and locked to the frequency reference. This indicates that the PLL was fully functional. Initial testing of the PLL indicated the loop had positive feedback. Careful examination of the layout revealed that the phase detector inputs were reversed. This was remedied by interchanging the VCO reference and control inputs on the test PCB. By testing the PLL as a system, the functionality of the divider and phase detector was confirmed. The lock-in time of the PLL was measured by gating the enable signal (pins 23 and 44) of the transmitter and measuring the time

required for the loop filter output to settle. Measurements indicate the lock-in time to be 258 μsec which is much longer than the 28 μsec calculated from Equation 3.11. The discrepancy arises because the equation in Chapter 3 does not account for the time required for the VCO to build up oscillations upon enablement. The digital controller for the implantable allows for a PLL startup time of up to 1 msec. Thus the PLL lock-in time is acceptable.

5.2.4 Mixer

Characterization of the mixer is constrained because the carrier frequency inputs of the mixer are not accessible off chip. The only mixer input which can be externally controlled is the digital data input (pins 27, 40). Resultantly, all mixer testing consists of measuring the mixer output with the spectrum analyzer for various forms of digital data input. The mixer's functionality is then determined by comparing the measured output spectrum to the ideal spectrum expected for each type of digital data input. Three types of digital data input used in the testing are no digital input, a square wave digital input and a spread spectrum digital input. No digital input theoretically results in a single spectral peak located at the 916 MHz carrier frequency. A square wave digital input theoretically results in suppression of the carrier peak with spectral peaks located at the odd harmonic frequencies of the digital square wave centered about 916 MHz. The digital square wave for this test is supplied by the frequency reference and therefore should yield spectral peaks located at 916 MHz +/- (3.5796 MHz, 10.738 MHz ...). A direct sequence spread spectrum digital signal theoretically results in a sinc^2 output spectrum (Figure 4.1) with the first null located at 916 MHz +/- the chipping rate of the

spread digital signal [5]. The spread spectrum generator used in this test had a chipping rate of 894.9 kHz.

Figure 5.4 shows the mixer output (pins 37 and 38) with no digital data modulation for the single-ended drive mixer. This figure indicates the presence of the carrier frequency at the output in addition to undesired spectral peaks located approximately 3.579 MHz (reference frequency of the PLL) from the carrier. The undesired peaks may be the result of noise coupling into the power supply from the frequency reference. Because the unwanted spectral interferers are 20 dB below the carrier they should not present significant problems to the transmitter system.

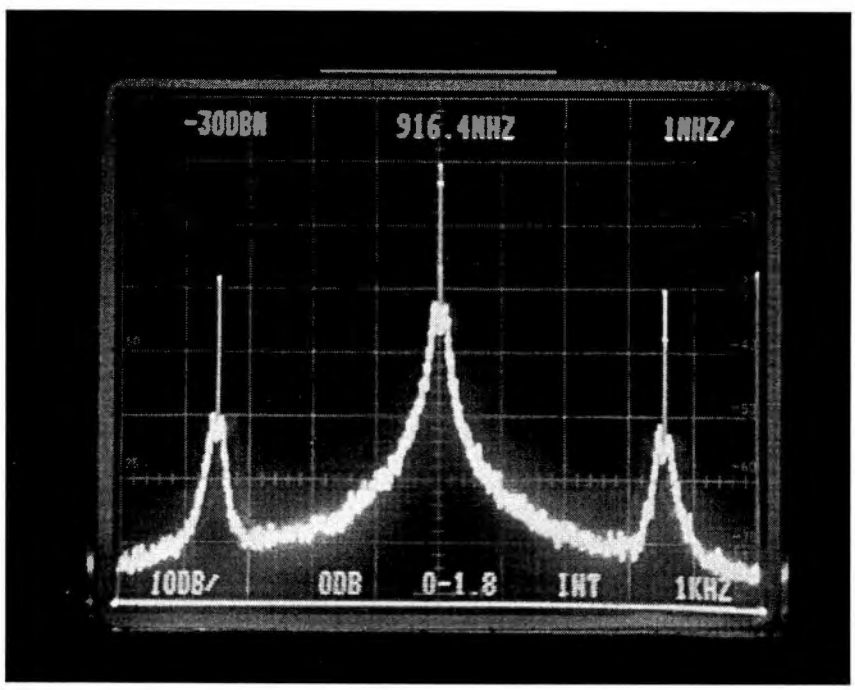

Figure 5.4 - Single-Ended Driven Mixer Output (No Modulation)

Modulating the single-ended drive mixer with the frequency reference results in the spectrum shown in Figure 5.5. The frequency reference harmonics are present at the output in addition to the carrier frequency. The presence of the 916 MHz carrier frequency at the output indicates the mixer is not performing in an ideal manner. Figure 5.6 is the measured output spectrum for a spread spectrum digital data input modulation for the single-ended drive mixer. The resulting spectrum has improper shaping and null location which indicates the single-ended driven mixer configuration is not functional. When modulating the mixer with the spread data, the receiver (vector signal analyzer) is unable to demodulate the data correctly. Resultantly, the transmitter system which incorporates the single-ended mixer drive is not functional.

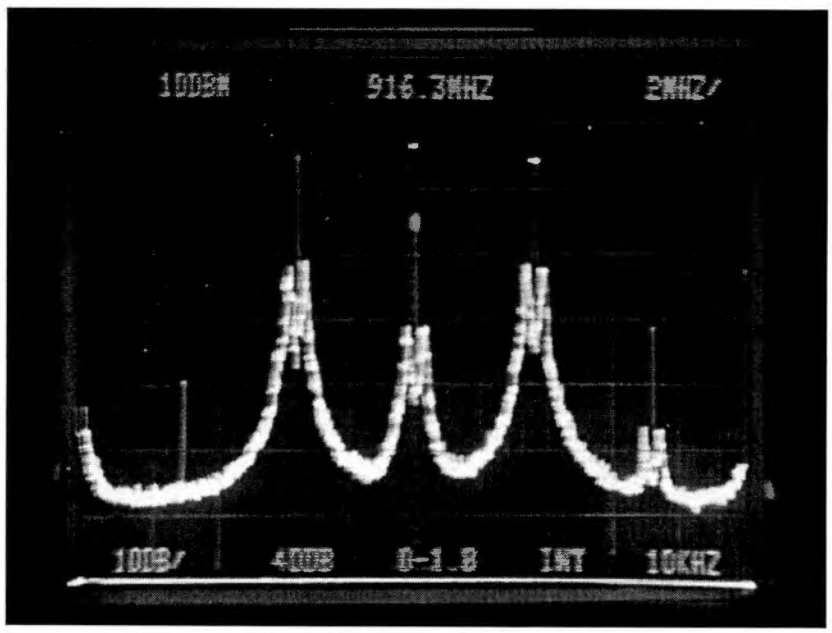

Figure 5.5 - Single-Ended Driven Mixer Output (Square Wave Modulation)

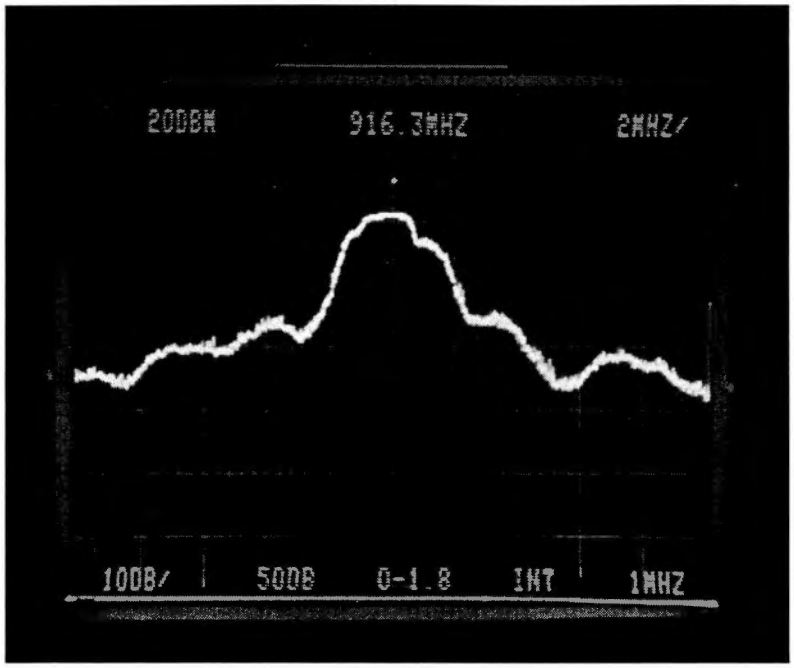

Figure 5.6 - Single-Ended Driven Mixer Output (Spread Spectrum Modulation)

Efforts were made to improve mixer performance by changing the bias current level to the mixer, but this had no effect. Simulation results in Chapter 4 indicated that the mixer's output has phase imbalance for the single-ended type of carrier frequency input driving configuration. This is likely the cause of the mixer's poor performance characteristics (Figure 4.8).

Similar testing of the differentially driven mixer resulted in the output spectra shown in Figures 5.7 and 5.8. No modulation input and square wave modulation resulted in the same output spectrum shown in Figure 5.7. Figure 5.7 is incorrect for either type of modulation and indicates a broad spectral peak located about the carrier frequency. Figure 5.8 is the output spectrum for a spread spectrum data input and is also incorrect.

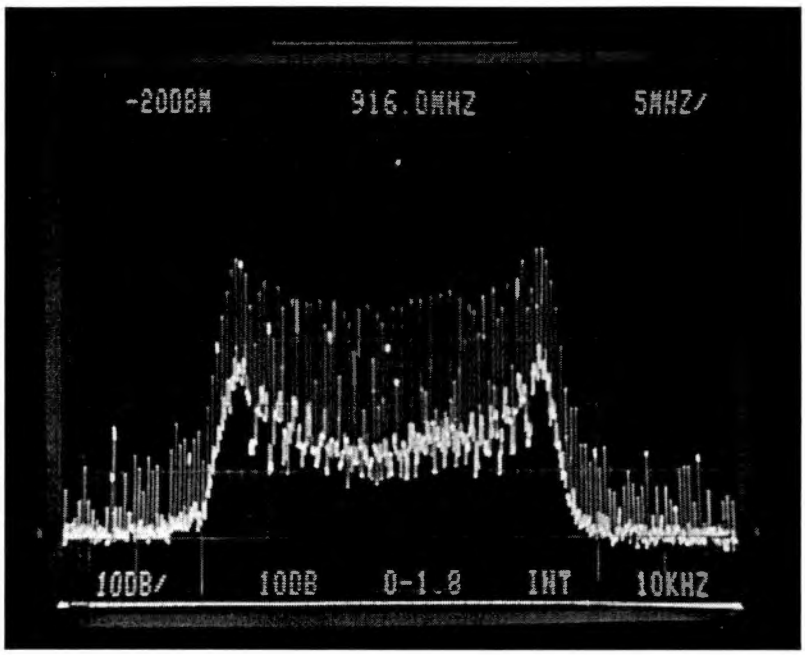

Figure 5.7 - Differentially Driven Mixer Output

(No Modulation and Square Wave Modulation)

The reason for the poor performance of the differentially driven mixer is not fully understood. Potential non-linearity and attenuation of the RF carrier introduced by the phase splitting network of Figure 4.7 is likely to be one of the reasons for this poor performance. Simulations of the differentially driven mixer in Chapter 4 included the phase splitting network and indicated the circuit to be functional. However, the simulations rely heavily on the accuracy of the device models which may be inaccurate at high frequencies. Further analysis of this configuration will be conducted in the future to determine the reason for poor performance.

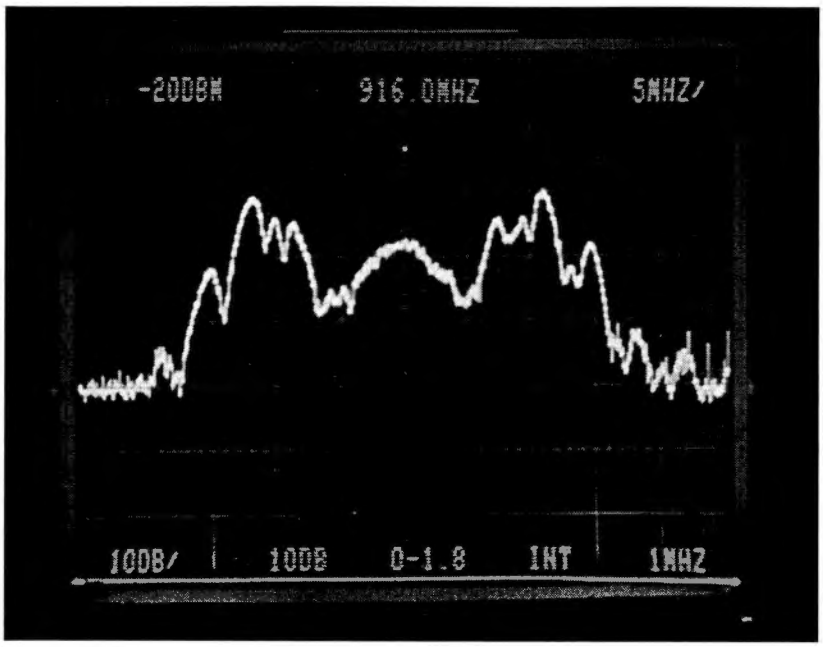

Figure 5.8 - Differentially Driven Mixer Output (Spread Spectrum Modulation)

Both mixer configurations are not functional. Further simulations indicate that the single-ended drive configuration may operate correctly if the carrier frequency input is attenuated. Future efforts must be directed toward mixer design improvements especially to proper design of the RF carrier driving circuit.

5.3 Complete Transmitter System

Both transmitter systems on the chip are partially functional. The frequency reference and PLL work properly. The transmitter is unable to modulate data properly due to poor performance of the mixer circuits and their corresponding carrier frequency driving configurations. Table 5.2 is a summary of each transmitter's performance. The

difference in operating power between the two transmitter systems is a result of different mixer bias current levels (R18, R19) and the additional power consumed by the phase splitting network of the differentially driven mixer. The receiver is unable to correctly demodulate the transmitted signal of either transmitter system with any regularity. The receiver has correctly interpreted only two data packets to date. Future efforts will be directed toward the design of a more robust transmitter system which performs successful data modulation.

Table 5.2 - Transmitter Chip Performance Summary

Performance Parameter	**Single-Ended Drive Transmitter**	**Differential Drive Transmitter**
PLL Reference Frequency	3.579615 MHz	3.579615 MHz
PLL Tuning Range	100 MHz	100 MHz
PLL Lock-In Time	258 μsec	258 μsec
Modulator Functional	No	No
Operating Power	122 mW	77 mW

Chapter 6

Conclusions and Future Work

A transmitter system has been designed, fabricated in the HP-0.5μm process and tested. Two complete transmitter systems are implemented on the same chip for comparison. One transmitter system drives the carrier frequency inputs of the mixer directly from the single-ended PLL output and the other uses a single-ended to differential converter circuit. This chapter summarizes the overall performance of each transmitter system and the direction of future work for improvement of the transmitter. The next version of the transmitter system is scheduled for fabrication submission in January 1999. This revised version will implement many of the design modifications recommended in this chapter.

6.1 Conclusions

Testing of the frequency reference discussed in Chapter 2 indicates the oscillator circuit to be fully functional. The circuit exhibits a stable output frequency and low operating power. Close examination of the layout revealed a floating well that will be

connected to the positive supply rail in the next design cycle. However, that is the only change required for the next fabrication run.

Test results indicate the PLL, described in Chapter 3, operates in a stable fashion, producing an output frequency of 916 MHz. However, the phase detector inputs are switched in the PLL layout resulting in a positive feedback system. This was remedied by switching the VCO inputs at the test PCB level. The next design cycle will incorporate the correct PLL connection. In addition, efforts will be made to obtain a narrower tuning range of the VCO with realizable on-chip values for the bias resistors (< 500 KΩ).

The RF mixer discussed in Chapter 4 is the transmitter circuit most in need of redesign. The single-ended driving configuration of the 916 MHz carrier input to the mixer exhibited poor modulation characteristics. The spectral shape of the modulated digital data message is distorted, resulting in the inability to demodulate the transmitted signal correctly except on rare occasion (twice to date). The poor modulation characteristics of the single-ended drive configuration are evident in simulation results conducted after the chip was in fabrication. These simulations reveal a phase imbalance between the mixer's differential outputs. Later simulations of the mixer indicate a single-ended driving configuration with a reduction in voltage swing of the carrier input yields a better output characteristic. Future efforts can therefore be directed toward attenuating the PLL output before driving the mixer in single-ended configuration. The differential mixer drive configuration, which appeared the most promising from simulations, exhibited almost no output signal. This is likely due to severe attenuation of the carrier frequency output of the PLL by the phase splitting network of Figure 4.7. The

discrepancy between simulation results and test measurements are attributed to poor device models at high frequencies. The phase-splitting circuit requires significant redesign in order to operate correctly at 916 MHz. One or both modified driving implementations will be implemented in the next design cycle.

In summary, the overall transmitter performance suffers from the poor performance of the mixer and associated 916 MHz driving networks. Resultantly, the transmitter is not consistently functioning properly as a system. Carrier frequency generation accomplished by the frequency reference and PLL function properly, but significant efforts must be focused on improving the data modulation portion of the transmitter.

6.2 Future Work

Future research for the transmitter system will be directed toward reduction in operating power and improvement in transmitter performance. Development of new topologies for the PLL which produce an inherently differential output in addition to a lower operating power is central to improving transmitter performance. Development of digital cells which run at a reduced voltage level will lead to lower power operation. In addition, replacing the NMOS flip-flop at the first stage of the divider with a custom CMOS flip-flop capable of operating at 916 MHz will reduce power consumption. Replacing the active mixer topology with a passive implementation followed by an RF output amplifier may result in superior modulation and transmission performance while reducing power consumption. Better simulation models for the transistors are needed to

provide more accurate simulation results of circuit performance at high frequencies. Efforts are underway to characterize transistors fabricated in the HP-0.5μm process using commercially available test systems and software.

In addition to the existing transmitter system, the supply independent biasing cell discussed in the latter half of Chapter 4 (Figure 4.16) will be implemented in the next design cycle. The bias circuit will be fully characterized to determine the power supply rejection that is provided.

Efforts will also be directed toward minimizing the number of external components required by the transmitter to reduce the size of the implantable. Once functional, the transmitter will be incorporated on a single chip with the analog measurement electronics and the digital controller. This will implement a highly miniaturized, integrated measurement system that is suitable for use as an implantable.

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Appendices

Appendix 1

Process Parameters and Device Models

MOSIS PARAMETRIC TEST RESULTS

RUN: N83X VENDOR: HP-NID
TECHNOLOGY: SCN05H FEATURE SIZE: 0.5 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SMN3MLC06

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.9/0.60			
Vth		0.74	-0.89	Volts
SHORT	15/0.60			
Idss		359	-172	uA/um
Vth		0.67	-0.89	Volts
Vpt		10.0	-10.0	Volts
WIDE	15/0.60		-10.0	Volts
Ids0		4.0	0.3	pA/um
LARGE	5.4/5.4			
Vth		0.78	-0.93	Volts
Vjbkd		11.6	-10.1	Volts
Ijlk		-18.4	-1.4	pA
Gamma		0.51	0.48	V^0.5
Delta length (L_eff = L_drawn-DL)		0.10	0.12	microns
Delta width (W_eff = W_drawn-DW)		0.44	0.38	microns
K' (Uo*Cox/2)		89.3	-25.4	uA/V^2

COMMENTS: Delta L varies with design technology as a result of the different mask biases applied for each technology. Please adjust the delta L in this report to reflect the actual design technology of your submission.

Design Technology Delta L

SCN_SUBM (lambda=0.3), CMOSH,	
HP_AMOS14TB	no adjustment
SCN (lambda=0.35)	add 0.1 um

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	UNITS
Sheet Resistance	2.0	2.2	1.9	0.07	0.07	0.05	ohms/sq
Width Variation	-0.31	-0.25	-0.05	0.14	0.00	-0.39	microns
(measured - drawn)							
Contact Resistance	3.6	1.8	1.8		0.54	0.30	ohms
Gate Oxide Thickness	98						angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	N_WELL	UNITS
Area (substrate)	551	942	88	29	13	8	93	aF/um^2
Area (N+active)		3538						aF/um^2
Area (P+active)		3340						aF/um^2
Area (poly)			59	18	11			aF/um^2
Area (metal1)				42	16			aF/um^2
Area (metal2)					45			aF/um^2
Area (cap well)		2243						aF/um^2
Fringe (substrate)	203	226						aF/um
Overlap (N+active)		256						aF/um
Overlap (P+active)		365						aF/um

CIRCUIT PARAMETERS		UNITS
Inverters	K	
Vinv	1.0	1.31 Volts
Vinv	1.5	1.45 Volts
Vol (100 uA)	2.0	0.22 Volts
Voh (100 uA)	2.0	3.01 Volts
Vinv	2.0	1.54 Volts
Gain	2.0	-20.61
Ring Oscillator Freq.		
DIV4 (31-stage,3.3V)		132.66 MHz
Ring Oscillator Power		
DIV4 (31-stage,3.3V)		7.35 uW/MHz/g

COMMENTS: SUBMICRON

SPICE LEVEL2/LEVEL3 parameters not available.

N83X SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

```
* DATE: 98 Aug 14
* LOT: n83x              WAF: 97
.MODEL CMOSN NMOS                       LEVEL  = 49
+VERSION = 3.1          TNOM   = 27     TOX    = 9.8E-9
+XJ    = 1.5E-7         NCH    = 1.7E17 VTH0   = 0.6926001
+K1    = 0.7517284      K2     = -0.0275839 K3  = 26.5643237
+K3B   = 0.0258233      W0     = 6.649233E-6 NLX = 1E-9
+DVT0W = 0              DVT1W  = 5.3E6  DVT2W  = -0.032
+DVT0  = 6.6105572      DVT1   = 0.7856988 DVT2 = -0.1371922
+U0    = 472.8503859    UA     = 4.533417E-10 UB = 1.688441E-18
+UC    = 5.349131E-11   VSAT   = 1.198985E5 A0  = 0.8787629
+AGS   = 0.2233624      B0     = 2.806272E-7 B1  = 1E-6
+KETA  = -7.83313E-3    A1     = 0      A2     = 1
+RDSW  = 1.125307E3     PRWG   = 2.81017E-3 PRWB = -1E-3
+WR    = 1              WINT   = 2.35844E-7 LINT = 1.008283E-7
+DWG   = -1.674553E-8   DWB    = 7.248074E-9 VOFF = -0.1155467
+NFACTOR = 1.6252996    CIT    = 0      CDSC   = 4.563611E-4
+CDSCD = 0              CDSCB  = 0      ETA0   = 1.571529E-3
+ETAB  = -1.0698E-3     DSUB   = 0.0315029 PCLM = 0.6523044
+PDIBLC1 = 0.1197024    PDIBLC2 = 1.297161E-3 PDIBLCB = 0
+DROUT = 0.5527975      PSCBE1 = 1.204532E10 PSCBE2 = 6.023475E-9
+PVAG  = 3.985695E-3    DELTA  = 0.01   MOBMOD = 1
+PRT   = 0              UTE    = -1.5   KT1   = -0.11
+KT1L  = 0              KT2    = 0.022  UA1   = 4.31E-9
+UB1   = -7.61E-18      UC1    = -5.6E-11 AT  = 3.3E4
+WL    = 0              WLN    = 1      WW    = 0
+WWN   = 1              WWL    = 0      LL    = 0
+LLN   = 1              LW     = 0      LWN   = 1
+LWL   = 0              CAPMOD = 2      CGDO  = 2.56E-10
+CGSO  = 2.56E-10       CGBO   = 0      CJ    = 5.68712E-4
+PB    = 0.99           MJ     = 0.6094506 CJSW = 2.284659E-10
+PBSW  = 0.99           MJSW   = 0.1    PVTH0 = 5.180777E-3
+PRDSW = -112.5042317   PK2    = 7.830156E-3 WKETA = -1.97987E-3
+LKETA = -8.90227E-3
*
*
.MODEL CMOSP PMOS                       LEVEL  = 49
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+VERSION = 3.1        TNOM   = 27        TOX    = 9.8E-9
+XJ    = 1.5E-7       NCH    = 1.7E17     VTH0   = -0.8611243
+K1    = 0.4251539    K2     = 0.0178745  K3     = 48.3069795
+K3B   = -0.4919902   W0     = 5.631345E-6 NLX   = 1.051056E-9
+DVT0W  = 0           DVT1W  = 5.3E6      DVT2W  = -0.032
+DVT0   = 2.7431352   DVT1   = 0.484266   DVT2   = -0.1179261
+U0    = 170.7833624  UA     = 9.839213E-10 UB    = 1.397311E-18
+UC    = -3.74016E-11 VSAT   = 1.50608E5  A0     = 0.905698
+AGS   = 0.1799768    B0     = 7.232635E-7 B1    = 1E-6
+KETA  = -1.238016E-3 A1     = 0          A2     = 1
+RDSW  = 1.873051E3   PRWG   = -8.860299E-5 PRWB  = -1E-3
+WR    = 1          WINT   = 2.296034E-7 LINT   = 6.27625E-8
+DWG   = -2.364966E-8 DWB    = 1.342602E-8 VOFF   = -0.1033981
+NFACTOR = 2         CIT    = 0          CDSC   = 1.413317E-4
+CDSCD  = 0          CDSCB  = 0          ETA0   = 0.0715904
+ETAB  = -3.889763E-3 DSUB   = 0.2863572  PCLM   = 6.952727
+PDIBLC1 = 9.998236E-4  PDIBLC2 = 2.388926E-4  PDIBLCB = 2.37525E-3
+DROUT  = 0.9322171   PSCBE1 = 9.697351E9  PSCBE2 = 5.002859E-9
+PVAG  = 14.9894242   DELTA  = 0.01       MOBMOD = 1
+PRT   = 0          UTE    = -1.5       KT1    = -0.11
+KT1L  = 0          KT2    = 0.022      UA1    = 4.31E-9
+UB1   = -7.61E-18    UC1    = -5.6E-11    AT     = 3.3E4
+WL    = 0          WLN    = 1          WW     = 0
+WWN   = 1          WWL    = 0          LL     = 0
+LLN   = 1          LW     = 0          LWN    = 1
+LWL   = 0          CAPMOD = 2          CGDO   = 3.65E-10
+CGSO  = 3.65E-10     CGBO   = 0          CJ     = 9.414558E-4
+PB    = 0.9251013    MJ     = 0.4816618    CJSW   = 2.321999E-10
+PBSW  = 0.8142544    MJSW   = 0.2177408    PVTH0  = 6.407216E-3
+PRDSW = -148.1555679 PK2    = 4.115514E-3  WKETA  = 1.067439E-3
+LKETA  = -5.308404E-3
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*
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MOSIS PARAMETRIC TEST RESULTS

RUN: N86L VENDOR: HP-NID
TECHNOLOGY: SCN05H FEATURE SIZE: 0.5 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar

measurements on a selected wafer are also attached.

COMMENTS: SMN3MLC06

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.9/0.60			
Vth		0.73	-0.87	Volts
SHORT	15/0.60			
Idss		340	-166	uA/um
Vth		0.67	-0.89	Volts
Vpt		10.0	-9.8	Volts
WIDE	15/0.60		-10.0	Volts
Ids0		0.4	-0.0	pA/um
LARGE	5.4/5.4			
Vth		0.72	-0.90	Volts
Vjbkd		11.7	-10.0	Volts
Ijlk		-1.5	-4.1	pA
Gamma		0.63	0.49	V^0.5
Delta length (L_eff = L_drawn-DL)		0.17	0.12	microns
Delta width (W_eff = W_drawn-DW)		0.47	0.46	microns
K' (Uo*Cox/2)		74.9	-23.6	uA/V^2

COMMENTS: Delta L varies with design technology as a result of the different mask biases applied for each technology. Please adjust the delta L in this report to reflect the actual design technology of your submission.

Design Technology	Delta L
SCN_SUBM (lambda=0.3), CMOSH, HP_AMOS14TB	no adjustment
SCN (lambda=0.35)	add 0.1 um

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	UNITS
Sheet Resistance	2.3	2.2	2.1	0.07	0.07	0.05	ohms/sq
Width Variation			0.01	0.19	0.09	-0.34	microns
(measured - drawn)							
Contact Resistance	2.3	2.2	1.9		0.63	0.43	ohms
Gate Oxide Thickness	97						angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	N_WELL	UNITS
Area (substrate)	550	942	84	26	10	7	87	aF/um^2
Area (N+active)			3554					aF/um^2
Area (P+active)			3374					aF/um^2
Area (poly)				59	18	10		aF/um^2
Area (metal1)					43	16		aF/um^2
Area (metal2)						45		aF/um^2
Area (cap well)			2237					aF/um^2
Fringe (substrate)	236	217						aF/um
Overlap (N+active)			377					aF/um
Overlap (P+active)			357					aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	1.30	Volts
Vinv	1.5	1.45	Volts
Vol (100 uA)	2.0	0.27	Volts
Voh (100 uA)	2.0	2.95	Volts
Vinv	2.0	1.54	Volts
Gain	2.0	-20.91	
Ring Oscillator Freq.			
DIV4 (31-stage,3.3V)		125.47	MHz
Ring Oscillator Power			
DIV4 (31-stage,3.3V)		5.07	uW/MHz/g

N86L SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

```
* DATE: 98 Sep  2
* LOT: n86l                WAF: 11
.MODEL CMOSN NMOS (                      LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 9.7E-9
+XJ      = 1.5E-7       NCH     = 1.7E17      VTH0    = 0.6983859
+K1      = 0.7659797    K2      = -0.0301713  K3      = 22.5760829
+K3B     = 0.3813678    W0      = 4.768711E-6 NLX     = 1E-10
```

```
+DVT0W  = 0          DVT1W  = 5.3E6      DVT2W  = -0.032
+DVT0   = 3.466035   DVT1   = 0.5856675  DVT2   = -0.1757707
+U0     = 477.9032949 UA    = 4.507669E-10 UB    = 1.627355E-18
+UC     = 5.785499E-11 VSAT  = 1.181417E5  A0    = 0.8195622
+AGS    = 0.2245344  B0     = 1.191666E-6 B1    = 4.5E-6
+KETA   = -0.0169633  A1    = 0          A2    = 1
+RDSW   = 1.128758E3  PRWG   = 2.150294E-3 PRWB   = -1E-3
+WR     = 1          WINT   = 2.60081E-7  LINT   = 1.003766E-7
+DWG    = -1.585744E-8 DWB   = 8.848359E-9  VOFF   = -0.121124
+NFACTOR = 1.3591886  CIT    = 0          CDSC   = 5.899894E-4
+CDSCD  = 0          CDSCB  = 0          ETA0   = 2.99992E-3
+ETAB   = -1.782462E-3 DSUB  = 0.0693573  PCLM   = 0.7154819
+PDIBLC1 = 0.1012028  PDIBLC2 = 1.455176E-3 PDIBLCB = -1E-3
+DROUT  = 0.5634651  PSCBE1 = 1.209752E10 PSCBE2 = 5.658387E-9
+PVAG   = 0.0164415  DELTA  = 0.01       MOBMOD = 1
+PRT    = 0          UTE    = -1.5       KT1    = -0.11
+KT1L   = 0          KT2    = 0.022      UA1    = 4.31E-9
+UB1    = -7.61E-18  UC1    = -5.6E-11   AT     = 3.3E4
+WL     = 0          WLN    = 1          WW     = 0
+WWN    = 1          WWL    = 0          LL     = 0
+LLN    = 1          LW     = 0          LWN    = 1
+LWL    = 0          CAPMOD = 2          CGDO   = 3.77E-10
+CGSO   = 3.77E-10   CGBO   = 0          CJ     = 5.708693E-4
+PB     = 0.99       MJ     = 0.6173498  CJSW   = 2.679761E-10
+PBSW   = 0.99       MJSW   = 0.1        PVTH0  = 1.247984E-3
+PRDSW  = -109.2224469 PK2  = 5.637233E-3 WKETA  = -2.842339E-3
+LKETA  = -6.835557E-3 )
*
*
.MODEL CMOSP PMOS (                     LEVEL  = 49
+VERSION = 3.1       TNOM   = 27         TOX    = 9.7E-9
+XJ     = 1.5E-7     NCH    = 1.7E17     VTH0   = -0.8702226
+K1     = 0.3959269  K2     = 0.0250288  K3     = 27.8616279
+K3B    = -0.0125995 W0     = 4.638367E-6 NLX    = 5.504094E-9
+DVT0W  = 0          DVT1W  = 5.3E6      DVT2W  = -0.032
+DVT0   = 0.8963451  DVT1   = 0.3806866  DVT2   = -0.2992995
+U0     = 171.3912088 UA    = 1.135428E-9 UB    = 1.216149E-18
+UC     = -4.87919E-11 VSAT  = 1.722989E5  A0    = 0.763782
+AGS    = 0.1148865  B0     = 2.729393E-6 B1    = 5E-6
+KETA   = -4.979939E-3 A1   = 0          A2    = 1
+RDSW   = 1.911508E3  PRWG   = -8.46039E-5 PRWB   = -1E-3
+WR     = 1          WINT   = 2.486655E-7 LINT   = 7.180512E-8
+DWG    = -2.269793E-8 DWB   = 1.176893E-8 VOFF   = -0.1092326
+NFACTOR = 2         CIT    = 0          CDSC   = 4.674361E-4
```

```
+CDSCD  = 0          CDSCB  = 0          ETA0   = 0.0141517
+ETAB   = -1.074722E-3 DSUB  = 0.1298303   PCLM   = 3.7909533
+PDIBLC1 = 8.691023E-3  PDIBLC2 = 0.01      PDIBLCB = 0.0964449
+DROUT  = 1          PSCBE1 = 2E10       PSCBE2 = 5.003682E-8
+PVAG   = 0.8438828  DELTA  = 0.01       MOBMOD = 1
+PRT    = 0          UTE    = -1.5       KT1    = -0.11
+KT1L   = 0          KT2    = 0.022      UA1    = 4.31E-9
+UB1    = -7.61E-18  UC1    = -5.6E-11   AT     = 3.3E4
+WL     = 0          WLN    = 1          WW     = 0
+WWN    = 1          WWL    = 0          LL     = 0
+LLN    = 1          LW     = 0          LWN    = 1
+LWL    = 0          CAPMOD = 2          CGDO   = 3.57E-10
+CGSO   = 3.57E-10   CGBO   = 0          CJ     = 9.406393E-4
+PB     = 0.9474411  MJ     = 0.4900716  CJSW   = 2.195826E-10
+PBSW   = 0.99       MJSW   = 0.2133867  PVTH0  = 2.999625E-3
+PRDSW  = -117.9159292 PK2  = 3.869835E-4 WKETA  = 4.477811E-3
+LKETA  = -0.0108283  )
*
*
```

MOSIS PARAMETRIC TEST RESULTS

RUN: N83W VENDOR: HP-NID
TECHNOLOGY: SCN05H FEATURE SIZE: 0.5 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: Hewlett Packard CMOS14TB.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.9/0.60			
Vth		0.74	-0.91	Volts
SHORT	15/0.60			
Vth		0.67	-0.91	Volts
Vpt		10.0	-10.0	Volts
Vbkd		11.3	-9.8	Volts

Idss	366	-176	uA/um
WIDE	15/0.60		
Ids0	0.4	-0.1	pA/um
LARGE	5.4/5.4		
Vth	0.78	-0.95	Volts
Vjbkd	11.7	-9.9	Volts
Ijlk	-28.9	-9.4	pA
Gamma	0.50	0.47	V^0.5
Delta length (L_eff = L_drawn-DL)	0.11	0.13	microns
Delta width (W_eff = W_drawn-DW)	0.44	0.39	microns
K' (Uo*Cox/2)	91.0	-25.6	uA/V^2

COMMENTS: DL_HP_CMOS14TB

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	UNITS
Sheet Resistance	2.0	1.9	1.9	0.07	0.07	0.05	ohms/sq
Width Variation (measured - drawn)		-0.01	0.13	0.10	-0.40		microns
Contact Resistance	2.1	2.1	1.7		0.48	0.42	ohms
Gate Oxide Thickness	96						angstroms

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	UNITS
Area (substrate)	556	956	84	26	11	8	aF/um^2
Area (N+active)		3593					aF/um^2
Area (P+active)		3371					aF/um^2
Area (poly)			56	19	11		aF/um^2
Area (metal1)				51	17		aF/um^2
Area (metal2)					48		aF/um^2
Fringe (substrate)	215	206					aF/um
Fringe (N+active)		31					aF/um
Fringe (P+active)		126					aF/um

CIRCUIT PARAMETERS	UNITS

Inverters	K		
Vinv	1.0	1.29	Volts
Vinv	1.5	1.43	Volts
Vol (100 uA)	2.0	0.21	Volts
Voh (100 uA)	2.0	3.02	Volts
Vinv	2.0	1.52	Volts
Gain	2.0	-19.41	
Ring Oscillator Freq.			
DIV4 (31-stage,3.3V)		135.53	MHz
Ring Oscillator Power			
DIV4 (31-stage,3.3V)		6.18	uW/MHz/g

SPICE LEVEL2/LEVEL3 parameters not available.

N83W SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

```
* DATE: 98 Jun  5
* LOT: n83w              WAF: 03
.MODEL CMOSN NMOS                          LEVEL   = 49
+VERSION = 3.1          TNOM    = 27       TOX     = 9.6E-9
+XJ      = 1.5E-7       NCH     = 1.7E17   VTH0    = 0.6632924
+K1      = 0.7869982    K2      = -0.038467 K3     = 55.9588187
+K3B     = 5.4030104    W0      = 4.897908E-6 NLX  = 7.845091E-9
+DVT0W   = 0            DVT1W   = 5.3E6    DVT2W   = -0.032
+DVT0    = 4.7728592    DVT1    = 0.7561203 DVT2   = -0.1869997
+U0      = 452.9346401  UA      = 1.090303E-10 UB  = 2.127865E-18
+UC      = 6.660445E-11 VSAT    = 1.246145E5 A0    = 0.8206228
+AGS     = 0.1988785    B0      = 1.740405E-7 B1   = 1.5E-6
+KETA    = -8.024E-3    A1      = 0        A2      = 1
+RDSW    = 1.199022E3   PRWG    = 1.46696E-3 PRWB  = -5E-3
+WR      = 1            WINT    = 2.370077E-7 LINT = 1.129098E-7
+DWG     = -2.017324E-8 DWB     = 1.105753E-8 VOFF = -0.1362826
+NFACTOR = 2            CIT     = 0        CDSC    = 2.4E-4
+CDSCD   = 0            CDSCB   = 0        ETA0    = 0.3116869
+ETAB    = -0.059698    DSUB    = 0.9346521 PCLM   = 0.6657297
+PDIBLC1 = 3.945737E-3  PDIBLC2 = 1.287379E-3 PDIBLCB = 0
+DROUT   = 0.0579612    PSCBE1  = 1.076526E9 PSCBE2 = 5E-9
+PVAG    = 0.1052285    DELTA   = 0.01     MOBMOD  = 1
+PRT     = 0            UTE     = -1.5     KT1     = -0.11
+KT1L    = 0            KT2     = 0.022    UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11 AT      = 3.3E4
+WL      = 0            WLN     = 1        WW      = 0
```

```
+WWN   = 1          WWL   = 0          LL    = 0
+LLN   = 1          LW    = 0          LWN   = 1
+LWL   = 0          CAPMOD = 2         CGDO  = 4.09E-10
+CGSO  = 4.09E-10   CGBO  = 0          CJ    = 5.784E-4
+PB    = 0.99999    MJ    = 0.62809    CJSW  = 2E-11
+PBSW  = 0.99999    MJSW  = 0.58207    PVTH0 = 3.866872E-3
+PRDSW = -90.1570124 PK2  = 6.901807E-3 WKETA = -3.35376E-3
+LKETA = -3.69461E-3
*
*
.MODEL CMOSP PMOS                     LEVEL = 49
+VERSION = 3.1      TNOM  = 27         TOX   = 9.6E-9
+XJ    = 1.5E-7     NCH   = 1.7E17     VTH0  = -0.8895465
+K1    = 0.3863059  K2    = 0.0254171  K3    = 70.4744077
+K3B   = -2.747978  W0    = 1E-5       NLX   = 5.299631E-9
+DVT0W = 0          DVT1W = 5.3E6      DVT2W = -0.032
+DVT0  = 3.1421499  DVT1  = 0.5213812  DVT2  = -0.1295075
+U0    = 207.6760845 UA   = 2.110139E-9 UB   = 6.179747E-19
+UC    = -5.39389E-11 VSAT = 1.948744E5 A0   = 1.0911467
+AGS   = 0.1657677  B0    = 5.965541E-7 B1   = 1E-6
+KETA  = -9.27E-3   A1    = 0          A2    = 1
+RDSW  = 1.787782E3 PRWG  = -1.486547E-4 PRWB = -5E-3
+WR    = 1          WINT  = 2.340014E-7 LINT  = 6.774859E-8
+DWG   = -2.452417E-8 DWB  = 9.219785E-9 VOFF  = -0.15
+NFACTOR = 2        CIT   = 0          CDSC  = 6.593084E-4
+CDSCD = 0          CDSCB = 0          ETA0  = 0.0778247
+ETAB  = 0          DSUB  = 0.2543482  PCLM  = 5.7067949
+PDIBLC1 = 0        PDIBLC2 = 3.59637E-3 PDIBLCB = 0
+DROUT = 6.264922E-4 PSCBE1 = 2E10     PSCBE2 = 5.01001E-9
+PVAG  = 12.1425411 DELTA = 0.01       MOBMOD = 1
+PRT   = 0          UTE   = -1.5       KT1   = -0.11
+KT1L  = 0          KT2   = 0.022      UA1   = 4.31E-9
+UB1   = -7.61E-18  UC1   = -5.6E-11   AT    = 3.3E4
+WL    = 0          WLN   = 1          WW    = 0
+WWN   = 1          WWL   = 0          LL    = 0
+LLN   = 1          LW    = 0          LWN   = 1
+LWL   = 0          CAPMOD = 2         CGDO  = 4.09E-10
+CGSO  = 4.09E-10   CGBO  = 0          CJ    = 9.5787E-4
+PB    = 0.94178    MJ    = 0.49097    CJSW  = 1.9544E-10
+PBSW  = 0.94178    MJSW  = 0.13556    PVTH0 = 2.592914E-3
+PRDSW = -129.3988503 PK2  = 3.008572E-3 WKETA = -1.09527E-3
+LKETA = 1.51748E-3
*
*
```

Appendix 2

Circuit Simulation Files

```
******For PSPICE Simulator******
*
* Author(s):   Ryan E. Lind
* Description: crystal oscillator circuit
*
*********************************
.include 'osc4.spice'

vdd  100  0  3.3 pulse (0 3.3 5u 1n 1n 1 2)
vss  110  0  0.0

ven   4  0  pulse (0 3.3 10u 1n 1n 1 2)
*********************************
rf    1  2  1Meg
cg    2  0  18pf
cd    1  0  18pf
cout  5  0  1pf
*********************************
ls    2   50  19.9mH
cs    50  60  0.1pF
rs    60   1  250
co    2    1  7pF
*********************************
.tran 25n  1000u
.op
.ic  v(2)=3.3 v(1)=3.3
*********************************
.include 'n56s.mod'

.options POST

.END

* osc4.spice
*
* File Location       /msd25/lind/rf/osc
* File Created        Wed Feb 11 10:11:43 1998
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options     -h -mm -n -M -N -V -gc -m -n -mg -M -N -h -g -gc -h -mm -n -V -m
*
****** top level cell is /msd25/lind/rf/osc/osc4.ext
M1 1 2 100 3 CMOSP M=2 W=2.45U L=0.70U GEO=0
M2 1 4 100 3 CMOSP M=2 W=1.75U L=0.70U GEO=0
M3 1 4 6 7 CMOSN W=1.75U L=0.70U GEO=0
```

```
M4 6 2 110 7 CMOSN W=1.75U L=0.70U GEO=0
M5 5 1 100 3 CMOSP M=2 W=2.45U L=0.70U GEO=0
M6 5 1 110 7 CMOSN W=1.75U L=0.70U GEO=0
C1 3 100 28.0F
C2 7 110 2.0F
C3 7 6 1.0F
C4 2 1 1.0F
C5 7 5 1.0F
C6 2 4 1.0F
C7 100 1 1.0F
C8 3 5 6.0F
C9 7 1 1.0F
C10 3 1 11.0F
C11 110 0 3.0F
C12 2 0 8.0F
C13 5 0 5.0F
C14 4 0 4.0F
C15 1 0 17.0F
C16 100 0 23.0F
*** Node Listing for subckt:  osc4
** N0                == IdealGND
** N1          [U=5]   == c_out
** N2          [U=2]   == c_in
** N3          [U=3]   == 6_7_30#
** N4          [U=2]   == enable
** N5          [U=2]   == osc_out
** N6          [U=2]   == 8_46_2#
** N7          [U=3]   == 6_7_7#
** N100        [U=3]   == N100
** N110        [U=2]   == N110
************************************************************

* ringosc: Simulation
* File created on Wed Nov 18 11:48:10 1998

.include 'ringosc.spice'
.include 'n56s.mod'


**************************************************
*
* Author(s): Ryan E. Lind
* Description: Current Starved Invertor Ring Oscillator
**************************************************
```

```
Vdd Vdd 0 3.3 *pulse(0 3.3 10n 1n 5n 10 20)
Vgnd Gnd 0 dc 0

VBIAS Vbias 0 dc 1.46 pulse(1.76 1.16 100n 800n 50n 1n 1u)

cl Vout 0 500fF

*.tran .1n 1u
.op
**********************************************************

.options post

Vsub Vsub 0 DC 0V $NWell Process
*Vsub Vsub 0 DC 5V $PWell Process
*
.END

* ringosc.spice
*
* File Location       /msd25/lind/rf/mar18run/vco
* File Created        Wed Nov 18 13:08:09 1998
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options     -h -mm -n -M -N -V -gc -m -n -mg -M -N -h
*

** Subcircuit definition for nmos_cs_inv
** Extraction file is /msd25/lind/rf/mar18run/vco/nmos_cs_inv.ext
.SUBCKT nmos_cs_inv mid vp Vdd 4 out in GND
M1 mid in GND GND CMOSN M=2 W=4.20U L=0.70U GEO=0
M2 out mid GND GND CMOSN M=2 W=4.20U L=0.70U GEO=0
M11 mid vp Vdd 4 CMOSP M=2 W=10.50U L=0.70U GEO=0
M12 out vp Vdd 4 CMOSP M=2 W=10.50U L=0.70U GEO=0
C1 Vdd out 1.0F
C2 Vdd mid 1.0F
C3 out GND 2.0F
C4 out 4 27.0F
C5 mid GND 2.0F
C6 Vdd vp 2.0F
C7 mid 4 27.0F
C8 Vdd 4 88.0F
C9 vp 0 5.0F
C10 GND 0 14.0F
C11 mid 0 9.0F
```

```
C12 out 0 6.0F
C13 Vdd 0 23.0F
C14 in 0 4.0F
*** Node Listing for subckt:  nmos_cs_inv
** N0                  == IdealGND
** N4          [U=3]   == 6_288_118#
************************************************************
** GND          [U=5]
** in           [U=2]
** mid          [U=4]
** out          [U=3]
** Vdd          [U=3]
** vp           [U=3]
.ENDS

** Subcircuit definition for nmosringb
** Extraction file is /msd25/lind/rf/mar18run/vco/nmosringb.ext
.SUBCKT nmosringb out 2 Vdd GND 5 vp
** Instance-id:nmos_cs_inv_0
X1 5 vp Vdd Vdd 2 out GND nmos_cs_inv
M1 out 2 Vdd Vdd CMOSP M=2 W=12.25U L=0.70U GEO=0
M2 out 2 GND GND CMOSN M=2 W=4.20U L=0.70U GEO=0
C1 out GND 3.0F
C2 out Vdd 31.0F
C3 Vdd vp 1.0F
C4 vp 0 2.0F
C5 GND 0 33.0F
C6 Vdd 0 42.0F
C7 out 0 28.0F
C8 2 0 5.0F
*** Node Listing for subckt:  nmosringb
** N0                  == IdealGND
** N2          [U=4]   == nmos_cs_inv_0/$out
** N5          [U=2]   == nmos_cs_inv_0/$mid
************************************************************
** GND          [U=4]
** out          [U=4]
** Vdd          [U=5]
** vp           [U=2]
.ENDS
****** top level cell is /msd25/lind/rf/mar18run/vco/ringosc.ext
** Instance-id:nmosringb_0
X1 csout cs2 Vdd Gnd cs1 Vbias nmosringb
M4 2 csout Vdd Vdd CMOSP M=2 W=33.60U L=0.70U GEO=0
```

```
M4a Vout 2 Vdd Vdd CMOSP M=6 W=33.60U L=0.70U GEO=0
M7 2 csout Gnd Gnd CMOSN M=2 W=9.45U L=0.70U GEO=0
M7a Vout 2 Gnd Gnd CMOSN M=6 W=9.45U L=0.70U GEO=0
C1 csout Gnd 1.0F
C2 Gnd csout 2.0F
C3 csout Gnd 1.0F
C4 csout 2 1.0F
C5 2 Gnd 4.0F
C6 Vout Gnd 13.0F
C7 2 Vout 5.0F
C8 2 Vdd 85.0F
C9 Vdd Vout 256.0F
C10 Gnd 0 51.0F
C11 Vdd 0 184.0F
C12 csout 0 9.0F
C13 Vout 0 29.0F
C14 cs1 0 1.0F
C15 cs2 0 1.0F
C16 2 0 18.0F
C17 Vbias 0 1.0F
*** Node Listing for subckt:  ringosc
** N0                  == IdealGND
** N2          [U=4]   == 8_96_247#
************************************************************
** cs1         [U=1]
** cs2         [U=1]
** csout       [U=3]
** Gnd         [U=5]
** Vbias       [U=1]
** Vdd         [U=5]
** Vout        [U=2]
************************************************************

* VCO_bias.mag: Simulation
* File created on Thu Nov 19 21:44:58 1998

.include 'VCO_bias.mag.spice'

.include 'n56s.mod'


**************************************************
*
* Author(s): Ryan E. Lind
```

```
* Description: VCO Simulation
*
**************************************************
*
**************************************************
Vdd Vdd 0 3.3 *pulse(0 3.3 10n 1n 5n 10 20)
Vgnd GND 0 dc 0

vt  200 0 1.524
rt  200 0 1K

vm  300 0 1.452
rm  300 0 1K

vb  400 0 1.38
rb  400 0 1K


Vref VREF 0 dc 1.65
Vvco VCO_CONTROL 0 dc 1.65 pulse(3.3 0.0 100n 1m 50n 1n 2m)

Rtune 0  I_max 634K
Roffset Vdd I_offset 53.6K

Vstby STANDBY_bar 0  3.3 *pulse(0 3.3 20n 1n 1n 1 2)

*Rp Vp 0 1MEG

.tran 1u 1m
.op
**************************************************

.options post


.END

* VCO_bias.mag.spice
*
* File Location       /msd25/lind/rf/mar18run/vco
* File Created        Thu Nov 19 21:44:58 1998
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options     -h -mm -n -M -N -V -gc -m -n -mg -M -N -h
*
```

```
****** top level cell is /msd25/lind/rf/mar18run/vco/VCO_bias.mag.ext
M1 2 2 Vdd Vdd CMOSP W=28.00U L=4.20U GEO=0
M2 diff_S 2 Vdd Vdd CMOSP M=2 W=70.00U L=4.20U GEO=0
M3 Vp Vp Vdd Vdd CMOSP M=2 W=3.85U L=2.10U GEO=0
M5 LEFT_diff VCO_Control diff_S Vdd CMOSP M=4 W=17.50U L=3.50U GEO=0
M6 7 Vref diff_S Vdd CMOSP M=4 W=17.50U L=3.50U GEO=0
M8 LEFT_diff LEFT_diff GND GND CMOSN W=35.00U L=2.10U GEO=0
M9 7 7 GND GND CMOSN W=35.00U L=2.10U GEO=0
M10 Vp 7 GND GND CMOSN W=35.00U L=2.10U GEO=0
MSB1 Vp STANDBY_bar Vdd Vdd CMOSP W=4.20U L=5.25U GEO=0
MSB2 2 STANDBY_bar Vdd Vdd CMOSP W=2.10U L=4.20U GEO=0
MSB3 2 STANDBY_bar I_max GND CMOSN W=32.20U L=0.70U GEO=0
MSB4 I_Offset STANDBY_bar 7 GND CMOSN W=32.20U L=0.70U GEO=0
M_C1 Vdd 2 Vdd Vdd CMOSP W=27.65U L=16.80U GEO=0
M_C2 Vdd Vp Vdd Vdd CMOSP W=21.35U L=57.05U GEO=0
M_C3 GND 7 GND GND CMOSN W=17.50U L=36.40U GEO=0
C1 diff_S Vref 6.0F
C2 2 Vdd 83.0F
C3 2 I_Offset 2.0F
C4 2 Vref 2.0F
C5 diff_S VCO_Control 6.0F
C6 Vp GND 14.0F
C7 GND I_max 12.0F
C8 diff_S STANDBY_bar 2.0F
C9 2 VCO_Control 2.0F
C10 Vp Vdd 26.0F
C11 7 GND 28.0F
C12 2 STANDBY_bar 3.0F
C13 7 Vdd 91.0F
C14 LEFT_diff GND 14.0F
C15 GND I_Offset 12.0F
C16 Vref 7 1.0F
C17 LEFT_diff Vdd 91.0F
C18 VCO_Control LEFT_diff 1.0F
C19 2 7 2.0F
C20 diff_S Vdd 605.0F
C21 2 GND 12.0F
C22 7 0 103.0F
C23 diff_S 0 140.0F
C24 GND 0 241.0F
C25 Vdd 0 444.0F
C26 VCO_Control 0 58.0F
C27 I_Offset 0 25.0F
C28 2 0 84.0F
```

```
C29 I_max 0 33.0F
C30 Vref 0 59.0F
C31 LEFT_diff 0 66.0F
C32 STANDBY_bar 0 89.0F
C33 Vp 0 45.0F
*** Node Listing for subckt:  VCO_bias.mag
** N0                  == IdealGND
** N2           [U=6]   == 8_1191_767#
** N7           [U=6]   == Vn
*****************************************************************
** diff_S        [U=3]
** GND           [U=11]
** I_max         [U=1]
** I_Offset      [U=1]
** LEFT_diff     [U=3]
** STANDBY_bar   [U=4]
** VCO_Control   [U=1]
** Vdd           [U=18]
** Vp            [U=5]
** Vref          [U=1]
*****************************************************************

* vco1c: Simulation
* File created on Fri Feb 27 15:33:56 1998

.include 'vco1c.spice'

.include 'n56s.mod'


*****************************************************
*
* Author(s): Ryan E. Lind
* Description: VCO Simulation
*
*****************************************************
*
*****************************************************
Vdd Vdd 0 3.3 pulse(0 3.3 10n 1n 5n 10 20)
Vgnd GND 0 dc 0

Vref VREF 0 dc 1.65
Vvco VCO_CONTROL 0 dc 1.65 *pulse(1.9328 1.3671 100n 1800n 50n 1n 2u)
```

```
Rtune 0  I_max 634K
Roffset Vdd I_offset 53.6K

Vstby STANDBY_bar 0  3.3 pulse(0 3.3 20n 1n 1n 1 2)

cl  VCO_out 0 .5pF 10K 200K

.tran .1n 1u
.op
*****************************************************

.options post


.END

* vco1c.spice
*
* File Location       /msd25/lind/rf/mar18run/vco
* File Created        Tue Nov 17 15:27:18 1998
* Ext2spice Version    ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options    -h -mm -n -M -N -V -gc -m -n -mg -M -N -h
*

** Subcircuit definition for nmos_cs_inv
** Extraction file is /msd25/lind/rf/mar18run/vco/nmos_cs_inv.ext
.SUBCKT nmos_cs_inv mid vp Vdd 4 out in GND
M1 mid in GND GND CMOSN M=2 W=4.20U L=0.70U GEO=0
M2 out mid GND GND CMOSN M=2 W=4.20U L=0.70U GEO=0
M11 mid vp Vdd 4 CMOSP M=2 W=10.50U L=0.70U GEO=0
M12 out vp Vdd 4 CMOSP M=2 W=10.50U L=0.70U GEO=0
C1 4 Vdd 88.0F
C2 Vdd out 1.0F
C3 Vdd mid 1.0F
C4 GND out 2.0F
C5 4 out 27.0F
C6 GND mid 2.0F
C7 vp Vdd 2.0F
C8 4 mid 27.0F
C9 vp 0 5.0F
C10 GND 0 14.0F
C11 mid 0 9.0F
C12 out 0 6.0F
C13 Vdd 0 23.0F
```

```
C14 in 0 4.0F
*** Node Listing for subckt:  nmos_cs_inv
** N0                    == IdealGND
** N4            [U=3]    == 6_288_118#
*************************************************************
** GND            [U=5]
** in            [U=2]
** mid            [U=4]
** out            [U=3]
** Vdd            [U=3]
** vp            [U=3]
.ENDS

** Subcircuit definition for nmosringb
** Extraction file is /msd25/lind/rf/mar18run/vco/nmosringb.ext
.SUBCKT nmosringb out 2 Vdd GND 5 vp
** Instance-id:nmos_cs_inv_0
X1 5 vp Vdd Vdd 2 out GND nmos_cs_inv
M1 out 2 Vdd Vdd CMOSP M=2 W=12.25U L=0.70U GEO=0
M2 out 2 GND GND CMOSN M=2 W=4.20U L=0.70U GEO=0
C1 GND out 3.0F
C2 Vdd out 31.0F
C3 Vdd vp 1.0F
C4 vp 0 2.0F
C5 GND 0 33.0F
C6 Vdd 0 42.0F
C7 out 0 28.0F
C8 2 0 5.0F
*** Node Listing for subckt:  nmosringb
** N0                    == IdealGND
** N2            [U=4]    == nmos_cs_inv_0/$out
** N5            [U=2]    == nmos_cs_inv_0/$mid
*************************************************************
** GND            [U=4]
** out            [U=4]
** Vdd            [U=5]
** vp            [U=2]
.ENDS

** Subcircuit definition for vcoc
** Extraction file is /msd25/lind/rf/mar18run/vco/vcoc.ext
.SUBCKT vcoc Vdd STANDBY_bar VCO_Control Vref Vp I_Offset GND I_max out
+ out1 16 17 18
X1 out1 17 Vdd GND 18 Vp nmosringb
```

```
M1 2 2 Vdd Vdd CMOSP W=28.00U L=4.20U GEO=0
M2 diff_S 2 Vdd Vdd CMOSP M=2 W=70.00U L=4.20U GEO=0
M3 Vp Vp Vdd Vdd CMOSP M=2 W=3.85U L=2.10U GEO=0
M4 14 out1 16 16 CMOSP M=2 W=33.60U L=0.70U GEO=0
M4a out 14 16 16 CMOSP M=6 W=33.60U L=0.70U GEO=0
M5 LEFT_diff VCO_Control diff_S Vdd CMOSP M=4 W=17.50U L=3.50U GEO=0
M6 7 Vref diff_S Vdd CMOSP M=4 W=17.50U L=3.50U GEO=0
M7 14 out1 GND GND CMOSN M=2 W=9.45U L=0.70U GEO=0
M7a out 14 GND GND CMOSN M=6 W=9.45U L=0.70U GEO=0
M8 LEFT_diff LEFT_diff GND GND CMOSN W=35.00U L=2.10U GEO=0
M9 7 7 GND GND CMOSN W=35.00U L=2.10U GEO=0
M10 Vp 7 GND GND CMOSN W=35.00U L=2.10U GEO=0
MSB1 Vp STANDBY_bar Vdd Vdd CMOSP W=4.20U L=5.25U GEO=0
MSB2 2 STANDBY_bar Vdd Vdd CMOSP W=2.10U L=4.20U GEO=0
MSB3 2 STANDBY_bar I_max GND CMOSN W=32.20U L=0.70U GEO=0
MSB4 I_Offset STANDBY_bar 7 GND CMOSN W=32.20U L=0.70U GEO=0
M_C1 Vdd 2 Vdd Vdd CMOSP W=27.65U L=16.80U GEO=0
M_C2 Vdd Vp Vdd Vdd CMOSP W=21.35U L=57.05U GEO=0
M_C3 GND 7 GND GND CMOSN W=17.50U L=36.40U GEO=0
C1 GND 14 4.0F
C2 Vdd LEFT_diff 91.0F
C3 2 STANDBY_bar 3.0F
C4 VCO_Control diff_S 6.0F
C5 2 7 2.0F
C6 LEFT_diff VCO_Control 1.0F
C7 I_Offset GND 12.0F
C8 STANDBY_bar diff_S 2.0F
C9 16 out 256.0F
C10 GND Vp 14.0F
C11 2 GND 12.0F
C12 Vdd Vp 27.0F
C13 GND 7 28.0F
C14 GND out 13.0F
C15 2 Vref 2.0F
C16 2 Vdd 83.0F
C17 out 14 5.0F
C18 7 Vref 1.0F
C19 I_Offset 2 2.0F
C20 Vdd 7 91.0F
C21 GND LEFT_diff 14.0F
C22 16 14 85.0F
C23 2 VCO_Control 2.0F
C24 GND out1 2.0F
C25 Vref diff_S 6.0F
```

```
C26 out1 14 1.0F
C27 Vdd diff_S 605.0F
C28 I_max GND 12.0F
C29 7 0 103.0F
C30 diff_S 0 140.0F
C31 GND 0 343.0F
C32 Vdd 0 505.0F
C33 VCO_Control 0 57.0F
C34 I_Offset 0 24.0F
C35 I_max 0 33.0F
C36 out 0 29.0F
C37 2 0 84.0F
C38 16 0 122.0F
C39 14 0 18.0F
C40 Vref 0 57.0F
C41 LEFT_diff 0 66.0F
C42 STANDBY_bar 0 86.0F
C43 Vp 0 46.0F
C44 out1 0 11.0F
*** Node Listing for subckt:  vcoc
** N0                  == IdealGND
** N2          [U=6]   == 8_456_442#
** N7          [U=6]   == Vn
** N14         [U=4]   == 8_1498_58#
** N16         [U=5]   == 6_1472_44#
** N17         [U=2]   == X1/nmos_cs_inv_0/$out
** N18         [U=2]   == X1/nmos_cs_inv_0/$mid
************************************************************
** diff_S       [U=3]
** GND          [U=17]
** I_max        [U=2]
** I_Offset     [U=2]
** LEFT_diff    [U=3]
** out          [U=3]
** out1         [U=4]
** STANDBY_bar  [U=5]
** VCO_Control  [U=2]
** Vdd          [U=20]
** Vp           [U=7]
** Vref         [U=2]
.ENDS
****** top level cell is /msd25/lind/rf/mar18run/vco/vco1c.ext
X1 Vdd STANDBY_bar VCO_CONTROL VREF Vp I_OFFSET GND I_max VCO_out
buff_out
```

```
+ Vdd cs2 cs1 vcoc
C1 VCO_out 0 3.0F
C2 buff_out 0 1.0F
C3 GND 0 78.0F
C4 VCO_CONTROL 0 3.0F
C5 I_OFFSET 0 3.0F
C6 I_max 0 3.0F
C7 VREF 0 3.0F
C8 STANDBY_bar 0 4.0F
C9 Vp 0 1.0F
C10 cs1 0 1.0F
C11 cs2 0 1.0F
C12 Vdd 0 486.0F
*** Node Listing for subckt:  vco1c
** N0                    == IdealGND
************************************************************
** buff_out        [U=1]
** cs1             [U=1]
** cs2             [U=1]
** GND             [U=1]
** I_max           [U=1]
** I_OFFSET        [U=1]
** STANDBY_bar     [U=1]
** VCO_CONTROL     [U=1]
** VCO_out         [U=1]
** Vdd             [U=2]
** Vp              [U=1]
** VREF            [U=1]
************************************************************

* PFD: Simulation
* File created on Sun Nov 22 20:30:40 1998

.include 'PFD.spice'
.include 'n56s.mod'

*****************************************************
*
* Author(s): Ryan E. Lind
* Description: PLL Correction mode test
*
*****************************************************
Vdd Vdd 0 dc 3.3 pulse(0 3.3 10n 1n 5n 10 20)
Vss Gnd 0 dc 0.0
```

```
*PFD Clocking Signals
Vref fref 0 dc 0.0 pulse(0 3.3 137.7n 1n 1n 137.7n 277.4n)
Vdiv div256 0 dc 0.0 pulse(0 3.3 131n 1n 1n 131n 264n) *high range

* Loop Filter
Rlf1 PFD_out 50 234K
Rlf2 50 51 56K
Clf 51 0 0.0001uF


Venable enable 0  3.3
.ic V(50)=1.65

.tran .1u 10u
.op
*****************************************************
.options POST
.options METHOD=GEAR


Vsub Vsub 0 DC 0V $NWell Process


.end

* PFD.spice
*
* File Location       /msd25/lind/rf/mar18run/PLL
* File Created        Sun Nov 22 20:30:40 1998
* Ext2spice Version   ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options    -h -mm -n -M -N -V -gc -m -n -mg -M -N -h
*

** Subcircuit definition for nanf211
** Extraction file is /msd25/lind/rf/mar18run/PLL/nanf211.ext
.SUBCKT nanf211 2 3 4 5 7
M1 1 2 3 3 CMOSP W=8.05U L=0.70U GEO=0
M2 1 4 3 3 CMOSP W=8.05U L=0.70U GEO=0
M3 5 1 3 3 CMOSP W=9.10U L=0.70U GEO=0
M4 1 2 6 7 CMOSN W=7.35U L=0.70U GEO=0
M5 6 4 7 7 CMOSN W=7.35U L=0.70U GEO=0
M6 5 1 7 7 CMOSN W=4.90U L=0.70U GEO=0
C1 5 7 2.0F
```

```
C2 1 2 1.0F
C3 5 3 18.0F
C4 1 7 3.0F
C5 1 3 21.0F
C6 6 7 1.0F
C7 1 4 1.0F
C8 4 0 3.0F
C9 2 0 3.0F
C10 1 0 7.0F
C11 5 0 4.0F
C12 7 0 5.0F
C13 3 0 6.0F
*** Node Listing for subckt:  nanf211
** N0                  == IdealGND
** N1          [U=5]   == O1
** N2          [U=3]   == A1
** N3          [U=7]   == Vdd!
** N4          [U=3]   == B1
** N5          [U=3]   == O2
** N6          [U=2]   == 150
** N7          [U=6]   == GND!
.ENDS

** Subcircuit definition for nanf301
** Extraction file is /msd25/lind/rf/mar18run/PLL/nanf301.ext
.SUBCKT nanf301 1 2 3 4 5 7
M1 1 2 3 3 CMOSP W=8.40U L=0.70U GEO=0
M2 1 4 3 3 CMOSP W=8.40U L=0.70U GEO=0
M3 1 5 3 3 CMOSP W=8.40U L=0.70U GEO=0
M4 6 2 7 7 CMOSN W=8.05U L=0.70U GEO=0
M5 6 4 8 7 CMOSN W=8.05U L=0.70U GEO=0
M6 8 5 1 7 CMOSN W=8.05U L=0.70U GEO=0
C1 1 7 3.0F
C2 1 3 37.0F
C3 1 5 1.0F
C4 8 7 1.0F
C5 1 4 1.0F
C6 6 7 1.0F
C7 1 0 6.0F
C8 5 0 3.0F
C9 2 0 3.0F
C10 4 0 3.0F
C11 7 0 5.0F
C12 3 0 6.0F
```

```
*** Node Listing for subckt:  nanf301
** N0                  == IdealGND
** N1          [U=5]   == O
** N2          [U=3]   == A1
** N3          [U=7]   == Vdd!
** N4          [U=3]   == B1
** N5          [U=3]   == C1
** N6          [U=2]   == 150
** N7          [U=5]   == GND!
** N8          [U=2]   == 151
.ENDS

** Subcircuit definition for norf211
** Extraction file is /msd25/lind/rf/mar18run/PLL/norf211.ext
.SUBCKT norf211 2 4 5 6 7
M1 1 2 3 4 CMOSP W=10.50U L=0.70U GEO=0
M2 3 5 4 4 CMOSP W=10.50U L=0.70U GEO=0
M3 6 1 4 4 CMOSP W=10.85U L=0.70U GEO=0
M4 1 2 7 7 CMOSN W=2.80U L=0.70U GEO=0
M5 1 5 7 7 CMOSN W=2.80U L=0.70U GEO=0
M6 6 1 7 7 CMOSN W=5.95U L=0.70U GEO=0
C1 6 4 21.0F
C2 3 4 9.0F
C3 1 7 2.0F
C4 1 4 21.0F
C5 6 7 2.0F
C6 2 0 3.0F
C7 5 0 3.0F
C8 6 0 4.0F
C9 1 0 9.0F
C10 7 0 7.0F
C11 4 0 8.0F
*** Node Listing for subckt:  norf211
** N0                  == IdealGND
** N1          [U=5]   == O2
** N2          [U=3]   == A1
** N3          [U=2]   == 120
** N4          [U=6]   == Vdd!
** N5          [U=3]   == B1
** N6          [U=3]   == O1
** N7          [U=7]   == GND!
.ENDS

** Subcircuit definition for norf201
```

```
** Extraction file is /msd25/lind/rf/mar18run/PLL/norf201.ext
.SUBCKT norf201 1 2 4 5 6
M1 1 2 3 4 CMOSP W=10.85U L=0.70U GEO=0
M2 3 5 4 4 CMOSP W=10.85U L=0.70U GEO=0
M3 1 2 6 6 CMOSN W=2.80U L=0.70U GEO=0
M4 1 5 6 6 CMOSN W=2.80U L=0.70U GEO=0
C1 3 4 9.0F
C2 1 6 1.0F
C3 1 4 20.0F
C4 1 0 4.0F
C5 2 0 2.0F
C6 5 0 3.0F
C7 6 0 4.0F
C8 4 0 5.0F
*** Node Listing for subckt:  norf201
** N0                 == IdealGND
** N1          [U=4]   == O
** N2          [U=3]   == A1
** N3          [U=2]   == 120
** N4          [U=4]   == Vdd!
** N5          [U=3]   == B1
** N6          [U=5]   == GND!
.ENDS

** Subcircuit definition for dfrf311
** Extraction file is /msd25/lind/rf/mar18run/PLL/dfrf311.ext
.SUBCKT dfrf311 2 3 4 6 10 11 15 16
M1 1 2 3 3 CMOSP W=10.15U L=0.70U GEO=0
M2 4 1 3 3 CMOSP W=10.15U L=0.70U GEO=0
M3 5 6 3 3 CMOSP W=9.10U L=0.70U GEO=0
M4 5 1 7 3 CMOSP W=9.10U L=0.70U GEO=0
M5 7 4 8 3 CMOSP W=7.70U L=0.70U GEO=0
M6 8 9 3 3 CMOSP W=7.70U L=0.70U GEO=0
M7 8 10 3 3 CMOSP W=7.70U L=0.70U GEO=0
M8 9 7 3 3 CMOSP W=7.70U L=0.70U GEO=0
M9 1 2 11 11 CMOSN W=8.40U L=0.70U GEO=0
M10 4 1 11 11 CMOSN W=8.40U L=0.70U GEO=0
M11 12 9 3 3 CMOSP W=7.35U L=0.70U GEO=0
M12 12 4 13 3 CMOSP W=7.35U L=0.70U GEO=0
M13 14 1 3 3 CMOSP W=10.50U L=0.70U GEO=0
M14 14 15 13 3 CMOSP W=10.50U L=0.70U GEO=0
M15 13 10 3 3 CMOSP W=10.85U L=0.70U GEO=0
M16 15 13 3 3 CMOSP W=10.85U L=0.70U GEO=0
M17 16 15 3 3 CMOSP W=10.15U L=0.70U GEO=0
```

```
M18 17 6 11 11 CMOSN W=6.65U L=0.70U GEO=0
M19 17 4 7 11 CMOSN W=6.65U L=0.70U GEO=0
M20 7 10 18 11 CMOSN W=5.25U L=0.70U GEO=0
M21 18 9 19 11 CMOSN W=5.25U L=0.70U GEO=0
M22 19 1 11 11 CMOSN W=5.25U L=0.70U GEO=0
M23 9 7 11 11 CMOSN W=5.25U L=0.70U GEO=0
M24 20 9 11 11 CMOSN W=4.55U L=0.70U GEO=0
M25 20 10 21 11 CMOSN W=4.55U L=0.70U GEO=0
M26 21 1 13 11 CMOSN W=4.55U L=0.70U GEO=0
M27 13 4 22 11 CMOSN W=5.95U L=0.70U GEO=0
M28 22 15 23 11 CMOSN W=5.95U L=0.70U GEO=0
M29 23 10 11 11 CMOSN W=5.95U L=0.70U GEO=0
M30 15 13 11 11 CMOSN W=7.35U L=0.70U GEO=0
M31 16 15 11 11 CMOSN W=4.20U L=0.70U GEO=0
C1 20 11 1.0F
C2 9 3 15.0F
C3 7 11 4.0F
C4 16 3 20.0F
C5 4 11 3.0F
C6 15 3 21.0F
C7 19 11 1.0F
C8 7 3 23.0F
C9 23 11 1.0F
C10 14 3 9.0F
C11 9 1 2.0F
C12 4 3 17.0F
C13 18 11 1.0F
C14 5 3 8.0F
C15 13 11 4.0F
C16 22 11 1.0F
C17 12 3 6.0F
C18 13 4 1.0F
C19 1 11 4.0F
C20 17 11 1.0F
C21 13 3 40.0F
C22 10 11 2.0F
C23 21 11 1.0F
C24 9 7 1.0F
C25 8 3 33.0F
C26 9 11 2.0F
C27 1 3 19.0F
C28 2 11 1.0F
C29 16 11 2.0F
C30 15 11 3.0F
```

```
C31 10 3 1.0F
C32 16 0 4.0F
C33 15 0 9.0F
C34 9 0 9.0F
C35 4 0 9.0F
C36 7 0 11.0F
C37 1 0 22.0F
C38 13 0 9.0F
C39 10 0 14.0F
C40 6 0 3.0F
C41 11 0 23.0F
C42 2 0 3.0F
C43 3 0 26.0F
C44 8 0 2.0F
*** Node Listing for subckt:  dfrf311
** N0                  == IdealGND
** N1          [U=8]   == 21
** N2          [U=3]   == CLK2
** N3          [U=27]  == Vdd!
** N4          [U=7]   == 25
** N5          [U=2]   == 120
** N6          [U=3]   == DATA1
** N7          [U=6]   == 22
** N8          [U=3]   == 121
** N9          [U=6]   == 24
** N10         [U=6]   == RST3
** N11         [U=26]  == GND!
** N12         [U=2]   == 123
** N13         [U=7]   == 28
** N14         [U=2]   == 124
** N15         [U=7]   == Q
** N16         [U=3]   == Q_b
** N17         [U=2]   == 150
** N18         [U=2]   == 152
** N19         [U=2]   == 151
** N20         [U=2]   == 153
** N21         [U=2]   == 154
** N22         [U=2]   == 155
** N23         [U=2]   == 156
.ENDS

** Subcircuit definition for invf103
** Extraction file is /msd25/lind/rf/mar18run/PLL/invf103.ext
.SUBCKT invf103 1 2 3 4
```

```
M1 1 2 3 3 CMOSP M=3 W=8.75U L=0.70U GEO=0
M2 1 2 4 4 CMOSN M=3 W=4.20U L=0.70U GEO=0
C1 2 3 1.0F
C2 1 2 1.0F
C3 1 4 4.0F
C4 1 3 41.0F
C5 1 0 7.0F
C6 2 0 5.0F
C7 4 0 5.0F
C8 3 0 7.0F
*** Node Listing for subckt:  invf103
** N0                  == IdealGND
** N1          [U=3]   == O
** N2          [U=3]   == A1
** N3          [U=3]   == Vdd!
** N4          [U=3]   == GND!
.ENDS

** Subcircuit definition for invf101
** Extraction file is /msd25/lind/rf/mar18run/PLL/invf101.ext
.SUBCKT invf101 1 2 3 4
M1 1 2 3 3 CMOSP W=9.10U L=0.70U GEO=0
M2 1 2 4 4 CMOSN W=4.20U L=0.70U GEO=0
C1 1 4 2.0F
C2 1 3 18.0F
C3 1 0 4.0F
C4 2 0 3.0F
C5 4 0 3.0F
C6 3 0 4.0F
*** Node Listing for subckt:  invf101
** N0                  == IdealGND
** N1          [U=3]   == O
** N2          [U=3]   == A1
** N3          [U=3]   == Vdd!
** N4          [U=3]   == GND!
.ENDS

** Subcircuit definition for phfdet2
** Extraction file is /msd25/lind/rf/mar18run/PLL/phfdet2.ext
.SUBCKT phfdet2 PH_OUT VDD GND 6 F_REF ENABLE 9 RF_IN
** Instance-id:nanf211_0
X1 11 VDD 9 4 GND nanf211
** Instance-id:norf201_1
X2 11 12 VDD 13 GND norf201
```

```
** Instance-id:dfrf311_1
X3 14 VDD 15 VDD RESET GND 17 12 dfrf311
** Instance-id:invf103_2
X4 14 18 VDD GND invf103
** Instance-id:invf101_1
X5 18 F_REF VDD GND invf101
** Instance-id:invf101_5
X6 19 9 VDD GND invf101
** Instance-id:norf201_2
X7 6 UP_BAR VDD 11 GND norf201
** Instance-id:invf101_4
X8 UP_BAR 21 VDD GND invf101
** Instance-id:invf101_3
X9 13 22 VDD GND invf101
** Instance-id:invf101_2
X10 23 12 VDD GND invf101
** Instance-id:nanf301_0
X11 RESET 24 VDD 17 ENABLE GND nanf301
** Instance-id:norf211_0
X12 21 VDD 19 UP GND norf211
** Instance-id:invf103_1
X13 21 25 VDD GND invf103
** Instance-id:norf201_0
X14 25 22 VDD 23 GND norf201
** Instance-id:dfrf311_0
X15 26 VDD 27 VDD RESET GND 24 22 dfrf311
** Instance-id:invf103_0
X16 26 28 VDD GND invf103
** Instance-id:invf101_0
X17 28 RF_IN VDD GND invf101
M1 PH_OUT 4 GND GND CMOSN M=4 W=6.30U L=1.40U GEO=0
M2 PH_OUT UP VDD VDD CMOSP M=4 W=11.90U L=1.40U GEO=0
C1 12 VDD 1.0F
C2 PH_OUT UP 1.0F
C3 4 PH_OUT 1.0F
C4 11 VDD 1.0F
C5 PH_OUT VDD 65.0F
C6 PH_OUT GND 8.0F
C7 6 VDD 1.0F
C8 GND VDD 2.0F
C9 9 0 8.0F
C10 F_REF 0 2.0F
C11 25 0 5.0F
C12 UP_BAR 0 2.0F
```

```
C13 26 0 3.0F
C14 4 0 9.0F
C15 24 0 7.0F
C16 RF_IN 0 2.0F
C17 13 0 9.0F
C18 23 0 11.0F
C19 GND 0 93.0F
C20 22 0 8.0F
C21 RESET 0 27.0F
C22 12 0 10.0F
C23 21 0 10.0F
C24 UP 0 10.0F
C25 11 0 15.0F
C26 VDD 0 129.0F
C27 27 0 4.0F
C28 PH_OUT 0 112.0F
C29 18 0 3.0F
C30 14 0 3.0F
C31 28 0 3.0F
C32 17 0 8.0F
C33 6 0 18.0F
C34 19 0 7.0F
C35 15 0 4.0F
C36 ENABLE 0 2.0F
*** Node Listing for subckt:  phfdet2
** N0                  == IdealGND
** N4          [U=2]   == nanf211_0/O2
** N6          [U=2]   == norf201_2/O
** N9          [U=3]   == invf101_5/A1
** N11         [U=3]   == norf201_1/O
** N12         [U=3]   == dfrf311_1/Q_b
** N13         [U=2]   == invf101_3/O
** N14         [U=2]   == invf103_2/O
** N15         [U=1]   == dfrf311_1/25
** N17         [U=2]   == dfrf311_1/Q
** N18         [U=2]   == invf101_1/O
** N19         [U=2]   == invf101_5/O
** N21         [U=3]   == invf103_1/O
** N22         [U=3]   == dfrf311_0/Q_b
** N23         [U=2]   == invf101_2/O
** N24         [U=2]   == dfrf311_0/Q
** N25         [U=2]   == norf201_0/O
** N26         [U=2]   == invf103_0/O
** N27         [U=1]   == dfrf311_0/25
```

```
** N28          [U=2]    == invf101_0/O
*********************************************************
** ENABLE        [U=2]
** F_REF         [U=2]
** GND           [U=20]
** PH_OUT        [U=3]
** RESET         [U=3]
** RF_IN         [U=2]
** UP            [U=2]
** UP_BAR        [U=2]
** VDD           [U=22]
.ENDS

** Subcircuit definition for phasedet4
** Extraction file is /msd25/lind/rf/mar18run/PLL/phasedet4.ext
.SUBCKT phasedet4 LOCK_DET F_REF_IN 3 PWR_EN enable PH_OUT RF_IN 8
** Instance-id:phfdet2_0
X1 PH_OUT 8 3 LOCK_DET F_REF_IN enable PWR_EN RF_IN phfdet2
C1 PWR_EN PH_OUT 1.0F
C2 enable 0 21.0F
C3 LOCK_DET 0 40.0F
C4 RF_IN 0 5.0F
C5 F_REF_IN 0 5.0F
C6 PWR_EN 0 60.0F
C7 PH_OUT 0 88.0F
*** Node Listing for subckt:  phasedet4
** N0                 == IdealGND
** N3           [U=2]    == phfdet2_0/$GND
** N8           [U=2]    == phfdet2_0/$VDD
*********************************************************
** enable        [U=2]
** F_REF_IN      [U=2]
** LOCK_DET      [U=2]
** PH_OUT        [U=2]
** PWR_EN        [U=2]
** RF_IN         [U=2]
.ENDS
****** top level cell is /msd25/lind/rf/mar18run/PLL/PFD.ext
** Instance-id:phasedet4_0
X1 lock div256 Gnd enable enable PFD_out fref Vdd phasedet4
C1 div256 0 1.0F
C2 enable 0 19.0F
C3 Vdd 0 9.0F
C4 Gnd 0 5.0F
```

```
C5 fref 0 1.0F
C6 PFD_out 0 14.0F
C7 lock 0 1.0F
*** Node Listing for subckt:  PFD
** N0                    == IdealGND
*****************************************************************
** div256          [U=1]
** enable          [U=2]
** fref            [U=1]
** Gnd             [U=1]
** lock            [U=1]
** PFD_out         [U=1]
** Vdd             [U=1]
*****************************************************************

* mix_se: Simulation
* File created on Tue Nov 24 18:04:10 1998

.include 'mix_se.spice'
.include 'n56s.mod'

*****************************************************
*
* Author(s): Ryan E. Lind
* Description: Single Ended Mixer Drive from VCO
*
*****************************************************
****************************
*Ib  0  Ibias  100uA
Ib  0  Ibias  1000uA
****************************
v1  DI  0  dc  3.3  pulse (3.3 0 40n .1n .1n 40n 81n)
v2  DI_bar  0  dc  0    pulse (0 3.3 40n .1n .1n 40n 81n)
****************************
vrf_dc  carrier_dc_bias  0  dc  1.65
vrf  PLL  0  dc  1.65  ac 1 sin(1.65 1.65 916e6 0 0)
****************************
vdd  Vdd  0  dc 3.3
vgnd Gnd  0  dc 0
****************************
venable  enable  0  dc 3.3  *pulse (3.3 0 20n .1n .1n 50n 100n)
****************************
rloada 12  0  50
rloadb 10  0  50
```

```
.options post
.op
.tran  0.01n 80n .1n

*** Node Listing for subckt:  mix_se
** N0                    == IdealGND
** N2            [U=4]    == 8_327_248#
*****************************************************************
** 10            [U=1]
** 12            [U=1]
** carrier_dc_bias  [U=1]
** DI            [U=1]
** DI_bar          [U=1]
** enable          [U=1]
** Gnd             [U=5]
** Ibias           [U=1]
** VCO_out             [U=3]
** PLL             [U=2]
** Vdd             [U=5]
************************************************
.END

* mix_se.spice
*
* File Location       /msd25/lind/rf/mar18run/vco
* File Created        Tue Nov 24 19:33:21 1998
* Ext2spice Version    ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options    -h -mm -n -M -N -V -gc -m -n -mg -M -N -h
*

** Subcircuit definition for invf101
** Extraction file is /msd25/lind/rf/mar18run/vco/invf101.ext
.SUBCKT invf101 1 2 3 4
M1 1 2 3 3 CMOSP W=9.10U L=0.70U GEO=0
M2 1 2 4 4 CMOSN W=4.20U L=0.70U GEO=0
C1 4 1 2.0F
C2 3 1 18.0F
C3 1 0 4.0F
C4 2 0 3.0F
C5 4 0 3.0F
C6 3 0 4.0F
*** Node Listing for subckt:  invf101
** N0                    == IdealGND
```

```
** N1          [U=3]   == O
** N2          [U=3]   == A1
** N3          [U=3]   == Vdd!
** N4          [U=3]   == GND!
.ENDS

** Subcircuit definition for mult_ms1
** Extraction file is /msd25/lind/rf/mar18run/vco/mult_ms1.ext
.SUBCKT mult_ms1 SDI SDI_BAR RF_IN_BAR RF_IN ibias MIX_OUT1 MIX_OUT2
pwr_en
+ Vdd GND
** Instance-id:invf101_0
X1 9 pwr_en Vdd GND invf101
M1 5 SDI 7 GND CMOSN M=16 W=14.00U L=0.70U GEO=3
M2 6 SDI_BAR 7 GND CMOSN M=16 W=14.00U L=0.70U GEO=3
M3 5 5 Vdd Vdd CMOSP M=4 W=21.00U L=0.70U GEO=3
M4 6 6 Vdd Vdd CMOSP M=4 W=21.00U L=0.70U GEO=3
M5 13 5 Vdd Vdd CMOSP M=16 W=21.00U L=0.70U GEO=3
M6 11 6 Vdd Vdd CMOSP M=16 W=21.00U L=0.70U GEO=3
M7 MIX_OUT2 RF_IN 13 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M8 MIX_OUT1 RF_IN 11 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M9 MIX_OUT1 RF_IN_BAR 13 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M10 MIX_OUT2 RF_IN_BAR 11 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M17 7 14 GND GND CMOSN M=24 W=14.00U L=0.70U GEO=3
M18 14 14 GND GND CMOSN M=4 W=14.00U L=0.70U GEO=3
M19 GND 14 GND GND CMOSN W=16.80U L=9.10U GEO=0
M20 14 9 GND GND CMOSN M=2 W=10.85U L=0.70U GEO=1
M21 ibias pwr_en 14 GND CMOSN M=12 W=9.45U L=0.70U GEO=2
C1 ibias pwr_en 6.0F
C2 MIX_OUT1 MIX_OUT2 3.0F
C3 SDI_BAR 7 10.0F
C4 RF_IN MIX_OUT2 1.0F
C5 ibias GND 26.0F
C6 5 6 1.0F
C7 7 14 2.0F
C8 RF_IN_BAR MIX_OUT2 1.0F
C9 RF_IN MIX_OUT1 1.0F
C10 Vdd 11 1610.0F
C11 GND 6 52.0F
C12 5 13 11.0F
C13 11 MIX_OUT2 1.0F
C14 RF_IN_BAR MIX_OUT1 1.0F
C15 Vdd 6 107.0F
C16 RF_IN_BAR RF_IN 5.0F
```

C17 6 MIX_OUT2 1.0F
C18 11 MIX_OUT1 1.0F
C19 Vdd 13 1610.0F
C20 GND 5 52.0F
C21 SDI GND 1.0F
C22 11 RF_IN 15.0F
C23 13 MIX_OUT2 1.0F
C24 6 MIX_OUT1 1.0F
C25 Vdd 5 107.0F
C26 SDI SDI_BAR 2.0F
C27 11 RF_IN_BAR 17.0F
C28 13 MIX_OUT1 1.0F
C29 5 MIX_OUT2 1.0F
C30 6 RF_IN 1.0F
C31 SDI_BAR GND 1.0F
C32 13 RF_IN 15.0F
C33 5 MIX_OUT1 1.0F
C34 6 RF_IN_BAR 1.0F
C35 SDI 7 10.0F
C36 14 GND 53.0F
C37 Vdd MIX_OUT2 1137.0F
C38 6 11 11.0F
C39 13 RF_IN_BAR 18.0F
C40 5 RF_IN 1.0F
C41 9 14 1.0F
C42 7 GND 190.0F
C43 Vdd MIX_OUT1 1137.0F
C44 5 RF_IN_BAR 1.0F
C45 ibias 0 33.0F
C46 GND 0 293.0F
C47 Vdd 0 562.0F
C48 pwr_en 0 30.0F
C49 MIX_OUT1 0 179.0F
C50 MIX_OUT2 0 187.0F
C51 11 0 196.0F
C52 13 0 185.0F
C53 14 0 88.0F
C54 RF_IN 0 284.0F
C55 RF_IN_BAR 0 286.0F
C56 SDI_BAR 0 80.0F
C57 SDI 0 85.0F
C58 5 0 158.0F
C59 6 0 158.0F
C60 7 0 141.0F

```
C61 9 0 9.0F
*** Node Listing for subckt:  mult_ms1
** N0                    == IdealGND
** N5            [U=4]    == N5
** N6            [U=4]    == N6
** N7            [U=3]    == N7
** N9            [U=2]    == N9
** N11           [U=3]    == N11
** N13           [U=3]    == N13
** N14           [U=6]    == N14
*****************************************************************
** GND           [U=14]
** ibias         [U=2]
** MIX_OUT1      [U=3]
** MIX_OUT2      [U=3]
** pwr_en        [U=3]
** RF_IN         [U=3]
** RF_IN_BAR     [U=3]
** SDI           [U=2]
** SDI_BAR       [U=2]
** Vdd           [U=14]
.ENDS
****** top level cell is /msd25/lind/rf/mar18run/vco/mix_se.ext
** Instance-id:mult_ms1_0
X1 DI DI_bar carrier_dc_bias VCO_out Ibias 10 12 enable Vdd Gnd mult_ms1
M4 2 PLL Vdd Vdd CMOSP M=2 W=33.60U L=0.70U GEO=0
M4a VCO_out 2 Vdd Vdd CMOSP M=6 W=33.60U L=0.70U GEO=0
M7 2 PLL Gnd Gnd CMOSN M=2 W=9.45U L=0.70U GEO=0
M7a VCO_out 2 Gnd Gnd CMOSN M=6 W=9.45U L=0.70U GEO=0
C1 carrier_dc_bias Vdd 1.0F
C2 Vdd VCO_out 2.0F
C3 Ibias Vdd 1.0F
C4 VCO_out Vdd 271.0F
C5 PLL 2 1.0F
C6 VCO_out Gnd 20.0F
C7 2 Vdd 85.0F
C8 PLL Gnd 1.0F
C9 Ibias Gnd 1.0F
C10 2 Gnd 4.0F
C11 enable Gnd 1.0F
C12 VCO_out 2 5.0F
C13 VCO_out 0 103.0F
C14 Ibias 0 6.0F
C15 carrier_dc_bias 0 10.0F
```

```
C16 enable 0 5.0F
C17 Vdd 0 688.0F
C18 2 0 18.0F
C19 10 0 16.0F
C20 12 0 16.0F
C21 Gnd 0 301.0F
C22 DI 0 2.0F
C23 PLL 0 14.0F
C24 DI_bar 0 2.0F
*** Node Listing for subckt:  mix_se
** N0                    == IdealGND
** N2            [U=4]    == 8_327_248#
*****************************************************************
** 10            [U=1]
** 12            [U=1]
** carrier_dc_bias  [U=1]
** DI            [U=1]
** DI_bar          [U=1]
** enable          [U=1]
** Gnd             [U=5]
** Ibias           [U=1]
** PLL             [U=2]
** VCO_out         [U=3]
** Vdd             [U=5]
*****************************************************************

* mix_diff: Simulation
* File created on Tue Nov 24 18:12:56 1998

.include 'mix_diff.spice'
.include 'n56s.mod'

*****************************************************
*
* Author(s): Ryan E. Lind
* Description: Differential Mixer Drive
*
*****************************************************
**************************
Ib  0  Ibias  100uA
**************************
v1  DI  0  dc  3.3  pulse (3.3 0 40n .1n .1n 40n 81n)
v2  DI_bar  0  dc  0    pulse (0 3.3 40n .1n .1n 40n 81n)
**************************
```

```
vbbias bal_bias 0 dc 3.3
vrf  VCO_out  0  dc  1.65  ac 1 sin(1.65 1.65 916e6 0 0)
**************************
vdd  Vdd  0  dc 3.3
vgnd Gnd  0  dc 0
**************************
venable  Enable  0  dc 3.3  *pulse (3.3 0 20n .1n .1n 50n 100n)
**************************
rloada 12  0  50
rloadb 10  0  50

.options post
.op
.tran  0.01n 80n .1n

*** Node Listing for subckt:  mix_diff
** N0                    == IdealGND
*****************************************************************
** 10             [U=1]
** 12             [U=1]
** bal_bias        [U=2]
** DI             [U=1]
** diff_out        [U=2]
** diff_out_bar     [U=2]
** DI_bar          [U=1]
** Enable          [U=1]
** Gnd             [U=2]
** Ibias           [U=1]
** VCO_out         [U=1]
** Vdd             [U=2]
*****************************************

.END

* mix_diff.spice
*
* File Location       /msd25/lind/rf/mar18run/vco
* File Created        Mon Nov 30 13:39:07 1998
* Ext2spice Version    ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*         Options    -h -mm -n -M -N -V -gc -m -n -mg -M -N -h
*

** Subcircuit definition for invf101
** Extraction file is /msd25/lind/rf/mar18run/vco/invf101.ext
```

```
.SUBCKT invf101 1 2 3 4
M1 1 2 3 3 CMOSP W=9.10U L=0.70U GEO=0
M2 1 2 4 4 CMOSN W=4.20U L=0.70U GEO=0
C1 4 1 2.0F
C2 3 1 18.0F
C3 1 0 4.0F
C4 2 0 3.0F
C5 4 0 3.0F
C6 3 0 4.0F
*** Node Listing for subckt:  invf101
** N0                 == IdealGND
** N1          [U=3]   == O
** N2          [U=3]   == A1
** N3          [U=3]   == Vdd!
** N4          [U=3]   == GND!
.ENDS

** Subcircuit definition for mult_ms1
** Extraction file is /msd25/lind/rf/mar18run/vco/mult_ms1.ext
.SUBCKT mult_ms1 SDI SDI_BAR RF_IN_BAR RF_IN ibias MIX_OUT1 MIX_OUT2
pwr_en
+ Vdd GND
** Instance-id:invf101_0
X1 9 pwr_en Vdd GND invf101
M1 5 SDI 7 GND CMOSN M=16 W=14.00U L=0.70U GEO=3
M2 6 SDI_BAR 7 GND CMOSN M=16 W=14.00U L=0.70U GEO=3
M3 5 5 Vdd Vdd CMOSP M=4 W=21.00U L=0.70U GEO=3
M4 6 6 Vdd Vdd CMOSP M=4 W=21.00U L=0.70U GEO=3
M5 13 5 Vdd Vdd CMOSP M=16 W=21.00U L=0.70U GEO=3
M6 11 6 Vdd Vdd CMOSP M=16 W=21.00U L=0.70U GEO=3
M7 MIX_OUT2 RF_IN 13 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M8 MIX_OUT1 RF_IN 11 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M9 MIX_OUT1 RF_IN_BAR 13 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M10 MIX_OUT2 RF_IN_BAR 11 Vdd CMOSP M=32 W=14.00U L=0.70U GEO=3
M17 7 14 GND GND CMOSN M=24 W=14.00U L=0.70U GEO=3
M18 14 14 GND GND CMOSN M=4 W=14.00U L=0.70U GEO=3
M19 GND 14 GND GND CMOSN W=16.80U L=9.10U GEO=0
M20 14 9 GND GND CMOSN M=2 W=10.85U L=0.70U GEO=1
M21 ibias pwr_en 14 GND CMOSN M=12 W=9.45U L=0.70U GEO=2
C1 7 14 2.0F
C2 SDI GND 1.0F
C3 MIX_OUT2 RF_IN_BAR 1.0F
C4 MIX_OUT1 RF_IN 1.0F
C5 6 5 1.0F
```

C6 13 Vdd 1610.0F
C7 RF_IN 13 15.0F
C8 MIX_OUT1 5 1.0F
C9 RF_IN_BAR 6 1.0F
C10 5 GND 52.0F
C11 SDI_BAR GND 1.0F
C12 MIX_OUT2 11 1.0F
C13 MIX_OUT1 RF_IN_BAR 1.0F
C14 13 5 11.0F
C15 5 Vdd 107.0F
C16 14 GND 53.0F
C17 11 6 11.0F
C18 RF_IN_BAR 13 18.0F
C19 RF_IN 5 1.0F
C20 SDI SDI_BAR 2.0F
C21 7 GND 190.0F
C22 RF_IN RF_IN_BAR 5.0F
C23 MIX_OUT2 6 1.0F
C24 MIX_OUT1 11 1.0F
C25 MIX_OUT2 MIX_OUT1 3.0F
C26 RF_IN_BAR 5 1.0F
C27 SDI 7 10.0F
C28 11 Vdd 1610.0F
C29 9 14 1.0F
C30 ibias GND 26.0F
C31 RF_IN 11 15.0F
C32 MIX_OUT2 13 1.0F
C33 MIX_OUT1 6 1.0F
C34 MIX_OUT2 Vdd 1137.0F
C35 6 GND 52.0F
C36 ibias pwr_en 6.0F
C37 MIX_OUT2 RF_IN 1.0F
C38 SDI_BAR 7 10.0F
C39 6 Vdd 107.0F
C40 RF_IN_BAR 11 17.0F
C41 MIX_OUT1 13 1.0F
C42 MIX_OUT2 5 1.0F
C43 RF_IN 6 1.0F
C44 MIX_OUT1 Vdd 1137.0F
C45 ibias 0 33.0F
C46 GND 0 293.0F
C47 Vdd 0 562.0F
C48 pwr_en 0 30.0F
C49 MIX_OUT1 0 179.0F

```
C50 MIX_OUT2 0 187.0F
C51 11 0 196.0F
C52 13 0 185.0F
C53 14 0 88.0F
C54 RF_IN 0 284.0F
C55 RF_IN_BAR 0 286.0F
C56 SDI_BAR 0 80.0F
C57 SDI 0 85.0F
C58 5 0 158.0F
C59 6 0 158.0F
C60 7 0 141.0F
C61 9 0 9.0F
*** Node Listing for subckt:  mult_ms1
** N0                  == IdealGND
** N5          [U=4]   == N5
** N6          [U=4]   == N6
** N7          [U=3]   == N7
** N9          [U=2]   == N9
** N11         [U=3]   == N11
** N13         [U=3]   == N13
** N14         [U=6]   == N14
*****************************************************************
** GND          [U=14]
** ibias        [U=2]
** MIX_OUT1     [U=3]
** MIX_OUT2     [U=3]
** pwr_en       [U=3]
** RF_IN        [U=3]
** RF_IN_BAR    [U=3]
** SDI          [U=2]
** SDI_BAR      [U=2]
** Vdd          [U=14]
.ENDS

** Subcircuit definition for se_to_diff
** Extraction file is /msd25/lind/rf/mar18run/vco/se_to_diff.ext
.SUBCKT se_to_diff vdd_rf diff_out_b single_end_in gnd_rf diff_out ext_bias1
+ ext_bias2
C1 1 3 HPCAP50 SCALE=591.67
*C1P 3 CAPerror! HPCAP50P SCALE=591.7
* C1=2106.36FF C1P=0.06FF
C2 2 4 HPCAP50 SCALE=591.67
*C2P 4 CAPerror! HPCAP50P SCALE=591.7
* C2=2106.36FF C2P=0.06FF
```

```
M1 1 single_end_in 2 8 CMOSN M=4 W=17.50U L=0.70U GEO=0
M2 vdd_rf 4 diff_out 8 CMOSN M=4 W=17.50U L=0.70U GEO=0
M3 vdd_rf 3 diff_out_b 8 CMOSN M=4 W=17.50U L=0.70U GEO=0
M4 2 gnd_rf gnd_rf 8 CMOSN M=4 W=17.50U L=0.70U GEO=0
R1 1 vdd_rf RHPPOLYSB50 SCALE=11.00
* R1=990.0 (width=1.75U)
R2 diff_out_b gnd_rf RHPPOLYSB50 SCALE=11.00
* R2=990.0 (width=1.75U)
R3 gnd_rf 2 RHPPOLYSB50 SCALE=11.00
* R3=990.0 (width=1.75U)
R4 gnd_rf diff_out RHPPOLYSB50 SCALE=11.00
* R4=990.0 (width=1.75U)
R5 3 ext_bias1 RHPPOLYSB50 SCALE=11.00
* R5=990.0 (width=1.75U)
R6 ext_bias2 4 RHPPOLYSB50 SCALE=11.00
* R6=990.0 (width=1.75U)
C3 2 8 38.0F
C4 diff_out_b 3 2.0F
C5 gnd_rf 2 1.0F
C6 4 vdd_rf 2.0F
C7 vdd_rf 8 43.0F
C8 diff_out_b 8 16.0F
C9 diff_out 4 2.0F
C10 3 8 17.0F
C11 diff_out 8 16.0F
C12 single_end_in 2 2.0F
C13 4 8 17.0F
C14 gnd_rf 8 22.0F
C15 1 8 16.0F
C16 gnd_rf single_end_in 3.0F
C17 single_end_in 1 9.0F
C18 diff_out_b vdd_rf 3.0F
C19 vdd_rf 3 2.0F
C20 diff_out vdd_rf 3.0F
C21 diff_out 0 44.0F
C22 vdd_rf 0 339.0F
C23 diff_out_b 0 43.0F
C24 single_end_in 0 45.0F
C25 ext_bias1 0 13.0F
C26 ext_bias2 0 13.0F
C27 1 0 56.0F
C28 2 0 78.0F
C29 3 0 37.0F
C30 4 0 40.0F
```

```
C31 gnd_rf 0 157.0F
*** Node Listing for subckt:  se_to_diff
** N0                  == IdealGND
** N1          [U=3]   == N1
** N2          [U=4]   == N2
** N3          [U=3]   == N3
** N4          [U=3]   == N4
** N8          [U=4]   == 6_795_112#
*****************************************************************
** CAPerror!      [U=2]
** diff_out       [U=3]
** diff_out_b     [U=3]
** ext_bias1      [U=2]
** ext_bias2      [U=2]
** gnd_rf         [U=6]
** single_end_in  [U=2]
** vdd_rf         [U=4]
.ENDS
****** top level cell is /msd25/lind/rf/mar18run/vco/mix_diff.ext
** Instance-id:mult_ms1_0
X1 DI DI_bar diff_out_bar diff_out Ibias 10 12 Enable Vdd Gnd mult_ms1
** Instance-id:se_to_diff_0
X2 Vdd diff_out_bar 1 Gnd diff_out bal_bias bal_bias se_to_diff
M4 2 VCO_out Vdd Vdd CMOSP M=2 W=33.60U L=0.70U GEO=0
M4a 1 2 Vdd Vdd CMOSP M=6 W=33.60U L=0.70U GEO=0
M7 2 VCO_out Gnd Gnd CMOSN M=2 W=9.45U L=0.70U GEO=0
M7a 1 2 Gnd Gnd CMOSN M=6 W=9.45U L=0.70U GEO=0
C1 diff_out_bar Vdd 1.0F
C2 Vdd diff_out_bar 1.0F
C3 Vdd diff_out 1.0F
C4 diff_out Vdd 1.0F
C5 diff_out Vdd 3.0F
C6 bal_bias Vdd 2.0F
C7 Vdd bal_bias 2.0F
C8 Vdd Ibias 1.0F
C9 diff_out Vdd 5.0F
C10 2 Gnd 4.0F
C11 1 2 5.0F
C12 1 Vdd 256.0F
C13 VCO_out 2 1.0F
C14 diff_out_bar Vdd 10.0F
C15 1 Gnd 13.0F
C16 2 Vdd 85.0F
C17 VCO_out Gnd 1.0F
```

```
C18 diff_out 0 35.0F
C19 bal_bias 0 44.0F
C20 VCO_out 0 9.0F
C21 diff_out_bar 0 109.0F
C22 Ibias 0 5.0F
C23 Vdd 0 498.0F
C24 10 0 11.0F
C25 12 0 11.0F
C26 1 0 120.0F
C27 Gnd 0 870.0F
C28 DI 0 4.0F
C29 Enable 0 3.0F
C30 2 0 18.0F
C31 DI_bar 0 4.0F
*** Node Listing for subckt:  mix_diff
** N0                  == IdealGND
** N1          [U=3]   == se_to_diff_0/$single_end_in
** N2          [U=4]   == 8_1799_348#
*****************************************************************
** 10          [U=1]
** 12          [U=1]
** bal_bias      [U=2]
** DI          [U=1]
** diff_out      [U=2]
** diff_out_bar    [U=2]
** DI_bar        [U=1]
** Enable        [U=1]
** Gnd           [U=6]
** Ibias         [U=1]
** VCO_out       [U=2]
** Vdd           [U=6]
*****************************************************************

*****************************************
*       bias4.cir         *************
*****************************************
.op
.tran .01u 10u
.options post
.options method=gear
*****************************************
*VCC   100  0  sin(3.3 .3 1000K 0 0 0)
VCC   100  0  pulse(3.3 2.3 0 9.9u .05u .05u 10u)
*VCC   100  0  dc 3.3
```

```
Vimon  5 4  dc 0.0
*****************************************

M1 2 1 0 0      CMOSN M=1 W=70U L=7U GEO=0
M2 2 3 100 100          CMOSP M=1 W=70U L=14U GEO=0
M3 3 3 100 100          CMOSP M=1 W=70U L=14U GEO=0
M4 3 2 1 0      CMOSN M=1 W=14U L=1.4U GEO=0
M5 4 1 0 0      CMOSN M=1 W=70U L=7U GEO=0

Rbias 1 0 95K

Rload 5 100 100K

Ccomp 2 3 1pF

.include 'n56s.mod'

.end
```

Vita

Ryan Lind was born on November 9, 1973, in Crystal Lake, Illinois. In 1979, Ryan moved with his family to Knoxville, Tennessee, where he currently resides. After receiving his high school diploma from Christian Academy of Knoxville in 1992, Ryan attended The University of Tennessee, Knoxville, where he was married in 1995, and earned a Bachelor of Science Degree in Electrical Engineering in 1997. He immediately began pursuing a Master of Science Degree in Electrical Engineering. While getting his Masters Degree Ryan worked in the Monolithic Systems Development Group at Oak Ridge National Laboratory as part of the UT/ORNL Joint Program in Mixed Signal VLSI and Integrated Sensors program. Ryan also became a father in December 1997. Ryan's hobbies include anything that keeps him outdoors such as fishing, mountain biking, windsurfing, hiking, and hunting in addition to the design of analog integrated circuits.