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# High-Speed Differential Via Optimization using a High-Accuracy and High-Bandwidth Via Model


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***Abstract*— A physics-based equivalent model of the high-speed differential via pair with high accuracy and high bandwidth is proposed for the first time. The proposed physics-based equivalent circuit model of the differential via pair includes the effect of adjacent ground (GND) vias. The proposed model is verified using 3D full-wave numerical simulation results. In addition, the change in electrical performance due to change in anti-pad radius, the via pitch and the GND-via- -to-differential-via distance is analyzed. Based on the analysis, electrical performance of differential via pair can be accurately and rapidly optimized with respect to design parameters, such as the via pitch, the anti-pad radius and the GND-via-to-differential-via distance using the proposed model, to provide pre-layout design guide for high-speed channel designers. By using the proposed high-accuracy and high-bandwidth physics-based via model, the via optimization time can be drastically reduced with high accuracy.**



***Keywords—High-speed via optimization, differential via, high-accuracy, high-bandwidth***


## I. INTRODUCTION

With trend in technology scaling down and the data rate increasing continuously, high-speed channel design and optimization have become more challenging [1]. Maintaining signal integrity is an inevitable challenge for high-speed printed circuit board (PCB) designers during the product development stage [2]. In high-speed channels, vertical interconnects, commonly known as vias, are used to route signals on different layers for different channels, which are typical impedance discontinuity inducing components in high-speed channels, which can result in profound signal integrity and power integrity issues. Thus, it is essential to design the vias with high electrical performance, to meet required impedance, return loss, and insertion loss specifications.

Generally, 3D full-wave simulation software, such as HFSS and CST, are used for the optimization of the via transition. Based on 3D full-wave simulation, the via stub resonance, the impact of non-functional pads and the ground via numbers were investigated in [3]. The time domain impedance (TDR) for the through hole vias, the blind vias and the buried vias was studied in [4]. Due to the structural complexity of the via transition and high number of design parameters for optimization, the via optimization by 3D full-wave simulation is very time consuming. Many equivalent models for high-speed differential via pair have been developed to reduce the optimization time. A differential via pair modeling methodology was introduced in [5], where accuracy decreases after 20 GHz. Moreover, some modeling strategies of the high-speed via was investigated in paper [6] and non-function pads placement optimization for high-speed channel based on multiple reflection theory was proposed [7],[8]. However, to apply techniques introduced in [7] and [8], accurate high-speed differential via model is required.

To help reduce the high-speed channel design time, this paper introduces the high-speed differential via optimization based on a physics-based via model with high accuracy and high bandwidth, which can work up to 70 GHz, for the first time. The proposed physics-based equivalent model of differential via verified by 3D full-wave simulation (ANSYS HFSS). Unlike the conventional physics-based via models, the proposed equivalent circuit model considers the impact of the higher-order modes in the parallel-plate for increased accuracy in high frequency region. In addition, the change in electrical performance with respect to change in the anti-pad radius, the via pitch and the ground (GND)-via-to-differential-via distance are analyzed. The electrical performance of differential via pair can be accurately and rapidly optimized based on the proposed model, to save time during high-speed channel design.

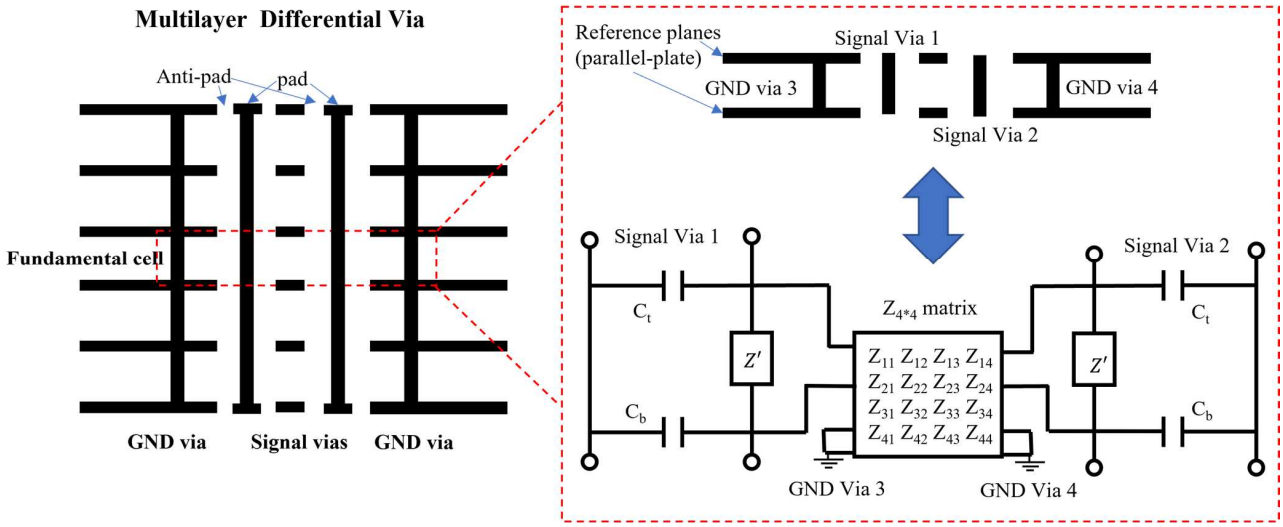


Fig. 1. Proposed physics-based equivalent circuit model of the differential via with individual anti-pad.

## II. The Proposed Differential Via Pair Model

A high-accuracy and high-bandwidth single signal via model was proposed in [9]. The application range of the high-accuracy and high-bandwidth via model was investigated in [10]. Based on the high-accuracy and high-bandwidth equivalent circuit model of single signal via, the physics-based equivalent circuit model of the differential via pair with the individual anti-pad is proposed in this paper, as shown in Figure 1, which corresponds to differential via pair segment crossing a cavity enclosed by two reference plates. The equivalent circuit model includes four capacitors for the via-to-parallel-plate coupling, the high-order mode parallel-plate impedances $Z'$ for each signal via, and the 4 by 4 Z matrix for the coupling of all vias due to fundamental parallel-plate mode. In the 4 by 4 Z matrix, the self-impedance $Z_{ii}$ represents the fundamental parallel-plate impedance for each via while the mutual-impedance $Z_{ij}$ represents the via coupling due to the fundamental parallel-plate mode. The key difference with the previous method [6] is that the proposed equivalent model considers the impact of higher-order parallel-plate modes, to achieve high accuracy for high bandwidth application.

The coupling capacitance between the via and the parallel plate has been analyzed in the past, and the via-to-plate capacitance calculations are proposed in [11],[12], and[13]. In this paper, the coupling capacitances are calculated based on [12].

The self-impedance $Z_{ii}$ represents the coupling between the via and the parallel-plate due to the fundamental parallel-plate mode, which can be calculated in terms of the modal fields. When the parallel plate is infinitely large or the boundary condition of the plate consists of perfectly matched layers (PMLs), the self-impedance can be calculated as [14]

$$Z_{ii} = \frac{k_0^2 H_0^2\left(k_0 r_0^i\right) h}{2\pi r_0 j\omega\varepsilon_0\varepsilon_r k_0 H_1^2(k_0 r_0^i)} \quad (1)$$

, where $i$ is the via number, $r_0^i$ is the radius of the $i_{th}$ via. $k_0 = k' - jk''$, which is a complex wavenumber. $k' = \omega\sqrt{\mu_0\varepsilon_0\varepsilon_r}$ and $k'' = \omega\sqrt{\mu_0\varepsilon_0\varepsilon_r}(tan\delta + \frac{d_s}{h})/2$, and $\omega$ is the angular frequency. $\varepsilon_0$ and $\mu_0$ are the permittivity and permeability of free space, respectively. $\varepsilon_r$ is relative permittivity, $tan\delta$ is the loss tangent of the dielectric material, $d_s = \sqrt{2/\omega\mu_0\sigma}$ is the skin depth of conductor with conductivity of $\sigma$. $h$ and $t$ are the parallel-plate height and plate thickness, respectively. $H_0^2$ and $H_1^2$ is the zero-order and first-order Hankel function of the second kind, relatively. When the parallel plate is finite or the boundary condition of the plate is a perfect electric or magnetic conductor (PEC or PMC) boundary, the self-impedance $Z_{ii}$ can be calculated based on the cavity method [15].

The mutual-impedance $Z_{ij}$ represents the coupling between the vias due to the fundamental parallel-plate mode, which can also be calculated by the modal fields. When the parallel plate is infinitely large, we can calculate the mutual-impedance as [14]

$$Z_{ij} = \frac{k_0^2 a_0 H_0^2(k_0 r_{ij})\ hJ_0(k_0 r_0^j)}{2\pi r_0^i j\omega\varepsilon_0\varepsilon_r k_0 a_0 H_1^2(k_0 r_0^i)} \quad (6)$$

Where $j$ is the via number, $r_0^j$ is the radius of the $j_{th}$ via, $r_{ij}$ is the pitch size of the $i_{th}$ via and of the $j_{th}$ via. $J_0$ is the zero-order Bessel function. When the parallel plate is finite, the mutual impedance can be calculated based on the cavity method [15].

The high-order parallel-plate modes impedances $Z'$ for each signal via can also be calculated in terms of the modal fields, which are excited at the anti-pad boundary. For the higher-

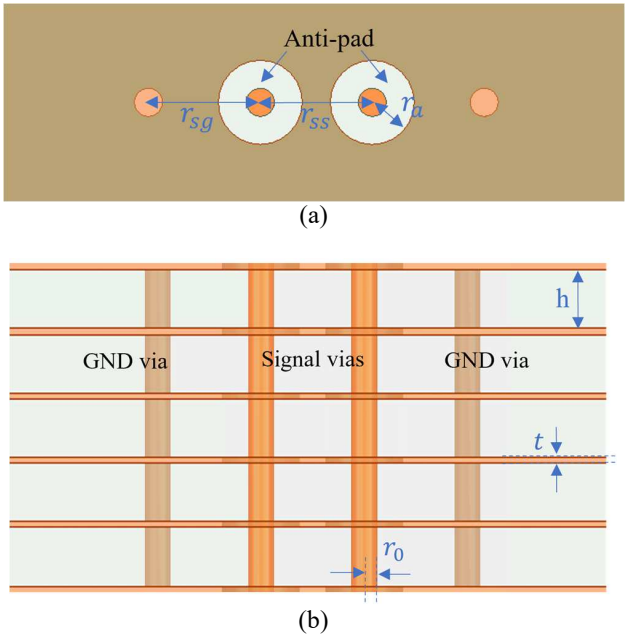


Fig. 2. Differential via with GND vias in 6 layers board. (a) top view, (b) side view.

order modes, only $TM_{0n}$ modes are considered here. Because the via structure we consider is circular and symmetric, only $TM_{0n}$ modes (higher-order modes, which are axially isotropic modes) are excited [16]. The impedance $Z'$ is calculated as

$$Z' = \frac{h\sum_{n=1}^{N} k_n H_0^2(k_n r_a)}{j2\pi r_a \omega \varepsilon_0 \varepsilon_r \sum_{n=1}^{N} H_1^2(k_n r_a)} \quad (8)$$

where $k_n = \sqrt{k_0^2 - (n\pi/h)^2}$, n represents the mode number, N is the total number of higher-order modes it counts for the via modeling. The derivation of $Z'$ can be found in the reference [9].

## III. Verification and Optimization

In this section, the proposed equivalent circuit model of differential via pair with adjacent GND vias is verified 3D full-wave numerical simulation. Change in electrical performance due additional high-order parallel plate modes is analyzed. Based on the proposed model, the differential via pair's electrical performance can be optimized by parametric analysis on the via pitch, the anti-pad radius and GND-via-to-differential-via distance.

Figure 2 shows the top view and the side view of the differential via pair with GND vias with 6 GND layers, for 3D full-wave numerical simulation. All via radius are $r_0$ while the anti-pad radius is $r_a$, the parallel-plate high is $h$ and each plate thickness is $t$. The signal via pitch is $r_{ss}$ and the via pitch for the signal via and the GND via is $r_{sg}$. The boundary condition for the model is PML.

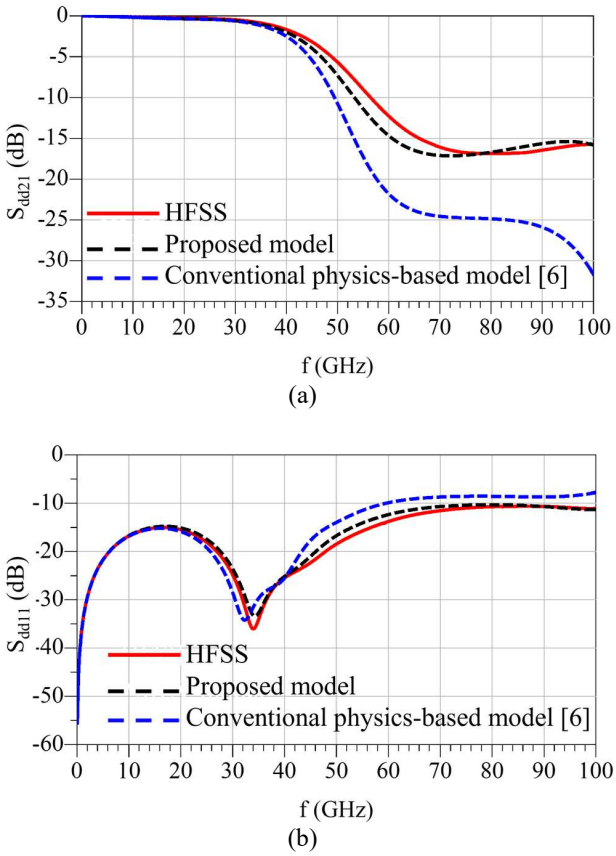


Fig. 3. Differential S-parameters comparison for different methods: (a) Differential insertion loss Sdd21. (b) Differential return loss Sdd11.

### A. *Effect of High-Order Parallel Plate Modes*

In first set of analysis, the $r_0$ and $r_a$ are 5 mils and 10 mils, respectively. Meanwhile, the $h$ and the $t$ are 10 mils and 1 mil, the $r_{ss}$ and $r_{sg}$ are both 40 mils. The total thickness of the model is 56 mils. The comparison between the differential insertion loss and the differential return loss of the differential via model are plotted in Figure 3, between the proposed equivalent model and HFSS results. The red solid curve are the results from the 3D full-wave numerical simulation, ANSYS HFSS, the black dotted curve are the results from the proposed equivalent model while the blue dotted curve represents the results from the conventional physics-based equivalent model from [6].

We can observe that the differential S-parameters from the proposed equivalent model shows high correlation with the 3D full-wave numerical simulation, up to 100 GHz. However, the differential S-parameters from the conventional physics-based equivalent model shows much larger difference with the simulation results above 40 GHz because it does not consider the high-order parallel-plate modes impedance $Z'$. The proposed equivalent model's high accuracy at high frequency is verified. . In addition, the importance of high-order parallel-plate modes for high frequency via modeling is also verified..

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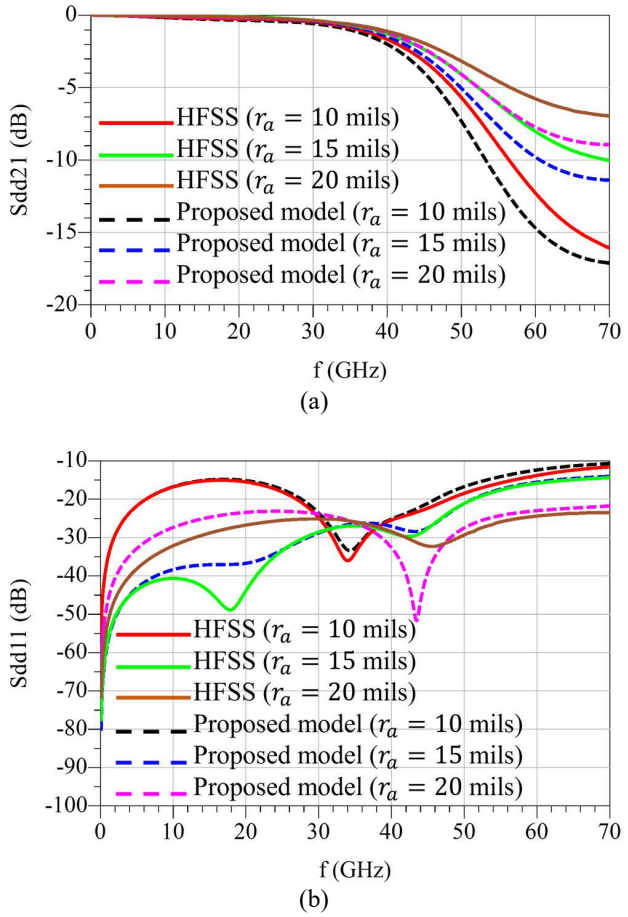


Fig. 4. Differential S-parameters comparison for various anti-pad radii. (a) Differential insertion loss Sdd21, (b) Differential return loss Sdd11.

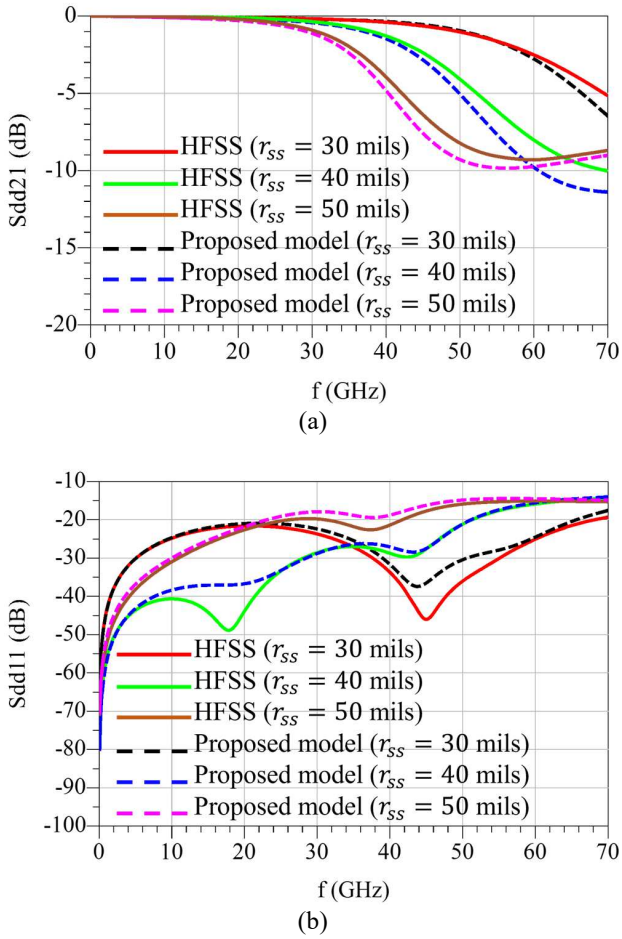


Fig. 5. Differential S-parameters comparison for various via pitches. (a) Differential insertion loss Sdd21, (b) Differential return loss Sdd11.

### *B. Parametric Anlaysis on Anti-pad Radius*

To investigate the effect of changes in anti-pad radius, the anti-pad radius is swept from 10 mils to 20 mils with a step of 5 mils in the second case. All other geometrical parameters of the differential via are unchanged from the first case in sub-section A. The differential S-parameters of the differential via are plotted in Figure 4.

The differential insertion loss from the proposed model shows high level of correlation with the simulation results up to 70 GHz. The differences in differential insertion loss between the proposed model and the simulation is less than 2 dB. The differential return loss from the proposed model also shows relatively a high level of correlation with simulation results, with the exception of a few frequency points where the magnitude is below -30 dB.

Additionally, the differential insertion loss decreases with the increase of the anti-pad radius. The differential return loss can be decreased below 30 GHz and can be increased above 40 GHz with the increase of the anti-pad radius.

The proposed model accurately model the effect of change in anti-pad radius on electrical performance.

### *C. Parametric Anlaysis on Via Pitch*

The effect of change in via pitch on the differential via's electrical performance is analyzed in the third case. The $r_{ss}$ is equal to the $r_{sg}$. They are both swept from 30 mils to 50 mils with a step of 10 mils. The anti-pad radius for the signal via is 30 mils. Except the anti-radius and the via pitch size, other geometrical parameters of the differential via remain unchanged as the configurations in the first case. The differential S-parameter comparison of the differential via is plotted in Figure 5.

From the differential S-parameter comparison, it is verified again that the proposed model can accurately model the differential via up to 70 GHz, both for differential insertion loss and the differential return loss. Differential insertion loss and the differential return loss of the differential via can decrease for a larger via pitch above 30 GHz. However, for the frequencies below 20 GHz, the larger via pitch can result in increased the differential return loss.

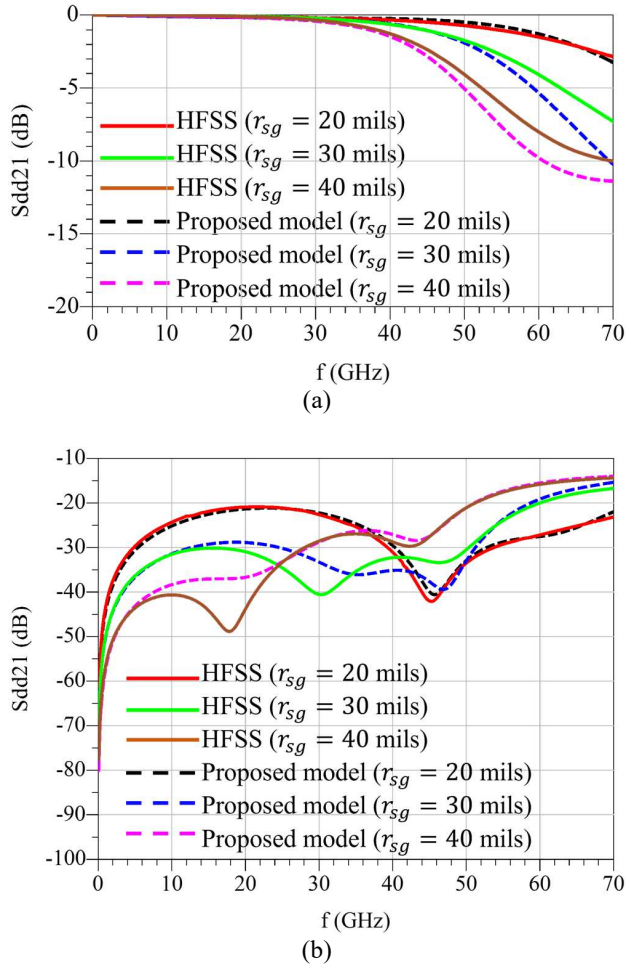


Fig. 6. Differential S-parameters comparison for various GND-via-to-differential-via distances. (a) Differential insertion loss Sdd21, (b) Differential return loss Sdd11.

### *D. Parametric Anlaysis on GND Via Distance*

For fourth set of analysis, the signal via pitch $r_{ss}$ is fixed as 40 mils, but the pitch $r_{sg}$ of signal via and the GND via is swept from 20 mils to 40 mils, with 10 mils step. Similarly, the geometry configurations of the differential via remains unchanged as the differential via in third set of analysis. The differential S-parameters are plotted in Figure 6.

The proposed model continues to show high correlation to simulation. The distance $r_{sg}$ between the signal via and the GND via can also affect the differential via's electrical performance. Unlike the third set of analysis, the small GND-via-to-differential-via distance can help decrease the differential insertion loss and the differential return loss in the frequencies above 30 GHz because the return current return loop size for the differential via pair decreases as the GND-via-to-differential-via distance decreases.

The proposed equivalent model of the differential via pair with adjacent GND vias is verified up to 70 GHz. The effects of the anti-pad radius, the via pitch and GND-via-to-differential-via distance are analyzed. In addition, the computational resource cost of the first set of analysis in 3D full-wave FEM simulation and the proposed model are compared in table I. The simulation was conducted in a server with 3.45 GHz CPU and 512 GB RAM memory. The proposed method is shows higher time and resource efficiency when compared to 3D full-wave simulation with comparable level of accuracy. PCB designers can use the proposed model to optimize high speed channels with at reduced computational resources and time.

Table I. Comparison of Computational Resources Cost (per case A)

| Method | Memory Cost (GB) | CPU Time (hours) |
|---|---|---|
| Simulation (HFSS) | 29 | 2.1 |
| Proposed model | 0.2 | 0.02 |

## IV. Conclusion

High-accuracy and high-bandwidth physics-based equivalent circuit model of differential via pair with the individual anti-pad and adjacent GND vias is proposed in the paper, for the first time. The accuracy of the proposed equivalent circuit model is verified using comparison to 3D full-wave numerical simulation over multiple cases studies with different anti-pad radius, via pitch size and GND-via-to-differential-via distance up to 70 GHz. Differential via can be optimized by increasing the anti-pad radius or decreasing the via pitch size. Decreasing the GND-via-to-differential-via distance can also help improve the differential via's electrical performance. When compared to 3D full-wave numerical simulation, the proposed model can save computational resources and time. The proposed differential via model will allow high speed channel designers to optimize differential via with different parameters with reduced computation resources and time. Most importantly, the proposed model also provides physical insight to guide differential via optimization for high-speed channels.

## V. Acknowledgements

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