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ESD Behavior of RF Switches and Importance of System Efficient ESD Design

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***Abstract*— RF switches are typically used in the RF front-end of portable devices such as antenna or matching tuners to improve the RF link performance. They are usually the first active devices after the antenna and are vulnerable to primary or secondary ESD discharges to the antennas. This paper investigates the ESD behavior of one of the high frequency switches used in the RF-front-end of portable devices and expresses the importance of the ESD pulse that passes through the switch and reaches the next stage in the RF path, possibly damaging the next stage**

Keywords*— *RF SEED, Electrostatic discharge (ESD) protection, RF Switch

I. INTRODUCTION

High frequency system designers typically add an ESD protection device after the antenna to protect the RF front ends using data sheet information. This approach is not an efficient methodology as it neglects the interaction of the external protection device with the surrounding components, traces, and internal protections of the ICs. An improved approach has been introduced [1]. The system efficient ESD design (SEED), uses a co-design methodology of on-board and on-chip ESD protection.

In some applications, the RF front-end cannot be protected by transient voltage suppressors (TVS) due to strict harmonic distortion requirements and RF voltages that can reach as high as 30 V. This requires the accurate ESD modeling of the RF path components to evaluate the robustness of the system. The first active component in the RF-path after the antenna is usually an RF switch, e.g., a matching tuner, an aperture tuner or an RX/TX switch. An aperture tuner uses switches to select between a couple of inductance and capacitance values that are placed in shunt or in series to the RF path to improve the matching performance of the transceiver in different situations, e.g., to compensate for effects of hand and head in proximity to the antenna [2, 3, 4, 5] . Eventually, this switch passes the RF signal to the next stage that may be a low-noise amplifier, Saw filter, diplexer or triplexer. In general, it is believed that the first component after the antenna is the most endangered IC in the RF chain. This leads the manufacturer of these switches to consider a very robust internal protection for these switches using the SOI (Silicon on Insulator) CMOS technology [6, 7]. Most of the articles in this area focus on how to improve the robustness of the switch looking into the ESD properties of the standalone switch using standard TLP (Transmission Line Pulser) measurements with 100 ns pulse width for ESD characterization [8] but suffer from having a systematic design approach which is usually referred to as the SEED approach [9, 10]. Using the 100 ns pulses provides information about the general ESD behavior and the robustness level of the switch but it is not applicable for evaluating the system robustness and predicting the system level damaging thresholds.

A robust RF-switch is a necessary but not sufficient first step. As the designer should not neglect the ESD pulse that passes through the switch [11, 12] and reaches the next stage. It may cause hard failure in the next stage ICs. This pulse is referred to by us as ESD21 as it resembles S21 in ESD. ESD21 of a standalone switch depends mainly on its internal protection device structure, the switch status, and its load impedance at the output. On the other hand, a fixed high pass matching network is usually used between the antenna and matching tuner to improve the matching performance of the antenna and to suppress the low frequency components of the ESD event. This circuitry performs as a pulse shaping network and plays an important role in the ESD robustness of the system. The ESD behavior of a RF switch in a system design approach has been studied in [11]. It has been shown that an ESD event may even pass through and open switch and some portion of the ESD pulse reach the next stage.

This paper examines the ESD behavior of a RF switch in various situations and shows the importance of considering ESD21, or more generally, using the SEED approach in system design. It has been shown that the ESD21 may damage the next stage IC. In addition, the effect of circuity after the antenna on the damaging threshold has been investigated. To prove the concept, a low noise amplifier is considered as the next stage IC after the switch. The ESD behavior and damage threshold of this LNA have been measured under various conditions. Meanwhile, the effect of pulse shaping networks has been studied from the point of view of ESD protection using simulations and measurements. Since this paper treats system level ESD, thus HBM and CDM do not form relevant test standards. Both are unpowered and both do not take an

decoupling capacitors into account. In CDM the pulse type is determined by the size of the IC, not by the external treat. In HBM the rise time is very slow, such slow rising pulses cannot reach an RF switch due to inductances to GND within the RF path.

II. Pulse Shaping Network

Typically, a network is added between the antenna and the matching tuner to improve matching performance and to provide AC coupling between the antenna and the RF front-end circuitry. These circuitries, which usually form a high-pass LC filter, serve as pulse-shaping circuits for ESD pulses so that only narrow pulses, having a width of less than a few nanoseconds reach the IC. The series capacitor in this matching network plays an important role in the ESD behavior of the RF front end. Its capacitance value and case size affect the sparking voltage and, more importantly, the amplitude and width of the pulse that passes through it and reaches the next stages. Usually, the antenna designers include an inductive path from the antenna to the ground to serve as low frequency ESD protection. This inductive path provides the antenna to be discharged after the ESD event and may prevent the matching network's series capacitor from sparking.

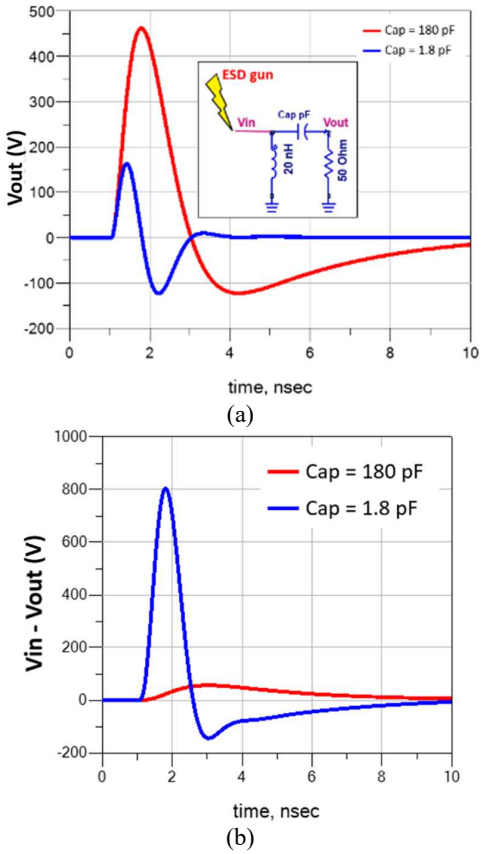

Fig. 1. (a) The series capacitor output voltage and (b) the voltage across it, for 8 KV ESD gun voltage contact mode discharge.

Fig. 1 shows SPICE simulation results of the effect of the series capacitor value on the output voltage and the voltage drop across the capacitor when the ESD gun is discharged to the antenna. The capacitor's output voltage matters for the next stages ESD behavior, and the voltage drop across the capacitor is critical for its sparking. In both simulations, an inductive path with inductance of 20 nH is used, which provides a low frequency path for the ESD event to the ground and is helpful for the protection of the switch.

It is seen that by increasing the capacitor value, the width of the output pulse becomes wider, and its amplitude increases so that the next IC is more endangered. On the other hand, for smaller values of the series capacitors, the voltage drop across it increases, which increases the likelihood of sparking. Therefore, in addition to the RF requirements, ESD protection should be considered in the selection of these components.

III. Evaluating the ESD Behaviour of the Switch

Fig. 1 shows that even for a large value series capacitor of 180 pF, and due to the presence of the inductor, the maximum pulse length that reaches the IC is shorter than 2 ns. On the other hand, the IEC standard states that the rise time of IEC-61000-4 waveforms is allowed to vary in the range of 800 ps ± 25%. Thus, the fastest rise time for ESD gun contact mode discharges is about 600 ps. Therefore, a TLP system having a 2 ns pulse width and 500 rise time is used to evaluate the ESD behavior of the switch. It should be noted that full-width at half maximum (FWHM) is considered to define pulse width. Although the 500 ps rise time is very fast compared to all commercially available ESD guns, it emulates the strict limits of the IEC standard and prevents the systems designer from overestimating the robustness level of the system in the IEC 61000-4-2 standard. The rise time of the TLP normalized waveform used for the switch's characterization is compared with the longest and shortest rise time of the IEC waveform and is shown in Fig. 2.

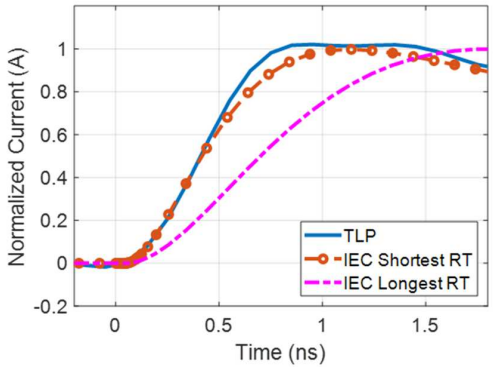

Fig. 2. Comparing TLP waveform with the longest and shortest possible rise time of the IEC waveform

The switch is characterized by measuring the input voltage, input current and output voltage of the switch. The input voltage is measured using a 1 kΩ voltage pick-up resistor which is 2 mm from the IC and the IC's input current is measured using a 3mm long inductive current probe placed just before the voltage pick-up. The frequency response and the output waveform of the current probe is used later to reconstruct the switch's input current. The output voltage was measured by a 50 Ω oscilloscope with 2 GHz bandwidth. The test vehicle used for the measurements is shown in Fig. 3. This test vehicle is designed such that it can be a module of the already developed modular SEED system for further measurements [13].

In the past there was a need to distinguish vf-TLP from TLP due to the lack of current and voltage probes that can be directly placed at an IC. This forced the use of reflective measurements used in vf-TLP. Nowadays probing directly at

the IC is available, thus, TLP measurement methods can be used for any rise time. As it is possible to make the measurements with < 400 ps rise times in the current TLP systems, thus, from a rise time perspective it is a vf-TLP.

The switch is measured for positive and negative polarity of the TLP waveforms, in its open and closed status and for different output loads which are 50 Ω, 10 Ω and 2 Ω. The different output loads are used to represent the ESD protection of the next stage. Normally, the next stage offers a 50 Ohm load, however, if its ESD protection turns on, it provides a low impedance path to the ground. The leakage current of the switch input pin is used as failure criterion for the switch. It is measured after each TLP pulse. Normally, an IV curve is plotted based on the 70% – 90% time data from 100 ns TLP pulses [6,14]. Since the TLP pulse is very narrow in these measurements the I-V and I-I curves are plotted based on the peak value of the input voltages and currents.

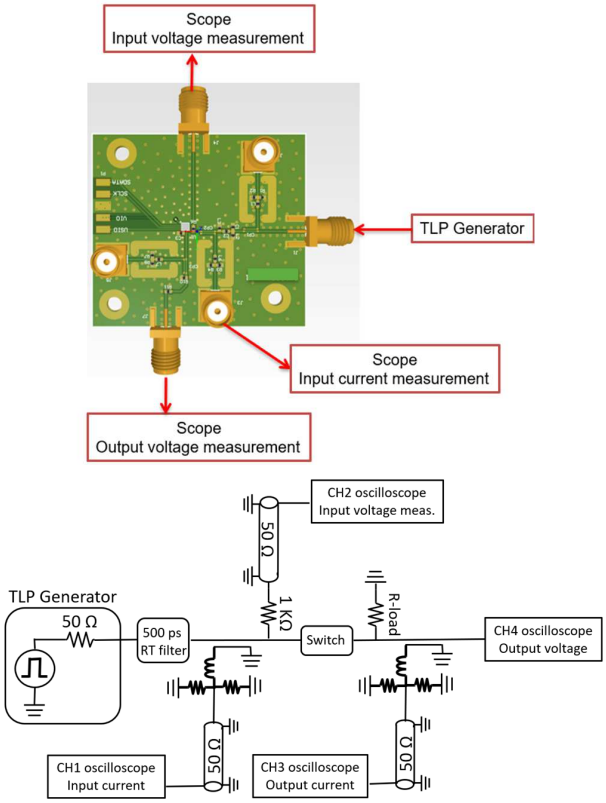

Fig. 3. A view of the switch's test vehicle and schematic of the test setup

The switch is created from two chains of FETs, one is in the shunt path to the ground for protection and one in the series path to create the switching performance [5]. Indeed, the input current is the composition of the output current that passes the series FET's path to the output load and the current flowing through the internal protection device: The FET chains that connect to ground. The switch status is determined by the gate voltage of FETs in the series path. The FET chains to GND are only for ESD protection as when the switch is open there is no input current at low voltages of TLP. The pulse at the input of the switch can also capacitively increase the gate voltage of these FETs and create a voltage drop across the drain-source. If this voltage drop is high enough, the state of the switch changes momentarily from open to closed, and some current flows to the output load [3]. The switch's input voltages at which the series and shunt FETs turn on are determined by the capacitance between the switch's input and the FETs' C_{GD}. For the current switch, our measurements show that the series FET's chain turns on earlier than the shunt path.

Fig. 4 shows the transient input and output voltages of the closed switch for different negative pulses. It is seen that at low TLP voltages, the output voltage follows the input voltage until the switch's internal protection turns on. The gate voltage of FETs is shunt chain increases due to the existing capacitance between the gate and the drain of the protection path and after some amount of input voltage the gate voltage is high enough so that the protection path turns on [3]. Measurement results at higher TLP voltages show that the switch has a robust internal protection which starts conducting at about ±80 V input voltage of the IC and clamps completely at ±130 V input voltage. However, the turn-on behavior of the internal protection depends to the output load and the state of the switch.

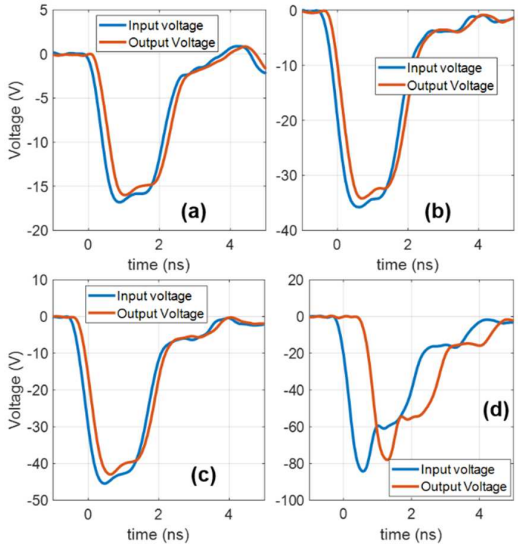

Fig. 4. Transient input and output voltage of the closed switch for 50 Ω output load vs. different TLP charge voltages. (a) -50V, (b) -70V, (c) -100V, and (d) -200V,

Measurement results also show that the switch structure is completely symmetric with respect to the pulse polarity. As evidence, Fig. 5 shows the input IV curve of the input pin with an output load of 50 Ω when the switch is open for both polarities. For comparison, the absolute values of the voltages and the currents for the negative polarity are plotted in this figure. It is seen that at very low input voltages, e.g. region A, the input current is zero as the switch is open and the internal protection device is OFF. As the input voltage surpasses 50 V, the ESD event turns the switch on and the current starts flowing into the output load, e.g. region B. In region C, the internal protection device starts conducting so that at higher voltages e.g., region D, it has been already clamped and turned on completely with a low impedance and there is a huge current flowing into it.

The output current and protection device current vs. input current curves are measured and shown in Fig. 6. These I-I curves are plotted for different output loads which are 50 Ω, 10 Ω and 2 Ω. Fig. 6 (a) clearly shows for input currents below 1 A the switch state matters. The switch remains open, i.e., the output current is zero. Once the input current reaches 2 A, the

ESD will force the switch closed. Thus, the input and the output currents are similar.

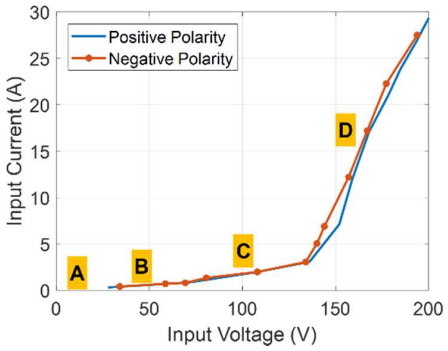

Fig. 5. Comparing the positive and negative input IV curve of the input pin for 50 Ω output load when the switch is open.

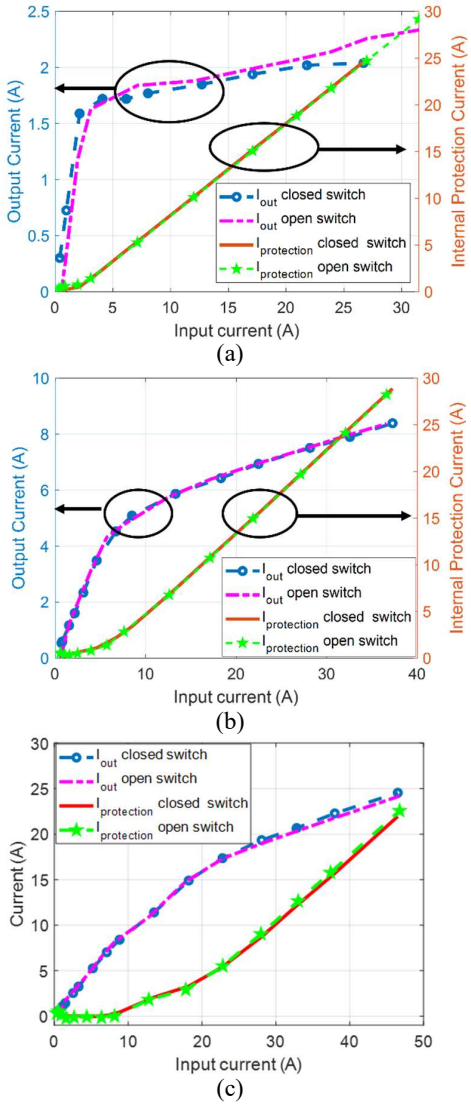

Fig. 6. Output current and internal protection current of the switch vs. input current for different output loads that are (a) 50 Ω, (b) 10 Ω, and (c) 2 Ω

The switch offers a low resistive path which is about 0.8 Ω. Thus, a small output load will force more current through the switch into the output. Fig. 6 (c) confirms this behavior. If the output load is small and its impedance is in the range of the internal protection device, both carry about the same current. By increasing the input current and regardless of the output load, the ratio between the current of the protection circuit and the output current increases: The protection circuit takes more and more current, thus, the maximal output current is limited. The limit itself, depends on the output load. The maximum measured input, output and the protection current is shown in TABLE I.

TABLE I. MAXIMUM OF THE INPUT, THE OUTPUT, AND THE PROTECTION CURRENT OF THE SWITCH

	50 Ω	**10 Ω**	**2 Ω**
Protection current (A)	27	27	23
Output current (A)	2	8	24
Input current (A)	29	35	47

The measurement results, summarized in TABLE I, for high input currents show that the device is very robust against the ESD events. The portion of current flowing into the protection device determines the damaging threshold which is the change of leakage current at the input pin. The measurements show that the switch is damaged when the current in the internal protection device exceeds 25 A for a 2 ns pulse. The robustness of the switch and the fact that it passes the ESD current suggests that the focus of the ESD protection should be expanded to include the stage that follows the switch.

IV. EVALUATING THE ESD BEHAVIOR OF AN AMPLIFIER

A low noise amplifier is considered as the next IC after the switch and its ESD behavior has been measured using the same TLP system for both polarities and different pulse widths to obtain its damaging threshold. The damage can manifest itself as a change in gain, noise figure or DC current. The measurements are done from low TLP voltages and after each discharge these parameters are checked to find the damaging threshold.

The measurement results show that this amplifier does not have any protection device for the positive and negative polarities as the input impedance of the amplifier remains constant and in the range of 50 Ω when the pulse level is increased. It is robust for the positive pulses so that it remained intact for about 7 A input current but the damaging threshold for the negative pulses is very low so that the amplifier damages when its input current reaches -1 A for negative pulses. As the input impedance of the amplifier remains constant and equal to 50 Ω, the data presented in Fig. 6 (a) should be considered. They show that the output current of the switch will be limited to 2 A which represents 100 V output voltage without any damage to the switch. In addition, when the switch's input current is about 2 A which occurs at very low input voltages, e.g. about 100V, the output current is 1 A and according to our measurement, this portion of current is sufficient to damage the amplifier.

V. ESD21 MEASUREMENT IN THE RF CHAIN

Electronic product manufacturers are usually assessing the ESD robustness of an I/O by directly zapping the ESD gun into an exposed pin. The RF system investigated consists of two different high pass matching networks, the switch, and the low noise amplifier. The system allows to measure the switch's input voltage and the current after the matching

network. Further, the input voltage and current of the amplifier are captured. Fig. 7 shows the schematic of the test setup.

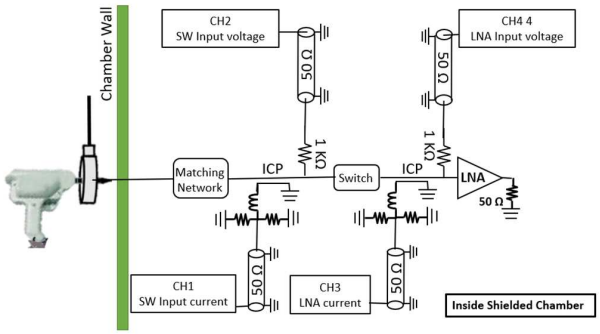

Fig. 7. ESD21 test setup including ESD gun, matching network, switch, LNA and the probes

TABLE II. THE COMPONENTS OF THE MATCHING NETWORKS

	L1 (nH)	C1 (pF)	L2 (nH)
Network 1	12	180	22
Network 2	20	12	7.5

The matching circuit is a pi network consisting of one series capacitor (C1) and two parallel inductors, (L1) before the capacitor and (L2) after. The values of these components are shown in TABLE II.

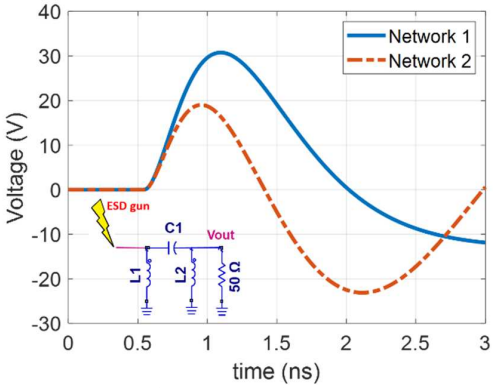

Fig. 8. Simulation results of ESD gun discharge into matching networks for 1 kV ESD gun

Simulation results for 1 kV ESD gun contact mode discharge to the circuits of TABLE II with a 50 Ω output load is shown in Fig. 8. The series capacitor in Network 1 is large and the length of the pulse that reaches the switch is about 1 ns. For Network 2, the pulse length after the matching circuitry would be narrower due to the smaller series capacitor value and the pulse length is about 600 ps. It is expected that the circuit with the smaller value of series capacitor be more robust than the other circuits. The results shown in TABLE III confirm this expectation.

TABLE III. THE MEASURED DAMAGING CONDITION OF THE LNA FOR TWO MATCHING NETWORKS IN THE ESD21 EXPERIMENT

	Network 1		Network 2	
	Gun voltage required for damage	**LNA damage threshold**	**Gun voltage required for damage**	**LNA damage threshold**
closed	-2 kV	-50 V	-4 kV	-50 V
open	-3 kV	-50 V	-8 kV	-50 V

The damaging conditions of the amplifier in different situations are shown in TABLE III. Measurement are made using the ESD gun contact mode discharge for the open and closed states of the switch. The same matching networks in the TLP measurement are used in this experiment. The results confirm those obtained from the TLP measurements of the standalone amplifier, which were -50 V of the amplifier input voltage in all situations. The results show that when the series capacitor is larger, the amplitude of the pulse that reaches the IC is higher and the next stage amplifier damages at lower ESD gun voltages. On the other hand, the status of the switch has an effect on the ESD gun voltage at which the amplifier is damaged. The gun voltage damaging threshold is higher when the switch is open as it needs higher voltages until the switch closes and the ESD event reaches the amplifier. It should be noted that in the aforementioned case the voltage across the series capacitor of the matching's network is not that high until the series capacitor sparks.

VI. CONCLUSION

ESD events can reach the antenna via different mechanisms. The ICs that are used as antenna tuner or matching tuners are the first endangered ICs after the antenna. They can be selected to be robust enough against ESD events. In this paper the ESD behavior of one of these RF switches is highlighted to warn the system designers of the possibility of the ESD event that may pass through the RF switches and reach the next stage in the RF front-end and cause hard failure. In this regard, a LNA is considered as the next stage IC after the switch, and it is shown that this amplifier can be damaged by the ESD event while the switch remains intact. The damaging threshold depends on the matching circuitry before the switch, the switch's ESD behavior and its status. This emphasizes the importance of designing the RF-front end protection based on the SEED approach.

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