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An Analysis on the Effectiveness of 2 and 3 Terminal Capacitors in PDN Design

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***Abstract*—The parasitic inductance of a capacitor depends on its physical structure. Due to the geometry of 3-terminal capacitors, they boast a lower parasitic inductance compared to 2-terminal capacitors of the same and possibly smaller package sizes. While the parasitic inductance of a single 3-terminal capacitor may be lower, using multiple 2-terminal capacitors may result in similar performance. In this work, the inductance of 2-terminal (0201, nominal 2.2 uF) and 3-terminal (0402, nominal 4.3 uF) capacitors is extracted and compared through measurements. From our de-embedding method and characterized capacitors, the inductance of 2-terminal capacitors is only about ~20 pH higher than the characterized 3-terminal capacitor. On a power net of a real product, 3-terminal capacitors of the same type as characterized were replaced with 2-terminal capacitors of the same type as characterized. From measurement results, the measured inductance at 100 MHz is lower by only about 3.45 pH, or 2.62%, when using 3-terminal capacitors.**

Keywords— Power distribution network, decoupling capacitors, inductance, ESL

I. Introduction

In the design of power distribution networks (PDNs) for printed circuit boards (PCBs), decoupling capacitors may be used to filter out noise or act as a temporary source of charge. The performance of a decoupling capacitor depends heavily on its inductive parasitics, characterized as its equivalent series inductance (ESL), and is a function of the capacitor geometry. The 'common' multi-layer ceramic capacitor (MLCC) is the 2-terminal capacitor, whose ESL is directly related to the package size. Via placement and routing strategies aside, smaller package capacitors translate to lower inductances when compared to larger package capacitors of the same design. To further reduce the inductance contributed by the capacitor body, many other capacitor geometries have been explored. Among them, there exist multi-terminal capacitors, such as the 3, 8 and even 10-terminal capacitors [1], which leverage both multiple and shorter internal current paths for much lower ESL, often lower than even 2-terminal capacitors of comparably smaller package size.

Even 3-terminal capacitors can have much lower parasitic inductance compared to 2-terminal capacitors of equivalent or even smaller package sizes [2][3]. For this reason, lower loop inductance and lower PDN impedance can be achieved by using 3-terminals or using 3-terminals in combination with 2-terminals. The total board space needed and number of components used may also be reduced. The caveat though, is an increased number of vias for 3-terminal capacitor pads, and more careful trace routing and power/ground plane designs may be required to accommodate.

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While the per-unit inductance of a 3-terminal capacitor may be lower than that of a 2-terminal capacitor, multiple 2-terminal capacitors may still be comparable in performance to a single 3-terminal. It may be that the advantage of 3-terminal capacitors in some cases, and heavily depending on the particular capacitor in question, is overstated. Depending on the design and designer, multiple 2-terminals of particular types may cost less compared to individual 3-terminals and be a competitive alternative.

In this paper, the performance of an available 2 and 3-terminal capacitor is compared. Fixtures for capacitor characterization are manufactured, with the inductances of the capacitors extracted through measurement. In addition, the performance of multiple of the 2-terminal capacitors are compared with single 3-terminals by looking at the measured loop inductance including the test fixture inductance.

For validation, simulation and measurements are performed on a real product using 3-terminal capacitors of the same type as characterized. In simulation, the extracted impedances and inductances are compared when using 3-terminals, and when replacing the 3-terminals with 2, 2-terminal capacitors of the same type as characterized, using both experimentally measured models and vendor provided models. To validate the simulations, measurements on the real product are performed using both 2 and 3-terminals.

II. 2 and 3-Terminal Capacitor Structure

The internal structures of the 2-terminal and 3-terminal MLCC are given in Fig. 1. For a simplified view, the internal structure of the 2-terminal MLCC is made up of a series of metallic and dielectric layers [2]. Each set of metal-dielectric-metal layers forms a single parallel capacitor plate pair, with multiple sets of metal-dielectric-metal layers used to increase the total capacitance. Metallic terminals at the ends of the capacitor connect the capacitor to the rest of the board. Current travels from the board, up a metallic terminal, along the horizontal metallic sheets, and through displacement current, travels from metal layer to metal layer. The current then exits through the other terminal to a return of the PCB board. The current flow path is one-way.

The 3-terminal capacitor is made up of 2 power terminals and 1 return terminal. Internally, the capacitor consists of the same metallic-dielectric-metallic layers. The orientation of the metallic layers, however, is alternating, with one metallic layer internally connecting the power terminals, and the next layer, the return terminals [2]. The result is that the displacement current reaching the ground-terminal-metallic plates has two parallel, but also shorter paths from power to return, when compared to a 2-terminal of the same size. As a result, the inductance is reduced. 3-terminal capacitors

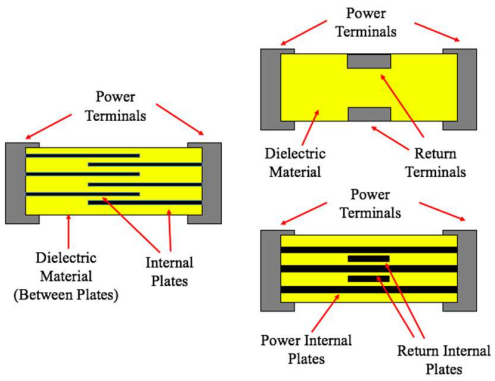

Fig. 1. Internal structure of the 2-terminal capacitor (left), top-down external view of 3-terminal capacitor (top right), and internal side view of 3-terminal capacitor picturing internal plates (bottom right).

can be mounted in either a shunt or feedthrough configuration, where for the shunt configuration, the power terminals are connected to the same continuous plane, and in the feedthrough, the power terminals join disconnected power planes [4]. Depending on the configuration, the behavior and parasitics seen may vary.

III. Fixture Design

The 3D model for the 2-terminal capacitor fixture and the corresponding de-embedding fixture used for characterization is shown in Fig. 2. The designs are two-layer boards, with FR-4 dielectric at 0.1 mm thickness, a solid bottom signal layer, and a solid top return layer. Horizontal rectangular pads are used for micro-probing. Vias on the outer rectangular pads carry current down to the bottom plane. The current travels along the bottom plane, up the vias below the capacitor pad, through the capacitor body, across the top plane, then to the return of the microprobes. For de-embedding, a short trace shorts the capacitor pads.

The 3D model for the 3-terminal capacitor fixture and the corresponding de-embedding fixture is given in Fig. 3. The fixture is also of a two-layer design, with the same thickness and via connections between planes. Vias connect to both signal pads of the 3-terminal capacitor. For de-embedding, the signal pads are shorted to the return pad with traces. For this fixture, the bottom signal layer is solid, so the 3-terminal capacitor when mounted is in the shunt configuration.

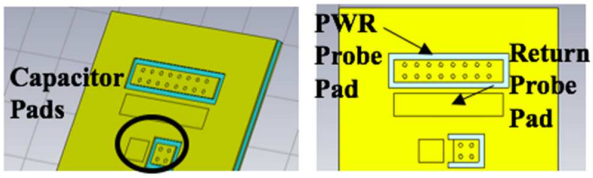

Fig. 2. Test fixture for 2-terminal capacitors (left), and de-embedding fixture (right).

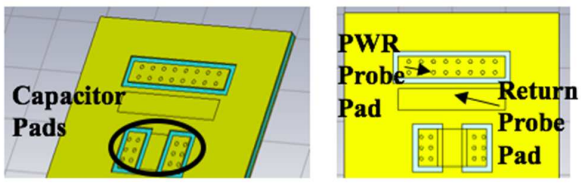

Fig. 3. Test fixture for a 3-terminal capacitor (left), and de-embedding fixture (right).

IV. Capacitor ESL Extraction

For ESL extraction, boards were manufactured based on the test fixtures of Fig. 2 and Fig. 3. The manufactured fixtures for the 2-terminal and 3-terminal fixtures are shown in Fig. 4. For de-embedding, the pads of the capacitor (as pictured in Fig. 4) are shorted together with a solder connection to emulate the shorting traces in Fig. 2 and 3. The thicknesses of the manufactured board match the thickness in 3D models (0.1 mm), so the effect of capacitor-to-plane mutual coupling on the extracted capacitor inductance should be the same in measurement as in simulation [5].

For the extraction of the capacitor ESL, 2-port measurements are performed for more accuracy [6]. The S21 is measured and converted to Z21 using (1) [5]. Micro-probes, calibrated up to the tip using a calibration substrate, were used for measuring and landed on the horizontal, rectangular pads at the top of the fixture.

$$Z_{21} = 25\frac{S_{21}}{1-S_{21}} \tag{1}$$

For removing the contribution of the fixture, (2) is used, where Z_{cap} is the extracted impedance of the capacitor with fixture contribution removed, $Z_{cap+fixture}$ is the extracted impedance of the fixture with the capacitor mounted using (1), and Z_{short} is the impedance of the short fixture used for de-embedding also extracted using (1) [7].

$$Z_{cap} = Z_{cap+fixture} - Z_{short} \tag{2}$$

In addition to the 2-terminal and 3-terminal characterizations, two 2-terminal capacitors were soldered onto the pads of the 3-terminal fixture. Measurements were taken without de-embedding. The inductance is extracted and compared with the inductance when the 3-terminal capacitor is mounted to the fixture. Fig. 5 shows the 2-terminal capacitors mounted to the 3-terminal pads.

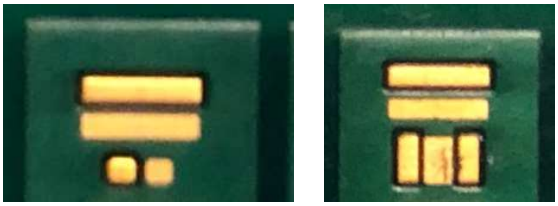

Fig. 4. Manufactured 2-terminal (left) and 3-terminal (right) test fixtures.

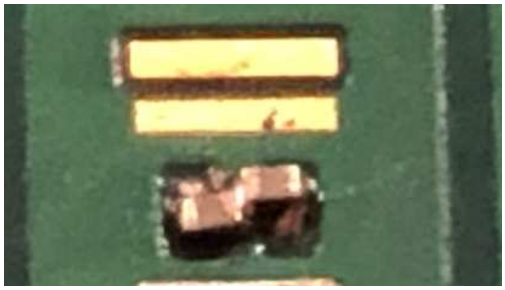

Fig. 5. 2-terminal capacitors soldered on 3-terminal pads.

A. Extracted Inductances

The general specifications for the capacitors characterized are given in Table I, using nominal values from the datasheet, ESL extracted at 200 MHz from vendor provided S-Parameters, and for conditions of 0 V DC bias and 25 degree Celsius operating temperature. The same measurement conditions as the vendor model were used in the characterization (0 V DC, ~25 degree Celsius, or at least under no temperature extremes). The inductances are extracted at 200 MHz with the assumption that the capacitor would is acting wholly inductive in that region. While prices are omitted from Table I, for the real product design used later for validation, it has been stated by the product designers that at least the cost of two of the 2-terminals characterized is less than one of the 3-terminals characterized, at least at time of measurements.

From measurements, the extracted capacitor inductance (fixture contribution de-embedded) of the 2 and 3-terminals is given in Table II, at 200 MHz. Comparisons of the mounted 3-terminal inductance and mounted inductance when using two 2-terminal capacitors on the 3-terminal pads are given in Table III. The mounted inductance refers to the inductance when the capacitor is mounted to the fixture, without fixture de-embedding. Measurements for each test case, without reusing capacitors, are given in Tables II and III.

The extracted inductance of a single 2-terminal capacitor is about 20 pH higher than that of the 3-terminal. The difference in inductance when comparing the mounted 3-terminal capacitor to two, 2-terminal capacitors was at most 7.26 pH or 6.89%. The performance of using two 2-terminal capacitors, at least with the capacitor and fixture design used, is comparable to using a single 3-terminal.

There is a variation in the inductance extracted for the single 2-terminal capacitor, and while that difference may be due to measurement and de-embedding error, it may also be due to a possible variation in extracted inductance due to capacitor plate orientation [8][9]. To check, the exact same capacitors used in the 2-terminal measurements were carefully rotated on the fixture, and the inductance again extracted. By rotating the capacitors on the pads, the orientation of the internal capacitor plates relative to the plane of the fixture was changed. The extracted inductances when rotating the 2-terminals are given in Table IV. The variation in extracted inductance for the 2-terminals was in the range of ~8 to ~20 pH, but it could be likely that the variation could be due to other causes like damage to capacitors or capacitor pads from soldering/de-soldering, or to overall variation in soldering quality.

TABLE I. CHARACTERIZED CAPACITORS SPECIFICATIONS

Specs.	2-Terminal	3-Terminal
C	2.2 uF	4.3 uF
ESL (@ 200 MHz)	150.54 pH	52.13 pH
Rated Voltage	4 V DC	4 V DC
Temp.	-55 – 85 C	-55 – 85 C
Size	0201	0402

TABLE II. EXTRACTED 2 AND 3-TERMINAL CAPACITOR INDUCTANCES (FIXTURE INDUCTANCE REMOVED) AT 200 MHZ

Sample	2-Terminal	3-Terminal
1	61.11 pH	38.73 pH
2	67.07 pH	38.63 pH
3	54.22 pH	41.91 pH

TABLE III. EXTRACTED MOUNTED INDUCTANCES (CAPACITOR + FIXTURE INDUCTANCE) OF TWO, 2-TERMINAL AND 3-TERMINAL CAPACITORS

Sample	Two 2-Terminal	3-Terminal
1	106.87 pH	99.51 pH
2	104.70 pH	99.41 pH
3	104.67 pH	102.68 pH

TABLE IV. EXTRACTED 2-TERMINAL CAPACITOR INDUCTANCES AFTER ROTATION OF CAPACITOR BODY

Sample	2-Terminal	2-Terminal Rotated
1	61.11 pH	53.05 pH
2	67.07 pH	46.75 pH
3	54.22 pH	66.60 pH

The extracted impedances of each 2-terminal capacitor, for the data in Table II, along with the vendor provided model, is given in Fig. 6. The main point of interest is the much lower impedances extracted at higher frequencies of the measured models compared to the vendor model. The inductance extracted from the vendor model at the measured point nearest 200 MHz is 150.54 pH, about 80 – 100 pH higher than what was characterized. The de-embedding method used by the vendor is briefly explained in [10], but the exact details are not clear and it is difficult to determine what information about the capacitor is being captured by the model. For the characterization method described in this work at least, de-embedding was performed by shorting the capacitor pads with solder. The current path taken in the de-embedding fixture should then be similar if not the same path taken for when the capacitor is mounted to the test fixture. Some amount of the inductance associated with the length of the capacitor, is therefore removed during de-embedding. While the differences with the vendor method is unknown, de-embedding of the length associated with the capacitor should be more appropriate, especially with 3D solvers. By having a de-embedding fixture that, to some extent, removes the inductance associated with the length of the capacitor, the inductance associated with generated ports in 3D solvers can be accounted for in the measured model and not double counted in simulation [11].

As for why the self-resonance point is much lower for the measured models, it may be that the solder connection used for de-embedding had too high resistive losses compared to the capacitor resistance. When removing the fixture contribution then, the resulting impedance around the self-resonance is lower and probably inaccurate.

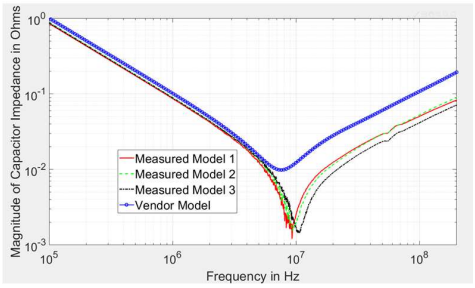

Fig. 6. Impedances for measured 2-terminal capacitor and vendor model.

B. Simulation Verification of Measurement

For simulation verification, the fixtures were recreated in CST and 2-port simulations were performed. The simulation setups are given in Fig. 7 and 8, for the 2 and 3-terminal fixtures, respectively.

Lumped elements connect the signal pads to the ground pads of the capacitors. For the 2-terminal fixture, lumped inductance values of 46.75 pH and 67.07 pH were assigned. For the 3-terminal fixture, for each of the lumped elements, an inductance value of 77.26 pH (2 × 38.63 pH) is assigned. The assumption is that there are two signal pads for current to travel through, and so the lumped elements act in parallel. The equivalent inductance from the lumped elements is then expected to be half the assigned value. In simulations, the inductance with the lumped elements and without de-embedding, is extracted at 200 MHz. The simulation results are compared with the mounted capacitor inductances extracted from measurements, with the results given in Table V. The correlation between measurement and simulation is close, with a max error of 5.22 pH (3.34%) for the 2-terminal case, and 5.89 pH (5.59%) max error for the 3-terminal case.

V. Simulation and Measurement In A Real Product

On a particular power net of a real product, multiple 3-terminal capacitors, of the same type as characterized, are used and placed in the shunt configuration. For verification, each 3-terminal capacitor is replaced in simulation and measurement with two 2-terminal capacitors, of the same type as characterized. The total capacitance provided remains about the same. In simulation, the two 2-terminal capacitors were simulated using measured and vendor provided S-Parameters. In both simulation and measurement, the 2-terminal capacitors (0201 size) are placed on the pads of the 3-terminal capacitors (0402 size). As a result, the total board area used is unchanged. This may not be true for other capacitor substitutions, but for the product used, the total board space and routing when using the 2-terminals is the same as that used when using single 3-terminals. In addition, the S-Parameters of the vendor models are under 0 V DC bias and at 25 degree Celsius.

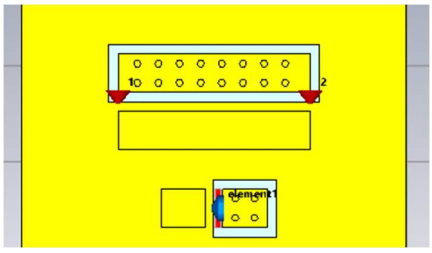

Fig. 7. Simulation setup for 2-terminal fixture.

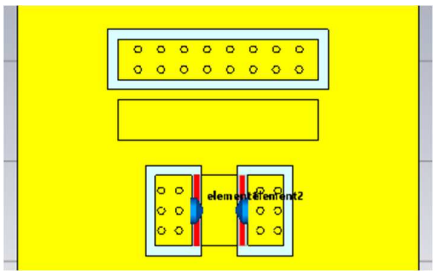

Fig. 8. Simulation setup for 3-terminal fixture.

TABLE V. Extracted Mounted Inductances (Capacitor + Fixture Inductance) Comparing Simulation and Measurement

Case	Simulation	Measurement	% Error
2-Terminal (46.75 pH)	156.26 pH	151.04 pH	3.34%
2-Terminal (67.07 pH)	177.25 pH	171.36 pH	3.32%
3-Terminal	105.30 pH	99.41 pH	5.59%

A. Simulation Result in Real Product

Fig. 9 depicts the placement of two 2-terminal capacitors on the pads of the 3-terminal capacitors in Cadence PowerSI. 2-port simulations were done by creating ports on BGA balls of the relevant net.

Fig. 10 gives the simulated impedance curves for: 1) using the vendor-provided model for the 2-terminal capacitor at 0 V DC bias and 25 degrees Celsius [12], 2) using measured S-Parameters (46.75 pH extracted model) for the 2-terminal capacitor, and 3) using measured S-Parameters (67.07 pH extracted model) for the 2-terminal capacitor.

Fig. 11 gives the simulated impedance curves, for 1), using the vendor-provided model for the 3-terminal capacitor, in the shunt configuration, at 0 V DC bias and 25 degrees Celsius [12], 2), using vendor-provided models for the 2-terminal capacitor at 0 V DC bias and 25 degrees Celsius, and 3), using measured S-Parameters for the 2-terminal capacitor (67.07 pH extracted model).

From the simulated impedances of Fig. 10, the inductance was extracted from the imaginary part, at an interested frequency point of 100 MHz. Simulation using the vendor 2-terminal model simulation gives 154.43 pH. The measured S-Parameters (46.75 pH model) used for simulation gives 126.89 pH (17.83% difference) and 131.46 pH (14.87%, 67.07 pH model). The differences in the de-embedding between vendor models and the measured models resulted in a difference of ~23-28 pH.

At the second resonance point in the impedance curves of Fig. 10 and 11, there is a mismatch in amplitude between simulations using the vendor model and measured models. That mismatch could come from the excess resistance of the solder bridge used for de-embedding like in Fig. 6. The first resonance point comes from larger size decoupling capacitors on the net, which were not characterized, and used vendor models in simulation.

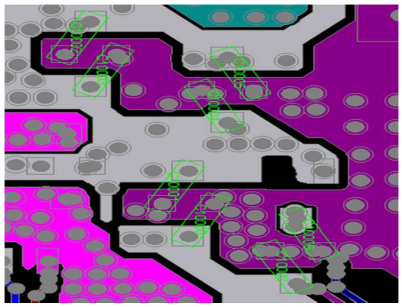

Fig. 9. Placement of 2-terminal capacitors on 3-terminal pads in simulation

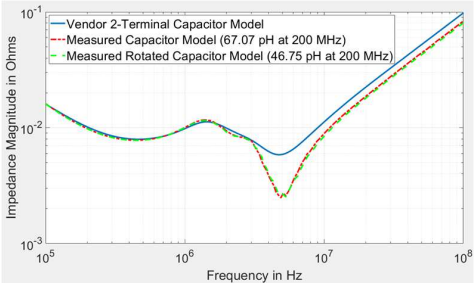

Fig 10. Simulated impedance curves comparing the vendor 2-terminal model with measured 2-terminal models.

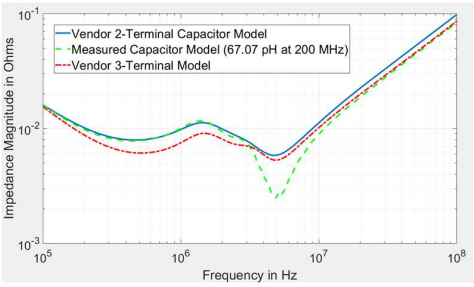

Fig 11. Simulated impedance curves comparing vendor and measured 2-terminal models with vendor 3-terminal models.

For the simulated impedances of Fig. 11, the extracted inductance at 100 MHz, for the simulation using the vendor model of the 3-terminal capacitor, is 135.16 pH. Depending on the measured 2-terminal capacitor model used for simulation, the inductance using 2-terminal capacitors is lower by only about 4-9 pH. This difference is for practical purposes not too relevant, but the use of 2-terminal capacitors in simulation seem competitive with using 3-terminals, with the caveat of measurement and de-embedding variability/accuracy of the models used in simulation.

B. Measurement Result in Real Product

For measurement validation, on the same power net as in the simulation, measurements were performed with 3-terminal capacitors and with 3-terminals removed. Two 2-terminal capacitors were soldered to the 3-terminal capacitor pads, as shown in Fig. 12. Two-port measurements were performed on the BGA balls with microprobes as pictured in Fig. 13. The measurement was performed at room temperature, or at least not in any temperature extreme, and with 0 V DC bias applied to the capacitors.

Fig. 14 plots the Z21, extracted from the S21, comparing the impedance when using 3-terminal capacitors vs using 2-terminal capacitors. The inductance extracted using 3-terminals at 100 MHz is about 128.31 pH, compared to about 131.76 pH using 2-terminals. The difference is only about 3.45 pH, or 2.62%. Compared to the simulation results of Fig. 11, the simulated inductance at 100 MHz using the measured model was about 131.46 pH, a very good match with the measurement. Simulation using the measured 46.75 pH model of Fig. 10 however, predicts a slightly lower inductance of 126.89 pH; a mismatch of about 5 pH (3.7%).

While in the inductive region the measurement correlates well with the simulation, there is a major difference that can be observed between the measurement of Fig. 14 and the simulation of Fig. 11. Looking around the first resonance

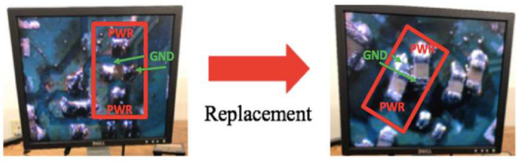

Fig 12. 2-terminal capacitors on 3-terminal pads.

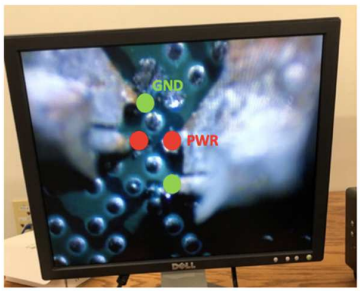

Fig 13. Micro-probing on BGA Balls.

point, the measured impedance is much lower than in simulation. This mismatch may be attributable to a difference in the resistive part of model of the responsible for the first resonance point. That larger size capacitor however, was not characterized in this work. Fig 15. plots the real part of 1) DUT measurement using 2-terminals, 2) simulation of DUT using measured 2-terminal models (67.07 pH), and 3), simulation of DUT using vendor 2-terminal models. From Fig 15, around the first resonance, the measured resistance is lower by about 3 mOhms, indicating that the vendor model of the larger size capacitor is including some additional resistance. In contrast, at the second resonance point, the simulation with the measured models has a lower resistance than in measurement, again likely due to the de-embedding process, whereas the simulation with vendor models has a larger resistance compared to measurement. In either case, it is likely that neither the vendor models nor the measured models is accurately capturing the resistance associated with the capacitor, with the true value lying in between, and in between the two de-embedding methods.

The measurements performed were done within limited measurement conditions; changes in capacitor behavior due to the operating temperature or applied DC biases would also affect the impedance seen. While not characterized in measurement, additional simulations was performed using vendor models of the 2 and 3-terminal capacitors with the real product. Vendor models under a 3 V DC bias and an operating temperature of 70 degrees Celsius were used, and the simulation results compared with vendor models under 0 V DC bias at 25 degrees Celsius (as used in Fig 10 and 11), in Fig. 16. Depending on the operating conditions, there can be significant changes in the measured impedances, which may result in insufficient performance.

VI. Conclusion

Due to their internal structure, single 3-terminal capacitors provide much lower parasitic inductance when compared to single 2-terminal capacitors of the same and possibly smaller package size. However from measurement and simulation results, specifically for the capacitor models used, the measurement conditions (0 V DC bias, at room temperature), and the real product used for validation, using

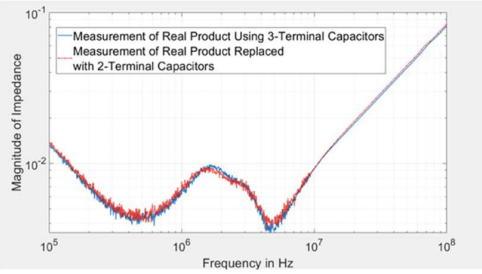

Fig 14. Measured impedance using 3-terminal capacitors vs. 2-terminal capacitors.

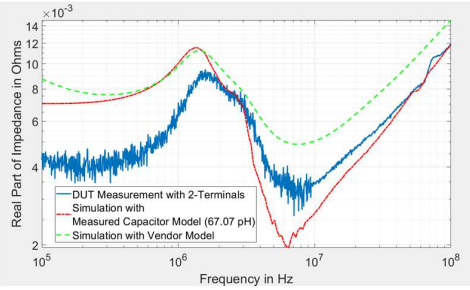

Fig 15. Comparisons of the real part of the impedance, between simulation and measurement of a real product.

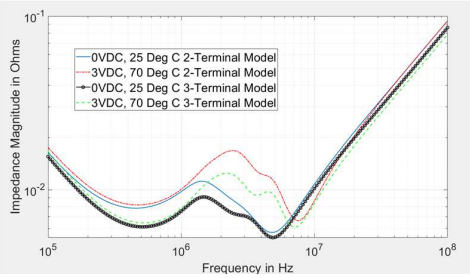

Fig 16. Simulation results of real product, using 2 and 3-terminal capacitors. Conditions of 0 V DC bias at 25 degree Celsius operation, vs 3 V DC bias at 70 degree Celsius operation.

two, 2-terminal capacitors of the same type characterized is comparable in inductance (at 100 MHz) to a single 3-terminal capacitor of the same type characterized. For a real use case, 3-terminal capacitors used on a power net of a real product were replaced with two 2-terminal capacitors, with the measured inductance using 3-terminals lower by only about 3.45 pH, or 2.62%, at 100 MHz. The inductive performances for this test case is about the same using either 2 or 3-terminals. In simulation, it was shown that under different operating conditions, substitution from 3-terminals to 2-terminals may significantly change the impedance, especially in the lower frequency region, and substitution to 2-terminals may not be always viable. For cost, while the exact numbers has been kept confidential, per the product designers and at the time of measurement, the cost of two of the characterized 2-terminals is less than the cost of one of the characterized 3-terminals.

For measurements using the real product, the 2-terminal capacitors (0201 size) are soldered directly on the pads of 3-terminals (0402 size) originally used in the design. The total board space used for this test case is unchanged but this may not be true for other package size substitutions. Similarly, as the 2-terminal capacitors fit neatly on the 3-terminal pads, the same routing is used. If the substitution is from a larger to a smaller package size, depending on the number of capacitors used and allowed space, it may be possible to route by using the same/similar pad placements and pad sizes of 3-terminals. Pads could also be shared by 2-terminals to increase the density of capacitors. Though if the substitiution were to a larger package size, the routing may be more complex and more board space may be needed.

3-terminal capacitors in the power net of interest were also placed in the shunt configuration rather than the feedthrough. 3-terminal capacitors in the feedthrough configuration can join together disconnected power planes and act like a low pass filter due to the internally connected plates. While 2-terminals can act as filters by shunting signals to the return, they cannot join disconnected power planes due to having no direct internal connection. They may also require a larger array of capacitor values placed in parallel to achieve the same bandwidth as a 3-terminal filter in feedthrough. 2-terminals capacitors likely cannot replace 3-terminals placed in the feedthrough, but could have comparable performance to 3-terminals for the purpose of decoupling (shunt configuration). Design and cost allowing, using multiple 2-terminal decoupling capacitors over a single 3-terminal decoupling capacitor could yield competitive or equal inductive performance, and may be worth further investigation depending on use case.

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