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System Level PDN Impedance Optimization Utilizing the Zeros of the Decoupling Capacitors

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***Abstract*—System-level power distribution network (PDN) impedance optimization utilizing the zeros of the decoupling capacitors (decaps) is discussed in this paper. An example of a practical PDN application is proposed to validate the poles and zeros algorithm (P&Z) presented. The system-level PDN is with the printed circuit board (PCB), package (PKG), and chip, as well as the low-frequency decaps on the PCB and the on-PKG decoupling capacitors. The PDN optimization results are compared with those from the genetic algorithm (GA) to show the reasonableness and validity of the P&Z algorithm.**

Keywords—System level PDN, decoupling capacitors, poles and zeros algorithm, genetic algorithm, PDN impedance optimization

I. INTRODUCTION

The power integrity (PI) design is a challenging problem in processor chips and other electrical systems with large current draw. The power distribution network (PDN) delivers the supply voltage to the circuits in the system. To meet system stability requirements, the PDN should be designed to have a low input impedance looking in from the IC port that is lower than the target impedance [1].

The simplified system-level PDN contains the printed circuit board (PCB), the package (PKG), the chip, the interactions of the PCB – PKG and the PKG – Chip, as well as the electrical components such as the decoupling capacitors (decaps), inductors, and resistors on the PCB, PKG, and chip. The inductance of the current path on the PCB is the dominant part of the large PDN impedance and should be optimized to ensure the effectiveness of the design. Different capacitances and associated inductances from the above-mentioned parts can lead to a solution to lower the PDN input impedance over a wide frequency range.

A schematic representation of the system level PDN impedance is shown in Fig. 1. The bulk, or low-frequency decaps on the PCB have a large charge storage capacity and are effective at low frequency. The SMT decoupling capacitors on the PCB are effective at the middle-frequency range of tens to hundreds of megahertz depending upon the target impedance. The PKG impedance model is also dominated by the inductance but with the on-PKG decaps, the system PDN impedance at tens of megahertz can be reduced. The chip capacitance is utilized to suppress the high-frequency noise because of the closest distance to the load, and thus the least loop inductance at the location of chip capacitance.

There are some studies focusing on the behavior of the system-level PDN. A physics-based circuit modeling methodology for the system-level power integrity analysis and design is detailed in [2]. The work in [3] focuses on the transceiver system and the transmitter phase noise. A design guideline to model PDN agilely in a simplified method is given in [4]. As for the optimization of the decoupling capacitors, several algorithms are proposed and studied based on different methods. A non-random exploration-based method to optimize the response of the power delivery network (PDN) using the minimum number of capacitors is proposed in [5]. Decap selection for different patterns is studied in [6]. A fast capacitor assignment algorithm capable of finding the decoupling solution scheme is given by [7]. The genetic algorithm (GA) has also been utilized to achieve the target impedance [8]-[9].

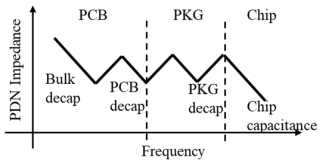

Fig. 1. System-level PDN impedance

In this paper, a decap selection algorithm – the Poles and Zeros Algorithm (P&Z) is herein developed using the zeros of the decoupling capacitor with the inductance of the current path to optimize the system-level PDN impedance. The algorithm validation is done by applying a practical PDN system with PCB, package, and chip. The decap selection using the poles and zeros algorithm is conducted at different levels of the PDN system. The PDN optimization performance is compared with the genetic algorithm.

II. SYSTEM PDN MODELING AND OPTIMIZATION METHODOLOGY

A. PDN Impedance Matrix Computation

To optimize the PDN impedance, the PCB PDN is first modeled based on the physical structure and converted to the impedance matrix to represent the combined inductance, capacitance, conductance, and resistance terms, as well as the connections between the vias and planes. The modeling approach is detailed in [10], with the approach of cavity segmentation, RLGC calculation, via-plane connection identification, impedance matrix built using a node-voltage method, and KCL theory [11]. A PCB PDN impedance matrix with one PCB IC port and several ports for decoupling capacitors connection can be obtained.

For the system-level PDN impedance matrix computation, the PKG and Chip impedance models need to be cascaded with the PCB impedance model. The PKG and Chip can be simplified as a 2-port model [12], as shown in Fig. 2, and based on the system hierarchy, the PCB, PKG, and Chip model can be connected following the current direction through the system using the n-port S-parameter cascading

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methodology proposed in [13]. After this step, the PDN impedance matrix is with 1 input port from the chip side and several ports for the capacitors. The system with PCB, PKG, and Chip is ready to optimize using the decoupling capacitors.

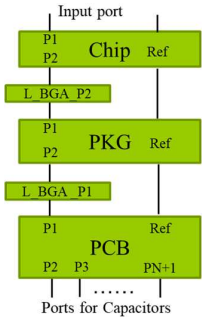


Fig. 2. Schematic of system level PDN with the simplified port assignment.

Correctly selecting the capacitors is required to effectively optimize the PDN impedance. The decap selection algorithm will be introduced in Section II. B. During the process, the capacitors need to be cascaded to the system PDN impedance matrix, and a 1-port decap equivalent model is utilized [14]. With the cascaded decoupling capacitors, if the system level PDN impedance is below the target impedance within the frequency range of interest, the design is finished. Otherwise, if the maximum possible number of decaps is reached and the PDN impedance is still above the target impedance, the design fails.

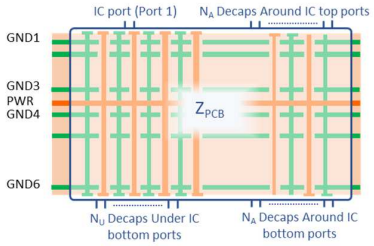


Fig. 3. Impedance matrix for PDN optimization [9].

B. Poles & Zeros Algorithm

Before placing the capacitors, the location of the decap is determined first. The PCB PDN has been represented as an impedance matrix with N_u decap ports for under IC locations and $2*N_A$ decap ports for around IC locations as shown in Fig. 3. Because the IC power vias are grouped as one single port on the top layer, for the N_u decaps that can be placed under the IC, the introduced loop inductance can be regarded as the same. For the around IC $2*N_A$ decaps, the keep-in area for the decap placement is determined based on the power net area-fill shape, and in each keep-in region, there is a grid of possible decap locations with a specific pitch size. Further details about the decap port locations are provided in Section III. A and Fig. 6. With the determined possible decap locations, firstly, the board side to put the decaps on is determined. If the power net area-fill layer is closer to the top layer, then the top board side will be used for decap placement. Otherwise, the decaps will be placed on the bottom board side. The capacitors that are determined will first be placed at the vias closer to the IC center with smaller loop inductance, and the capacitors selected later will be located farther out from the center.

The capacitance, equivalent series inductance (ESL) and equivalent series resistance (ESR) value of the decap, together with a portion of the current path inductance of the connection will form the zero in a specific frequency in the decap impedance profile. However, when the decap is placed on the board, the equivalent inductance above the top ground plane looking into the decoupling capacitor L_{PCB_above} [15] will be introduced. The loop resistance from the associated vias is also considered in forming the resonance. If a decoupling capacitor is placed on the PDN with a certain resonance frequency, the PDN impedance will be reduced at the corresponding frequency. The PCB plane inductance L_{PCB_Plane} and via inductance L_{PCB_decap} [16] associated with the introduced decap will also be included by enabling the corresponding via branch in the impedance matrix.

The poles and zeros algorithm (P&Z) proposed for the decap selection is based on the frequency difference between the intersection frequency *f1* of the PDN impedance and target impedance, and the decap resonance frequency *f2* as shown in Fig. 4. There are four decaps showing the different resonance frequency *f*2 in dots of different colors, and for each *f*2, the frequency difference to *f*1 is regarded as the value Δf. The algorithm starts to handle the impedance violations from low frequency to high frequency. The decaps are limited to the capacitance values in a specific decap library, but this can be changed for different designs. For each frequency point *f1* where the PDN impedance exceeds the target impedance, for each type of decap, the algorithm will calculate the resonance frequency *f2* of the decap formed by the inductance (including the loop inductance after adding the decap, and the ESL of the decap) and the capacitance of the decap. Among all the resonance frequencies, a resonance frequency *f2* that is closest to *f1* is identified as the resonance frequency from Decap 1 with smallest Δf in Fig. 4, and the corresponding decap is selected. After placing the decap, the PDN impedance at the frequency *f2* closest to *f1* will be reduced. And then the next *f1* at higher frequency where there is an impedance violation will be determined, and the same process of selecting the decaps is repeated.

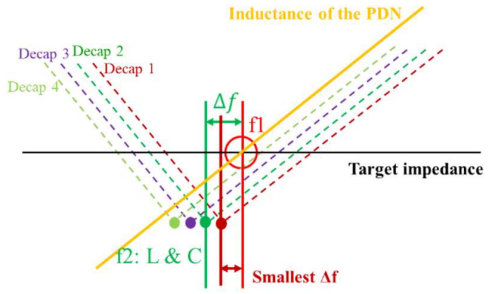


Fig. 4. Example for the poles and zeros algorithm

The decap selection process is implemented from low frequency to high frequency to ensure the PDN impedance can be optimized within the entire frequency range of interest. This decap selection algorithm is valid for any type of target impedance since it only focuses on the frequency of a target impedance violation.

III. Application Example

A. PCB Model

The specific PCB model used as the application example in this paper has a stack-up as shown in Fig. 5. The layers in blue are the ground layers. The power-net area-fill layer is at the 11th layer counting from the topmost layer shown in red,

with a supply voltage of 1.2 V. The layers in yellow represent the dielectric layers.

The IC pin map, power net area fill, as well as the possible decap locations are shown in Fig. 6. The total area of the PCB is 5000×5000 mil^2. The IC pin map is shown in blue dots (ground vias) and red dots (power vias) in the center and right side. There are 29 possible locations to be used to place the decaps under the IC shown as indicated by the black lines between the red dots and blue dots. There are 3 low-frequency decaps placed on the PCB top layer as shown in Fig. 6 (a) in thick black lines at the left top corner. There are 6 low-frequency decaps placed very close to the IC on the PCB bottom layer as shown in Fig. 6 (b). The capacitance of the low-frequency decaps is 100 µF. The low-frequency decaps are always considered before the PDN impedance optimization to ensure the PDN impedance at low frequency can meet the target impedance. There are 122 doublet pairs of decap locations available around the IC decap keep-in area in the yellow region of Fig. 6 (a). The red dots represent the power vias of the decaps and the green dots represent the ground vias of the decaps. The decap pairs used are limited to 100 pairs considering the cost and the area for placement of on-PCB components.

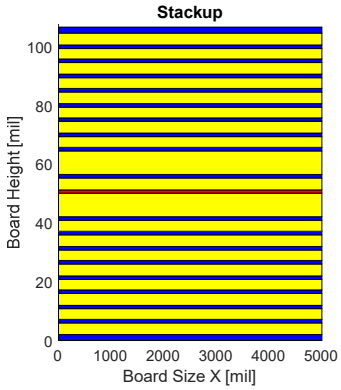


Fig. 5. The stack-up of the example production PCB. The power net area fill is at the 11th conductive layer counting from the top.

B. PKG Model

Using the PowerSI simulation tool, the PKG model with the corresponding power net to the PCB is simulated as a 5-port S-parameter model. One port is defined to connect with the PCB, one port is reserved for the Chip connection, and the others are for three 2 µF on-PKG capacitor connections. The ESL (considering the L_{above}) and ESR of the capacitors are 35 pH and 10 mΩ, separately. The interaction inductance of the BGA balls for PKG-PCB connection and Chip-PKG connection is also considered and modeled. The input impedance of the PKG model with and without the on-PKG capacitors is shown in Fig. 7. The detailed information on the PKG model can be found in [12].

C. Chip Model

The chip model is represented by the equivalent capacitance and resistance values. The chip capacitance is not specified but can be approximated by 50 nF per Ampere of current from experience with this type of design. The power net of interest for the PCB model of this application example can handle a maximum of 2.5 A DC current from the chip. The chip capacitance can herein be calculated as 125 nF. The chip resistance is estimated at 0.12 mΩ.

D. Target Impedance

Considering the PCB power supply voltage of 1.2 V, the allowed voltage ripple of 1.46%, IC DC current of 2.5 A, and the current derating factor of 0.5, the target impedance is approximately 14 mΩ calculated as

$$Z_{target} = \frac{power\ supply\ voltage \times allowed\ ripple}{\max DC\ current \times current\ derating\ factor} \quad (1)$$

within the target frequency range from 100 kHz to 50 MHz.

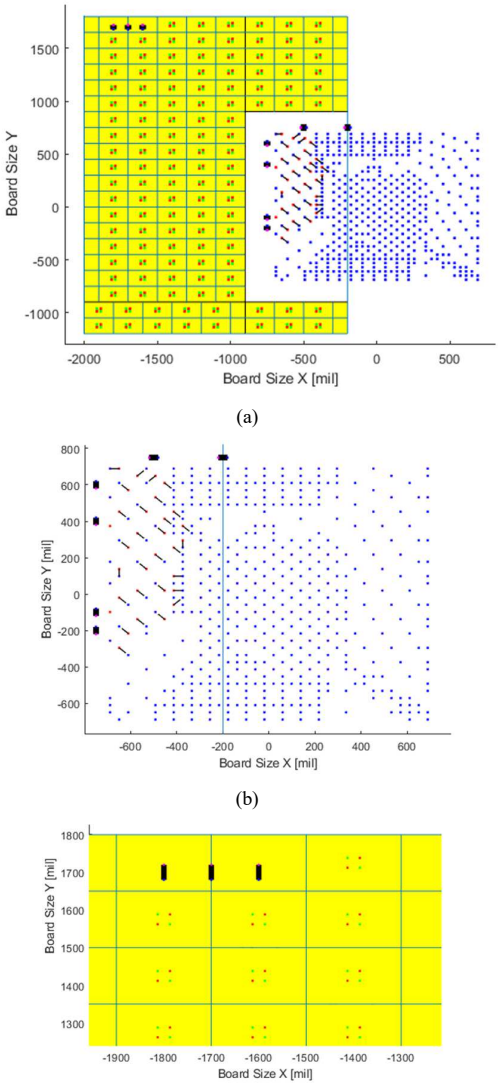


Fig. 6. (a) Overview of the PCB. The blue rectangle represents the power net area fill. The yellow regions are the around IC decap keep-in area. The region on the right side with blue and red dots are the IC pins, details are in (b). The green and red dots in the yellow region are the possible ground and power vias for around IC decaps. The small black squares are low-frequency decaps. (b) IC pin map. Blue and red dots are ground and power pins for the IC footprint. Dashed lines between blue and red dots are possible locations for decaps under the IC region. Black squares are the low-frequency decaps near the IC region. (c) The low-frequency decaps on the left top corner of the power net area fill in black squares, as well as the example for around IC decap possible locations.

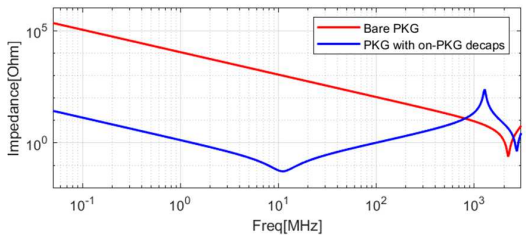


Fig. 7. PKG impedance without and with on-PKG capacitors

E. Decap Library

The decaps used for PDN impedance optimization are selected from the library listed in TABLE I. The ESL, ESR, and capacitance values are detailed. The package size of the decaps is 0402 based on the IC pitch size and the around IC decap keep-in area setting. The ESL value provided by the manufacturer is measured in a specific setup and is frequency dependent. Considering the frequency at which the high-frequency capacitors take effect (typically from several megahertz to hundreds of megahertz, for the examples in this paper, narrower frequency bandwidth to be optimized from several megahertz to tens of megahertz as shown in Fig. 8, in which situation the ESLs are close), and also the same package size in the decap library, the ESL of the capacitors in the decap library is 0.4 nH. Even though the ESL values for all the decaps are the same, in decap selection process, the actual loop inductance L_{above} with more mounting details from the ground to the capacitor is included in the decap selection process as stated in Section II. B.

IV. PDN Optimization Results

Four cases are studied for the system-level PDN optimization: 1) the bare PCB with only the low-frequency decaps, 2) the PCB with low-frequency decaps and PKG (without on-PKG capacitors), 3) the PCB with low-frequency decaps and PKG (with on-PKG capacitors), and 4) the PCB with low-frequency decaps and PKG (with on-PKG capacitors) and chip. The first three cases do not arise in the actual electronic system because the system provides functions to support the chip. But in this paper, the different cases are used to give examples of how the poles and zeros algorithm will work at different levels of PDN design for illustrative purposes. The bare PCB impedance with the low-frequency decaps is shown in Fig. 8(a) in light green. When cascading the PKG model without the on-PKG capacitors, the system PDN impedance is shown in Fig. 8(b) in light green. With on-PKG capacitors, the system PDN impedance is changed as the light green curve in Fig. 8(c). The complete PDN system with PCB, PKG (with on-PKG capacitors), and the chip has an impedance as shown in Fig. 8(d) in light green before the optimization.

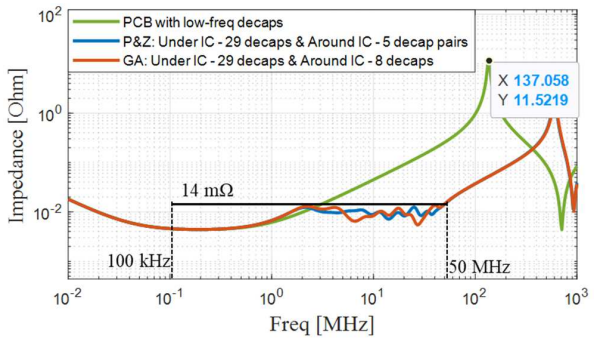
For the first case, if the system only contains the PCB PDN, with the low-frequency decaps already added, the PDN impedance optimization results using the poles and zeros algorithm are shown in Fig. 8(a). To lower the PDN impedance within the frequency range from 100 kHz to 50 MHz and below the target impedance of 14 mΩ, twenty-nine decaps are selected in the algorithm to be placed under the IC, and five pairs of decaps in a doublet pattern around the IC region. The decap selection result using the genetic algorithm is used as a validation. In the GA algorithm, twenty-nine decaps under IC and eight decaps in a single decap pattern around the IC region are selected. The two optimized impedance curves are both below the target impedance. However, the discrepancy between the two curves shows the different selection of decap types.

TABLE I. Decap Library for Under (U-) and Around (A-) IC

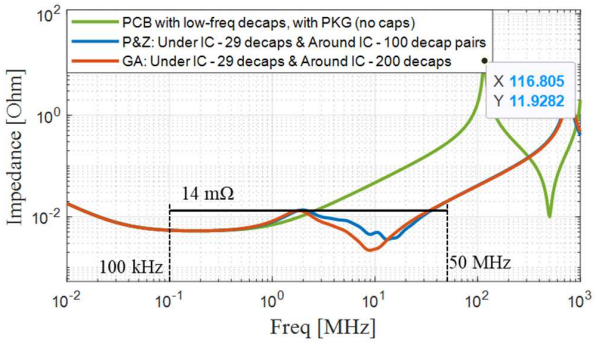
Decap Name	ESL	ESR	C
U16 – A1	0.4 nH	60 mΩ	10 nF
U17 – A2	0.4 nH	43 mΩ	22 nF
U18 – A3	0.4 nH	38 mΩ	47 nF
U19 – A4	0.4 nH	28 mΩ	100 nF
U20 – A5	0.4 nH	20 mΩ	220 nF
U21 – A6	0.4 nH	16 mΩ	470 nF
U22 – A7	0.4 nH	12 mΩ	1 μF
U23 – A8	0.4 nH	9 mΩ	2.2 μF
U24 – A9	0.4 nH	7 mΩ	4.7 μF

The details of the number of decap types and the order to select the decap using the poles and zeros algorithm (P&Z) and genetic algorithm (GA) are shown in TABLE II and TABLE III for the PCB-only case as an example. The two algorithms give similar decap number solutions. For the poles and zeros algorithm, the optimization is from low frequency to high frequency, thus decaps with larger capacitance will be selected first, and then decaps with small capacitance will be selected for the high-frequency optimization. However, the order of decap selection does not strictly follow the rule of from large decaps to small decaps because the selected decap in one round whose resonance frequency *f2* may be higher or lower than the intersection frequency *f1* so it may cause an increase or decrease in the total PDN inductance. This is the reason why the order of decap selection will change back and forth between two adjacent decap types. As for the genetic algorithm, the optimization is global and the decap selection order is more random, as can be seen in TABLE III.

For the second case, when the package model is attached, some additional effects are introduced into the system. If only the package model itself is considered, the capacitance of the package will be in parallel with the PCB PDN capacitance and make the total capacitance larger, and the inductance of the package will increase the total inductance of the system. As a result, the main resonance at approximately a hundred megahertz will shift to a lower frequency, as shown in Fig. 8(a), (b), from 137.058 MHz to 116.805 MHz, which will make it harder to reduce the system PDN impedance within the target frequency range. Also, the introduced inductance cannot be optimized using the decaps in high frequency due to the maximum decap number limitation and the low target impedance. In this case, with all the available decaps, the design is not achievable using either the poles and zeros algorithm or the genetic algorithm. However, introducing a bare package does not always cause optimization to fail. It depends on the package inductance and also the target impedance level and the frequency range of interest.



(a)



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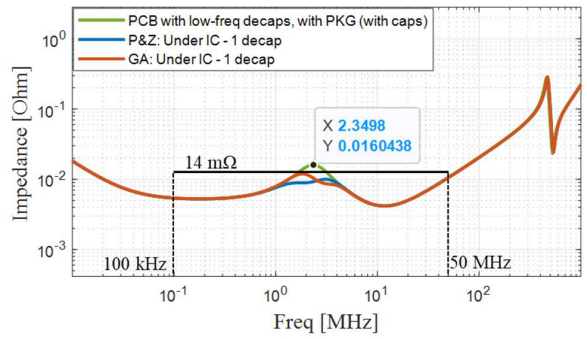
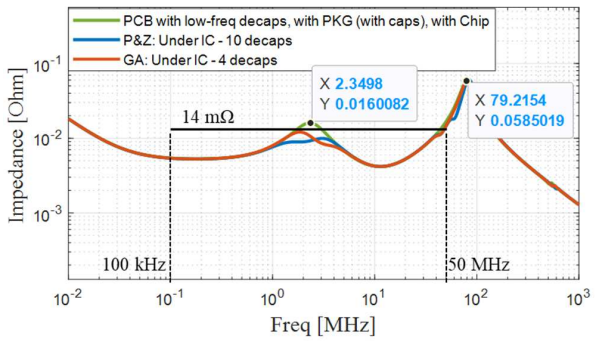


(c)



(d)

Fig. 8. Optimization results for the case (a) only the PCB with the low-frequency decaps (b) PCB with the low-frequency decaps, with the PKG (no on-PKG decaps) (c) PCB with the low-frequency decaps, with the PKG (with on-PKG decaps) (d) PCB with the low-frequency decaps, with the PKG (with on-PKG decaps), with Chip

TABLE II. # OF DECAPS UNDER IC AND (AROUND IC) OPTIMIZED FOR THE PCB ONLY CASE USING POLES& ZEROS ALGORITHM AND GENETIC ALGORITHM

Decap Name	P&Z	GA
U16 – A1 (10 nF)	7 (10)	2 (6)
U17 – A2 (22 nF)	8	16 (1)
U18 – A3 (47 nF)	5	3
U19 – A4 (100 nF)	4	3
U20 – A5 (220 nF)	2	1 (1)
U21 – A6 (470 nF)	1	3
U22 – A7 (1 µF)	1	0
U23 – A8 (2.2 µF)	1	1
Total	29 (10)	29 (8)

TABLE III. SELECTION ORDER OF DECAPS UNDER IC AND (AROUND IC) OPTIMIZED FOR THE PCB ONLY CASE USING POLES& ZEROS ALGORITHM AND GENETIC ALGORITHM

Decap Name	P&Z	GA
U16 – A1 (10 nF)	21-25,27,29 (30-39)	28-29 (31-36)
U17 – A2 (22 nF)	12,14,17-20,26,28	11-18,20-27 (30)
U18 – A3 (47 nF)	10-11,13,15-16	8-10
U19 – A4 (100 nF)	6-9	5-7
U20 – A5 (220 nF)	4-5	3 (37)
U21 – A6 (470 nF)	3	2,4,19
U22 – A7 (1 µF)	2	
U23 – A8 (2.2 µF)	1	1

For the third stage, the on-package capacitors can help reduce the system PDN impedance at mid-frequency. For the product example utilized in this paper, after adding the on-PKG capacitors, the package model has a resonance at around 10 MHz because of the large capacitance, thus before the optimization process, the system PDN impedance is reduced at the same frequency range, as the blue curve shown in Fig. 7 and the light green curve shown in Fig. 8(c). Only one low-Q pole at 2.35 MHz needs to be optimized then. The poles and zeros algorithm and the genetic algorithm both give the solution of using one decap. The poles and zeros algorithm results in a 4.7 µF decap under IC decap, while the genetic algorithm results in a 2.2 µF under IC decap.

Finally, for the fourth case, with the chip model included in the system, besides the pole formed by the total system inductance and the on-PKG capacitance in the last case, there is a pole resulting due to the on-chip capacitance at 79.22 MHz. The on-chip resistance will reduce the Q of the pole. The green curve in Fig. 8(d) shows the situation for the entire system with the PCB, package, and chip to be optimized. One decap will be used to reduce the first pole as in the third case. For the second pole, the impedance near the highest target frequency of 50 MHz increases due to the insufficient chip resistance. In this case, nine more decaps results using the poles and zeros algorithm, and three more decaps are required with the genetic algorithm to lower the impedance near the second pole. However, not all chip additions will cause difficulties in the PDN impedance optimization at higher frequencies. This mainly depends on the target impedance level, PDN inductance value, and chip inductance and resistance values.

The comparison of the time required for optimizing the above four cases using the poles and zeros algorithm and the genetic algorithm is listed in TABLE IV. The elapsed time data is collected on the same machine. For the first three cases, with the same or similar solution of total decap number, the

poles and zeros algorithm requires much less time than the genetic algorithm because of the straightforward decap selection methodology. For the fourth case, the GA results in a better decap solution at high frequency than the poles and zeros algorithm and has less running time. The optimization speed analysis above is for the cases specified in this paper. For different environments, the speed of the process may be different.

TABLE IV. TOTAL OPTIMIZATION TIME COMPARISON FOR THE FOUR TEST CASES

Case	P&Z	GA
PCB	119.81s	445.58s
PCB + PKG (no on-PKG caps)	336.09s	3971.64s
PCB + PKG (with on-PKG caps)	10.21s	25.26s
PCB + PKG (with on-PKG caps) + Chip	34.91s	19.93s

The optimization time comparison for the two algorithms given in TABLE IV. is for the situation when it achieves the target or reaches the maximum number of capacitors. For these cases, the decap number selections from the two methods are different so the speed advantage of the poles and zeros algorithm is not intuitively explained. In order to control all factors to be consistent and purely compare the speed of selecting the decaps for the two algorithms, the computing cost investigations were done based on a second case – PCB with PKG (no on-PKG caps) by changing the number of around IC decap port numbers. In this investigation, the number of decaps selected in the optimization process is identical with the number of decap ports. Therefore, the influence potentially caused by the different number of capacitors was excluded. The total time required for the two algorithms to select the decaps is given in TABLE V. The poles and zeros algorithm demonstrates an advantage in terms of time.

TABLE V. OPTIMIZATION TIME COMPARISON FOR DIFFERENT NUMBERS OF DECAP PORTS

Number of Decap Ports	P&Z	GA
Under IC 29 + Around IC 26	2.77 s	23.75 s
Under IC 29 + Around IC 46	6.13 s	48.66 s
Under IC 29 + Around IC 102	35.63 s	362.61 s
Under IC 29 + Around IC 148	90.65 s	1029.65 s
Under IC 29 + Around IC 244	353.76 s	4328.78 s

V. CONCLUSIONS

A simple, yet effective algorithm – poles and zeros algorithm, is presented herein for selecting the proper decoupling capacitors for the system-level PDN impedance optimization. A practical PDN system with PCB, package, and chip model is utilized as an example for testing the poles and zeros algorithm. The optimization results are validated by the genetic algorithm with a good and consistent agreement. The total number selected by the poles and zeros algorithm to lower the system PDN impedance is quite close to that from the genetic algorithm while with a higher speed.

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