

# Performance Quantization and Comparative Assessment of Voltage Equalizers in Mismatched Photovoltaic Differential Power Processing Systems

Xue Wang, *Student Member, IEEE*, Huiqing Wen, *Senior Member, IEEE*, Guanying Chu, *Member, IEEE*,  
Yinxiao Zhu, *Student Member, IEEE*, Yong Yang, *Senior Member, IEEE*,  
Yiwang Wang, and Lin Jiang, *Member, IEEE*

**Abstract**—Voltage equalizers (VEs) are essential for partially shaded photovoltaic (PV) modules by equalizing the voltage of PV modules and preventing anti-paralleled diodes from bypassing the shaded PV modules, resulting in improved power yield under partial shading conditions (PSCs). Recently, different topologies for VEs have been discussed based on the distributed maximum power point tracking (DMPPT) principle at the module level. Considering that the power flow distribution, operation modes, and actual performance of these VEs show distinct differences, it becomes increasingly important for the performance quantification and comparative assessment of various topologies both theoretically and experimentally. Here, three typical differential-power-processing based VEs are selected, including series-resonant-voltage-multiplier (SRVM), flyback-based PV-to-IP (Flyback-PV-IP), and flyback-based PV-to-Bus (Flyback-PV-Bus). Key performance indexes for VEs have been defined, including the processed power, power losses, and overall system efficiency. To quantify the performance of different topologies of VEs, an algorithm is developed in MATLAB with daily irradiation and temperature under various PSCs. Moreover, three experimental prototypes for the selected topologies have been built and main tests under different mismatching conditions have been conducted. With a systematic performance quantification and fair comparison of typical VEs, this article will propose a systematic evaluation method for VE schemes. Meanwhile, the optimal VE topology with its control for typical PSC cases will be identified.

**Index Terms**—Differential power processing (DPP), performance quantization, power loss analysis, voltage equalizer.

## NOMENCLATURE

SRVM	Series resonant voltage multiplier.
Flyback-PV-IP	Flyback-based PV-to-IP.
Flyback-PV-bus	Flyback-based PV-to-bus.

$V_{pri}$	Primary side voltage.
$V_{sec}$	Secondary side voltage.
$P_{rated}$	Rated Power.
$P_{o-SRVM}$	Required Power to compensate the string power.
$P_{mpp}$	Maximum available power.
$P_{i-SRVM}$	Required input power for the SRVM.
$\eta_{proc-SRVM}$	Conversion efficiency of the SRVM.
$P_{l-SRVM}$	Output power for load in SRVM.
$\eta_{SRVM}$	Overall efficiency in SRVM.
$P_{loss-SRVM}$	Total power loss in SRVM.
$i_{pv,x}$	PV module current at different situations.
$V_{pv,x}$	PV module voltage at peak power point.
$N_{sub}$	Number of the PV modules.
$I_{s-IP}$	String Current in Flyback-PV-IP converter.
$i_{dpp,x}$	Primary side current of flyback converters.
$V_{ref}$	Reference voltage at VE.
$P_{proc-IP}$	Processed power in Flyback-PV-IP converter.
$P_{eq-loss-IP}$	VE power loss in Flyback-PV-IP converter.
$P_{o-IP}$	Output power in the flyback converter.
$P_{loss-boost}$	Power loss in central boost converter.
$\eta_{boost}$	Conversion efficiency in boost converter.
$P_{t-IP}$	Total output power of Flyback-PV-IP.
$\eta_{IP}$	System Efficiency in Flyback-PV-IP.
$P_{loss-IP}$	Total power loss in Flyback-PV-IP.
$I_{s-bus}$	String current in Flyback-PV-bus.
$P_{proc-bus}$	Processed power in Flyback-PV-bus.
$P_{eq-loss-bus}$	VE power loss in Flyback-PV-bus.
$P_{o-bus}$	Output power in the flyback converter.
$P_{t-bus}$	Total output power of Flyback-PV-bus.
$\eta_{bus}$	System Efficiency in Flyback-PV-bus.
$P_{loss-bus}$	Total power loss in Flyback-PV-bus.
$E_V$	Error between the $V_{pv,x}$ and the equalization voltage.
$V_{stress}$	The maximum voltage stress on the switches at peak power point.

## I. INTRODUCTION

Currently, various renewable energy sources have been developed rapidly due to their environmental merits and government incentive policies [1]. Among them, photovoltaic (PV) energy has occupied the largest share due to its relative simple structure, easy control implementation, and rapidly declining cost [2]. However, the photovoltaic mismatches will significantly affect the actual power yield, damage PV elements and reduce lifetime due to environmental factors (e.g. partial shading and uneven irradiance) and non-environmental factors (e.g. non-uniform aging and manufacturing tolerant), respectively [3]. Fig. 1 illustrates the detailed internal construction and typical P-V and I-V characteristic curves of PV modules under partial shading conditions (PSCs), indicating possibly multiple peaks rather than one peak. Specifically, the internal

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Xue Wang, Huiqing Wen, and Guanying Chu are with the School of Advanced Technology, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China (e-mail: Xue.Wang19@student.xjtlu.edu.cn; Huiqing.Wen@xjtlu.edu.cn; Guanying.Chu02@xjtlu.edu.cn).

Yinxiao Zhu is with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: yinxiao.zhu@zju.edu.cn).

Yong Yang is with the School of Rail Transportation, Soochow University, Suzhou 215131, China (e-mail: yangy1981@suda.edu.cn).

Yiwang Wang is with the Suzhou Vocational University, Suzhou 215104, China (e-mail: wyiwang@163.com).

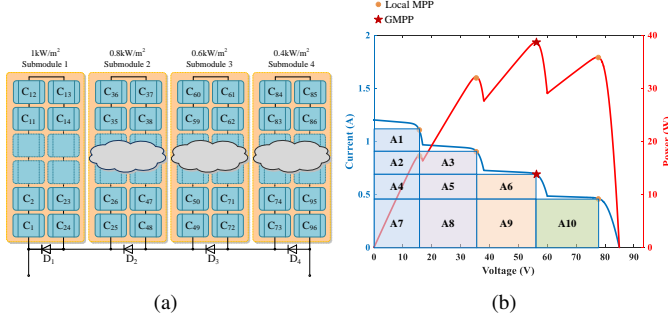


Fig. 1: P-V and I-V characteristic curves under partial shading conditions: (a) Internal connection structure of three series-connected PV modules. (b) P-V and I-V characteristic curves.

construction of a total-96-Cell PV module can be divided into four sub-modules as shown in Fig. 1(a). Each sub-module has 24 cells and one anti-parallel diode. When sub-module 2, 3, and 4 are experiencing PSCs, their anti-parallel diodes will be activated so that the output power from these three sub-modules is affected. Considering that the module output current is determined by the weakest sub-module current, the P-V characteristic curve of the PV module under the defined PSC will exhibit four peaks, as shown in Fig. 1(b) [4].

To deal with this issue, globe maximum power point tracking (GMPPT) techniques have been proposed to replace conventional maximum power point tracking (MPPT) techniques. Numerous GMPPT schemes have been made to improve tracking accuracy and dynamic performance.

In [5], a current-sensor-based GMPPT was proposed to improve the tracking speed during PSCs through the reduction in the tracking range of duty cycle. In [6], a novel modified rat swarm optimizer method (MRSO) with a dedicated detection for the occupance of PSCs was approached, indicating ultra-fast tracking speed. Besides, an adaptive PSO algorithm was proposed for PV systems with cuk converter as the power interface [7]. Although these GMPPT algorithms are effective in determining the global maximum power point (GMPP), there are still a certain amount of power yield losses in mismatched PV power systems. As shown in Fig. 1(b), although the GMPP could be correctly determined, the power yield losses shown as the area A1, A2, A3 and A10 are still observed, which demands further design optimization considering the large-scale application of PV systems.

To further eliminate power yield losses, distributed maximum power point tracking (DMPPT) techniques have been proposed, which can be classified into two categories: full-power-processing (FPP) based voltage equalizers (VEs) [8], [9], [25], [26] and differential power processors (DPP) based VEs, such as PV-IP [10], [11], PV-Bus [19]–[21], [27] and PV-PV [13], [14], [28], [29]. The basic concept of VEs is to equalize the voltage of PV modules and to prevent anti-parallel diodes from bypassing the shaded PV modules. Regarding FPP schemes, a single-switch-flyback converter working as the PV module power interface was proposed in [8] with a bus controller to achieve real-time DMPPT. In [9], a multiple buck-boost converter was used and the

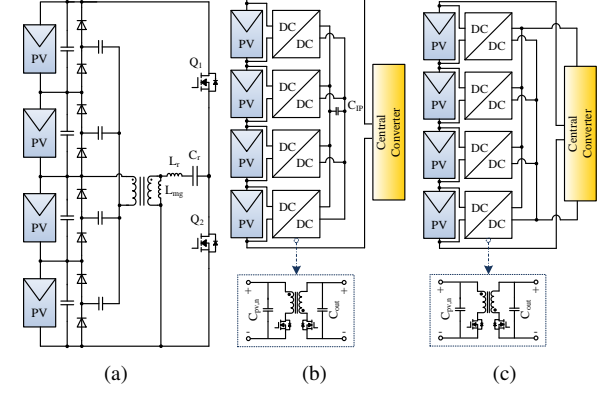


Fig. 2: Different topologies of DPP: (a) SRVM converter, (b) Flyback-PV-IP architecture, (c) Flyback-PV-Bus architecture.

multidimensional P&O(MPO) algorithm was adopted for the centralized control. For FPP architectures, each PV element, module, or sub-module level, will be equipped with one dedicated power converter, enabling true-MPPT operation of each element to tackle the issue of PSC. However, all output power from PV elements has to pass through FPP converters, affecting the power conversion efficiency of the whole PV system.

Compared with FPP, DPP-based VEs show the advantage of lower processing power and higher efficiency. Among three DPP architectures, PV-PV features the mismatch compensation among neighbor modules and one less DPP converters compared with the other two DPP architectures. In [12], a ladder configuration was used for DPP converters and a feedback loop was designed to calculate the average MPP current. Other topologies such as Switched inductor (SL) and switched capacitor (SC) have been discussed for PV-PV VEs [13], [14], [17], where the SL achieves true MPPT while SC achieves VE. Additionally, buck-boost converters are also utilized to build PV-PV schemes, where VE is achieved by voltage balance control in [15] whereas true MPPT is achieved by PI control in [16]. In [15],  $n - 1$  buck-boost converters are required for a series connection of  $n$  cells, to reach low consumption and high efficiency. A synchronous MPPT (SMPPT) is developed in a multi-input multi-output (MIMO) DPP system, which achieves simple scheme and high efficiency by separation of the easily decoupled dominant part of the system coupling [18]. A SC-based DPP architecture was proposed in [29] with the aim of reducing the voltage stress on capacitors. Moreover, diffusion capacitance of PV cells can be further utilized to construct the SC topology for mobile and vehicular applications, which can simplify the circuit meanwhile reducing the size [3], [30]. To summarize the advantages of the PV-PV, it can achieve small size, high power density, and long-string application.

In PV-IP architecture, bidirectional flyback topology was widely used to realize VE [10], [11]. In [10], flyback converters are controlled by perturbation & observation method to balance voltages under mismatching conditions. In [11], a module-level current sensor works for MPP tracking by downstream power electronics. Each submodule-integrated flyback converter is controlled independently from the others.

TABLE I: Comparison of Different DMPPT Schemes

System Structure	Converter Topology	System Control	Independent MPPT	Switch Number	Size ( $mm^2$ )	True MPPT or VE	Isolation	Maximum Voltage Stress on Switches (V)	PV Level	Rated Power (W)
FPP	Single-Switch Flyback [8]	Coordinated DMPPT	No	n	-	True MPPT	Yes	18	Module	270
FPP	Multiple Buck-Boost [9]	Multidimensional P&O(MPO)	No	n	$36 \times 30$	True MPPT	No	11.85	Module	200
PV-IP	Bidirectional Flyback [10]	P&O	No	2n	-	VE	Yes	17	Submodule	240
PV-IP	Bidirectional Flyback [11]	IP Voltage Balance	No	2n	-	VE	Yes	12, 36	Submodule	60
PV-PV	Ladder Configurations [12]	Current Sensorless Control	No	2(n-1)	-	True MPP	No	20	Module	430
PV-PV	Switched Inductor [13]	Image-Based Control	No	n+1	-	True MPPT	No	12.95	Submodule	100
PV-PV	Switched Capacitor [14]	String Current P&O	No	2(n-1)	-	True MPPT	No	13.4	Submodule	60
PV-PV	Buck-boost [15]	Voltage Balance	No	n-1	$70 \times 30$	VE	No	3	Cell	13.3
PV-PV	Buck-boost [16]	PI Control	Yes	2n	-	True MPPT	No	12	Module	300
PV-PV	Switched Capacitor [17]	Voltage Balance	No	2n	-	VE	No	31.5	Module	1052
PV-PV	MIMO [18]	SMPTT	Yes	2(n-1)	-	True MPPT	No	16.9	Submodule	300
PV-Bus	Bidirectional Flyback [4]	TMPP	Yes	2n	-	True MPPT	Yes	17	Submodule	80
PV-Bus	Bidirectional Flyback [19]	Unit-Minimum LPPT	Yes	2n	-	VE	Yes	40	Submodule	400
PV-Bus	Bidirectional Flyback [20]	PBP-LPPT	Yes	2n	-	VE	Yes	17	Submodule	80
PV-Bus	Bidirectional Flyback [21]	String-Current PI Control	Yes	2n	-	True MPPT	Yes	51.2	Submodule	330
PV-Bus	Bidirectional Flyback [22]	Voltage Balance	No	n	-	VE	Yes	8	Module	240
PV-Bus	LLC-Based VM [23]	Open-Loop Control	No	2	$90 \times 70$	VE	Yes	80	Module	200
PV-Bus	SRVM-based BSRC [24]	Open-Loop Control	No	n	$121 \times 94$	VE	Yes	120	Module	1000

Bidirectional flyback converters are also widely utilized in PV-bus DPP converter with various control algorithms, such as total-minimum power point (TMPP) [4], unit-minimum LPPT [19], power-balancing-point based TMPP (PBP-TMPP) [20], string-current PI control [21], and voltage balance [22]. Regarding the system control, with the same bidirectional flyback topology adopted in [4], [19], [19]–[21], two different system control strategies were utilized in previous researches. Other system controls include the sting-level power rating balance (PRB) for the modular design [31]. It is worth noting that the bidirectional flyback converter is simplified in [22], where integrated planar transformer is designed without any secondary-side circuits. Additionally, the integrated transformer with the active clamp structure shows zero-offset magnetizing current and achieves low RCD snubber losses. Other topologies such as Series Resonant Voltage Multiplier (SRVM) was reported in [23], [24], [32]–[35], utilizing LLC resonant converter and voltage multiplier. Specifically, an LLC inverter operates to drive the module-level or sub-module-level voltage multiplier, which can provide power to the shaded modules and realize the voltage balance. The SRVM achieves advantages in small size, favorable expandability, and fewer switches, whereas the parameters must be exactly estimated since circuits are highly coupled.

Regarding the PV-element control, there are two possible schemes, namely the true MPPT and voltage equalization (VE). A true MPPT method was used in [14], [36] by using a distributed P&O algorithm. VE, also known as the voltage balancing in [37], is capable of reaching equalized voltage of each module at a point close to its MPP rather than a true MPP. The differences among these recently proposed DPP-based VEs lie not only in the topology, but also in the control strategies, including both the system control and PV-element control, which will affect the power flow distribution, operation modes, and actual performance of VEs. TABLE I summarizes main features of these VE strategies proposed in recent years.

Considering the intensive researches for DPP-based VEs, it becomes increasingly important for the performance quantification and comparative assessment of various topolo-

gies both theoretically and experimentally. According the key features shown in TABLE I, three typical DPP-based VEs are selected, including series-resonant-voltage-multiplier (SRVM) [23], flyback-based PV-to-IP (Flyback-PV-IP) [10], and flyback-based PV-to-Bus (Flyback-PV-Bus) [4], [20]. Fig. 2 shows the circuit structure of these selected VEs. The performance quantization is assessed in terms of the processed power in each converter, total output power, and efficiency under both slightly and severely partial shading conditions in one whole day. Three prototypes for these topologies were designed and main experimental tests were conducted for a fair performance comparison under both short-term and long-term real-day irradiance and temperature conditions.

Compared with a preliminary theoretical comparison of several VE schemes in [38], this article presents a deeper analysis and more comprehensive comparison of typical VEs under various PSC conditions. Key performance indexes for VEs have been systematically defined, include the processed power, power losses, and overall system efficiency. More importantly, three experimental prototypes for the selected VE schemes have been built and main tests under different mismatching conditions have been conducted. Thus, both simulation and experimental results have been provided and analyzed to give a systematic performance quantification and fair comparison of these VEs. Main contributions of this paper can be summarized as follows:

- 1) **A systematic evaluation method for VE schemes:** In this article, key performance indexes for VEs have been systematically defined. Mathematical models of typical VEs have been built by considering the power distribution and the related control for power interfaces. Then, an algorithm is developed in MATLAB with daily irradiation and temperature under various PSCs to quantify performance of different topologies of VEs.
- 2) **Determination of the optimal VE scheme under typical PSC operating conditions:** In this article, a comprehensive comparison of nearly twenty recently-proposed VE schemes has been conducted. Besides, three experimental prototypes for the selected topologies have been built and main tests under different mismatching conditions

have been conducted. With a systematic performance quantification and fair comparison of typical VEs, the optimal VE topology with a proper control strategy for typical PSC operating conditions will be identified, which is extremely important for specific industrial applications.

This paper is divided into seven sections. In the Section II, control algorithm of each VE is introduced. The theoretical includes mathematical models in Section III, and power flow and power loss in IV, respectively. The performance quantization and comparative assessment is displayed in Section V and experiment results are displayed in Section VI. The Section VII summarizes the results and advantages of the proposed DPP.

## II. CIRCUIT AND CONTROL OF THREE VES

### A. SRVM

For the SRVM scheme, there are totally two switches working with fixed duty cycle and switching frequency. The main function of the LLC inverter is to generate proper ac square voltage to drive the voltage multiplier at the secondary side of the transformer, while the voltage multiplier keeps the voltage balance of the PV string. Therefore, the SRVM scheme can achieve the simplest control complexity among three VEs.

The module voltage of the  $PV_x$  can be expressed as [23]:

$$v_x = \frac{2}{\pi}(V_{PV,x} + 2V_D) \sin \omega_r t \quad (1)$$

where  $V_D$  is the forward voltage of the diodes. Hence, the amplitudes of the capacitor current  $I_{m-C_i}$  is displayed as:

$$I_{m-C_i} = \frac{2}{\pi} \frac{V_{TS} - (V_{PV,x} + 2V_D)}{\sqrt{r_i^2 + (\frac{1}{\omega_r C_i})^2}} \quad (2)$$

where  $r_i$  represents the equivalent series resistance of  $C_i$ . The peak amplitude of the current through the magnetic inductor of the transformer is  $I_{m-Lmg}$  shown as:

$$I_{m-Lmg} = \frac{N(\frac{1}{2}V_{PV,i} + V_D)DT_S}{2L_{mg}} \quad (3)$$

where  $D$  is the duty cycle of each switch. Besides, the peak amplitude of the current through the leakage inductor of the transformer is  $I_{m-Lr}$  as

$$I_{m-Lr} \approx \frac{2}{\pi} \frac{V_{string} - NV_{TS}}{R_r} \quad (4)$$

Therefore, the average input current of the LLC resonant inverter can be calculated as:

$$I_{in-ave} = \frac{1}{T_S} \int_0^{0.5T_S} I_{m-Lr} \sin \omega t dt = \frac{I_{m-Lr}}{\pi} \quad (5)$$

Based on the analyses the LLC resonant inverter can be simplified to an equivalent dc circuit with an input resistance, i.e.  $R_{in}$ , which can be shown as:

$$V_{string} - NV_{TS} = I_{in-ave} R_{in} \quad (6)$$

### B. Flyback-PV-IP and Flyback-PV-bus

For the Flyback-PV-IP scheme, the essential item is to keep the primary-side voltage and secondary-side voltage equal for DPP converters. The primary-side voltage  $V_{pri}$ , the secondary-side voltage  $V_{sec}$ , and the duty cycle  $D$  in the DPP converter with the selected topology of flyback have the following relation:

$$V_{sec} = V_{pri} \frac{D}{1-D} \quad (7)$$

For the Flyback-PV-Bus scheme, the LPPT is utilized to track the total minimum processing power through the DPP converters, while the boost converter is regulated to control the MPP current of PV sub-modules. Additionally, a time-sharing MPPT algorithm with enabled clock signals is utilized to control DPP converters, which can reduce the number of the MPPT controller units. Through the time-sharing MPPT algorithm, the reference voltage and the duty cycle are the output signals for each flyback converter. The execution sequence of MPPT units is regulated by an enabled clock signal. Specifically, the enabled clock signal will be set as '1', '0', and '-1' for three PV modules 1, 2, and 3. Considering that both schemes use a flyback converter topology, their circuit operation analysis is the same.

The average circuit model of the DCM flyback converter is shown as [39]:

$$\begin{aligned} i_{dpp,x} &= \frac{T_s}{2L} v_{sub,x} d_{pri,x}^2 \\ i_{sec,x} &= -\frac{T_s}{2L} v_{sec} d_{sec,x}^2 \end{aligned} \quad (8)$$

where  $T_s$ ,  $L$ ,  $i_{dpp,x}$ , and  $i_{sec,x}$  represent the PWM switching period, magnetic inductance of the transformer, the primary side current, and the secondary side current, respectively.

The secondary side current can be expressed by a function of the primary side current as:

$$i_{sec,x} = \frac{v_{sub,x}}{v_{sec}} i_{dpp,x} \quad (9)$$

The primary side current can be expressed as a function of the unified duty cycle:

$$\begin{aligned} i_{dpp,x} &= \frac{T_s}{2L} v_{sub,x} g_x(d_x) d_x^2; \\ g_x(u) &= \begin{cases} 1 & u \geq 0 \\ -(\frac{v_{sec}}{v_{sub,x}})^2 & u < 0 \end{cases} \end{aligned} \quad (10)$$

The duty cycle is given by the voltage difference in the time-domain as:

$$d_x(t) = K_p H(t) * A(t) * (v_{sub,x}(t) - v_{sec}(t)) \quad (11)$$

where  $K_p H(t)$  and  $A(t)$  represent the impulse responses of the compensator and the low-pass.

The voltage derivatives are given by the primary side and secondary side capacitors, i.e.,  $c_{pri}$  and  $c_{sec}$ , respectively.

$$\frac{d}{dt} v_{sub,x} = \frac{1}{c_{pri}} (I_{pv,x}(v_{sub,i}) - i_{dpp,x} - i_{s-IP}) \quad (12)$$

$$\frac{d}{dt} v_{sec} = \frac{1}{NC_{sec}} \sum_x i_{sec,x} \quad (13)$$



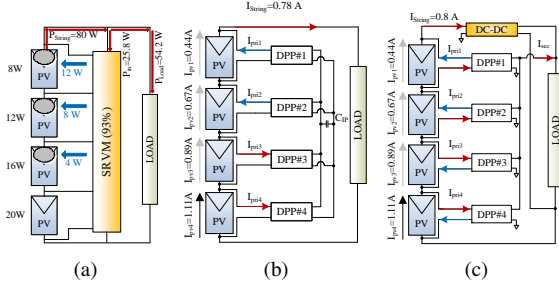


Fig. 3: Power flow and current flow of dc-dc converter. (a) SRVM. (b) Flyback-PV-IP. (c) Flyback-PV-Bus.

When the system operates at the steady-state point, the time derivatives is set to zero. The non-linear algebraic equations can be expressed as:

$$I_{PV,x}(V_{sub,x}) - I_{dpp,x} = \frac{1}{R_{MPP}} \sum_x V_{sub,x} \quad (14)$$

$$I_{dpp,x} = \frac{T_s}{2L} v_{sub,x} g_x(d_x) \quad (15)$$

$$\sum_x V_{sub,x} I_{dpp,x} = 0 \quad (16)$$

### III. THEORETICAL ANALYSIS OF PERFORMANCE INDEXES FOR THREE VES

In this section, several key performance indexes for VEs have been defined, include the processed power, total power losses, power loss distribution, cost, and reliability. Based on the power flow analysis, theoretical analysis of these defined performance indexes for three VEs will be presented.

#### A. Power Flow Analysis

The selected topologies of three VEs are shown in Fig. 2. The SRVM structure contains an LLC resonant inverter and a voltage multiplier (VM), where LLC inverter will generate the ac wave while VM aims to generate equal voltages at the outputs of DPP converters. With the SRVM, the current would flow to the heavily shaded PV module whose output voltage is lower than other modules. The Flyback-PV-IP structure employs flyback topology for DPP converters considering that Flyback provides galvanic isolation and bidirectional current flow ability. Different from the Flyback-PV-IP structure, the Flyback-PV-Bus structure will employ a boost central converter so that the string current can be regulated to follow the optimal value with respect to the minimum power losses through DPP converter in a real-time mode.

A case study of 4-PV-string under severe partial shading conditions is conducted here, where four PV modules, PV<sub>1</sub>-PV<sub>4</sub>, will generate the output power of 8 W, 12 W, 16 W, and 20 W (rated), respectively. The corresponding power flow and current flow for three VEs are illustrated in Fig. 3, while the measured efficiencies of different dc-dc converters with respect to the proceeded power is illustrated in Fig. 4.

For the SRVM scheme, considering that all modules in the string are subjected to the same string current and the function of voltage equalization is successfully implemented, the output

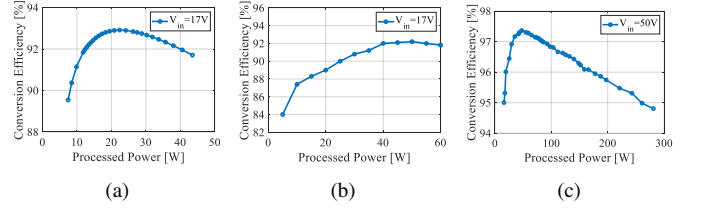


Fig. 4: Experimental conversion efficiencies for different dc-dc converters. (a) SRVM converter. (b) Flyback converter. (c) Boost converter.

voltage of all modules are regulated equal while shaded modules of PV<sub>1</sub>-PV<sub>3</sub> receive differential power, namely 12W, 8W, and 4W, respectively. Assume that the conversion efficiency of SRVM is 93%, the input power to the voltage equalization circuit is calculated as 25.8W. Then, the output power of the SRVM is calculated as 54.2W. The detailed power flow is demonstrated in Fig. 3(a).

Under the same partial shading condition, Fig. 3(b) illustrates the current flow through different dc-dc converters in the Flyback-PV-IP scheme when the string current  $I_{string}$  is regulated at 0.78 A. PV<sub>3</sub> and PV<sub>4</sub> provide the current to the isolated port. Specifically, the corresponding currents are calculated at 0.33 A and 0.11 A for  $I_{pri3}$  and  $I_{pri4}$ , respectively. The corresponding currents injected to the shaded PV<sub>1</sub> and PV<sub>2</sub> are calculated as 0.34 A and 0.11 A, respectively.

In the Flyback-PV-Bus structure, an optimal string current is obtained with the time-sharing MPPT algorithm to realize the least processing power in DPP converters. Specifically, the excessive currents will be extracted from PV<sub>3</sub> and PV<sub>4</sub>, while the shaded modules PV<sub>1</sub> and PV<sub>2</sub> will receive the injected current, as illustrated in Fig. 3(c).

#### B. Processed Power, Output Power, and Efficiency

Here, the dc-dc power conversion of three VEs are built. The analysis aims to explain the power and current processing through the DPP converters under PSCs. Furthermore, the output powers, efficiencies, and power losses can be calculated for comparison according to the analysis.

1) *SRVM*: For the SRVM, the processing power through the VE is analyzed here. Firstly, the rated power ( $P_{rated}$ ) of the PV string is the sum of each module, which is 80 W in this paper.

To compensate the string power under the partial shading condition, the required power,  $P_{o-SRVM}$ , can be expressed as:

$$P_{o-SRVM} = P_{rated} - P_{mpp} \quad (17)$$

where maximum available power is  $P_{mpp}$ .

The requested input power for the SRVM scheme is expressed by:

$$P_{i-SRVM} = \frac{P_{o-SRVM}}{\eta_{proc-SRVM}} \quad (18)$$

The output power for the load is calculated as:

$$P_{l-SRVM} = P_{rated} - P_{i-SRVM} \quad (19)$$

The total output energy can be obtained by the time integration of  $P_{l-SRVM}$ . Then, the overall system efficiency and total power loss expressions can be obtained respectively.

$$\eta_{SRVM} = \frac{P_{l-SRVM}}{P_{mpp}} \quad (20)$$

$$P_{loss-SRVM} = P_{mpp}(1 - \eta_{SRVM}) \quad (21)$$

2) *Flyback-PV-IP*: In principle, the Flyback-PV-IP scheme will only process the mismatched power through DPP converters. When the topology of flyback is adopted for DPP converters, the power provided by DPP converters in the Flyback-PV-IP scheme depends on the primary side current of DPP converters,  $i_{pv,x}$ . When all modules are regulated at the same voltage, the string current can be calculated as:

$$I_{s-IP} = \frac{\sum_{x=1}^{N_{sub}} i_{pv,x}}{N_{sub}} \quad (22)$$

The primary side current of each DPP converter,  $i_{dpp}$ , can be expressed by:

$$i_{dpp} = I_{s-IP} - i_{pv,x} \quad (23)$$

Considering that the proceeded power in this scheme would be regulated bidirectionally, the processed power,  $P_{proc-IP}$ , can be expressed as:

$$P_{proc-IP} = V_{ref} \sum_{x=1}^{N_{sub}} |i_{dpp}| \quad (24)$$

where  $V_{ref}$  is the reference voltage at VE.

The corresponding power yield loss due to the VE control can be expressed as:

$$P_{eq-loss-IP} = P_{mpp} - V_{ref} I_{s-IP} \quad (25)$$

Assume the flyback converter efficiency is  $\eta_x$ , the output power from flyback converters can be expressed as:

$$P_{o-IP} = \sum_{x=1}^N \eta_x V_{ref} |i_{dpp}| \quad (26)$$

Assume the boost converter efficiency is  $\eta_{boost}$ , the power losses in the central boost converter can be calculated as:

$$P_{loss-boost} = P_{o-IP}(1 - \eta_{boost}) \quad (27)$$

Then, the total output power,  $P_{t-IP}$ , can be calculated as:

$$P_{t-IP} = P_{mpp} - P_{proc-IP}(1 - \eta_x) - P_{eq-loss-IP} - P_{loss-boost} \quad (28)$$

The total output energy can be obtained by the time integration of  $P_{t-IP}$ . Then, the mathematical expressions for the system efficiency and the total power loss by using the Flyback-PV-IP scheme can be obtained respectively.

$$\eta_{IP} = \frac{P_{t-IP}}{P_{mpp}} \quad (29)$$

$$P_{loss-IP} = P_{mpp}(1 - \eta_{IP}) \quad (30)$$

3) *Flyback-PV-Bus*: In the Flyback-PV-Bus architecture, the string current may affect the processed power in DPP converters. According to the MPP currents in PV modules, there would be different operation modes with PV modules regulated at their MPPs. For any operation mode, the total power proceeded by DPP converters for four-module based Flyback-PV-Bus architecture can be expressed as:

$$P_{proc-bus} = V_{ref}(|I_{s-bus} - I_{pv1}| + |I_{s-bus} - I_{pv2}| + |I_{s-bus} - I_{pv3}| + |I_{s-bus} - I_{pv4}|) \quad (31)$$

Among different Flyback-PV-Bus architectures, the architecture in [4] shows advantages of high efficiency and easy

in implementation, where a centralized converter can directly control the string current,  $I_{string-bus}$ . The corresponding power yield loss due to VE can be expressed as:

$$P_{eq-loss-bus} = P_{mpp} - V_{ref} I_{s-bus} \quad (32)$$

The output power of flyback converter,  $P_{o-bus}$ , is expressed as:

$$P_{o-bus} = \sum_{x=1}^N \eta_x V_{ref} |I_{s-bus} - I_{pv,x}| \quad (33)$$

The power loss in the boost converter,  $P_{loss-boost}$ , can be expressed as:

$$P_{loss-boost} = P_{out-bus}(1 - \eta_{boost}) \quad (34)$$

Therefore, the total output power,  $P_{t-bus}$ , can be expressed as:

$$P_{t-bus} = P_{mpp} - P_{proc-bus}(1 - \eta_x) - P_{eq-loss-bus} - P_{loss-boost} \quad (35)$$

The total output energy can be obtained by the time integration of  $P_{total\_Flyback-PV-bus}$ . Then, the overall system efficiency and the total power loss in the Flyback-PV-Bus scheme can be obtained respectively.

$$\eta_{bus} = \frac{P_{t-bus}}{P_{mpp}} \quad (36)$$

$$P_{loss-bus} = P_{mpp}(1 - \eta_{bus}) \quad (37)$$

### C. Power Loss Distribution

Here, the power loss distributions of three VEs under various PSCs will be presented.

1) *SRVM*: The power losses through the SRVM,  $P_{loss-SRVM}$ , can be analyzed into two parts: the power losses in LLC resonant inverter  $P_{resonance}$  and the power loss in VM ( $P_{VM}$ ) [23]. The corresponding expression for  $P_{resonance}$  is given by:

$$P_{resonance} = \frac{\omega\pi}{2\omega_r N^2} R_r I_{m-VM}^2 \quad (38)$$

where,  $\omega_r$  and  $\omega$  represent the resonant angular frequency and the operation angular frequency, respectively.  $N$  is the turns ratio in the transformer.  $R_r$  is the equivalent resistance of the resonant tank, while  $I_{m-VM}$  is the peak current of the VM.

$P_{VM}$  can be further divided into the capacitor losses  $P_C$  and the diode conduction loss  $P_D$ . Their mathematical expressions are given by:

$$P_D = V_{D1} I_{m-Ci} \quad (39)$$

$$P_C = \frac{\omega\pi}{2\omega_r} R_{ci} I_{m-Ci}^2 + R_{cout} I_{m-Ci}^2 \left( \frac{2\omega\pi}{\omega_r} - 1 \right) \quad (40)$$

where  $V_{D1}$ ,  $R_{ci}$  and  $R_{cout}$  are the diode forward voltage and the capacitor equivalent resistance of  $C_{in}$  and  $C_{out}$ , respectively.  $I_{m-Ci}$  is the peak current through the capacitor in the VM.

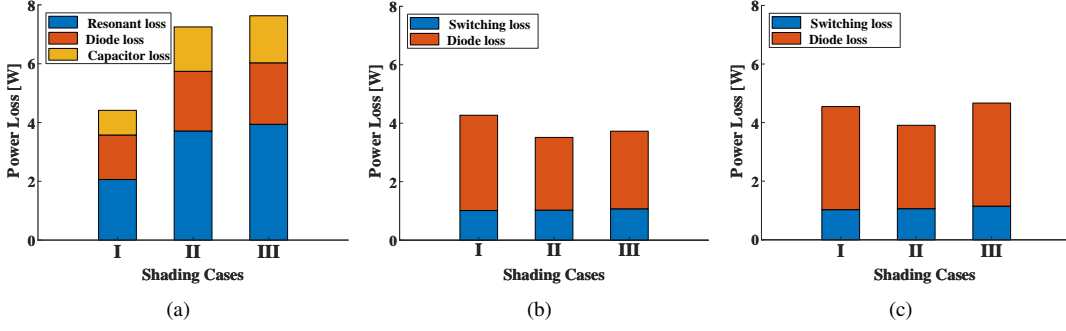


Fig. 5: Evaluated power loss distribution of there VEs under different PSCs: (a) SRVM. (b) Flyback-PV-IP. (c) Flyback-PV-Bus.

2) *Flyback-PV-IP*: In the Flyback-PV-IP architecture, the power losses through the flyback converter contain two parts, namely the power loss in MOSFET  $P_{SW}$  and the transformer iron losses  $P_{loss-MG}$ . For  $P_{SW}$ , the corresponding expression can be given by:

$$P_{SW} \cong R_{ds,on} i_{SW,RMS}^2 + t_{tr} V_{SW} i_{SW,peak} f_{SW} + (V_{GS}^2 C_{iss} + V_{SW}^2 C_{oss}) f_{SW} \quad (41)$$

where  $R_{ds,on}$ ,  $C_{iss}$ , and  $C_{oss}$  represent the static drain-to-source on resistance, input and output capacitance of MOSFET, respectively.  $i_{SW,RMS}$  and  $i_{SW,peak}$  represent the rms current and the peak current through the MOSFET, respectively.  $V_{SW}$  and  $V_{GS}$  are the voltage across the MOSFET and the gate driving voltage.  $f_{SW}$  is the switching frequency.

The corresponding expression for  $P_{loss-MG}$  is given by:

$$P_{loss-MG} = I_{avg-FBC}^2 R_{CD-FBC} \quad (42)$$

where  $I_{avg-FBC}$  and  $R_{CD-FBC}$  represent the average current through transformer and transformer DC resistance, respectively.

For the power loss distribution analysis in the central boost converter, three components are considered, including the switching loss, the diode conduction loss  $P_{loss-D1}$ , and the inductor DC loss  $P_{loss-L1}$ . The switching losses in the boost converter can be calculated according to (41). The corresponding expressions for the latter two components are given by:

$$P_{loss-D1} = V_{D1} I_{s-IP} \quad (43)$$

$$P_{loss-L1} = I_{ave-boost}^2 R_{CD-L1} \quad (44)$$

where  $V_{D1}$  refers to the diode forward voltage.  $I_{ave-boost}$  and  $R_{CD-L1}$  represent the inductor average current and the parasitic DC resistance, respectively.

3) *Flyback-PV-Bus*: In the Flyback-PV-Bus architecture, the power loss analysis is similar to the Flyback-PV-IP. The total power loss in the Flyback-PV-bus architecture can be divided into three parts: switching losses, diode losses, and the magnetic losses. Similar as that in the Flyback-PV-IP architecture, the magnetic loss is found much smaller compared with other two components.

The evaluated power loss distributions in three VEs are illustrated in Fig. 5, where three cases are selected to distinguish slightly shaded case, medium shaded case, and severely shaded case. Case I is defined with the irradianations for four PV modules set as 100%, 100%, 100%, and 80%; Case II is

defined with the irradianations for four PV modules set as 100%, 100%, 60%, and 40%; Case III is defined with the irradianations for four PV modules set as 100%, 60%, 50%, and 40%;

Fig. 5 shows the power loss distributions of three VEs under the defined PSCs. For SRVM, the power losses will increase with respect to the severity of PSCs. For the Flyback-PV-IP and Flyback-PV-Bus architecture, the diode conduction loss take the largest proportion while the switching loss is relative small with less variations. Considering that  $P_{mg}$  and  $P_{loss-L1}$  are extremely small, the two components will not be shown in Fig. 5 (b) and (c). Fig. 6 illustrates the detailed power loss distribution among different components in Flyback-PV-IP and Flyback-PV-Bus, indicating the central converter loss will account for the largest ratio for both architectures. The flyback power loss will increase with the severity of PSCs, while the trend for the central boost converter is different, which depends on the specific PSC. As the severity of PSC increases, the advantages of Flyback-PV-IP will become more apparent compared to Flyback-PV-Bus.

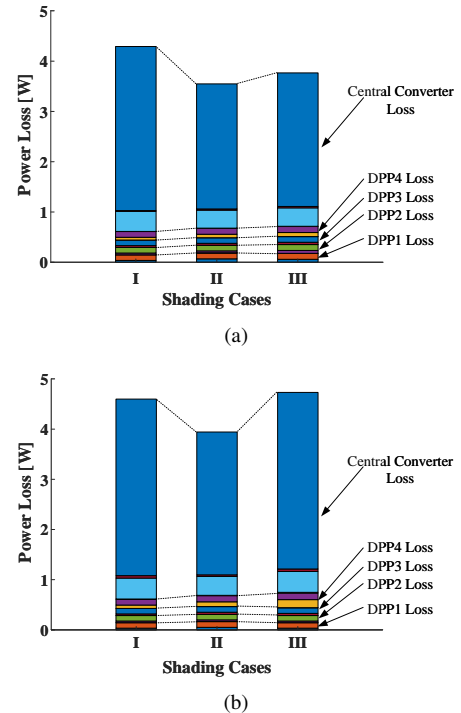


Fig. 6: Comparison of power loss distributions of two architectures under different PSCs: (a) Flyback-PV-IP, (b) Flyback-PV-Bus.

#### D. Reliability

Here, the component-level reliability analysis is conducted, where the component failure rate or hazard rate  $\lambda$  is utilized to assess the engineering reliability. The component-level reliability analysis will concentrate on the failure rate of the essential electronic components, including MOSFETs, capacitors, and magnetic devices according to empirical model in the military handbook for the reliability prediction of electronic equipment (MIL-HDBK-217). The system failure rate  $\lambda_{sys}$  of three VEs can be derived as follows:

$$\lambda_{sys} = \lambda_{sw} + \lambda_{TR} + \lambda_C + \lambda_D \quad (45)$$

where  $\lambda_{sw}$ ,  $\lambda_C$ , and  $\lambda_{TR}$  represent the failure rate of MOSFETs, capacitors, and transformers, respectively.

For  $N$ -channel MOSFETs,  $\lambda_{sw}$  is expressed as:

$$\lambda_{sw} = \lambda_{b,sw} \pi_T \pi_A \pi_Q \pi_E \quad (46)$$

where  $\lambda_{b,sw}$ ,  $\pi_T$ ,  $\pi_A$ ,  $\pi_Q$ , and  $\pi_E$  refer for the basic failure rate of MOSFETs, temperature factor, application factor, quality factor, and environmental factor, respectively. Normally,  $\lambda_{b,sw}$ ,  $\pi_A$ ,  $\pi_Q$ , and  $\pi_E$  remain constant at 0.012, 8, 8, and 1 according to MIL-HDBK-217.  $\pi_T$  can be expressed as:

$$\pi_T = \exp[-1925(\frac{1}{T_J + 273} - \frac{1}{298})] \quad (47)$$

where  $T_J$  is the junction temperature.

The failure rate of transformer,  $\lambda_{TR}$ , is expressed as:

$$\lambda_{TR} = \lambda_{b,TR} \pi_Q \pi_E \quad (48)$$

where  $\lambda_{b,TR}$  is the basic failure rate for transformers as 0.0028 under the temperature of 40°C.

The failure rate of the electrolytic capacitor,  $\lambda_C$ , is given by:

$$\lambda_C = \lambda_{b,C} \pi_{CV} \pi_Q \pi_E \quad (49)$$

where  $\pi_Q$  keeps constant at 1.  $\pi_{CV}$  is the capacitance factor and expressed by:

$$\pi_{CV} \approx 0.34C^{0.18} \quad (50)$$

where,  $\pi_{b,C}$  is given by:

$$\pi_{b,C} = 0.00254[(\frac{2V_{OP}}{V_{rated}})^3 + 1] \exp[5.09(\frac{T_A + 273}{358})^5] \quad (51)$$

The failure rate of the diodes,  $\lambda_D$ , can be expressed by:

$$\lambda_D = \lambda_{b,D} \pi_T \pi_S \pi_C \pi_Q \pi_E \quad (52)$$

where  $\lambda_{b,D}$  is a constant value equal to 0.069. The temperature factor, denoted as  $\lambda_T$ , is 1.6 at 40°C. The variables  $\pi_S$ ,  $\pi_C$ ,  $\pi_Q$ , and  $\pi_E$  represent electrical stress factor, contact construction factor, quality factor, environment factor, respectively. These variables are assumed to remain constant throughout the analysis according to MIL-HDBK-217.

Based on the analysis above, the failure rate of three VEs can be obtained according to different circuit configurations and power loss distributions. The calculated failure rates of three VEs under three shading cases are presented in Fig. 7.

It is worth noting that the failure rate of SRVM increases with the severity of PSC, while the trend of other two VEs is exactly opposite. Furthermore, the failure rate of SRVM is much lower compared to other VEs.

#### E. Cost

TABLE II shows the component models, quantities, and unit prices in US dollars. On this basis, the price distribution and total price charts for different VEs can be obtained, as shown in Fig. 8. With the increase of modules, the switching cost in the SRVM remains constant since only two switches are utilized in the SRVM. As shown in Fig. 8(a), the total cost increases slowly with the number of capacitors and diodes. In the Flyback-PV-IP and Flyback-PV-bus, the number of flyback converters rises accordingly with respect to the PV module number, which makes the total cost rise approximately linearly. Specifically, for a string with four modules, the cost of magnetic elements takes the largest account in these VEs, while the switches takes 14% in SRVM and 42% in other VEs. The diodes only take 2% in Flyback-PV-IP and Flyback-PV-bus, while it takes much larger in SRVM at 17%.

### IV. PERFORMANCE QUANTIZATION OF THREE VES UNDER REAL METEOROLOGICAL CONDITIONS

In this section, a comprehensive performance quantization and comparative assessment of three selected VEs under real meteorological conditions is conducted, including proceeded power, output power, system efficiency, and total power loss.

#### A. Performance Quantization Algorithm

To quantify performance of different VEs, an algorithm is developed in MATLAB with daily irradiation and temperature under various PSCs. Main algorithm structures for three VEs are listed below, where main performance indexes of DPP converters, including processed power, output power, and total power loss corresponding to different PSCs throughout the day can be calculated. For the algorithm implementation, the changing irradiation data represented by  $t_i$  will be iterated in the outer loop while all PV modules will be iterated in the inner loop for the calculation.

##### Algorithm 1 Calculation for SRVM

---

```

1: For  $t_i$ :  $t_0$  to  $t_f$ 
2: For  $x$ : 1 to  $N_{sub}$ 
3: Calculate  $P_{o-SRVM}$ , and  $P_{mpp}$ 
4: Extract  $\eta_{SRVM} = f(P_{proc-SRVM})$  from line tracking
5:  $P_{i-SRVM} = \frac{P_{o-SRVM}}{\eta_{proc-SRVM}}$ 
6:  $P_{l-SRVM} = P_{rated} - P_{i-SRVM}$ 
7:  $\eta_{SRVM} = \frac{P_{l-SRVM}}{P_{mpp}}$ 
8:  $P_{loss-SRVM} = P_{mpp}(1 - \eta_{SRVM})$ 
9: Calculate the produced energy
10: End
11: End

```

---

#### B. Simulation Evaluation on Various PSCs

Based on the above analysis, the performance quantization algorithm is implemented in MATLAB for quantization and comparative assessment of three voltage equalization architectures. A string with 4 modules is utilized in the simulation, where the rated power of each module is 20 W. The real-day irradiance is shown in Fig. 9, which was collected in the University of Nevada, United States. When there are no

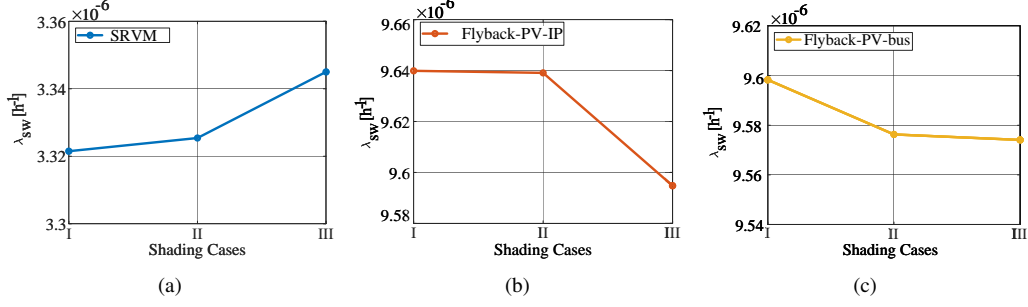


Fig. 7: Evaluated failure rates for different VEs.(a) SRVM. (b) Flyback-PV-IP. (c) Flyback-PV-Bus.

TABLE II: Key parameters for the system cost comparison in various VE schemes

Flyback-PV-IP and Flyback-PV-bus				SRVM			
Parameter	Model and Value	Qty	Unit Price <sup>1</sup>	Parameter	Model and Value	Qty	Unit Price <sup>1</sup>
PV module	-	4	-	PV module	-	4	-
Flyback converter switch	IRFP460	8	2.51	Switch	FDS86240	2	1.46
Boost converter switch	IRFP250N	1	1.12	Resonant capacitance	62 nF 400 V	1	1.31
Transformer framework <sup>2</sup>	EE28	4	6.22	Transformer framework <sup>2</sup>	EI40	1	3.11
Primary capacitance	220 $\mu$ F 50 V	4	0.34	Input capacitance	94 $\mu$ F 50V	4	0.84
Secondary capacitance	47 $\mu$ F 250 V	4	0.47	Output capacitance	94 $\mu$ F 50V	8	0.84
Boost converter capacitance	47 $\mu$ F 250 V	1	0.47	VM diodes	SB1045	8	0.46
Diode	FR107	8	0.21	-	-	-	-

The component unit price is in US \$ and originated from <https://www.digikey.cn>.

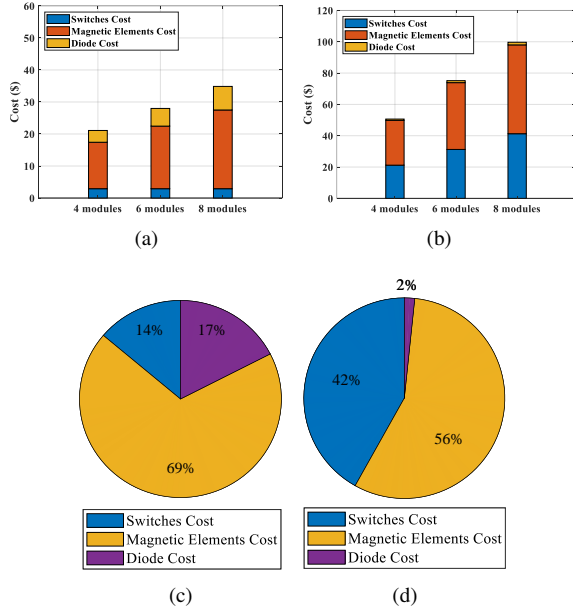


Fig. 8: System cost comparison. (a) Total cost of SRVM with respect to module numbers. (b) Total cost of Flyback-PV-IP and Flyback-PV-bus with respect to module numbers. (c) Cost distribution of SRVM. (d) Cost distribution in Flyback-PV-IP and Flyback-PV-bus.

mismatching, the condition is defined as 100%.  $I_r$  represents the real-day irradiance in the University of Nevada. Under the slight PSC, there are no mismatching for three modules except PV4, while the irradiation for PV4 is 100% of  $I_r$ . Under the medium PSC, there are no mismatching for PV1 and PV2, while the irradiation values for PV3 and PV4 are set as 100% of the rated irradiation and 80% of  $I_r$ , respectively. Under the severe PSC, only one PV module, PV1, is with 100% of the rated irradiation, the irradiation values for

#### Algorithm 2 Calculation for Flyback-PV-IP

- 1: For  $t_i: t_0$  to  $t_f$
- 2: For  $x: 1$  to  $N_{sub}$
- 3: Calculate  $P_{mpp}$ ,  $I_{s-IP}$ , and  $i_{dpp}$
- 4:  $P_{proc-IP} = V_{ref} \sum_{x=1}^{N_{sub}} |i_{dpp}|$
- 5: Extract  $\eta_x = f(P_{proc-IP})$  from line tracking
- 6: Extract  $\eta_{boost} = f(P_{proc-boost})$  from line tracking
- 7: Calculate the output power of the FBCs, power losses in central converter and VE loss.
- 8: Obtain the output power  $P_{t-IP}$ .
- 9:  $\eta_{IP} = \frac{P_{t-IP}}{P_{mpp}}$
- 10:  $P_{loss-IP} = P_{mpp}(1 - \eta_{IP})$
- 11: Calculate the produced energy
- 12: End
- 13: End

#### Algorithm 3 Calculation for Flyback-PV-Bus

- 1: For  $t_i: t_0$  to  $t_f$
- 2: For  $x: 1$  to  $N_{sub}$
- 3: Calculate  $P_{mpp}$ ,  $I_{s-Bus}$ , and  $i_{dpp}$
- 4:  $P_{proc-bus} = V_{ref} \sum_{x=1}^N |i_{dpp}|$
- 5: Extract  $\eta_x = f(P_{proc-bus})$  from line tracking
- 6: Extract  $\eta_{x-boost} = f(P_{proc-boost})$  from line tracking
- 7: Calculate total power losses in FBCs, power losses in central converter and VE loss.
- 8: Calculate the total output power  $P_{t-bus}$
- 9:  $\eta_{bus} = \frac{P_{t-bus}}{P_{mpp}}$
- 10:  $P_{loss-bus} = P_{mpp}(1 - \eta_{bus})$
- 11: Calculate the produced energy
- 12: End
- 13: End

PV2, PV3, and PV4 are set as 60% of the rated irradiation, 40% of the rated irradiation, and 40% of  $I_r$ , respectively. TABLE III displays the comparison about maximum output power ( $P_{max}$ ), maximum efficiency ( $\eta_{max}$ ), and produced energy (E) during the day in the simulation. The details of the evaluation setup are shown below.



- 1) PV1: 100%, PV2: 100%, PV3: 100%, PV4:  $I_r$ ;
- 2) PV1: 100%, PV2: 100%, PV3: 80%, PV4:  $0.8 \times I_r$ ;
- 3) PV1: 100%, PV2: 60%, PV3: 40%, PV4:  $0.4 \times I_r$ .

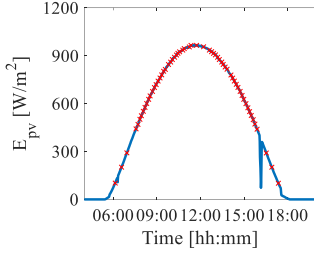


Fig. 9: Meteorological data profile in University of Nevada, US, on April 2, 2015.

TABLE III: Comparison of Different DPP Architectures

Cases		$P_{max}$ (W)	$\eta_{max}$ (%)	$E$ (Wh)
Case I: slight PSC	SRVM	79.04	99.74	$9.30 \times 10^3$
	Flyback-PV-IP	79.13	99.90	$9.24 \times 10^3$
	Flyback-PV-Bus	79.2	99.94	$9.36 \times 10^3$
Case II: medium PSC	SRVM	70.48	98.72	$1.42 \times 10^3$
	Flyback-PV-IP	70.73	99.07	$1.42 \times 10^3$
	Flyback-PV-Bus	70.89	99.30	$1.43 \times 10^3$
Case III: severe PSC	SRVM	49.49	95.76	$1.05 \times 10^3$
	Flyback-PV-IP	50.55	97.82	$1.07 \times 10^3$
	Flyback-PV-Bus	50.69	98.09	$1.08 \times 10^3$

1) *Slight PSC*: Under the slight PSC, the fourth module works with the daily data while the others work with fixed irradiance at  $1000 \text{ W/m}^2$ . Main simulation results of this case are shown in Fig. 10. The mismatch condition changes accordingly as the irradiance rises. The processed power in DPP converters also decreases, whereas the output power and efficiency increase, respectively. For the Flyback-PV-Bus architecture, although there is an extra boost converter utilized in the architecture with the LPPT control algorithm, it always has the advantage in terms of the processed power, system efficiency, and total power loss for the majority operation range among the three DPP converters. Comparing the SRVM and the Flyback-PV-IP construction, the processing powers are similar, whereas the output power and efficiency of SRVM are slightly higher than those of Flyback-PV-IP when the solar irradiation is lower than  $602.62 \text{ W/m}^2$ . Under the slightly shaded condition, the SRVM provided the lowest output power and efficiency. The calculated maximum output power of SRVM, Flyback-PV-IP construction, and Flyback-PV-Bus construction is 79.04W, 79.13W, and 79.2W, with the corresponding maximum efficiency of 99.74%, 99.90%, and 99.94%. The accumulated energy over the day for SRVM and Flyback-PV-IP is  $9.30 \times 10^3 \text{ Wh}$ ,  $9.24 \times 10^3 \text{ Wh}$ , while Flyback-PV-Bus construction has a higher energy of  $9.36 \times 10^3 \text{ Wh}$ .

2) *Medium PSC*: Under the medium PSC, main simulation results are shown in Fig. 11. Similar to the slight PSC, the partial shading condition for PV3 and PV4 varies accordingly, whereas the input irradiation is always lower than that in the slight PSC. Among the three DPP converters, the Flyback-PV-Bus converter processes the lowest power distinctly during the whole day. Additionally, both the output power and efficiency

are higher than those of other VE architectures. The calculated maximum output powers of SRVM, Flyback-PV-IP construction, and Flyback-PV-Bus construction are 70.48W, 70.73W, and 70.89W, with the corresponding maximum efficiency of 98.72%, 99.07%, and 99.30%. The accumulated energy of SRVM and Flyback-PV-IP is  $1.42 \times 10^3 \text{ Wh}$ , while Flyback-PV-Bus construction has a higher energy as  $1.43 \times 10^3 \text{ Wh}$ .

3) *Severe PSC*: This case is designed to show the comparison under severely mismatch conditions in Fig. 12. The efficiency of SRVM is found lower than that of Flyback-PV-Bus and Flyback-PV-IP at about 4%, while more power loss of SRVM is found compared with other two architectures, which is approximately 1.5W. It is worth noting that the processed power of SRVM is much larger than that of the other two converters, which results in the lowest output power, the lowest efficiency, and the most power loss. Comparing Flyback-PV-Bus converter and Flyback-PV-IP converter, the advantages of the former one are not prominent. Under severe shaded conditions, the SRVM provided the lowest output power and efficiency. The calculated maximum output powers of SRVM, Flyback-PV-IP construction, and Flyback-PV-Bus construction is 49.49W, 50.55W, and 50.69W, with the corresponding maximum efficiency of 95.76%, 97.82%, and 98.09%. The accumulated energy over the day for SRVM and Flyback-PV-IP are  $1.05 \times 10^3 \text{ Wh}$ ,  $1.07 \times 10^3 \text{ Wh}$ , while Flyback-PV-Bus construction has a higher energy as  $1.08 \times 10^3 \text{ Wh}$ . It shows that in the severely shaded conditions, the SRVM shows low adjust-ability.

### C. Simulated Output Voltage Comparison

Fig. 13 displays the comparison of the voltage balance effects of each DPP scheme. The irradiance on the fourth module changes from  $100 \text{ W/m}^2$  to  $1000 \text{ W/m}^2$  with the step at  $100 \text{ W/m}^2$ , when the others work under full irradiance at  $1000 \text{ W/m}^2$ . The output voltage of the SRVM increases as the irradiance rises from  $100 \text{ W/m}^2$  to  $900 \text{ W/m}^2$ , whereas the output voltages drop to 18 V when there is no shading condition. The average values of the output voltages in SRVM vary from 17.66 V to 18.92 V showing larger fluctuations than those in Flyback-PV-Bus converter and Flyback-PV-IP converter. The output voltages of each modules in the Flyback-PV-Bus converter and Flyback-PV-IP converter show more stability with the solar irradiance increasing. The average output voltages in the Flyback-PV-Bus converter and Flyback-PV-IP converter keep nearly at 18 V when the solar irradiance of the forth module is above  $200 \text{ W/m}^2$ . As shown in the above analysis, when the equalized voltage is selected at 18 V, the maximum error between theoretical values and simulation values of the SRVM is 5%, while the maximum errors of Flyback-PV-IP and Flyback-PV-bus are 4.4%.

## V. INDOOR EXPERIMENTAL EVALUATIONS

To verify the theoretical analysis of three VEs for different PSCs, the indoor experiment evaluation was conducted. The DC power supply is used to supply power to the PV module (PV-20 SFP2136). The DC electronic load works as the load to emulate MPP by controlling the output module voltage. Main

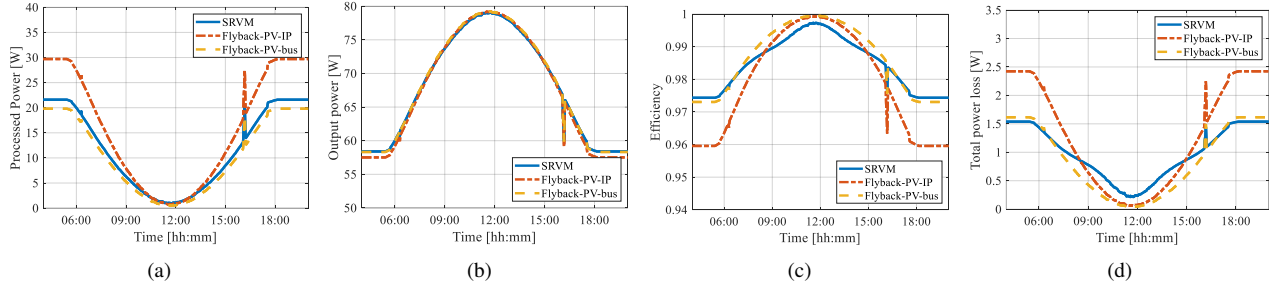


Fig. 10: Simulation results under slight PSC. (a) Processed power. (b) Output power. (c) System efficiency. (d) Total Power losses.

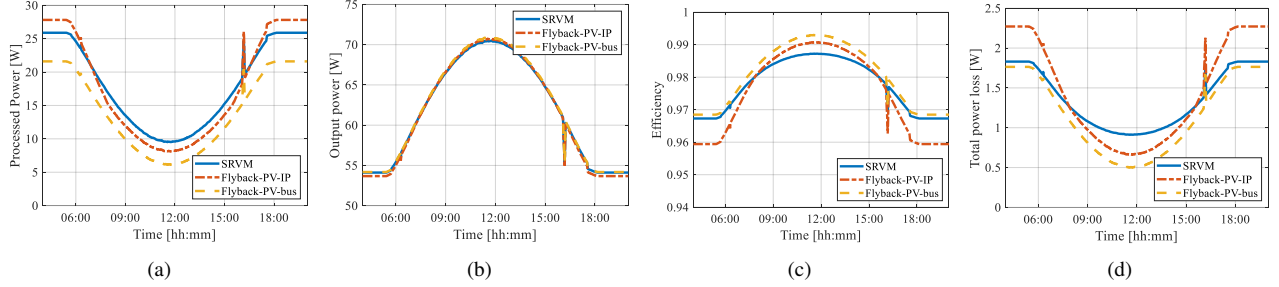


Fig. 11: Simulation results under medium PSC. (a) Processed power. (b) Output power. (c) System efficiency. (d) Total Power losses.

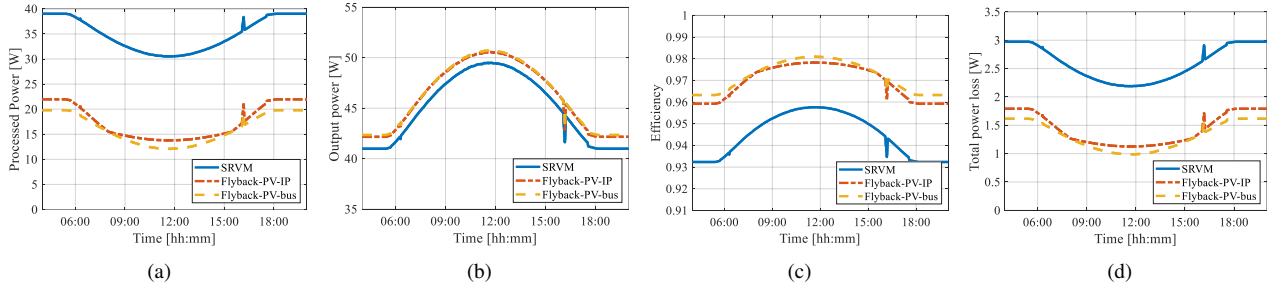


Fig. 12: Simulation results under severe PSC. (a) Processed power. (b) Output power. (c) System efficiency. (d) Total Power losses.

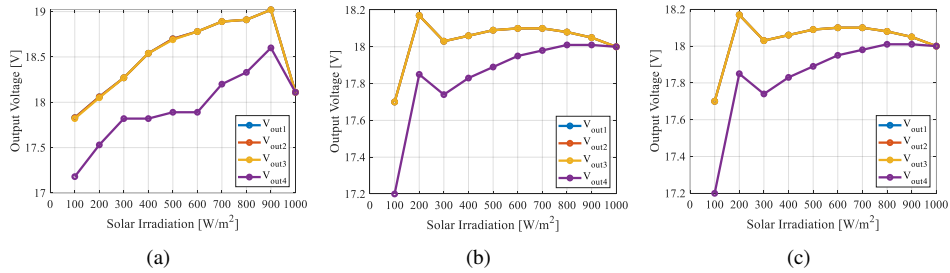


Fig. 13: Simulation output voltage of each PV module in case 1. (a) Output voltage of SRVM. (b) Output voltage of Flyback-PV-IP. (c) Output voltage of Flyback-PV-Bus.

components and parameters for the built prototypes are shown in TABLE IV. The experiment setup is shown in Fig. 14, where Flyback-PV-IP and Flyback-PV-bus are conducted in a hardware by changing the connection of the boost converter. In order to accurately control the irradiation, the indoor experiment bench is arranged. For the slight PSC experiment, no mismatches are set for PV1, PV2, and PV3, while 72 discrete operation points are used for PV4 to emulate the real-day irradiance in the University of Nevada. The detailed distribution of the selected 72 typical points is illustrated in

Fig. 9. Similarly, 62 discrete operation points are used for PV4 to emulate 80% of  $I_r$  under the medium PSC. 54 discrete operation points are used for PV4 to emulate 40% of  $I_r$  under the severe PSC. Other irradiation conditions are set the same as the simulation.

#### A. Slight PSC

In the first experimental case, there are 72 points selected for the fourth module as shown in the curve in Fig. 9. The experiment results show in Fig. 15, the output power curves

TABLE IV: Main components and parameters of the built experimental prototypes

SRVM		Flyback-PV-Bus and Flyback-PV-IP	
Parameter	Model and Value	Parameter	Model and Value
Switches	FDS86240	Flyback converter switch	IRFP460
Resonant capacitor	62 nF	Boost converter switch	IRFP250N
Transformer magnetic inductor	85 $\mu$ H	Magnetic inductor	300 $\mu$ H
Transformer leakage inductor	5.25 $\mu$ H	Inductor	0.5 mH
Transformer turns ratio	4:1	Primary side capacitance	220 $\mu$ F
VM Capacitor	94 $\mu$ F	Secondary side capacitance	47 $\mu$ F
VM Diode	SB1045L	Boost converter capacitance	47 $\mu$ F

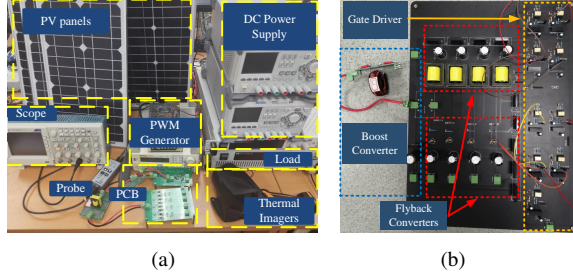


Fig. 14: Photograph of the prototypes: (a) SRVM with the experiment set. (b) Flyback-PV-IP and Flyback-PV-bus.

show a similar tendency to the simulation results, which vary from 52W to 72W. The practical output powers of three DPPs are approximately equal. Although the efficiency show a similar tendency to the simulation results, there is still fluctuation, especially under the low irradiation. In most cases, the efficiency of SRVM is approximate 92% - 95%, which is larger than the other two DPP converters at around 2%, while the power loss of SRVM is lower around 3W.

### B. Medium PSC

The medium partial shading case is designed as second condition. Meanwhile, the last module works under continuously-changing cases under 800 W/m<sup>2</sup>. The experiment results show in Fig. 16, the output power curves show a similar tendency to the simulation results, which vary from 47.75W to 63.92W. In this case, the output power of per DPP architecture is approximately equal. Actually, the output power of the SRVM is a little higher than those of Flyback-PV-IP and Flyback-PV-Bus converter, which shows slight advantages in the long-term application. The maximum output power of the SRVM is 67.22W, whereas the maximum output powers of Flyback-PV-IP and Flyback-PV-Bus are 70.77W and 70.75W, respectively. The efficiency in all DPP systems fluctuates largely between 89% and 95% with the power losses oscillating greatly between 6W and 3.2W.

### C. Severe PSC

In the severely shaded case, the condition is set as the third item. The experiment results show in Fig. 17, the output power curves show a similar tendency to the simulation results. The output powers of the SRVM are evidently lower than the output powers of the Flyback-PV-IP and Flyback-PV-bus, which is similar to the simulation results. The maximum efficiencies of the Flyback-PV-bus and the Flyback-PV-IP achieve 89.17% and 88.33%, while the SRVM can only achieve 85.88%. The

average power loss of Flyback-PV-bus and the Flyback-PV-IP is approximately 5.11W and 5.33W, respectively whereas the average power loss of the SRVM is 5.97W.

All results are compared to experimental results with the bypass-diode scheme. The experimental results indicated that all VEs can provide larger power for the load in almost all cases.

As shown in Fig. 15, in a few slightly-shadow cases, the output power and efficiency of the bypass-diode schemes are larger compared to the Flyback-PV-IP and Flyback-PV-bus.

### D. Indoor Experimental Power Loss Distribution

Since three VEs all utilized the voltage equalization method, none of these schemes are able to reach the actual maximum power points. Here the total power loss can be categorized into two parts: one is the power losses in DPP converters, which is named as DPP power losses. The other is the power losses due to the voltage equalization, which is named as voltage equalization losses. Fig. 18 and Fig. 19 displays the measured voltage equalization losses and DPP power losses, respectively. It is indicated that the voltage equalization losses change relatively smoothly with solar irradiation. Furthermore, the measured voltage equalization losses of SRVM is slightly less than other VEs. The Flyback-PV-bus demonstrates fewer voltage equalization losses compared to the Flyback-PV-IP in all cases due to the minimal power processing algorithm. Under severe PSC, the measured DPP power losses of the SRVM is higher than other VEs.

### E. Indoor Experimental Output Voltage Drift

The output voltage of each module, e.g.  $V_{pv,x}$ , is measured as shown in Fig. 20. The working conditions are set the same with the simulation. For a quantitative analysis of the voltage balance performance, the balance error  $E_V$  is introduced to investigate the difference between the actual output voltage of PV modules  $V_{pv,x}$  and the expected equalization voltage  $V_{ref}$ , which is expressed as:

$$E_V = \frac{|V_{PV,x} - V_{ref}|}{V_{ref}} \quad (53)$$

Although  $V_{pv}$  of the shaded module in SRVM is lower than the others, it shows voltage balance of each output voltage with maximum error at around 4.56%. The average output voltage drifts are changing from 17.79 V to 18.67 V. The Flyback-PV-IP scheme and Flyback-PV-bus scheme show similar varying trends since both schemes utilize VE algorithms. The average output voltage drifts are changing from 17.59 V to 18.35 V with maximum error at 6.11%. When the solar irradiance on

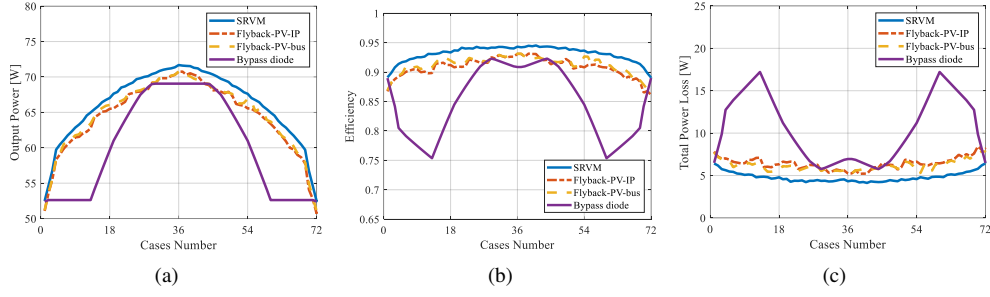


Fig. 15: Indoor experimental results under slightly partial shading condition as case 1. (a) Output powers. (b) System efficiency. (c) Total Power losses.

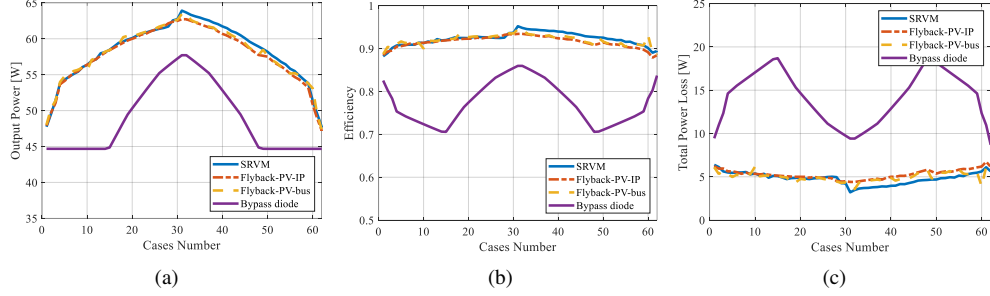


Fig. 16: Indoor experimental results under medium partial shading condition as case 2. (a) Output powers. (b) System efficiency. (c) Total Power losses.

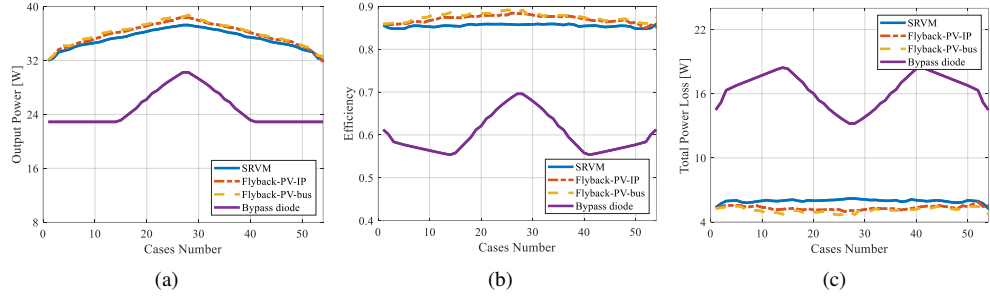


Fig. 17: Indoor experimental results under severely partial shading condition as case 3. (a) Output powers. (b) System efficiency. (c) Total Power losses.

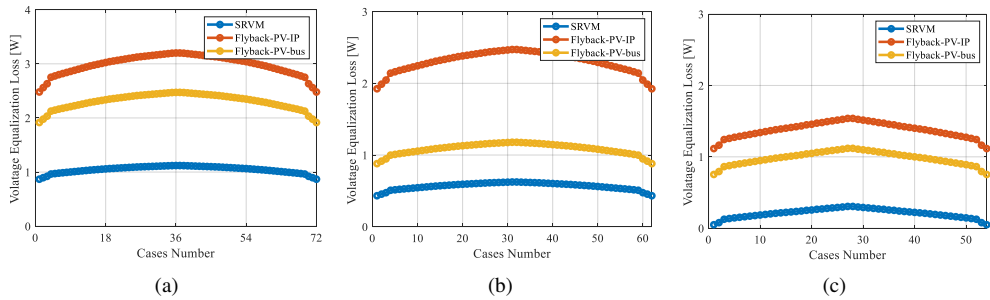


Fig. 18: Measured voltage equalization losses under different PSCs. (a) Slight PSC. (b) Medium PSC. (c) Severe PSC.

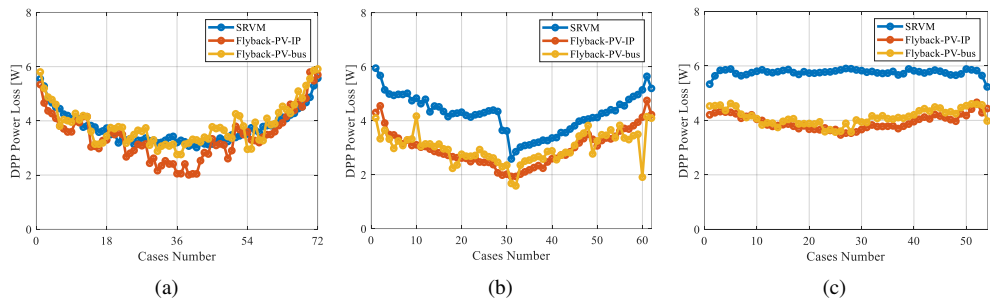


Fig. 19: Measured DPP power losses under different PSCs. (a) Slight PSC. (b) Medium PSC. (c) Severe PSC.



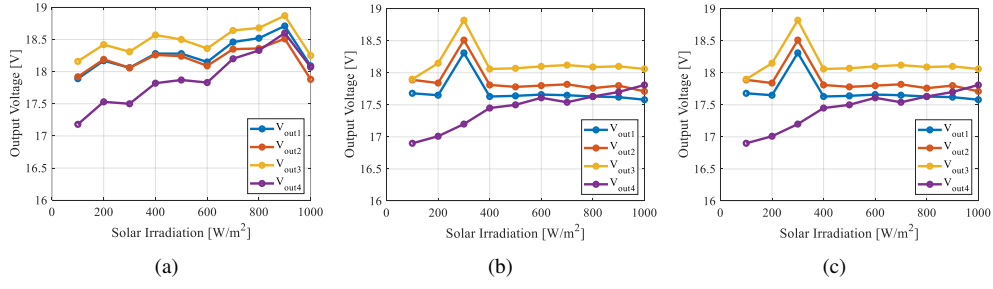


Fig. 20: Indoor experimental output voltage of each PV module in case 1. (a) Output voltage of SRVM. (b) Output voltage of Flyback-PV-IP. (c) Output voltage of Flyback-PV-Bus.

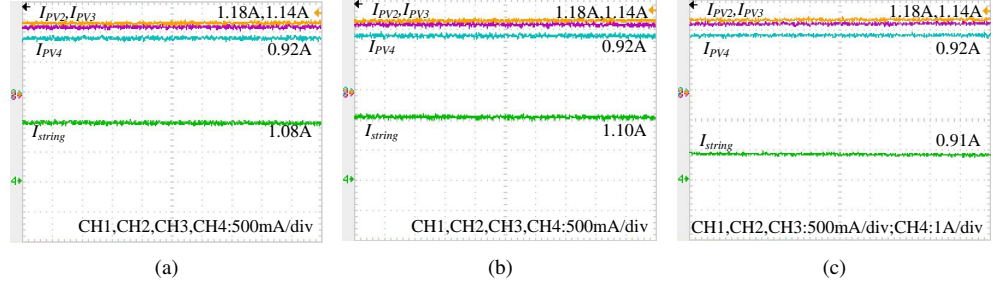


Fig. 21: Indoor experimental module current and string current under slight PSC. (a) SRVM, (b) Flyback-PV-IP, (c) Flyback-PV-bus.

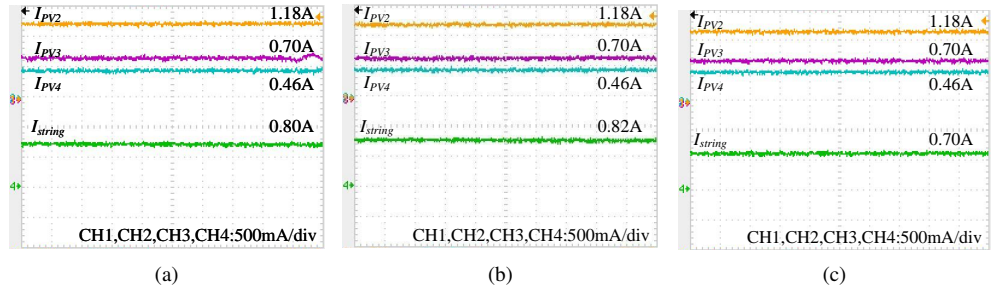


Fig. 22: Indoor experimental module current and string current under medium PSC. (a) SRVM, (b) Flyback-PV-IP, (c) Flyback-PV-bus.

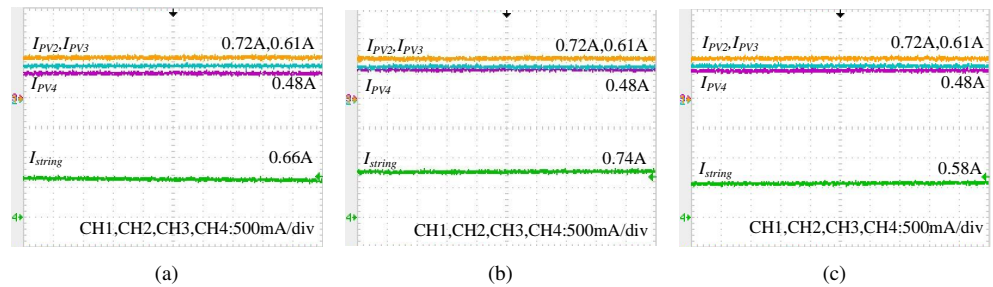


Fig. 23: Indoor experimental module current and string current under severe PSC. (a) SRVM, (b) Flyback-PV-IP, (c) Flyback-PV-bus.

TABLE V: Indoor experimental voltage drift under different PSCs

Test Conditions	SRVM (%)			Flyback-PV-IP(%)			Flyback-PV-bus(%)		
	Maximum	Minimum	Average	Maximum	Minimum	Average	Maximum	Minimum	Average
Slight PSC	1.83	0.39	0.74	6.24	3.41	4.67	6.24	2.41	4.40
Medium PSC	1.83	0.50	1.10	6.24	2.65	4.12	6.24	2.41	4.13
Severe PSC	2.00	0.10	0.83	6.47	3.41	3.76	6.47	2.41	3.93

TABLE VI: Indoor experimental current distribution under different PSCs

Test Conditions	SRVM (%)			Flyback-PV-IP(%)			Flyback-PV-bus(%)		
	Maximum	Minimum	Average	Maximum	Minimum	Average	Maximum	Minimum	Average
Slight PSC	16.32	6.12	9.69	17.59	4.52	8.79	21.15	0	6.25
Medium PSC	46.67	18.67	35.67	48.22	21.04	34.63	70.49	0	52.46
Severe PSC	38.46	6.15	31.92	63.13	4.31	31.56	70.49	0	30.73



TABLE VII: California Efficiency of Each Module Under Different Conditions

Test Conditions	SRVM					Flyback-PV-IP				Flyback-PV-bus			
	PV 1	PV 2	PV 3	PV 4	PV 1	PV 2	PV 3	PV 4	PV 1	PV 2	PV 3	PV 4	PV 4
100%	99.47%	98.95%	98.95%	99.47%	98.95%	99.47%	98.95%	98.95%	99.47%	99.47%	98.42%	98.95%	98.95%
75%	96.20%	98.45%	96.97%	97.78%	96.97%	98.45%	96.97%	97.94%	96.30%	98.45%	96.97%	97.78%	97.78%
50%	96.54%	95.35%	94.05%	96.54%	97.74%	97.62%	94.16%	94.04%	98.81%	97.62%	96.54%	94.76%	94.76%
30%	95.75%	96.42%	92.84%	94.18%	96.42%	96.64%	95.75%	95.30%	94.41%	97.32%	95.97%	93.96%	93.96%
20%	92.59%	89.26%	85.19%	91.11%	91.85%	87.41%	92.96%	86.30%	81.85%	86.30%	90.74%	82.60%	82.60%
10%	87.96%	90.74%	72.22%	81.48%	82.41%	72.22%	71.30%	75.00%	82.41%	72.22%	71.30%	75.00%	75.00%
California Efficiency	95.92%	96.81%	94.67%	95.89%	96.32%	96.51%	95.10%	95.15%	95.48%	96.53%	95.49%	95.07%	95.07%

TABLE VIII: Comparison Results of Key Performance Indicators based on indoor Experimental Evaluations

DPP Schemes	Average Power (W)			Average Efficiency			Average Power Loss (W)			Maximum $E_V$	$V_{stress}$ (V)	Maximum $V_{dr}(\%)$	Maximum $R_T(\%)$	California efficiency(%)
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3					
SRVM	66.08	58.28	35.19	93.14%	92.30%	85.49%	4.80	4.81	5.97	4.56%	80	2.00	46.67	95.82
Flyback-PV-IP	64.47	57.81	35.83	90.85%	91.57%	87.03%	6.42	5.27	5.32	6.11%	20	6.47	63.13	95.88
Flyback-PV-bus	64.73	58.09	36.05	91.23%	92.01%	87.55%	6.16	5.00	5.11	6.11%	22	6.47	70.49	95.64

the forth module is less than  $400 \text{ W/m}^2$ , the  $V_{pv}$  of each module shows large disturbance. When the solar irradiance improves above  $400 \text{ W/m}^2$ , the change becomes gentle.

The maximum values, minimum values, and average values of voltage drift for three VEs under different operation conditions are shown in TABLE V. It is noted that the voltage drift of SRVM remains in a relatively stable state with respect to the severity of PSCs whereas the drift of the other two VEs would increase accordingly.

Furthermore, the maximum voltage stress on the switches,  $V_{stress}$ , can also be calculated accordingly. In Flyback-PV-IP and Flyback-PV-bus,  $V_{stress}$  equals to the output voltage of each module whereas the corresponding  $V_{stress}$  in SRVM equals to the string voltage. Therefore, if the PV string is extended to  $n$  modules,  $V_{stress}$  in the Flyback-PV-IP and Flyback-PV-bus will maintain at  $V_{pv}$  while the  $V_{stress}$  increases with the number of PV modules and equals to  $nV_{pv}$  in SRVM.

#### F. Indoor Experimental Current Distribution

Fig. 21, Fig. 22, and Fig. 23 display the experimental string currents and module currents of three VEs under slight PSC and severe PSC, respectively. All these converters are working on continuous current modes. It can be seen that the string current in Flyback-PV-IP and SRVM, i.e.  $I_{s-IP}$  and  $I_{s-SRVM}$ , are approximately equal to the average value of  $I_{PV,x}$ .  $I_{s-bus}$  follows the value of selected  $I_{PV,x}$ . In slight PSC case,  $I_{s-bus}$  follows  $I_{PV4}$ , while it follows  $I_{PV3}$  in severe PSC, which ensure the least processing power.

TABLE VI displays maximum, minimum, and average current in three VEs. It indicates that the Flyback-PV-bus achieve the least current under slight PSC while the SRVM deliver the largest current under severe PSC.

#### G. California Efficiency

In this section, the weighted efficiency standard from the California Energy Commission is utilized to assess the system efficiency [40].

In the measurement, the PV power under various PSCs is measured as the input power and the system output power after the designed VE schemes is measured as the output power. Therefore, the weighted efficiency will indicate the recovery capability of VEs for various PSCs.

The weighted efficiency, i.e.,  $\eta_w$ , is calculated using the data taken at the various levels of power as the following equation:

$$\eta_w = F_1\eta_5 + F_2\eta_{10} + F_3\eta_{20} + F_4\eta_{30} + F_5\eta_{50} + F_6\eta_{75} + F_7\eta_{100} \quad (54)$$

where,  $\eta_5$ ,  $\eta_{10}$ ,  $\eta_{20}$ , etc., is the measures efficiency values at 5%, 10%, 20%, ect. of rated power from the official document.  $F_1$ ,  $F_2$ ,  $F_3$ , etc. are the weighting factors, which are defined by the standard [40]. TABLE VII displays the measured efficiency of each scheme under different conditions, where the conversion efficiency is calculated by (54). Consequently, the average California efficiency of SRVM, Flyback-PV-IP, and Flyback-PV-bus is 95.82%, 95.88%, and 95.64%. TABLE VIII summarizes the indoor experimental results and the performance quantization of three VEs.

## VI. OUTDOOR EXPERIMENTAL EVALUATIONS

### A. Outdoor Experimental Setup

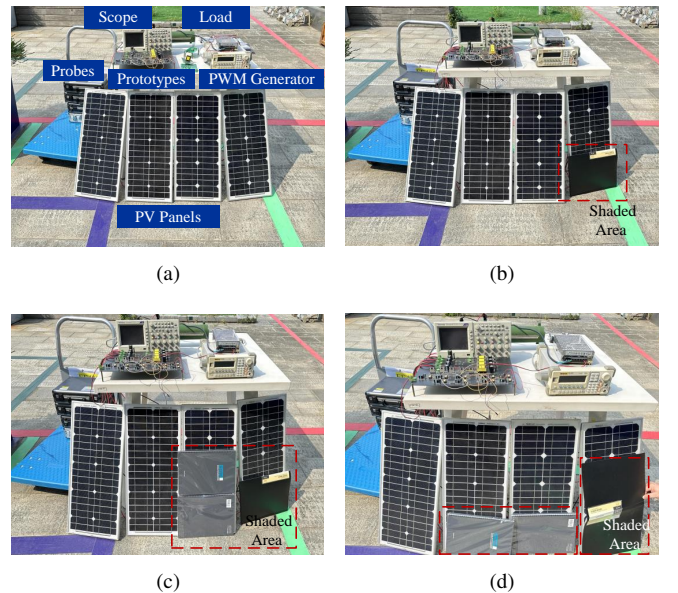


Fig. 24: Outdoor experimental Prototype under different conditions. (a) The whole prototype, (b) Slightly shaded case, (c) Medium shaded case, (d) Severely shaded case.

Fig. 24(a) shows the outdoor experimental set-up, where PV panels, oscilloscopes, voltage and current probes, converters,

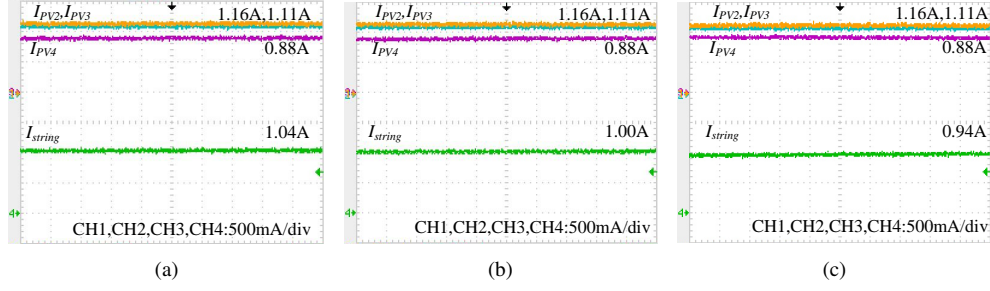


Fig. 25: Outdoor experimental module current and string current under slight PSC. (a) SRVM, (b) Flyback-PV-IP, (c) Flyback-PV-bus.

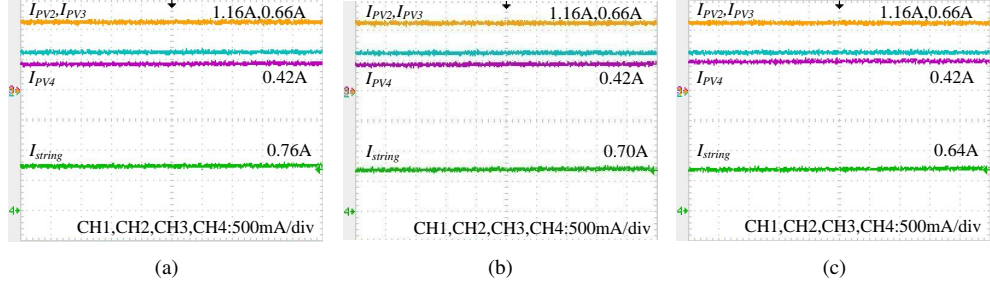


Fig. 26: Outdoor experimental module current and string current under medium PSC. (a) SRVM, (b) Flyback-PV-IP, (c) Flyback-PV-bus.

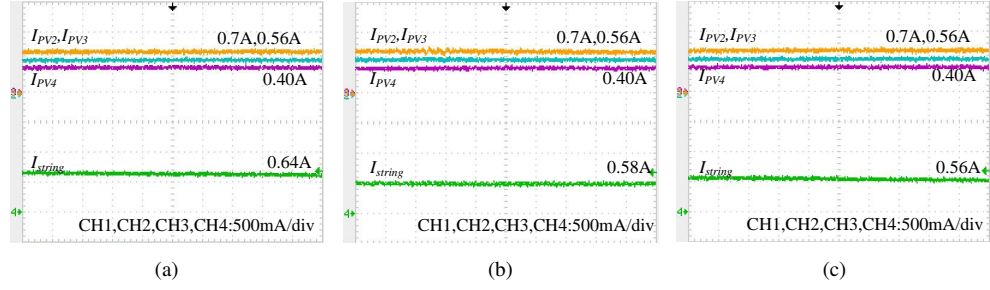


Fig. 27: Outdoor experimental module current and string current under severe PSC. (a) SRVM, (b) Flyback-PV-IP, (c) Flyback-PV-bus.

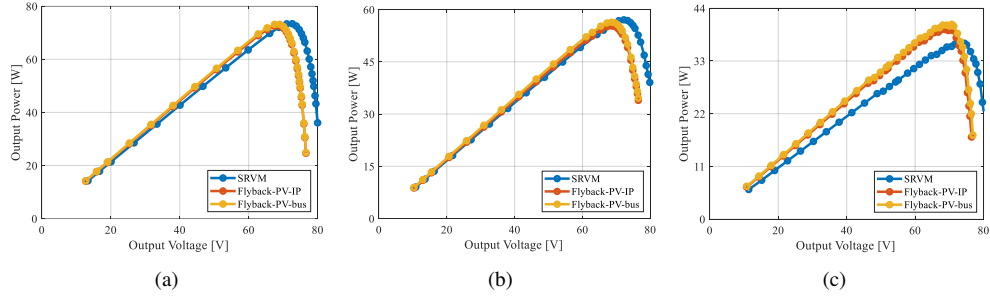


Fig. 28: Outdoor experimental results under different conditions. (a) Slightly shaded case, (b) Medium shaded case, (c) Severely shaded case.

micro-controllers, and loads are placed on a moving cart. The whole system is placed in an open outdoor area. In the outdoor experiments, the modules are covered by plastic panels of different areas to emulate different partial shading conditions, as illustrated in Fig. 24(b), Fig. 24(c), and Fig. 24(d) respectively.

### B. Outdoor Experimental Results

The output current of each module under different shadow cases are shown in Fig. 25, Fig. 26, Fig. 27. Fig. 28 displays the measured output power results of each shadow case in

outdoor experiments. Experimental results prove that all three schemes can operate and eliminate mismatch successfully under real outdoor conditions. Regarding the output power, the measured result for SRVM is around 74V while the corresponding results for Flyback-PV-IP and Flyback-PV-bus is around 68V. Under the slightly-shadow case and the medium-shadow case, the measured output power of SRVM will be slightly higher than the other two schemes. Under the case of heavy shading, the measured output power of SRVM is found much lower than the other VE schemes.

TABLE IX: Comparison Summary for Key Performance Indexes

Feature	SRVM	Flyback-PV-IP	Flyback-PV-bus
Reliability	High	Low	Medium
Cost	Low	High	High
Coupling degree	Low	Medium	High
Application	Distributed generation	Large scale	Large scale
Function Extension	Fault tolerant	Arc fault detection	Arc fault detection

## VII. CONCLUSION

In this paper, a comprehensive comparison among three typical VE schemes, including SRVM, Flyback-PV-IP, and Flyback-PV-Bus with LPP algorithm, is conducted. Main characteristics and performance indexes such as the control algorithm, the processed power, the output power, power losses, efficiencies under different PSCs, arc fault detection, long-string or large-scale application are covered systematically. TABLE IX lists the comparison results of three VEs through simulation and experimental evaluations. Main findings are summarized as follows:

- 1) **Control Flexibility:** For the Flyback-PV-IP scheme, the closed-loop voltage balance should be implemented. In addition to the voltage balance control, the total-LPPT algorithm is also demanded for the Flyback-PV-bus. However, the SRVM usually works with fixed duty cycle and fixed switching frequency by the open-loop control, which is easy-to-implement.
- 2) **Power Losses under various PSCs:** The power loss analysis of VEs under different PSCs shows that the power loss in SRVM increases with the deterioration of mismatching conditions due to the sharp increase in the processing power. For Flyback-PV-IP and Flyback-PV-bus schemes, the loss distribution shows distinct difference. Specifically, the losses in the flyback converter also increase with the deterioration of mismatching conditions, while the loss increase in the central converter is not obvious.
- 3) **Output Power and Efficiencies:** As shown in the experimental results, the efficiencies of all DPPs vary almost between 90% to 95% under mild and moderate shaded conditions. Although the efficiency of SRVM under mild and moderate shaded conditions is generally good, the output powers and efficiency of the SRVM under the severely shaded conditions are much lower than that of Flyback-PV-IP and Flyback-PV-Bus architectures. In general, the research in this article shows that the Flyback-PV-Bus architecture has advantages in terms of output power and efficiency. The simulation and experiment results also show that all the DPP schemes achieve the voltage balance at around 18 V. With the deterioration of mismatching conditions, the Flyback-PV-IP and Flyback-PV-Bus DPP converters exhibit better adaptability considering that more output power and higher efficiency can be achieved compared with SRVM.
- 4) **Long-string or large-scale Applications:** SRVM has the advantages of small size and high voltage balance capability. However, for long-string applications, the switch voltage stress will be sharply increased with the PV module number. Therefore, SRVM is more suitable for

module level or even sub-module level applications. For long-string or large-scale applications, the architecture of the Flyback-PV-IP, the Flyback-PV-bus will be better.

- 5) **Arc Fault Detection:** The control algorithms for Flyback-PV-bus converters exhibits more control flexibility. Therefore, it can achieve additional function, such as arc fault detection, which will be further discussed in future.
- 6) **VE Selection:** For the situations where the weather changes frequently, Flyback-PV-IP and Flyback-PV-bus are suggested to address the severely shaded cases. For areas with relatively stable weather SRVM is a proper scheme to maintain efficient and stable output power.

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**Xue Wang** (Student Member) was born in Hebei, China, in 1993. She received the B.S. degree in applied physics from Hebei Agricultural University, Baoding, China in 2015. In 2020, she received the master degree in sustainable energy from Xi'an Jiaotong-Liverpool University, Suzhou, China. She is currently working toward the Ph.D. degree at the University of Liverpool, U.K..

Her current research interests include DC–DC converter, photovoltaic generation system, differential power processing technologies, fault detection,

and fault tolerant.





**Huiqing Wen** (Senior Member, IEEE) received the B.S. and M.S. degrees from Zhejiang University, Hangzhou, China, in 2002 and 2006, respectively, and the Ph.D. degree from the Chinese Academy of Sciences, Beijing, China, in 2009, all in electrical engineering. From 2009 to 2010, he was an Electrical Engineer with the GE (China) Research and Development Center Company, Ltd., Shanghai, China. From 2010 to 2011, he was an Engineer with the China Coal Research Institute, Beijing, China. From 2011 to 2012, he was a Postdoctoral Fellow

with the Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates. Since 2013, he has been with the Department of Electrical and Electronic Engineering, Xi'an Jiaotong-Liverpool University (XJTLU), Suzhou, China, where he is currently an Professor. He has authored or co-authored more than 50 peer-reviewed technical papers in leading journals.

His research interests include renewable energy, electric vehicle, power electronics, microgrid, and power semiconductor devices. Dr. Wen is the Associate Editor of IEEE Access, International Journal of Photoenergy, and Journal of Power Electronics. He is a Fellow of the Institution of Engineering and Technology (FIET).



**Guanying Chu** (Member, IEEE) received the B.S. and M.S. degrees in electrical and electronic engineering from the University of Sheffield, Sheffield, U.K., in 2014 and 2015, respectively. In 2021, he received Ph.D. degree in electrical and electronic engineering from the University of Liverpool, Liverpool, U.K.. He is currently a Lecturer in the Department of Electrical and Electronics Engineering, School of Advanced Technology at Xi'an Jiaotong-Liverpool University (XJTLU), Suzhou, China.

His current research interests include bidirectional DC-DC converter, photovoltaic generation system, and differential power processing technologies.



**Yinxiao Zhu** (Member, IEEE) received the B.Eng. degree in microelectronic science and engineering from the Tianjin University of Technology and Education, Tianjin, China, in 2017. He received the M.Sc. (with Distinction) degree in sustainable energy technology and the Ph.D. degree in electrical and electronic engineering from the University of Liverpool, Liverpool, U.K., in 2019 and 2023, respectively. He is currently a Postdoctoral Research Fellow with the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His current research interests include the grid-integration of photovoltaic systems and control of power electronics, in particular, grid supportive controls and differential power processing technologies.



**Yong Yang** (Senior Member, IEEE) received the B.S. degree in automation from Xiangtan University, Xiangtan, China, in 2003, the M.S. degree in Electrical Engineering from Guizhou University, Guiyang, China, in 2006, and the Ph.D. degree in Electrical Engineering from Shanghai University, Shanghai, China, in 2010.

He is currently a full Professor with the School of Rail Transportation, Soochow University. From December 2017 to December 2018, he was a Visiting Scholar with Center for High Performance Power Electronics (CHPPE) of The Ohio State University, Columbus, USA. He has coauthored more than 120 journal and conference papers. His current research interests include model predictive control in power electronic converters, distributed energy resource interfacing and high-performance motor drive control.



**Yiwang Wang** (Member, IEEE) received the B.S. degree in electrical engineering and automation from the Kunming University of Science and Technology, Kunming, China, in 2005, the M.S. degree in power electronics from Jiangnan University, Wuxi, China, in 2008, and the Ph.D. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2020. From June 2016 to June 2017, he was a Visiting Scholar with the CURENT Research Center, University of Tennessee, Knoxville, TN, USA. He is currently an Associate Professor

with the Collaborative Innovation Center of Smart Energy Equipment and Power Conversion, Suzhou Vocational University, Suzhou, China. His research interests include power electronics intelligent control, and the applications of power electronics and renewable energy generation.



**Lin Jiang** (Senior Member,) received the B.Sc. and M.Sc. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, and the Ph.D. degree in electrical engineering from the University of Liverpool, Liverpool, U.K., in 1992, 1996, and 2001, respectively. He was a Post-Doctoral Research Assistant with the University of Liverpool from 2001 to 2003 and a Post-Doctoral Research Associate with the Department of Automatic Control and Systems Engineering, University of Sheffield, Sheffield, U.K., from 2003 to 2005. He was a Senior Lecturer with the University of Glamorgan, Wales, U.K., from 2005 to 2007, and joined the University of Liverpool in 2007. He is currently a Reader with the Department of Electrical Engineering and Electronics, University of Liverpool, U.K..

His current research interests include control and analysis of power system, smart grid, and renewable energy.