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BURN-IN COMPENSATION WITH FOVEATED RENDERING DISPLAY

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TECHNOLOGICAL FIELD

[0001] Examples of this disclosure relate generally to methods, apparatuses, and computer program products for reducing organic light-emitting diode (OLED) degradation associated with the electronic devices.

BACKGROUND

[0002] Artificial reality is a form of reality that has been adjusted in some manner before presentation to a user, which may include, for example, a virtual reality, an augmented reality, a mixed reality, a hybrid reality, Metaverse reality or some combination or derivative thereof. Artificial reality content may include completely computer-generated content or computer-generated content combined with captured (e.g., real-world) content. The artificial reality content may include video, audio, haptic feedback, or some combination thereof, any of which may be presented in a single channel or in multiple channels (such as stereo video that produces a three-dimensional (3D) effect to the viewer). Additionally, in some instances, artificial reality may be associated with applications, products, accessories, services, or some combination thereof, that may be used to, for example, create content in an artificial reality or are otherwise used in (e.g., to perform activities in) an artificial reality. Head mounted displays (HMDs) including one or more near-eye displays may often be used to present visual content to a user for use in artificial reality applications.

[0003] Many head mounted display systems may include one or more near-eye displays comprising an OLED display. With the varying uses of head mounted display systems, these devices may need high resolution OLED displays for optimal user experience and to avoid motion sickness that may be associated with head mounted display systems. Providing high resolution requires an abundance of data to be transmitted through the display system, which may increase degradation of the OLED display. To reduce the amount of transferring data between the application processor (AP) and the display driver integrated circuit (DDIC) and reduce general processing unit utilization or reduce power of AP many head mounted display systems may utilize foveated rendering. Foveated rendering may be a rendering technique which uses an eye tracker integrated with a head mounted display system to reduce the rendering

workload by reducing image quality in the peripheral vision, outside of the zone gazed by the fovea. In such systems, the OLED display may need a burn-in mechanism in the display driver integrated circuit (DDIC) to reduce image stick and improve lifetime of the OLED display. Although, this method may improve lifetime, the burn-in mechanism may utilize an enormous size of memory in the DDIC because the burn-in mechanism may still use all areas of display (foveal, blend, peripheral, or etc.) regardless of foveated rendering display, therefore leading to increased chip size of the DDIC.

[0004] In view of the foregoing drawbacks, it may be beneficial to provide an improved burn-in mechanism (herein referred to as burn-in compensation mechanism) to reduce memory needed to render foveated rendering displays and reduce chip size of DDIC in head mounted display systems, therefore reducing costs, and improving lifetime of OLED displays.

BRIEF SUMMARY

[0005] Examples of the present disclosure are described for a head-mounted display system which may be associated with foveated rendering utilizing a burn-in compensation mechanism. The burn-in compensation mechanism may determine the stress of each pixel of an image with varying block sizes, control foveal, blend, and peripheral area of image or display separately to reduce visual artifacts.

[0006] In an example, a head mounted display system may include a display panel (e.g., an OLED display) including a plurality of pixels; a second processor configured to divide the display panel into a plurality of simulated blocks, estimated via an OLED lifetime decay curve, associated with areas captured by foveated rendering (e.g., foveal, blend, and peripheral) and stress data; a first processor to calculate stress data using the simulated blocks, and to compensate image data based on an accumulation of stress data, wherein the first processor is further configured to generate the accumulate stress data for each block separately.

[0007] In some examples, the first processor may be configured to convert a data signal to an analog data signal to drive digital processing of the data signal, wherein the first processor is further configured to generate a timing signal to drive TFT; and a timing controller configured to control the data driver and the burn-in compensation simulator.

[0008] In some other examples, the first processor may further be configured to calculate the stress data of the pixels in the blocks, a first memory to transmit stress data to a second memory;

a second memory configured to receive and store the stress data from the a first memory, wherein the second memory comprises a look up table, and a second processor configured to simulate blocks based on a received stress signal from the second memory.

[0009] The first processor may be configured to calculate an average value of stress values to represent a degradation degree of the pixels in a block, and to output the average value as the stress data in every frame. The first processor may sequentially output a stress value that represents a degradation degree of a respective pixel of the pixels in the blocks as the stress data in every frame.

[0010] Additional advantages will be set forth in part in the description which follows or may be learned by practice. The advantages will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The summary, as well as the following detailed description, is further understood when read in conjunction with the appended drawings. For the purpose of illustrating the disclosed subject matter, there are shown in the drawings exemplary embodiments of the disclosed subject matter; however, the disclosed subject matter is not limited to the specific methods, compositions, and devices disclosed. In addition, the drawings are not necessarily drawn to scale. In the drawings:

[0012] FIG. 1 illustrates an example head mounted display associated with artificial reality content.

[0013] FIG. 2 illustrates a block diagram of an exemplary hardware or software architecture, in accordance with an example.

[0014] FIG. 3 illustrates example areas captured via foveated rendering.

[0015] FIG. 4 is a block diagram illustrating an example data pipeline associated with a burn-in compensation mechanism, in accordance with an example.

[0016] FIG. 5 is a block diagram illustrating a head mounted display system according to an example.

[0017] FIG. 6A, FIG. 6B and FIG. 6C illustrates exemplary blocking of a display panel.

[0018] FIG. 7A, FIG. 7B and FIG. 7C illustrates example burn-in compensated blocks, in accordance with an example.

[0019] FIG. 8A, FIG. 8B, FIG. 8C and FIG. 8D illustrates burn-in compensation associated with image data, according to an example.

[0020] FIG. 9A and FIG. 9B illustrate compensation of blended area block, in accordance with an example.

[0021] FIG. 10 illustrates parameter chart of blocks associated with areas of views captured via foveated rendering, in accordance with an example.

[0022] FIG. 11 exemplary burn-in compensation mechanism simulated block size of each foveal rendered area, in accordance with an example.

[0023] FIG. 12 is a flowchart illustrating a method of compensating image or video data associated with a burn-in compensation mechanism.

[0024] The figures depict various embodiments for purposes of illustration only. One skilled in the art will readily recognize from the following discussion that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles described herein.

DETAILED DESCRIPTION

[0025] Some embodiments of the present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which some, but not all embodiments of the invention are shown. Indeed, various embodiments of the invention may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Like reference numerals refer to like elements throughout.

[0026] As defined herein a “computer-readable storage medium,” which refers to a non-transitory, physical or tangible storage medium (e.g., volatile or non-volatile memory device), may be differentiated from a “computer-readable transmission medium,” which refers to an electromagnetic signal.

[0027] As referred to herein a “display driver IC (DDIC)” may refer to a core device, integrated circuit, or processor that provide translation, interface, and control between a microprocessor (MPU), microcontroller (MCU) or other circuitry system for displays such as

liquid crystal display (LCD), light emitting diode (LED), OLED, digital light processing (DLP), vacuum fluorescent and active-matrix organic light-emitting diode (AMOLED).

[0028] As referred to herein a "static random-access memory (SRAM)" may refer to a type of random-access memory (RAM) that is volatile memory, meaning data is lost when power is removed.

[0029] As referred to herein a "flash memory" may refer to a type of nonvolatile memory that may erase data in units called blocks and may rewrite data at a byte level.

[0030] As referred to herein a "block" may refer to 'M' by 'N' pixels corresponding to a group of pixels that may correspond to the unit of accumulating stress and compensation.

[0031] As referred to herein a "OLED display" may refer to an organic light-emitting diode in which the emissive electroluminescent layer is a film of organic compound that emits light in response to an electric current. This organic layer is situated between two electrodes; typically, at least one of these electrodes is transparent.

[0032] As referred to herein a "foveated rendering display" may refer to a rendering technique which uses an eye tracker integrated with a virtual reality headset to reduce the rendering workload by reducing the image quality in the peripheral vision (outside of the zone gazed by the fovea)

[0033] As referred to herein a "OLED lifetime curve" may refer to a dynamic model that predicts asset failure of OLED through the application of data science principles. Leveraging statistical distribution, the lifetime curve may quantify the uncertainty around a probability of failure curve.

[0034] It is to be understood that the methods and systems described herein are not limited to specific methods, specific components, or to particular implementations. It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting.

[0035] Head mounted display systems including one or more near-eye displays may often be used to present visual content to a user for use in artificial reality applications. One type of near-eye display may include an enclosure that houses components of the near-eye display or is configured to rest on the face of a user, such as for example a frame. The near-eye display may be comprised of an OLED display that may direct light from a projector to a location in front of a user's eyes. Utilizing human eye characteristics foveated rendering may be used to reduce

transmission of data through HMDs to focus detail on the foveal region of a user's eye and reduce resolution of images in the peripheral regions of the user's vision. Although, foveated rendering may reduce some transmission of data, all data from the image is assessed in the system at once requiring an abundance of memory to successfully render high resolution images, which may lead to costly HMD. Therefore, a method for reducing memory use during foveated rendering may be beneficial to reducing costs of HMD, while improving lifetime of OLED displays.

[0036] The present disclosure is generally directed to systems and methods for an improved foveated rendering system utilizing a burn-in compensation mechanism for artificial reality devices. Examples in the present disclosure may include HMDs and other artificial reality devices that may include a DDIC, a burn-in compensation mechanism, a SRAM, and a flash memory coupled to an OLED display. The OLED display may be configured to direct images from a light source to one or more eyes of a user. Although the following description discloses examples of a HMD, it may be contemplated that the examples of the present disclosure may be utilized for any system or device that comprises a display that is associated with content being displayed to a user, such as smart glasses, an augmented or virtual reality device, a desktop computer, notebook or laptop computer, netbook, a tablet computer (e.g., a smart tablet), e-book reader, television, GPS device, a camera (e.g., camera 104), personal digital assistant, handheld electronic device, cellular telephone, smartphone, smart watch, charging case, or any other suitable electronic device.

[0037] FIG. 1 illustrates an example head-mounted display (HMD) 100 associated with artificial reality content. HMD 100 may include enclosure 102 (e.g., an eyeglass frame), a camera 104, an OLED display 108, and a light source 110. The OLED display 108 may be configured to direct images to a user's eye. In some examples, head-mounted display 100 may be implemented in the form of augmented-reality glasses. Accordingly, the OLED display 108 may be at least partially transparent to visible light to allow the user to view a real-world environment through the OLED display 108. FIG. 1 also shows a representation of an eye (e.g., eye 106) that may be a real eye or an artificial eye-like object that may be for testing or using HMD 100.

[0038] The camera 104 and the light source 110 may be located on frame 102 in different positions. Camera 104 may be arranged or located along a width of a section of frame 102. In some other examples, the camera 104 may be arranged on one side of frame 102 (e.g., a side of

frame 102 nearest to an eye of a user). Alternatively, in some examples, the camera 104 may be located on OLED display 108.

[0039] FIG. 2 illustrates a block diagram of an exemplary hardware or software architecture such as, for example, user equipment (UE) 30. In some exemplary embodiments, the UE 30 may be a computer system such as for example HMD 100, smart glasses, an augmented or virtual reality device, a desktop computer, notebook or laptop computer, netbook, a tablet computer (e.g., a smart tablet), e-book reader, television, GPS device, a camera (e.g., camera 104), personal digital assistant, handheld electronic device, cellular telephone, smartphone, smart watch, charging case, or any other suitable electronic device. As shown in FIG. 2, the UE 30 (also referred to herein as node 30) may include a processor 32, non-removable memory 44, removable memory 46, a speaker or microphone 38, a keypad 40, a display, touchpad, or indicators 42, a power source 48, a global positioning system (GPS) chipset 50, and other peripherals 52. The power source 48 may be capable of receiving electric power for supplying electric power to the UE 30. For example, the power source 48 may include an alternating current to direct current (AC-to-DC) converter allowing the power source 48 to be connected or plugged to an AC electrical receptable or Universal Serial Bus (USB) port for receiving electric power. The UE 30 may also include one or more cameras 54. In an exemplary embodiment, the camera(s) 54 may be a smart camera configured to sense images or video appearing within one or more bounding boxes. The UE 30 may also include communication circuitry, such as a transceiver 34 and a transmit or receive element 36. It will be appreciated the UE 30 may include any sub-combination of the foregoing elements while remaining consistent with an embodiment.

[0040] The processor 32 may be a special purpose processor, a digital signal processor (DSP), a plurality of microprocessors, one or more microprocessors in association with a DSP core, a controller, a microcontroller, Application Specific Integrated Circuits (ASICs), Field Programmable Gate Array (FPGAs) circuits, any other type of integrated circuit (IC), a state machine, and the like. In general, the processor 32 may execute computer-executable instructions stored in the memory (e.g., memory 44 or memory 46) of the node 30 in order to perform the various required functions of the node. For example, the processor 32 may perform signal coding, data processing, power control, input or output processing, or any other functionality that enables the node 30 to operate in a wireless or wired environment. The

processor 32 may run application-layer programs (e.g., browsers) or radio access-layer (RAN) programs or other communications programs. The processor 32 may also perform security operations such as authentication, security key agreement, or cryptographic operations, such as at the access-layer and/or application layer for example.

[0041] The processor 32 is coupled to its communication circuitry (e.g., transceiver 34 and transmit/receive element 36). The processor 32, through the execution of computer executable instructions, may control the communication circuitry in order to cause the node 30 to communicate with other nodes via the network to which it is connected.

[0042] The transmit/receive element 36 may be configured to transmit signals to, or receive signals from, other nodes or networking equipment. For example, in an exemplary embodiment, the transmit/receive element 36 may be an antenna configured to transmit and/or receive radio frequency (RF) signals. The transmit/receive element 36 may support various networks and air interfaces, such as wireless local area network (WLAN), wireless personal area network (WPAN), cellular, and the like. In yet another exemplary embodiment, the transmit/receive element 36 may be configured to transmit and/or receive both RF and light signals. It will be appreciated that the transmit/receive element 36 may be configured to transmit and/or receive any combination of wireless or wired signals. The transmit/receive element 36 may also be configured to connect the UE 30 to an external communications network, such as network 12, to enable the UE 30 to communicate with other nodes (e.g., other UEs 30, network device 160, etc.) of the network.

[0043] The transceiver 34 may be configured to modulate the signals that are to be transmitted by the transmit/receive element 36 and to demodulate the signals that are received by the transmit/receive element 36. As noted above, the node 30 may have multi-mode capabilities. Thus, the transceiver 34 may include multiple transceivers for enabling the node 30 to communicate via multiple radio access technologies (RATs), such as universal terrestrial radio access (UTRA) and Institute of Electrical and Electronics Engineers (IEEE 802.11), for example.

[0044] The processor 32 may access information from, and store data in, any type of suitable memory, such as the non-removable memory 44 and/or the removable memory 46. For example, the processor 32 may store session context in its memory, as described above. The non-removable memory 44 may include RAM, SRAM, ROM, a hard disk, or any other type of memory storage device. The removable memory 46 may include a subscriber identity module

(SIM) card, a memory stick, a secure digital (SD) memory card, and the like. In other exemplary embodiments, the processor 32 may access information from, and store data in, memory that is not physically located on the node 30, such as on a server or a home computer.

[0045] The processor 32 may receive power from the power source 48, and may be configured to distribute and/or control the power to the other components in the node 30. The power source 48 may be any suitable device for powering the node 30. For example, the power source 48 may include one or more dry cell batteries (e.g., nickel-cadmium (NiCd), nickel-zinc (NiZn), nickel metal hydride (NiMH), lithium-ion (Li-ion), etc.), solar cells, fuel cells, and the like. The processor 32 may also be coupled to the GPS chipset 50, which may be configured to provide location information (e.g., longitude and latitude) regarding the current location of the node 30. It will be appreciated that the node 30 may acquire location information by way of any suitable location-determination method while remaining consistent with an exemplary embodiment.

[0046] FIG. 3 illustrates example areas captured via foveated rendering. The HMD system 100 of FIG. 1 may include foveated rendering to mitigate or reduce data transmission through the system utilizing the fact that the eye may capture views of images or the environment of up 110˚ eccentrically with varying detail depending on the degree from the central axis of the eye. In such examples, an image (e.g., frames of video, video, or etc.) captured via foveated rendering may experience some compensation, reduced resolution, or reduced rendering quality in peripheral view or region of an eye (e.g., eye 106) of a user, corresponding to 10˚ to 110˚ eccentrically. Whereas, in the central region of the eye associated with the fovea (area of the eye that may be more capable for detailed vision than peripheral vision) the image may have a greater or increased resolution.

[0047] The fovea or fovea centralis may be located in the center of the macula lutea, a small, flat spot located exactly in the center of the posterior portion of the retina, which is located centrally to the eye. The macula lutea portion of the retina may be responsible for fine detail in vision. This portion of the eye spans the central 18˚ around the gaze point, or 9˚ eccentricity (the angular distance away from the center of gaze). The fine detail of vision is processed by cones, found mainly in the fovea, and at eccentricities past 9˚ there may be a rapid fall off of cone density. The human eye may be capable of capturing a view of the environment up to 100˚ eccentrically. Furthermore, the central visual field ends at 30˚ eccentricity with 10˚ to 30˚ largely

considered near peripheral, as cone density falls off, and may be considered an overlap of the peripheral view and the foveal view (e.g., a blend). Although, the central visual field has less cones than the foveal region, this visual region may still capture some detail, therefore, in many foveated rendering systems this region may have reduced resolution than the foveal region while retaining more resolution than the outer portion of the peripheral region, 30˚ to 110˚ eccentrically. In areas where peripheral vision is within 100˚ to 110˚ eccentrically, many foveated rendering systems do not use this degree of vision as outer peripheral vision does not contain detailed visual characteristics nor is vision great in that area.

[0048] FIG. 4 is an block diagram illustrating an example data pipeline 400 associated with a burn-in compensation mechanism. Data pipeline 400 may include an application processor (AP) 402, a processor (display driver integrated circuit (DDIC) 410), a first memory (e.g., SRAM 430), a second memory (e.g., flash memory 440), a simulator 460, and a display panel 450. The display panel 450 may include a plurality of pixels. A plurality of data lines and a plurality of scan lines may be formed in the display panel 450. A plurality of pixels may be formed in crossing areas of the data lines and the scan lines. In some example embodiments, each of the pixels may include a pixel circuit, a driving transistor, and an organic light emitting diode (OLED). In this case, the pixel circuit may transfer a data signal provided through the data line to the driving transistor in response to an estimated block determined via processor (e.g., DDIC 410). The driving transistor may control a driving current flowing through the OLED based on the data signal. The OLED may emit light based on the driving current. OLED included in each of the pixels may be degraded, and luminance of the pixel may decrease, as an accumulation driving time and an accumulation driving amount of the pixel increases. AP 402 may receive data via an application on a user device and transmit the received data (i.e., image data, video data, or any other suitable data type) to the processor (e.g., DDIC 410). AP 402 may be a system on a chip designed to support applications running in a devices operating system environment. In some examples, AP 402 in mobile devices may be independent from other specialized processors in the same mobile device, such as a phone's baseband (wireless communications) processor. Data transmitted or transferred to the processor (e.g., DDIC 410) may undergo a series of processes within DDIC 410. Data in the DDIC 410 may undergo pre-processing 411, burn-in compensation 420, post-processing 415, and digital-to-analog conversion (DAC) 416. In some examples, data sent and received via AP 402 may be in a digital format associated with images,

videos, or any other digital means of data. The digital data may undergo pre-processing 411, which may include, in some examples, algorithms such as edge enhancement, decompression, or etc. to formulate the digital data into a more calculable form. After pre-processing 411, the digital data (e.g., video data) may undergo burn-compensation 420.

[0049] Burn in compensation may include accumulation 412, SRAM 430, offset & gain 413, and compensation 414. Accumulation 412 may convert video data to stress data, for each pixel of the video data, using look up tables (LUT). LUTs may be stored within any memory associated with the pipeline 400. The stress data may be calculated based on luminance information, load information, temperature information, information of a degree of the stress per each of grayscales, etc. as well as based on the video or image data. The stress data may be used later in association with compensation 414 to compensate the decreased luminance of each pixel. Once video data converted to stress data, via accumulation 412, the data may be stored or loaded to SRAM 430 of DDIC 410, where SRAM may communicate with flash memory 440 the accumulated stress data. In some examples, SRAM 430 (e.g., first memory) may be electronically connected to flash memory 440 (e.g., second memory), The flash memory 440 may receive simulated block sizes via a simulator 460 and communicate the block sizes to DDIC 410 via SRAM 430. Flash memory 440 may store stress data determined via accumulation 412.

[0050] The simulator 460 (e.g., burn-in compensation simulator) may be any device that is connected, via any suitable connection (e.g., BLUETOOTH, wi-fi, or etc.) to the burn-in compensation mechanism. Simulator 460 may divide the display panel 450 into a plurality of blocks, associated with the compensation 414 of the pixels included in each of the blocks, where the blocks are estimated using the equation: $\frac{L(T)}{L(\theta)} = \exp\left[-\left(A^n x \frac{T}{t_i}\right)^{\beta}\right]$ corresponding to a decay curve of OLED lifetime, where L(T) is the brightness at time T, L(θ) is initial brightness, A is luminance delta ratio, n is the acceleration factor of luminance, T is time, t_i is the time constant, and β is shape of the decay curve. In some examples, look up tables determined via simulator 460 may be stored in flash memory 440 or other non-volatile memory for selecting offset or gain of compensation. Once block sizing is simulated based on stress data associated with the video data, the DDIC may begin offset & gain 413.

[0051] Offset & gain 413 may comprise LUTs to convert stress data to offset, compensation data, considering scale factor gain, e.g., temperature, level of luminance, or any other

characteristic of the stress data associated with the video data. Following offset & gain 413, the video data now accompanied with offset may undergo compensation 414. The video data may then undergo post-processing 415, which may in some examples comprise a gamma table to convert gray level (e.g., 8 bit, 0 - 255) associated with the video data, offset, and compensation data to gamma code matching voltage level for digital to analog convertor (DAC) to drive panel blocking. Then the video data, offset, and compensation (also referred to as compensated video data) data may be converted to analog data via DAC 416. Once the data is converted to analog data the compensated video data may be presented to a user via display panel 450.

[0052] FIG. 5 is a block diagram illustrating a head mounted display system 500 according to an example. The system 500 may include a DDIC 510, a display panel 550, and a second memory (e.g., flash memory 540). The system 500 may be connected via any suitable connection to a simulator 560 to simulate blocks associated with stress data representing video data. DDIC 510 may further include a first memory (e.g., SRAM 530) and a burn-in compensation mechanism 520. DDIC 510 may receive video data and be configured to calculate stress and alter received video data based on the stress and location of the pixels in relation to the fovea of a user. DDIC 510 may communicate via SRAM 530 and flash memory 540 with simulator 560 to create blocks associated with the stress data and foveal view corresponding to a user. Blocking sizes may be larger in regions outside of the foveal view of a user, where these larger blocks may experience compensation as the user visual acuity may not notice decrease image properties in these areas. In some areas flash memory 540 may include a look up table associated with the OLED display lifetime curve used to simulate blocks, via simulator 560. The look up tables may store data and blocking configurations for certain positioning of the pixels and their relative stress data. Once the blocking for the video data has been determined the video data may undergo more processes within DDIC 510 such as compensation in areas outside of the foveal view or the outer portions of the video data, the video data may be post-processed, and converted to an analog video signal to allow viewing to a user via display panel 550.

[0053] In some examples DDIC 510, may further include a calculator. The calculator may calculate the stress data of the pixels included in each of the blocks of FIG. 6A, FIG. 6B and FIG. 6C. The calculator may calculate the stress data based on the video or image data. Further, the calculator may calculate the stress data based on luminance information, load information, temperature information, information of a degree of the stress per each of grayscales, etc. as well

as based on the video or image data. In some examples, the calculator may calculate an average value of the stress values that represents a degradation degree of the pixels included in the estimated block (e.g., FIGS. 6A, 6B, 6C) in every frame as the stress data. In other examples, the calculator may sequentially output a stress value that represents a degradation degree of one pixel of the pixels included in the estimated block as the stress data. For example, the calculator may sequentially output the degradation degree of the pixel included in the block of FIG. 6B as the stress data during frames when the unit block includes 16x16 pixels.

[0054] The first memory (e.g., SRAM 530) may receive the stress data from the calculator and may store the stress data by block in conjunction with the second memory (e.g., flash memory 540). The second memory 540 may store the accumulated stress data by adding the stress data provided from the calculator. For example, the second memory 540 may be a non-volatile memory device. The second memory 540 may store each of the accumulated stress data of the blocks of FIG. 6A, FIG. 6B, and FIG. 6C.

[0055] The DDIC 510 may compensate the video or image data based on the accumulated stress data. The DDIC may determine a degradation amount and may compensate the image or video data to generate compensation data based on the degradation amount. The degradation amount corresponds to the degradation of the blocks which may be different from each other based on their pixel size and the accumulate stress data of the blocks. The DDIC may generate compensation data where the image or video data is compensated by adjusting the degradation amount based on each of the accumulated stress data to the pixels included in each of the blocks (i.e., blocks of FIG. 6A, FIG. 6B, FIG. 6C and FIG. 7A, FIG. 7B, FIG. 7C). The DDIC may also generate a data signal based off the compensation data and may provide the data signal to the pixels. In some examples, the DDIC may include a timing controller. In such examples the DDIC may generate the data signal corresponding to the compensation data in response to a control signal provided from the timing controller and may output the data signal to the display panel 550.

[0056] FIG. 6A illustrates conventional blocking of burn-in compensation mechanisms. In conventional systems blocking, DDIC 510 may block the entire image, frames of images, or video in equal sized blocks. Although there may be blocking, the video data for each pixel within each block is still assessed and presented to the user at optimal quality, including areas outside of foveal region of view. FIG. 6B and FIG. 6C illustrates exemplary blocking of a display panel in

accordance with a burn-in compensation mechanism of the present disclosure. Blocking in the burn-in compensation mechanism may be adjusted based on the area determined by a user device, via eye tracking, to be where the users gaze is or where their fovea is positioned. For example, in FIG. 6B and FIG. 6C a user may be focused on the center of a display (e.g., display panel 550). Due to the positioning of the fovea, simulated blocking may be smaller in the area associated with the foveal view, where smaller blocking may be associated with areas where video image data may be enhanced for optimal resolution for a user to view and video data may not experience compensation. Blocking outside of the foveal view associated with the eyes of a user may be larger than the blocking within the foveal view of the user, where larger blocking may be associated with compensation of video image data to a lower resolution in areas where the human eye may be unable to determine or discern lower resolution. Blocking determined by simulator 560 may be of any size, pixel size, or any suitable size relative to the size of a display panel (e.g., display panel 550). The blocks of FIGS. 7A, 7B, and 7C may include “M” x “N” pixels, where the M and N are integers that are greater than or equal to 1.

[0057] Referring to FIGS. 7A, 7B, and 7C the burn-in compensation simulator may divide a display panel (e.g., display panel 550) into a plurality blocks depending on calculated stress data associated with characteristics of the video data and determined foveal view, associated with a user. The blocks of FIGS. 6A, 6B, 6C may include “M” x “N” pixels, where the M and N are integers that are greater than or equal to 1. For example, as shown in FIG. 7A the block may include 8x8 pixels. The simulator 560 may move the block of FIG. 7A in the path to the first memory (e.g., SRAM 530) via an electronic communication with the second memory (e.g., flash memory 540) in response to an accumulate stress data associated with video data. Once the stress data is incorporated with the blocking from the simulator 560, DDIC 510 may further compensate the video data in areas outside of the foveal region, where the larger the blocking more compensation may occur.

[0058] FIGS. 8A, 8B, 8C, and 8D illustrates burn-in compensation associated with image data 801. FIG. 8A illustrates a static image to be compensated via burn in compensation mechanism. In the case of static images, 8x8 compensation (e.g., FIG. 8B) may not be suitable depending on the image, whereas in real-time or live video an environment shown in FIG. 8B input video data may change continuously. Thus, 8x8 compensation (FIG. 8B) may have suitable performance, where 16x16 compensation (FIG. 8C) and 32x32 compensation (FIG. 8D) have

better performance than static image input due to the changing stressed pixels. In this example, foveated burn-in compensation is more effective because it may be difficult for a user to distinguish the luminance difference between pixels.

[0059] FIGS. 9A and 9B illustrate exemplary compensation of blended area block, in accordance with an example. In this example, the foveal region or area 902 may be 8x8 pixels, whereas the peripheral region or area 904 may be 16x16 pixels. Image stick in the peripheral region 904 may be apparent if data from AP (e.g., AP 402) is a static image, due to specific pixel degradation in static images result in worse or more image stick. In real time situations or video data is inputted into the burn-in compensation mechanism, meaning the input image changes continuously. FIG. 9B illustrates this real time situation. In this case, large block size, lower compensation performance, is enough to compensate burn-in of peripheral region in 9B.

[0060] FIG. 10 illustrates parameter chart of blocks associated with areas of views captured via foveated rendering, in accordance with an example. DDIC (e.g., DDIC 410) may support diverse resolution and foveal/blend area. DDIC may change block size of burn-compensation in response to the parameters illustrated.

[0061] FIG. 11 illustrates an exemplary burn-in compensation mechanism block size of each rendered area, in accordance with an example. Foveal area 1103 may be the most important feature of the eye, where the human eye is the most sensitive to light, change, or etc. Due to the properties of the eye, a smaller block size and a high compensation performance may be used to provide a user with optimal resolution for viewing. The Peripheral area 1101 may have a larger block size. If the difference between foveal region 1103 and peripheral 1101is large, the device may provide the user with undesirable or unnatural pictures. Therefore, the blend area 1102 may be needed for smoothing the edge of each area.

[0062] FIG. 12 is a flowchart illustrating a method of burn-in compensation associated with image or video data. A method 1200 of burn-in compensation associated with image or video data may include receiving video data, via application processor (e.g., AP 402); pre-processing (e.g., pre-processing 411) the video data; calculating stress data associated with the video data; dividing the display panel into a plurality of blocks, which may correspond to stress data and areas determined by foveated rendering (step 1202); generating compensation data and compensating video data in areas outside of foveal view; converting video data into an analog

video signal to enable a user to view the video (step 1204); and generating compensation data (step 1206).

[0063] At step 1202, a device (e.g., HMD 100) may receive video data via AP 402, video data may be pre-processed, which may refer to manipulation or removal of data before it is used, in order to clean or enhance the received data to a calculable form, suppressing distortions, noise, or enhancing some image features important for further processing the of received data. Pre-processing may include many techniques such as geometric transformation of images (e.g., rotation scaling, translation), image data resizing, converting image to grayscale, image augmentation, or any technique suitable for pre-processing of data within a system or device.

[0064] At step 1204, a device (e.g., HMD 100) may calculate stress data associated with each pixel of the video data, store stress data within a first memory (e.g., SRAM 430). At step 1206, stored stress data may be transmitted via any suitable communication link to a secondary memory (e.g., flash memory 440), where the secondary memory may communicate with a burn-in simulator (e.g., simulator 460) to divide the display panel 550 into a plurality of blocks estimated via a decay curve of OLED lifetime. Each of the blocks estimated may include a plurality of pixels comprised of original image. In some examples simulator 460 may further comprise data associated with eye tracking to determine foveal view associated with a user's eye. In such examples, estimated blocking may be altered to block for optimal view in foveal view of the user's eye. In some examples, a device (e.g., HMD 100) may calculate an average value of the stress values that represents a degradation degree of the pixels included in the block in every frame and may output the average value as the stress data. In another example, the device may sequentially output the stress value that represents the degradation degree of one respective block and the pixels included in that block as the stress data in every frame of the data. The device may generate accumulated stress by adding up, accumulating, or summing the stress data.

[0065] At step 1208, HMD 100 may compensate the video data based on the blocking determined via simulator 560, and accumulated stress data. A device (e.g., HMD 100) may determine the degree of compensation, reduction of resolution, or reduction of quality based on the degradation amount determined. As a result, display quality may vary based on the blocks estimated and the degradation amount determined based on the pixel stress. At step 1210, compensated video data may be converted to an analog video signal for display, via display panel (e.g., display panel 450), to a user of the device (e.g., HMD 100). In some examples, in

addition to the HMD 100, the display 108, the display panel 450, or the display 550 may perform the steps of the method 1200.

[0066] Display quality may be reduced in areas outside of the foveal region, where stress of each block may be determined sequentially, separately, or at different times thus greatly reducing the need for a large memory or SRAM 530 in conventional systems due to only one block being controlled or assessed at a time. Also, due to the functional qualities of SRAM 520 data may be readily overwritten for the next block, whereas flash memory 540 or second memory may retain important stress information for a previous block stress calculation. The configuration of the memories may allow for a reduced flash memory 540 size as there may be less data assessed at once. Therefore, reducing the size of both the first memory 530 and the second memory 540 may reduce costs in HMDs.

[0067] The foregoing description of the examples has been presented for the purpose of illustration; it is not intended to be exhaustive or to limit the patent rights to the precise forms disclosed. Persons skilled in the relevant art may appreciate that many modifications and variations are possible in light of the above disclosure.

[0068] Some portions of this description describe the examples in terms of applications and symbolic representations of operations on information. These application descriptions and representations are commonly used by those skilled in the data processing arts to convey the substance of their work effectively to others skilled in the art. These operations, while described functionally, computationally, or logically, are understood to be implemented by computer programs or equivalent electrical circuits, microcode, or the like. Furthermore, it has also proven convenient at times, to refer to these arrangements of operations as modules, without loss of generality. The described operations and their associated modules may be embodied in software, firmware, hardware, or any combinations thereof.

[0069] Any of the steps, operations, or processes described herein may be performed or implemented with one or more hardware or software modules, alone or in combination with other devices. In one embodiment, a software module is implemented with a computer program product comprising a computer-readable medium containing computer program code, which may be executed by a computer processor for performing any or all of the steps, operations, or processes described.

[0070] Examples also may relate to an apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a computing device selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a non-transitory, tangible computer readable storage medium, or any type of media suitable for storing electronic instructions, which may be coupled to a computer system bus. Furthermore, any computing systems referred to in the specification may include a single processor or may be architectures employing multiple processor designs for increased computing capability.

[0071] Examples also may relate to a product that is produced by a computing process described herein. Such a product may comprise information resulting from a computing process, where the information is stored on a non-transitory, tangible computer readable storage medium and may include any embodiment of a computer program product or other data combination described herein.

[0072] The language used in the specification has been principally selected for readability and instructional purposes, and it may not have been selected to delineate or circumscribe the inventive subject matter. It is therefore intended that the scope of the patent rights be limited not by this detailed description, but rather by any claims that issue on an application based hereon. Accordingly, the disclosure of the examples is intended to be illustrative, but not limiting, of the scope of the patent rights, which is set forth in the following claims.

[0073] Herein, “or” is inclusive and not exclusive, unless expressly indicated otherwise or indicated otherwise by context. Therefore, herein, “A or B” means “A, B, or both,” unless expressly indicated otherwise or indicated otherwise by context. Moreover, “and” is both joint and several, unless expressly indicated otherwise or indicated otherwise by context. Therefore, herein, “A and B” means “A and B, jointly or severally,” unless expressly indicated otherwise or indicated otherwise by context.

WHAT IS CLAIMED:

1. A device comprising:

an application processor configured to generate a data signal;

a second processor configured to determine, via a decay curve, a plurality of simulated blocks;

a first processor configured to compensate a data signal, wherein the processor is further configured to:

calculate stress data separately for the pixels associated with the data signal;

degrade image data to generate compensation data based on accumulated stress data;

control the transmission of data from the first processor to the display panel; and

communicate with a first memory, wherein:

the first memory is configured to communicate with a second memory;

the second memory configured to store stress data and communicate with the simulator; and the second memory stores the accumulated stress data of the estimated blocks.

2. The device of claim 1, wherein the device comprises a head-mounted display.

3. The device of claim 1, wherein the device further comprises a display or a display panel comprising a plurality of pixels.

4. A method comprising:

receiving a data signal via an application processor;

calculating a stress value for a plurality of pixels associated with the data signal;

storing the stress value in a second memory;

dividing a display panel comprising a plurality of pixels into one or more simulated blocks comprising pixels associated with stress data of an original image;

determining an accumulated stress data separately for the simulated;

generating an accumulated stress data based on an accumulation of stress values associated with the simulated blocks;

degrading data associated with the original image to generate compensation data based on the accumulated stress data; and converting compensation data to an analog signal to display to a user.

ABSTRACT OF THE DISCLOSURE

Systems, methods, and devices for compensating image(s) or video(s) data are provided. A device may divide a display panel including a plurality of pixels into one or more estimated blocks including pixels associated with an original image. The device may also calculate stress data separately for the estimated blocks by calculating a stress value of the pixels associated with the estimated block. The device may also generate an accumulated stress data based on an accumulation of stress data. The device may also degrade data associated with the original image to generate compensation data based on the accumulated stress data.

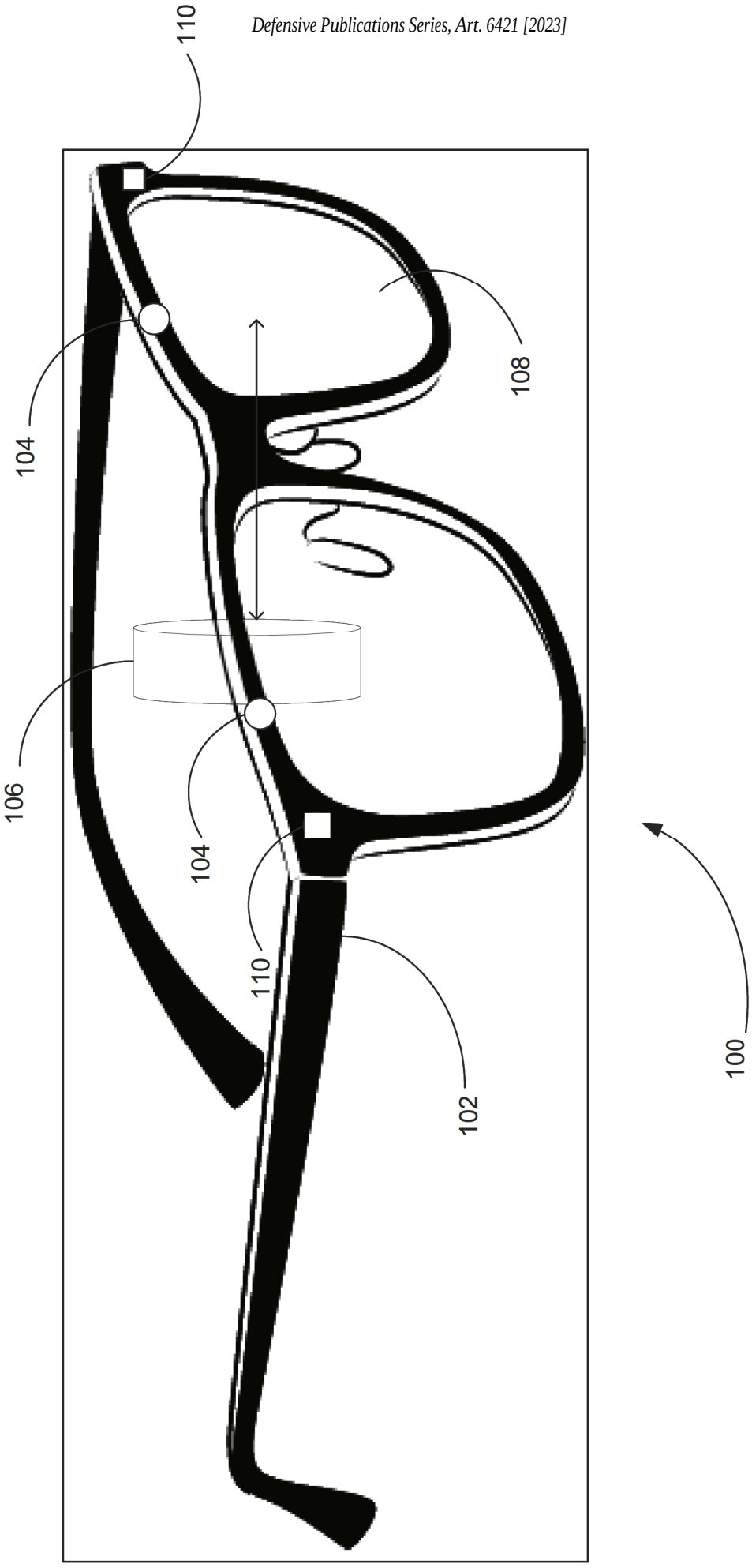


FIG. 1

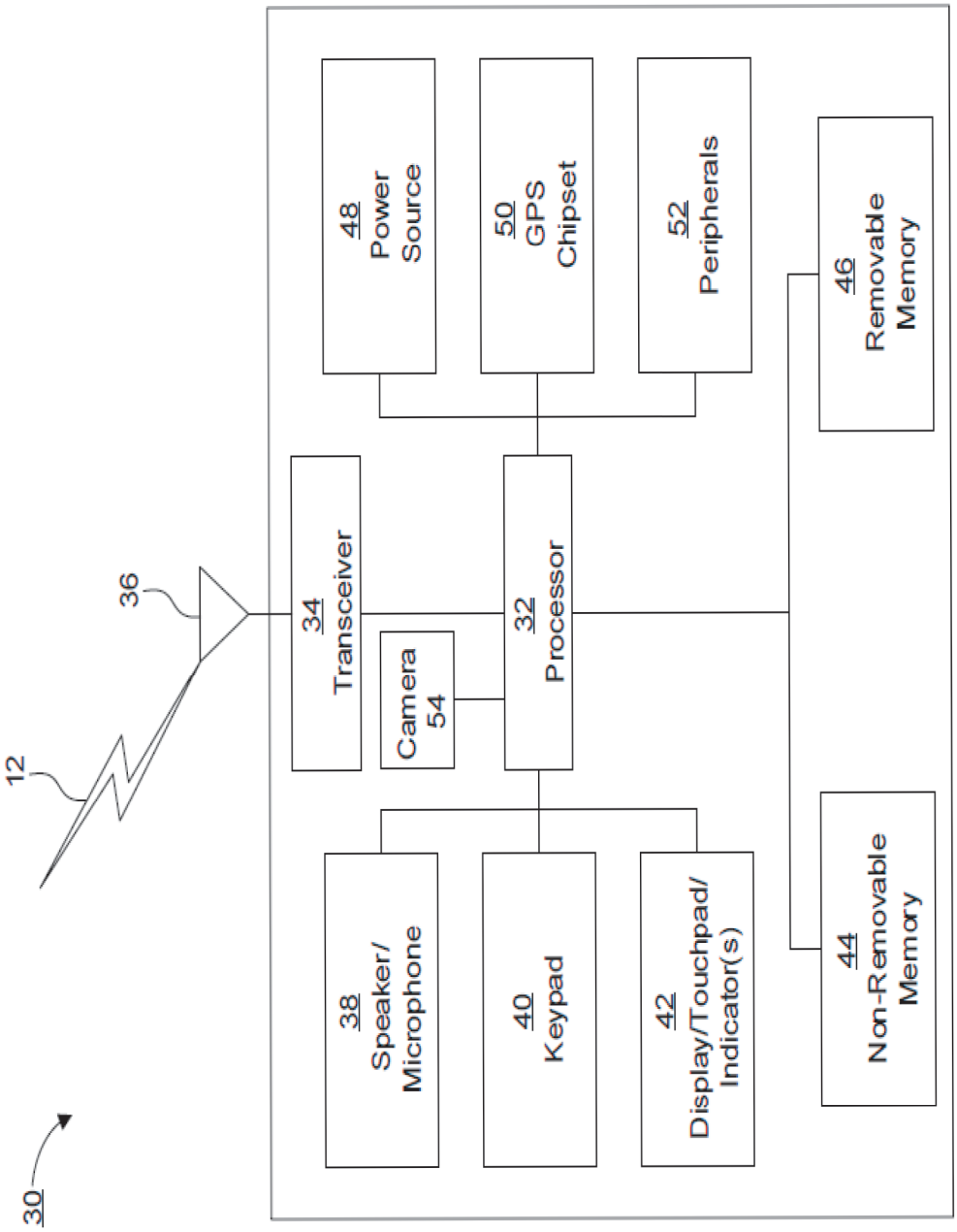

30
12
36
34 Transceiver
Camera 54
32 Processor
48 Power Source
50 GPS Chipset
52 Peripherals
46 Removable Memory
38 Speaker/ Microphone
40 Keypad
42 Display/Touchpad/ Indicator(s)
44 Non-Removable Memory

FIG. 2

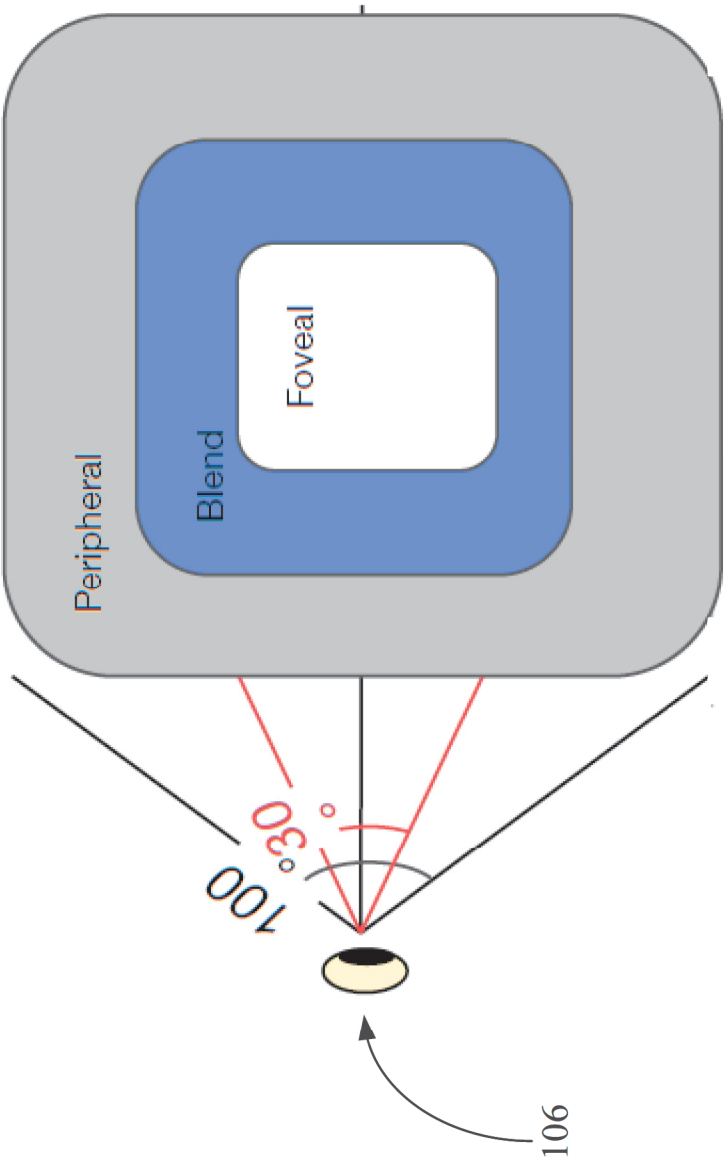


FIG. 3

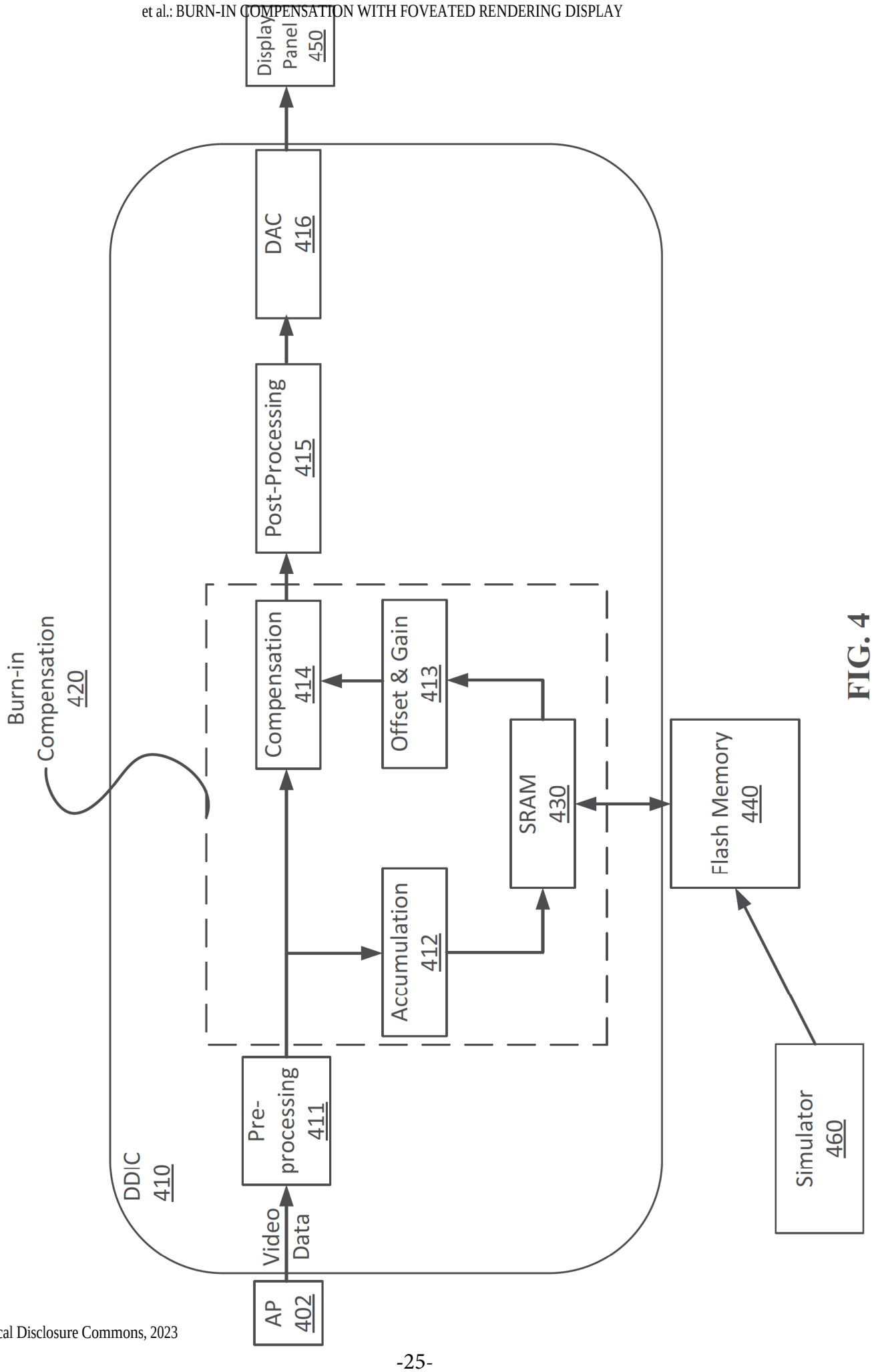

AP
402
Video Data
DDIC
410
Pre-processing
411
Burn-in Compensation
420
Compensation
414
Offset & Gain
413
Accumulation
412
SRAM
430
Flash Memory
440
Simulator
460
Post-Processing
415
DAC
416
Display Panel
450

FIG. 4

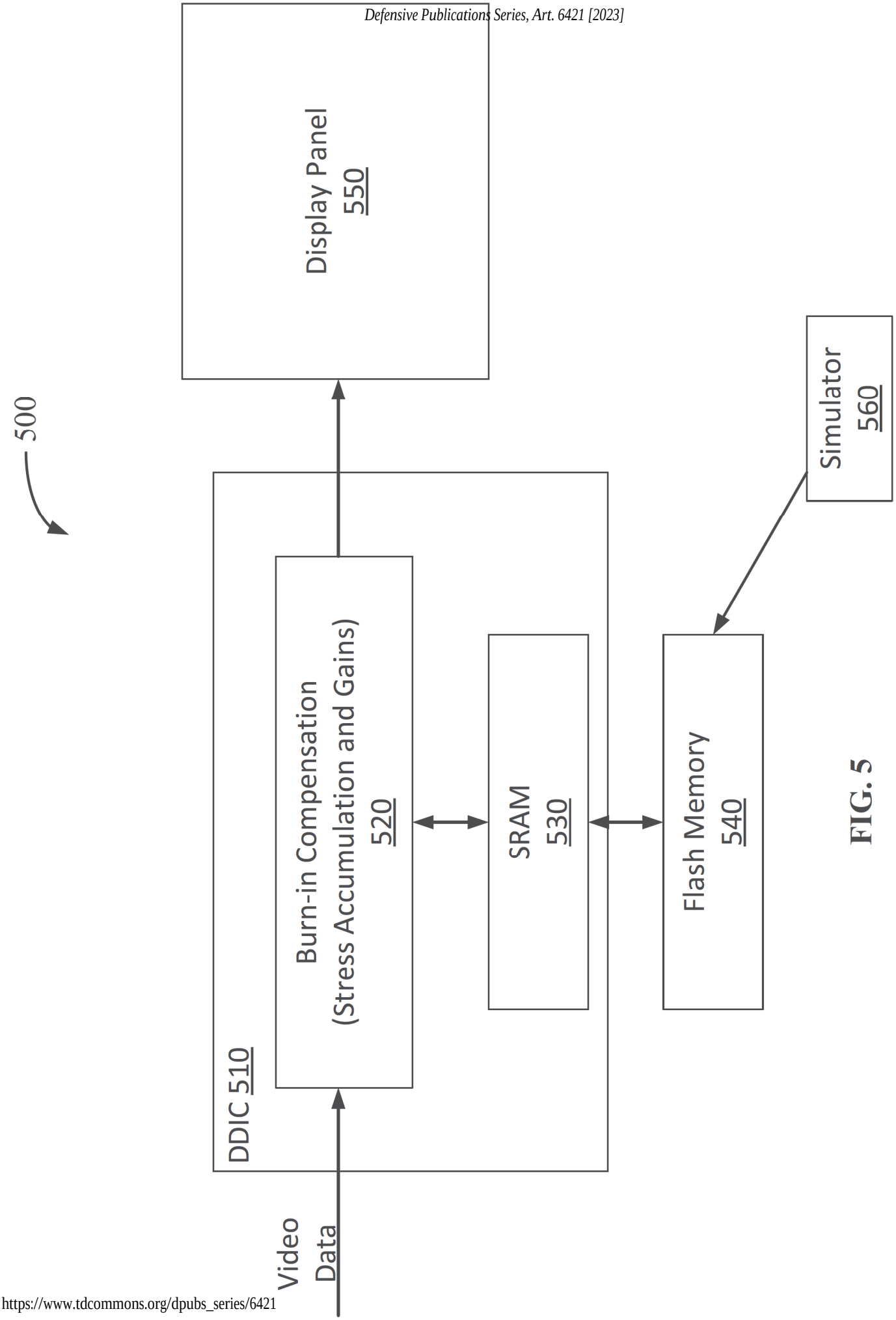

500
Display Panel
550
Simulator
560
DDIC 510
Burn-in Compensation
(Stress Accumulation and Gains)
520
SRAM
530
Flash Memory
540
Video
Data

FIG. 5

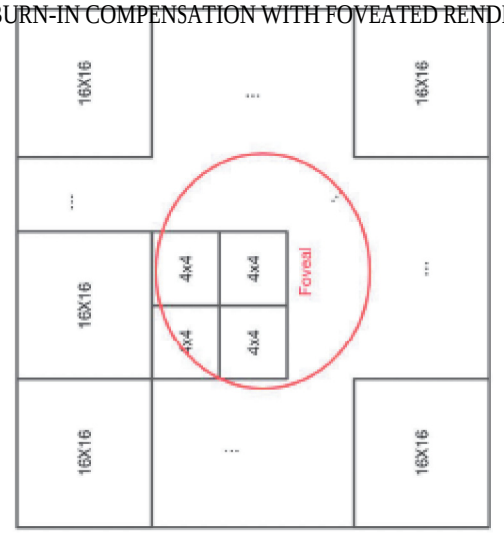


FIG. 6C

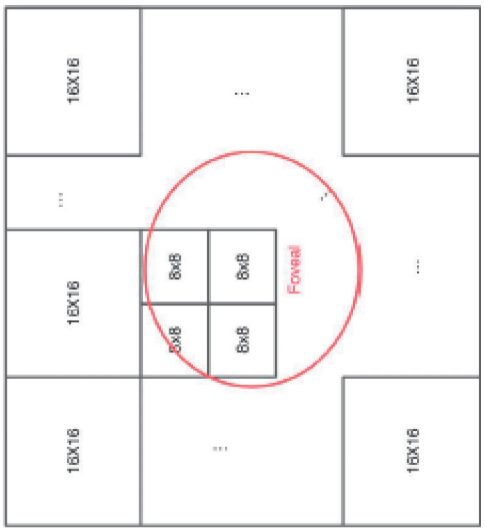


FIG. 6B

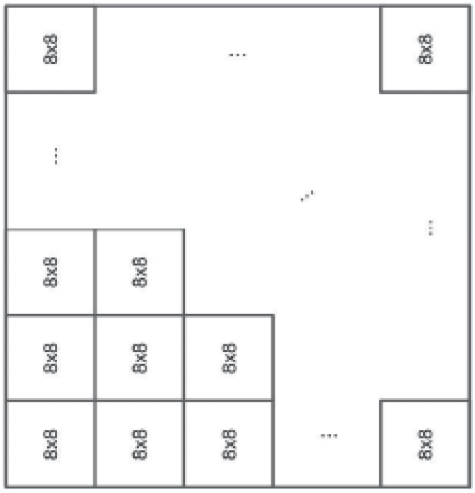


FIG. 6A

< 32x32 Compensation >

FIG. 7C

< 16x16 Compensation >

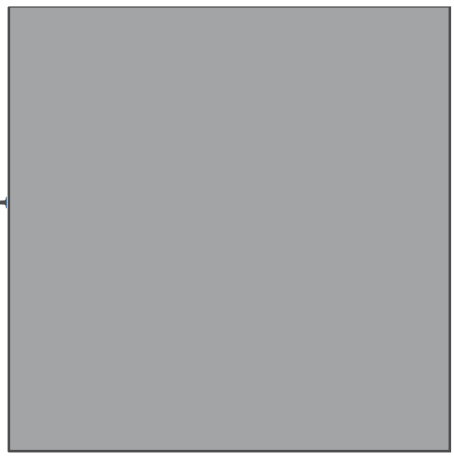


FIG. 7B

< 8x8 Compensation >

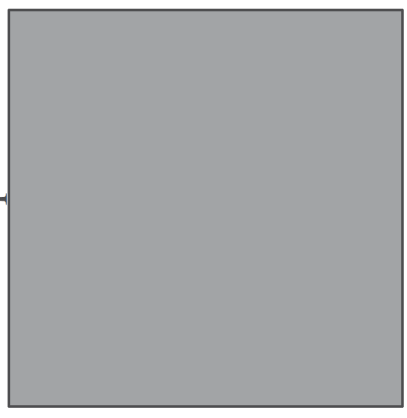


FIG. 7A

< Input – Constant Image >

FIG. 8A

< 8x8 Compensation >

FIG. 8B

< 16 x16 Compensation >

FIG. 8C

< 32 x 32 Compensation

FIG. 8D

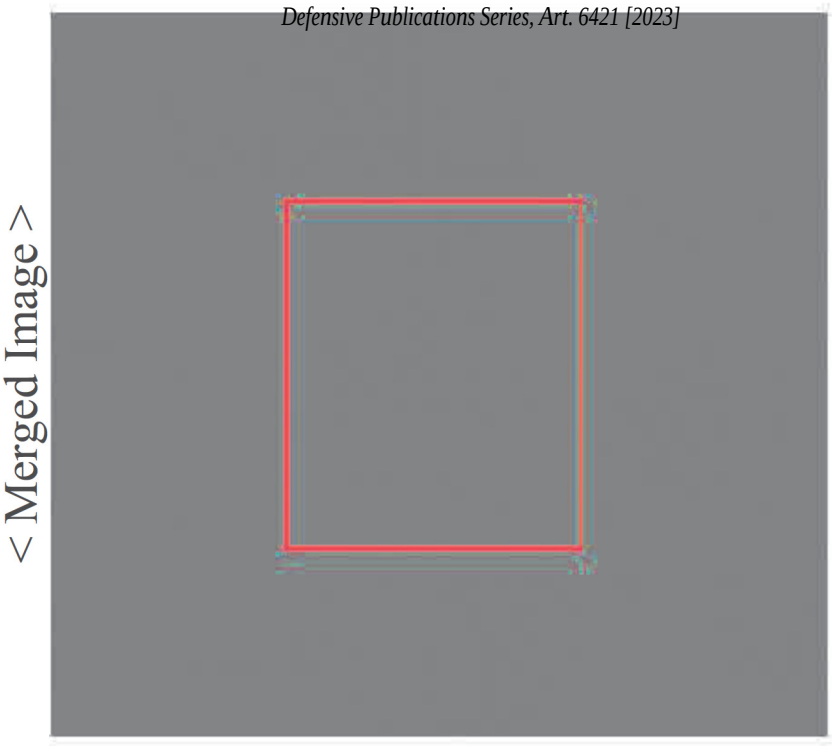


FIG. 9B

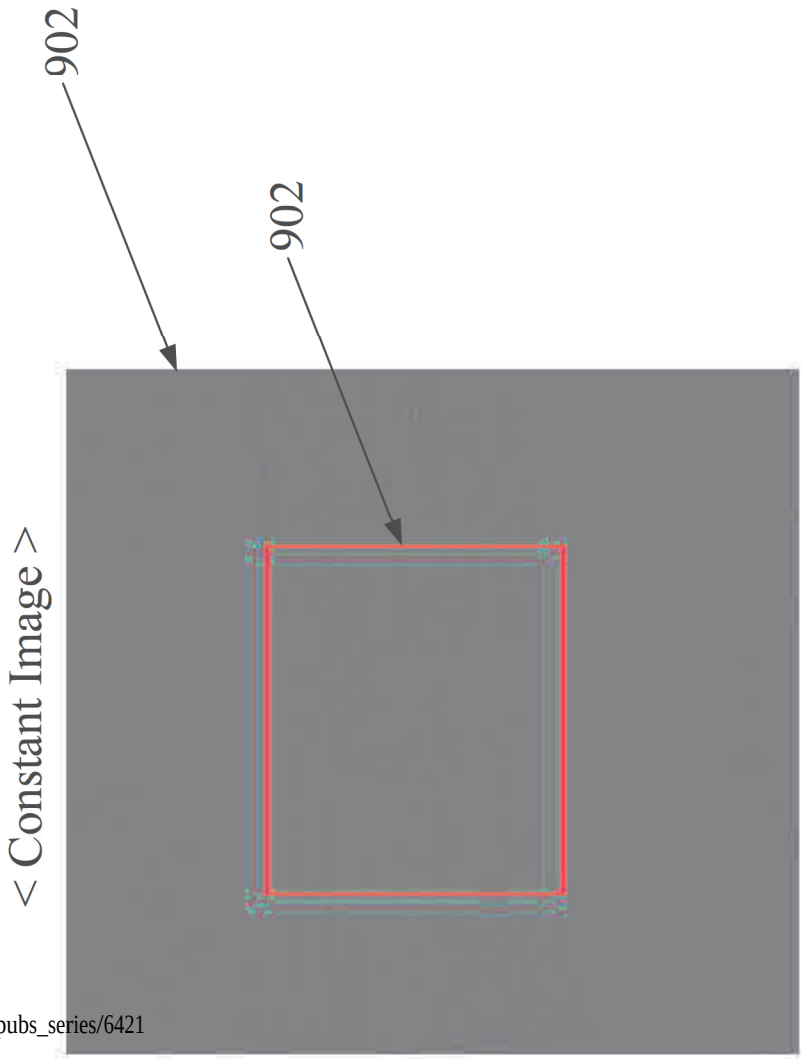
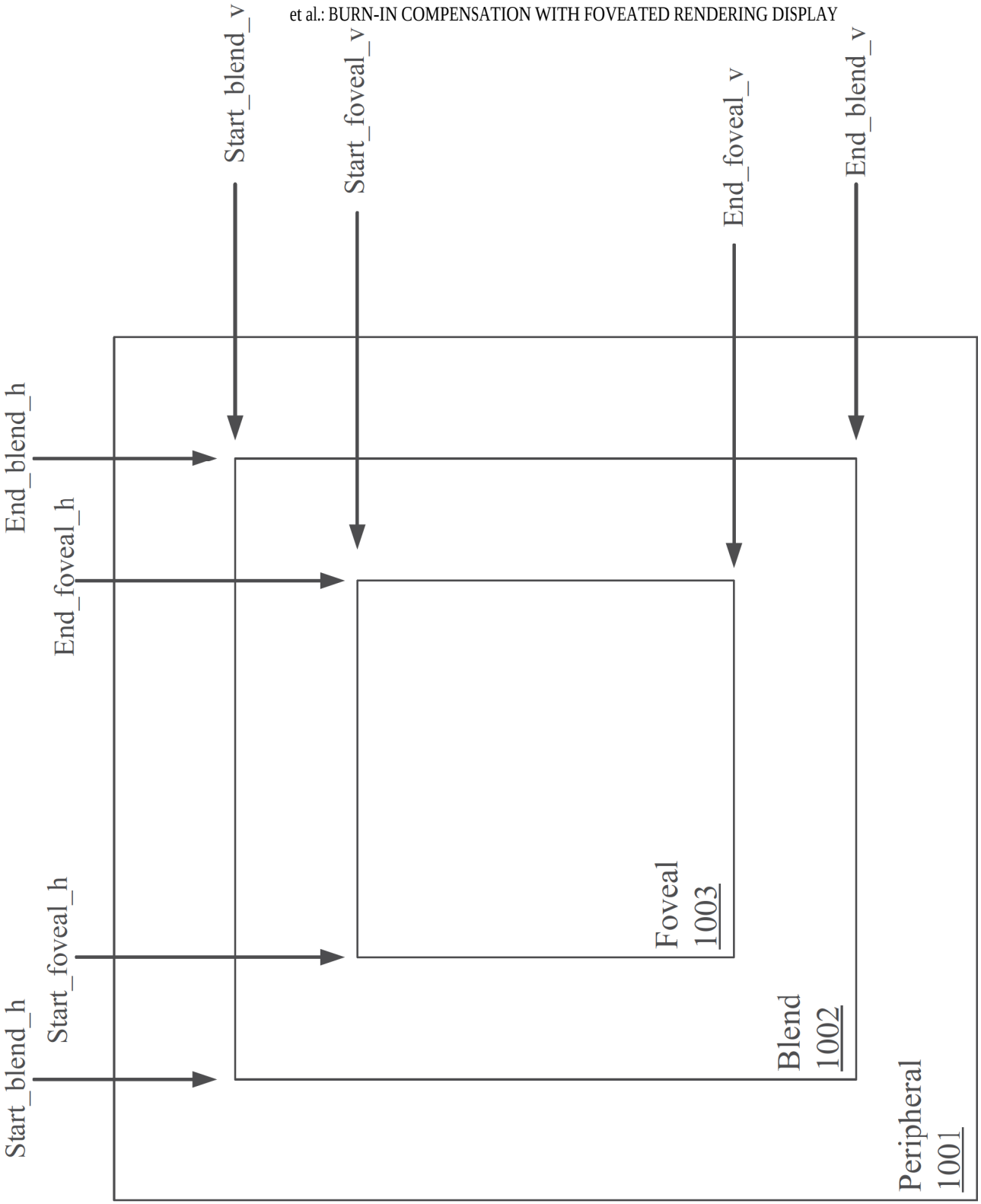


FIG. 9A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Start_foveal_v
End_foveal_v
End_blend_v
End_blend_h
End_foveal_h
Start_foveal_h
Start_blend_h
Foveal
1003
Blend
1002
Peripheral
1001

FIG. 10

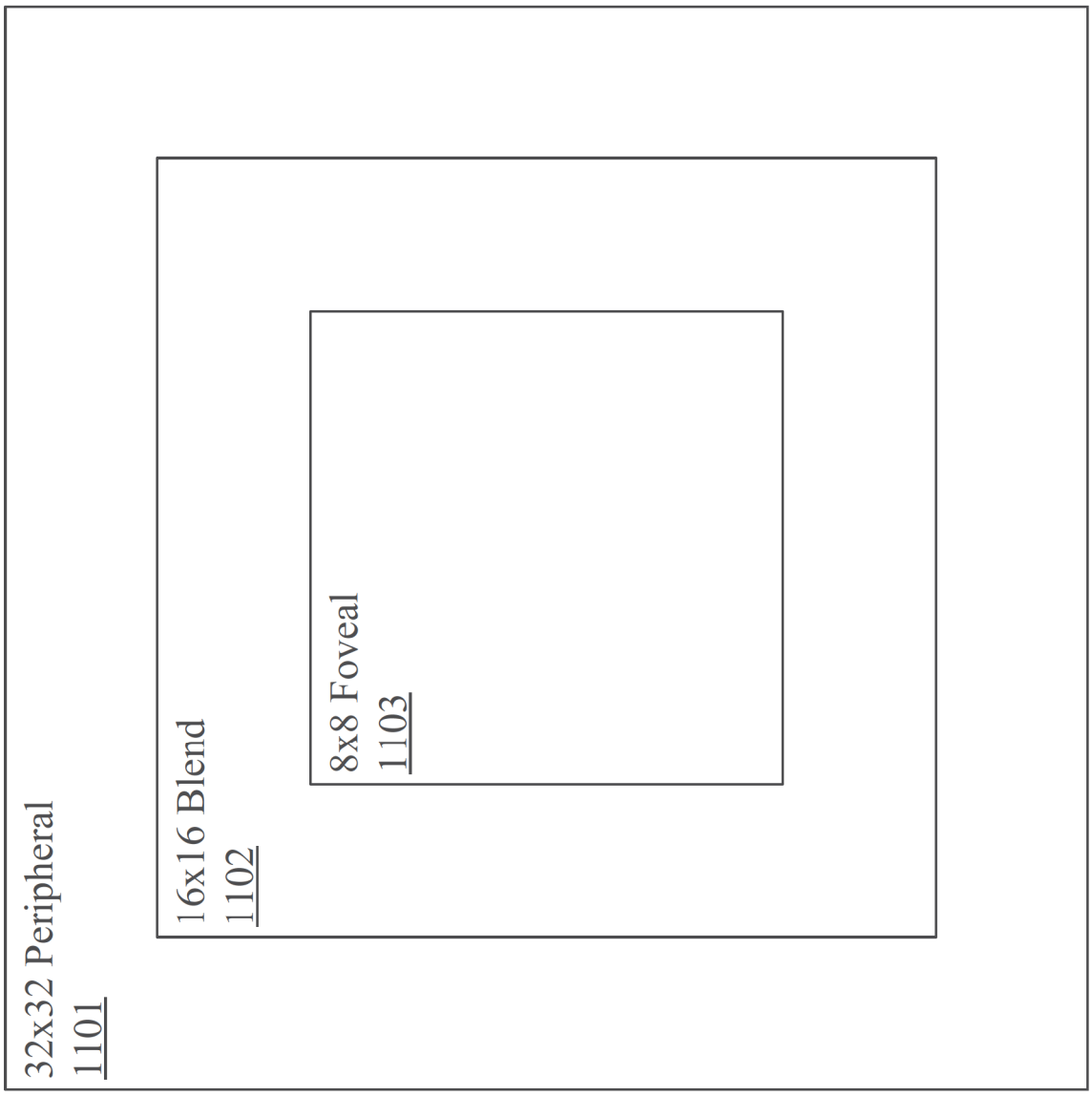

FIG. 11

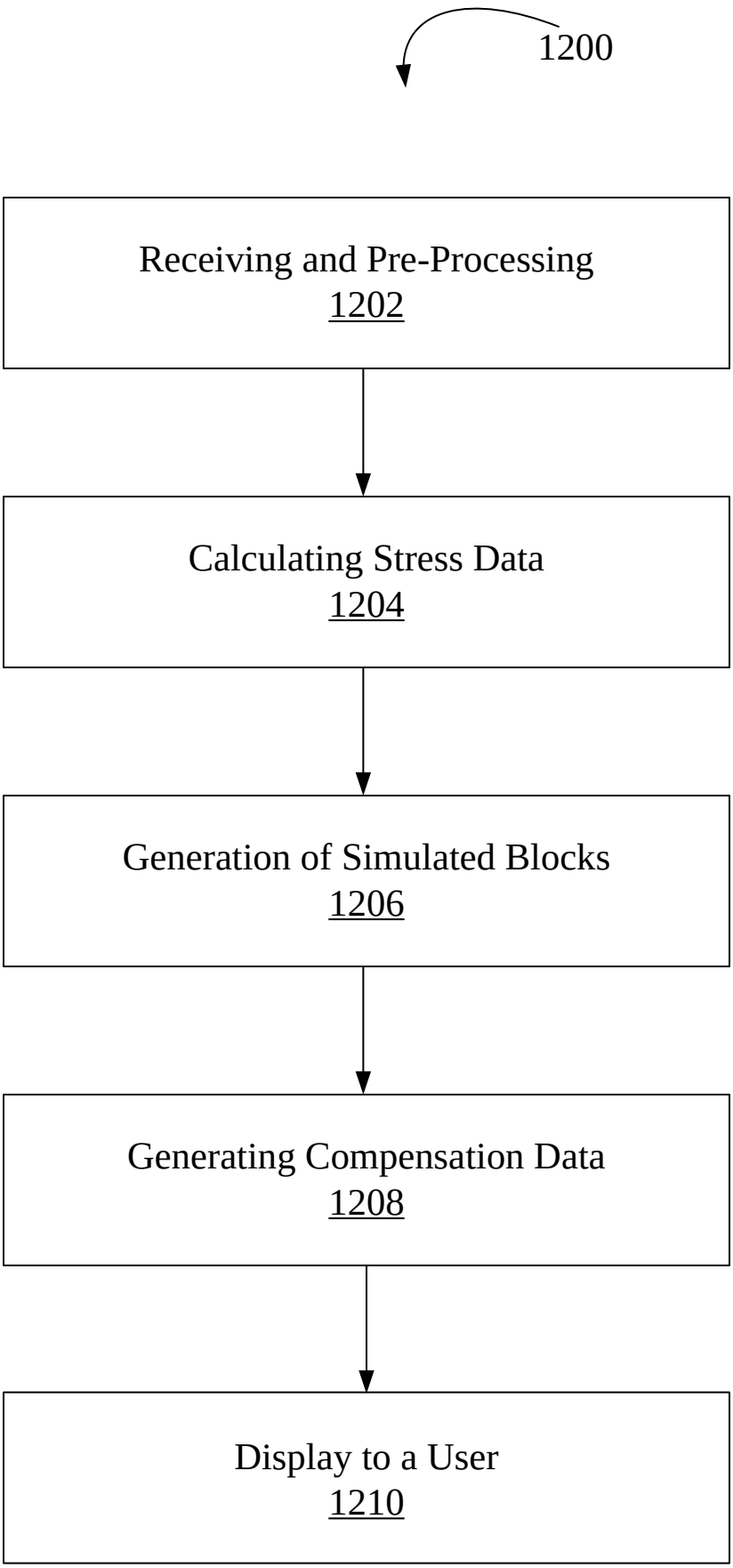
1200
Receiving and Pre-Processing
1202
Calculating Stress Data
1204
Generation of Simulated Blocks
1206
Generating Compensation Data
1208
Display to a User
1210

FIG. 12