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Power Stage Driving Schemes for Multilevel Converter

Anonymous

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The disclosure is directed to an improved multilevel DC-DC converter, which is commonly used by electronic devices with subsystems that have different voltage needs. The improved DC-DC converter is more efficient and smaller than conventional converters.

Multilevel DC-DC converte`rs can offer several advantages in terms of efficiency and power density as compared to traditional DC-DC converters but their power stage implementation is usually complicated. Due to the relatively high number of power MOSFETs used in those converters and with varying voltages at their source terminals, their drive scheme isn't straightforward. The drive scheme for those power MOSFETs usually requires several external supplies and special devices (e.g. MOSFETs of higher voltage rating) to implement them along with several bootstrapping capacitors.

Due to the above considerations, the existing drive schemes for those multilevel converters suffer from one or more of the following limitations:

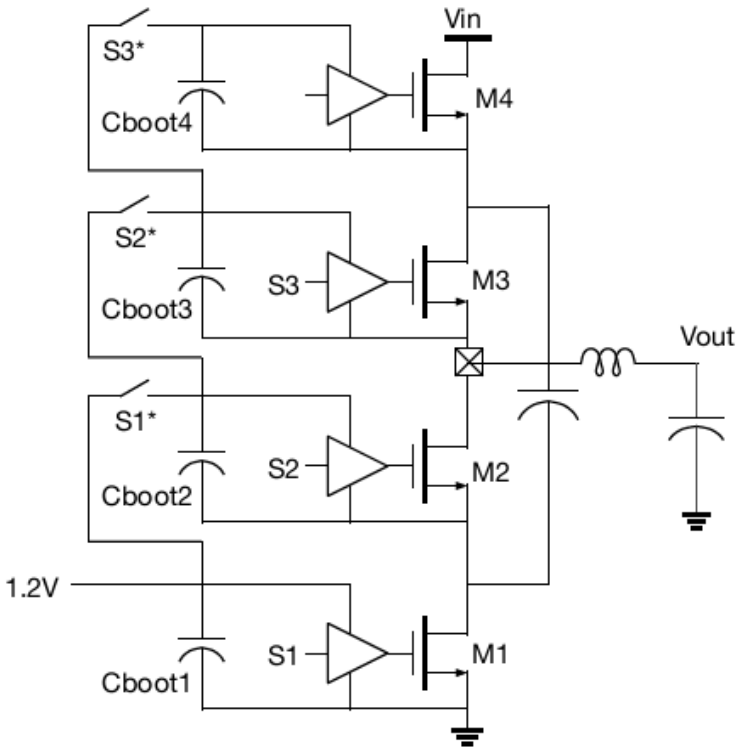
- The power MOSFETs aren't driven with the maximum overdrive voltage hindering the converter efficiency specially at high load currents
- The drive scheme requires several auxiliary supplies that are a burden to generate
- The drive scheme requires a lot of implementation area (driver FETs + bootstrapping capacitors)
- The efficiency of the drive scheme itself is low hindering the converter overall efficiency
- The drive scheme can limit the converter operation in certain ranges of input voltage, output voltage, and output current
- The drive scheme might cause functionality issues for the converter due to overlap between control signals, etc.

A drive scheme for a 3-level buck converter is proposed. It uses stacked drive FETs along with stacked bootstrapping capacitors to generate the internal supplies for the local drivers of each power FET. Two sub-schemes are proposed. The first sub-scheme is an all-way stacked drivers which requires only one auxiliary external supply. The second sub-scheme is a half-way stacked drivers which requires two auxiliary external supplies. The proposed driving scheme has the following features:

- It allows for seamless transition between the operating regions of the converter above and below 50% duty cycle.
- The drive scheme allows for extended operation region of the 3-level buck converter specially at low input voltages.
- It requires few number of auxiliary supplies (one or two)
- The drive scheme has low inherent losses improving the converter overall efficiency.
- It doesn't require special devices for implementation where low-voltage MOSFETs can be employed (less implementation area and higher efficiency)
- The same drive scheme can be extended to other multilevel converters (for example, 4-level converter or higher)

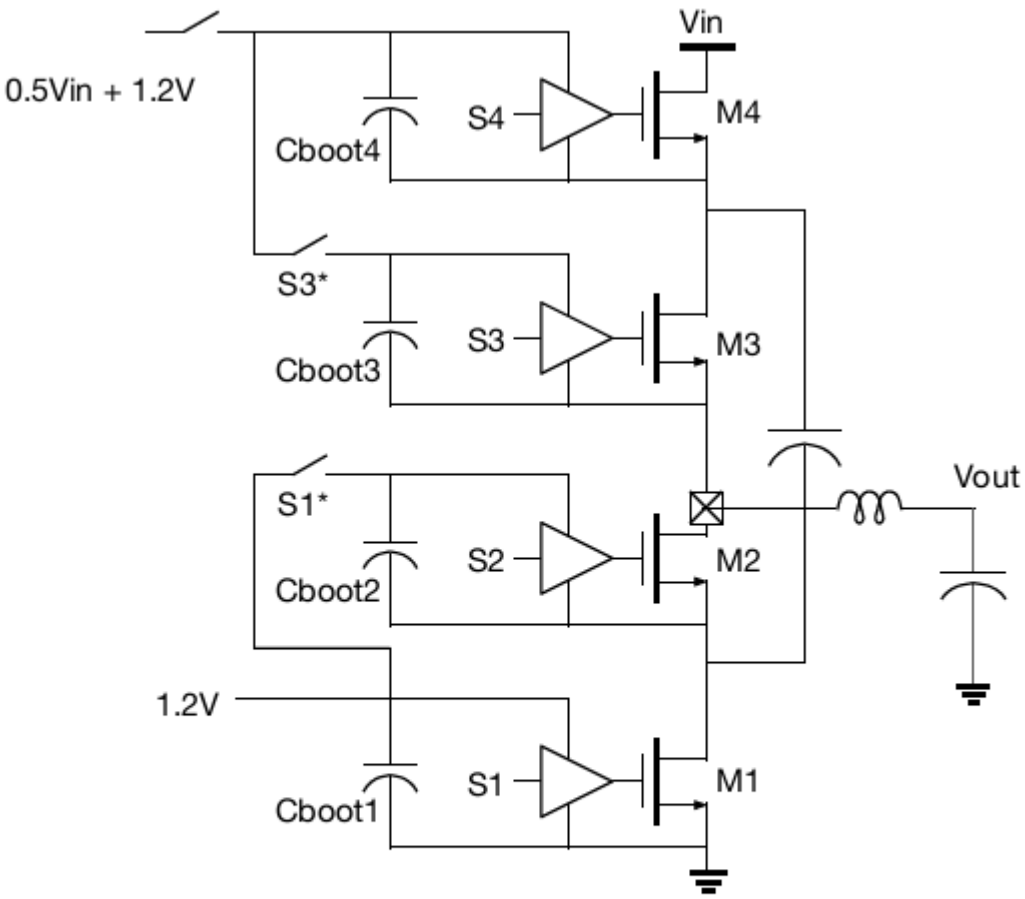
Driver functionality:

- In scheme 1, Cboot1 is used to provide charges to Cboot2 when M1 is ON by turning on S1*. Similarly, Cboot2 is used to charge Cboot3 when M2 is ON by turning on S2*, and so on.
- In scheme 2, Cboot1 is used to charge Cboot1 when M1 is ON by turning on S1*. Cboot4 is used to charge Cboot3 when M3 is ON by turning on S3*.
- S1*, S2*, S3* are generated versions from S1, S3, and S3 respectively with some added deadtime.



Scheme 1: All-way stacked driver

- Low-side bootcap needs to be bigger
- Same scheme for above/low 50% duty cycle



Scheme 2: Half-way stacked driver

- One additional supply needed
- Bootcap can be smaller
- Same scheme for above/low 50% duty cycle