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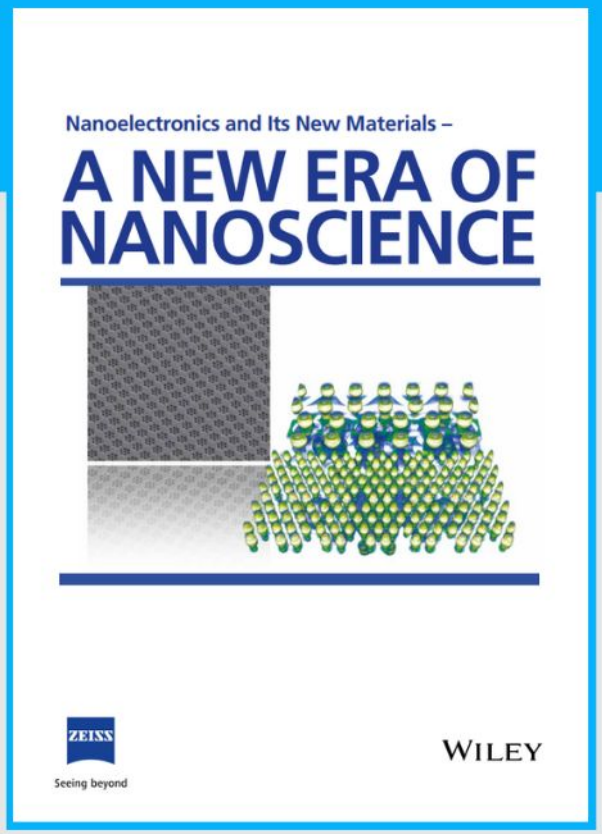

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Black Ultra-Thin Crystalline Silicon Wafers Reach the $4n^2$ Absorption Limit–Application to IBC Solar Cells

M. Garín, T. P. Pasanen, G. López, V. Vähänissi, K. Chen, I. Martín, and H. Savin*

Cutting costs by progressively decreasing substrate thickness is a common theme in the crystalline silicon photovoltaic industry for the last decades, since drastically thinner wafers would significantly reduce the substrate-related costs. In addition to the technological challenges concerning wafering and handling of razor-thin flexible wafers, a major bottleneck is to maintain high absorption in those thin wafers. For the latter, advanced light-trapping techniques become of paramount importance.
Here we demonstrate that by applying state-of-the-art black-Si nanotexture produced by DRIE on thin uncommitted wafers, the maximum theoretical absorption (Yablonovitch's $4n^2$ absorption limit), that is, ideal light trapping, is reached with wafer thicknesses as low as 40, 20, and 10 µm when paired with a back reflector. Due to the achieved promising optical properties the results are implemented into an actual thin interdigitated back contacted solar cell. The proof-of-concept cell, encapsulated in glass, achieved a 16.4% efficiency with an $J_{SC} = 35$ mA cm^{-2}, representing a 43% improvement in output power with respect to the reference polished cell. These results demonstrate the vast potential of black silicon nanotexture in future extremely-thin silicon photovoltaics.

1. Introduction

Crystalline-silicon photovoltaic (PV) modules, both mono-crystalline and multi-crystalline, account for ≈95% of the global market share,[1] with mono-crystalline Si panels dominating with an increasing share of, currently, 84%[2] due to their high efficiencies and competitive production costs. Silicon itself remains the most expensive material of a PV module. Typically, ≈30% of the module cost could be attributed just to the price of polysilicon and wafering; this percentage suddenly increased to ≈50% last year due to recent issues and shortages in the distribution chain.[1] As a consequence, there has always been a strong interest by the industry to progressively reducing wafer thickness, from the early 350 to ≈155 µm at present, and with thicknesses ≈135 µm anticipated within the next ten years thanks to enhancements in wire sawing techniques.

Despite the technological challenges[3–10] involving wafering, handling, and processing of very thin substrates, there is still a huge potential for economic savings by dramatically going thin,[11] that is, to the order of tens of micrometers or even less (named ultra-thin throughout the text). Not only would this reduce material usage to a minimum, but it might even improve the overall cell efficiency in certain cases[12,13] thanks to the lower bulk losses associated to the reduced recombination volume in thinner substrates, which translates to an improvement on open-circuit voltage. In fact, using conventional cell technologies, wafer thicknesses have already been cut down to ≈40 µm without significantly sacrificing high efficiencies.[8,14–16] However, due to the weak absorption of Si at long wavelengths, further reducing the wafer thickness seriously jeopardizes light absorption, with absorption lengths becoming larger than the wafer thickness for photons in the near infrared (NIR) spectral region.

Photon absorption can be significantly improved in low absorbing media by using appropriate light management (so-called light trapping) techniques, leading to a much longer optical path through internal dispersion and scattering. According to Yablonovitch, in a weak absorbing slab of refractive index n, absorption can be enhanced up to a factor $4n^2$ as compared to a single-pass absorption.[17] For silicon this represents an enhancement factor of ≈50 in the NIR, with a ≈5 µm Si slab absorbing as much as a 250 µm of silicon in a single-pass, if perfect light trapping was implemented. Chemical texturization through random pyramids is, by far, the most common texturing technique used in current silicon photovoltaics for the front surface. In addition to reducing reflectance, random pyramids also provide light trapping to some extent. However, its optical performance is far

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from the Yablonovitch's limit, and the relatively large amount of Si consumed during its formation (the typical pyramid height is in the range of some microns) makes wet chemical etching less appealing for ultra-thin photovoltaics. Advanced nanopatterning techniques based on lithography methods (e.g., conventional, nanoimprint, or colloidal, to name a few) can produce nanotextures with minimal material consumption and excellent optical performance that is close to the $4n^2$ limit.[18–20] However, those techniques can be laborious, expensive, or difficult to apply to large surfaces or ultra-thin standalone substrates. Consequently, the development of cost-effective nanopatterning techniques with minimum silicon consumption and surface damage becomes critical for mass-produced ultra-thin c-Si photovoltaics to ever become a commercial reality.

In the last years, new silicon surface nano-texturing methods, forming the so-called black silicon (bSi), have been developed and successfully applied to conventional PV cells. Black silicon is a random nanotexture that reduces surface reflectance from all directions to a minimum, so that Si becomes black to the naked eye as opposed to conventional micron-scale random pyramids. Black silicon can be produced through different methods[21] most notably through metal assisted chemical etching (MACE)[22] and through deep reactive ion etching (DRIE) at cryogenic temperatures.[23] Black silicon obtained through DRIE techniques offer unique characteristics that make them particularly appealing for high-efficiency ultra-thin solar cells. First, the nanotexture is formed in a self-limiting etching process, resulting in a very low Si consumption. Additionally, it is created with minimum surface damage leading to very low surface recombination in combination with Al_2O_3 passivation techniques.[24] As a result, this material has been successfully applied, for example, to high-efficiency IBC solar cell structures[25] and to photodiode detectors exhibiting near-unity External Quantum Efficiency (EQE) in a broad band[26] and above 1.3 EQE in the ultraviolet (UV).[27]

This study focuses on the application of bSi nanotexture to standalone commercially-available ultra-thin monocrystalline substrates for high-efficiency photovoltaics. First, we focus on the application of bSi nanotexture, obtained through cryogenic DRIE, to standalone ultra-thin Si substrates with thicknesses down to 10 μm. The result is uncommitted standalone thin wafers with one or both surfaces nanotextured. Next, we study the optical absorption of the textured substrates paying special attention to the light trapping properties for NIR photons, which are critical in such thin devices. Finally, we present a proof-of-concept 40 μm bSi PV cell with an interdigitated back-contacted (IBC) structure and encapsulated with a front glass. The EQE results are compared with the previous raw absorption measurements and discussed in the light of optical simulations.

2. Results and Discussion

2.1. Substrate Nanotexturing

The starting material was commercial prime-quality double-side-polished monocrystalline FZ ultra-thin Si wafers with three different thicknesses: 40 ± 4, 20 ± 2 and, 10 ± 2 μm. The diameter of the wafers was 2 inches for the case of 40 μm wafers and 1 inch for the rest. In all cases, the material was *n*-type, phosphorous doped, with resistivity in the range of 1–5 Ω cm and bulk lifetime over 500 μs. Prior to processing, the 40 μm wafers went through a standard RCA (Radio Corporation of America) cleaning process followed by a dip in HF. On the contrary, 20 and 10 μm wafers were processed directly from the box, as they were too fragile to be cleaned using standard equipment.

Black silicon nanotexturing was introduced on the front surface of the substrates through cryogenic deep reactive-ion etching (DRIE). However, ultra-thin Si wafers cannot be directly processed by the standard equipment, requiring temporary mechanical support.[28] For all samples processed in this work, we have used standard 4 inch polished c-Si wafers as carrier substrates for the DRIE process with the thin substrates bonded using standard (AZ5214, 1.4 μm) positive photoresist. This provided good thermal contact, as required by the cryogenic DRIE process, while allowing us to easily detach the substrates after the processing. The photoresist was deposited on the carrier wafer by spin coating using a standard recipe. The thin substrate was then placed on the center and gently pressed to the carrier using compressed nitrogen. Next, the carrier was placed in a vacuum desiccator for 5 min to improve the contact and, finally, hard baked for 30 min at 120 °C. After the bonding, bSi was created onto the thin substrate through a 7 min. DRIE etch in SF_6 + O_2 ambient at cryogenic temperature (−120 °C). Flow rates were set to 40 and 18 sccm for SF_6 and O_2, respectively, powers for the capacitively and inductively coupled power sources were set between 2 and 1000 W, respectively, and process chamber pressure was 10 mTorr. Finally, the ultra-thin wafers were separated from the carrier in an ultrasonic acetone bath and rinsed in IPA and deionized water. To avoid damaging the wafers due to the surface tension when introducing and removing them from the liquid baths, they were always handled sandwiched between two cleanroom wipes. After retrieving the thin substrate, the process may be repeated again on the other side in order to nano-texture both surfaces. In this work, however, two-side texturing was only attempted with 40 μm substrates. **Figure 1**(b–e) shows a scanning electron microscope (SEM) image of the black Si nanotexture obtained with DRIE as well of pictures of a finished 10 μm black silicon wafer once detached from the carrier.

Although all three wafer thicknesses were successfully processed following the above steps, failure rate was significantly higher with the 20 and 10 μm substrates due to bubbles trapped between the wafers and the temporary carrier, most probably due to resist degassing during the hard bake. These bubbles would, sometimes, break or detach those substrates during the high-vacuum before the DRIE process. Yield with the thinner substrates was significantly improved by engraving a square array of shallow grooves on the carrier substrate, allowing a path for trapped gases to escape during the process.

2.2. Optical Characterization

Thin substrates were optically characterized using a Cary 5000 UV–Vis–NIR spectrometer equipped with an integrating sphere. Absorbance, *A*, of ultra-thin substrates was determined as $A = 1-R-T$, where *R* and *T* are, respectively, the total (specular + diffuse) reflectance and transmittance. Some samples were measured on top of an aluminum mirror (back reflector); transmission is obviously zero in such cases, and it was not measured.

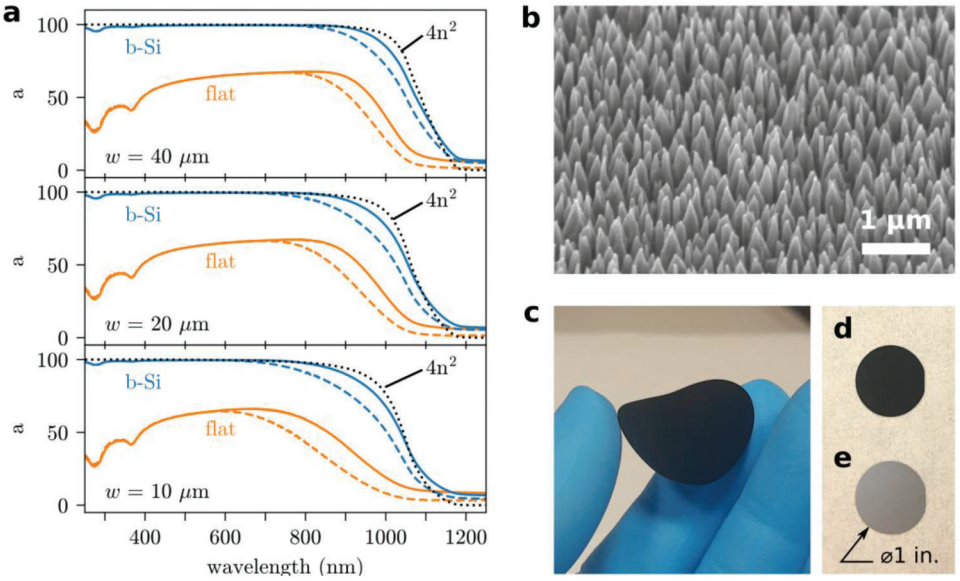

Figure 1. a) Measured absorption of thin silicon wafers (10, 20, and 40 μm nominal thickness) with polished surfaces (orange) and with black silicon texture etched on the front side (blue). Solid and dashed lines represent absorption with and without back a reflector, respectively. The dotted line corresponds to Yablonovitch's $4n^2$ absorption limit. b) Scanning electron microscope (SEM) image, bird's eye view, of the black silicon nanotexture obtained by DRIE. The scale bar represents 1 μm. c) A free-standing 10μm-thick black silicon wafer, where its high flexibility can be appreciated. d,e) Top view of two 10 μm wafers: d) textured with black silicon and e) out-of-the-box with polished surfaces.

Figure 1(a) summarizes the measured absorptance for ultra-thin wafers with 10, 20, and 40 μm nominal thickness both, out of the box with both surfaces polished, and after texturing the frontside. Notice that dashed lines correspond to measurements without back reflector (surrounded by air) while continuous lines correspond to measurements with back reflector. The maximum theoretical absorption for a thin slab with perfect light trapping, that is, the well-known $4n^2$ limit established by Yablonovitch,[17] is included in dotted lines for comparison purposes and will be discussed later on.

Let's start by focusing on the results without back reflector. Absorption in polished substrates is limited to around 70% in the visible (Vis), due to the expected reflection losses on the polished front surface, with absorption decreasing rapidly in the red and NIR due to insufficient material thickness. In the worst case, 10 μm thick wafers, this reduction starts at 600 nm wavelength, while absorption starts to decrease at around 800 nm for 40 μm-thick wafers. As the figure shows, there is a huge absorption boost after introducing bSi texturing in the front surface. First, absorption increases up to nearly 100% in the whole UV–Vis spectrum, even for the 10 μm wafer. Second, absorption also extends toward the IR, decreasing now at 800 nm for the 10 μm thick wafer and at 925 nm for the 40 μm thick wafer.

Including the back reflector improves absorption in all cases by further extending it toward the IR. Due to the relatively low absorption coefficient of silicon in the NIR range, photons that would otherwise be transmitted and escaped by the rear surface have now a second chance to be absorbed, increasing the apparent thickness of the slab. It is worth mentioning that excellent back reflectance is of paramount importance for high-efficiency ultra-thin silicon photovoltaics, which can be easily included in the final device through, for example, a PERC/PERL rear contact. Consequently, when the back reflector is included, the absorption values reported here should be indicative of the absorption potential for a finished cell in the best-case scenario.

After the introduction of black silicon, the improvement in absorption in the UV/Vis range, where the absorption coefficient of silicon is high, can be explained by the wide-band wide-angle almost-zero reflection induced by the bSi nanotexture. This anti-reflective (AR) effect has been typically attributed to a smooth monotonic variation of the effective refractive index at the nanotextured interface,[23] similarly to what has been claimed in moth-eye-like AR nanostructures.[29–32] As a result, the interface would behave as an effective gradual-index AR coating that would reduce reflection and enhance absorption in the UV/Vis range. However, this effect would not help improving absorption in the NIR region, where Si absorption is low, since it would not scatter light nor introduce any light trapping effect. Based on this hypothesis, Figure S1 (Supporting Information) shows the calculated absorption for both planar and bSi textured samples without considering any scattering. While calculations perfectly fit the polished absorption data, surprisingly there is a huge discrepancy (≈200 nm in the absorption edge position) for textured samples indicating that bSi also provides good light trapping properties, that is, it induces light dispersion within the substrate.

The scattering ability of black silicon also becomes apparent by analyzing the reflection haze, defined as the ratio between the diffuse fraction of reflectance, R_d, and the total (diffuse + specular) reflectance, R:

$$haze = \frac{R_d}{R} \tag{1}$$

Figure 2 shows the haze for a 20 μm wafer with bSi on the front surface along with the total and diffuse reflectance com-

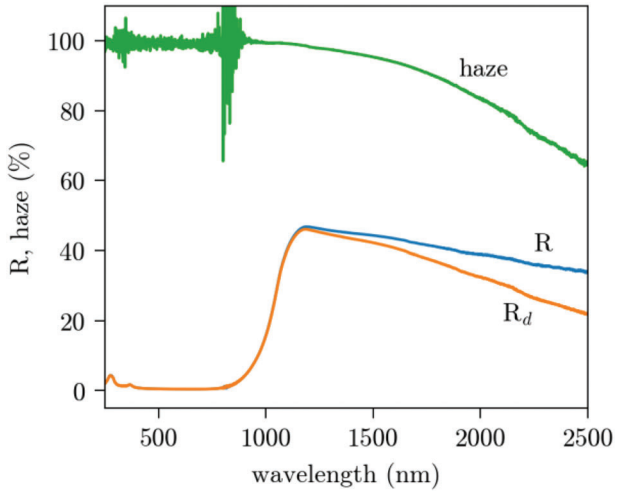

Figure 2. Total reflectance (specular + diffuse), R, diffuse reflectance, R_d, and haze (R_d/R) for a silicon wafer with a thickness of 20 µm and black silicon on the front surface.

ponents. As the figure shows, the reflectance is completely diffuse (100% haze) in the whole spectrum range of interest ($\lambda <$ 1250 nm) and slowly decays in the IR for increasing wavelengths. At $\lambda = 2500$ nm, the haze is still above 60%, demonstrating the excellent scattering ability of bSi in the NIR.

As already mentioned, ultra-thin silicon substrates suffer from a low absorption in the NIR spectral range due to the low absorption coefficient of Si. Texturing and light-trapping techniques can improve absorption in this range by increasing the average path that light travels inside the bulk. The so-called Yablonovitch's $4n^2$ limit defines the maximum absorption enhancement, under ray optics approximation, that can be achieved through light trapping. It states that, with ideal surface texturing (i.e., complete internal light randomization) and ideal back reflectance, absorption in a low-absorbing material can be enhanced up to a factor of $4n^2$ with respect to a single-pass absorption, with n being the refractive index of the material. According to this theory, the maximum absorption in a silicon slab can be determined as[12]:

$$A_{4n^2} = \left(1 + \frac{1}{\alpha w 4n^2}\right)^{-1} \quad (2)$$

where w is the thickness of the wafer, α is the absorption coefficient, and n is the refractive index of the material.

The $4n^2$ absorption limit represents, therefore, an excellent benchmark to evaluate the effectiveness of a defined light trapping scheme and, for this reason, we already included it in Figure 1 as a dotted line for the nominal wafer thickness. As it can be seen, the experimental reflectance with a back reflector is really close to the $4n^2$ even though just the front surface is textured. Interestingly, further texturing the back surface with bSi leads to a further, albeit minor, improvement of the absorption (see Figure S2, Supporting Information). Taking into account that a fraction of the total thickness is lost during the etching of bSi on both surfaces[21] we might consider, for all intents and purposes, that this structure is on par with the $4n^2$ absorption limit. Most importantly, this is achieved by texturing only one of the surfaces.

Despite the widely-accepted smooth-interface oversimplification, it is important to clarify that this is not the first time that strong scattering by bSi has been reported in the literature. Most prominently, Ingenito et al. also noticed it in their well-known work[18] where they demonstrated a proof-of-concept ultra-thin PV device approaching the $4n^2$ limit by integrating bSi nanotexturing in the front surface, for anti-reflection purposes, and random pyramid texturing in the back, for light-trapping purposes. Despite they introduced a back-texture specifically for light-trapping purposes, the data reported for the bSi front nanotexturing was similar to the one reported here. A comparison can be seen in the Figure S3 (Supporting Information) for the absorption of two wafers with front bSi nanotexture and identical thickness (20 µm). The one in this study has a polished back surface while the one from Intenito's work has a random pyramid texture on the backside. In spite of that, both absorption curves are almost identical. Notice that, as a strong difference to the present work, Ingenito's does not start from standalone ultra-thin substrates, but thinned down a standard wafer at certain windows defined by lithography, thus greatly simplifying handling and processing of the test devices.

For the sake of exploring the potential for sunlight harvesting of the standalone ultra-thin black substrates, we have computed the total photogenerated current that could be achieved under AM1.5G spectrum in a solar cell considering no shadowing losses and a 100% collection efficiency. Integration was performed in the wavelength range from 250 to 1200 nm. Results are shown in **Figure 3** for the three available thicknesses along with the calculations considering the $4n^2$ upper limit and the two-pass absorption as the lower reference. Notice that two-pass absorption would be equivalent to a wafer with an ideal back reflector and neither internal nor external front reflectance, but no light trapping. In the figure, we have included error bars that represent the uncertainty in the thickness as given by the manufacturer and considering 1.5 µm loss per every bSi etch. Additionally, symbols correspond to the actual thickness indirectly deduced by weighing the wafers in a precision scale. The single-side textured 40 µm wafer, however, broke before weighting and the nominal thickness was considered instead. As the figure shows, photogenerated current by a wafer with bSi in the front surface and surrounded by air is already significantly higher than two-pass absorption and, after including the back reflector, the calculated photocurrent is just around 1.5% lower than the one predicted for the $4n^2$ limit when considering the nominal thickness of the samples. The photocurrent determined from absorption measurements reaches 39.4 mA cm^{-2} for 10 µm wafer, and up to 41.7 mA cm^{-2} for the 40 µm wafer with bSi on both sides. These values are similar to the J_{sc} values present in standard-thickness high-efficiency solar cells, such as the certified $J_{sc} = 41$ mA cm^{-2} obtained with bSi interdigitated back-contacted (IBC) cells.[25]

In summary, all the above results prove that bSi nanotexturing is excellent for light trapping purposes, suggesting that texturing just the front surface could be efficient for both, reducing front reflectance and boosting absorption in the NIR. This conclusion undermines the usual assumption that bSi nanotextures can be understood primarily as an effective gradual index interface, even in the IR. Notice that, although the wavelength of IR light in air can be several times larger than the typical size of the nanostructures, the wavelength inside silicon is much closer to the needle

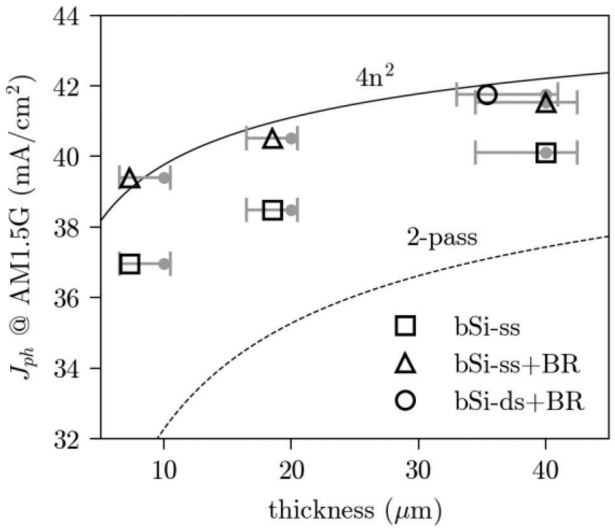

Figure 3. Calculated ideal photocurrent (J_{ph}) assuming AM1.5G spectrum (250–1200 nm) for black silicon (bSi) ultra-thin substrates with different thickness and backside configuration. The term bSi-ss (single-sided) correspond to substrates with bSi in the front and a polished back surface, whereas bSi-ds (double sided) corresponds to substrates with bSi on both surfaces. Notice that only 40 µm substrates where textured on both sides. The term BR (back reflector) indicates the substrate was backed with a mirror, otherwise the substrate was surrounded by air. The nominal thickness of the substrates is indicated by the solid dot with the error bars representing the uncertainty in thickness given by the manufacturer and due to the black Si etching. Symbols where placed at the thickness measured by weighting the wafers when possible, otherwise they are placed at the nominal wafer thickness value. For reference purposes the J_{ph} corresponding to the two-pass absorption and to the $4n^2$ absorption limit are shown in dashed and solid lines, respectively.

sizes. We believe that this fact, and the inherent random nature of bSi, could be the source of the excellent light randomization within the substrate.

2.3. Proof-Of-Concept Solar Cell

Thus far, we have reported on the nanotexturing of ultra-thin monocrystalline Si substrates. Given the promising optical results, we now try to transfer them into a proof-of-concept IBC solar cell that can exploit the optical advantage of a bSi front surface in the material. In particular, we used 40 µm ultra-thin silicon substrates. Notice that, at this point, bSi wafers were standalone (no carrier substrate), just as the new ones, but with a textured front surface. As mentioned earlier, one of the main challenges of ultra-thin PV is the handling of the substrates, which cannot be processed as usual without a carrier substrate. In our case, after front surface passivation with an Al_2O_3/SiC stack, we permanently glued the substrates on a 0.7 mm Schott Borofloat 33 glass using transparent epoxy EpoTek 303-3 M, leaving the back surface free for processing the IBC cells. We chose a conformal Al_2O_3 layer deposited by atomic layer deposition (ALD) as it offers excellent surface passivation of bSi nanotexture,[33] achieving average lifetimes above 250 µm in our bSi ultra-thin wafers (lifetime spectroscopy measurements are available in Figure S4, Supporting Information). The IBC c-Si solar cell structure used is based on vanadium oxide (VO_x) and laser processed phosphorus-doped silicon carbide stacks as hole and electron transport layers, respectively. These contact technologies are compatible with low-temperature processing and have already already successfully applied by some of the authors to fabricate ultra-thin c-Si PV cells.[34] The fabrication process used here was similar to what is described in,[34] the main difference being that the front surface of the substrate was textured with bSi, whereas the back surface was polished. A device with a polished front surface was also fabricated for a direct comparison. In our process we have observed absolute variations within 1% (<10% relative variation) in the efficiency of similar devices produced in close-by runs, although rigorous statistics cannot be performed due to the on-going learning curve and low overall yield because of the high risk of breaking the substrates during process handling. For this reason, special care was taken here to process both devices in parallel in order to minimize any device difference except for the surface texturing. This enables a very precise comparison of both samples and to study the relative effect of introducing bSi. **Figure 4** shows the schematic cross-section of the produced devices together with a picture of the rear surface of one of the fabricated solar cells where the spatial distribution of fingers, bus bars, and the aluminum pad can be seen.

In **Table 1**, we show the photovoltaic figures (open-circuit voltage, V_{oc}; short-circuit current density, J_{sc}, fill factor, FF and conversion efficiency, η) measured under 1 sun illumination and standard conditions (AM1.5 g, 25 °C) for the two front surface configurations namely polished and bSi nano texture. The I–V curve of the bSi cell in dark and under illumination can be seen in Figure S5 (Supporting Information). As we can see, the efficiency of the one with the bSi nanotexture is much better than for the one with polished surface and the effect of the bSi becomes apparent in the strong increase in J_{sc} from 27.1 to 35.4 mA cm^{-2}. This improvement, apart from a slightly better V_{oc} value, is the main reason behind the much better efficiency result of the bSi device.

In order to get a deeper insight into the J_{sc} improvement, in **Figure 5**(a) we compare the external quantum efficiency (EQE) of both cells, in symbols, the one with front nanotexture and the reference one. As it can be seen, the EQE of the bSi thin cell is above the polished one in the whole spectral range, especially in the UV and the NIR regions. The experimental EQE values can be analyzed in the light of optical calculations considering a 1D approximation of the devices. In the case of the polished device, we define the layered structure as indicated in Figure 5(b), where the optical parameters of the layers were determined by transmission/reflectance measurements (Borofloat 33 and EpoTEK 330), spectroscopic ellipsometry (Al_2O_3 and SiC layers) or from the literature (c-Si).[35] At the rear surface, we consider a perfect back reflector, which is a reasonable approximation to the optical behavior of the device structure found in the rear side of the device. With this optical model, we are able to calculate the photon absorption in the c-Si bulk expected in the device (blue dashed line in Figure 5(a)). This c-Si absorption can be considered as the maximum attainable EQE values since no electrical losses are considered. As it can be seen in Figure 5(a), this theoretical maximum EQE is higher than the measured EQE. However, the experimental EQE can be excellently fitted just considering a constant electrical loss of 8% along the full spectrum, that is, an internal

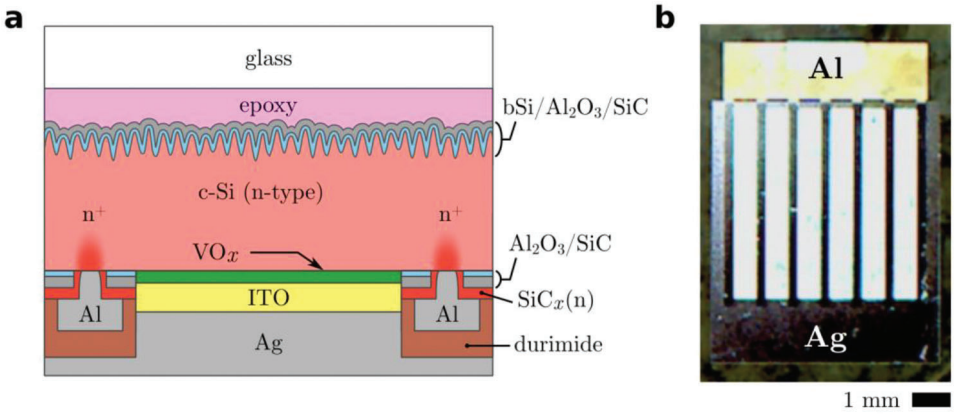

Figure 4. a) Schematic of the device cross-sectional structure. b) Picture of the rear surface of a finished device.

Table 1. Photovoltaic figures of the 40 µm PV cells with both polished and bSi front surface.

	V_{oc} [mV]	J_{sc} [mA cm^{-2}]	*FF* [%]	η [%]
Polished	600	27.1	70.7	11.5
bSi	633	35.4	73.4	16.4

quantum efficiency of 92%. These losses can be explained by the spatial distribution of the collection efficiency of the IBC configuration, as it has already been reported in the literature for similar devices.[34] On the one hand, minority carriers photogenerated in the vertical region above a hole-selective contact must travel just the thickness of the substrate before being collected, and the only recombination mechanism that could impact on their collection is the front surface recombination velocity. This parameter was measured during the fabrication procedure leading to ≈10 cm s^{-1} that does not explain the electrical loss. On the other hand, minority carriers photogenerated in the vertical region above a base (electron-selective) contact finger must flow horizontally a longer way, that is, half of the width of the finger in the worst case. Furthermore, the base contacts created by the laser introduce additional recombination paths for the minority carriers during this travel. As a consequence, a part of the cell is not providing a perfect collection efficiency and, what is more important, this effect is independent on the illumination wavelength, supporting the constant electrical losses deduced from the EQE experimental data and optical calculations.

The analysis of the planar device has allowed us to characterize the electrical losses of the device, leading to a good matching of the experimental EQE by means of an accurate 1D model of the optical response. Bearing these results in mind, we now model the EQE for the bSi device. Due to the significant difficulty in accurately modeling the bSi surface, we now start from the experimental absorptance of the bSi with a rear mirror shown in Figure 1. This absorptance is corrected by the optical response of the glass and the epoxy that can be obtained from the optical simulations with identical parameters than the ones used for the polished device. The obtained curve is shown in Figure 5(a) (orange dashed line) where we can see that the mean value is reduced from ≈97% to ≈95% due to the effect of the front reflectance. Additionally, a strong decrease in the UV for wavelengths below 400 nm is observed that corresponds to the absorption of

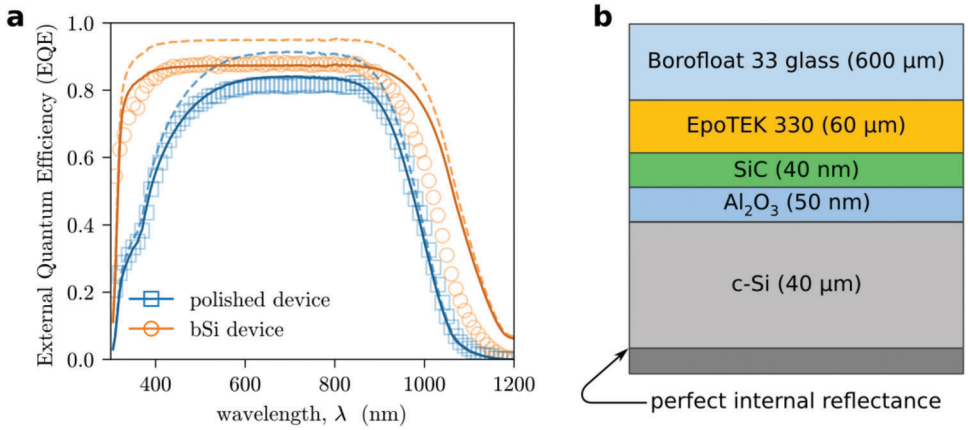

Figure 5. a) Comparison of the EQE spectra obtained for the polished (blue) and bSi (orange) devices. Experimental values are shown in symbols, while theoretical calculations are shown in solid lines. The calculated maximum EQE curves, that is, assuming no electrical losses, are also shown in dashes. b) Structure used in the optical simulations of the polished device.

the glass and epoxy. Once we have the expected absorptance in the bSi device, we apply the same factor for the electrical losses, that is, a polished collection efficiency of 92%, than the one we found for the polished device. The result is the curve shown in Figure 5(a) (orange solid line) that fits well the experimental EQE up to $\lambda = 900$ nm. Beyond this wavelength ($\lambda > 900$ nm) the experimental EQE of the bSi device is clearly below the values expected from the calculations.

For the bSi device, the good agreement between experimental and modeled EQE curves up to $\lambda = 900$ nm confirms that the excellent optical absorption measured in the previous sections can be successfully transferred to electrical performance. In fact, the reduction of the front reflectance is the main reason for the significant increase in J_{sc}. Regarding the spectrum beyond 900 nm, we can see that the bSi device clearly shows better results than the one with front polished surface, which confirms that bSi is providing light trapping properties; however, the EQE improvement lags behind the values expected from the optical characterization of the wafer. This reduction is not related to a low rear reflectance because we correctly reproduce the results (Vis/NIR) in the reference polished device by considering perfect back reflectance. As a consequence, a loss in scattering effectiveness of bSi should be the major mechanism that can explain the results in the NIR. These poorer-than-expected scattering properties of bSi could be explained by several effects that can take place simultaneously, all related to the device fabrication process. First, it is known that bSi nanotexturing is slightly etched during successive RCA cleaning steps,[36] slightly degrading its optical performance. Second, the multiple layers covering the nanostructures (Al_2O_3 + SiC_x + Epoxy + Glass) reduce the refractive index contrast and impedance mismatch, which would greatly reduce the scattering effect of the nanostructure. Additionally, the thin film deposition, specially the PECVD (Plasma-Enhanced Chamical Vapor Deposition) technique used for the SiC, could fill the gaps between silicon pillars leading to a smoother surface. All these effects should be studied in the light of 3D optical simulations and further experiments in order to fully understand and identify the dominant effects. . Still, all these negative effects could be potentially minimized through process optimization. For instance, the shape of the bSi nanotexture can be controlled through the DRIE etching parameters,[23] which could be optimized for scattering especially after cell processing. Some cell processes, such as the RCA cleaning steps and SiC deposition, can be optimized, or substituted in order to preserve the bSi texture sharpness. Finally, wafers with bSi on both surfaces could be used as starting material so that back surface scattering would also contribute to light trapping. The required optimization of the device structure and fabrication process is beyond the scope of this work where, despite all these effects that are jeopardizing the excellent light trapping properties of bSi, the reported proof-of-concept device demonstrates the huge potential of bSi surfaces on thin c-Si photovoltaic devices.

3. Conclusion

Black Si obtained by cryogenic DRIE etching on c-Si is an excellent nanotexture able to suppress reflection in the whole UV/Vis/NIR region while remaining compatible with high-efficiency PV. In this study, we have proven that this nanotexture can be successfully applied to ultra-thin c-Si substrates with thicknesses down to 10 µm, benefiting from low Si consumption. Optical measurements show that bSi is excellent for light-trapping, approaching the $4n^2$ limit even when applied only on the front surface with no texturing on the back surface whatsoever. Given the excellent optical results, we have fabricated a proof-of-concept 40 µm thick bSi IBC cell using low-temperature processes. The cell achieved a 16.4% efficiency with an $J_{SC} = 35$ mA cm^{-2}, representing a 43% improvement in output power with respect to the reference polished cell. EQE results with bSi front surface improve the identical device with polished front surface in all the measured spectrum ranges, from NIR to UV, demonstrating that the optical properties can be successfully transferred to electrical photovoltaic performance in a final, encapsulated, cell. Despite these excellent results, front encapsulation hindered the light-trapping effectiveness of the front bSi texture. This revealed some of the issues in the cell structure needing tackling in order to be able to unleash the full potential of bSi.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

black silicon, interdigitated back contact (IBC), lambertian light trapping, ultra-thin silicon solar cells, Yablonovitch's $4n^2$ limits

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