Comparison of Fast Switching High Current Power Devices

Ed Shelton[1], Kawsar Ali[1], Renke Han[1], Dan Rogers[1], Jeff Carter[2], Lathom Louco[2], Mike Beadman[3], Patrick Palmer[4]

[1] University of Oxford, United Kingdom
[2] Borg Warner, United States of America
[3] Cambridge Design Partnership, United Kingdom
[4] Simon Fraser University, Canada

Corresponding author: Ed Shelton, edward.shelton@eng.ox.ac.uk

Abstract

New GaN and SiC wide bandgap power devices offer impressively fast switching performance compared to their traditional Silicon counterparts. However, Silicon devices have not stood still, and new generations of these devices offer excellent performance at competitive prices. This paper makes a comparative study between the latest generation of high-current SiC, GaN, Si CoolMOS and Si IGBT power switching devices, switched as fast as possible using low inductance circuit design and no external gate resistors. An analysis of the factors that determine switch edge-rate is presented, along with an overview of circuits developed by the authors to achieve accurate measurement of switching energy loss.

1 Introduction

Increasing the switching frequency is a common trend in modern power supply design as it tends to reduce the sizes of passive components (inductors and capacitors), resulting in a more compact product. Very high switching frequency designs (100 kHz – 1 MHz) have been enabled by wide bandgap (WBG) Silicon Carbide SiC and Gallium Nitride (GaN) power switching devices, which can allow faster switching compared to conventional Si devices. However, WBG devices are yet to match Si devices in terms of price and availability, and a new generation of Si devices offer excellent switching performance at competitive prices. A like-for-like comparison of performance will help power supply designers make an informed choice.

Switching loss is directly proportional to switching frequency. There are two parts to the switching loss occurring in a MOSFET – one part is due to the stored charge in the output capacitance of the device, and the other part is due to the overlap between voltage and current during the switching transition. The first part should be minimised with careful Printed Circuit Board (PCB) layout that pays attention to the switched-node parasitic capacitance. The second part depends on how quickly the device is turned on or off. Both of these can be largely eliminated using soft-switching techniques, but that is not the subject of this paper.

Fastest switching of a device is achieved with zero external resistance in the gate path (note that there will always be some gate resistance internal to the device and gate-driver). Fast switching means less overlap region between device voltage and current leading to reduced switching loss. However, parasitic inductances in the device package and layout of the circuit causes oscillation and voltage overshoot, which increases the switching loss and EMI, and can lead to device failure by over-volting the device. For these reasons manufacturers recommend using external gate resistors to slow down switching and to dampen out this oscillation, but at the cost of increased switching loss.

In this work the latest and best-in-class Silicon and WBG devices are compared using a half-bridge test circuit with a 400 V-DC bus voltage and a 40 A switch inductive load current. We attempt to minimise the parasitic circuit inductance with careful layout and the use of a polyimide dielectric layer in the PCB stack-up. To accurately measure switching loss, voltage and current measurement circuits are embedded in to the PCB to avoid high-frequency noise artifacts typical of traditional voltage and current probes. Identical PCB layouts are used for each device type to create a level playing field to compare the performance of four different device technologies (SiC MOSFET, GaN HEMT, Si MOSFET, Si IGBT) in their respective packages (all are surface-mount).

In some of the tests presented in this paper, the devices are switched without an external gate resistor in order to achieve maximum switch speed and explore the limits of their performance.

The contributions of this paper are as follows:

1. A switching performance comparison between recent Si and commercial WBG devices.
2. An example of a circuit layout optimized for switching speed using non-conventional PCB construction methods.
3. A demonstration of the switching performance that can be achieved by using zero external gate resistance.
4. A comparison between experimentally measured switching losses, those predicted by switching theory, model-based SPICE simulation, and direct extrapolation from manufacturers' datasheets.

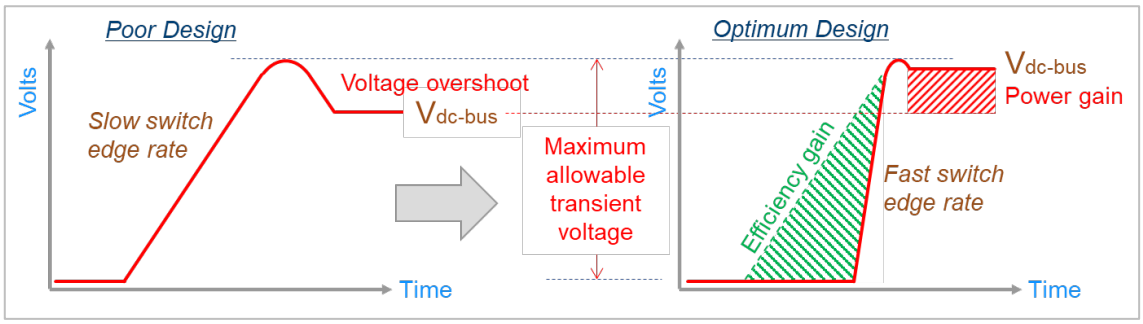


Figure 1: The motivation for reducing switching losses is to reduce the cost of thermal management, whilst at the same time reducing the size and cost of passive components by operating at higher switching frequencies.

The motivation for this work comes from the need to push the limits of a high switching frequency whilst achieving low losses, which are always positioned against one another as a trade-off. With optimal circuit design, a favorable trade-off between switching losses, voltage overshoot and power throughput can be achieved, as shown diagrammatically in *Figure 1*.

2 Switching theory

Switching does not occur instantaneously, but instead takes a finite transition time during which energy is dissipated. This is due to an overlap between switched voltage and current. A first-order approximation of the losses in a half-bridge switching circuit is shown in *Figure 2*. The dominant factors are switch edge rate, parasitic switch node capacitance, and on-state resistance.

A more sophisticated numerical approach is presented in this section. The following equations [4] are used to calculate the rise (r) and fall (f) times of current (i) and voltage (v) of the device during turn-on and turn-off events.

$$t_{\mathrm{ir}} = R_{\mathrm{G}} C_{\mathrm{iss}}(V_{\mathrm{DS}}) \times \ln\left(\frac{V_{\mathrm{GS+}} - V_{\mathrm{TH}}}{V_{\mathrm{GS+}} - V_{\mathrm{gp}}}\right) \quad (1)$$

$$t_{\mathrm{vf}} = R_{\mathrm{G}} \times \frac{Q_{\mathrm{GD(D)}}}{V_{\mathrm{DS(D)}}} \times \frac{V_{\mathrm{DS}}}{V_{\mathrm{GS+}} - V_{\mathrm{gp}}} \quad (2)$$

$$t_{\mathrm{on}} = t_{\mathrm{ir}} + t_{\mathrm{vf}} \quad (3)$$

$$t_{\mathrm{vr}} = R_{\mathrm{G}} \times \frac{Q_{\mathrm{GD(D)}}}{V_{\mathrm{DS(D)}}} \times \frac{V_{\mathrm{DS}}}{V_{\mathrm{gp}} + V_{\mathrm{GS-}}} \quad (4)$$

$$t_{\mathrm{if}} = R_{\mathrm{G}} C_{\mathrm{iss}}(V_{\mathrm{DS}}) \times \ln\left(\frac{V_{\mathrm{gp}} + V_{\mathrm{GS-}}}{V_{\mathrm{TH}} + V_{\mathrm{GS-}}}\right) \quad (5)$$

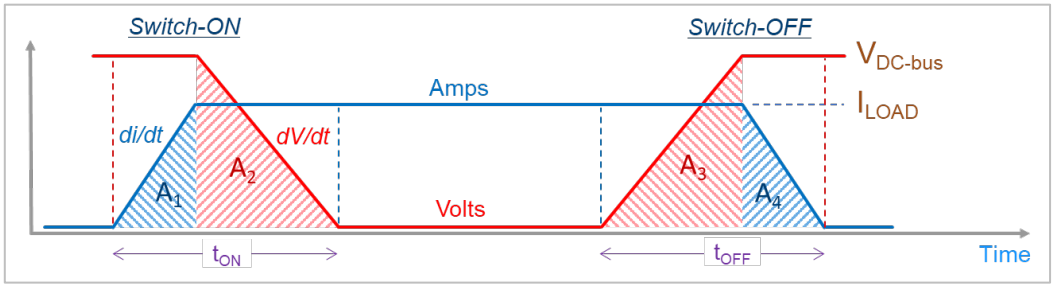
$$t_{\mathrm{off}} = t_{\mathrm{vr}} + t_{\mathrm{if}} \quad (6)$$

Here, R_G is the total gate resistance, C_{iss} is the effective input capacitance as seen by the gate drive circuit; V_{GS+}, V_{GS-} are the relative values of the positive and negative (respectively) bias voltage applied between gate and source. V_{DS}, V_{TH}, V_{gp} are drain-source, gate-threshold, and gate-plateau voltage respectively. $Q_{GD(D)}$ is the datasheet-specified gate-drain charge at the datasheet test condition with drain-source of $V_{DS(D)}$. Using the above equations, the switching energies during turn-on and turn-off can be calculated:

$$E_{\mathrm{on}} = \frac{1}{2} V_{\mathrm{DC}} I_{\mathrm{LOAD}} t_{\mathrm{on}} + \frac{1}{2} C_{\mathrm{OUT}}(V_{\mathrm{DC}}) {V_{\mathrm{DC}}}^2 \quad (7)$$

$$E_{\mathrm{off}} = \frac{1}{2} V_{\mathrm{DC}} I_{\mathrm{LOAD}} t_{\mathrm{off}} \quad (8)$$

Note that the CV^2 component of switching loss occurs only during the turn-on of the device. A charge-equivalent output capacitance [5] at the drain-source voltage of V_{DC} is calculated from manufacturers' datasheet plots.



$$P_{\mathrm{LOSS}} = (\tfrac{1}{2} \times V_{\mathrm{DC}} \times I_{\mathrm{LOAD}} \times [\, t_{\mathrm{ON}} + t_{\mathrm{OFF}} \,] \times f_{\mathrm{SW}}) + (\tfrac{1}{2} \times C_{\mathrm{OUT}} \times {V_{\mathrm{DC}}}^2 \times f_{\mathrm{SW}}) + (R_{\mathrm{DS(ON)}} \times {I_{\mathrm{LOAD}}}^2)$$

Figure 2: Switching diagram shows integration of area under idealized current and voltage switching transitions as a way to calculate energy dissipation in a single switch cycle. The power loss equation adds output capacitance discharge energy loss; These per cycle energy losses are multiplied by the switching frequency to give power loss. The addition of a conduction loss term completes this assessment of power loss in a half-bridge switch stage to a first order approximation.

In reality there are other parasitic loss mechanisms, such as body-diode Qrr reverse recovery charge, Miller and output capacitances, and source-pin inductance shared between gate-drive and power circuit, all of which act to increase switching losses. These are beyond the scope of the numerical analysis presented here. However, specific parasitic elements are considered further in the SPICE simulations section of this paper.

3 SPICE Simulation

Circuit simulation has been conducted in LT-Spice and P-Spice. The simulations place a device model within a circuit that is representative of the one used by the authors for getting experimental test data. Critically, the circuit simulation includes parasitic R, L and C elements to reflect the real-world design of the PCB.

3.1 Device models

The transistor models used here have been downloaded recently from the device manufacturers' websites. Unfortunately, the authors were not able to find a model for the specific SiC MOSFET from ST used in the experimental tests, so for the simulation of this device a model is used for a larger device in the same family, as a 'scaled-experiment'. In this case, the circuit components and parasitic elements were scaled by an estimation of the relative die area, and then the results were scaled back afterwards to suit the device used here. This is an established method in this field, although it requires some care. Three of the models work well in LT-Spice, but the IGBT model from Infineon only works in P-Spice. For this model the authors performed simulation using the latest version of P-Spice from TI.

3.2 Circuit Parasitics

There are several parasitic circuit inductances that must be considered when designing a circuit that can switch at very high edge rates. The most significant of these is the Switched Current Commutation Loop (SCCL), which is a circular path around both switches and the DC-bus capacitor. The significance of this circular current path is explained in *Figure 3*.

The main parasitic elements considered for the simulation circuits are:

1. *Switched Current Commutation Loop (SCCL) inductance:* This was measured on the test PCB with a VNA (Vector Network Analyser), and an equivalent value single lumped component added to the simulation circuit.
2. *Gate-drive loop inductance:* This was again measured with a VNA on the test PCB, and an inductor of equivalent value added in series with the simulation gate driver circuit.
3. *Switched node capacitance:* This was measured with a VNA and added to the simulation circuit as a capacitor component.

3.3 Circuit Board Parasitic Analysis

The authors used Ansys Q3D Extractor to obtain the parasitic values from the PCB layout. This is a quasi-static 2D and 3D analysis tool that enabled us to extract R, L, and C parameters from our PCB design; it also allowed us to explore design options and understand the intricate trade-offs between various possible implementations, before we committed to building boards. The extracted parameters were used in the circuit simulations to add representative parasitic elements, and for VNA measurement checking.

From our Q3D analysis and VNA measurements we found the following parasitic elements:

1. *Current commutation loop inductance* was found to be 0.4nH from Q3D, which compared favorably to the 0.6nH measured with the VNA on a bare PCB.
2. *Switch-node capacitance* was found to be 80pF using Q3D, and measured at 90pF with the VNA on a bare PCB. This is a close correlation.
3. *Gate-loop inductance* was found to be 8nH using the VNA to measure a bare PCB.

In all cases of measurement with a bare PCB, tracks we linked with copper braid and wire as needed to complete circuits, and SMA connectors soldered to the board to connect to the VNA, such that the VNA and Q3D were making the same measurements as close as practically possible.

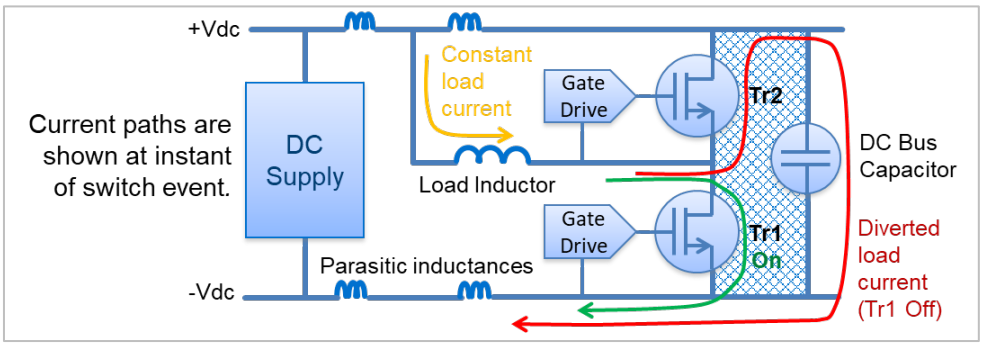


Figure 3: Schematic diagram showing parasitic switched commutation loop inductance, as a current loop around an area enclosing both power switches and the local DC-bus capacitor, with current paths before and after the moment of the switch event overlayed.

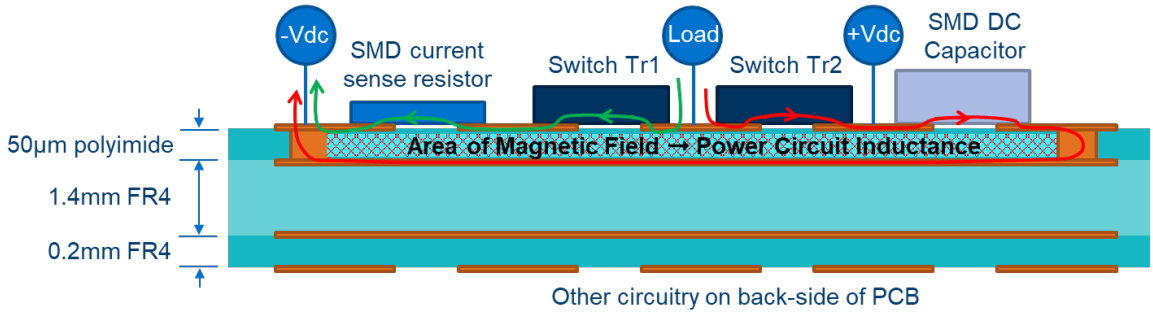


Figure 4: Hybrid circuit board construction achieves low inductance layout using multi-layer construction with a polyimide dielectric between the switching traces on the top layer and current return path directly underneath. In this way the opposing current directions cancel a magnetic field that would otherwise cause switching inductance.

4 Experimental Results

4.1 Test Platform and Measurements

The authors developed a test platform to obtain very fast switching edge rates from the power devices being studied. This includes power circuit and gate-drive designs optimised for minimum parasitic inductance and capacitance. *Figure 4* shows the SCCL superimposed onto a cross-section diagram of the PCB, with the current paths indicated. The area enclosed by this loop defines the SCCL. A very low SCCL inductance is achieved using a multi-layer PCB that puts the current return path directly under the main switching components. A thin polyamide dielectric layer is used to minimise the separation distance between these two opposing current paths, whilst achieving high-voltage electrical insolation barrier.

The experimental platform designed by the authors includes voltage and current measurement circuits embedded directly into the test PCB. This is shown schematically in *Figure 5*. There are several advantages in doing this, including improved signal fidelity, lower coupled noise, and higher bandwidth, when compared to externally connected oscilloscope probes. The measurement circuits were designed to minimise insertion effects on the switching devices and circuit being tested.

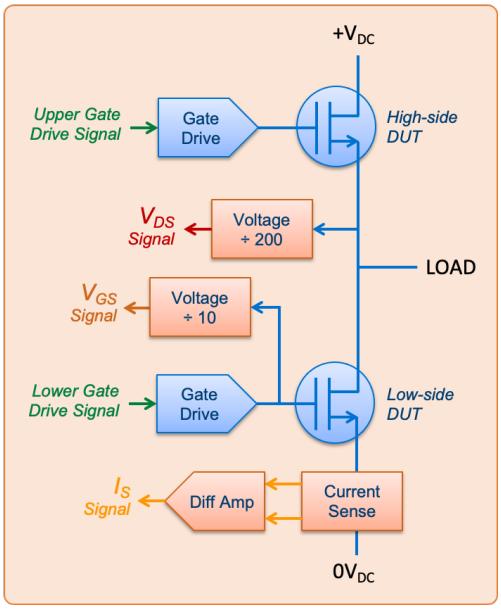


Figure 5: Schematic diagram of measurement and gate-drive circuits with transistors in a half-bridge configuration.

4.2 Experimental Setup

The experimental switching results for this paper were obtained using double pulse tests [3]. The current is ramped up through a load inductor and the device under test is then switched on and off under full voltage and current. The inductor is air cored, with a low turn-to-turn capacitance. Using on-board measurements ensures the signal path delays are matched, allowing for accurate calculation of the switching losses. Because the test is only repeated 4 times per second, there is no significant heat build-up in any of the components. The lack of heat generation means that heatsinking is not required.

4.3 Switching Waveform Comparison

Switching waveforms from the experimental tests with zero inserted gate resistances are set out in *Figure 6, Plots A-H*. In all cases the switching shows minimal overshoot voltages. No shoot-through currents are observed. In all cases, turn on proceeds as expected, with the fast devices creating a small voltage dip due to the high *di/dt* and low residual stray inductance. The upper SiC MOSFET diode reverse recovery and C_{OUT} discharge current is observed as a modest current peak at turn-on; this is seen in the GaN HEMT tests due only to C_{OUT}. Clearly the GaN HEMT and Si Coolmos devices switch very quickly with low losses. Both the Si Coolmos and SiC MOSFET turn off waveforms have some ringing. However, the GaN HEMT switches without ringing. In all cases, the upper and lower devices are identical except for the Si CoolMOS test where the upper switch device is replaced by a SiC Schottky diode. This is because the reverse recovery current of the body-diode in the CoolMOS device is unacceptably large and would hide the true switching capability. This would severely limit the performance of a hard-switched CoolMOS half-bridge in practice.

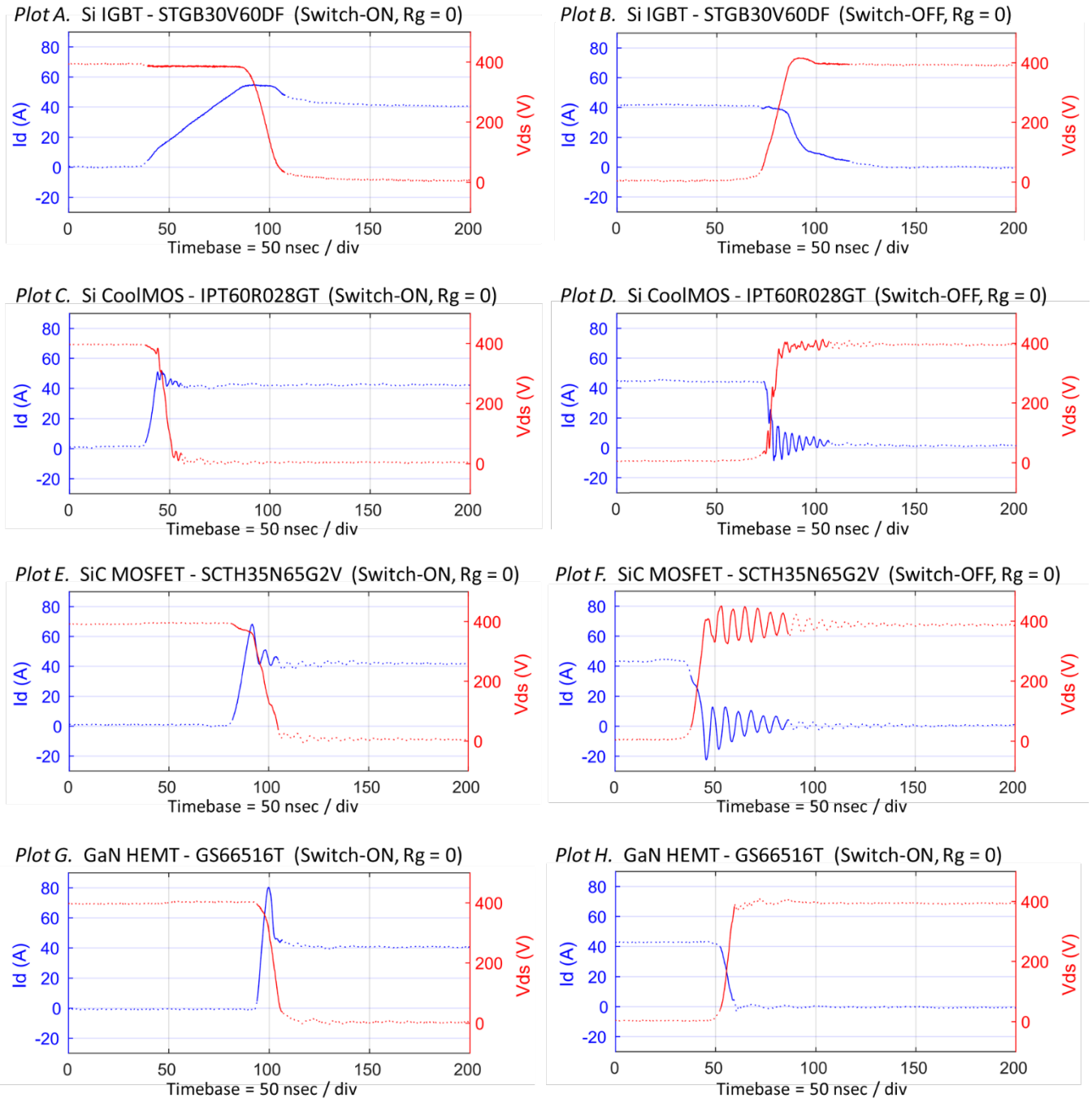


Figure 6: Switching waveforms at 0-ohms external gate resistance, for both switch-on and switch-off, shows the difference in switching performance between these four different types of power devices. The combination of fast transitions and wire-bonded packages for the CoolMOS and SiC devices results in ringing after the switch-off event, but is not sufficient to cause reliability issues or significant additional losses. The GaN and CoolMOS devices achieve very fast switching transitions.

5 Estimation of Switching Losses

When operating at high switching speeds, it is extremely difficult for the device manufacturers to fully parameterise their simulation models and perform the extensive testing required, including the many conditions that could be seen in the field. Device users also have some difficulty parameterising their circuits. Thus other options for loss estimation are also required: *Figure 2* describes the key features of idealised switching, which may be used in a geometric sense based on *dv/dt* and *di/dt*; Equations 1-8 also capture the gate plateau voltage effect, which varies with current and changes the timings of each of the four areas in *Figure 2*. Manufacturer datasheet loss values are valuable 'known points' which include the effect of the device, driver and circuit interactions. A capability to extrapolate from that point is very attractive. Note that considerable effort has been made by the manufacturer in the case of the SiC device to provide E_{ON} and E_{OFF} curves varying with current and therefore little extrapolation is needed for these devices.

Figure 7: A comparison between switching energy loss evaluation methods and experimental test results from the switching circuits developed by the authors, in relation to accuracy. All with datasheet recommended Rg unless otherwise noted.

Notes: (1) First order approximation for GaN HEMT assumes over-lapping V & I at switch-off (as seen in experimental test waveforms), halving switch-off energy losses. (2) CoolMOS simulations and test setup are with a Schottky diode in the top switch position, so reverse recovery losses of the diode are negligible, in contrast to the body diode that would be very large. (3) Where data is not available, the table is left blank. (4) Losses are per switch cycle, for switch-on + switch-off.

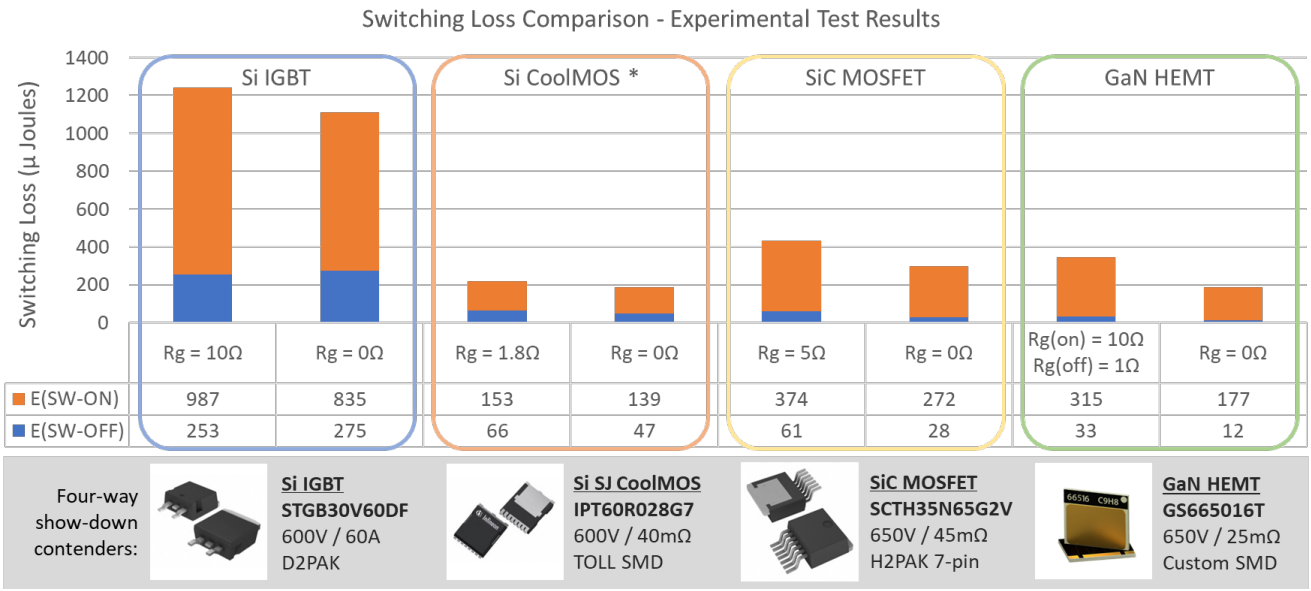


*Figure 8: Comparison of switching losses. RG is an externally fitted gate resistor. The driver and switching device have their own internal resistance that is not changed during these tests. * CoolMOS tests are single-end switching with a Schottky diode in the top switch position, otherwise the body-diode causes significant shoot-through.*

The authors used five methods to calculate losses:

1. First-order approximation: A geometric method based only on voltage rise and fall times, which can be measured in a practical, compact, low-inductance power circuit without the additional complexity of embedding measurement.
2. Vishay method: Calculation using (1)-(8).
3. Reduced complexity simulation, using simple idealised models to give insight into the most relevant device parameters.
4. Simulation using manufacturer SPICE models.
5. Datasheet extrapolation of switching energy.

A comparison of each of these methods, along with experimental results, is set out in *Figure 7, Charts A-D*. Values are with manufacturer recommended gate-resistors, unless otherwise stated.

In *Figure 7*, the Si Coolmos and SiC MOSFET device losses are captured very successfully by the first order approximations based on an assumption of the voltage and current fall and rise times being equal, *Figure 2*. This is not entirely realistic, given the waveforms in *Figure 6*, where the current slew times are a small portion of the overall t_{on} and t_{off}. This is potentially a valid approach in the case of CoolMOS, where the datasheet does not offer sufficient details to take a different approach. For CoolMOS, the simplified modelling also produces good estimations, as the transconductance is high, leading to little variation with current and therefore the voltage rise / fall dominates. For SiC, the split between V and I losses is not equal, so it is clearly most appropriate to use the equation-based linear extrapolation from the detailed curves, although directly applying equations 1-8 also works well.

In contrast, for GaN the first order approximation performs poorly, unless an allowance is made for the V and I overlap during switch-off. While the transconductance is high, the gate drive over threshold voltage is low, reducing the apparent advantage of the high transconductance. The reduced-order simulation (based on a simple transconductance amplifier model) also fails here, probably also due to an overemphasis on the gate threshold voltage, although the equation-based method works better. Linear extrapolation from measured data works well.

Simplified simulation of the IGBT is not easy, due to the stored charge in the conductivity-modulated drift region. Although the selected device is a very fast IGBT, the effects are clearly seen in *Figure 6*, with the tail current during turn-off and the low initial current gain at turn-on, as the current gain takes time to be established, leaving the IGBT to behave initially as a small-area MOSFET. Thus, the detailed simulation and first order approximation are poor at predicting the losses, although the equation-based analysis does capture the losses, which is less surprising when it is understood that the turn-on loss is the most significant and the IGBT looks more like an ideal MOSFET during this region. The linear datasheet extrapolation is less acceptable here, as the triangular turn on area A1 is very large in *Figure. 6*, making both the time and slew rates dependant on the load current being switched, which is a non-linear relationship.

6 Discussion

Figure 8 shows the data derived from the waveforms in *Figure 6*. In each case, using zero inserted gate resistance leads to a reduction in switching losses, most notably for the GaN HEMT, which implies the datasheet conditions are

conservative, possibly related to the 2 nH SCCL inductance quoted, compared to 1nH found here.

The author's latest test platform with embedded measurements and low inductance has enabled a comparison of switching devices for practical high-speed switching. The authors believe that the gate driver is now is the limiting factor in this design, i.e. that a further speed-up may be possible if the gate driver were to be improved. The GaN devices offer remarkably clean switching waveforms, likely due to low gate-to-drain capacitance. This low capacitance results in negligible ringing, and the corresponding gate-to-source capacitance of the GaN HEMT indicates there is little danger of shoot-through currents due to miller switch-on effects.

One issue which arises is related to the output capacitance of the devices. This is seen in the current measurement, where the output capacitance of the off-device in the inverter leg contributes to the switching device current, either as an increased current [2] or a reduced current during the voltage rise, *Figure 6*. The experimental results here show that even at high switching rates the voltage and current waveforms are affected by the output capacitance, but only in a minor way. The effect is similar to the use of a turn-off snubber, reducing the current in the resistive channel during turn-off. However, the energy retained in the capacitor is subsequently lost in the switching device at turn-on; although such a capacitive turn-off snubber can reduce the overall switching losses, so a trade-off could be made, its effect would be small in the results seen here. As the simulation and analyses are not yet capable of estimating losses with high accuracy, over-emphasis on this aspect is unwarranted, being of the order of 10-15 uJ for all the devices tested here.

Attempting detailed calculations of losses analytically or by simulation is possible and can be performed quickly [7]. However, the calculations are very dependent on the parameters such as the gate threshold voltage, particularly for GaN and Si CoolMOS devices, where the transconductance is high. The threshold voltage is also known to vary with temperature in most devices.

In many cases we wish to have fast loss calculations for sinewave loading. The linear interpolation between calculations [7] can be used. Here, a simplified approach of linear extrapolation with load current is quite effective assuming the DC-bus voltage remains relatively constant. We have shown that linear extrapolation from accurate experimental results is a simple and effective method of switching loss estimation in such applications. Loss estimation from the measured voltage rise time may also be used once some confidence in the overall circuit operation has been established. As switching speeds are increased with improved circuit design, the details of the gate driver become more important.

7 Conclusions

There are some considerable differences between SiC MOSFETS and GaN HEMTs in terms of their switching performance, despite both being wide bandgap devices. The authors have shown that shoot-through current would not be expected in well a crafted GaN circuit, even when switching at around twice the datasheet voltage and current slew rates. A variety of features noted in the switching waveforms for the SiC MOSFET require further analysis. If commercial readily available gate drivers are to be used with confidence in high-speed switching, they will require characterisation. It is also clear that the Si CoolMOS devices are very competitive, except for their poor body-diode behaviour. In contrast, the GaN HEMT has been shown here to have an exemplary diode-like reverse conduction and fast low loss switching in half-bridge circuits. Accurately modelling the behaviour of these devices at fast switch edge rates remains a challenge.

8 References

[1] Shelton, Edward, et al. "Low inductance switching for SiC MOSFET based power circuit." 2017 IEEE Energy Conversion Congress & Exposition 2017.

[2] Shelton, Ed, et al. "Design and measurement considerations for WBG switching circuits." 2017 19th European Conference on Power Electronics and Applications (EPE'17 Europe). IEEE, 2017.

[3] Palmer, Patrick, et al. "An experimental comparison of GaN, SiC and Si switching power devices." IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society. 2017.

[4] Siliconix, Vishay. "Power MOSFET basics: Understanding gate charge and using it to assess switching performance." Application Note (2016).

[5] Kasper, Matthias, Ralph M. Burkart, Gerald Deboy, and Johann W. Kolar. "ZVS of power MOSFETs revisited." IEEE Transactions on Power Electronics 31, no. 12 (2016): 8063-8067.

[6] Bryant, Angus T., Nii-Adotei Parker-Allotey, and Patrick R. Palmer. "The use of condition maps in the design and testing of power electronic circuits and devices." IEEE Transactions on Industry Applications 43, no. 4 (2007): 902-910.

[7] Bryant, Angus T., Philip A. Mawby, Patrick R. Palmer, Enrico Santi, and Jerry L. Hudgins. "Exploration of power device reliability using compact device models and fast electrothermal simulation." IEEE transactions on industry applications 44, no. 3 (2008): 894-903.