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Design considerations for the bottom cell in perovskite/silicon tandems: a terawatt scalability perspective†

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Perovskite/silicon tandems have smashed through the 30% efficiency barrier, which represents a promising step towards high efficiency solar modules. However, the processing used to fabricate high efficiency devices is not compatible with mass production. For this technology to be impactful in the urgent fight against climate change and be scalable to the multi-terawatt (TW) level, a shift in mindset is required when designing the silicon bottom cell. In this work, we outline the design requirements for the silicon cell, with a particular focus on the constraints imposed by industrial processing. In doing so, we discuss the type of silicon wafers used, the surface treatment, the most appropriate silicon cell architecture and the formation of metal contacts. Additionally, we frame this discussion in the context of multi-TW markets, which impose additional constraints on the processing relating to the sustainability of the materials used. The discussion herein will help to shape the design of future silicon solar cells for use in tandems, so that the LCOE of solar electricity can be driven to new lows.

Broader context

Solar photovoltaics (PV) will play a crucial role in limiting global warming by replacing traditional fossil fuel generation. To transition the energy economy at the required rate to address climate change, a rapid expansion in the production of solar PV is needed in the coming decade. Crystalline silicon solar cells currently dominate the PV market. Over the past 20 years, the efficiency of industrial silicon solar cells has steadily improved, however, the technology is approaching a fundamental limit in performance. Perovskite/silicon tandem solar cells offer a pathway to overcome these limitations. Multiple groups have demonstrated efficiencies exceeding 30%, which is a massive achievement. However, some processing approaches and materials used in high efficiency tandem demonstrations are not compatible with mass production. To have a tangible impact on climate change, these high efficiency cells must be produced on a terawatt (TW) scale. In this work, we highlight the disconnect between current research techniques on perovskite/silicon tandem solar cells and the stringent constraints imposed by large scale mass manufacturing. By doing so, we highlight some of the critical design criteria that must be considered for this technology to become a commercial reality.

1. Introduction

The urgent need to reduce CO_2 emissions to mitigate the devastating impacts of climate change requires a rapid upscaling of solar photovoltaics (PV)[1,2] Solar PV is increasingly used to replace electricity generation from fossil fuel sources and also for long-term storage *via* the formation of green hydrogen through electrolysis[3–5] In 2021, a total global cumulative production of 191 GW of solar PV was manufactured, however, predictions suggest that this must expand to at least 1 TW (1000 GW) per year by 2030 to meet the Paris agreement[6,7] Over the past 15 years, the cost of solar PV modules, as quantified in dollars per watt of power produced under peak sun light ($/$W_p$), has plummeted, reducing by a factor of 15 between 2008 and 2018.[8] These cost reductions have been driven partly by technological advancements in both manufacturing and design, partly by scaling effects, and partly by moving most of the supply chain and manufacturing to China.[9] This rapid reduction in module cost means the overall

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cost of a PV system is less dependent on the cost of the solar panel and more dependent on the other components, including the inverter, wiring and mounting systems, referred to as the balance of system (BOS). An effective way to achieve reductions in the levelized cost of electricity (LCOE) is therefore to increase the efficiency of the solar panels, which consequently reduces the BOS costs.[10] This is particularly true in scenarios where the BOS costs are area-dependent, such as in the residential market.[11]

The theoretical efficiency limit for a single junction silicon solar cell is 29.4%,[12] however, the practically achievable efficiency is lower. The world record efficiency using a silicon heterojunction architecture is 26.7% in the laboratory,[13] while an efficiency of 26.81% has been achieved in an industrial laboratory at LONGi Solar[14,15] Industrial mainstream silicon solar cells have an efficiency between about 23.5% and 24.5%, depending on cell design. The efficiency of single junction solar cells is therefore approaching a fundamental barrier, which will severely limit the potential for further reductions in LCOE. To overcome this efficiency barrier, a tandem solar cell approach is required, whereby two semiconductors with different band gap energy (E_g) are stacked together[16,17] When two materials with the ideal band gaps are combined, the limiting efficiency is increased to 46%.[18] In the near to mid future, the bottom cell in a tandem structure will be provided by a silicon solar cell, which has a E_g of 1.12 eV at 300 K. When coupled with the ideal top cell, the limiting efficiency for such a tandem device is $\sim$ 43%,[19] which significantly opens the scope for efficiency enhancements and reduced LCOE from solar PV modules. Metal halide perovskites are the leading candidate for these tandem cells with silicon. Following this may be perovskite-perovskite-silicon triple junction cells, with two perovskite absorbers of varying E_g. Such a structure would allow for further efficiency enhancements compared to a conventional single junction silicon cell, pushing the fundamental efficiency limit beyond 50%.[20]

There are several technical reasons why the leading candidate as the top cell in a tandem architecture with silicon is perovskites.[21] These include the low Urbach energy, which leads to high V_{OC} in the "radiative limit"[22–24] a remarkably high tolerance to crystalline defects, the tunability of the E_g[25,26] and strong absorption coefficient.[22,27] Additionally, the cost and material abundance indicate that perovskites may be applicable for TW scale mass production, if sufficient stability can be achieved.[28] The current efficiency record for a perovskite/silicon tandem cell is 32.5% achieved by Helmholtz-Zentrum Berlin (HZB).[29] This represents a remarkable achievement and a tangible indication that tandem cells can practically circumvent the efficiency limitations on single junction silicon solar cells. However, many of the fabrication processes used to achieve this efficiency are not compatible with mass production. Aside from using deposition methods for the perovskite absorber layers that are unscalable, such as spin-coating, factors including the area of the device, approaches to metal contact formation and the use of unsustainable materials such as indium mean that these high efficiency demonstrations are not compatible with mass production. First early products up to the multi-GW scale will be feasible with the use of indium containing ITO top transparent contacts, as is being pursued for single junction silicon heterojunction manufacturing, however, targeting the TW-scale necessitates focusing upon and transitioning to entirely sustainable materials. Although the research attention on tandem solar cells has primarily focused on the perovskite cell, in this review we analyse the design requirements from the point of view of the silicon bottom cell. The silicon PV industry has been optimizing cell design for over 30 years, however, the design criteria for making a high efficiency and low-cost single junction solar cell are very different to those for a bottom cell in a tandem architecture. As the prospects of perovskite/silicon tandems improve, the conventional approaches to designing the most efficient single junction silicon solar cell require a rethink. The design problem needs to be viewed in a new light, with new rules. The purpose of this review is to survey the current landscape of industrial single junction silicon solar cells and outline the new

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design criteria that will enable suitable bottom silicon cells in a tandem architecture.

Section 2 provides a comprehensive overview of the existing cell designs for single junction silicon solar cells. It provides a historical perspective of the evolution of cell design and outlines the different efficiency potential for each approach. It further provides context to the evolutionary design of silicon devices, which may be unfamiliar to many in the perovskite community. Section 3 discusses some fundamental design properties of perovskite/silicon tandem solar cells, including the number of terminals, perovskite polarity of the perovskite cell and interconnection scheme. Then, the design criteria for a silicon bottom cell are discussed in section 4. These include the type of silicon wafer, surface treatments, cell architecture and metallisation. In section 5, additional design considerations, including sustainability of materials and stability issues are explored.

2. Existing landscape of silicon cell architectures

A critical invention for the industrial processing of silicon solar cells was the development of screen-printed metal contacts, first reported by Spectrolab in 1975.[30] The screen-printing process refers to the application of a metal paste onto the silicon surface through a mesh screen, which is subsequently treated at high temperatures (referred to as firing) to form the metal to silicon contacts. This removes the need for a vacuum and thus facilitated the mass production of solar cells. Almost every silicon cell technology employs this screen-printing approach for contact formation, however, several cell processing routes exist. This section provides a historical perspective of the evolution of single junction silicon cell design.

The first silicon cell architecture that allowed for upscaled mass production (>50 GW per year) is the aluminium back surface field (Al-BSF) cell. A schematic diagram of the Al-BSF cell structure is shown in Fig. 1. The processing steps involved in Al-BSF manufacturing include (i) surface cleaning and wet chemical texturing of the p-type Si wafer, (ii) phosphorous doped (n^+) emitter formation by high temperature thermal diffusion, (iii) deposition of a SiN_x layer to provide surface passivation and anti-reflection coating (ARC) on the front side and (iv) screen printing contact formation, Ag fingers on the front and full-area Al on the rear. The n^+ emitter formation creates the p–n junction near the front surface, which provides carrier separation. This simple cell design was the workhorse of the PV industry until about 2018 and enabled the first wave of relatively cheap large-scale PV manufacturing. One unique aspect of this cell design is the full area metallization on the rear, as displayed in Fig. 1. This full area contact between the silicon and metal means that the dangling bonds at the silicon surface remain unpassivated, causing severe recombination losses. However, the aluminium rear contact does provide some field-effect passivation. During contact firing at elevated temperatures (typically ~ 750 °C), an alloy between the aluminium and silicon forms above the eutectic temperature of 577 °C.[31,32] The aluminium acts as a p-type dopant in silicon, forming a p^+ region at the rear surface, which is referred to as the "aluminium back surface field". This surface field provides some field-effect passivation that reduces recombination, however, due to the solubility of aluminium in silicon the doping concentrations reached are on the order of 3×10^{18} cm^{-3},[33] which is low compared to phosphorous and boron doping processes.

The main advantage of the Al-BSF design is the simplicity of the processing. The duration of the phosphorus diffusion was about 20 minutes but could be done simultaneously with

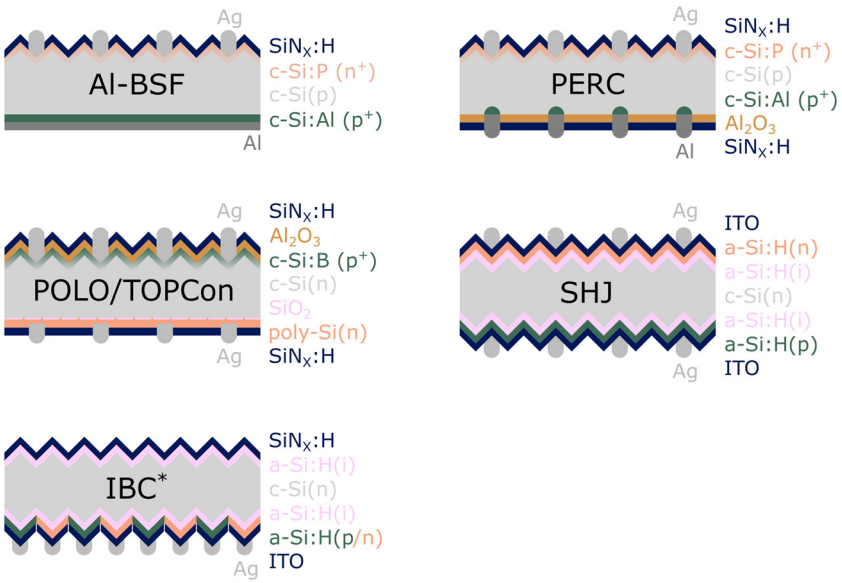

Fig. 1 Schematic illustration of different single junction crystalline silicon cell architectures. *The IBC structure is depicted with a-Si passivation, however, multiple different approaches are possible.

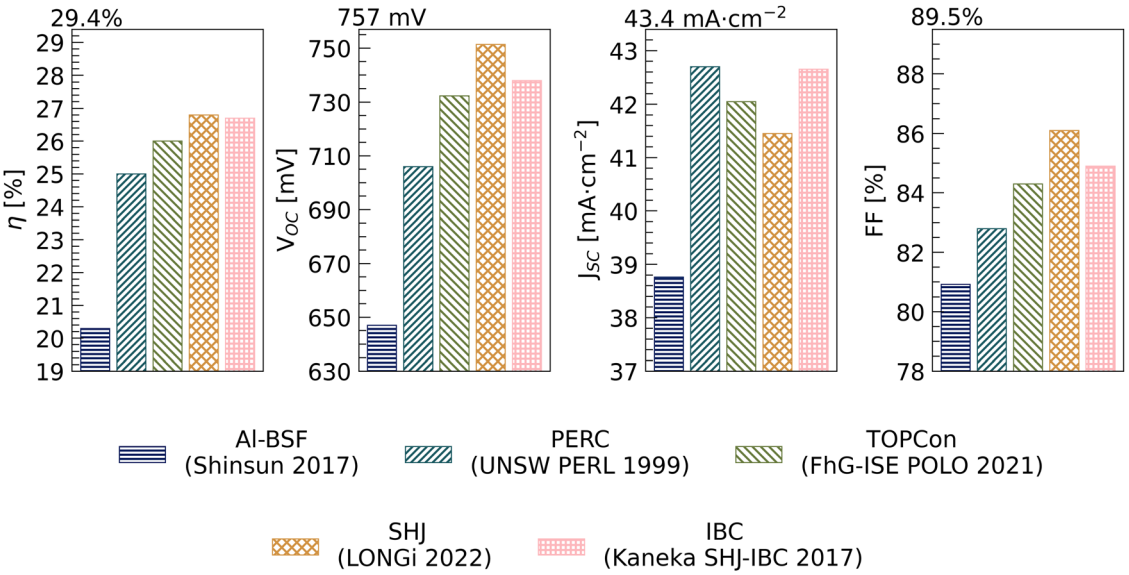

Fig. 2 Record current–voltage characteristics achieved with different crystalline silicon solar cell technologies. The values on top of each chart represent the theoretical maximum value of the corresponding parameter based on the Auger parameterization from Niewelt *et al.*[12]

approximately 2000 wafers stacked in a long boat in pairs, so only one side was diffused, all in a single tube furnace, enabling high throughput at temperatures near 850 °C. The Al-alloy at the back surface was formed within three seconds at typically ~ 750 °C during firing after screen-printing. This firing also released hydrogen from the SiN_x front layer, passivating surface and bulk defects. In this way, a n^+ layer formed a high conductivity of electrons and a low conductivity of holes towards the front contact, and *vice versa* in the p^+ layer for the rear contact. Economically, the Al-BSF cell was advantageous as the manufacturing tools converged into a single set over time. Thus, various competing tool manufacturers could sell numerous copies of the same tool to all cell manufacturers, which enabled efficient knowledge transfer between companies. The manufacturers, in turn, competed with each other *via* fine-tuning processes on their rather identical equipment, and by buying the newest equipment in as large numbers as possible to reduce prices. This also aligns with and stimulates the supply chain, for example for metal-printing pastes. In thin-film technologies, notably CdTe and $CuInSe_2$, convergence to a single set of manufacturing tools did not happen, which hindered gaining market share. This led to complete dominance of silicon solar cells in the PV market from about 2010 onwards.

Fig. 2 displays the highest efficiency achieved with each cell design. This indicates that the efficiency of Al-BSF is limited to ~20%, caused primarily by recombination at the rear that limits V_{OC} to less than 650 mV. This fundamental limitation on the efficiency led to the adoption of a new technology, referred to as 'passivated emitter and rear cell'' (PERC).[34,35]

The fundamental difference between the PERC and Al-BSF structure is the dielectric passivation on the rear surface. The main advantage of PERC is that the rear Al-BSF is reduced to small stripes, and this was beneficial because the remaining rear area, not covered by these ''local Al-BSFs'', could be effectively passivated by aluminium oxide, AlO_x, which came to PV as late as 2004. A schematic illustration of the PERC device structure is shown in Fig. 1. The first report of a high efficiency PERC cell was published by the University of New South Wales (UNSW) in 1989, then using SiO_2 (instead of AlO_x).[34,36] The dielectric layer significantly reduces the amount of recombination centres at the rear surface by passivating dangling bonds.[37–39] Additionally, the dielectric can increase the reflection of light on the rear surface, which increases the short circuit current density (J_{SC}). Initial designs incorporated a SiO_x/SiN_x stack on the rear surface. The SiO_x effectively passivates dangling bonds and the SiN_x acts as a hydrogen source, however, the intrinsic fixed charge in the SiO_x and SiN_x is not effective at providing field effect passivation for p-type surfaces. A major advancement was made when the SiO_x was replaced with AlO_x, which contains a large negative intrinsic charge.[40,41] This negative fixed charge repels minority carrier electrons at the p-type surface, further reducing recombination. This field effect passivation has led to surface recombination velocities (SRV) of <2 cm s^{-1} on p-type silicon,[40] which results in very low surface dark saturation current density (J_{0s}) on the rear surface of a PERC cell.[42] The term J_{0s} is an important metric used in silicon PV to assess the level of recombination occurring at the surfaces. As such, AlO_x has become ubiquitous within PERC cell manufacturing.

Fig. 2 displays a comparison of the record efficiency for Al-BSF and PERC. The efficiency for PERC is increased by about $4\%_{abs}$. This is primarily related to the V_{OC}, which increases from 647 mV to 708 mV due to improved rear surface passivation. The J_{SC} is also higher due to the improved rear surface reflection. In contrast to the full area contact in Al-BSF, the contacts in PERC are made by forming local openings in the dielectric layer. Compared to the standard Al-BSF cell, the

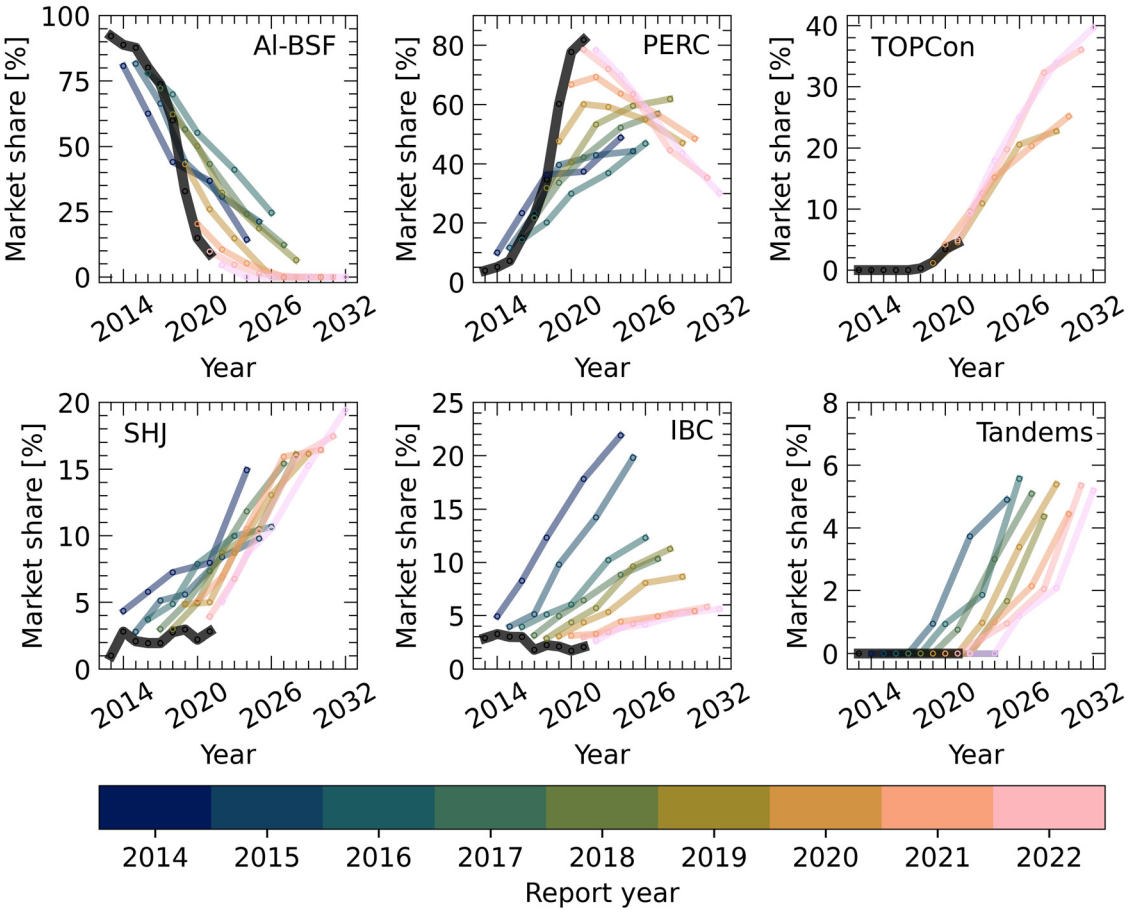

Fig. 3 Market share projections for each silicon technology based on the International Technology Roadmap for Photovoltaics (ITRPV) annual reports. The black lines represent the estimated market share of the year prior to each report, which provide an estimate of the actual market share in each year. Figure based on ref. 71.

additional processing for PERC is thus the deposition of the dielectric stack on the rear and the laser contact opening. Apart from this, the processing flow is identical to Al-BSF, which made it easily implementable into the existing mass production lines. Due to the vastly improved efficiency with little modification to the process flow, the PERC architecture has completely surpassed Al-BSF as the preferred technology. Fig. 3 displays the market share of silicon cell technologies over time, as taken from the international technology roadmap for photovoltaic (ITRPV) reports. The ITRPV report identifies trends in industrial photovoltaic manufacturing by questionnaires sent to companies and is compiled by a group of international experts associated with various aspects of PV manufacturing, including poly Si producers, cell and module manufacturers and equipment suppliers. Within the silicon community, the ITRPV reports is used as a roadmap to indicate future trends in PV manufacturing. The black line in Fig. 3 represents the estimated market share for the year prior to the report (which closely resembles actual market share), while the coloured lines display the predicted market share from various ITRPV reports.[43] Fig. 3 displays the more rapid than anticipated decline in Al-BSF in 2019. This directly correlates with a sharp increase in the market share of PERC. This increase in PERC occurred much quicker than previous projections in the ITRPV. Despite the fact that Al-BSF lines could be upgraded to PERC lines, most Al-BSF lines were decommissioned, sometimes over-night. PERC manufacturing required much cleaner factory environments to achieve higher efficiencies. Additionally, lines became more and more automated, and fabrication tools with higher throughput lowered capital expenditure (CAPEX) per GW fabrication capacity enormously. Today, PERC remains the dominant technology, accounting for $\sim$ 90% of the market share in 2022, despite past predictions in Fig. 3. The main reasons for this dominance are that mass fabrication has reduced technological diversity and complexity to a degree that inter-firm knowledge spillover has increased tremendously.[44] On top of this, cell manufacturing is primarily clustered not only in one country but in one region near Shanghai, which improves the mobility of employees and hence the inter-firm transfer of skills. The lower degree of complexity also allows R&D departments to decode and absorb external knowledge more easily.[44] Si PV has the lowest number of international patents of all the fields of PV[45] and in China, companies file national patents mainly to signal their inventiveness rather

than to protect their inventions. For these reasons, improvements penetrate the whole Si PV industry very rapidly, leading to incremental but steady development that formed the fast "moving target" of the PERC technology. This has made it difficult so far for other cell designs, discussed below, to enter the mainstream.

The dominance of PERC is related to the combination of much higher efficiency and only slightly increased manufacturing cost compared with Al-BSF. However, the V_{OC} of this approach is still limited. Historically, this was caused by the direct contact between the metal and semiconductor. In regions where the metal directly contacts the silicon, dangling bonds remain unpassivated, so the J_{0s} in these regions (referred to as $J_{0s,met}$) is much higher than in non-contacted regions. This caused significant recombination in early cell designs. However, in industrial PERC cells, the fraction of metal regions is small ($\sim$2%) and the $J_{0s,met}$ has been drastically reduced due to optimisation of the metal pastes.[46,47] Thus, the impact of recombination in contacted regions on V_{OC} potential is diminishing. Instead, the V_{OC} in PERC solar cells is primarily limited by recombination losses in the n^+ emitter region. This is due to a rather heavy phosphorus diffusion, causing Auger recombination and surface recombination.[48–50]

To overcome this recombination, the contacts should be designed such that they provide the dual purpose of passivating the surface and extracting charge, while removing the need for a heavy diffusion in the c-Si. Such a design is referred to as a 'passivating contact', this area of research has received immense interest over the past decade with the aim of overcoming the efficiency limitations of PERC cells.[51–53] Materials investigated to achieve passivating contacts include thin oxide/doped polysilicon,[54] amorphous silicon[55] and various metal oxides.[56,57] Of these, only the combination of a thin silicon oxide coated with a heavily doped polysilicon layer has been intensely studied as a passivating contact for industrial silicon solar cells.[58,59] This passivation approach removes the need for a heavy diffusion in the following way. A tunnelling oxide on the wafer surface only allows one type of charge carrier to pass because there is a highly doped polycrystalline silicon layer behind, which pins the Fermi level to a band, which, in turn, is contacted by metal. Since the blocked charge carrier type cannot reach the metal contact, recombination at the Si/metal interface does not affect cell performance. Additionally, the tunnelling layer can be very well passivated. The heavy doping of the poly-layer only slightly diffuses into the wafer, so this contact can be applied over the whole cell area. Research into this contact approach first appeared in the 1980s,[60,61] however, the incorporation into a silicon solar cell re-emerged in 2014.[54,62] Such a structure is referred to as a tunnel oxide passivating contact (TOPCon) solar cell.

A schematic illustration of the TOPCon cell architecture is displayed in Fig. 1. Silicon cells adopting this contacting scheme may also be referred to as polysilicon-on-oxide (POLO), since the current transport can occur *via* pin-holes in the interfacial oxide enabling direct contact between the doped polycrystalline layer and the underlying Si wafer - not exclusively tunnelling – depending on the thickness of the interfacial oxide.[39,63–65] TOPCon cells are typically fabricated on an n-type wafer, with the thin oxide and n^+ doped polysilicon forming the n-type contact on the rear surface. This contact is also coated with a hydrogen-containing dielectric which releases hydrogen during contact firing and acts as either as a reflector or ARC for bifacial cell structures. The n^+ doped TOPCon rear contact serves as an excellent passivating contact, with reported $J_{0s} < 3$ fA cm^{-2} and corresponding resistivities <3 mΩ cm^2.[54,66,67] The surface passivation is controlled by the combination of chemical passivation of defects at the c-Si/SiO_x interface, as well as field effect passivation provided by the heavily doped poly silicon layer.

In contrast to PERC, which contains localized rear contacts, the rear surface contact is full area, which has the additional impact of avoiding current crowding on the rear.[68] In a TOPCon solar cell, the thickness of the SiO_x is carefully controlled to $\sim$1.3 nm such that tunnelling of carriers can occur. To promote the tunnelling current, the thickness must be precisely controlled. Alternatively, a slightly thicker oxide may be employed and other current transport mechanisms, such as conduction through pinholes, can be utilized.[63] This partially reduces the stringent thickness control required to facilitate tunnelling, however, high temperature treatments are required to amplify alternative conduction pathways.[64] The efficiency potential for TOPCon cells is higher than PERC. Fig. 2 shows that demonstrated efficiency for TOPCon has reached 26%. This is related to the higher V_{OC} potential of 720 mV for the following reasons. Firstly, the rear passivating contact and the front boron diffusion have both lower J_{0s} values than front and rear of PERC. Secondly, the base doping can be lower than in PERC due to the higher electron than hole mobility, which enables high bulk excess carrier lifetimes. A concomitant increase in FF is observed, related to the higher pseudo FF (pFF) caused by the higher V_{OC}[69] and by a relatively higher share of Auger in the recombination processes.[70]

In mass production, TOPCon cells are typically $\sim$24.5% efficient, which is about 1%$_{abs}$ more than PERC. However, it is important to note that TOPCon cells – despite becoming mainstream – are limited by the front surface. On the one hand, boron-diffused surfaces have higher recombination losses than phosphorus-diffused surfaces. One the other hand, recombination at the front contact is very high because the boron concentration is lower than phosphorus concentration in PERC, due to lower dopant solubility. These factors will limit the scope for further efficiency enhancements in industrial manufacturing, provided the manufacturing process should remain relatively simple (the 26% efficient cells in Fig. 2 were achieved with elaborate processing). Adding a passivating contact to the front side currently appears to be difficult because even a very thin poly Si layer would cause significant parasitic absorption at the front, so the passivating contact must be restricted to the front finger area, which increases processing complexity.

TOPCon cells are currently becoming mainstream despite manufacturers' lower margins than with PERC. This may be

surprising but is driven by two key factors. First, the PV industry is currently expanding by near 50% per annum, so tools are bought in large quantities. Investing such resources into PERC is risky, as the efficiency potential is close to saturation. Second, once TOPCon is dominating the market, PERC lines will probably not be upgradable to TOPCon, even though only two new tools need to be added and most lines have reserved floor space for this. This is expected to be so because the other tools have improved in throughput (up to 10 000 wafers per hour) and in quality, so too many tools would have to be upgraded. However, the current introduction of TOPCon cells into mainstream poses risks considering that TOPCon efficiency may be hard to improve further due to limitations at the front surface. This is in sharp contrast to PERC, which has improved by $\sim 3.5\%_{abs}$ since becoming the dominant commercial technology.

An alternative approach to form a passivating contact is hydrogenated amorphous silicon (a-Si:H).[55,72] This can provide excellent chemical passivation at the c-Si/a-Si:H interface, due to the concentration of hydrogen in the film, which passivates dangling bonds, as well as achieving good conduction through the a-Si layers. Passivation with a-Si:H is incorporated into a cell *via* the silicon heterojunction (SHJ) architecture, a schematic diagram of a typical SHJ solar cell is shown in Fig. 1. The early development of this cell design was driven by Sanyo (acquired by Panasonic in 2009), who championed this approach in the 1990s.[73,74] In contrast to Al-BSF, PERC and TOPCon, SHJ cells do not contain a thermal diffusion of dopants into the c-Si to form a p–n junction within the silicon itself (often referred to as a 'homojunction'). Instead, the carrier selectivity is determined by doping in the a-Si layers. Due to the removal of the thermal diffusion of dopants and firing of metal pastes to form the contacts, the temperature range of SHJ manufacturing is typically <230 °C, which is much lower than PERC and TOPCon. As a consequence, low temperature screen printed silver pastes are used for contact formation. In the initial iteration of the technology, the doped a-Si layers were deposited directly onto the c-Si. However, the defect density in these doped layers is large, thus, the surface passivation was ineffective and devices with this configuration did not achieve high V_{OC}. To overcome this issue, a thin undoped or 'intrinsic' layer (a-Si:H(i))) is deposited on the surface to provide excellent surface passivation.[75] The large hydrogen concentration in these films facilitates very effective chemical passivation, where the dangling silicon bonds at the surface are saturated with atomic hydrogen. This is characterized by a reduction in the density of interfacial defect states, D_{it}.[75,76] In addition to this effective surface passivation, the lack of heavy doping at the c-Si surface reduces the constraints placed by Auger recombination and thus V_{OC} as high as 750 mV has been achieved with SHJ cell architectures.[77,78] In a standard p–n junction, the lateral conduction of carriers occurs in c-Si, either in the emitter or the bulk. However, due to the defect density in the doped a-Si causing relatively low mobility, the lateral conductivity is poor. Therefore, it is necessary to include a transparent conducting oxide (TCO) to allow for lateral conduction of carriers to the contact metal fingers, the TCO is displayed in Fig. 1. The achievable efficiency for the SHJ architecture is better than all purely crystalline Si architectures. As shown in Fig. 2, the record efficiency of 26.8% was achieved with a SHJ structure. These excellent efficiencies are caused by the high V_{OC} (~ 750 mV) as well as exceptionally high FF ($\sim 86\%$). The efficiency values are higher than all other Si technologies and represent a significant increase compared with PERC. However, despite this clear efficiency advantage, SHJ cells have still yet to capture a large share of the market. Fig. 3 displays the forecasted increases in the SHJ market share which have yet to be realized, with the current market share at $\sim 2\%$. One of the main barriers to market entry has been the larger capital expenditure for a SHJ production line, compared to PERC and TOPCon, due to both expensive manufacturing tools and expensive safety infrastructure for the gasses. Additionally, the intrinsic a-Si layer cannot be deposited in a PECVD tube, where wafers are stacked in boats, but must be laid side by side. This prevents larger wafers from helping to achieve higher throughput. Investments in SHJ lines were considered risky because the manufacturing tools are incompatible with PERC and TOPCon lines, so downgrading to cheaper cell designs is impossible. However, recently, the situation changed. Because TOPCon cells are limited by the front contact, which is not passivating, and there are no upgrades to TOPCon in immediate sight, this has piqued manufacturing interest in SHJ as the next upgrade. Chinese tool manufacturers took on a simplified engineering approach in tool development and are reducing CAPEX over time. The promise of high efficiency has sparked significant commercial interest, with companies such as LONGi, Tongwei and Hevel Solar producing SHJ and companies such as Meyer Burger and Tri Sun establishing new heterojunction production capacity in Europe. The schematic diagram shown in Fig. 1 depicts the standard industrial approach to SHJ manufacturing. This includes a thin intrinsic layer and doped n^+ a-Si layer on the front surface, covered with ITO for lateral conduction. The rear surface contains a stack of intrinsic and p^+ doped a-Si, coated with ITO. Over the past couple of years, concerted efforts have been made to improve the cell design. In particular, intense research efforts have aimed to reduce the parasitic absorption losses. The presence of the intrinsic and doped a-Si layers, as well as the ITO, causes severe parasitic absorption on the front surface, which limits the J_{SC}.[79] As such, SHJ cells with the standard cell architecture shown in Fig. 1 typically have J_{SC} values limited to approximately 38 mA cm^{-2}. This is much lower than industrial PERC cells, which typically achieve ~ 41 mA cm^{-2} due to the dielectric ARC on the front surface. One approach to reduce such parasitic absorption losses is to replace the n^+ doped a-Si on the front with an alternative that has less absorption at short wavelengths. Examples of this include ZnO as an electron selective contact and MoO_x as a hole selective contact.[80–82] The ITO layer contributes to parasitic losses and is also required on both the front and rear surface. This layer is additionally problematic due to the scarcity of indium, which will severely limit the upscaled manufacturing of SHJ cells (this is discussed at length in

Section 5.1). As such, the development of 'TCO free' SHJ cell designs are gaining interest.[83]

The final cell design detailed in Fig. 1 is the interdigitated back contact (IBC) design. The unique aspect of IBC cells is the lack of contacts on the front surface. Both p- and n-type contacts are located on the rear surface in an 'interdigitated' arrangement. This means there are no optical losses on the front surface due to the reflection of light from metal contacts. However, the lateral collection of excess carriers at the rear side is limited to 'electronic shading'. Hence, this architecture offers the potential for high J_{SC}. IBC cells were initially designed for concentrator applications, where the light intensity is much larger than 1 sun.[84] For this high light intensity, resistive losses, particularly related to the sheet resistance of the front emitter in other cell architectures, are more problematic. Placing all contacts on the rear, where they can occupy a much larger area, significantly reduces the resistive losses. The p- and n- contacts on the rear can be formed *via* various passivating contact methods. For example, the previous world record efficiency of 26.7% for a single junction silicon cell was achieved by using an IBC architecture with a-Si passivation, as with the SHJ design. The performance parameters are displayed in Fig. 2. Note the much higher J_{SC} value compared with the standard SHJ cell design. A POLO style approach can also be used, an efficiency of 26.1% was achieved with a POLO IBC architecture.[64] Although this contacting scheme provides benefits, it also modifies some of the design requirements. The tolerable surface passivation on the front surface is more stringent for IBC, as all carriers need to be transported to the rear. In the same way, the bulk lifetime of the silicon wafer must be high to allow for sufficient carrier diffusion and collection at the rear. Having contacts with both polarities on the rear increases the complexity and cost of processing, due to the precise patterning required. This increased complexity has limited the commercial uptake of IBC cells. As shown in Fig. 3, the predicted market uptake of IBC cells has vastly outweighed the reality, which closely reflects the projections for SHJ cells. Despite the small market, US manufacturer Sunpower has maintained leadership in the commercial production of IBC cells, demonstrating an efficiency of 25% suitable for area-constrained sectors.

3. Tandem design

3.1. Architecture (two-terminal (2T) *vs.* four-terminal (4T))

Tandem cells can be fabricated with a variety of architectures. The conceptually simplest design from a manufacturing viewpoint is four-terminal (4T), where two individual cells, made with different E_g, are stacked together. A schematic illustration of a 4T architecture is shown in Fig. 4a. In this arrangement, the cells are optically coupled, meaning that the incident light is shared between the two cells. However, the cells each have their own positive and negative contact and thus are not electrically coupled. Each individual cell will generate an I–V curve that is electrically independent of the other, although the incident light is shared between the cells. Due to the physical separation of the fabrication of each cell, the processing conditions can be optimised independently, which reduces the constraints on cell processing. The fact the cells share the same light source does mean that at least three transparent contacts are required, so that the bottom cell can absorb light. This places a practical limit on the achievable efficiency. Although the processing is less constrained, 4T tandem cells are fundamentally different to a single junction silicon cell, as there are now four contacts. This makes the formation of modules and BOS design more difficult. Due to this difficulty, less research has focused on 4T designs as a viable approach for commercial module manufacturing.

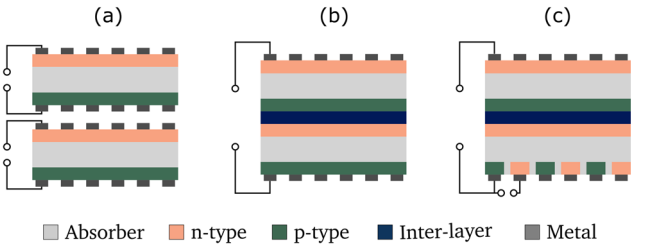

Fig. 4 Schematics of the different interconnection schemes for tandem solar cells. (a) four terminals, (b) three terminals and (c) two terminals. Please note that for simplicity the same contact order was used (p-type contact on the rear, n-type contact on the front).

An alternative approach, which seems more favourable for module manufacturing, is the two -terminal (2T) approach. A schematic of a 2T design is shown in Fig. 4b, which shows that the cell contains only one positive and one negative contact. In this case, the top cell and bottom cell must be fabricated together to make one combined system, this approach is often referred to as 'monolithic'. This is much more favourable for module formation and system design, as the contact scheme mimics that of a single junction silicon cell. Additionally, only one transparent contact is required, which can reduce parasitic absorption losses. Furthermore, since the overall current density generated by the tandem cell is approximately half that of the single junction silicon cell, the conductivity of the transparent contact can be reduced by a factor of 4, for the same resistive power losses. However, the fabrication of both cells onto one substrate in a monolithic fashion introduces many new design constraints that are not present in the 4T architecture. First, the processing sequences used, including the temperature, use of solvents and surface preparation, must be compatible between the two individual cells. Second, due to the electrical coupling, the series connection means that the overall photocurrent is limited by the lowest sub-cell current. To maximise efficiency, the current must be matched between the two cells. Therefore, the E_g and thickness of the absorbers, parasitic absorption within non-active layers and internal reflections and interference between layers of varying refractive index must be carefully controlled. The subcell photocurrent limitations imposed by electrical coupling result in a narrower optimum bandgap for the top cell than 4T counterparts.[19]

To overcome some of these drawbacks of 2T and 4T designs, a three-terminal (3T) configuration is introduced,[85] as shown in

Fig. 4c. In this configuration, an IBC architecture is utilised for the Si bottom cell. The top cell is grown monolithically, which reduces the need for two TCOs in the top cell, as with the 4T case. This reduces the current loss due to parasitic absorption at the interface layer. This structure also alleviates the need for precise current matching conditions, which is a major design constraint for 2T design. The third terminal allows the additional current from either cell to be extracted.[86] This also means that the cell is robust against spectral variations that occur throughout the day at different location on earth. However, for 3T, a complexity arises on the fact that it requires an IBC configuration for the bottom cell. From an industrial point of view, this may be less of a problem now than in the past, since more companies are now producing IBC cells with simpler processing steps. Another aspect of this 3T idea is modifying the 4T configuration to 3T connection. As previously mentioned, from module manufacturing point of view, the additional terminal adds significant cost to the BOS component. If the rear contacts of the two cells are connected, this will result in 3T configuration, while still maintaining the simplicity of the individual cell fabrication process as well as the reduced constraints of current matching.

3.2. Perovskite configuration

Perovskite solar cells originate from the dye-sensitized solar cell community. Perovskite absorbers were first employed to sensitize a mesoporous n-type titania semiconductor to visible light.[87] Switching the liquid junction electrolyte to the benchmark hole transport material [2,2′,7,7′-tetrakis(*N*,*N*-di-*p*-methoxyphenyl-amine)9,9′-spirobifluorene] (spiro-OMeTAD) pushed efficiency beyond 10% and eliminated deleterious stability issues arising from the liquid electrolyte.[88,89] A key development was the elimination of the mesoporous scaffold,[90–92] termed a planar heterojunction device. This innovation opened up the possibility of using planar contacts made with organic n- and p-type materials developed by the organic electronics community. Efficient devices were soon demonstrated on top of p-type layers in an 'inverted polarity' architecture.[93,94] Inverted polarity refers to a device structure with the p-type contact on the bottom (sun-facing side), rather than the n-type contact on the bottom. To avoid confusion, the community adopted the terminology n–i–p to designate a device where the 'intrinsic' perovskite is deposited atop an n-type layer, then coated with a p-type layer (Fig. 5(a)). The p–i–n configuration is used where the perovskite is deposited on the p-type layer before an n-type layer completes the stack (Fig. 5(c)). Thus, the configuration n–i–p or p–i–n designates the sequence of fabrication, regardless of the sun-facing side (Fig. 5(b) and (d), respectively). In a single junction device, where the layers are all processed on a TCO-coated substrate, this configuration also represents the pathway of incident light. However, this is reversed in a 2T tandem with silicon, since the device is completed with a top TCO, rather than built upon one. A detailed review of the early evolutionary development of perovskite architectures is beyond the scope of this manuscript, and the keen reader is directed to the following reviews.[95,96]

The first perovskite/silicon tandem solar cell featured an n–i–p configuration using the benchmark titania and spiro-OMeTAD n- and p- charge transport layers, respectively.[97] Since sunlight is incident on the p-type side, contrary to the standard n-type sun facing direction, the optical properties of the HTL become critical. This architecture suffers from parasitic absorption from the HTL that is not experienced in single junction configurations, which limits the conversion efficiency.[11,21] Single junction devices with n–i–p configurations have historically had higher efficiencies than their p–i–n counterparts. Due to the reactivity of the perovskite layer, the charge transport layers deposited atop the perovskite are exclusively organic, since they can be deposited by soft means, such as solution processing and thermal evaporation. However, the absence of an organic HTL with good transparency over the entire solar spectrum required to absorb in both sub-cells, motivated the development of p–i–n perovskite solar cells for tandem applications,[98] where optically thin layers of the n-type C_{60} have little parasitic absorption.

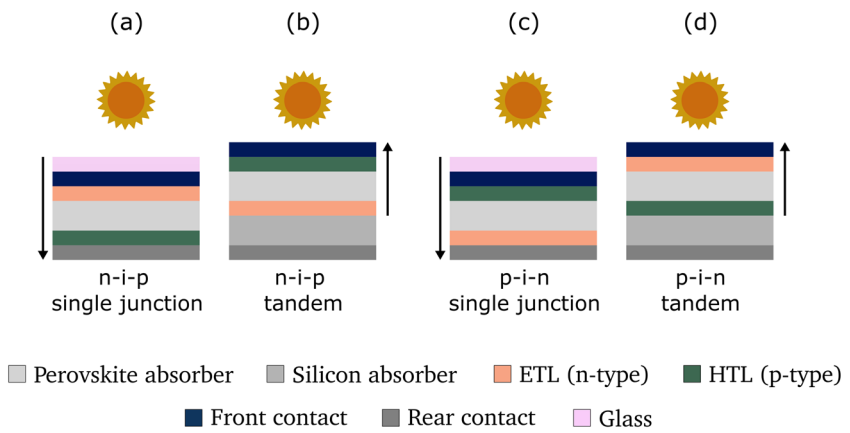

Fig. 5 (a) n-i-p perovskite single junction solar cell where the n-type contact faces the sun, (b) n-i-p perovskite/silicon tandem solar cell where the p-type contact faces the sun, (c) p-i-n perovskite single junction solar cell where the p-type contact faces the sun, (d) p-i-n perovskite/silicon tandem solar cell where the n-type contact faces the sun.

Today, p–i–n is the polarity of choice in multiple demonstrations of perovskite/silicon tandem solar cells with conversion efficiencies above 28%, including the previous world record of 31.25% and presumably the present world record of 32.5%. Yet, Aydin *et al.* have recently demonstrated conversion efficiencies exceeding 27% for an n-i-p perovskite/silicon solar cell, employing a very thin organic p-type layer in combination with a vanadium oxide p-type "buffer layer".[99] In a perovskite/silicon tandem structure, the front perovskite cell produces the larger fraction of the power. Therefore, one should choose the perovskite polarity that favours the perovskite top cell. However, the choice of perovskite polarity, silicon wafer polarity and p–n junction location in the silicon bottom-cell are interconnected. The wafer type determines the junction location for a given perovskite polarity. Similarly, selecting the junction location will determine the silicon wafer polarity required.

In traditional p-type silicon homojunction solar cells, the p–n junction is located at the front. The same was observed in the first n-type SHJ solar cells. However, the high quality of n-type silicon wafers used in SHJ solar cells enabled a shift of the junction to the rear of such devices. Due to continuous improvement in the carrier lifetime of p-type silicon wafers, the same could happen to p-type homojunction silicon solar cells.

Switching to a rear-junction configuration can be advantageous in a single junction silicon solar cell, as the electrical requirements of the front surface layers are relaxed. This provides room for minimising optical and recombination losses in these layers. However, the ideal silicon bottom-cell p–n junction location is not yet defined for perovskite/silicon tandem solar cells.

Recent work from Ballif *et al.* suggested that a front-junction configuration minimises the negative impact that shunts in the perovskite top-cell have on the conversion efficiency of the complete tandem device[100]. This was evidenced in their work, where p–i–n perovskite/silicon tandem solar cells were fabricated with p- and n-type FZ silicon wafers featuring poly-Si carrier selective contacts. Combining a p-type silicon wafer with the p–i–n perovskite structure (hence a front junction) resulted in a peak-conversion efficiency of ~28%. On the other hand, when an n-type silicon wafer was used (hence a rear junction), they observed a peak conversion efficiency of only ~24%. This example illustrates the importance of considering the relationship between perovskite polarity, silicon wafer polarity and p–n junction location when designing perovskite/silicon tandem solar cells.

3.3. Interconnection schemes in monolithic tandems

As discussed earlier, 2T monolithic tandem cells are composed of two sub-cells, each with a positive and negative side, however, the total device only has one positive and one negative terminal. Therefore, to ensure current continuity across the whole device, one type of carrier from the top cell must recombine with the opposite carrier type from the bottom cell. This occurs at the interface between the two cells. In 2T perovskite/silicon tandem solar cells, three main types of interconnection approaches have been explored. These are displayed schematically in Fig. 6.

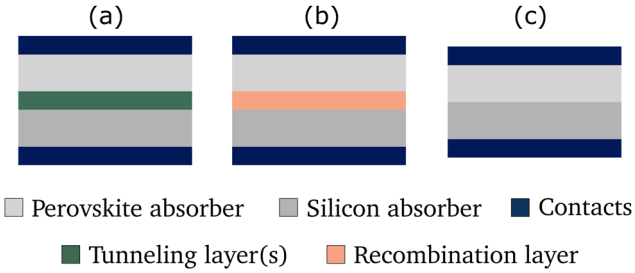

Fig. 6 Different tandem interconnection arrangements (a) tunnelling layer, (b) recombination layer, (c) interconnection free.

The first approach is a heavily doped tunnel junction, as displayed in Fig. 6(a). The first demonstration of a tunnelling diode was presented in 1958 by degeneratively doping a germanium p–n junction.[101] Quantum mechanical tunnelling refers to the movement of electrons through classically forbidden regions. This is facilitated by heavily doping both the p- and n-side, such that the depletion region width is significantly reduced. In a perovskite/silicon tandem under illumination, a constant supply of electrons and holes will flow to this junction and annihilate *via* interband tunnelling. For a p–i–n perovskite arrangement, holes are supplied by the perovskite while electrons are supplied by the silicon cell).[102] The physical principles of this process in tandems are comprehensively reviewed in ref. 102. This tunnel junction approach was commonly used in III–V tandem structures, which contain degenerative doping and atomically sharp interfaces. Mailoa *et al.* took this approach in the first demonstrations of a 2T perovskite/silicon tandem solar cells.[97] The tunnel junction was formed by depositing a n-doped a-Si layer *via* PECVD on top of a p^{++} doped silicon emitter. The a-Si was subsequently annealed at 680 °C for 15 mins to activate the dopants. This device architecture used an n-i-p perovskite arrangement, therefore electrons were injected from the perovskite through the TiO_2 electron transport layer towards the interconnection, while holes were injected from the p^{++} silicon emitter.

Efficient tunnelling in such structures requires an interface between two degenerately doped regions. In some cell architectures, this is not always achievable. In this case, it is possible to enhance recombination of majority carriers by the insertion of a 'recombination layer'.[103,104] This is achieved by the formation of a 'metallic' layer in between the silicon and perovskite solar cells, TCOs such as ITO are typically used. This is displayed schematically in Fig. 6b. In essence, the recombination that occurs is similar to Shockley Read Hall recombination in the silicon bulk, however, it involves majority carriers from two different absorbers, rather than a majority and minority carrier within silicon. In principle, this could also be achieved by the inclusion of an ultrathin metal layer. This interconnection approach is particularly suited for SHJ cells, as they already contain a TCO on the front surface, which is already optimised for a low contact resistivity. The main drawback of this

approach is the parasitic absorption introduced by the addition of the TCO.[97,98] Additionally, the sheet resistance of this added conductor must be carefully considered. If the overlying perovskite top cell suffers from severe shunting due to pinhole formation (for example due to a textured surface), the sheet resistance of the layer must remain high to avoid shunting[102]. Notably however, since conductivity in the lateral plane is not required, nor desired, very thin ($\sim$10 nm) or low conductivity ($\sim$1000 Ω $\square^{-1}$) TCOs are ideal, and hence additional parasitic absorption losses can be minimised. Using this approach, Zheng *et al.* recently reported a conversion efficiency of 27.2% (FF = 82.4%) for perovskite/silicon tandem solar cell featuring a 1.7 nm-thick sputtered ITO interconnection layer.[105] Interestingly, the authors observed non-complete coverage of the silicon bottom cell surface for thinner sputtered ITO layers.

A third approach is the so-called 'interlayer-free' design, in which the top cell and bottom cell are directly connected. This is displayed in Fig. 6c. The advantages of this approach include, (i) possible simplified device processing, (ii) avoiding additional parasitic absorption and (iii) minimising shunting issues by removing the conductive TCO. However, to satisfy the conditions of current continuity, carriers must be able to recombine at the interface. Shen *et al.* demonstrated an interlayer-free tandem cell approach by depositing n-type TiO_2 by ALD on top of underlying p^+ silicon.[106] This TiO_2 layer additionally acted as the n-type layer for an n–i–p perovskite top cell. Low contact resistance was attained at the interface, leading to an efficiency of 24.1% with a passivating contact silicon bottom cell.

4. Silicon bottom cell design

4.1. Silicon wafer type

There are many considerations when choosing the most appropriate silicon wafer type for each cell technology. The first is the crystal structure. The simplest and lowest cost approach to silicon wafer fabrication is directional solidification to form multi-crystalline silicon (mc-Si).[107] In this approach, molten silicon in a crucible is solidified to form a brick. As implied by the name, this wafering technique produces silicon wafers that do not contain the same crystal orientation, instead, the material contains small crystal grains of varying size and orientation. This reduces the material quality, due to the amount of structural defects and grain boundaries, which can be electrically active and act as trap sites for metallic impurities.[108] Thus, although mc-Si wafers are significantly cheaper to produce, the material quality is low, which limits the efficiency of subsequent solar cells. Nevertheless, until 2017 mc-Si wafers dominated the market. One reason for the initial dominance of mc-Si was the fact that the surface passivation of industrial cells was not well developed, meaning the efficiency was less sensitive to bulk recombination. This allowed for tolerance of lower quality silicon to be used. However, as surface passivation techniques have rapidly improved, the requirements on the bulk quality of the silicon have become more stringent.[109] An alternative approach is to use a seed crystal to form a monocrystalline silicon ingot, which is then sliced into wafers. The most popular technique to do so was developed in 1917 by Jan Czochralski and is referred to as Czochralski (Cz) growth.[110] In Cz growth, a pure seed crystal with a particular crystal orientation is dipped into molten silicon, held by a metal pulling rod. As the seed is slowly removed and rotated, a cylindrical silicon ingot is formed that has a uniform crystal orientation, matching that of the seed.[111,112] This monocrystalline silicon contains significantly fewer structural defects and can thus achieve higher carrier lifetimes. Since 2018, Cz became the dominant wafer type, owing to significant cost reductions in making Cz ingots and wafers. Monocrystalline silicon wafers can also be formed using the 'float zone' (FZ) process. In float zone manufacturing, a molten region is made in a Cz silicon ingot by a moving a heating coil along the axis and surrounding a section of the silicon ingot. Impurities and dislocations are preferentially segregated into the molten region, which is moved to the top of the ingot and subsequently removed. In this way, very high purity monocrystalline material, with exceptionally high bulk lifetime, can be formed.[113] However, the additional cost of FZ means it is not cost competitive for commercial cell manufacturing.

The second consideration is the doping polarity of the wafer. Silicon wafers can either be p-type, by doping with either boron or gallium, or n-type, by doping with phosphorous. Historically, silicon solar cells have been fabricated with p-type wafers. Although p-type wafers displayed poorer electrical properties, they exhibited better tolerance to radiation experienced in space, extra-terrestrial applications as such were the primary applications during the 1960s.[114,115] There are several technical factors that also make p-type advantageous for manufacture of industrial cells. First, the segregation coefficient of boron at the silicon liquid–solid interface is much higher than phosphorous.[116] This means that the doping concentration of a boron-doped p-type wafers is much more uniform across the ingot than for phosphorous doped n-type, allowing for greater ingot utilisation within the required resistivity range. Second, minority carriers in p-type are electrons, which have a higher mobility than holes by approximately a factor of 3 (depending on the doping level).[115] This can relax the requirements for the bulk diffusion length compared to n-type. Additionally, forming an n-type emitter in p-type silicon is less technically challenging than the formation of a boron emitter. As such, using p-type wafers in a PERC architecture allows for more emitter optimisation through the formation of a selective emitter.

From a fundamental viewpoint, the upper practical efficiency limit is similar for p-type and n-type wafers,[12] however, in practice, n-type Cz wafers typically exhibit better material properties. The wafer polarity influences subsequent cell processing. For example, PERC cells are typically processed with p-type wafers. Emitter formation therefore requires an n-type region at the surface, which is achieved by a thermal diffusion with a phosphorous source. Instead, in TOPCon cells n-type

wafers are typically required, which means that the emitter formation requires a p-type region, formed by a boron diffusion. Thermal diffusion with boron requires higher temperatures and longer times and is thus less desirable for production. The primary reason for the continued dominance of p-type wafers is the cost. In 2021, LONGi stated that the cost of n-type Cz wafers is 10% higher than p-type Cz. The increased cost for n-type is related to increased brick costs, due to the fewer times the crucible can be re-used, lower yields and stricter impurity requirements.[117]

Another critical wafer property is the bulk lifetime. This determines how well carriers generated in the bulk can be transported to the contacts for collection and thus has a large impact on the cell performance. The bulk lifetime provides a measure of the amount of recombination-active defects in the silicon wafer. Crystallographic defects can cause recombination in the bulk, thus, mc-Si wafers typically have lower lifetimes, which limits cell efficiency. Although Cz wafers have significantly less crystallographic defects, impurities in the bulk can also cause undesirable recombination. Thus, Cz wafers can have bulk lifetimes spanning several orders of magnitude, depending on the concentration of contaminants. The unintentional incorporation of oxygen during ingot formation can lead to the formation of boron–oxygen (BO) defects in boron-doped p-type wafers. The formation of BO defects under illumination has caused significant loss in V_{OC} and efficiency for p-type solar cells.[118–120] This can be overcome by replacing boron with gallium as the p-type dopant.[121–123] Additionally, unwanted oxygen in the wafer can form oxygen precipitates or thermal donors when processed at elevated temperatures.[111,124] These defects appear as circular rings and can manifest in both p-type and n-type wafers.[125] Metallic impurities, such as iron, copper, chromium and aluminium can also be incorporated into the wafer during manufacturing.[108] These impurities can cause undesirable recombination and can also form recombination-active complexes, such as Fe–B pairs. Thus, there are many factors that can influence bulk recombination and cause reductions in the bulk lifetime. When considering the bottom silicon cell in a tandem structure, it is important to acknowledge that the processing route employed for the silicon cell can modify bulk lifetime. For high temperature processing routes, such as PERC and TOPCon, several processes inherent in the processing can cause the bulk quality to improve. Defect engineering can occur *via* two processes, (i) high temperature diffusions can migrate impurities to the surface region, which is subsequently etched off. This process is referred to as 'gettering'. (ii) High temperature firing of hydrogen-containing dielectrics introduces hydrogen into the bulk, where it can passivate defects.[126] For SHJ cells, where processing occurs at <250 °C, these defect engineering processes are not incorporated into the cell processing, therefore, this cell architecture has stricter requirements on the wafer quality.[109] High temperature processing can also activate grown-in defects, such as thermal donors, which can reduce bulk lifetime. Therefore, it is important to consider not only the bulk lifetime of the as-cut wafer, but also the potential changes in the bulk during cell processing.

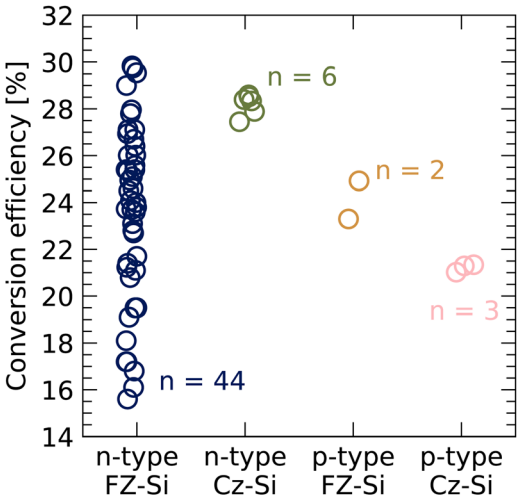

Fig. 7 Comparison of reported cell efficiencies for different wafer types used for perovskite/silicon tandems. Note, the world record efficiencies are not shown due to lack of reported information.

Fig. 7 displays a breakdown of the different wafer types used to date for perovskite/silicon tandem solar cells. This demonstrates an overwhelming tendency to use expensive, high lifetime n-type FZ wafers. These are often used for high efficiency passivating contact designs such as SHJ, which is useful to explore the efficiency potential for a specific cell design. However, it must be acknowledged that this wafer type is too expensive for industrial production. It is important to understand the impact the reduce bulk quality of Cz wafers will have on the practical efficiency of industrial perovskite/silicon tandems.

4.2. Silicon surface optics

A bare silicon wafer in air has reflectance in the range of 30–40%. In a single junction silicon cell, there are two main processes used to reduce the reflection on the front surface. The first process is texturing, which refers to a chemical etching process to change the physical structure of the surface. In monocrystalline wafers, the different etching rates for different crystallographic planes is exploited. An alkaline chemical etchant, typically potassium hydroxide (KOH), is used to anisotropically etch the surface. The etching rate of the ⟨100⟩ plane is much faster than for the ⟨111⟩ plane, therefore, careful control over the solution concentration and etching temperature can preferentially etch the ⟨100⟩ plane, leaving the ⟨111⟩ planes exposed. This leads to the formation of a pyramidal structure on the front surface. Fig. 8a shows an SEM image of a typical industrial textured silicon surface. The size of the pyramid base is typically in the range from 3–8 μm. On a planar surface, any reflected light is lost and cannot contribute to photocurrent generation. However, when the surface is fully covered with pyramids, the angle of reflection predominantly leads to the reflected light bouncing on a Si surface a second time and being absorbed. Thus, the improved absorption for a textured surface of a bare silicon wafer in air reduces reflection

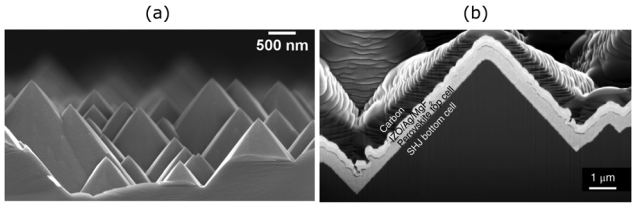

Fig. 8 (a) Alkaline textured random pyramids on a monocrystalline silicon surface (b) cross sectional SEM image of the full perovskite solar deposited on a textured silicon surface.[129]

to about 10%. For multicrystalline silicon, which is comprised of many different grains with varied orientations, the same approach cannot be used. Instead, an acidic texturing is used to roughen the surface.[127,128] The second approach to reduce reflection is the deposition of a dielectric anti-reflection coating. By carefully controlling the stoichiometry and thickness of the dielectric, typically PECVD SiN_x, the reflection is reduced by destructive interference. A typical SiN_x layer used as an ARC in PERC solar cells will have a refractive index of ~ 2 and thickness of 75 nm. Combining the surface texturing with the ARC can lead to reflectance of almost less than 1% at the optimised wavelength.

Micron-size pyramids are very effective for reducing reflection in single junction silicon solar cells, however, in monolithic perovskite/silicon tandems, this surface is not as compatible with all processing methods used for the perovskite top cells. Due to the small diffusion length in the perovskite material, the thickness must be kept to ≤ 1 μm to avoid recombination losses. In single junction perovskite solar cells, the layers are commonly deposited *via* solution processing. However, such thin layers cannot be deposited on top of micron-scale pyramids using solution coating techniques. As such, all demonstrations of monolithic perovskite/silicon tandem cells prior to 2018 were formed using a silicon wafer with a polished front surface. This is advantageous, as the perovskite and carrier selective layers can be deposited conformally, however, the planar surface has three major drawbacks, (i) significantly higher reflection on the front silicon surface, (ii) reduced light trapping at long wavelengths and (iii) significantly increased cost compared with alkaline textured surfaces. In 2018, Sahli *et al.* demonstrated the first perovskite/silicon tandem fabricated with a fully textured monocrystalline silicon front surface.[129] The key to achieving this was the modified perovskite deposition technique. Rather than simply spin-coating, the perovskite layer was formed by a two-step process. The first process involved the co-evaporation of a conformal porous lead iodide (PbI_2) and cesium bromide (CsBr) precursor film. Next, the organic ammonium halide salt solution was spin-coated to form the perovskite. The initial co-evaporation process serves as a conformal scaffold for the perovskite formation. The subsequent spin-coating wets and coats the PbI_2/CsBr scaffold. The scaffold acts as an anchor, so that the perovskite layer remains conformally coated. An SEM image of the conformal deposition onto the micro-size textured c-Si surface is shown in Fig. 8b. Initial attempts to form the perovskite by spin-coating without the scaffold did not work, the liquid solution accumulated in the valleys of the c-Si pyramids, leading to a non-conformal coating and significant device shunting. The authors achieved an efficiency of 25.2% using the two-step perovskite deposition on a textured surface, which was the highest efficiency for a monolithic 2T device at the time of publication in 2018.[129] This significant achievement was attributed to the improved optical management in the textured monolithic device. The fully textured device was compared to a similar device prepared on a polished surface. The loss in J_{SC} in the device with the polished surface was 3.14 mA cm^{-2}. This was reduced to 1.64 mA cm^{-2} for the textured wafer. The improved photocurrent generation was caused by reduced reflectance on the silicon front surface as well as better light trapping in the infra-red region. Despite the gains in J_{SC}, the efficiency is limited by the relatively low FF of 73.1%.

An alternative approach to improve the compatibility between the silicon surface and the perovskite deposition is to reduce the size of the surface pyramids. Although the industry standard micron size pyramids are not compatible with solution processed perovskite films, reducing the feature size could allow for subsequent conformal solution processing. Alasfour *et al.* provided a comprehensive study of the use of wet chemical etching to form nanoscale texturing on a silicon surface.[130] They showed that the ability to form nanoscale pyramids required both a slow etching rate as well as a large number of nucleation sites. If the ratio of nucleation sites to etch rate is sufficiently large, the surface becomes saturated with nucleation sites so that pyramids of >1 μm dimension are unable to form. To achieve these conditions, Alasfour *et al.* reduced the etchant concentration to reduce the etch rate and increased the concentration of the potassium silicate (K_2SiO_3), which controls the number of nucleation sites. By doing so, they were able to create nanoscale pyramids with a wide range of sizes, the minimum pyramid size was 62 nm. Reducing the pyramid size introduces a fundamental trade-off. Smaller pyramids are much more amenable with subsequent top cell solution processing, however, the reduced pyramid size also leads to increased reflection relative to standard micron-size pyramids.[130]

As an alternative to processing on highly textured silicon, inserting an ''optical-interlayer'' between the silicon and perovskite top cells can have a similar effect upon reducing reflectance losses. Including the top TCO and anti-reflective coating, the perovskite top cell is composed of up to 7 layers. This is hence an optical stack of materials for which the thickness of each layer requires optimising for minimising reflection losses and maximising absorption in the perovskite absorber layer and forward transmission into the Si cell. A key challenge in minimising the reflectance between the perovskite and silicon layers, is the significant contrast in refractive index of the perovskite (~ 2 to 2.5) and silicon (~ 3.5). Inserting an optically transparent layer which is approximately the mean of the refractive index of adjacent layers, and with a thickness of $\sim \frac{1}{4}$ the wavelength of the relevant light, leads to constructive

interference for forward transmission. Mazzarella *et al.* demonstrated that the insertion of a nanocrystalline silicon/silicon oxide interlayer on top of a mechanically polished SHJ cell resulted in significantly enhanced IR transmission of light,[131] and matched the at the time certified world record efficiency of Sahli *et al.*[129]

Recent excellent results from EPFL/CSEM and HZB demonstrated monolithic perovskite/silicon tandem cells with efficiency exceeding 30% for both planar and textured wafers. For the planar wafers, the perovskite was fully solution processed, while on the textured surface the two-step "hybrid" deposition process, first described by Sahli *et al.*,[129] was employed. From the CSEM/EPFL work, the efficiency achieved for planar and textured wafers was 30.93% and 31.25%, respectively.[100] The slightly higher efficiency on the textured surface was attributed to an increase in J_{SC} of $\sim$0.6 mA cm^{-2}. As discussed above, this was related to reduced reflection at short wavelengths and improved light trapping at long wavelengths. However, the issue for the textured approach is the lower FF, which was $>1\%_{abs}$ lower in the planar cell. If this issue can be addressed by preventing shunting, the efficiency potential for textured wafers could be much higher. However, the increased complexity of the two-step deposition process may introduce a trade-off between cost and efficiency. Notably, the present world-record of 32.5% from HZB was achieved on a polished Si wafer with the inclusion of the nanocrystalline SiO_x optical interlayer, regaining the lost photocurrent and sustaining a high FF. This questions whether reduced texture with optical interlayer optimisation is preferable to industrially standard full texture.

4.3. Surface passivation and junction formation approaches

The next choice to make for the bottom cell is the cell architecture. Section 2 provided a comprehensive overview of the existing cell designs for single junction silicon cells. Although PERC cells currently dominate the silicon PV market, by far the most prominent cell architecture for perovskite/silicon tandems with efficiency exceeding 25% is SHJ.[132] Fig. 9 displays a breakdown of the bottom cell type used to fabricate perovskite/silicon tandems to date. This indicates that SHJ is the most popular choice. There is a range of reasons why the SHJ architecture is advantageous as the bottom cell in a tandem design. These include.

- Potential for high V_{OC} due to the excellent a-Si surface passivation.
- The cell design already incorporates a TCO on the front surface, which easily integrates into tandems.
- Excellent flexibility of the placement of the n or p selective contact means it can be integrated with different perovskite configurations.
- The parasitic absorption losses at short wavelengths caused by passivation layers and TCO, which are the primary efficiency barrier for single junction cells, are not a problem when used as a bottom cell as short wavelengths are absorbed in the top cell.

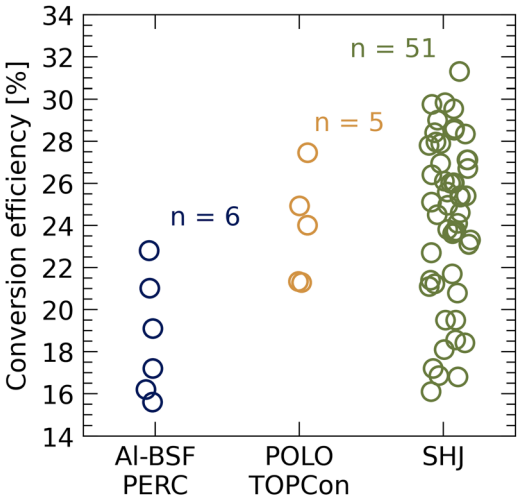

Fig. 9 Comparison of reported cell efficiencies for different bottom cell architecture from literature. Note, the world record efficiencies are not shown due to lack of reported information.

Al-Ashouri *et al.* reported a certified efficiency exceeding 29% for a monolithic tandem device using an SHJ cell as the bottom cell.[133] The silicon surfaces are passivated using intrinsic amorphous silicon. The carrier selective layer on the front surface is an n-type nanocrystalline – SiO_x, capped with ITO to form the recombination layer. The V_{OC} from this bottom cell was $\sim$715 mV, under approximately half sun illumination. The certified efficiency and V_{OC} value were 29.15% and 1.90 V, respectively. The same group has further reported improved conversion efficiency for this structure to 29.8%.[134] This was achieved mainly by modifying the silicon heterojunction bottom cell structure. First, a sinusoidal nano-texture was applied to the wafer's front surface, which reduced reflection losses and improved fabrication yield in comparison to planar front surfaces. Secondly, the authors implemented a reflector with a dielectric buffer layer, which reduced parasitic absorption at near-infrared wavelengths.

This shows clear potential for high efficiency devices, however, as shown in Fig. 3, the current market share for single junction SHJ cells is $<5\%$. This is caused primarily by the additional costs compared to PERC and TOPCon. For perovskite/silicon tandem solar cells to reach commercial production and thus have a tangible impact on reducing CO_2 emissions, a large set of stringent criteria must be met, including efficiency, cost, stability and sustainable production. In terms of manufacturing cost, it is also important to consider other cell designs. Messmer *et al.* provided a comprehensive analysis of performance, cost and LCOE for tandem cells using four different bottom cell designs.[135] Those designs included (i) PERC (which was denoted as P[E]RC as the diffused n^+ emitter on the front surface was directly contacted with ITO and thus not technically passivated), (ii) TOPerc, where the n^+ diffused emitter was replaced with a tunnel oxide/n^+ doped poly Si contact, (iii) TOPCon[2], where both surfaces contain thin oxide/doped poly Si (n^+ on the front surface), and (iv) SHJ,

which followed the standard structure with an n-type wafer, as displayed in Fig. 1. The authors used Sentaurus TCAD for optical simulations of the whole perovskite/silicon stack and Quokka3 for electrical simulations of the silicon cell. Electrical simulation on the perovskite cell were not performed, typical empirical values for performance were taken from literature. Their analysis showed that the highest efficiency potential was achieved with the SHJ bottom cell, the efficiency was $\sim 1.5\%_{abs}$ higher compared to the P[E]RC bottom cell. The efficiency potential for TOPerc and TOPCon^2 was in between SHJ and P[E]RC. The matched J_{SC} for all four bottom cell designs was similar, so the efficiency potential was primarily determined by differences in V_{OC} and FF. The V_{OC} for the SHJ bottom cell was 725 mV, which is more than 50 mV higher than P[E]RC. This was simply attributed to the much better surface passivation from the a-Si layers. Note that this value is lower than typically reported values, as the illumination intensity is lower than 1 sun due to absorption in the perovskite. The FF potential was also highest for the SHJ cell and followed a similar trend to V_{OC}. This was attributed to the higher pseudo FF (pFF) linked to higher V_{OC}. Interestingly, Fu *et al.* plotted the FF as a function of V_{OC} for sixty-four real *I–V* measurements of perovskite/silicon tandems.[132] A direct correlation between FF and V_{OC} was not observed. In fact, FF was often higher in high temperature homojunction c-Si bottom cell designs that exhibited lower V_{OC}. This indicates that FF losses in real devices are largely governed by resistive losses, indicating significant scope for further efficiency increases. However, we also note that the FF is a minimum when current matching is perfect. Since many experimental cells will not be perfectly current matched, the FF are usually higher than expected from the single junction cells and more variable.

When comparing the bottom cell design in terms of cost of production, a very different story emerged. Of the four cell designs, the cost of TOPerc was the lowest, at 47.8 €ct per cell. This was followed by P[E]RC at 48.4 €ct per cell, TOPCon^2 at 54.5 €ct per cell and SHJ at 61.2 €ct per cell. The same trend emerged but with slightly different costs when the recombination layer was replaced with a silicon tunnel junction interconnection layer. Finally, the costs and efficiency potential were compiled to calculate the €ct per W_p for each approach. Fig. 10 displays all module costs, in terms of €ct per W_p, for the four potential tandem configurations, as well as a reference PERC cell. For all cases, the tandem cells have lower cost compared to the PERC reference, however, there is very little distinction in €ct per W_p for the four different bottom cell arrangements. The cost varies from 19.4 €ct per W_p for the TOPerc bottom cell to 20.9 €ct per W_p for the SHJ bottom cell, however, due to the large uncertainty in some cost inputs, the values are all within the stated errors. This indicates that the race for the most appropriate bottom cell is still well and truly on, despite the overwhelming weight of research focus on SHJ cells.

One drawback of Messmer *et al.* analysis is the lack of consideration for sustainability of materials used in each design. For example, the SHJ cell in the above analysis is assumed to contain a 70 nm ITO layer on the rear of the cell, which is not amenable with TW-scale PV production (this is discussed in Section 5.1). As such, it is very useful to consider

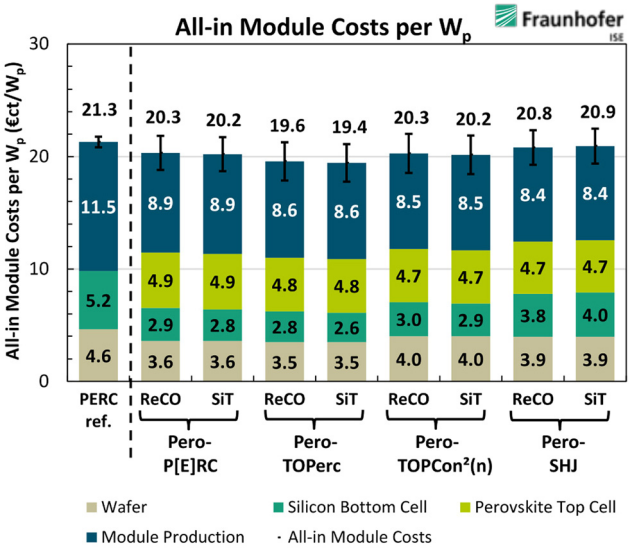

Fig. 10 All-in module costs per Wp for the four investigated bottom cell designs. 'ReCO' refers to recombination layer interconnection, while 'SiT' refers to a silicon tunnel junction interconnection.[135]

the industry mainstay PERC design, as it does not require indium and uses less Ag than SHJ and TOPCon.[136] Messmer *et al.* simulated the performance of perovskite/silicon tandems with a range of modified PERC cell as the bottom cell.[137] The authors emphasise that quite different design constraints apply when considering the front surface. In terms of a single junction PERC cell, the emitter is designed with the following considerations in mind, (i) the optical properties of short wavelength light, (ii) lateral transport of carriers to metal contacts, (iii) surface passivation, and (iv) low contact resistance with metal contacts. However, in a tandem architecture, the following differences apply, (i) short wavelengths are absorbed in the top cell and are thus not absorbed in the bottom cell, (ii) the magnitude of current is about half, (iii) the cell may not require lateral conduction in the emitter to local points and (iv) there is no thermal treatment for front contact formation. The relaxation of these strict design requirements for PERC may allow for a narrowing of the efficiency gap compared with SHJ, which is currently seen in single junction cells. In their simulations, Messmer *et al.* investigated five different front surface PERC designs, starting with a heavy n^+ emitter in direct contact with the ITO recombination layer, dielectric surface passivation with local openings and a variety of full area front surface passivation schemes. The simplest design, with the P[E]RC front cell yielded and efficiency of 29.5%, which increased to 30.5% for the TOPerc front cell. This efficiency is only $0.7\%_{abs}$ lower compared with a SHJ bottom cell, indicating the potential gains that PERC cells can gain by being incorporated into a tandem cell.

4.4. Metallisation

The contrast in typical processing routes for perovskite and silicon cells is perhaps most acutely felt when searching for metallisation approaches compatible with both cells. Record

perovskite single junction efficiencies are typically recorded on very small area devices <1 cm^2. Metal contacts in the small devices are formed using thermal evaporation. In this process, the samples are placed in a vacuum chamber under high vacuum ($<10^{-6}$ torr or mbar). The metal to be evaporated is heated in either a small boat or wrapped around a wire to the point where it vaporizes. The desired contact shape is defined with a simple shadow mask. This method is not currently employed for industrial silicon solar cells, as (i) the deposition rate is typically only on the order of a few angstroms per second, (ii) most of the evaporated metal is wasted coating either the shadow mask or the inside of the chamber and (iii) the deposited metal is orders of magnitude thinner than screen printed contacts, so the line resistance is very high and (iv) the vacuum level required is 10^3–10^4 times higher than is required for sputtering. In small area depositions, it is common for the metal contacts to be deposited outside the active cell area, a TCO is relied upon for lateral conduction of carrier to the contacts. This boosts the efficiency as it removes shading losses, however, when large area devices are formed, series resistance losses rise rapidly when using a TCO alone for lateral conduction. Therefore, a full metal contact grid is required. In contrast to very small area perovskite cells, metal contacts in silicon solar cells are formed using screen printing of metal pastes, typically silver or aluminium. The development of screen-printing metal contacts in 1975 revolutionised industrial solar cell design and allowed for the rapid upscaling that has subsequently occurred. Screen printed metal contacts allow for high throughput processing with low enough contact resistance and line resistivity to allow for high FF, even on device areas >200 cm^2. LONGi solar announced an efficiency of 26.5% for a full area front and back contacted SHJ solar cell with silver screen printed contacts and Sundrive have achieved $>26\%$ on SHJ cells with copper plating. Fig. 11 displays a comparison of solar cell area with the nominal power output for a range of perovskite/silicon tandems, industrial silicon cells and silicon modules. This analysis shows that the area and power output of typical high efficiency perovskite/silicon tandems are orders of magnitudes lower than the current industrial silicon solar cells and modules. For perovskite/silicon tandems to become a serious commercial product, they must traverse this curve to larger areas, with cell areas >244 cm^2. To do this, a fundamental shift in the metallisation is needed.

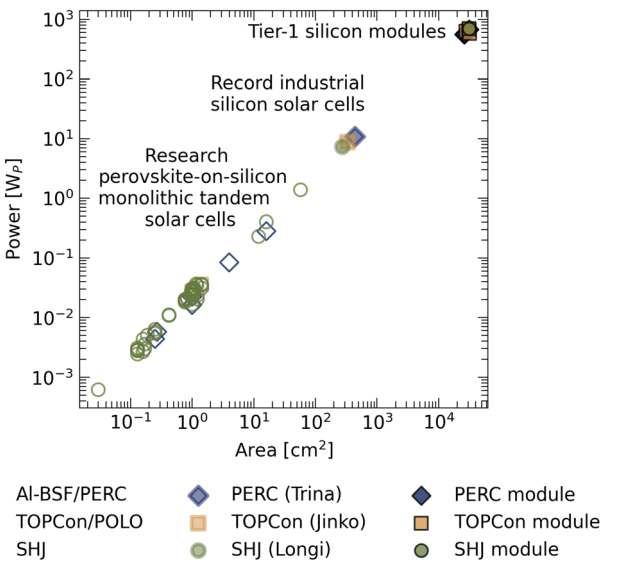

Fig. 11 (a) Comparison of nominal power and device area for various perovskite/silicon tandem solar cells, industrial silicon solar cells and silicon modules. Figure design based on ref. 139.

Kamino *et al.* took a first step in this direction in forming a perovskite/silicon tandem by low temperature screen printing.[138] They achieved an efficiency of 22.6% on this device, compared with 24.0% for a device with evaporated Ag contacts (area of 1.43 cm^2). The screen-printed contacts were cured at 130 °C due to the temperature constraints of the perovskite layer. A substantial loss in FF was observed in the screen-printed cell, primarily due to the contact resistance between the Ag and ITO. In the screen-printed contact cured at 130 °C, the contact resistance was 60 mΩ cm^2, as opposed to 0.02 mΩ cm^2 for the evaporated Ag contact annealed under the same conditions. The purpose of the curing step is to make the printed contact more compact, which reduces the resistance. When the curing temperature was increased from 130 °C to 210 °C, which is typical of cell processing for SHJ cells, the contact resistance reduced from 60 mΩ cm^2 to 10 mΩ cm^2. However, curing at this temperature will lead to degradation of the perovskite cell. This tension must be resolved to achieve high quality metal contacting for large area devices. The J_{SC} was also reduced compared to the evaporated cell due to shading from the contacts.

4.5. Summary of design considerations for silicon-based tandems

The design approach for the bottom cell in a 2T tandem is quite different to that of a single junction silicon cell. Here, we summarise the fundamental differences. A graphical overview of some of the critical design considerations is shown in Fig. 12.

Front surface. Rather than simply optimising the front surface for maximising absorption and carrier collection, the front surface must accommodate the fabrication of the top cell. The growth of nanoscale layers of the perovskite absorber and additional charge collection layers must be balanced against the desire optimal absorption and light trapping *via* surface texturing. When high throughput solution processing is desired, the surface morphology will require adjustments compared to the single junction case.

Interconnection. Electrical contact must be formed between the top cell and bottom cell. This may occur through a full area contact that only requires one dimensional carrier transport, or through local interconnections. The addition of a heavily doped tunnel junction adds processing complexity and a TCO recombination layer can induce additional parasitic absorption losses.

Metallisation. Although the silicon front surface does not require metal contacts, the metallisation approach for the

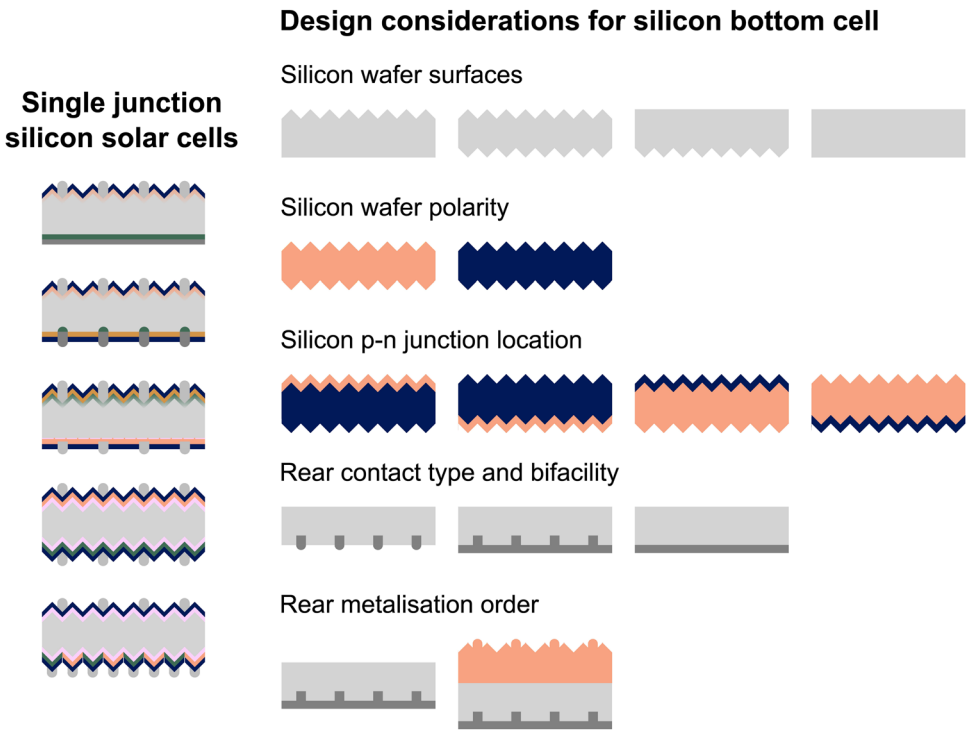

Fig. 12 Graphical overview of the design considerations for silicon bottom cell in the tandem architecture.

tandem is one of the most problematic. This is directly linked to the temperature constraints imposed by the top cell. Currently, the metallisation must not require temperatures exceeding ~130 °C, which is stark contrast to standard screen-printed silver contacts that are fired at >750 °C. Additionally, solutions must be found that allow for low resistive losses in large area devices (>244 cm^2).

5. Other design aspects

5.1. Sustainability of materials

To mitigate the impacts of climate change, other sectors besides electricity generation will need to shift away from fossil fuels to renewable energy. The energy transition to 100% renewables requires a drastic increase in the annual production capacity of solar PV. Verlinden and Haegel *et al.* predicts that a cumulative solar PV capacity of 70 TW is needed by 2050.[6,7] This will require a 30-fold growth in the annual production capacity, relative to 2020. Verlinden also warns that to reach this level, rapid initial growth, such that a production capacity of 3 TW is achieved by 2032, is needed to avoid subsequent market instabilities.[7] This points to the idea that the next ten years of solar production are critical in fighting climate change.

In light of the rapid upscaling of PV manufacturing required over the next decade, the consumption of the materials that go into making solar cells must be closely scrutinised. Most of the body of literature in solar cell research has focussed first on increasing the efficiency and stability of solar cells, then implementing these designs into mass production. Sustainability of the materials used in the cell design must now come to the forefront of the solar community's collective mindset. In particular, silver (Ag) and indium (In) are scarce materials that are integral components of modern solar cell design. Zhang *et al.* analysed how material consumption demands could limit the expansion of different single junction cell technologies.[136] Assuming the PV industry could use 20% of the global supply of a particular material, they estimated that the annual manufacturing capacity was 377 GW for PERC (limited by silver), 227 GW for TOPCon (limited by silver) and 37 GW for SHJ (limited by indium). This alarmingly shows that current cell designs, without modification, are not capable of sustaining a future TW solar PV market. Silver is used for contact formation in all three cell designs. Zhang *et al.* calculated that the Ag consumption for each cell technology is currently 15.4 mg W^{-1} for PERC, 25.6 mg W^{-1} for TOPCon and 33.9 mg W^{-1} for SHJ.[136] PERC has a lower Ag consumption as it uses aluminium for the rear metallisation. By contrast, SHJ structures require Ag metallisation on both surfaces and use more Ag due to the low temperature curing demanded of the a-Si passivation layers. The authors argue that this consumption must be reduced drastically to 2 mg W^{-1} if TW-scale markets are to be sustained, which has drastic implications for cell design.

As well as material consumption issues, the price volatility of Ag may also become a problem as the PV manufacturing expands. The cost of silver is approximately 10% of the selling price for a solar cell, however, for a smart phone it is only 0.01–0.05%, meaning other competing industries will be much more tolerant to price fluctuations.[136]

The absolute power loss due to the resistance in metal fingers can be calculated by:

$$\mathrm{Ploss}_{\text{finger resist; abs.}} = \int_0^{\frac{W_{\text{cell}}}{N_{\text{BB}}}} (x \cdot J_{\text{MP}} \cdot S_{\text{f}})^2 \cdot \frac{\rho_{\text{m}}}{W_{\text{f}} \cdot t_{\text{f}}} \cdot \mathrm{d}x$$

$$\mathrm{Ploss}_{\text{finger resist; abs.}} = \frac{{J_{\text{MP}}}^2 \cdot {S_{\text{BB}}}^3 \cdot {S_{\text{f}}}^2 \cdot \rho_{\text{m}}}{24 \cdot W_{\text{f}} \cdot t_{\text{f}}}$$

where x is the distance from the middle of the finger to the busbar, J_{MP} is the current density at maximum powerpoint, S_{f} is the finger spacing, ρ_{m} is the line resistivity of the fingers, W_{f} is the width of the finger, t_{f} is the finger height and S_{BB} is the busbar spacing.

This can be converted to a relative loss in the following way:

$$\mathrm{Ploss}_{\text{finger resist; rel.}} = \frac{\mathrm{Ploss}_{\text{finger resist; abs.}}}{P_{\text{unit cell}}} = \frac{J_{\text{MP}}}{V_{\text{MP}}} \cdot \frac{{S_{\text{BB}}}^2 \cdot S_{\text{f}} \cdot \rho_{\text{m}}}{12 \cdot W_{\text{f}} \cdot t_{\text{f}}}$$

This indicates that the power loss is dependent on the $J_{\text{MP}}/V_{\text{MP}}$ ratio. As such, it is advantageous to simultaneously reduce the current and increase the voltage. This presents a strengthened case for monolithic 2T tandem solar cells. Relative to any single junction silicon solar cell design, the J_{MP} will be lower, as the solar spectrum is split between the two absorbers. Additionally, the top cell is composed of a wide E_{g} material, which increases the voltage substantially relative to silicon. This improved tolerance to resistive losses opens potential opportunities to move away from Ag, such as the use of more resistive copper pastes.

Consumption of indium is also challenging for solar cell manufacturing. Although indium is more abundant in the earth's crust than silver, the useable fraction is much lower.[136] This is because indium is produced exclusively as a by-product of the processing of other metal-ores, namely zinc.[140] PERC and TOPCon cells do not require indium, however indium tin oxide (ITO) is used in SHJ cells to provide lateral conduction to the contacts and serves as an anti-reflection coating. In PERC and TOPCon cell designs, the lateral conduction of carriers occurs in the diffused emitter or silicon bulk. In a standard industrial SHJ cell, the ITO layer on the front and rear surface is typically in the range of 70–100 nm. Zhang *et al.* performed an analysis of the possible annual production capacity of SHJ cells based on indium consumption. Fig. 13 displays a contour plot showing the annual production as a function of indium usage, in mg W^{-1}, and % use of 2019 indium supplies. The upper and lower limit on indium consumption for industrial SHJ cells was 10.74 mg W^{-1} and 4.23 mg W^{-1}, respectively, based on literature and discussions with SHJ manufacturers. These upper and lower bounds of indium consumption are shown in the shaded region. Isolating the case where 20% of the total indium is required, this corresponds to an annual production capacity between 35–95 GW. This severe limitation caused by the dependence on ITO means the annual production capacity of SHJ cells, with the current industrial cell design, is more than an order of magnitude lower than required for TW-scale PV. As such, the authors

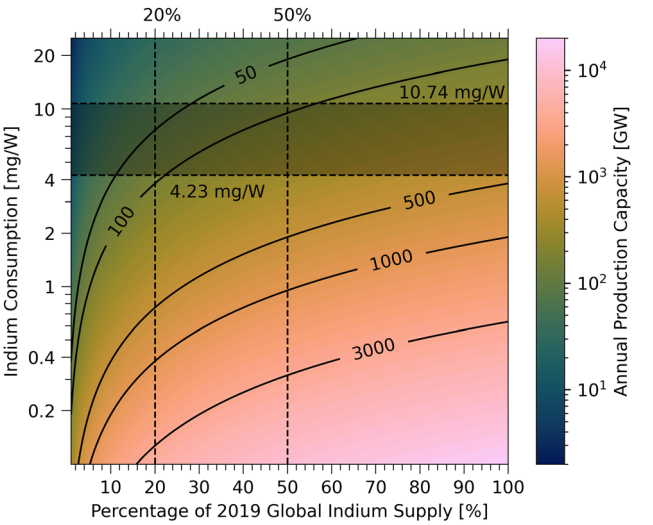

Fig. 13 Calculated allowable annual production capacity for SHJ solar cells as a function of both the indium consumption (mg W^{-1}) per cell and % of 2019 global indium supply.[136]

state, "Indium cannot be used in any significant manufacturing capacity for PV production, even for futuristic 30%-efficient tandem devices".[136]

Lennon *et al.* recently raised an additional concern regarding the sustainable production of TW scale solar PV.[141] By considering the ITRPV broad electrification scenario, which predicts a cumulative installation of 60 TW of solar PV by 2050, they calculated the required aluminium demand for PV production. The rapid increase in solar PV production demanded of this scenario meant the Al requirement by 2050 would be as high as 28.5 Mt per year. This demand is more than 40% of the 2019 total global Al production. Due to the very high average emissions intensity of primary aluminium production, this would lead to an alarming global warming potential. It should be noted, however, that the contribution associated with cell metallisation was negligible, meaning this would not limit the use of Al for cell designs. The primary contributors to Al demand were module frames, mountings and inverters. These results highlight the need to consider not only the material consumption for the TW scaling of PV, but also the CO_2 emissions associated with producing these materials.

5.2. Stability

The final consideration is the long-term stability of the cells and modules. It is widely known that perovskite solar cells have suffered from stability issues, however, significant research and development efforts have been expended upon understanding and mitigating the instabilities. The intrinsic stability issues of the perovskite material, particularly in the presence of moisture, and the various mitigation strategies have been reviewed in the following ref. 142–144. Herein, we focus on experimental demonstrations of stability in tandem solar cells. For a detailed analysis of stability issues in perovskite/silicon tandems, the reader is directed to ref. 145.

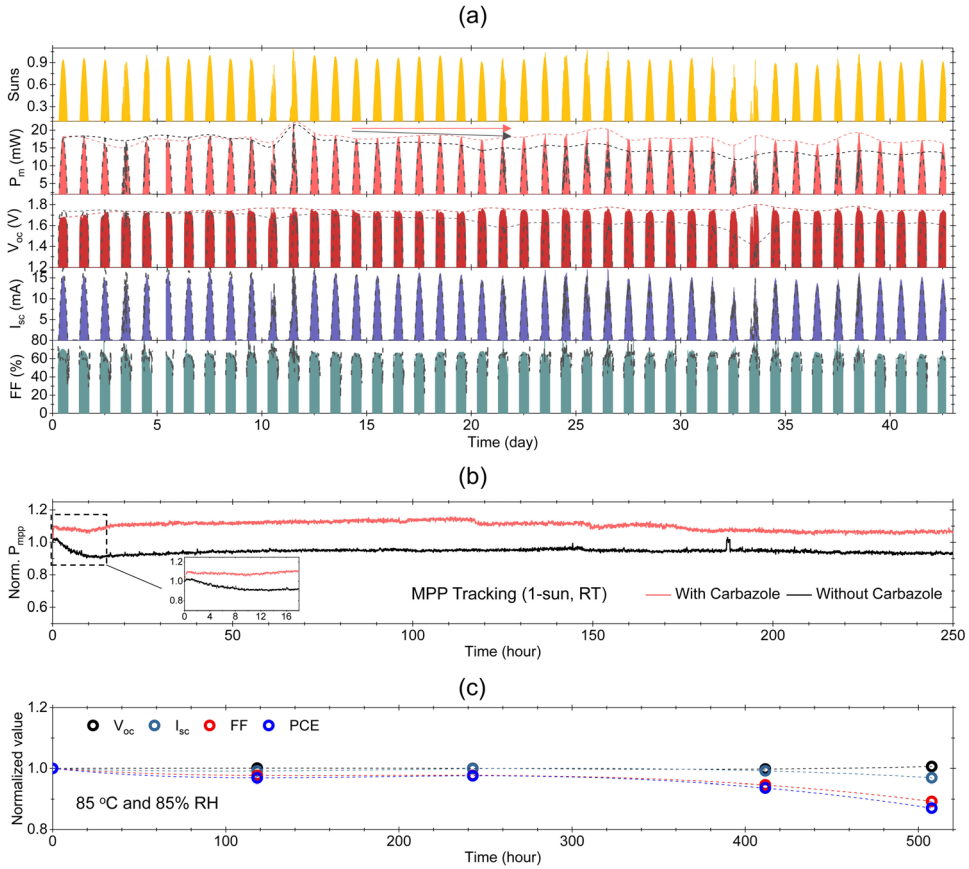

Fig. 14 Outdoor testing results over 43 days for perovskite/silicon tandem cell. (a) Light intensity, power output, V_{OC}, I_{SC} and FF, (b) power output of cells under constant illumination for 250 hours, (c) damp heat testing at 85 °C at 85% RH.[146]

Liu *et al.* investigated the performance of encapsulated perovskite/silicon solar cells under outdoor testing conditions in a hot and sunny environment.[146] The wide band gap perovskites used to form tandem cells typically show reduced stability compared to perovskites with E_g of 1.50–1.60 eV. These instabilities are often attributed to phase segregation under illumination. In their report, Liu *et al.* investigated the impact of carbazole as an additive to the perovskite precursor solution to assess the impact on the stability of perovskite/silicon tandems. Before testing, the devices were encapsulated between two pieces of cover glass with black butyl rubber sealant. Outdoor testing was performed on an open rack system at King Abdullah University of Science and Technology (KAUST). The average temperature was 45 °C, which increased to a maximum of 60 °C. The maximum illumination intensity was ~0.95 suns, measured by a pyranometer. Outdoor testing is rigorous, since it exposes the samples to operation under diurnal illumination, elevated temperatures and heat cycles from night-to-day. Fig. 14a displays the light intensity, power output, V_{OC}, I_{SC} and FF of perovskite/silicon tandems, with and without carbazole treatment across 43 days of continuous testing. At the end of the test period, the control device that was not treated with carbazole exhibited a power output 77% of the initial value. This degradation was seen primarily in V_{OC}, which was attributed to degradation of the perovskite itself. The PCE retention in the carbazole-treated samples was 93% for the 43 days of outdoor testing. First, compared with industrial silicon solar cells, this degradation is large. PV manufacturers routinely providing 25 year warranties on their products, with a typical expected degradation rate of 0.5%/per year. Second, the significant impact that the carbazole treatment had on stability indicates that degradation in the perovskite is limiting the overall stability. Following this, the further indoor testing was performed under continuous xenon lamp illumination with MPP tracking. Fig. 14b displays the power output of the cell under constant illumination for 250 hours. The untreated cell underwent ~8% degradation. In contrast, the carbazole treated cell did not display any signs of degradation in this testing period. Finally, the cells were tested under damp heat conditions of 85% RH at 85 °C. The results of the damp heat test are shown in Fig. 14c. After 500 hours under these conditions, the cells retained 87% of the initial efficiency. This degradation was caused by losses in FF, attributed to degradation of the top contact.

Current matching is very important for maximising the efficiency of a 2T tandem solar cell. Under STC conditions (25 °C), the optimum E_g of the perovskite, when coupled with silicon is ~1.73 eV.[19] When designing to maximise energy yield in a monofacial tandem, this drops to 1.65 eV, and even further when maximising the energy yield in a bi-facial tandem.[147]

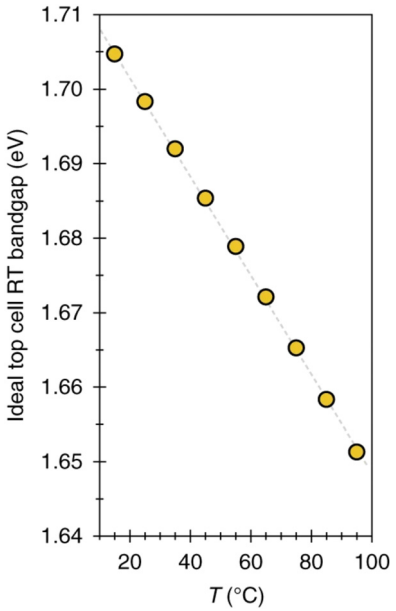

Fig. 15 Calculated optimum perovskite E_g for maximising efficiency under AM1.5 irradiance under varied operating temperature.[149]

These band gaps are achieved in perovskites by varying the stoichiometry of the halide. However, wider gap perovskites are known to experience phase segregation under illumination, which can cause current and voltage losses.[148] Aydin *et al.* studied the impact of temperature on the performance of perovskite/silicon tandems.[149] By varying the temperature from 25 °C to 75 °C, they showed that the current matching in the tandem device changes for varied temperature. This is related to the temperature dependence on the E_g. It is well known that the E_g of c-Si narrows as the temperature is increased. By varying the bromide concentration in $FACsMAPbI_{3-x}Br_x$ from 6% to 30%, the E_g of the perovskite at 25 °C was varied from 1.61 eV to 1.73 eV, respectively. The E_g was then measured for four different compositions as a function of temperature between 25 °C and 75 °C. This showed that the E_g of the perovskite widens as temperature increases, which is the opposite trend to the c-Si bottom cells. This implies that the optimum perovskite E_g for current matching at STC conditions may not perform the best under realistic conditions at elevated temperatures. The authors then recalculated the radiative efficiency limits for perovskite/silicon tandems by incorporating the impact of temperature on the E_g. The optimum perovskite E_g, as a function of operating temperature, is shown in Fig. 15. This shows that the optimum E_g shifts to lower values for higher temperatures, which may prompt a rethinking of the cell design. Combining the temperature dependence of the band gap, with the need to maximise energy yield rather than AM1.5 efficiency, and the general trend in the industry towards bi-facial modules, it is likely that the optimised band gap for a perovskite top cell is closer to 1.5 eV than to 1.7 eV.[150] This has a practical benefit for mixed bromine-iodine halide perovskites, as bromide-lean compositions, with $E_g < 1.65$ eV, are more stable under illumination due to less halide phase segregation and are also easier to obtain comparatively higher efficiency.[148,151]

To accelerate stress testing of perovskite/silicon tandems, Babics *et al.* reported a one-year duration outdoor stability investigation, retaining 80% of the device PCE over the test period.[152] Unlike previous studies, in which only butyl edge sealant was employed, this study used transparent thermoplastic polyurethane (TPU) to encapsulate the perovskite and mitigate the volatility of alkylammonium halides. SIMS-depth profiling revealed that trace cesium had migrated into the TPU film. During outdoor testing, a transient response in the *I–V* parameters of the tandem cell were observed. This is largely attributable to the perovskite, since the performance of a companion single junction SHJ cell remained unchanged during the duration. Most promising are the trends in V_{OC} and FF retention. Initially, the V_{OC} increased from 1.71 V to 1.77 V as the passivated NiO/perovskite interface stabilised. Laboratory testing after one-year of outdoor testing reported a V_{OC} of 1.75 V, indicating no damaging formation of deep traps during one year of service.

The investigation uncovered several effects on tandem J_{SC} which warrant the attention of the community. Under outdoor conditions, the tandem J_{SC} is influenced by a complex interplay of top-cell bandgap, device history, sub-cell temperature coefficients, and incident spectrum. Babics *et al.* observed a subtle narrowing of the perovskite bandgap from 1.67 to 1.63 eV.[152] Notably, masked regions of the device retained their original bandgap, consistent with photo- or field-induced halide redistribution. The study highlights an important shortcoming of the standard AM 1.5G spectrum as it applies to real-world tandem operation. The standard spectrum has allowed researchers to optimise their solar cells under comparable conditions, improving confidence in interlaboratory comparisons. However, significant local spectrum deviations from the standard AM 1.5G spectrum can exaggerate current mismatch conditions and impact energy yield. Furthermore, soiling of the glass surface with dust caused a spectral redshift through absorption or scattering.

The study highlights that constantly evolving outdoor conditions place considerable pressure on current mismatch. Beyond the obvious degradation factors, it is important to recognise that perovskite/silicon tandems will most frequently be operating under sub-cell-limited current conditions. More outdoor studies conducted under diverse climate conditions are required to untangle the environmental effects that impact mismatch and ultimately energy yield.

6. Conclusions

Perovskite/silicon tandem solar cells represent an exciting opportunity to increase the efficiency and reduce LCOE of the incumbent single junction silicon technology. They have just broken through the 30% efficiency barrier, which represents a promising milestone given the relative infancy of this approach. However, there exists a technological disconnect

between the fabrication of small area record tandems devices and the processing required for industrial mass production. The constraints imposed by the perovskite top cell require a rethink of the design of an industrial silicon solar cell. We highlight the new mindset required for designing the silicon. In this article, we outline the new design considerations for the bottom silicon cell, including (i) modifying the front surface to accommodate the top cell processing, (ii) electrical interconnection between the silicon cell and perovskite, (iii) forming metal contacts given the temperature constraints of the top cell. Importantly, we also discuss the design constraints in the view of multi-TW manufacturing and describe how material consumption will influence aspects of cell design. Critically, the use of silver and indium must be minimised or removed from tandem manufacturing for TW deployment. Reductions in LCOE from solar PV are needed to upscale manufacturing to the level required to reduce CO_2 emissions and avoid a climate disaster. The discussion in this paper outlines the required shift in mindset when designing silicon bottom cells for >30% tandem cells in the future.

Conflicts of interest

There are no conflicts to declare.

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