Journal of Applied Physics

RESEARCH ARTICLE | AUGUST 21 2023

Bias-voltage photoconductance and photoluminescence for the determination of silicon-dielectric interface properties in SiO_2/Al_2O_3 stacks

Paul Masuch ; Christian Reichel ; Ruy Sebastian Bonilla ; Armin Richter ; Jan Benick

J. Appl. Phys. 134, 075705 (2023)
https://doi.org/10.1063/5.0153204

Journal of Applied Physics ARTICLE pubs.aip.org/aip/jap

Bias-voltage photoconductance and photoluminescence for the determination of silicon-dielectric interface properties in SiO_2/Al_2O_3 stacks

Cite as: J. Appl. Phys. **134**, 075705 (2023); doi: 10.1063/5.0153204
Submitted: 5 April 2023 · Accepted: 24 July 2023 ·
Published Online: 21 August 2023

Paul Masuch,[1,a)] Christian Reichel,[1] Ruy Sebastian Bonilla,[2] Armin Richter,[1] and Jan Benick[1]

AFFILIATIONS

[1]Fraunhofer Institute for Solar Energy Systems (ISE), Heidenhofstrasse 2, 79110 Freiburg, Germany
[2]Department of Materials, University of Oxford, Oxford OX1 2JD, United Kingdom

[a)]**Author to whom correspondence should be addressed:** paulmasuch0@gmail.com. **Now with:** NexWafe GmbH, Hans-Bunte-Straße 19, 79108 Freiburg, Germany.

ABSTRACT

This paper presents an advanced measurement method for controlling the surface charge carrier density of passivated silicon wafers during photoconductance and photoluminescence measurements, by employing semitransparent poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) electrodes with an applied bias voltage. This is employed to study and analyze charge carrier dynamics in dielectric layers by measuring their direct influence on effective lifetime. With this method, the carrier population at the surface and the effective carrier lifetimes of n- and p-type samples can be investigated, from which the fixed charge carrier density Q_f of the passivation can be extracted. Additionally, the defect density D_{it} can also be derived from the minimum lifetime values at flatband voltage. In SiO_2/Al_2O_3 stacks with varying SiO_2 interlayer thickness, it was shown that by changing the SiO_2 thickness, the carrier density Q_f can be tuned to a wide range of values, which corresponds to the results obtained in other studies. An increase in interlayer thickness resulted in a decrease in Q_f. Varying the SiO_2 thickness, the behavior of the respective effective lifetime under bias voltage also changes, exhibiting hysteresis-like effects, which are attributed to additional charges getting trapped at the surface during bias-voltage application. This effect is much more pronounced for samples with a thinner SiO_2 layer as well as for the n-type samples. Additionally, the doping type also influences the magnitude of Q_f, with p-type samples generally reaching lower absolute values. It was also shown that aging of the samples had a significant effect on the measured Q_f, which was increased compared to the initial Q_f of the passivation. This effect was more pronounced for the n-type samples. The measurements were realized by a cost-effective and easy-to-use microcontroller-based potentiostat, which can be used as a simple add-on to existing photoconductance or photoluminescence measurement setups.

INTRODUCTION

In the 21st century, silicon surface passivation has gained major importance in being the limiting factor for device efficiency of silicon solar cells.[1–5] Many improvements in the production process of pure silicon have led to a decrease in defect density in the silicon bulk, increasing the influence of surfaces and interfaces of solar cell structures. These constitute abrupt discontinuities of the crystal lattice, which introduce defect states in the forbidden bandgap. These states then facilitate recombination of charge carriers via the Shockley–Reed–Hall mechanism, which lowers the efficiency of the solar cell. Surface passivation is the technique to reduce the amount of recombination. In practice, this is done mainly by applying a dielectric layer to the cells surface. This layer lowers the defect density (D_{it}) by saturating the so-called "dangling bonds." Additionally, the passivation layer can introduce a fixed charge density (Q_f) at the interface, which can influence the

amount of recombination at the interface. The fixed charges generate a mirror charge in the substrate by establishing an electric field that penetrates the interface, modifying the charge carrier density at the interface. The fixed charge density can increase or decrease the ratio of carrier concentrations and, thus, lower the amount of surface recombination.[5]

As the fixed charge density Q_f greatly influences the performance of silicon devices, determining its exact value and gaining insight into the precise mechanisms of charge formation and charge dynamics is of great interest. However, accurate determination of Q_f is often a difficult task, as it requires the control of the charge carrier concentrations in the space charge region. The most commonly employed measurement techniques for this task are capacitance–voltage measurement (C–V)[6] or corona charge deposition.[7] For C-V measurements, the sample must be made into a metal–insulator–semiconductor (MIS) structure, using metal contacts on both sides. A range of DC bias voltages is then applied to the sample and the capacitance is measured by a superimposed small AC signal.[8] This method has the disadvantage of requiring specific, time-consuming sample preparation, which inhibits further determining the charge carrier lifetime by photoconductance measurements of the same sample. Corona charge deposition works by applying a strong voltage between the sample and a sharp metal electrode that rests above the sample, resulting in chain ionization of the air and charge deposition on the dielectric.[9] The amount of charge is then measured with a Kelvin probe and the lifetime of the sample is determined in dependence of the deposited charge. This measurement process has the disadvantage of consisting of multiple steps, during which charge leakages can occur. This makes it relatively cumbersome if a larger range of surface charges are to be investigated. It also suffers from large errors in determination of charge as certain dielectrics do not hold charge for a long enough period of time to complete successful measurements. Both methods suffer greatly from such dielectric conduction, making them not suitable for all types of dielectrics.

One alternative method is to add a very thin metal gate on top of the dielectric layer, thus creating a metal–insulator–semiconductor (MIS) structure and then testing the sample by photoconductance. Applying a bias voltage to the metal gate can then be used to control the surface charge density, and thus drive the device into the accumulation, depletion, or inversion regimes. This so-called Bias-Voltage Photoconductance (Bias-PCD) method with semitransparent electrodes was first introduced by Jellett and Weber,[10] using an ultra-thin aluminum layer on both sides of the sample. The metal gate, however, lowers the amount of light that can enter the device, impeding charge carrier injection and, therefore, hindering the characterization of the sample via photoconductance measurements. This can be overcome by very finely tuned deposition of extremely thin metal gates as done in Ref. 10, keeping them semitransparent. Other more novel methods exist, like a dual mercury probe setup,[11] but these are based on assumptions of the charge dynamics inside the samples or suffer from similar problems as the aforementioned methods.

An alternative approach was developed by Bonilla,[12] using a conductive organic polymer, poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS), as a gate electrode of the MIS structure instead. The latter technique is based on a simple, cheap, and reliable sample preparation and measurement technique. It can be used to easily extract information about the fixed charges at the interface and even about the defect density via modeling of the measured dependence of the charge carrier lifetime or surface recombination velocity over the bias voltage.[13] In this paper, an advanced version of this method is presented. It is realized in the form of a low-cost add-on device for the Sinton WCT-120 photoconductance measurement unit,[14] which can be connected via universal serial bus (USB) to the same measurement computer. With this device, external voltages of up to ±14 V can be applied to samples prepared with semitransparent electrodes. This voltage is used to control the surface charge carrier concentration, allowing for a quick and easy determination of the fixed charge density Q_f at the silicon–dielectric interface for many different passivation layer configurations. The defect density D_{it} can also be estimated based on the minimum lifetime values at flatband voltage. With precise modeling following the Girisch-Aberle algorithm,[15,16] implemented in Matlab,[13] these values can be determined with high precision.

In this report, we present the results obtained by using our advanced implementation of the Bias-PCD method with a set of crystalline silicon samples with dielectric layers applied by plasma enhanced atomic layer deposition (PEALD). A capping layer of 20 nm of aluminum oxide (Al_2O_3) combined with an interlayer of silicon dioxide (SiO_2) with thicknesses between 0 and 10 nm was used. This sample configuration was chosen as Al_2O_3 passivation layers are known to exhibit excellent passivation properties[17–19] with defect densities as low as $D_{it} \sim 10^{11}$ eV^{-1} cm^{-2} and high negative fixed charges of up to $Q_f \sim -10^{13}$ cm^{-2}. The exact mechanism of charge formation in Al_2O_3-passivated samples is an area of intense research. Most studies conclude that these negative fixed charges form at the interface during the ALD growth process.[2] A very thin interlayer of SiO_X forms between the c-Si substrate and the Al_2O_3 layer, which is crucial for the charge injection from the substrate into the dielectric. It was previously shown that growing a SiO_2 interlayer before depositing Al_2O_3 weakens this charge injection. This can be exploited to tune Q_f to a desirable value.[20,21] This way, the passivation can be adjusted to different substrates or for different device applications. This set of samples serves as a robust example to demonstrate the working principle of the Bias-PCD method.

The focus of this study is on presenting an advanced characterization technique and using it to gain new insights into the changes in the passivation mechanisms as Al_2O_3 is combined with a SiO_2 interlayer. The impact of the interlayer thickness on the results is furthermore discussed in detail.

Preliminary tests on samples prepared with PEDOT:PSS showed large differences between samples tested at different times after their preparation. As studies have reported the humidity-related effects of aging on PEDOT:PSS layers,[22] a part of the samples was tested 1 month after the application of the PEDOT:PSS electrodes, to study whether similar effects can be observed with the gate electrodes. Additionally, the use of the device for Bias-Voltage Photoluminescence (Bias-PL) measurements is showcased. This can be used to obtain voltage-dependent PL images for the inspection of passivation uniformity or detection of inhomogeneous bulk defects.

BIAS-VOLTAGE MEASUREMENTS

The experimental setup developed in this work is illustrated in Fig. 1(a). The appropriately prepared sample rests on the sample stage of a Sinton WCT 120 lifetime tester,[14] which contains the sensor used for the photoconductance measurements. The bias-voltage device is connected to the electrode and silicon/wafer bulk contacts on the sample via spring-loaded probes and a pressure contact to a copper foil. This way voltage is applied between the passivated sides of the sample and the bulk silicon.

The device is designed as a simple and cost-effective potentiostat that can apply voltages up to ±14 V to a sample, while simultaneously logging the bias voltage and leakage current in real time. The design is based on Ref. 23 and expanded to meet the demands of the Bias-PCD method. Central to the hardware is an Arduino Nano microcontroller,[24] which serves as the USB connection to the PC, and via which the Inter-Integrated Circuit (I^2C) communication to the digital-analog converter (DAC) and analog-digital converter (ADC) is established. The DAC is configured to output a signal between 0 and 5 V, which serves as a set point for the desired voltage of up to ±14 V at the passivation layer. A combination of multiple operational amplifiers compares this signal and the measured potential, driving the output until the measured potential reaches the desired value. Figure 1(b) gives an overview of the employed circuitry.

The accompanying Bias-PCD software is designed to run in parallel to the Sinton Instruments Photoconductance Software.[25] While it is running, it constantly logs, displays, and controls the bias voltage and leakage current between the substrate and the gate electrodes. Photoconductance measurements at a certain bias voltage can be executed by inputting the appropriate voltage value, which is then held steadily by the device, followed by executing a measurement using the Sinton Instruments software. As the Bias-PCD software controls the Sinton Instruments software, no further modification of the original software is required. During this study, all photoconductance measurements were taken in transient mode with a flash time of 1/64 s, considering that all samples showed a sufficiently high effective lifetime before a voltage was applied. It must be noted that multiple measurements resulted in lifetimes below 200 μs, especially around the lifetime minimums, where the transient mode produces less reliable results. For the exact determination of D_{it}, additional measurements with the generalized mode and a flash time of 1 s should be performed, which was not in the scope of this work.

To facilitate measurements over a large range of different voltages, the software provides the automated "voltage sweep" method. A start and end value as well as the step width can be defined, which determines at which voltage values photoconductance measurements will be conducted. Various other measurement options are also available, for example, defining whether the sweep should be repeated with opposite polarity.

SAMPLE DETAILS

To verify the practicability of the presented Bias-PCD setup, n- and p-type 1 Ω cm float-zone (FZ) silicon wafers of 200 and 250 μm thickness, respectively, were studied. The samples were shiny-etched on both sides. They were subject to a standard RCA cleaning step,[26] before being oxidized at 1050 °C in dichloroethylene, oxygen, and argon to grow a 100 nm thermal silicon dioxide (SiO_2) layer on both sides, to deactivate FZ defects.[27] Before application of the final passivation layer, this SiO_2 layer was again removed by a buffered oxide etch. The dielectrics were then applied by means of plasma enhanced atomic layer deposition (PEALD) with a FlexAL system by Oxford Instruments at 140 °C. First, the SiO_2 interlayer was deposited with a thickness varying between 0 and 10 nm, using bisdiethylaminosilane (BDEAS) as a precursor. The samples were then all capped with a 20 nm layer of Al_2O_3, with trimethylaluminum (TMA) as the precursor. After the depositions, a forming gas anneal was performed at 425 °C for 25 min to activate the passivation on all samples. Passivation was always applied symmetrically on both sides of the sample.

Following the anneal, the wafers were broken into quarters and a layer of poly(3,4-ethylenedioxythiophene) polysterene sulfonate (PEDOT:PSS) was applied**.** The samples were spin-coated at 1000 rpm for 120 s with the solution F HC Solar,[28] after which they were left drying for 10 min at room temperature, and finally baked out on a hotplate for 120 s at 120 °C. This process was repeated on both sides of the sample. During the spin coating on the top side of the samples, the innermost corner was covered with a piece of adhesive foil. The adhesive foil was then peeled off and the passivation underneath was removed with a diamond scratcher to expose the substrate. Painted-on conductive silver varnish was then used to contact the substrate as well as the PEDOT:PSS gate electrodes.

Two sets of identical samples were prepared, of which the first set was tested by Bias-PCD immediately after having the semitransparent electrodes applied. A second set was prepared with PEDOT:PSS electrodes but tested at a later point in time, with a delay of approximately one month. This was done to investigate whether the aging of the PEDOT:PSS film might influence the charge dynamics at the interfaces.

EXPERIMENTAL DETAILS

To calculate the fixed charge density Q_f of the dielectrics, a simple parallel plate capacitor approximation was assumed. First, the surface charge density present at the gate contact Q_{Gate} is calculated via

$$Q_{Gate} = C\,(V_{Gate} - \Delta V), \tag{1}$$

where $C = \varepsilon_0\varepsilon_r/d$ is the surface capacitance with the vacuum permittivity ε_0, the relative permittivity of the dielectric ε_r ($\varepsilon_{SiO2} = 3.9$,[29] $\varepsilon_{Al2O3} = 9.34$[30]), and the thickness of the dielectric d. V_{Gate} is the voltage at the gate electrode (applied and measured by the Bias-PCD device) and ΔV is the work function difference. A nominal work function of 4.85 eV is assumed for the PEDOT:PSS,[31] which results in $\Delta V_n = 0.58$ V and $\Delta V_p = -0.13$ V for n- and p-type substrates, respectively.[32] To calculate the surface capacitance of the dielectric stacks consisting of part SiO_2 and Al_2O_3, the layers are considered capacitors connected in series.

To derive Q_f from the measured lifetime-over-voltage curve, it is assumed that the minimum represents the flatband condition. The voltage induced charge accumulation exactly cancels out the fixed charge density in the dielectric and Q_f can be readily extracted from the curve,

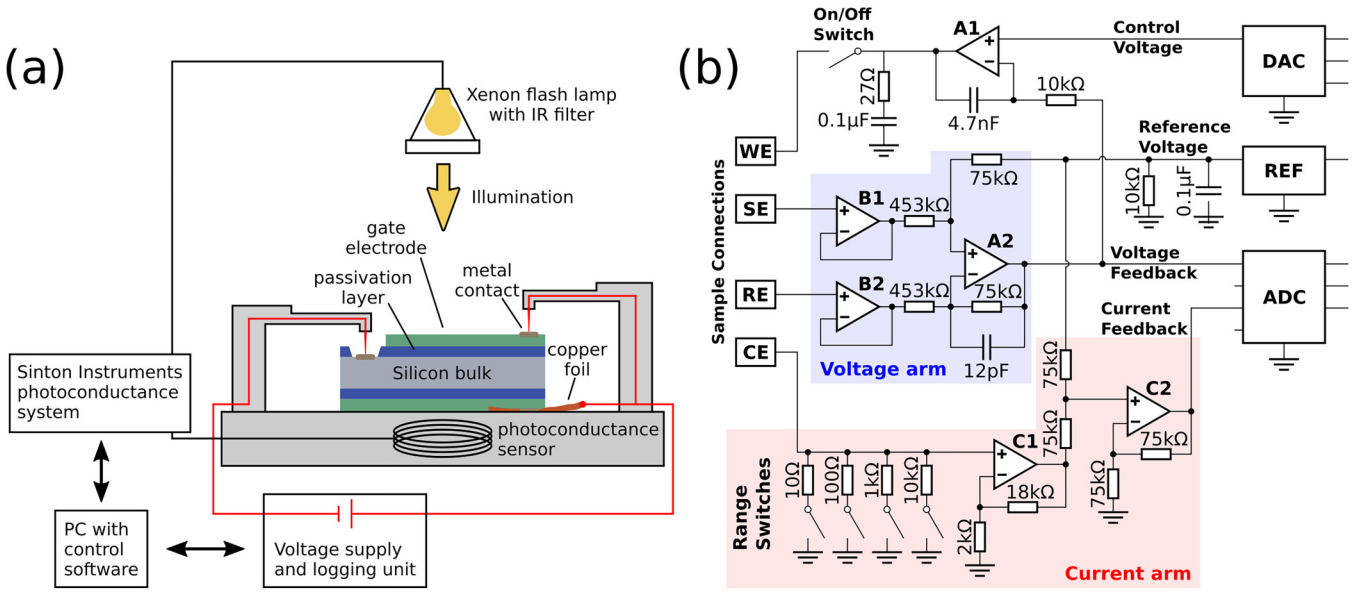

FIG. 1. (a) Schematic overview of the Bias-PCD measurement setup. The sample is prepared with a dielectric passivation layer and semitransparent PEDOT:PSS electrodes. Spring-loaded probes are used to apply a voltage while the PCD measurement is taking place. (b) Electronic circuitry of the voltage supply and logging unit. WE, SE, RE, and CE are the working, sensing, reference, and counter electrodes where the sample gets connected. A1-C2 are the operational amplifiers. On the right side, the digital-analog converter (DAC), reference voltage (REF), and the analog-digital converter (ADC) are visible. The parts of the circuit for measuring voltage and current are marked in blue and red, respectively.

$$Q_f = -Q_{Gate}(V_{min}), \tag{2}$$

with V_{min} as the voltage at which the effective lifetime reaches its local minimum. To obtain Q_f, it is therefore necessary that the lifetime curve shows a minimum and it must be assumed that a higher charge concentration at the surface impacts the lifetime positively.

It is also important to note that this approximation assumes that all charges are found directly at the dielectric/c-Si interface, which can be an oversimplification. However, the sum of charges in the dielectric can be characterized via an effective fixed charge density assuming the charge centroid being at the interface. It is this effective charge that influences the band bending and, consequently, the passivation properties. In the following, Q_f always stands for the effective charge density.

In this study, the samples were submitted to positive bias voltages of up to 12 V. The applied voltage was increased by 0.25 V between each lifetime measurement. After the measurement at the maximum value of 12 V, the voltage was again decreased stepwise, until reaching 0 V again. Figure 2(a) depicts this stepwise voltage increase over multiple measurements. This mode of operation was chosen to gain insights into the charge trapping in the dielectric[33] and to uncover the influence the voltage sweep itself might have on the sample.

Negative voltages were not applied to the samples. Preliminary tests of Al_2O_3-passivated samples showed a significant decrease in effective lifetime after being subject to negative voltage biases. This was also observed in similar studies.[12,34] All samples exhibited a lifetime minimum in the positive voltage region, making negative voltages unnecessary for the determination of Q_f with the method.

In addition to the experimental determination of Q_f, a matlab simulation software,[13] based on the Girisch-Aberle algorithm[15,16] was used to fit the lifetime curves over the full voltage range. The simulation uses a corrected model regarding the charge-induced potential fluctuations at the silicon surface, taking into account the fluctuations of charge concentrations.[13] This was used to generate a set of accurate fits for the determination of Q_f as well as defect density D_{it}. The obtained Q_f was used as a verification for the Q_f obtained directly from the flatband voltage.

RESULTS AND DISCUSSION

Figure 2(a) shows some exemplary Bias-PCD lifetime curves of one of the n-type samples, with a SiO_2 interlayer thickness of 2 nm. The results show that the charge carrier concentration at the interface can readily be controlled via the applied gate voltage. By changing the voltage, the effective lifetime can be manipulated due to changes in the recombination occurring at the surface, controlled by the access that charge carriers have to defects in the bandgap. This way, the specimen can be examined in different states from accumulation to depletion and inversion. As the bias voltage is increased, the curves shift to lower lifetimes until reaching a minimum at +2.5 V, after which the lifetimes increase again toward higher voltages. This implies a transition from inversion to depletion at the flatband voltage of approximately +2.5 V. The increase afterward represents the sample being driven into accumulation.

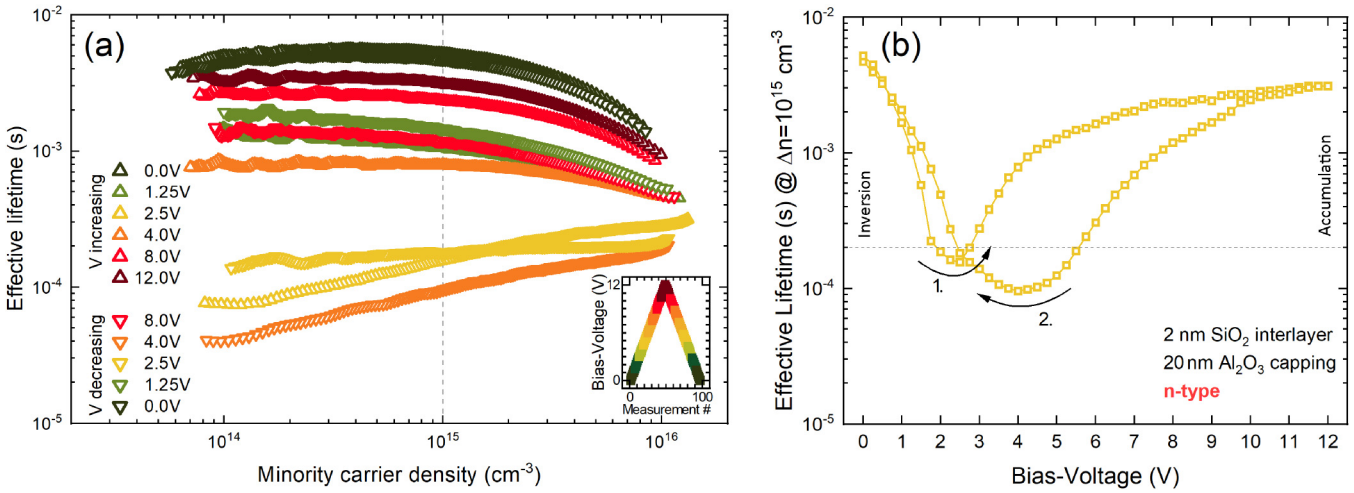

FIG. 2. Effective lifetime measurements of n-type samples with 2 nm SiO_2 interlayer and 20 nm Al_2O_3 capping layer. (a) Bias-PCD effective lifetime curves at some exemplarily chosen voltage values and (b) lifetimes at $\Delta n = 10^{15}$ cm^{-3} for all measured bias-voltage values. The arrows indicate whether the voltage was being increased or decreased.

After the maximum voltage of +12 V is reached, the sweep is repeated in reverse. The lifetime decreases again until reaching its second minimum at +4 V, implying depletion. As the voltage is decreased further toward 0 V, the interface reaches inversion again with an increase in lifetime, recovering to its original value. Figure 2(b) shows the effective lifetimes at a minority carrier density of $\Delta n = 10^{15}$ cm^{-3} for all bias voltages, to give a better overview of the data. A hysteresis effect is evident by a shift of the minimum to a higher voltage and lower lifetime, as well as the broadening of the curve. It can be concluded that the bias-voltage sweep has led to additional charges being trapped in the dielectric layers and a large level of non-uniformity, which is in line with observations made in similar studies.[33] The lower effective lifetime of the minimum means the defect density is higher after the sweep. Furthermore, it is apparent that the sample has a higher maximum lifetime in inversion than in accumulation, seen at the lower lifetime values toward maximum voltage.

The device used for the application of the bias voltage can also be used to perform Bias-Voltage Photoluminescence (Bias-PL) measurements.[35,36] For this, a photoluminescence measurement system was used as reported in Ref. 37. The employed setup can be seen in Fig. 3(a). The voltage was applied to the sample in the same way as with the Bias-PCD measurements. Bias-PL measurements were done every 0.5 V while the voltage was increased from 0 to 12 V. The result of one such voltage sweep can be seen in Fig. 3(b), together with the Bias-PCD measurement results for the same sample.

The Bias-PL lifetime data [purple curve in Fig. 3(b)] follow the same trend observable for the Bias-PCD measurement. With an increase in voltage, the lifetime decreases until a minimum is reached at flatband voltage, after which it increases again toward accumulation. The same behavior can be observed in the PL images in Fig. 3(b), with brighter hues representing higher lifetimes. Our advanced instrumentation to carry out the Bias-PCD method has allowed to evidence a change in charge concentrations in the observed dielectrics. This is proof that our tool enables an additional technique to investigate charging mechanisms while avoiding the previously mentioned challenges posed by other methods. It is noted, however, that a rather large offset in lifetime is visible over the whole voltage range. This is mainly attributed to an artifact of the PL measurements, which were being conducted at a slightly different carrier density than the PCD measurements.

Figures 4(a)–4(d) show the effective lifetimes at $\Delta n = 10^{15}$ cm^{-3} over the whole range of voltages for samples with SiO_2 interlayers of 0, 1, 2, 4, and 10 nm thickness obtained by Bias-PCD. This gives an overview of the lifetime-to-voltage characteristics. The sample shown in Fig. 2 can be found as the yellow curve in Fig. 4(a). The first part of the measurement during which the voltage is increasing is marked with an arrow of the same color.

Figures 4(a) and 4(b) show the voltage-dependent lifetime curves for the n- and p-type samples, which were tested immediately after having the semitransparent gate electrodes applied. Nearly all of them show a clear course of inversion–depletion–accumulation, apart from the sample without SiO_2 interlayer in Fig. 4(a), which shows some irregularities. It is obvious that the positions of the lifetime minima shift toward lower positive voltages with an increase in interlayer thickness. This indicates a higher concentration of effective charge at the interface for a layer stack with thinner SiO_2. Also, the minima show a higher effective lifetime with increasing interlayer thickness. This indicates that D_{it} is lower for higher interlayer thicknesses, which fits the results observed in Ref. 21. The differences between n- and p-type samples also become obvious: n-type samples generally show a higher lifetime, which could be attributed to either a higher bulk lifetime or a better passivation quality. Higher negative fixed charges are also observed in the n-type samples. The hysteresis-like effect is more

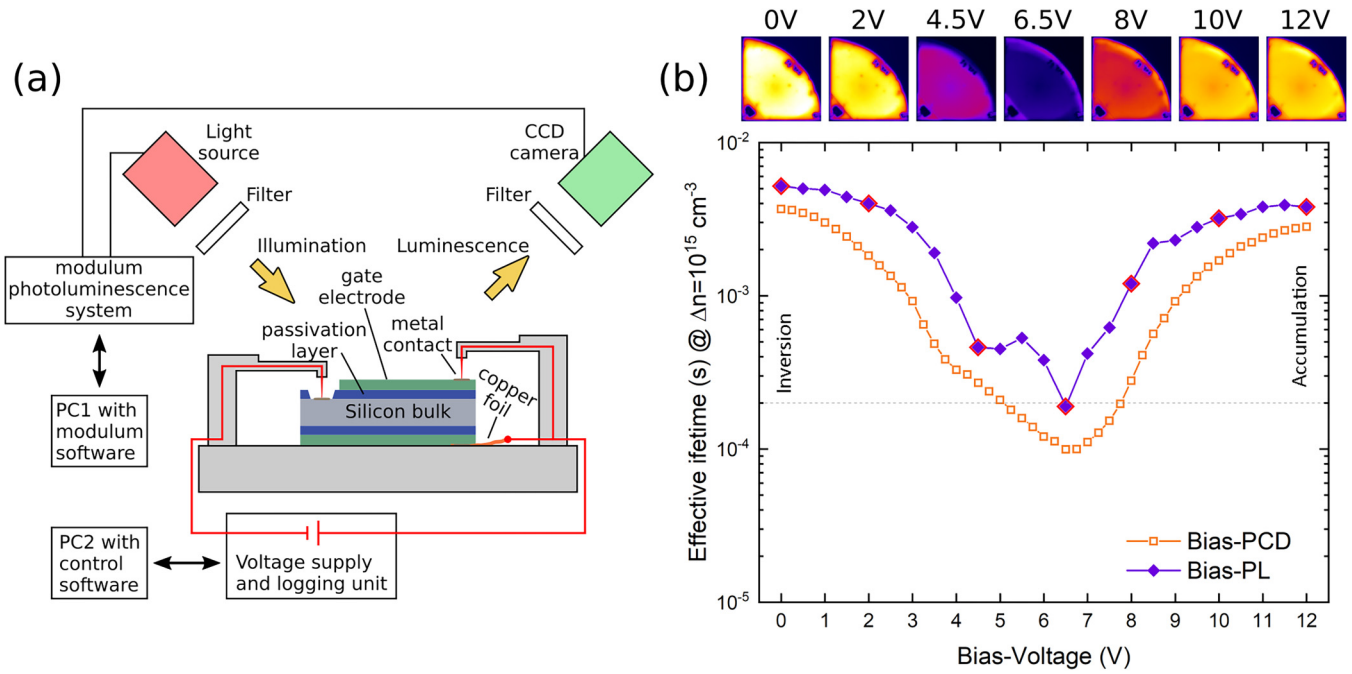

FIG. 3. Bias-Voltage Photoluminescence (Bias-PL) setup and results for an aged sample with a 2 nm SiO_2 interlayer. (a) The setup used for the Bias-PL measurements. The device was added to the modulum photoluminescence system.[38] (b) Comparison of lifetime data obtained by Bias-PCD and Bias-PL. Exemplary photoluminescence pictures at selected voltages are displayed and highlighted in the graph. Brighter hues signify higher effective lifetimes.

pronounced for the n-type samples than for the p-type samples. For the n-type sample without SiO_2 interlayer, some scatter and sudden drops in lifetime are observable while the voltage is being increased. This might be due to sudden shifting or formation of charges at the Si–Al_2O_3 interface, as also seen for samples with AlO_X/SiN_X passivation in Ref. 12. These effects are not yet fully understood and further investigation can be carried out using an advanced Bias-PCD instrument as the one here reported.

In Fig. 4(a), the strong shift of the minimums toward higher voltages after the sweep is visible. It can be concluded that for recently prepared n-type samples, applying a positive gate voltage modifies the charge density at the interface or in the dielectric stack, resulting in a larger amount of fixed negative charges after testing. As this effect is strongest for samples with a thinner SiO_2 interlayer, it seems to be influenced most by the interaction between the Al_2O_3 dielectric layer and the c-Si substrate. In the absence of an interlayer SiO_2, this charge transfer seems to be enhanced, allowing electron injection from silicon into the dielectric. This hysteresis-like effect is less pronounced for the aged samples and for the p-type samples in general.

The lifetime minimums of the p-type samples in Fig. 4(b) lie at comparably lower bias voltages, meaning the passivation layers have a lower negative Q_f. The hysteresis-like effect of the voltage sweeps is also much less prominent than with the n-type samples.

Figures 4(c) and 4(d) show the results for the aged samples. Nearly, all curves exhibit pronounced minimums and much less scattering. The hysteresis is much less pronounced for these samples. This can be due to a saturation of the trap states able to acquire and retain charge levels after bias-voltage testing. Advantageously, there does not seem to be a large degradation of such additional interface charges in the SiO_2/Al_2O_3 layer stack, indicating that they could promote improvements in the passivation of silicon surfaces when used on device structures. It is also observable that lower interlayer thicknesses show a higher lifetime in accumulation than in inversion. Higher interlayer thicknesses result in a higher lifetime when electrons are the majority charge carriers. It is immediately obvious that for all aged samples, the lifetime minima were obtained at considerably higher voltages, meaning the Q_f of the samples increased by aging. For the n-type sample without interlayer (dark green in 4c), no minimum is observable. If a minimum would be observable at higher voltages, this would mean that this sample has accumulated more than 3.0×10^{13} q/cm^2 negative fixed charges.

Figures 5(a) and 5(b) show the Q_f values derived via Eqs. (1) and (2) from the minimum positions of all tested specimens. Q_f is displayed vs the SiO_2 interlayer thickness for all prepared samples. The initial samples are represented by open triangles and the aged samples by closed triangles. Upwards or downwards pointing triangles signify Q_f while the voltage was being increased or decreased, respectively. The Q_f data from Ref. 21 are displayed as a comparison. Additionally, the results for Q_f obtained via the simulation are displayed.

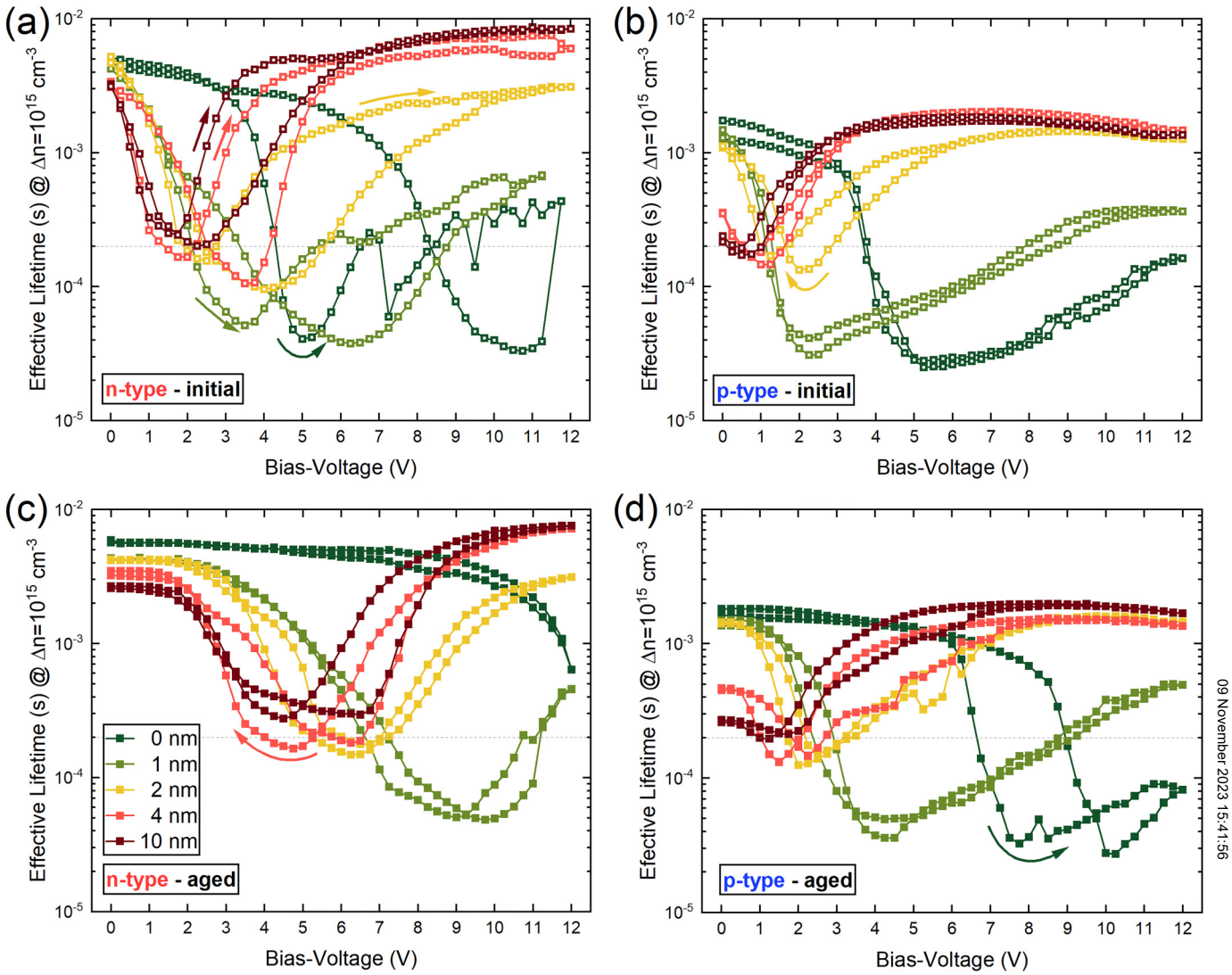

FIG. 4. τ_{eff} evaluated at 10^{15} cm^{-3} as a function of applied bias gate voltage. Results for n- and p-type samples with a SiO_2 interlayer of 0, 1, 2, 4, and 10 nm thickness and a Al_2O_3 capping layer of 10 nm. (a) and (b) show results obtained directly after applying the semitransparent gate electrodes (open) and (c) and (d) were obtained for aged samples (filled). The faint line at 2×10^{-4} s represents the lifetime value below which the exact lifetime values are less reliable due to the application of transient measurements. The arrows indicate the direction of voltage increase (first)/decrease (second) for samples with a pronounced hysteresis.

The overall trend is a continuous decrease in negative fixed charges with growing interlayer thickness for all types of samples. Except for the samples without a SiO_2 interlayer, all n-type samples show a higher negative Q_f than the p-type samples. This suggests that the availability of electrons is involved in the mechanism of fixed charged formation in these dielectrics. Of the initially tested set of samples, the highest Q_f values are observable when Al_2O_3 is applied directly onto the c-Si substrate, reaching approximately -1.1×10^{13} q/cm^2 for n-type and -1.4×10^{13} q/cm^2 for p-type samples. With an increase in interlayer thickness to 10 nm, the negative Q_f values decrease to -1.4×10^{12} q/cm^2 for the n-type samples and as far as approximately -7.4×10^{11} q/cm^2 for the p-type samples.

The initial n-type samples in Fig. 5(a) are in good agreement with the results obtained in Ref. 21 and with the values obtained with the simulation. After being subject to an increasing voltage sweep however, the Q_f values are increased by a factor of approximately 2, deviating strongly from the comparison data in Ref. 21. Applying a positive bias voltage has a very pronounced impact on the amount of fixed charges at these interfaces, with values as high as -2.6×10^{13} q/cm^2 being reached. The amount of trapped charges that can be activated by the voltage sweep is proportional

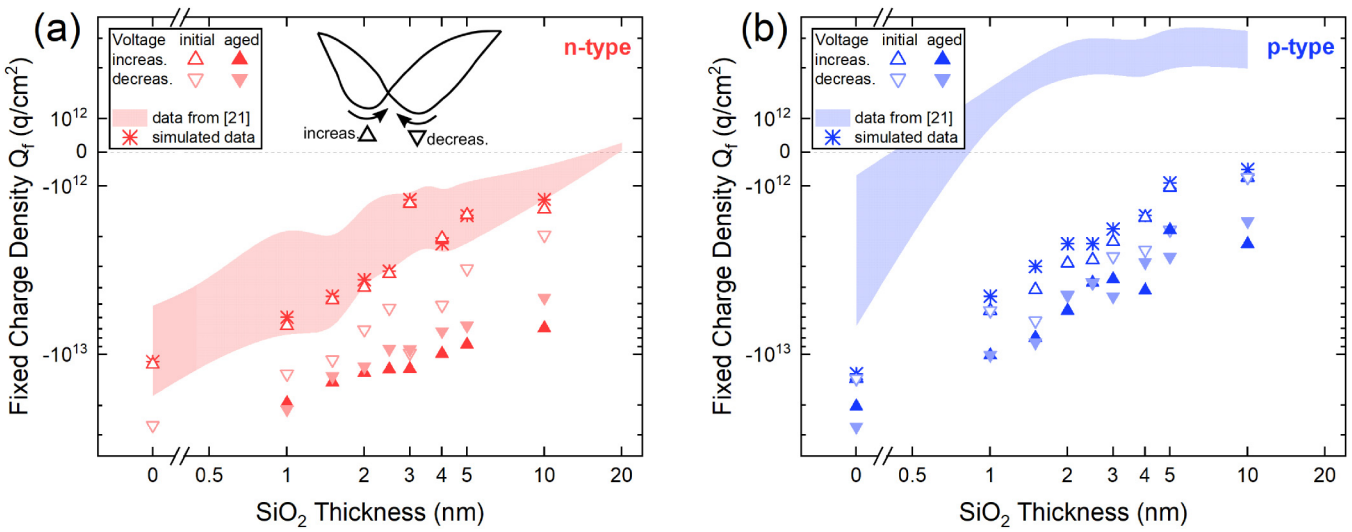

FIG. 5. Fixed charge densities as a function of SiO_2 interlayer thickness. Open triangles represent samples tested directly after the application of the PEDOT:PSS gates. Filled triangles represent the samples tested approximately 30 days later. The shapes represent if voltage was increasing (upwards triangle) or decreasing (downwards triangle) at this minimum. The colored areas signify the range of values measured in Ref. 19. Stars show results obtained via simulation.

to the amount of fixed charges already present in the dielectric. These findings correlate well with the findings in Refs. 33 and 34. However, an inversion of the fixed charges for higher SiO_2 thicknesses could not be observed here as it was in Ref. 21. It can be concluded that the thickness of the SiO_2 interlayer impedes charge formation during sample preparation as well as during the Bias-PCD measurement process. This is in good accordance with the findings of similar studies.[20,21,33,39,40]

Also visible in Fig. 5(a) is the influence of aging on the n-type samples. The application of the PEDOT:PSS gate electrodes seems to initiate a process by which the amount of interface charges gets increased. This effect was not visible with reference samples where the PEDOT:PSS was applied directly before the first measurements. This process, however, seems to take place over multiple weeks, as it is only visible with the samples measured approximately 1 month after the PEDOT:PSS was applied. This process also seems to change the way in which further voltage sweeps affect the samples: nearly all aged samples show a decrease in Q_f after the sweep to +12 V, rather than an increase. This decrease in Q_f, however, is much less drastic than with the initial samples.

It must be noted that a minimum for the aged sample without SiO_2 was not obtainable before or after the sweep. This could be due to the sample exhibiting an unusual high amount of fixed charges, which would result in a minimum at a voltage value beyond +12 V, which would thus not be acquirable with the current Bias-PCD setup. The possibility of the actual voltage deviating strongly from the applied voltage was ruled out by a set of voltage measurements at the gate electrodes during measurements. These showed a maximal deviation of ±0.5 V, so even under conservative assumptions Q_f must either be lower than -3.0×10^{13} q/cm^2 or simply must not be obtainable on this sample with the Bias-PCD method.

Figure 5(b) shows the results for the p-type samples. The general trend is overall the same as for the n-type samples, with Q_f becoming less negative with increasing SiO_2 thickness. Q_f values are generally lower for p-type, lining up with what similar studies have found.[21,33] The hysteresis-like effect is much less pronounced for this set of samples and there is no clear visible tendency of increased or decreased Q_f after the sweep. This was also observed in Ref. 34 but is contrasting with what was found in Ref. 33, requiring further studies. While the effect of aging is observable, it is much less intense than for the n-type substrates. The data from a study of a similar set of samples measured via capacitance–voltage[21] found much more positive Q_f values for the p-type samples [as seen in Fig. 5(b)], but very similar Q_f for the n-type samples. Another similar study, however, showed a similar overall trend as seen here.[20] It must be noted that the differences between the sample types could also stem from the fact that the doping level varied by approx. a factor of three between the n- and the p-type samples (approx. 5.0×10^{15} cm^{-3} for n-type and 1.5×10^{16} cm^{-3} for p-type). Further studies are needed to verify whether the carrier density might influence the susceptibility of the samples to hysteresis-like effects.

To obtain the D_{it} values for the different curves and to verify the Q_f values obtained above, a simulation software by Bonilla *et al.* was used to fit the sweep data.[13] Only the part of the measurements during which the voltage was being increased was fitted. Figure 6(a) shows the fits obtained for n- and p-type samples with interlayer thicknesses of 1 and 10 nm together with the respective Bias-PCD data. The resulting D_{it} midgap values are shown in Fig. 6(b), together with the comparative capacitance–voltage data from Ref. 21. For both types of samples, an overall trend of decreasing D_{it} is observable for an increase in SiO_2 thickness. p-type samples showed a higher defect density at all

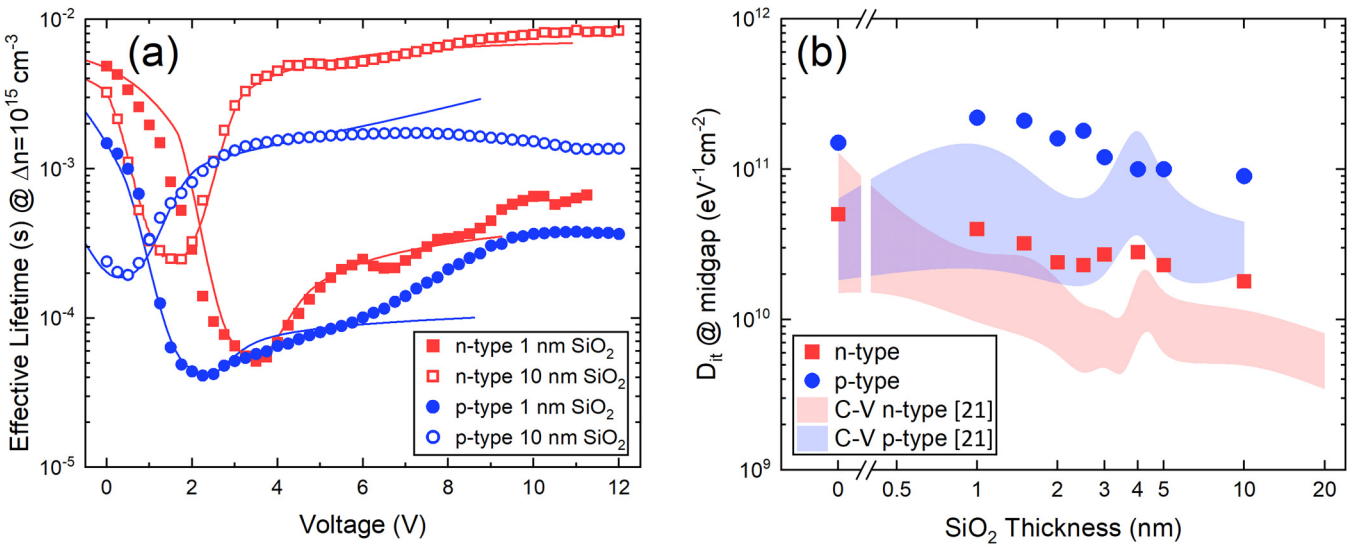

FIG. 6. (a) τ_{eff} evaluated at 10^{15} cm^{-3} as a function of applied bias gate voltage. Shown here are the results for the initial n- and p-type samples with a SiO_2 interlayer of 1 and 10 nm and an Al_2O_3 capping layer of 10 nm. The data were obtained while the voltage was being increased stepwise from 0 to 12 V. Lines indicate the fit using the simulation. (b) Defect densities D_{it} obtained from the fits for all initial samples. The colored areas signify the range of values from Ref. 21.

thicknesses. Both observations are in line with the results from Ref. 21 and also conform to the observation that SiO_2 generally is the passivation material, which forms interface layers with the lowest defect density D_{it} on c-Si substrates.[2] At most thicknesses, the samples show a higher D_{it} than the comparison data; however, it must be noted that the D_{it} obtained in Ref. 21 were surprisingly low in comparison to other studies,[13] possibly because of an underestimation of D_{it} in the C–V data. It must also be noted that all fits resulted in capture ratios $k = \sigma_n/\sigma_p$ of approximately 0.25, as was also observed by Bonilla *et al.*[13] An additional possible explanation for the deviation of the data could be the potential fermi-level dependence of the D_{it} of the samples. Additional research is needed to verify or refute this, as this dependence was not considered in this work.

CONCLUSIONS

The Bias-PCD method is shown to be a cost-effective and easy-to-use expansion of the established and widespread photoconductance lifetime measurement setup. It can be used to extract Q_f of adequately prepared n- and p-type c-Si samples in a wide range of values, while also granting insight into more detail of charge dynamics at the interface. By expanding it to a fully automated measurement method, a large number of samples can be characterized in a short time, providing key insights into the passivation mechanisms obtained for different dielectric thin films. The device employed in this work can be used as a simple add-on to an existing photoconductance measurement setup with the industry standard WCT-120.

The properties of n- and p-type samples with stack passivation of PEALD SiO_2/Al_2O_3 were shown to be highly dependent on the thickness of the SiO_2 interlayer. Very high (-1.4×10^{13} q/cm^2) fixed charge densities Q_f were observed when no SiO_2 interlayer was present. Q_f decreased with an increase in interlayer thickness. As this decreases the influence of the field-effect passivation, lifetimes also declined. n- and p-type samples showed relatively similar Q_f values in the initial state, with the values for n-type being generally slightly higher. Subjecting the n-type samples to the +12 V Bias-PCD voltage sweeps resulted in an increase in Q_f at the interface. This hysteresis-like effect was much less pronounced for the p-type samples. Both n- and p-type samples showed an increase in Q_f after aging, as well as a change in response to further voltage sweeps. n-type samples, in particular, showed a reverse in hysteresis behavior, with positive voltage sweeps lowering Q_f at the interface.

Crucial charge dynamics are taking place at this important interface, and so the electrical history of the interface is of key importance when assessing its passivation performance and potential deployment to device architectures.

ACKNOWLEDGMENTS

The authors would like to thank A. Leimenstoll, F. Schätzle, K. Zimmermann, E. Sarıgül, and H. Patel for support during the preparation of the samples and deposition of the layers. This work was funded by the German Ministry of Economic Affairs and Energy under Grant No. 03EE1031A "PaSodoble." R.S.B. was supported by the Royal Academy of Engineering under the Research Fellowship scheme and by the UK Engineering and Physical Sciences Research Council under Grant No. EP/V038605/1.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Paul Masuch: Data curation (equal); Formal analysis (equal); Investigation (equal); Software (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Christian Reichel:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Ruy Sebastian Bonilla:** Data curation (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Armin Richter:** Conceptualization (supporting); Investigation (equal); Supervision (supporting); Writing – review & editing (equal). **Jan Benick:** Conceptualization (supporting); Validation (supporting); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]A. G. Aberle *et al.*, "Limiting loss mechanisms in 23% efficient silicon solar cells," J. Appl. Phys. **77**(7), 3491–3504 (1995).
[2]R. S. Bonilla, B. Hoex, P. Hamer, and P. R. Wilshaw, "Dielectric surface passivation for silicon solar cells: A review," Phys. Status Solidi A **214**(7), 1700293 (2017).
[3]J. Schmidt, R. Peibst, and R. Brendel, "Surface passivation of crystalline silicon solar cells: Present and future," Sol. Energy Mater. Sol. Cells **187**, 39–54 (2018).
[4]A. G. Aberle, "Overview on SiN surface passivation of crystalline silicon solar cells," Sol. Energy Mater. Sol. Cells **65**(1–4), 239–248 (2001).
[5]A. Cuevas *et al.*, "Carrier population control and surface passivation in solar cells," Sol. Energy Mater. Sol. Cells **184**, 38–47 (2018).
[6]D. K. Schroder, in *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley, Hoboken, NJ, 2006).
[7]M. Schofthaler, R. Brendel, G. Langguth, and J. H. Werner, "High-quality surface passivation by corona-charged oxides for semiconductor surface characterization," in *Proceedings of 1994 IEEE 1st World Conference on Photovoltaic Energy Conversion - WCPEC (A Joint Conference of PVSC, PVSEC and PSEC), Waikoloa, HI, USA* (IEEE, 1994), pp. 1509–1512.
[8]F. Werner *et al.*, "Very low surface recombination velocities on p- and n-type c-Si by ultrafast spatial atomic layer deposition of aluminum oxide," Appl. Phys. Lett. **97**(16), 162103 (2010).
[9]A. Beyer, M. Rennau, and G. Ebest, "Corona charging of insulated surfaces and the application in the photovoltaic," in *Paper Presented at the 13th European Photovoltaic Solar Energy Conference* (H.S. Stephens, 1995), p. 1254; available at https://books.google.de/books/about/Thirteenth_European_Photovoltaic_Solar_E.html?id=GwVOxgEACAAJ&redir_esc=y
[10]W. E. Jellett and K. J. Weber, "Accurate measurement of extremely low surface recombination velocities on charged, oxidized silicon surfaces using a simple metal-oxide-semiconductor structure," Appl. Phys. Lett. **90**(4), 042104 (2007).
[11]E. Suzuki, H. Takato, K. Ishii, and Y. Hayashi, "Evaluation of the Si-SiO_2 interface by the measurement of the surface recombination velocity S by the dual-mercury probe method," Jpn. J. Appl. Phys. **29**(12), L2300–L2303 (1990).
[12]R. S. Bonilla, "Controlling surface carrier density via a PEDOT:PSS gate: An application to the study of silicon-dielectric interface recombination," Solar RRL **2**(10), 1800172 (2018).
[13]R. S. Bonilla, I. Al-Dhahir, M. Yu, P. Hamer, and P. P. Altermatt, "Charge fluctuations at the Si–SiO_2 interface and its effect on surface recombination in solar cells," Sol. Energy Mater. Sol. Cells **215**, 110649 (2020).
[14]Sinton Instruments, see https://www.sintoninstruments.com/products/wct-120 for "WCT-120, Sinton Instruments" (accessed 7 March 2022).
[15]R. B. M. Girisch, R. P. Mertens, and R. F. De Keersmaecker, "Determination of Si-SiO/sub 2/interface recombination parameters using a gate-controlled point-junction diode under illumination," IEEE Trans. Electron Devices **35**(2), 203–222 (1988).
[16]A. G. Aberle, S. Glunz, and W. Warta, "Impact of illumination level and oxide parameters on Shockley–Read–Hall recombination at the Si-SiO_2 interface," J. Appl. Phys. **71**(9), 4422–4431 (1992).
[17]G. Dingemans, W. Beyer, M. C. M. van de Sanden, and W. M. M. Kessels, "Hydrogen induced passivation of Si interfaces by Al_2O_3 films and SiO_2/Al_2O_3 stacks," Appl. Phys. Lett. **97**(15), 152106 (2010).
[18]J. Benick, A. Richter, M. Hermle, and S. W. Glunz, "Thermal stability of the Al_2O_3 passivation on p-type silicon surfaces for solar cell applications: Thermal stability of the Al_2O_3 passivation on p-type surfaces," Phys. Status Solidi RRL **3**(7–8), 233–235 (2009).
[19]A. Richter, S. W. Glunz, F. Werner, J. Schmidt, and A. Cuevas, "Improved quantitative description of Auger recombination in crystalline silicon," Phys. Rev. B **86**(16), 165202 (2012).
[20]N. M. Terlinden, G. Dingemans, V. Vandalon, R. H. E. C. Bosch, and W. M. M. Kessels, "Influence of the SiO_2 interlayer thickness on the density and polarity of charges in $Si/SiO_2/Al_2O_3$ stacks as studied by optical second-harmonic generation," J. Appl. Phys. **115**(3), 033708 (2014).
[21]A. Ek, C. Reichel, A. Richter, and J. Benick, "Influence of layer thickness on passivation properties in SiO_x/Al_2O_3 stacks," J. Appl. Phys. **127**(23), 235303 (2020).
[22]O. Abdulrazzaq *et al.*, "Comparative aging study of organic solar cells utilizing polyaniline and PEDOT:PSS as hole transport layers," ACS Appl. Mater. Interfaces **7**(50), 27667–27675 (2015).
[23]T. Dobbelaere, P. M. Vereecken, and C. Detavernier, "A USB-controlled potentiostat/galvanostat for thin-film battery characterization," HardwareX **2**, 34–49 (2017).
[24]Arduino, see https://docs.arduino.cc/hardware/nano for "Nano | Arduino Documentation" (accessed 7 March 2022).
[25]R. A. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," Appl. Phys. Lett. **69**(17), 2510–2512 (1996).
[26]W. Kern, "The evolution of silicon wafer cleaning technology," J. Electrochem. Soc. **137**(6), 1887–1892 (1990).
[27]N. E. Grant, V. P. Markevich, J. Mullins, A. R. Peaker, F. Rougieux, and D. Macdonald, "Thermal activation and deactivation of grown-in defects limiting the lifetime of float-zone silicon," Phys. Status Solidi RRL **10**(6), 443–447 (2016).
[28]Heraeus, see https://www.heraeus.com/media/media/hec/documents_hec/data_sheets_hep/Clevios_F_HC_Solar.pdf for "CLEVIOSTM F HC Solar."
[29]P. R. Gray, in *Analysis and Design of Analog Integrated Circuits*, 5th ed. (Wiley, New York, 2009).
[30]K. Z. Rajab *et al.*, "Broadband dielectric characterization of aluminum oxide (Al_2O_3)," J. Microelectron. Electron. Packag. **5**(1), 2–7 (2008).
[31]A. M. Nardes, M. Kemerink, M. M. de Kok, E. Vinken, K. Maturova, and R. A. J. Janssen, "Conductivity, work function, and environmental stability of PEDOT:PSS thin films treated with sorbitol," Org. Electron. **9**(5), 727–734 (2008).
[32]S. M. Sze, in *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, NY, 1981).
[33]P. M. Jordan, D. K. Simon, T. Mikolajick, and I. Dirnstorfer, "Trapped charge densities in Al_2O_3-based silicon surface passivation layers," J. Appl. Phys. **119**(21), 215306 (2016).
[34]H. Patel, C. Reichel, A. Richter, P. Masuch, J. Benick, and S. W. Glunz, "Effective charge dynamics in Al_2O_3/SiO_2 multilayer stacks and their influence on silicon surface passivation," Appl. Surf. Sci. **579**, 152175 (2022).
[35]H. Haug, Ø Nordseth, E. V. Monakhov, and E. S. Marstein, "Photoluminescence imaging under applied bias for characterization of Si surface passivation layers," Sol. Energy Mater. Sol. Cells **106**, 60–65 (2012).

[36]H. Haug, S. Olibet, Ø Nordseth, and E. Stensrud Marstein, "Modulating the field-effect passivation at the SiO_2/c-Si interface: Analysis and verification of the photoluminescence imaging under applied bias method," J. Appl. Phys. **114**(17), 174502 (2013).
[37]J. A. Giesecke, B. Michl, F. Schindler, M. C. Schubert, and W. Warta, "Minority carrier lifetime of silicon solar cells from quasi-steady-state photoluminescence," Sol. Energy Mater. Sol. Cells **95**(7), 1979–1982 (2011).
[38]Fraunhofer ISE, see https://www.ise.fraunhofer.de/en/research-projects/modulum.html for "modulum—Novel Characterization Tool for Photovoltaics," Fraunhofer Institute for Solar Energy Systems ISE (accessed 7 March 2022).
[39]D. K. Simon, P. M. Jordan, I. Dirnstorfer, F. Benner, C. Richter, and T. Mikolajick, "Symmetrical Al_2O_3-based passivation layers for p- and n-type silicon," Sol. Energy Mater. Sol. Cells **131**, 72–76 (2014).
[40]G. Dingemans, N. M. Terlinden, M. A. Verheijen, M. C. M. van de Sanden, and W. M. M. Kessels, "Controlling the fixed charge and passivation properties of $Si(100)/Al_2O_3$ interfaces using ultrathin SiO_2 interlayers synthesized by atomic layer deposition," J. Appl. Phys. **110**(9), 093715 (2011).