An Efficient and Linear SSPA With Embedded Power Flexibility for *Ka*-Band Downlink SatCom Applications

Rocco Giofrè, *Senior Member, IEEE*, Lorena Cabrìa, Rémy Leblanc, Mariano López, Fabio Vitobello, and Paolo Colantonio, *Senior Member, IEEE*

***Abstract*— This article presents the design, realization, and experimental characterization of a solid-state power amplifier (SSPA) conceived for *Ka*-band downlink (17.3–20.2 GHz) satellite communication (SatCom) applications. To the best of the author's knowledge, this is the first space-borne SSPA realized for this peculiar application to achieve a technology readiness level of 5, entirely based on European technologies. All the activities carried out during the development phase will be discussed, starting from the power budget analysis, moving through the *ad hoc* design and characterization of the elementary 10-W microwave monolithic integrated circuits (MMICs) power amplifier (PA) in the 100-nm gate length gallium nitride (GaN) on silicon technology, and ending with the circuit solutions conceived to achieve state-of-the-art performance like saturated output power larger than 125 W with a gain and an overall efficiency better than 70 dB and 22%, respectively, while satisfying all the space-derating rules. The SSPA is composed of two subunits: the radio-frequency tray (RFT) to amplify the useful RF signal and the electronic power conditioner (EPC) to interface the module with the satellite primary bus, to actuate remote telecommand/telemetry services and to set different operating modes. The latter is based on a space-qualified microcontroller, whereas the former exploits a low-loss radial splitter/combiner structure in the waveguide to spatially combine the power provided by 16 elementary 10-W MMIC PA. The RFT also includes an input and output isolator, a gain control unit (GCU), a driver, and an analog linearizer. The latter helps to achieve a noise-to-power ratio (NPR) better than 18 dB when the SSPA is tested with a white-noise-like signal having a peak-to-average power ratio (PAPR) of 10 dB and an instantaneous bandwidth of 2.9 GHz. In this working condition, the SSPA provides an average output power and efficiency close to 100 W and 22%, respectively. Finally, it is worth mentioning that the SSPA is equipped with a power flexibility feature that allows it to reduce its power consumption up to 20%, depending on the actual RF power needed at the satellite level.**

***Index Terms*— Gallium nitride (GaN), noise-to-power ratio (NPR), power spatial combining techniques, satellite communications (SatCom), solid-state power amplifiers (SSPAs).**

Manuscript received 10 July 2023; revised 7 September 2023 and 2 October 2023; accepted 3 October 2023. This work was supported by the European Union's Horizon 2020 Research and Innovation Programme under Grant 821830. *(Corresponding author: Rocco Giofrè.)*

Rocco Giofrè and Paolo Colantonio are with the Electronics Engineering Department, University of Rome Tor Vergata, 00133 Rome, Italy (e-mail: giofr@ing.uniroma2.it; paolo.colantonio@uniroma2.it).

Lorena Cabrìa and Mariano López are with TTI Norte, 39011 Santander, Spain (e-mail: lcabria@ttinorte.es; mlopez@ttinorte.es).

Rémy Leblanc is with Macom European Semiconductor Center (MESC), 94450 Limeil-Brévannes, France (e-mail: remy.leblanc@macom.com).

Fabio Vitobello is with the European Commission, 1040 Brussels, Belgium (e-mail: fabio.vitobello@ec.europa.eu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TMTT.2023.3322866.

Digital Object Identifier 10.1109/TMTT.2023.3322866

I. Introduction

SATELLITE communication (SatCom) services have become essential in our interconnected world, bridging the connectivity gap in remote and underserved areas. These services are utilized across various industries, including telecommunications, broadcasting, maritime, aviation, emergency response, and scientific research [1], [2]. Satellites provide reliable and wide-reaching coverage, enabling voice, data, and multimedia communication services. They play a vital role in enabling global connectivity, ensuring that people, businesses, and communities can stay connected regardless of their geographic location. As the ground network continues to advance with 5G and beyond [3], SatCom will continue to evolve, offering even faster data rates, higher capacity, and expanded capabilities, further enhancing the interoperability of our global communication infrastructure [4].

To support this evolution, the next step is the deployment of constellations of very-high-throughput satellites (vHTSs), which will have communication capacity even larger than 1 Tb/s per satellite, fully integrated with the terrestrial network and with high coverage and power flexibility [5], [6]. To this aim, technology breakthroughs at the payload level are needed. For instance, the use of complex modulated signals with a large peak-to-average power ratio (PAPR) is envisaged to maximize the data rate, thus the linearity of the transmitted signal will be a crucial figure of merit. Additionally, active antenna arrays together with solutions to maximize the efficiency of the system while reducing the output power are expected, to guarantee both coverage and power flexibility [7], [8]. These are relatively new concepts for space applications, which have to be added to the typical requirements such as high reliability, good thermal management, low size, and weight [9]. This scenario clearly complicates the design of power amplifiers (PAs), whose performances, considering the typical requirement of hundreds of watts needed at the satellite level, dramatically affect those of the overall payload. Indeed, the PA is the most power-hungry element, thus affecting the efficiency and thermal management of the payload, as well as the main responsible for the transmitted signal quality due to

its spectral regrowth. Also, mass and volume are significantly affected by the PA, since it is made redundant to face possible reliability issues [10].

High power at high frequency in space applications is traditionally linked to the adoption of traveling wave tube amplifiers (TWTAs), as power stage [11]. However, advancements in solid-state technologies, such as gallium nitride (GaN), nowadays offer potential solutions to realize solid-state PAs (SSPAs) addressing space challenges while introducing significant benefits with respect to TWTAs, such as lower hardware cost, absence of heating time, graceful degradation, enhanced flexibility, and so on [10], [12]. Efforts are continuously being made to develop high-performance SSPAs that try to strike the right balance among challenging and contrasting features such as power efficiency, thermal management, signal quality, space constraints, and many others [13], [14], [15], [16], [17], [18].

This article provides an additional contribution to this race, presenting the design, realization, and complete experimental characterization of an SSPA conceived for Ka-band downlink (17.3–20.2 GHz) SatCom applications. To the best of the author's knowledge, this is the first space-borne SSPA realized for the Ka-band, entirely based on European technologies, to achieve a technology readiness level of 5, which means that the SSPA has been validated in the relevant environment [19]. This article extends the content of the international microwave symposium (IMS) conference contribution [20], adding more insights into the SSPA design, above all stressing the conceived circuit solutions that have enabled the achievement of remarkable experimental results reported hereafter, and not included in [20]. In particular, the outcomes of the verification tests campaign will be detailed, including thermal and vacuum tests as well as the linearity performance in terms of the noise-to-power ratio (NPR) with modulated signals having PAPR and instantaneous bandwidth of 10 dB and 2.9 GHz, respectively.

This SSPA is the main outcome of a research project named FLEXGAN [21], founded under the H2020 program of the European Union. The team is composed of five entities: TTI Norte, Tecnnalia, Macom European Semiconductor Center (MESC), AIRBUS, and the E.E.Dept. of the University of Rome Tor Vergata.

This article is organized as follows. The SSPA concept and architecture are presented in Section II, discussing the innovative circuit solutions conceived during its development. The results of the experimental characterization, ranging from small- to large-signal measurements, thermal-vacuum cycles, and linearity characterization, are reported and discussed in Section III. Conclusions are drawn in Section IV.

II. SSPA Concept and Architecture

The main requirements of the SSPA, listed in Table I, have been defined by AIRBUS accounting for the expected needs of vHTSs. Three nominal operating points (NOPs) are foreseen, depending on the peculiarity of the signal to be amplified (continuous wave (CW) for NOP1 and multicarrier having up to 2.9-GHz instantaneous bandwidth and 10-dB PAPR, for NOP2 and NOP3) and the linearity level, in terms of NPR, to be achieved.

TABLE I
Requirements of the SSPA

Requirement	Value	Unit	Note
Frequency	17.3-20.2	GHz	
Pout@Sat	125	W	NOP1
Pout@18 dB NPR	65	W	NOP2
Pout@13 dB NPR	100	W	NOP3
Max Gain	70	dB	@NOP1
PAE	>25	%	@NOP1
PAE	>20	%	@NOP2
PAE	>23	%	@NOP3
Weight	<3	Kg	
Base Plate Temp.	-5 to 65	°C	
Power Supply	100	V	Regulated

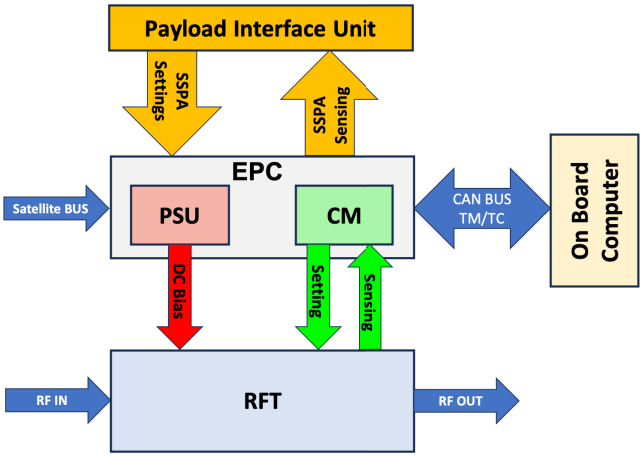
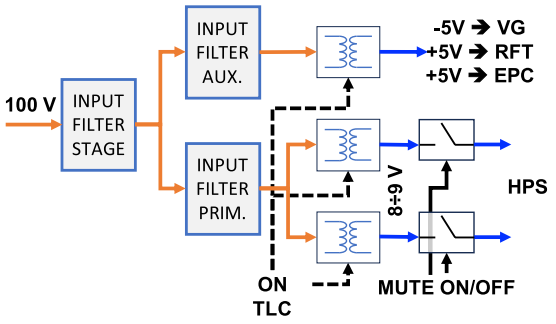


Fig. 1. Block diagram of the SSPA.

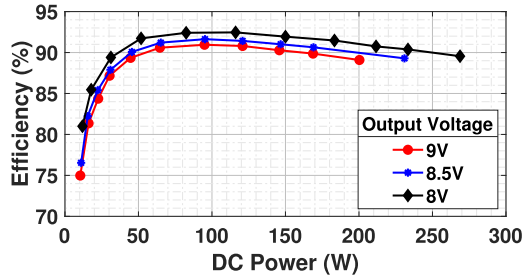
For the development of the flexible Ka-Band SSPA, the architecture depicted in Fig. 1 was proposed. It is composed of two main units: the low-frequency unit, named electronic power conditioner (EPC), and the radio-frequency tray (RFT) based mainly on GaN technology.

A. Electronic Power Conditioner Implementation

The EPC is divided into two subsystems: the power supply unit (PSU) and the control module (CM). The PSU interfaces the SSPA with the satellite external bus (100 V), thus providing the dc bias voltages to the SSPA internal devices. It is composed of the cascade of two filtering stages, needed to comply with the EMI/EMC requirements, followed by three galvanic isolated dc/dc converters, as shown in Fig. 2(a). In particular, one converter is used to provide the regulated voltage, from 5 to −5 V, to the low-power components of the RFT, whereas the other two feed the GaN power stages with a secondary voltage from 8 to 9 V. Considering the high power demanded to these converters, asynchronous half-bridge topology based on GaN switching devices with hysteretic mode control has been adopted. Moreover, a switching circuitry is embedded in the supply path to ensure the adequate biasing sequence of the normally-ON devices of the RFT. The PSU components have been selected accounting for their operating conditions, that is, peak current, peak voltage, and maximum temperature,



(a)



(b)

Fig. 2. (a) Schematic of the PSU and (b) its measured efficiency as a function of the delivered dc power for different secondary voltages.

also applying the space-derating standard. Fig. 2(b) shows its measured efficiency as a function of the delivered dc power for different secondary voltages, from 8 to 9 V. Efficiency values are in the range of 87%–93% for delivered output power larger than 40 W. It is worth mentioning that 9 V is the nominal drain bias voltage of the *ad hoc* designed MMIC PAs, whereas the feature of varying remotely the PSU output voltage down to 8 V was conceived to enable the SSPA power flexibility feature.

The CM is implemented relying upon a space-qualified microcontroller (SAMV71Q21RT from Microchip). As shown in Fig. 3, it implements the telemetry/telecommand (TM/TC) services as well as the remote control through the CAN bus. It monitors the SSPA behavior in terms of gain, power delivered, temperature in GaN devices, and so on and sets the internal parameters (i.e., the control signals) to actuate either the fixed gain mode (FGM) or the automatic level control (ALC) operating condition. In particular, when the FGM is enabled, the SSPA has to change and maintain a fixed gain value defined by the onboard computer (user), whereas when the ALC is ON, it has to maintain the output power selected by the user despite input power variation, from −18 to −29 dBm (i.e., IBO + 1 dB to IBO − 10 dB). Finally, if the satellite operator needs less output power, for instance, because of better weather conditions or coverage reallocation, the CM can enable the power flexibility feature.

B. RFT Design and Implementation

The RFT is conceived to properly amplify the input multicarrier signal from −19 dBm up to the required output power levels reported in Table I while assuring high linearity

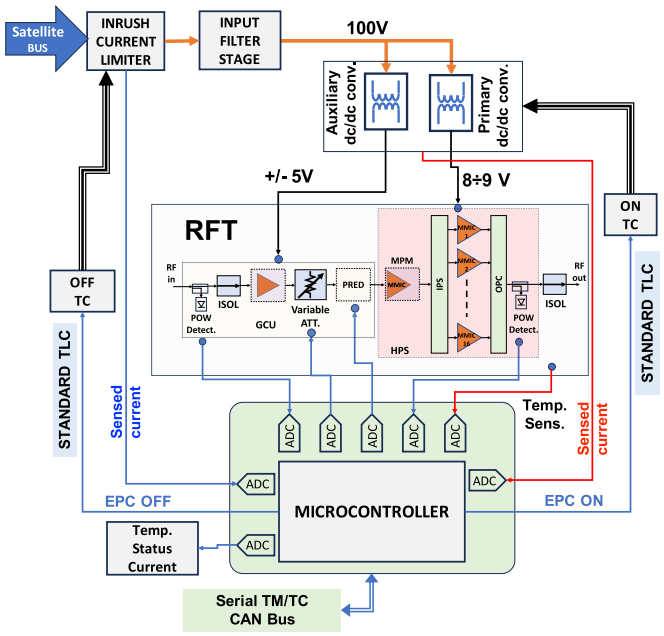


Fig. 3. CM architecture.

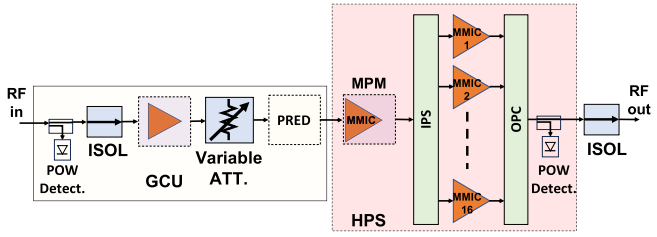
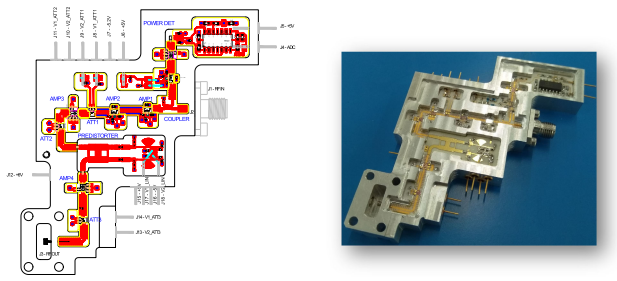


Fig. 4. Block diagram of the RFT of the SSPA.

and efficiency performance. It was divided into two main units: gain control unit (GCU) and high power section (HPS), as graphically depicted in Fig. 4.

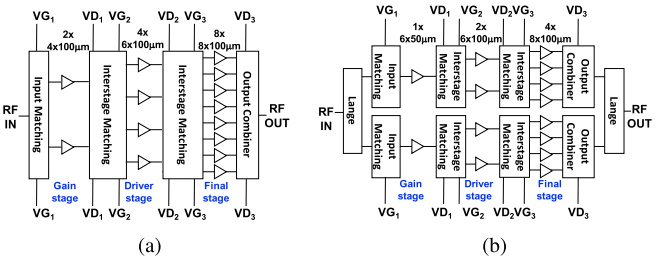
The GCU includes a signal conditioning part and an analog linearizer. The former, based on several commercial space-qualified MMIC low-level amplifiers (LLAs) and attenuators (ATTs), allows to set the different working modes of the SSPA (either FGM or ALC), as well as to compensate for thermal/aging variations of all electronic components present in the channel. The linearizer, composed of a 90° hybrid coupler loaded by two parallel Schottky diodes, was introduced to compensate for the unavoidable phase and amplitude distortions of the downstream MMIC PAs. The final layout and the photograph of the realized GCU are shown in Fig. 5, whereas its performance has been already discussed in [20], thus they are not reported here. In summary, the GCU can compensate up to 4.5 dB and 32° of gain compression and phase expansion, respectively.

The HPS represents the most challenging unit of this SSPA. Accounting for the requirements in Table I and the features of the selected MMIC technology, its architecture was derived through a power budget analysis. The idea is to combine 16 GaN MMIC PAs by using highly efficient spatial power-combining techniques. For its development, the research work was conducted following two main paths in parallel.



(a) (b)

Fig. 5. (a) Final layout and (b) photograph of the realized GCU.



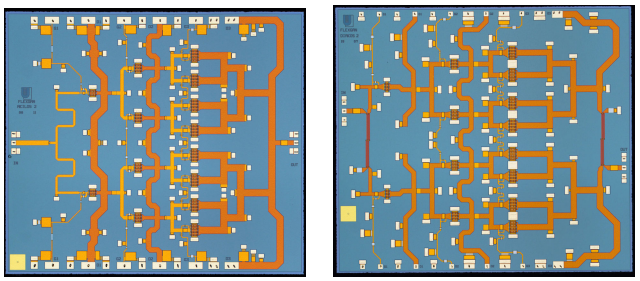
(a) (b)

Fig. 6. MMIC investigated architectures. (a) Corporate. (b) Balanced.

The first one was related to the *ad hoc* design of a high-efficiency and linear 10-W MMIC PA based on the commercially available and space-evaluated 100-nm GaN-Si technology of MESC, to be used as an elementary brick. It is important to highlight that the choice of not using different monolithic technology, such as GaN on silicon carbide (GaN-SiC) was intentional since one of the primary objectives of FLEXGAN was also to showcase the capabilities of the MESC GaN-Si process for SatCom applications.

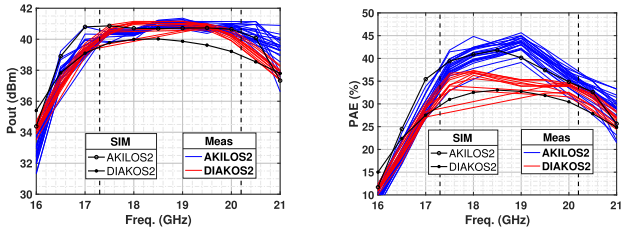
The second one focused on the identification of powerful methods to combine 16 of these elementary MMICs with maximum efficiency, to achieve more than 125-W output power, thus leading to an SSPA that is comparable with TWTAs.

To mitigate the risks associated with an MMIC implementation at this frequency, two different versions of PA were designed. Moreover, to be compliant with space-derating rules and to avoid possible reliability issues, the nominal drain bias voltage was reduced to 9 V, from the maximum nominal value of 15 V, whereas the current density was set to roughly 60 mA/mm, that is, class AB. Such bias point allows keeping the maximum junction temperature of the active devices lower than 160 °C in the worst-case condition, that is, when the base plate of the SSPA is at 65 °C. Both MMICs were based on a three-stage architecture but exploiting different circuit configuration, as shown in Fig. 6. The first MMIC named AKILOS2 exploits a standard corporate configuration [see Fig. 6(a)], whereas the other, named DIAKOS2, uses a balanced configuration with an input–output Lange coupler [see Fig. 6(b)]. The photograph of the realized chips is reported in Fig. 7. The detailed design of both MMICs together with their performance are reported in [22] and [23] for AKILOS2 and DIAKOS2, respectively. The output power and power added efficiency (PAE) measured on-wafer for several samples of both architectures are reported in Fig. 8. Both PAs provide more than 10 W of saturated output power all over the



(a) (b)

Fig. 7. Photograph of the realized MMICs. Chip size of (a) AKILOS2 is 5×4.4 mm^2, whereas for (b) DIAKOS2 is 5×4.5 mm^2.



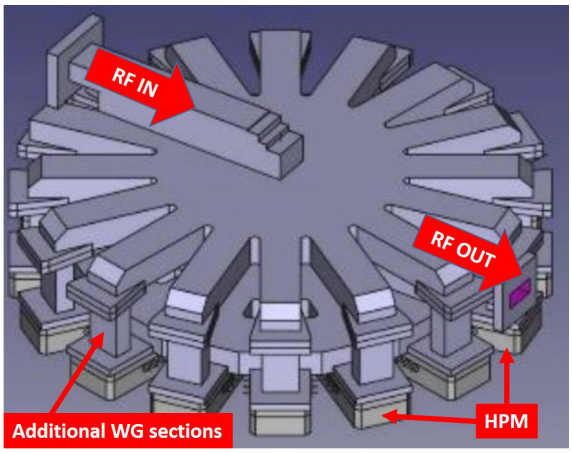
(a) (b)

Fig. 8. Comparison between simulated and on-wafer measured (a) output power and (b) PAE of both chips.

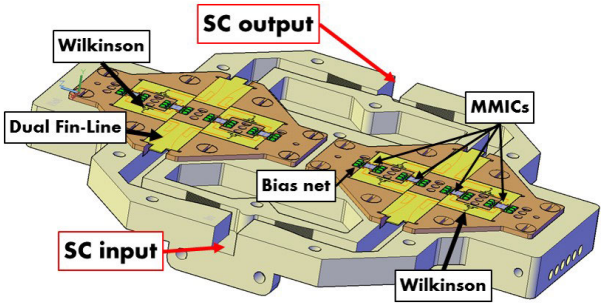
specified bandwidth with a gain larger than 24 dB. In terms of efficiency, AKILOS2 outperforms DIAKOS2 achieving a PAE peak of 45%. Therefore, after a careful evaluation of their performance and the investigation of their stability over time [24], AKILOS2 was selected to implement the elementary module of the SSPA. It is worth mentioning that the performance achieved by these MMICs represents the actual state-of-the-art PAs in this frequency range, at least using European technologies.

For their combination in the last stage of the HPS (see Fig. 4), the research work was focused on the investigation of spatial power combining techniques, since planar ones at this frequency and for this power level are characterized by unacceptable losses [25]. Specifically, two main technologies have been considered: the cavity-based radial combiner (RC) and the single-waveguide longitudinal probe spatial combiner (SC). Their 3-D view is reported in Fig. 9, for comparison. Both solutions have been deeply investigated, also implementing dummy prototypes to experimentally verify their performances in terms of insertion loss and combining efficiency, as well as other key aspects for space applications such as multipaction, size, weight, mechanical, and thermal behaviors. The design description of both structures is reported in [26], whereas Table II summarizes the main outcomes of the comparative study.

In terms of electrical performance, the RC shows better combination efficiency with respect to the SC (89% versus 73%), thanks to the lower insertion losses. This is mainly because, in the RC, the power coming from the 16 parallel modules is sum together in a single step, whereas in the SC, this function is accomplished by cascading three different levels of recombination [26]. On the other hand, thanks to a more compact and integrated structure, the SC outperforms



(a)



(b)

Fig. 9. 3-D view of (a) RC and (b) half SC structures.

TABLE II
COMPARISON BETWEEN RC AND SC

Feature	RC	SPC
Insertion Loss	0.5 dB	1.37 dB
Combining Efficiency	89%	73%
Size (mm^3)	160x122x63	123x146x21
Weight	1060 g	490 g
Graceful degradation	poor	good
Multipaction Free	yes	yes
Thermally Compliance	yes	yes

the RC in terms of size and weight. This is essential because, in the SC, the MMICs are not individually packaged, being the hermeticity achieved by sealing the shell of the structure with a laser. Together with the hermeticity, in a space environment, it is fundamental to guarantee that the adopted structure is multipactor-free and that the junction temperature (T_j) of the GaN MMIC components does not exceed the boundary limit of 160 °C. In this respect, both solutions have been simulated by using Spark3D software for verifying the multipaction compliance, whereas the thermal–mechanical behavior has been evaluated by using dedicated multiphysics tools. With respect to multipaction, a margin higher than 10 dB, when compared to the maximum power expected at the SSPA level (e.g., 51 dBm), has been obtained in both cases, which is sufficient to satisfy the European Cooperation for Space Standardization (ECSS) rules without carrying out dedicated tests. In terms of

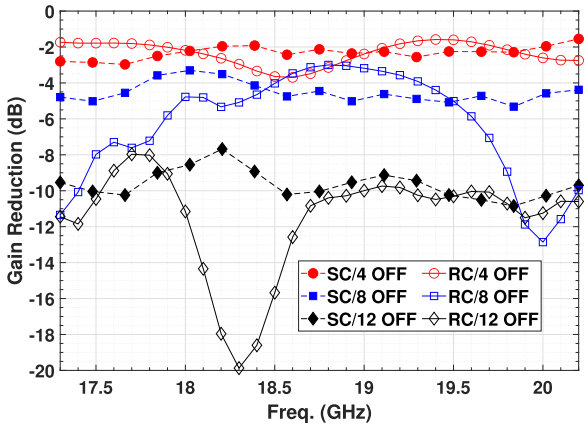


Fig. 10. Simulation of the gain reduction of both RC and SC when a certain number of PAs fails, that is, graceful degradation.

thermal assembly, the RC assures a better distribution of the heat generated by the MMICs, and then a lower T_j of the devices, essentially thanks to its bigger shape with respect to the SC, even if the latter, with the adoption of advanced materials with very high thermal conductivity, also complies with the T_j limit. Finally, the graceful degradation, that is, the variation of the performance of the combining structure when a certain number of MMIC PAs is assumed to fail, has been evaluated. Simulation results have shown that the RC, due to the absence of isolated networks, is more sensible to MMIC failures with respect to SC. Fig. 10 shows the gain of both solutions for a different number of died modules normalized to the reference state, that is, when all PAs are working perfectly. For instance, with four MMICs OFF, the insertion loss of the SC degrades by about 2 dB, whereas, for the same condition, that of the RC degrades up to 4 dB with a larger ripple.

At the end of the comparative study, considering the pros and cons of both solutions, as well as the boundary conditions to be respected at the payload level, the RC realized in WR-42 and made in aluminum was selected to implement the SSPA. Each individual path of such a structure was also experimentally characterized by using a two-port vector network analyzer (VNA). In particular, the measurements of the splitter were carried out by keeping port one of the VNA always connected to its input port, whereas port two was connected to one of the 16 output ports, with the other 15 parallel ports connected to WR-42 50-Ω terminations. Similarly, for the combiner, port two of the VNA was always connected to its output port, whereas port one was connected to one of the 16 input ports, with the other 15 parallel ports terminated with 50-Ω loads. Fig. 11 shows the results of this characterization in terms of magnitude and phase of the S_{21} parameter of each path. Notably, variations within ±0.3 dB and ±5° in terms of magnitude and phase, respectively, have been observed, mainly due to manufacturing tolerances. Clearly, being 1-to-16 and 16-to-1 structures, the average gain is around −12 dB.

To be compatible with the designed radial structure, each MMIC has been individually packaged and equipped with input–output microstrip-to-waveguide hermetic transitions showing negligible insertion loss. Fig. 12 shows the most relevant steps in the assembly of the MMICs, from the designed envelope to the final high-power module (HPM).

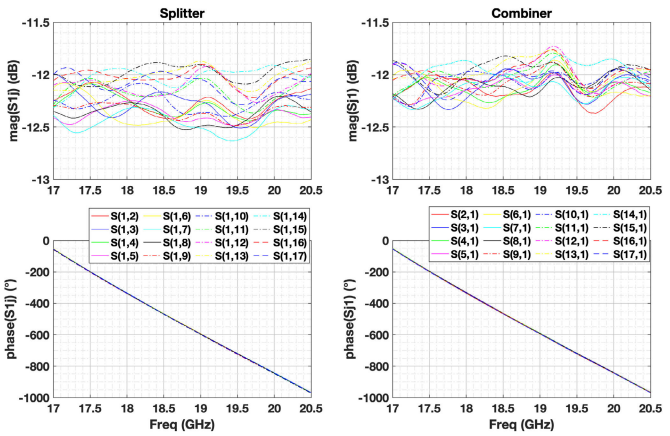


Fig. 11. Magnitude and phase of the measured paths of the input (left) and output (right) section of the RC.

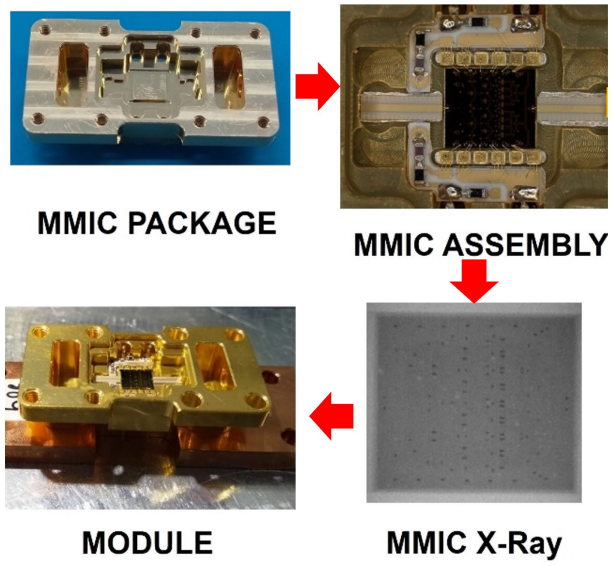


Fig. 12. Assembly of the MMIC in the developed package.

The package has been realized in copper, whereas hermetic feed-throughs have been used to bring the bias. Each HPM has been subject to an X-ray inspection to evaluate the presence of voids underneath the MMIC. Clearly, the higher the number of voids, the worse the thermal dissipation is. In our case, the eutectic process conceived for this assembly led to a very limited number of voids, as also visible in Fig. 12.

The RFT is completed by adding a gain stage between the GCU and the last stage of the HPS, namely the medium-power module (MPM) in Fig. 4. Also, this amplifier is based on AKILOS2 MMIC. The choice has been taken to optimize the cost and to have a driver working in almost linear conditions when the parallelized HPMs are pushed into compression or are subject to a gain reduction process, for instance, due to a temperature increase. The gain of the final stage is about 22 dB, thus the driver should provide a minimum output power of 51–22 = 29 dBm, which is well below the saturated output power of the developed MMIC. All 17 packaged MMICs (16 in the last stage plus the MPM) have been individually tested

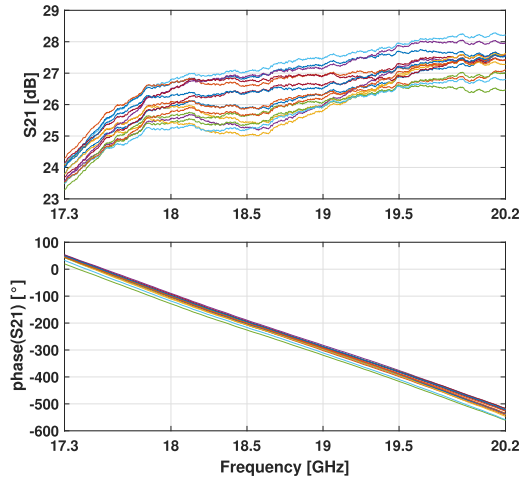
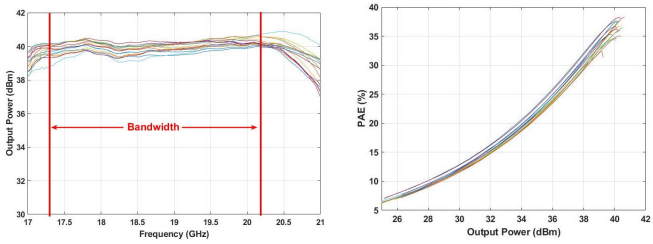


Fig. 13. Small signal gain and phase responses of the 17 HPMs.



(a) (b)

Fig. 14. (a) Measured output power as a function of the frequency and (b) PAE as a function of the output power at a center frequency of all HPMs.

before their integration into the HPS. Fig. 13 shows the linear performance of the assembled HPMs. The uniformity is quite good with an S_{21} variation among samples of about ± 1 dB and $\pm 20°$, in terms of magnitude and phase, respectively. Moreover, to maximize the recombination efficiency in the HPS, the position of each HPM was chosen accounting for their individual phase and amplitude responses, as well as those of each path of the radial splitter/combiner structures reported in Fig. 11. This was done by performing an optimization process in ADS Keysight software, in which the optimized variable was the position of each HPM, and the goal was the minimization of both the phase misalignment and amplitude variation among the 16 paths.

Finally, Fig. 14(a) shows the measured output power in CW of all packaged MMICs as a function of the frequency, whereas Fig. 14(b) reports their PAE as a function of the output power at center frequency. The performance is well in line with those measured on-wafer [20] with the modules achieving an output power larger than 40 dBm all over the bandwidth and a PAE larger than 35%.

C. SSPA Assembly

Once the realization and tests of every single subunit within the SSPA were completed, a structural box to accommodate all the electronic components in the smallest volume and footprint possible was designed. The SSPA envelope was specifically conceived to maximize the heat transfer toward the satellite chassis, also accounting for the forces and mechanical stress

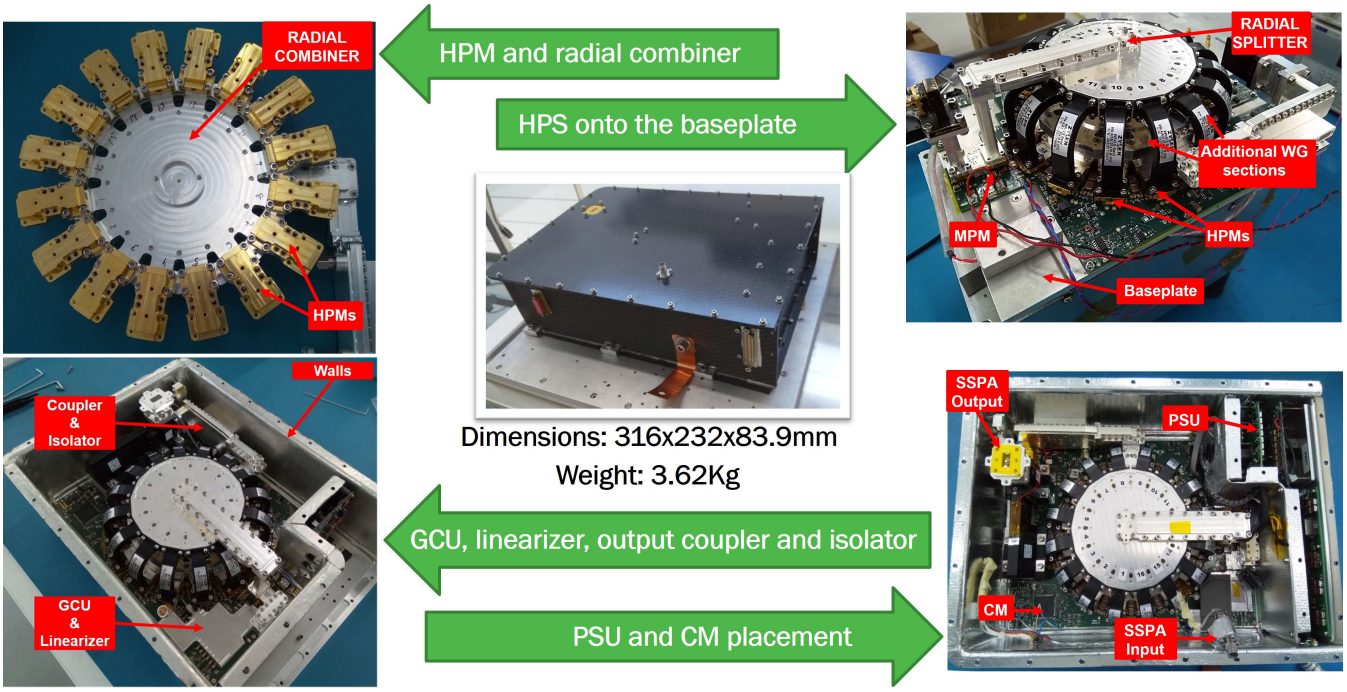


Fig. 15. Photographs of the SSPA during the assembly.

of a launch. Moreover, it was built by using lightweight composite materials, such as carbon fiber-reinforced plastic, to minimize the overall weight. The RFT was completed by adding a waveguide coupler at the output to sample the power and two isolators, one at the input and one at the output, to comply with the return losses requirement and, above all, to protect the SSPA against output load mismatch. Fig. 15 shows some photographs taken during the different phases of the assembly together with their final dimensions and weight.

III. Experimental Results

A detailed and complete test campaign has been conducted to verify the SSPA performance and reliability accounting for space environment requirements. Therefore, the main electrical performance, mechanical, environmental (vacuum and temperature), and EMI/EMC characteristics have been experimentally checked.

A. Small-Signal Characterization

Fig. 16 shows the scattering parameters measured for different attenuation levels, from 0 to 30 dB, and fixing the base plate temperature of the SSPA at $T_{BP} = 25$ °C. The specified gain of 70 dB is achieved with 10 dB of the attenuation set in the GCU. This was properly chosen to ensure a larger dynamic range for compensating thermal/aging variations all over the SSPA lifetime. Such measurements have been carried out without enabling the ALC or FGM operating mode, thus there is no compensation for the gain ripple. Anyway, the latter is within ±1 dB all over the specified bandwidth. The input and output return losses are always better than 20 dB, thanks to the presence of the isolators.

The small-signal parameters have also been measured enabling the power flexibility feature (i.e., setting the drain

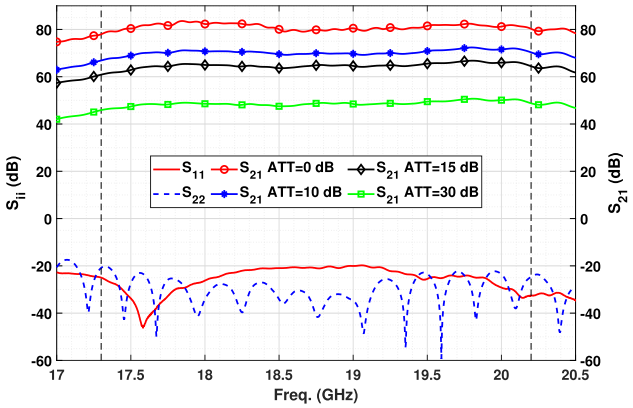


Fig. 16. Scattering parameters of the SSPA at $T_{BP} = 25$ °C setting different attenuation levels.

bias voltage of the HPMs from the nominal value of 9–8 V), and setting the attenuation to 10 dB. Fig. 17 compares the small-signal gain with and without power flexibility. The important aspect is that the shape of the gain does not change, since the average gain reduction of about 2 dB can be easily compensated by setting a different attenuation level in the GCU.

To verify the intrinsic gain stability over temperature (i.e., the SSPA is in an open loop with both ALC and FGM disabled), the scattering parameters were measured by varying the base-plate temperature (T_{BP}) from 25 °C to 65 °C with 20 °C step. Fig. 18 shows the behavior of the small-signal gain as a function of the frequency for such T_{BP}. Notably, the SSPA exhibited a quite stable gain with temperature from 17.3 to 18 GHz, with a negligible variation. From 18 GHz, the gain variation increases with frequency, achieving a peak of 3.5 dB at 20.2 GHz, whereas the average value in the rest

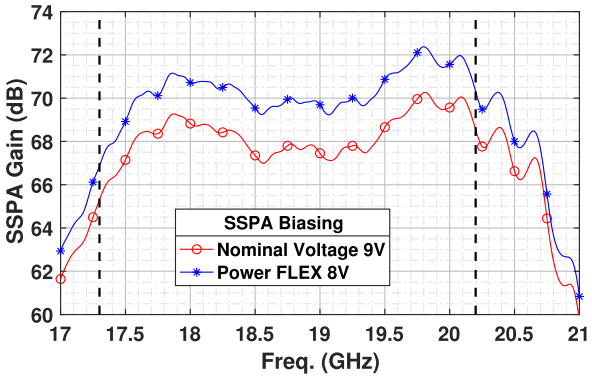


Fig. 17. Small-signal gain of the SSPA with and without the power flexibility enabled at $T_{\mathrm{BP}} = 25$ °C.

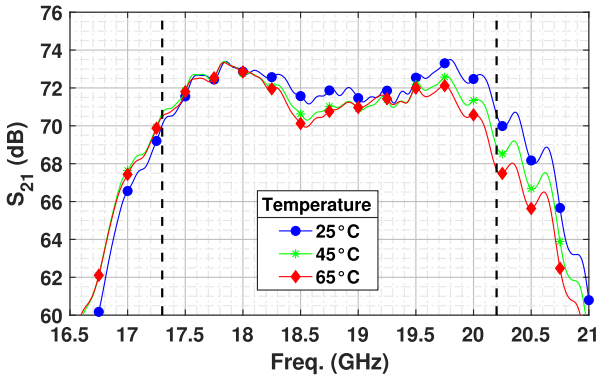


Fig. 18. Small-signal gain of the SSPA for different base-plate temperatures as a function of the frequency.

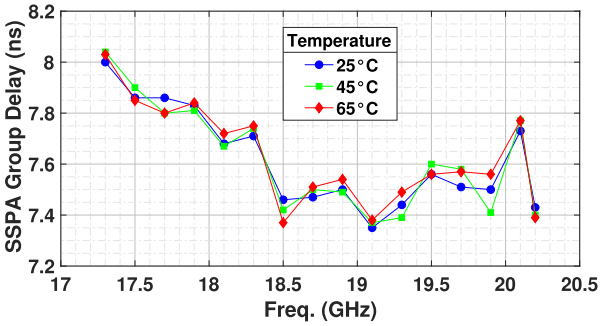


Fig. 19. Group delay of the SSPA at 25 °C, 45 °C, and 65 °C of the base plate temperature.

of the bandwidth is about 1.7 dB. For the same temperature conditions, the measured group delay and noise figure are reported in Figs. 19 and 20, respectively. For these figures of merits, requirements were set to 0.5 ns over any 36-MHz bandwidth and to 10 dB, respectively. Also, in this case, the final SSPA results to be compliant with the specs.

B. Large-Signal Characterization and Power Flexibility

Once completed the tests in linear conditions, the SSPA was subject to an extensive characterization campaign in a nonlinear regime to verify the most challenging requirements in terms of efficiency, linearity, and power levels.

Fig. 21 shows the measured output power and PAE of the overall SSPA when the input power is fixed to −19 dBm

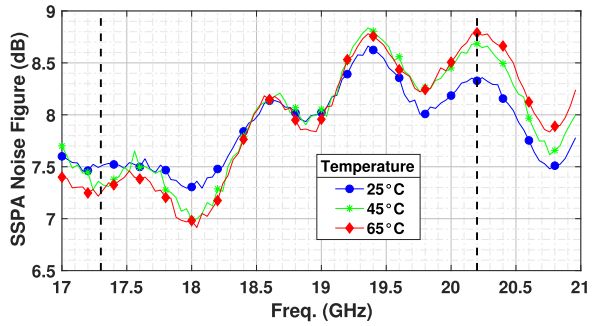


Fig. 20. Noise figure of the SSPA at 25 °C, 45 °C, and 65 °C of the base plate temperature.

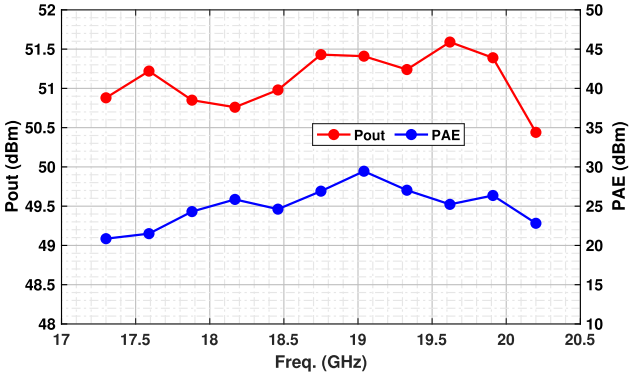


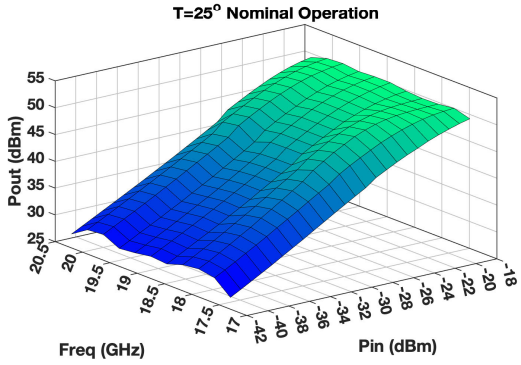
Fig. 21. SSPA output power and PAE at NOP1 and $T_{\mathrm{BP}} = 25$ °C as functions of the frequency for an input power of −19 dBm.

and $T_{\mathrm{BP}} = 25$ °C. The output power is even larger than 51 dBm with a PAE better than 24% over a large portion of the bandwidth. The same features as functions of both the frequency and the input power are shown in Fig. 22, for completeness.

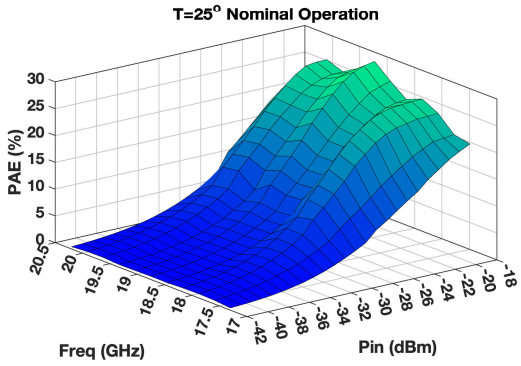
The output power and PAE at NOP1 have also been measured by varying T_{BP} from 25 °C to 65 °C, obtaining the results reported in Fig 23. The behaviors of such features look quite similar over temperatures, with an average reduction of the output power of 0.004 dB/°C only. This demonstrates the very good thermal management of the mechanical box designed, and the capability of the SSPA to efficiently provide an almost constant and high power all over the specified temperature range.

To verify the ALC functionality, the SSPA output power was fixed to NOP3 (50 dBm) at the center frequency, and its input power was swept from −18 to −29 dBm with a 1-dB step. Fig. 24 reports the measured output power as a function of the input power, showing a very stable behavior. Similar trends have been measured also fixing the output power to different thresholds.

As mentioned in Section II-B, the SSPA implements a power flexibility feature. Therefore, the satellite central control can reduce the output power, depending on the actual needs, by sending a telecommand signal. When this feature is exploited, the EPC varies the dc biasing voltage of the HPMs accordingly with the requested power value, thus minimizing the SSPA power consumption with a minimal degradation in terms of linearity. The calibration law between the output



(a)



(b)

Fig. 22. (a) SSPA output power and (b) PAE as functions of the frequency and input power at $T_{BP} = 25$ °C.

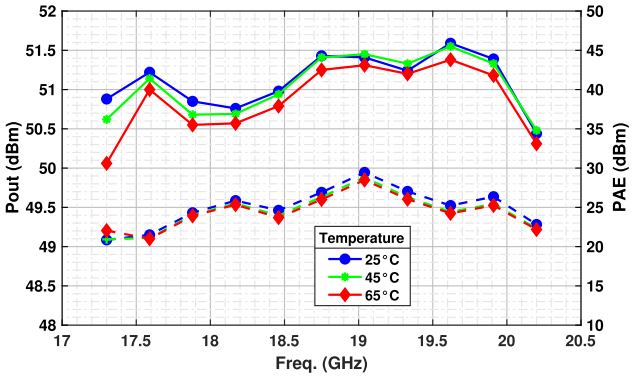


Fig. 23. SSPA output power and PAE at NOP1 as functions of the frequency for different T_{BP} values.

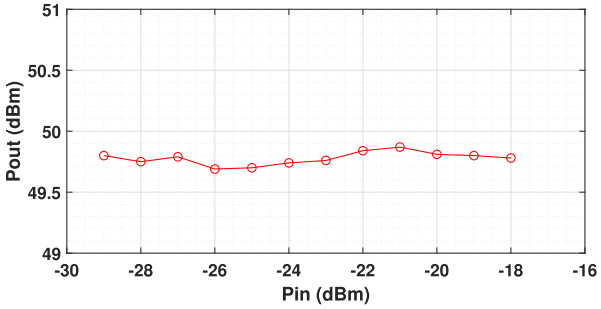


Fig. 24. SSPA output power fixed to 50 dBm by enabling the ALC algorithm versus input power at $T_{BP} = 25$ °C.

power and bias voltage was prederived by measuring the SSPA output power for different drain voltages, from 9 V, which corresponds to the nominal biasing point, to 8 V, which is the minimum level that the PSU can deliver. To appreciate the benefits introduced by such a quite innovative functionality, Table III reports the measured dc power consumption of the SSPA at center frequency for different biasing voltages, once the output power was fixed to a certain value. As can be noted, for NOP3 (50 dBm), the variation of the bias voltage from 9 to 8 V allows for a saving of nearly 100 W (22%) of dc power, whereas for NOP2 (48 dBm), the saving is of around 72 W (21%). Such results highlight the usefulness of the power flexibility feature in terms of power saving, even if its usability has to be confirmed also evaluating the associated linearity. As it will be shown, reducing the biasing voltage causes roughly 2 dB of reduction in terms of NPR for a given output power level.

TABLE III
SSPA DC POWER CONSUMPTION FOR DIFFERENT BIAS VOLTAGES AND OUTPUT POWER LEVELS

Output Power	9 V	8.5 V	8 V
50dBm	444W	363W	346W
49dBm	377W	316W	299W
48dBm	333W	276W	261W
47dBm	289W	245W	232W
46dBm	261W	219W	206W
45dBm	235W	198W	187W
44dBm	211W	179W	165W

The linearity of the SSPA has been evaluated at NOP2 and NOP3 by carrying out NPR measurements adopting a white-noise-like signal (29 001 carriers spaced 100 kHz) having a PAPR of 10 dB with an instantaneous bandwidth of 2.9 GHz (i.e., covering the entire 17.3–20.2-GHz band) and by varying the notch bandwidth from 125 to 250 MHz. Such a characterization was carried out by varying the base-plate temperature and with and without the power flexibility, to correctly address the linearity-efficiency tradeoff. Notably, the NPR is defined and evaluated as the ratio of the output power spectral density (PSD) of the analyzed system with the notch filter presented and measured within the filter band, to the output PSD without the notch filter and measured within the same notch filter bandwidth [27]. Fig. 25 shows one of the captured output spectra at NOP3 (100 W) with a 125-MHz notch filter and the power flexibility OFF at $T_{BP} = 25$ °C. In this condition, the measured NPR is 18.94 dB with a power consumption of 446 W and a corresponding PAE of 22.4%. From such a figure, simply comparing the level of the channel power inside and outside the notch filter bandwidth, the NPR could seem higher with respect to the reported value. However, it is worth highlighting that this is just a graphical result since the NPR has to be evaluated considering the PSD (dBm/Hz) inside and outside the notch filter.

The most relevant results of this peculiar and fundamental characterization are summarized in Tables IV–VII. Notably, when the drain bias voltage of the HPMs is set to 8 V, the maximum output power does not fully comply with the NOP3 level, probably due to the reduced voltage swing available. On the other hand, it is always possible to satisfy the output power at NOP2 with a significant reduction of the dc consumption, while providing almost the same NPR value.

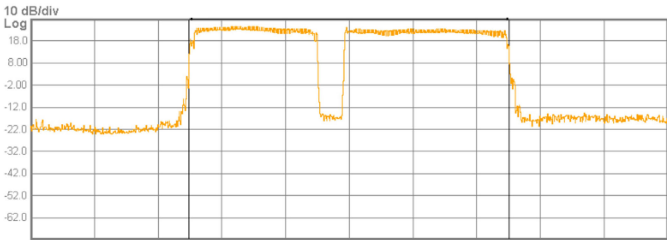


Fig. 25. SSPA output spectrum captured at NOP3 with a 125-MHz notch filter and $T_{BP} = 25$ °C.

TABLE IV
NPR RESULTS FOR THE $T_{BP} = 25$ °C AND 125-MHz NOTCH FILTER

Operation Point	Pout (W)	NPR (dB)	dc Power (W)	PAE (%)	Power Flexibility
NOP2	65	19.7	340	19.1	OFF-9V
NOP3	100	18.9	440	22.7	OFF-9V
NOP2	65	19.6	310	21	ON-8V
NOP3	95.5	18	405	23.6	ON-8V

TABLE V
NPR RESULTS FOR THE $T_{BP} = 25$ °C AND 250-MHz NOTCH FILTER

Operation Point	Pout (W)	NPR (dB)	dc Power (W)	PAE (%)	Power Flexibility
NOP2	65	22.4	335	19.4	OFF-9V
NOP3	100	21.9	436	22.9	OFF-9V
NOP2	65	22.6	300	21.7	ON-8V
NOP3	90	19.5	394	22.6	ON-8V

TABLE VI
NPR RESULTS FOR THE $T_{BP} = 65$ °C AND 125-MHz NOTCH FILTER

Operation Point	Pout (W)	NPR (dB)	dc Power (W)	PAE (%)	Power Flexibility
NOP2	65	22.2	347	18.7	OFF-9V
NOP3	100	19.4	447	22.4	OFF-9V
NOP2	65	21.8	308	21.1	ON-8V
NOP3	92	17.3	394	23.4	ON-8V

TABLE VII
NPR RESULTS FOR THE $T_{BP} = 65$ °C AND 250-MHz NOTCH FILTER

Operation Point	Pout (W)	NPR (dB)	dc Power (W)	PAE (%)	Power Flexibility
NOP2	65	23.5	343	19	OFF-9V
NOP3	100	20.2	452	22.1	OFF-9V
NOP2	65	23.1	308	21.1	ON-8V
NOP3	88	19	383	22.7	ON-8V

C. Thermal Vacuum Test

A thermal vacuum test is a fundamental step for space-borne SSPAs. The aim is to verify whether the component can survive, without loss of integrity and functionality, to thermal and pressure conditions experienced in the space environment. Additionally, it provides a first experimental assessment of the design robustness against those destructive phenomena, such as multipaction and corona breakdowns, that are hard to accurately predict during the development phase. Before reaching the vacuum conditions, a bake-out process of the system has been carried out to minimize the outgassing during the tests. The tests were carried out at the European High-Power Laboratory in Valencia (Spain). Table VIII summarizes the temperature limits adopted for the tests, whereas Table IX lists the adopted criteria.

TABLE VIII
TEMPERATURES FOR THE THERMAL VACUUM TEST

SSPA Condition	Minimum Temp. (°C)	Maximum Temp. (°C)
Non-operating	-40	+85
Start-up	-35	-
Operating	5	65

TABLE IX
THERMAL VACUUM CYCLING TEST PARAMETERS

Parameter	Value	Unit
Vacuum pressure	$\leq 133 \cdot 10^{-5}$	Pa
Dwell Time	2	hours
Temperature rate	2	dT/dt (°C/min)
Stabilization criteria	1	dT/dt (°C/h)
Number of cycles	8	

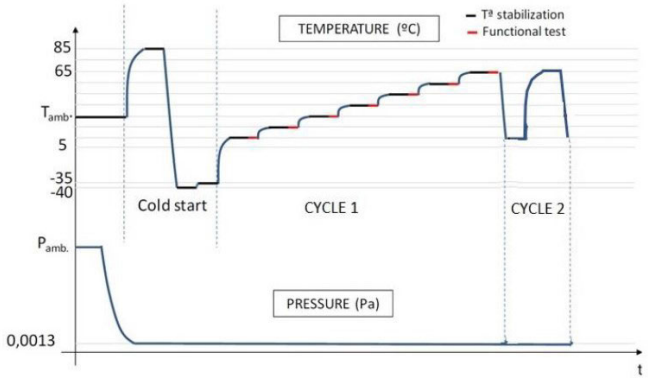


Fig. 26. Thermal vacuum test profile.

Finally, Fig. 26 shows the evolution of the temperature in the chamber during the first thermal cycle together with the time frames allowed to carry out the functional tests, to verify the SSPA integrity. In particular, the functional test consists of a power sweep at the center frequency performed every 10 °C, between +5 °C and 65 °C.

As can be noted from Fig. 27, where the PAE and gain at $T_{BP} = 25$ °C before and after the thermal-vacuum cycles are reported, no significant degradation has been observed. This, once again, confirms the robustness and reliability of the realized SSPA.

D. EMI, EMC, and Mechanical Tests

The SSPA was also subject to both EMI and EMC tests as well as several mechanical stress tests. Before and after each test, the functionality of the SSPA was verified by performing

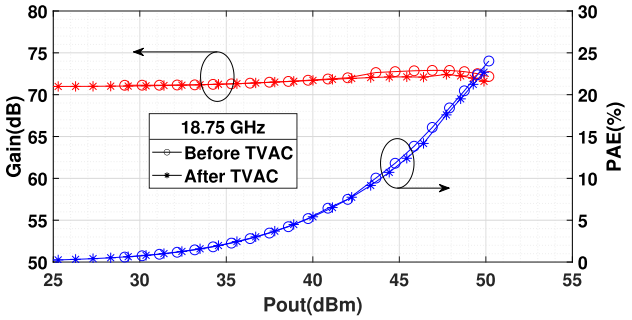


Fig. 27. PAE and gain of the SSPA before and after the thermal-vacuum cycles as functions of the output power at the center frequency.

a power sweep at center frequency. EMI and EMC results were in line with the expectations, whereas mechanical tests have highlighted that the unit has maintained structural integrity, and no failures have been observed.

IV. Conclusion

An SSPA conceived for the Ka-band downlink SatCom applications has been presented and deeply discussed. To the best of the author's knowledge, this is the first space-borne SSPA realized for this peculiar application to achieve a technology readiness level of 5, entirely based on European technologies. The SSPA has been subject to a very extensive and complete measurements campaign, demonstrating state-of-the-art results without evidencing reliability issues. Saturated output power larger than 125 W with a gain and an overall efficiency better than 70 dB and 22%, respectively, have been measured over different base-plate temperatures. The utility of the power flexibility feature was demonstrated, achieving a reduction in the power consumption up to 20%, without significantly worsening the linearity. Indeed, an NPR better than 18 dB was measured when the SSPA outputs an average power up to 100 W, being driven with a white-noise-like signal having a PAPR of 10 dB and an instantaneous bandwidth of 2.9 GHz. Such remarkable results pave the road toward vHTSs fully based on solid-state technology.

References

[1] M. M. Azari et al., "Evolution of non-terrestrial networks from 5G to 6G: A survey," *IEEE Commun. Surveys Tuts.*, vol. 24, no. 4, pp. 2633–2672, 4th Quart., 2022.

[2] M. Luglio, M. Quadrini, C. Roseti, and F. Zampognaro, "Modes and models for satellite integration in 5G networks," *IEEE Commun. Mag.*, vol. 61, no. 4, pp. 50–56, Apr. 2023.

[3] A. Yarali, "The future of wireless communication with 6G," in *From 5G to 6G: Technologies, Architecture, AI, and Security*. Hoboken, NJ, USA: Wiley, 2023, pp. 53–63.

[4] M. Y. Abdelsadek et al., "Future space networks: Toward the next giant leap for humankind," *IEEE Trans. Commun.*, vol. 71, no. 2, pp. 949–1007, Feb. 2023.

[5] S. D'Addio et al., "Technology developments and R&D activities at the European Space Agency for satellite communication payloads based on active antennas and digital processors," in *Proc. IEEE Int. Symp. Phased Array Syst. Technol. (PAST)*, Oct. 2022, pp. 1–6.

[6] M. López, S. B. Damsgaard, I. Rodríguez, and P. Mogensen, "An empirical analysis of multi-connectivity between 5G terrestrial and LEO satellite networks," in *Proc. IEEE Globecom Workshops (GC Wkshps)*, Dec. 2022, pp. 1115–1120.

[7] G. Amendola et al., "Low-Earth orbit user segment in the Ku and Ka-band: An overview of antennas and RF front-end technologies," *IEEE Microw. Mag.*, vol. 24, no. 2, pp. 32–48, Feb. 2023.

[8] V. Valenta and I. Davies, "Power amplification and integration challenges of reconfigurable antennas for space applications," in *Proc. Eur. Microw. Conf. Central Eur. (EuMCE)*, May 2019, pp. 457–460.

[9] N. Ayllon, I. Davies, V. Valenta, and C. Boatella, "Making satellites reliable: The definition and design considerations of space-borne solid-state power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 9, pp. 24–31, Sep. 2016.

[10] R. Emrick, P. Cruz, N. B. Carvalho, S. Gao, R. Quay, and P. Waltereit, "The sky's the limit: Key technology and market trends in satellite communications," *IEEE Microw. Mag.*, vol. 15, no. 2, pp. 65–78, Mar. 2014.

[11] C. Paoloni, D. Gamzina, R. Letizia, Y. Zheng, and N. C. Luhmann, "Millimeter wave traveling wave tubes for the 21st century," *J. Electromagn. Waves Appl.*, vol. 35, no. 5, pp. 567–603, Mar. 2021, doi: 10.1080/09205071.2020.1848643.

[12] W. Q. Lohmeyer, R. J. Aniceto, and K. L. Cahoy, "Communication satellite power amplifiers: Current and future SSPA and TWTA technologies," *Int. J. Satell. Commun. Netw.*, vol. 34, no. 2, pp. 95–113, Mar. 2016. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/sat.1098

[13] X.-D. Jing, S.-C. Zhong, H.-L. Wang, and F. You, "A 150-W spaceborne GaN solid-state power amplifier for BeiDou navigation satellite system," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 58, no. 3, pp. 2383–2393, Jun. 2022.

[14] Z. Wang, Y. Shen, Y. Tian, Y. Tian, and S. Dong, "S-band SSPA for navigation satellite system," in *Proc. Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, Sep. 2020, pp. 1–3.

[15] Y. Fei et al., "Q band solid-state power amplifier for aerospace," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Sep. 2020, pp. 1–3.

[16] R. Giofré et al., "Design realization and tests of a space-borne GaN solid state power amplifier for second generation Galileo navigation system," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 54, no. 5, pp. 2383–2396, Oct. 2018.

[17] R. Giofrè, F. Costanzo, A. Massari, A. Suriani, F. Vitulli, and E. Limiti, "A 20 W GaN-on-Si solid state power amplifier for Q-band space communication systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 413–415.

[18] J. Soric et al., "A 100-W W-band GaN SSPA," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 6, pp. 712–715, Jun. 2022.

[19] N. R. López, J. V. A. Cabal, M. C. Cuiñas, and F. O. Fernndez, "Applicability of technology maturity level evaluation methodologies within small- and medium-sized organizations: Prospects and proposals," *Systems*, vol. 11, no. 8, p. 387, Jul. 2023.

[20] R. Giofrè, L. Cabria, R. Leblanc, M. Lopez, F. Vitobello, and P. Colantonio, "A GaN-based solid state power amplifier for satellite communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2023, pp. 591–594.

[21] *Flexgan*. Accessed: Sep. 10, 2022. [Online]. Available: http://www.h2020-flexgan.eu/

[22] P. Colantonio, M. Lopez, L. Cabria, F. Vitobello, and R. Giofrè, "10 W high efficiency GaN-Si MMIC power amplifier for 17.3–20.2 GHz onboard satellite use," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 775–777.

[23] R. Giofrè, P. Colantonio, F. Costanzo, F. Vitobello, M. Lopez, and L. Cabria, "A 17.3–20.2-GHz GaN-Si MMIC balanced HPA for very high throughput satellites," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 3, pp. 296–299, Mar. 2021.

[24] R. Giofré et al., "On the burn-in of GaN-on-Si MMIC high power amplifiers for SATCOM applications," in *Proc. 17th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2022, pp. 224–227.

[25] D. Passi, A. Leggieri, F. Di Paolo, A. Tafuto, and M. Bartocci, "Spatial power combiner technology," in *Proc. Prog. Electromagn. Res. Symp.*, 2015, pp. 932–938.

[26] R. Giofrè, P. Colantonio, F. Di Paolo, L. Cabria, and M. Lopez, "Power combining techniques for space-borne GaN SSPA in Ka-band," in *Proc. Int. Workshop Integr. Nonlinear Microw. Millim.-Wave Circuits (INMMiC)*, Jul. 2020, pp. 1–3.

[27] R. Figueiredo, N. B. Carvalho, A. Piacibello, and V. Camarchia, "Nonlinear dynamic RF system characterization: Envelope intermodulation distortion profiles—A noise power ratio-based approach," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 9, pp. 4256–4271, Sep. 2021.

Rocco Giofrè (Senior Member, IEEE) received the Ph.D. degree in electronics from the University of Rome Tor Vergata, Rome, Italy, in 2008.

He joined the Electronics Engineering Department, University of Rome Tor Vergata, in 2009, where he is currently an Associate Professor of electronics. He has authored more than 200 peer-reviewed articles, two book chapters, and two contributions for the *Wiley Encyclopedia of Electrical and Electronics Engineering*. His research activities belong to the microwave and millimeter-wave electronics area ranging from active device characterization to the design and test of linear and nonlinear circuits and systems. In this wide research area, he is mainly focused on the development of innovative power amplifier schemes and architectures with high efficiency and linearity for both ground and space communication systems, including their integration in multifunctional chips such as single-chip front ends. He is involved in many research projects funded by international research agencies, such as the European Space Agency (ESA) and the Research Executive Agency (REA), European Commission, Brussels, Belgium.

Dr. Giofrè is a member of the IEEE MTT-S Subcommittee 12 on power amplifiers, an Associate Editor of IEEE ACCESS Journal, and a reviewer for the major journals and conferences of the field. He was a recipient of the 2005 Young Graduated Research Fellowship presented by the GAAS Association and the Best Paper Award at the EuMIC 2007.

Lorena Cabrìa received the Telecommunications Engineering and Ph.D. degrees from the University of Cantabria, Santander, Spain, in 2001 and 2007, respectively.

From 2001 to 2011, she was a Research Associate with the RF and Microwave Group, University of Cantabria. She is currently the Project Manager and the Design Engineer at TTI Norte, Santander. Her main research interests include RF and microwave integrated circuits, intermodulation distortion control on RF and microwave applications, high-efficiency power amplifiers, emerging wireless transmitter architectures, and the development of solid-state power amplifiers for particle accelerators and satellite payloads.

Dr. Cabrìa received the Extraordinary Doctoral Prize for her Ph.D. degree.

Rémy Leblanc received the Engineering degree in microwave electronics and optoelectronics from Paris Telecom-ParisTech "Grande Ecole," Paris, France, in 1983.

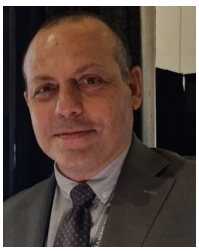
Since graduation, he always worked in the microwave and millimeter-wave fields, dealing with MMIC design, device modeling, reliability, and high-frequency test activities. He is currently the Director of electronic design engineering with Macom European Semiconductor Center, Limeil-Brévannes, France, mainly in charge of MMIC design, foundry support, and on-wafer test activities, related to cutting-edge high-frequency GaN, GaAs PHEMT, and GaAs MHEMT semiconductor processes. He has authored or coauthored more than 30 articles in the field of design or modeling of III–V devices, including MESFET, pseudomorphic and metamorphic HEMTs, and mixed-signal and GaN processes. This covers modeling activities, radio-altimeters, traveling-wave amplifiers, low-noise amplifiers, power amplifiers, optical fiber interface circuits, and multifunction chips, such as beamforming core chips, receivers, or single-chip front ends.

Mariano López received the master's degree in telecommunications engineering from the University of Cantabria, Santander, Spain, in 1997.

He was an RF Engineer with the Communications Department, University of Cantabria. Since 2000, he has been with TTI Norte, Santander, where he is currently a Senior RF Engineer. He has also been the Manager of several research and development and commercial projects in the RF domain, devoted to developing customized equipment such as RF transceivers, SSPAs, and low-noise amplifiers based on customer requirements at different frequency bands from L to Ka.

Fabio Vitobello received the master's degree (cum laude) in microelectronics engineering from the University of Padova, Padua, Italy, and the double master's degree in power electronics engineering from Illinois Institute of Technology (IIT), Chicago, IL, USA, in 2007.

He was a Researcher on GaN technologies at IIT until 2007. In 2008, he joined the Components Section, European Space Agency (ESA), The Nederland, where he worked for six years following research and development activities aiming at developing a European GaN process suitable for space mission insertion. Afterward, he joined Infineon Technologies, Villach, Austria, where he was a Quality Manager of the RF GaN process. Since 2015, he has been with the European Commission, Brussels, Belgium, first as a Space Program Officer managing and implementing Space EEE projects funded by the EU, in particular, managing research activities supporting the development and qualification of GaN technology for space applications. Then, since 2022, he has also been a Space Policy Officer at DG-DEFIS responsible for defining EU space policy and research and development programs in the area of space critical technologies for EU nondependence.



Paolo Colantonio (Senior Member, IEEE) received the Laurea degree in electronics engineering and the Ph.D. degree in microelectronics and telecommunications from the University of Rome Tor Vergata, Rome, Italy, in 1994 and 2000, respectively.

He is currently a Full Professor of microwave electronics at the University of Rome Tor Vergata. He has authored or coauthored more than 300 scientific articles. He has also authored the book titled *High Efficiency RF and Microwave Solid State Power Amplifiers* (Wiley, 2009), three book chapters, and four contributions to *Wiley Encyclopedia on Microwave Electronics* and holds one international patent. His research activities are mainly focused on the field of micro-wave and millimeter-wave electronics, and, in particular, on the design criteria for nonlinear microwave subsystems and high-efficiency power amplifiers.

Dr. Colantonio has been the Chair for EuMIC 2022 and is currently an Associate Editor of the IEEE MICROWAVE AND WIRELESS LETTERS.