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Performance evaluation of PI controlled series stacked power delivery architectures for high-efficiency data centers

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Bus topology

Abstract Series-stacked architectures have been successfully deployed for data center applications at substantially higher efficiencies than conventional power delivery architectures. In the series-stacked architectures, servers are series-connected electrically to reduce the high step-down conversion stage of voltage utilized in the conventional architectures. Differential power processing converters are, therefore, used to regulate the servers' voltages and compensate for the unpredicted mismatch between servers' currents. The main contribution of this paper comprises novel control approaches based on PI controllers purposeful for the two architectures that have reported the highest reliability and efficiency in differential power processing namely: server-to-bus and server-to-virtual bus. Both systems employ a dual active bridge (DAB) converter to accommodate the fluctuating loads of each server. Unlike hysteresis current/voltage control commonly employed in the available literature, the proposed control approaches offer less complexity, lower harmonics, and higher immunity towards the noise, thus no need for high-quality sensors to successfully achieve voltage balance and/or optimal string current flow. Moreover, a comparative study has been structured between the investigated series-stacked architectures under the proposed PI control approaches showing the merits and the demerits of each architecture. The proposed controllers have been validated based on simulations and experimentally.

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1. Introduction

With the rapid development of data and the prevalence of online services as cloud computing, streaming, and searching,

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the presence of a large number of modern data centers all over the world is now justified. Digitization has penetrated several aspects and sectors, and most importantly the governmental and commercial aspects, leading to the exponential increase of data centers across the globe. Therefore, the deployment of such systems requires adequate software data processing and optimized hardware to reduce losses in the data centers. Data centers consume energy all over the world between 1.1% and 1.5% of the global load [1]. Specifically, it reaches 1.8% of the total energy consumption in the USA and 1.5% for China [1,2]. The rapid growth of internet-based services promotes data centers to be an important energy consumer for national electricity grids. Thus, energy-efficient data centers are mandatory for the Information and Communication Technology (ICT) industry. The most energy-consuming parts of data centers are the servers due to embedded information processing and data storage functionality [1].

Conventionally, to distribute low DC voltage from the AC grid to the servers, the AC to DC power delivery of data centers can be achieved by one of the two following methods:

- The AC voltage is rectified to high DC voltage V_{Bus} (380 V–400 V), then cascaded DC-DC power electronics converters deliver a lower DC voltage of 12 V or 48 V to each server, as shown in Fig. 1(a).
- The AC voltage can be stepped down via a specially-designed transformer or cascaded transformers and delivered to the server racks. This is followed by parallel-connected rectifiers at each server, as shown in Fig. 1(b) [3–5].

These conventional power delivery architectures have limited system-level power conversion efficiency, which ranges from 51.64% to 72.7% and mostly depends on the power converters' efficiency[6]. Contingent on the correlation between the delivered power to servers and the processed power by the conversion stage(s), the losses of the power conversion increase as the delivered power to server and the number of servers increase. Therefore, increasing the efficiency of the voltage conversion is paramount for enhancing the overall system efficiency. Subsequently, establishing an efficient power delivery system for data centers is currently gaining more attention. The rationale behind this is the fact that the inefficient power converters not only increase the electricity demand for powering the servers but also increase the cooling load overheads as well as the cost of designing more bulky heat sinks for these converters. The major challenges that face data center operators are the rising electricity bills, growing carbon footprints, and unexpected power outages. An effective approach to tackle such problems is to investigate the implementation of efficient power supplies that offers the rack voltage levels required to power servers. Recently, the differential power processing (DPP) concept proved to potentially offer a smaller number of cascaded stepping down stages by connecting the servers in series and introducing a DPP converter to supply or withdraw current mismatch in the series-connected servers, as depicted in Fig. 2. DPP system can replace the conventional two-stage power electronics converter with an efficiently designed converter [1–4]. Differential power processing is a power distribution concept that enables decoupled load regulation by processing only the small portion of mismatched power between loads in case of heterogenous loading of series-connected voltage domains.

In DPP systems, loads are all supplied by a relatively bulky input voltage source, where voltage is divided across these loads and the total current drawn from this source decreases. Assuming that voltage domains are controlled, the total processed power becomes a function of current. Once the processed power by each converter is substantially reduced, the overall system efficiency is enhanced. Consequently, the series stacked DPP techniques offer a multitude of merits that include system scalability, smaller voltage step-down ratios, modularity, redundancy, lower cost, and size of the power delivery system. In [7], series-connected DPP concept is deployed for various applications, simulation and experimentation shows a 7–8% reduction in input power and a 6–7% increase in the conversion efficiency, compared to the cascaded conventional systems. A comparative study [8] is conducted between series-stacked power delivery architecture with a conventional best-in-class power delivery unit. Experimental results showed up to 20-times reduction in power conversion losses for DPP architecture compared to commercial counterparts for various loads, such as web traffic and computational loads.

The concept of differential power processing has previously been implemented in several applications that include photovoltaics [9–16], battery chargers [17,18], and computing loads [7,19]. Such applications are analogous to the series-stacked

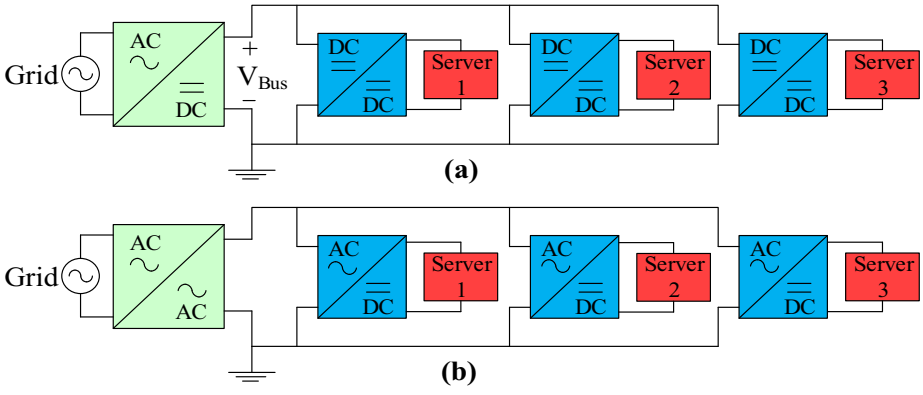


Fig. 1 Conventional power delivery system for data centers such that in (a) AC voltage is rectified, then cascaded DC-DC converters are employed, and in (b) AC voltage is stepped down using special transformer after which rectifiers are connected.

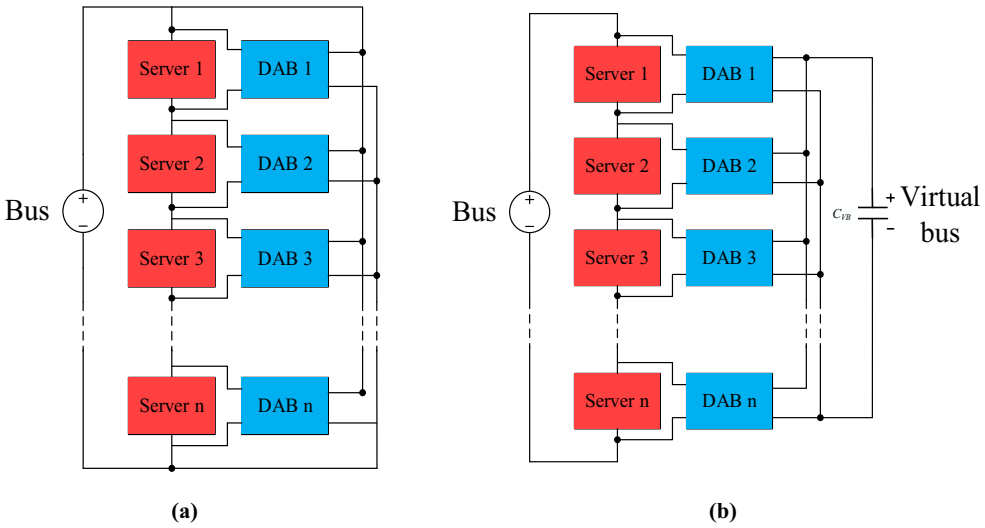


Fig. 2 Series stacked power delivery system for data centers. (a) Server-to-bus-architecture. (b) Server-to-virtual bus.

power delivery architecture for data centers [1]. The analogy is essentially due to the nature of operation in which the building block of a series-connected system undergoes a power mismatch due to considerable fluctuation in the current. In the case of data centers, such mismatch occurs due to the uneven loading of servers according to different computational loads of each sever. DPP systems of series-stacked servers can be classified according to their architecture into three main sections: server-to-server, server-to-bus, and server-to-virtual bus. In [1,8], the server-to-bus and the server-to-virtual-bus architecture are proposed as the series-stacked DPP architecture, employing the Dual Active Bridge (DAB) converter as the DPP unit, which is depicted in Fig. 2. A bidirectional hysteresis control is employed to regulate the servers' voltages and the virtual bus voltage. Several setbacks arise from using hysteresis controllers to regulate DC values, such as a low immunity to noise and the need for high-quality sensors especially when operation requires high-frequency switching.

Although the PI controller is widely studied in a multitude of applications, it has not been implemented in DPP of servers. Based on the available literature, PI controllers have been used in applications employing DPP such as PV-based generators using different converter types, namely: flyback converter [20] and bidirectional buck-boost converter [21], in which the control algorithm is entirely different from the approaches presented in this work. For DPP implementation in data centers, the hysteresis controller [22,23] has been the subject of almost all DPP studies on data center applications. Therefore, the novel PI-control approach, introduced in this work, can be considered more advantageous than that of hysteresis control [24–26]. The presented work in [27–29] shows the potential to attain high-efficiency and reliable DPP operation using the proposed PI-control approach.

Therefore, the proposed work in this paper provides two main points:

- To the best of the authors' knowledge, this work represents the first attempt to employ a novel and simple PI control approach. It performs voltage control over the Input Series Output Parallel (ISOP)-connected DPPs in the server-to-virtual bus architecture. It also accomplishes a unique string current control besides voltage control over the DPPs in the server-to-bus architecture. The proposed PI-control offers less complexity, lower harmonics, lowers filtering requirements than that of hysteresis control and higher immunity towards the noise, thus no need for high-quality sensors. The novelty of the employed control approaches involves the implementation of robust, fixed switching frequency and well-tuned PI controller in the successful performance of differential power processing in the data centers in general.
- Simulation-based comparative study between server-to-bus and server-to-virtual bus architectures, which proved to have the highest reliability for differential power processing

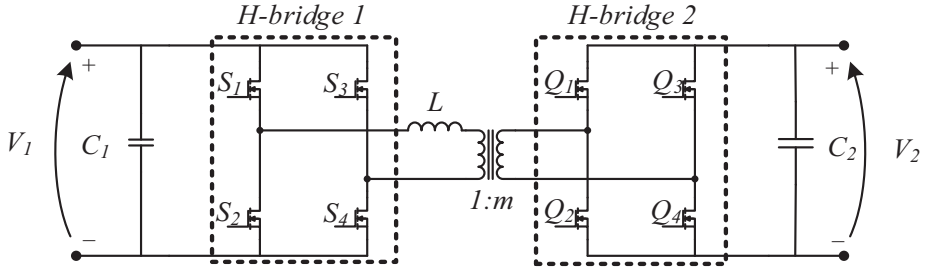


Fig. 3 Schematic of DAB converter.

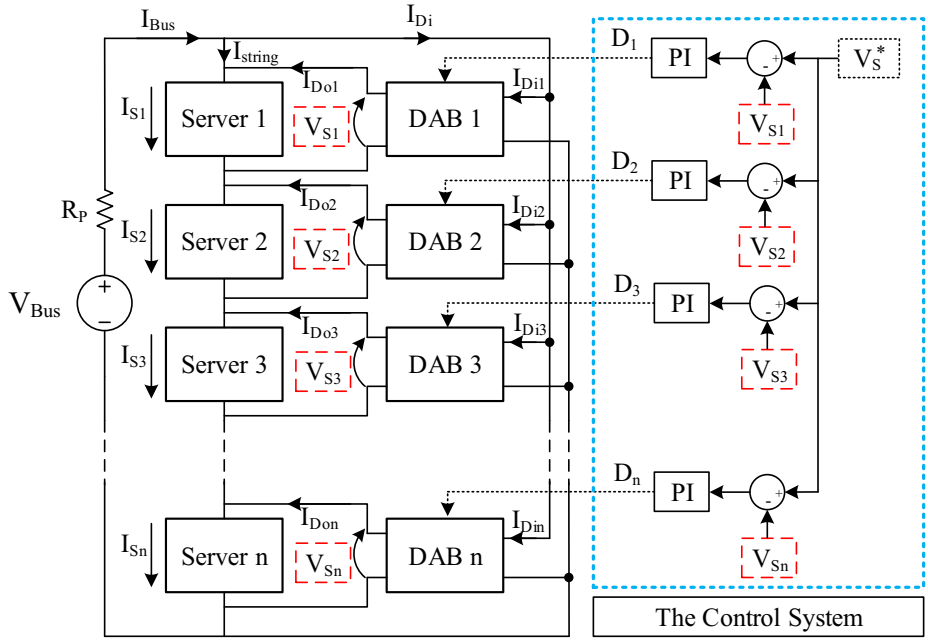


Fig. 4 Server-to-bus architecture (PI voltage control approach).

applications in general. Furthermore, an experimental investigation is conducted to practically validate the simulation results and offer a detailed account of comparison based on the same operating conditions and the same converter design in both architectures.

This paper is organized as follows: Section 2 presents background on the differential power processing architecture focused on server-to-virtual bus and server-to-bus architectures, Section 3 discusses the mathematical models and the employed control algorithms. Moreover, Section 4 discusses the system parameters design, Section 5 shows the simulation and experimental results and results of the proposed control approaches using simulation tools as well as experimental protocol, Section 6 concludes the paper.

2. Background

In this section, the Dual Active Bridge (DAB) converter, which is utilized in the discussed DPP systems, is presented. Besides, a brief review of the server-to-bus and server-to-virtual-bus DPP architectures is demonstrated, as they are the main scope of this work.

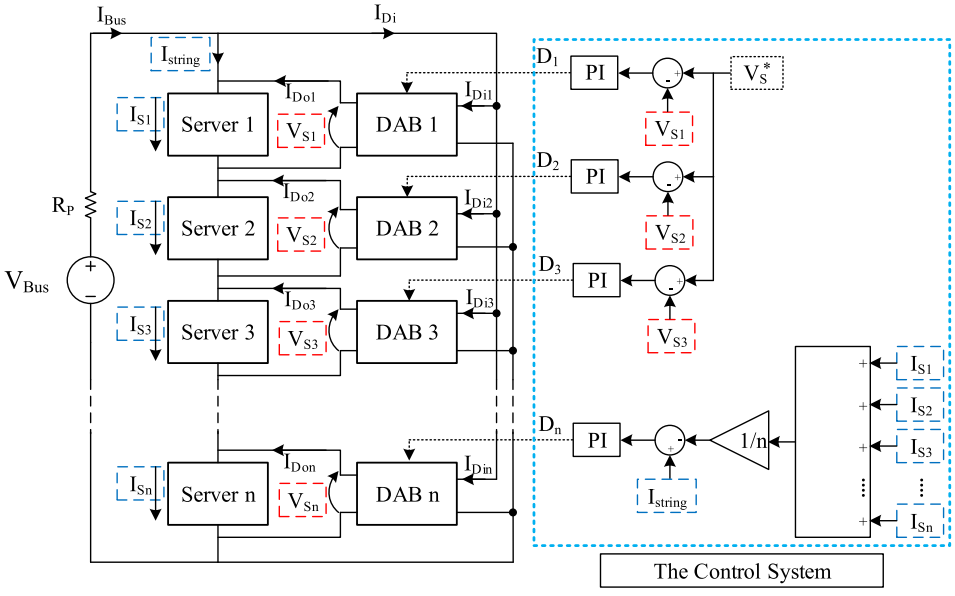


Fig. 5 Server-to-bus architecture (PI optimal string current control approach).

The DAB converter, shown in Fig. 3, is an isolated bidirectional DC-DC converter that offers several merits including simple structure, high power density, soft switching operation, bidirectional power flow capability, and easy implementation of its Phase Shift Modulation (PSM) control. Generally, DAB consists of two H-bridge converters, two DC link capacitors, and a High-Frequency Transformer (HFT) with a turns ratio of (m), and leakage inductance (L), which is considered the main energy transfer element. This HF transformer offers galvanic isolation, and voltage transformation. Single phase shift (SPS) control is applied to the DAB converter, which is considered most attractive due to several advantages, such as fast response, high dynamics. SPS has very simple control, which depends on one phase shift between the square-wave voltages of the primary and secondary sides of the HF transformer that is called an outer phase shift (D) [30].

2.1. Server-to-bus architecture

The general idea in this architecture is that each server has a designated DPP converter connected across the server, which steps down the bus voltage to the desired server operating voltage, as depicted in Fig. 2(a).

In [1], the first experimental protocol that serves as a proof of concept for server-to-bus DPP architecture for server power delivery is presented. It provides a detailed mathematical analysis that illustrates how the server-to-bus architecture surpasses its counterparts in terms of its ability to achieve minimum total processed power. This leads to the highest possible theoretical efficiency in power delivery and the highest reliability. To control the power mismatch between series-connected serves, two hysteresis-based control methodologies are implemented: voltage control methodology and optimal string current control methodology. The latter proved to be more efficient in different schemes of operation. On one hand, voltage control methodology is favorable in the case of well-balanced servers that run at the same computational load. On the other hand, the optimum string current control methodology prevails when the server loads are unbalanced, which leads to a case where the string current fluctuates and may not settle at the dictated current value, thus higher total processed power.

2.2. Server-to-virtual-bus architecture

In this architecture, the DPP converter is differentially connected between a server and a virtual bus as depicted in Fig. 2(b). In [5,8], detailed mathematical analysis to derive an expression for processed power in server-to-virtual bus architecture for power delivery to series-stacked loads is discussed. Two case studies are presented, the first assuming Gaussian distribution of computational loads across the servers, while the second investigated the hot-swapping operation. It has been depicted that regulating servers' voltages and virtual bus voltage in the server-to-virtual-bus architecture, is the key objective to process only the power mismatch between servers using DPP converters, which successfully reduces the power conversion loss. For the control technique presented in [8], to achieve the previous key objective, the bidirectional hysteresis control is utilized, in which each DPP converter keeps both its input (i.e., virtual bus) and output (i.e., server) voltage within a predefined hysteresis band by injecting or rejecting current to its server or the virtual bus. When voltage values are below both hysteresis bands, DPP converters are turned OFF to maximize the power delivery efficiency. However, in addition to the complexity of the control, increasing the switching frequency of the system makes the hysteresis control less immune to the increased noise, and high-quality sensing devices should be used.

The useful merit of such architecture is that a virtual bus is considered a free design parameter that can be set as the server nominal voltage, which further eliminates the voltage stepping stage that is required in server-to-bus architecture. The input and output terminals of the DPP converter, in this case, are identical, which makes the whole system easily scalable without the need to redesign the DPP converter [31].

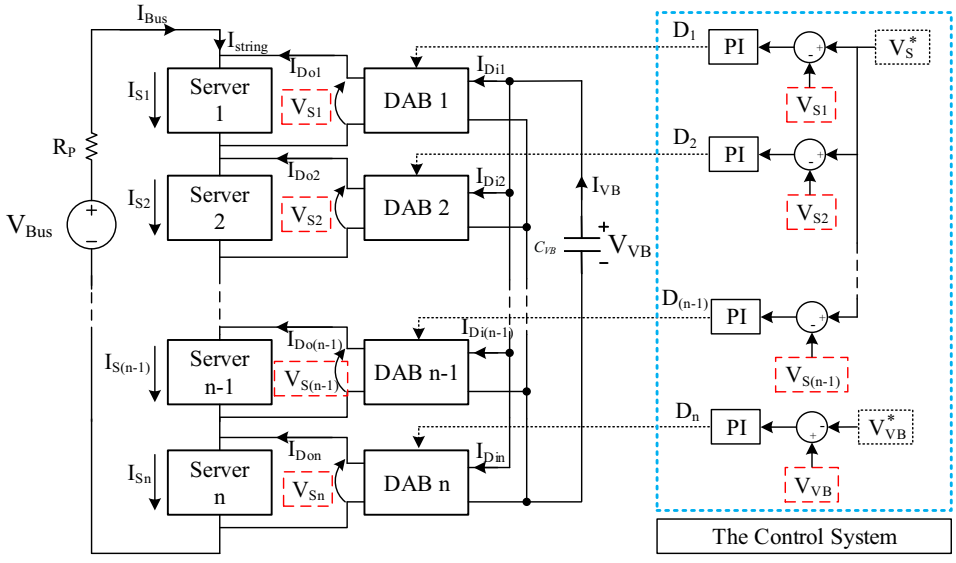


Fig. 6 Server-to-virtual-bus architecture (PI independent voltage control approach).

3. Mathematical modelling and control algorithm of the proposed control approches

In this section, detailed mathematical analyses are derived and discussed for how the differential power is processed in the proposed control approaches of both server-to-bus and server-to-virtual-bus architectures.

3.1. Server-to-bus architecture

In the server to bus architecture, shown in Fig. 2, the DPP converters used in this architecture are the DAB converters, which are to be one side parallelized and connected to the DC bus, while the other side is connected to the servers.

In the series-stacked data center architectures, the DAB converters are controlled in a manner to compensate for the mismatch between servers loading. Therefore, two control approaches are employed in server-to-bus architecture control. The first control approach is denoted as a PI voltage control approach and shown in Fig. 4, which focuses only on regulating the voltage of the series-connected servers with no use of current controllers. While the second control approach shown in Fig. 5 is denoted as PI optimal string current control approach. In this control approach, not only, servers' voltages are regulated, but also the string current is measured and controlled using a PI controller. Therefore, the control of string current can be employed to minimize the total power processed by the DAB converters. The two proposed control approaches are discussed in the subsequent sections with more details.

3.1.1. PI voltage control approach

The PI voltage control approach only requires voltage sensing to execute the control tasks. The sequence of operation starts by measuring the server voltage, which is then subtracted from the reference value V_s^*, obtained from (1), to derive the required DAB phase shift ratio using a PI controller, as shown in Fig. 4. This control approach lacks the capability of string current optimization to achieve minimum processed power in the DAB converters.

$$V_s^* = V_{Bus}/n \tag{1}$$

where V_{Bus} is the bus voltage, n is the number of series-connected servers. Then, the PI controllers are used to compensate for the error between the measured and the reference values of the server voltages, which generates the required phase shift ratio D_k for each DAB converter, as shown in Fig. 4.

All control approaches discussed in this context deal with the average values of current and voltage measurements. The rationale for such a claim is that the instantaneous values of the currents and voltages may fluctuate due to the switching actions of the converters or due to the fast-changing nature of the servers' loading. These ripples are small compared to the average value of voltages and currents; thus they can be neglected.

The parallel-side of the DAB converters is connected to the bus, which is considered the main power supply of the system and the source-side of the DAB, while the series-side is connected to the servers, which is considered the load-side of the DAB. For this particular architecture, the DAB converter includes HFT whose turns ratio must be equal to the number of the series-connected servers ($m = n$). The power flow of each DAB converter depends on the difference between the servers' currents. The power flow in the case of the DAB connected to the highest server current is from the source side to the load side, while the power flow in the case of the DAB connected to the lowest current server, is from the load side to the source side. The power flow of the other DABs depends on the current value of their connected servers. If a given server current is closer to the lowest server current in the stack, then its corresponding DAB current should have a lower magnitude and similar direction to that of its designated DAB current. Therefore, the current of each DAB is determined according to its power flow magnitude and direction. In this context, the string current is the average value of the servers' currents, which achieves the lowest DAB currents (processed currents). However, the aforementioned argument is solely valid if the total voltage drop across the series connection loop of the servers is completely neglected. However, if a slight voltage drop is considered across the series connection loop, which can practically exist due to the wiring or the supply internal resistance and is represented by the resistance (R_p) as depicted in Fig. 4, the string current is not the average value of the servers' currents. Consequently, the DAB currents are not minimized unless a current control algorithm is adopted. A simple voltage control approach lacks the advantage of optimizing processed power because the string current is not the optimum value and consequently DAB currents (processed currents) are not minimized. Hence, there are infinite combinations between DAB

Table 1 Simulation/experimental parameters.

Parameter	Value
Input voltage	36 V
No. of servers	3
Transformer turns ratio	3:1
Transformer leakage inductance (referred to 12 V side)	30 μH
Transformer magnetizing inductance (referred to 12 V side)	128 μH
Transformer core losses (R_c) (referred to 12 V side)	25 Ω
On-state resistance of the switching devices (R_{on})	0.27 Ω
Switching frequency	10 kHz
Capacitance at each server-side	1000 μF
Virtual bus capacitance	6600 μF

Table 2 Server loading intervals.

Time Interval	Server 1	Server 2	Server 3
0.1–0.2 s	2 A	3 A	4 A
0.2–0.4 s	4 A	2 A	3 A
0.4–0.6 s	3 A	4 A	2 A
0.6–0.8 s	4 A	2 A	4 A

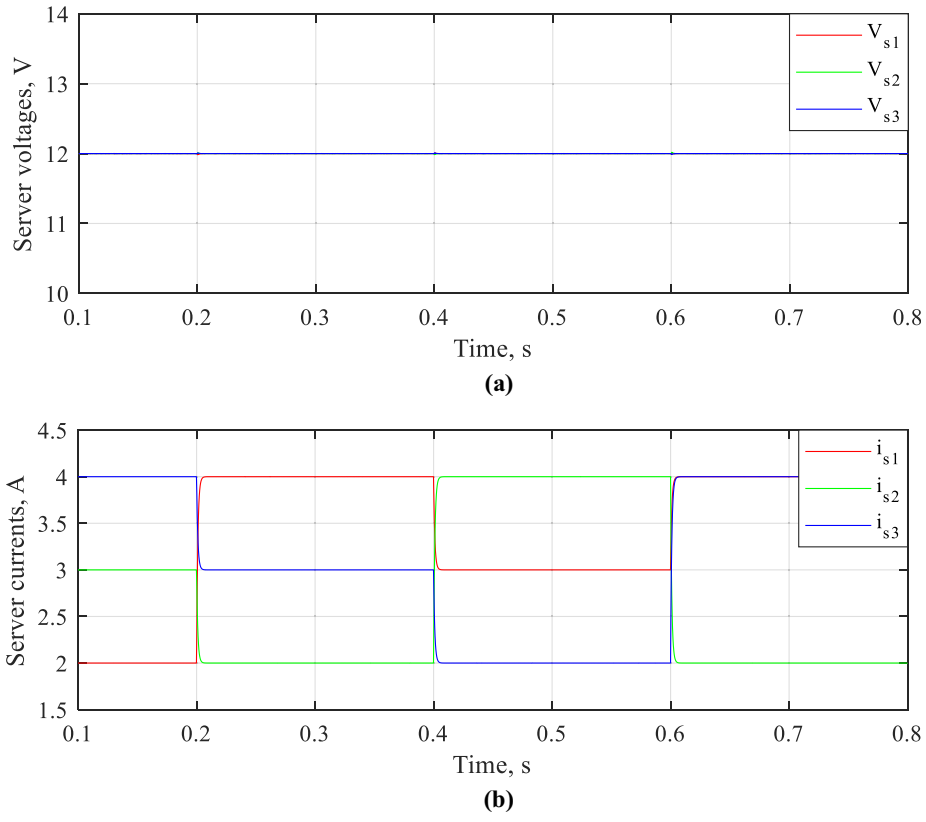


Fig. 7 Server-to-bus architecture (PI voltage control approach) simulation results. (a) Servers' voltages. (b) Servers' currents.

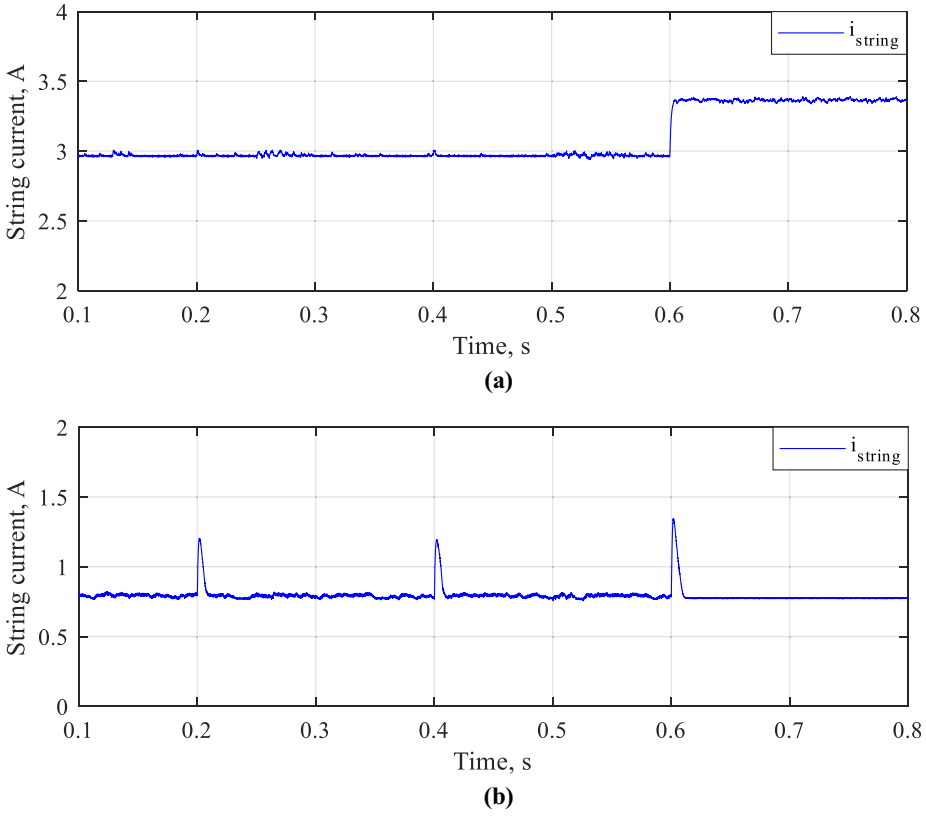


Fig. 8 Server-to-bus architecture (PI voltage control approach) string current. (a) Ideal case. (b) Considering hardware deficiencies.

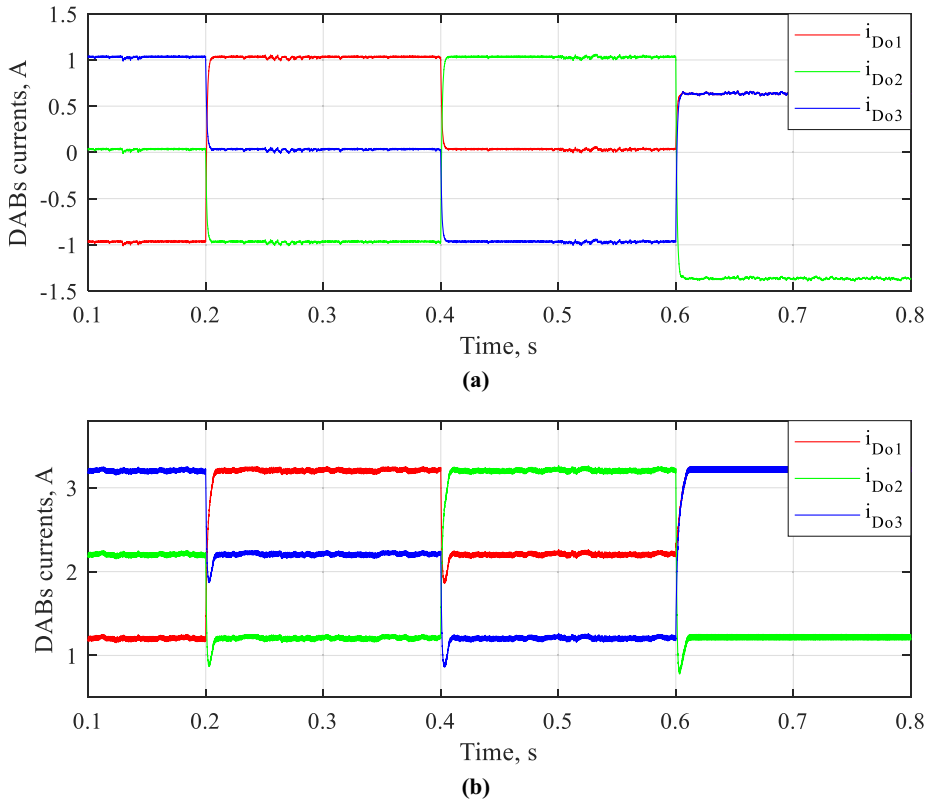


Fig. 9 Server-to-bus architecture (PI voltage control approach) DAB currents. (a) Ideal case. (b) Unideal case.

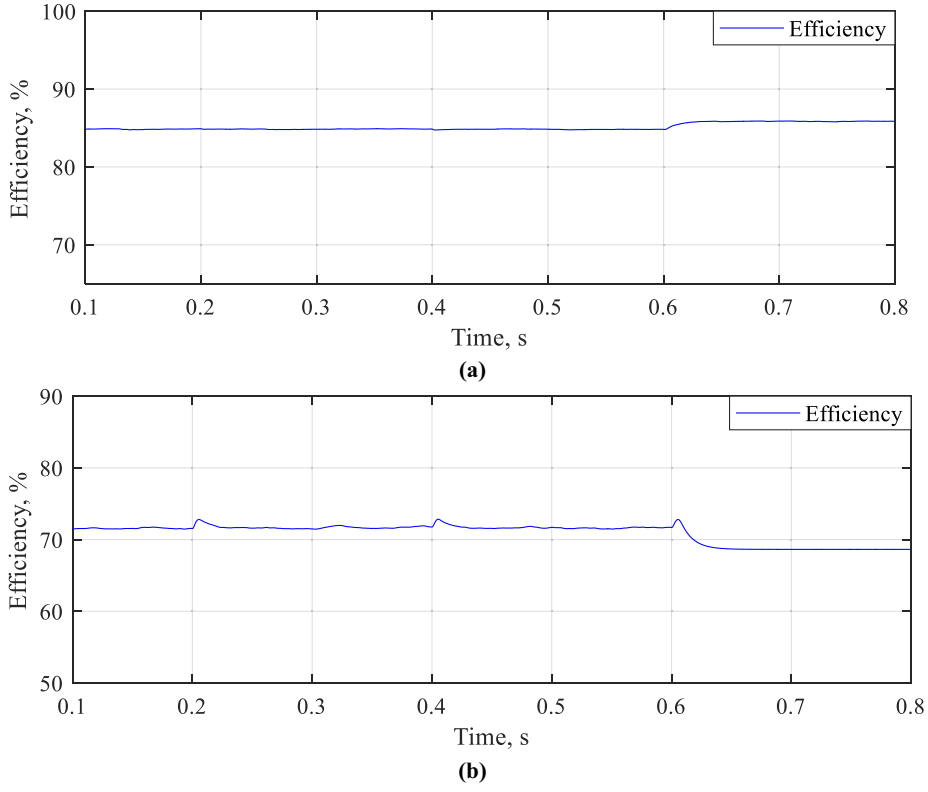


Fig. 10 Server-to-bus architecture (PI voltage control approach) efficiency. (a) Ideal case. (b) Unideal case.

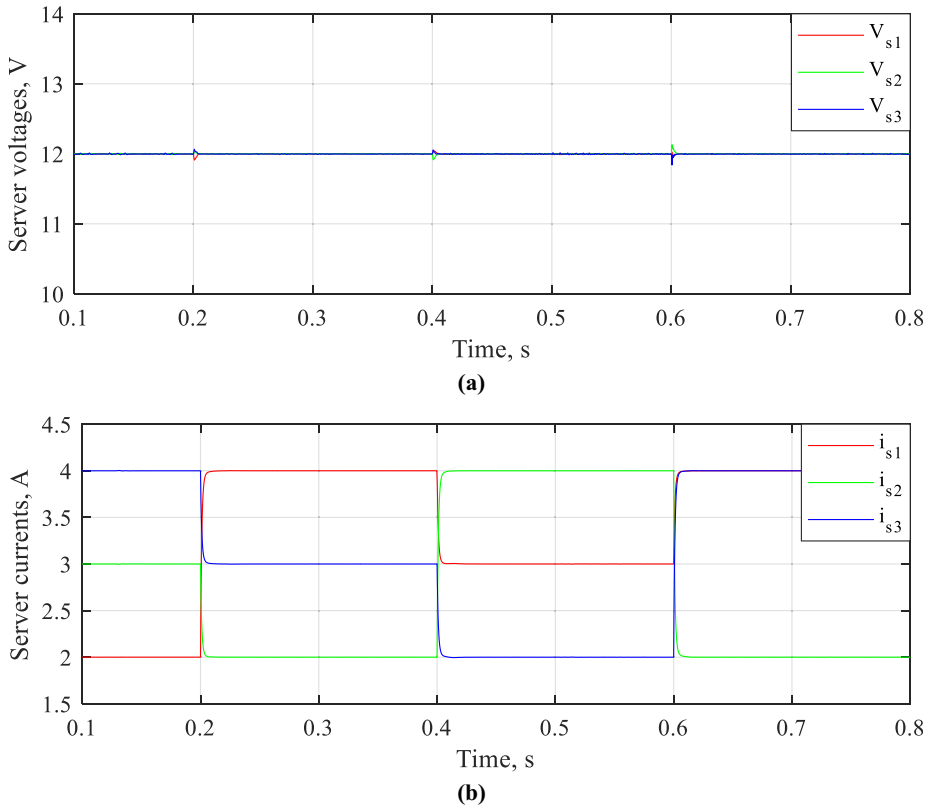


Fig. 11 Server-to-bus architecture (PI optimal string current approach) simulation results. (a) Servers' voltages. (b) Servers' currents.

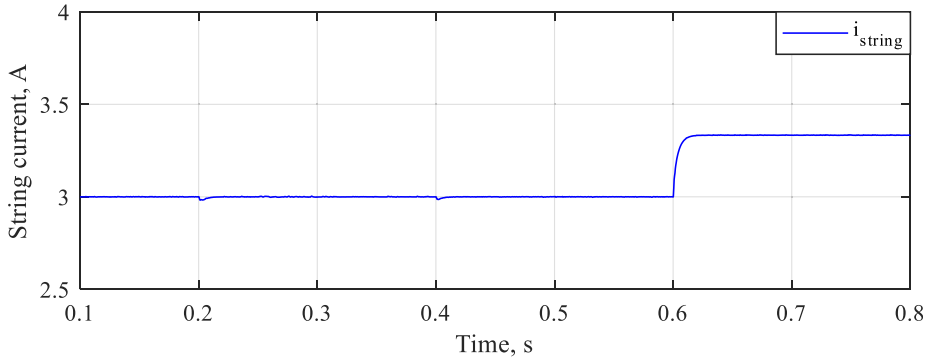


Fig. 12 Server-to-bus architecture (PI optimal string current approach) string current waveform.

currents and string currents that can achieve the same server currents, where the optimal combination cannot be guaranteed due to the nonideality of the practical systems.

Applying KCl at each DAB-server node in Fig. 4, then

$$I_{string} = I_{sk} - I_{Dok} \tag{2}$$

where I_{string} is the string current, $I_{sk}$is the k^{th} server current and I_{Dok} is the output processed current of the k^{th} DAB. The power handled by each DAB (P_{DABk}) is given by

$$P_{DABk} = V_{sk} I_{Dok} \tag{3}$$

where $V_{sk}$is the k^{th} server voltage.

The total processed powers in all DABs (P_{total}) is then given by

$$P_{total} = \sum_{k=1}^{n} V_{sk} I_{Dok} \tag{4}$$

Since the PI controllers equally regulate server voltages, then

$$P_{total} = V_s \sum_{k=1}^{n} I_{Dok} \tag{5}$$

The DAB converter is designed to achieve voltage conversion with ratio $1:n$. Hence, the DAB current of the parallel side I_{Dik} is given by

$$I_{Dik} = I_{Dok}/n \tag{6}$$

Thus, the sum of DAB parallel side currents I_{Di} is obtained by

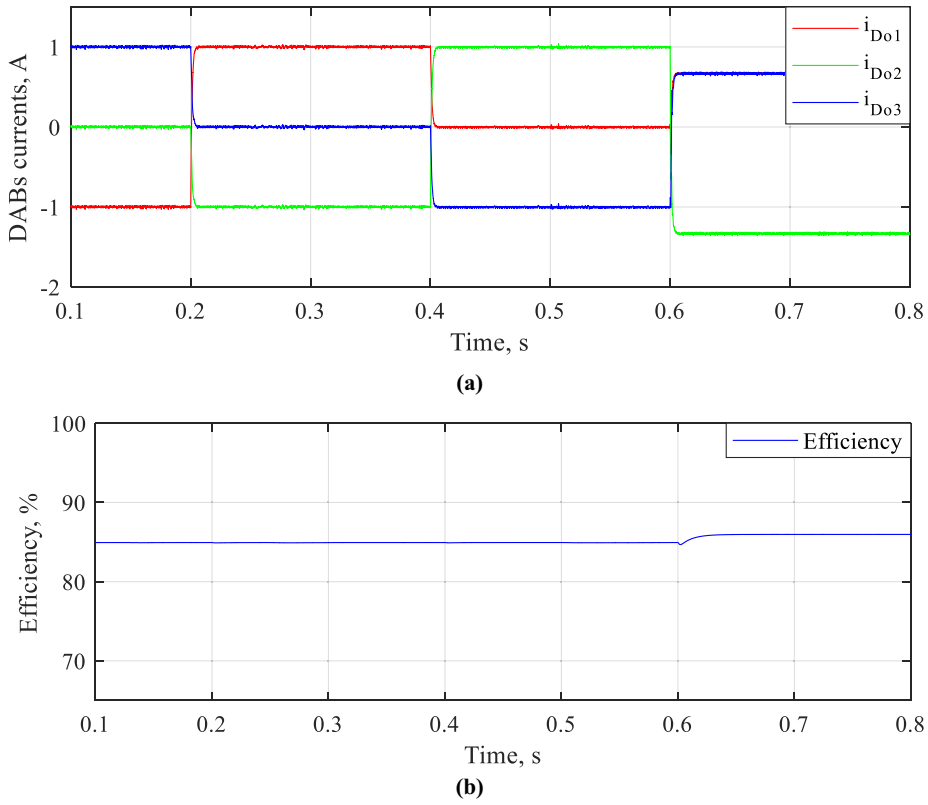


Fig. 13 Server-to-bus architecture (PI optimal string current approach). (a) DAB currents, and (b) efficiency.

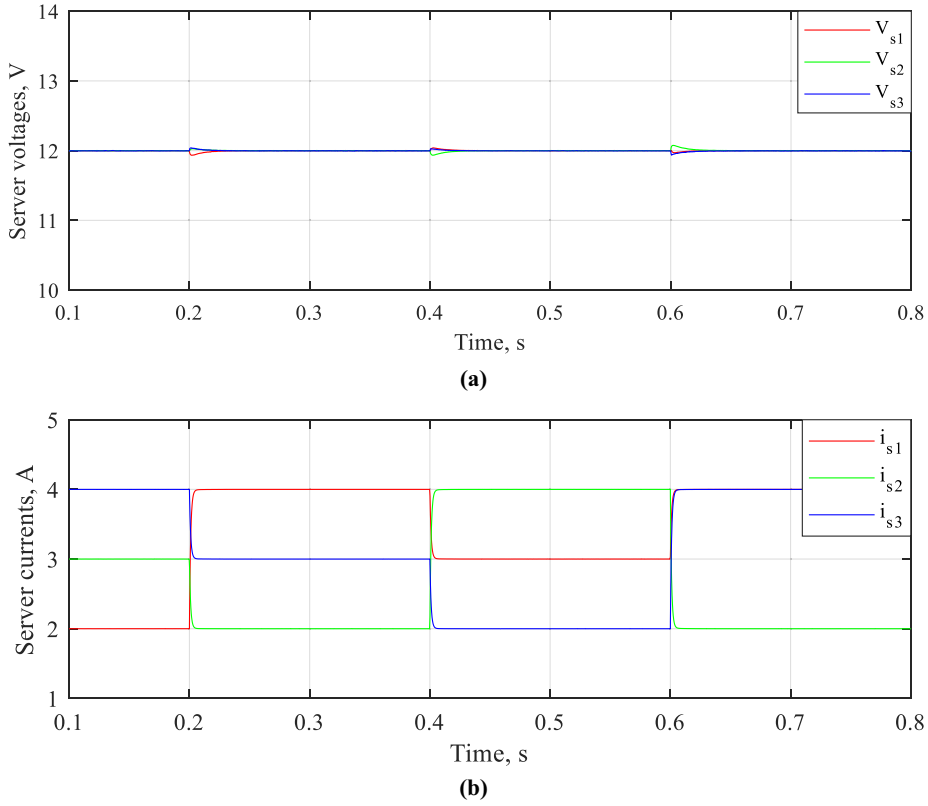


Fig. 14 Server-to- virtual bus architecture (PI independent voltage control approach) simulation results. (a) Servers' voltages. (b) Servers' currents.

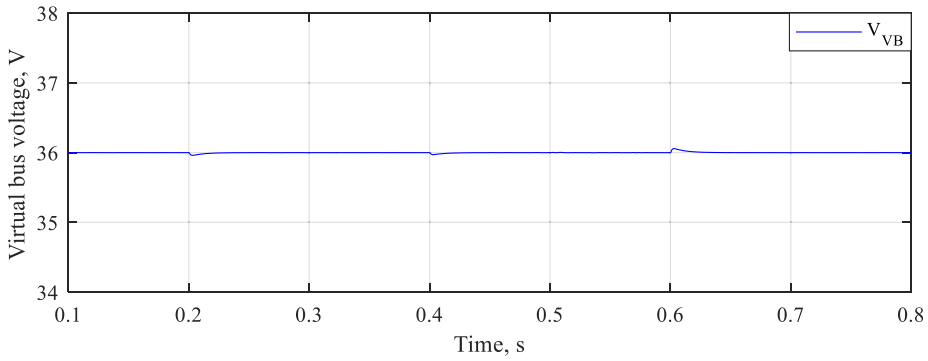


Fig. 15 Server-to-virtual bus architecture virtual bus (PI independent voltage control approach) voltage waveform.

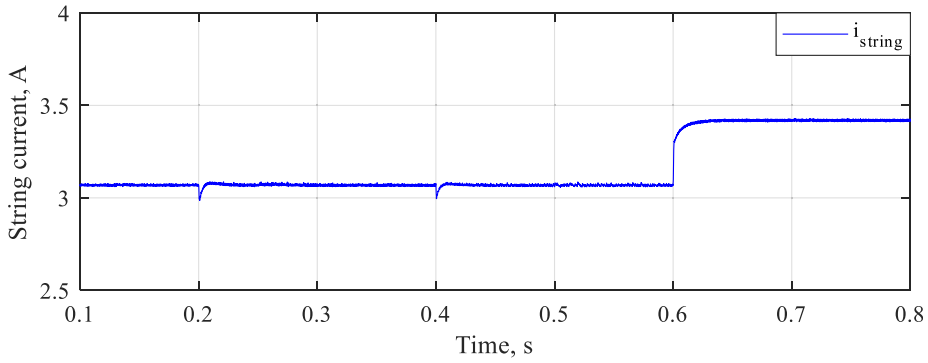


Fig. 16 Server-to- virtual bus architecture (PI independent voltage control approach) string current.

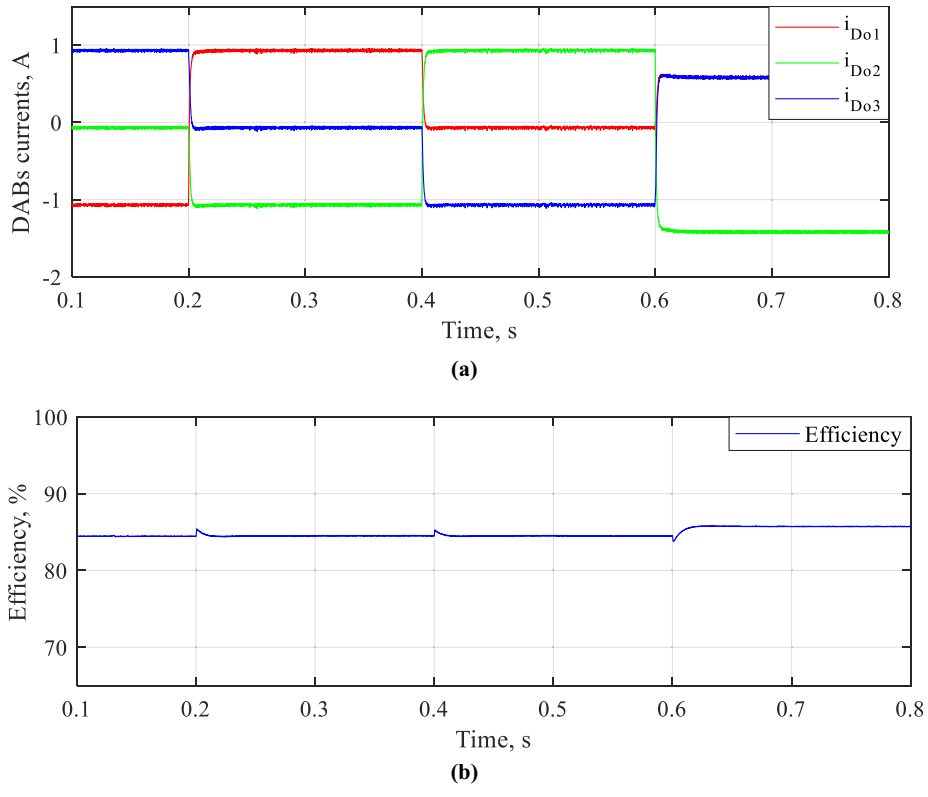


Fig. 17 Server-to- virtual bus architecture (PI independent voltage control approach). (a) DAB currents, and (b) efficiency.

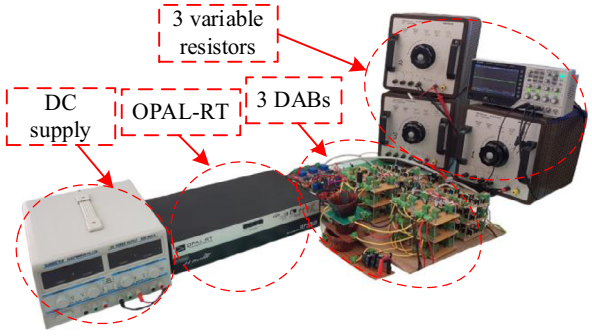


Fig. 18 Experimental setup.

$$I_{Di} = \sum_{k=1}^{n} I_{Dik} = \sum_{k=1}^{n} I_{Dok}/n = \frac{1}{n}\sum_{k=1}^{n} I_{Dok} = \frac{1}{n}\sum_{k=1}^{n}\left(I_{sk} - I_{string}\right) = \left(\frac{1}{n}\sum_{k=1}^{n} I_{sk}\right) - \left(\frac{1}{n}\sum_{k=1}^{n} I_{string}\right) = \left(\frac{1}{n}\sum_{k=1}^{n} I_{sk}\right) - I_{string} \quad (7)$$

Ideally, the bus current I_{Bus} is given by (8), which equals the average value of the servers' currents.

$$I_{Bus} = I_{Di} + I_{string} = \frac{1}{n}\sum_{k=1}^{n} I_{sk} \quad (8)$$

3.1.2. PI optimal string current control approach

In this control approach, the servers' voltages are equally regulated, while the string current is controlled to minimize the total power processed by the DAB converters irrespective of the unavoidable voltage drop due to the parasitic resistance (R_p). The controller block diagram for PI optimal string current control approach is shown in Fig. 5.

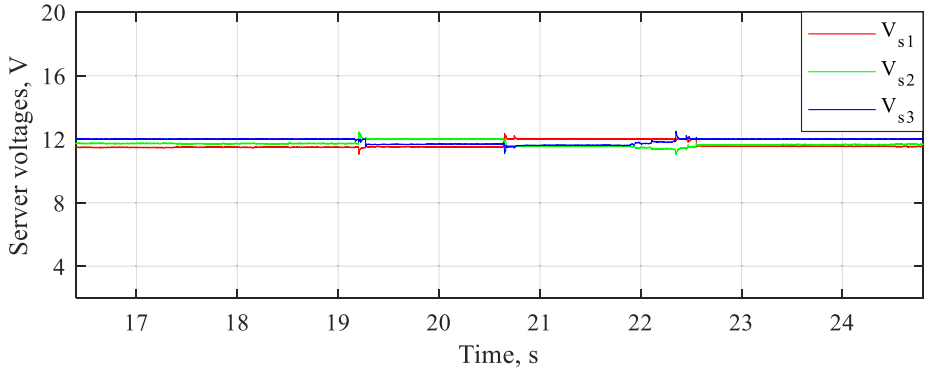
In this case, a higher number of sensors is required because the control algorithm requires both current and voltage measurements. The previous control objectives can be achieved by regulating the string current I_{string} to be equal to the average of the servers' currents given by (9).

$$I_{string} = \frac{1}{n}\sum_{k=1}^{n} I_{sk} \quad (9)$$

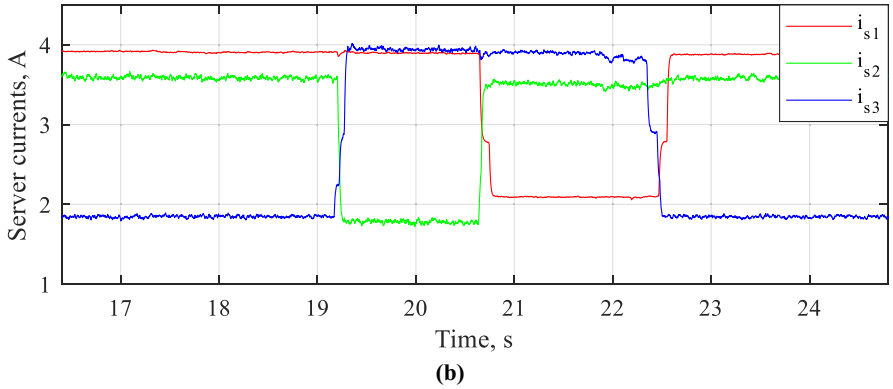
Accordingly, there are $(n+1)$ variables to be controlled, which are the string current I_{string} and n servers' voltages. These $(n+1)$ variables are controlled through n DAB converters. This is achieved by controlling $(n-1)$ servers' voltages using $(n-1)$ DAB converters, while the n^{th}server voltage V_{sn} is naturally regulated to the value given by (10) according to KVL.

$$V_{sn} = V_{Bus} - \sum_{k=1}^{n-1} V_{sk} \quad (10)$$

The n^{th} DAB converter is specifically responsible for controlling the string current I_{string}. Therefore, $(n-1)$ voltage measurement and $(n+1)$ current measurements are required. From (2), the DAB output current I_{Dok} is found as



(a)



(b)

Fig. 19 Server-to-bus architecture (PI voltage control approach) experimental results. (a) Servers' voltages. (b) Servers' currents.

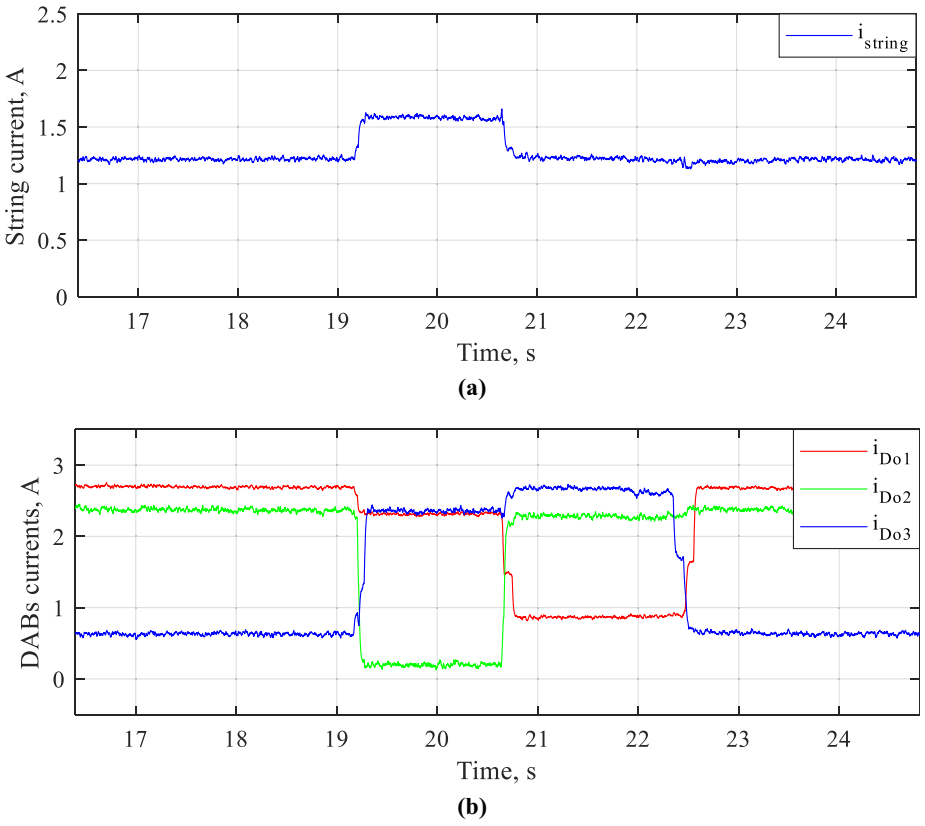


Fig. 20 Server-to-bus architecture (PI voltage control approach) experimental results. (Cont.). (a) String current. (b) DABs output currents.

$$I_{Dok} = I_{sk} - I_{string} \tag{11}$$

From (6), the DAB input current I_{Dik} is given by

$$I_{Dik} = \frac{1}{n}(I_{sk} - I_{string}) \tag{12}$$

By applying KCL at the node of the parallel side of DABs, the total DAB input current I_{Di} is given by

$$\begin{aligned} I_{Di} &= \sum_{k=1}^{n} I_{Dik} = \frac{1}{n}\sum_{k=1}^{n}(I_{sk} - I_{string}) \\ &= \left(\frac{1}{n}\sum_{k=1}^{n} I_{sk}\right) - \left(\frac{1}{n}\sum_{k=1}^{n} I_{string}\right) \\ &= \left(\frac{1}{n}\sum_{k=1}^{n} I_{sk}\right) - I_{string} \end{aligned} \tag{13}$$

From (9), the DAB input current I_{Di} equals

$$I_{Di} = \left(\frac{1}{n}\sum_{k=1}^{n} I_{sk}\right) - I_{string} = I_{string} - I_{string} = 0 \tag{14}$$

This means that the total absolute power processed by DAB converters is minimized and the bus current I_{Bus} is given by (8), which represents the average of the servers' currents.

To generate the error signal required for the DAB that performs the average current control, subtraction is reversed such that the average servers' currents (the reference signal) are subtracted from the actual value of string current. The error signal is then plugged into the PI controller to generate the required phase shift ratio for this particular DAB. The PI optimal string current control approach entirely depends on reversing the power flow to achieve the control objective and thus subtraction reversal is justified.

3.2. Server-to-virtual-bus architecture

The server-to-virtual bus DPP architecture and its PI independent voltage control algorithm are shown in Fig. 6, where n servers are connected in series. Each server is connected to a dual active bridge (DAB) acting as a differential converter. All DABs are then connected to a common capacitor representing a virtual dc bus. The PI independent voltage control algorithm aims to independently balance the voltages among the series-connected servers as well as maintaining the voltage of the virtual bus constant. Therefore, the servers' voltages in addition to the virtual bus voltage are measured and subtracted from reference values and the error is compensated using PI controllers. Since all the servers' voltages are not independent but coupled through their series connection, only $n-1$ DABs are needed to balance the voltages among the series-connected servers, where the voltage of the last server is inherently balanced due to KVL across the series-connected servers as given by (8).

$$V_{Bus} = \sum_{k=1}^{n} V_{sk} \tag{15}$$

Therefore, the goal of the PI controllers of $(n-1)$ DABs is to balance the voltage of their corresponding servers, while the remaining PI controller aims to keep the voltage of the

virtual bus constant, where $V_s^*$and V_{VB}^* are the reference values for the server voltage and the virtual bus voltage, respectively. In the case of virtual bus voltage control, the subtraction has been reversed for both the reference and actual voltages, as depicted in Fig. 6. This is simply because the power flow direction of the DAB controlling the virtual bus voltage has to be reversed.

Each PI controller produces the required duty ratio D_k of the corresponding DAB. Due to the server-to-virtual-bus architecture, there are no restrictions on the HFT turns ratio. Assuming a $1:m$ turns ratio, then

$$I_{Dik} = \frac{I_{Dok}}{m} \tag{16}$$

After applying KCL on each server node, then

$$I_{string} = I_{bus} = I_{sk} - I_{Dok} \tag{17}$$

The instantaneous voltage of the virtual bus is given by (18).

$$V_{VB}(t) = V_{VB}(t_0) + \frac{1}{C_{VB}} \int_{t_0}^{t} I_{VB}(\tau) d\tau \tag{18}$$

where V_{VB} and I_{VB} are the instantaneous values of virtual bus voltage and current, respectively, while C_{VB} refers to the virtual bus capacitance. According to (18), after applying the PI independent voltage control approach control of the virtual bus topology, the virtual bus voltage V_{VB} is maintained constant resulting in a zero virtual bus average current.

Applying KCL at the virtual bus side

$$I_{VB} = \sum_{k=1}^{n} I_{Dik} = 0 \tag{19}$$

Substituting by (16) into (19) gives (20).

$$I_{VB} = \sum_{k=1}^{n} \frac{I_{Dok}}{m} = 0 \tag{20}$$

Substituting (11) in (20), then

$$\sum_{k=1}^{n} \left(\frac{I_{sk} - I_{string}}{m} \right) = 0 \tag{21}$$

Finally, I_{string} is deduced and given by (22).

$$I_{string} = \frac{\sum_{k=1}^{n} I_{sk}}{n} \tag{22}$$

Since the string current is the average of the server currents despite the value of R_p is, then the processed current by each DAB is minimized and the efficiency is intrinsically maximized.

4. System design

This section is intended to provide a detailed design procedure that is employed to perform the simulation and experimental investigation of differential power processing for the server-to-bus architecture and server-to-virtual bus architecture. The design procedure includes the transformer leakage inductance, transformer turns ratio, and sizing of virtual bus capacitance.

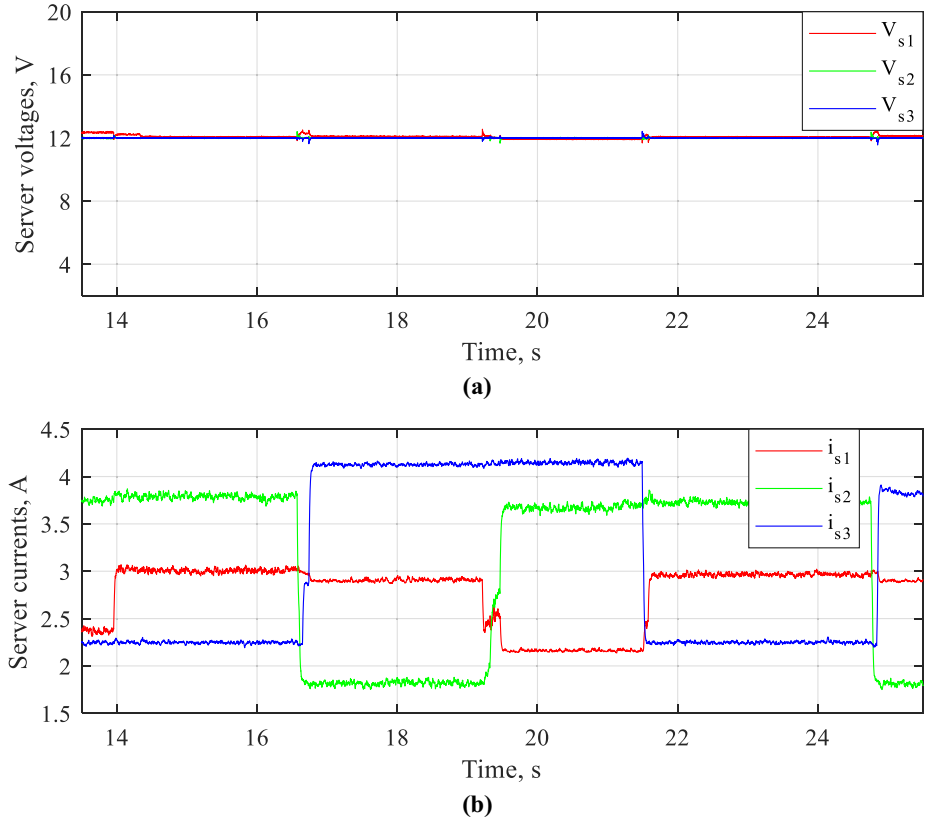


Fig. 21 Server-to-bus architecture (PI optimal string current approach) experimental results. (a) Servers' voltages. (b) Servers' currents.

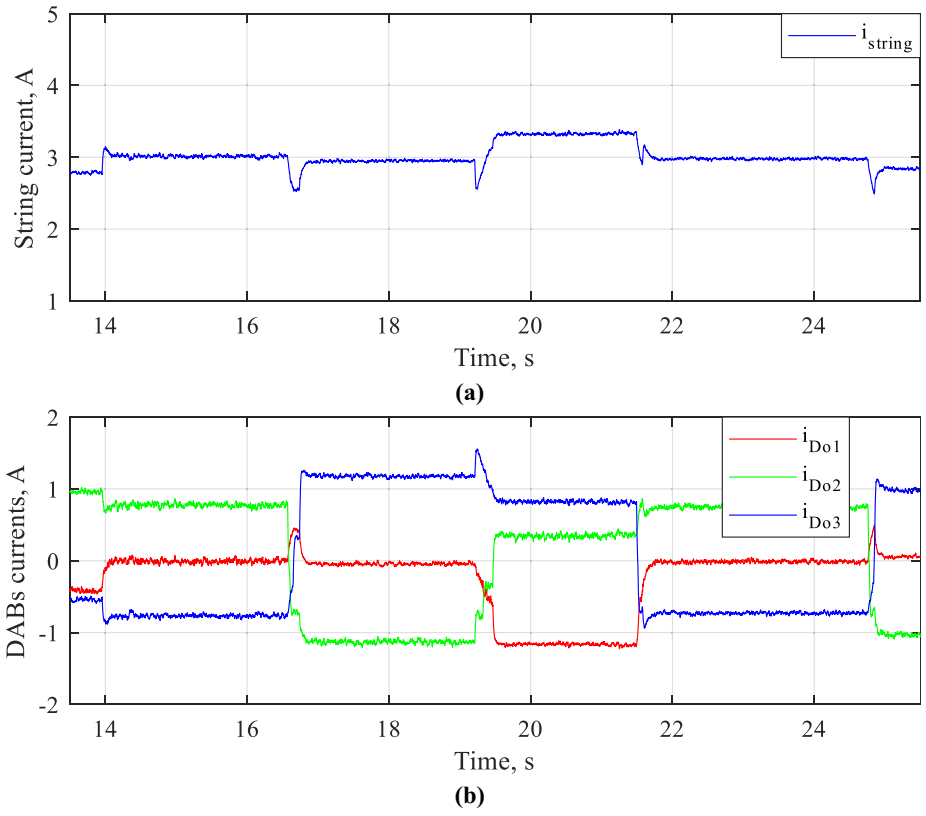


Fig. 22 Server-to-bus architecture (PI optimal string current approach) experimental results (Cont.). (a) String current. (b) DABs output currents.

4.1. Transformer

The power delivered by each DAB is determined according to the following equation as in [21]

$$P = \frac{mV_1V_2D(1-D)}{2f_sL} \tag{23}$$

where m is the transformer turns ratio, V_1, V_2 are the voltage of the primary and secondary sides, respectively, f_s is the switching frequency, and D is the phase shift ratio which ranges from -0.5 to 0.5.

The leakage inductance should be designed such that the maximum power delivered by the DAB equals the maximum power mismatch in the data center system, which can increase up to the server rated power. Therefore, the leakage inductance is given by;

$$L = \frac{mV_1V_2}{8f_sP_{rated}} \tag{24}$$

The transformer turns ratio is designed such that it is equal to the number of series-connected DABs ($m = n$) in the server to bus architecture. However, in the server to virtual bus architecture, there is no restriction on the selection of the transformer turns ratio. Hence, the preferred design in this study is a $1:1$turns ratio to decrease the voltage ratings of the employed semiconductor switches.

4.2. Virtual bus capacitor

The design of the virtual bus capacitor, C_{VB}, should carefully be selected to ensure small voltage ripples at the virtual bus side. Applying KCL at the virtual bus capacitor shown in Fig. 6, then

$$I_C = C_{VB}\frac{dV}{dt} = I_{VB} = \sum_{k=1}^{n} I_{Dik} \tag{25}$$

where, $I_C$is the output current of the virtual bus capacitor.

The DAB input current, referred to virtual bus voltage side, is calculated by [32],

$$I_{Di} = \frac{V_{VB}}{2f_sL}D(1-D) \tag{26}$$

Substituting from (26) in (25) gives

$$C_{VB}\frac{\Delta V_{VB}}{\Delta T} = \sum_{k=1}^{n}\frac{V_{VB}}{2f_sL}D_k(1-D_k) \tag{27}$$

where $\Delta V_{VB}$is the virtual bus voltage ripple and ΔT is the time difference, which can be substituted by $(1/f_s)$. Then, from (27), the value of the capacitance can be found as,

$$C_{VB} = \frac{V_{VB}}{2(\Delta V_{VB}){f_s}^2L}\sum_{k=1}^{n} D_k(1-D_k) \tag{28}$$

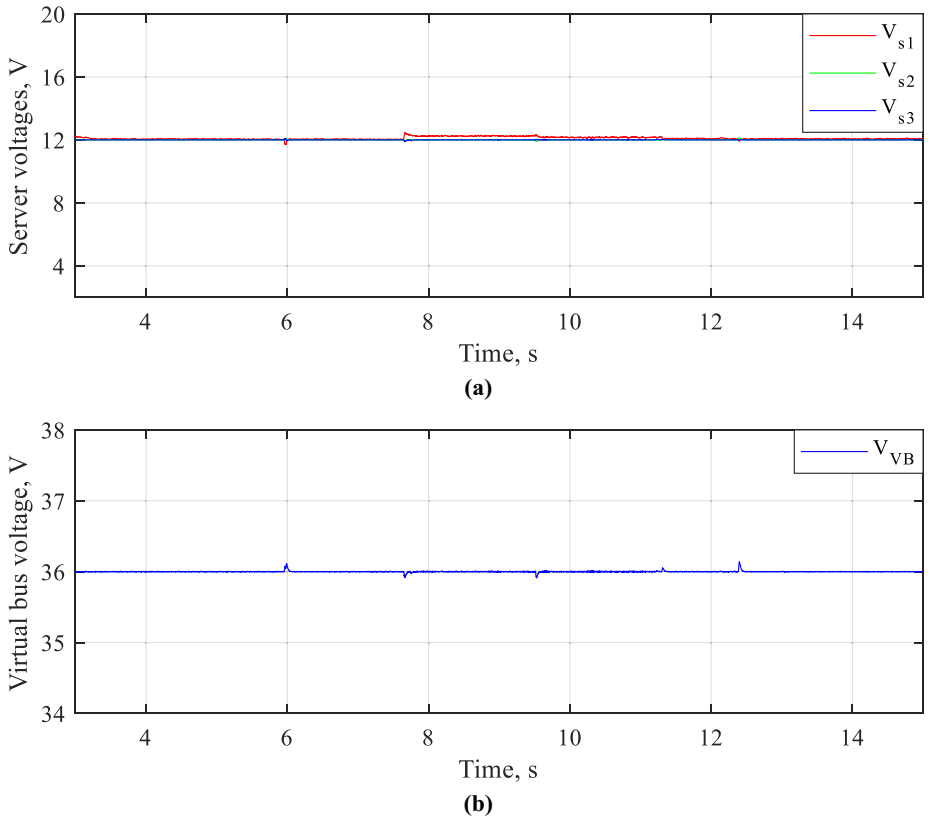


Fig. 23 Server-to-virtual bus architecture (PI independent voltage control approach) experimental results. (a) Server voltages. (b) Virtual bus voltage.

The capacitor should be designed at the worst-case scenario, where all the DABs operate at their maximum ratings such that $D_k = 0.5$. Then, the final capacitor formula is given by;

$$C_{VB} \geq \frac{nV_{VB}}{8(\Delta V_{VB})f_s^2 L} \tag{29}$$

5. Simulation and experimental results

Three MATLAB/SIMULINK models as well as an experimental rig are constructed to validate the proposed control approaches illustrated in the previous sections. The simulation models/experimental prototype comprise three series-stacked servers each rated at 12 V, three DAB converters each have a nominal power of 60 W, operates at 10 kHz, and has a leakage inductance of 30 μH referred to low voltage side, which is calculated according to (24). The transformer turns ratio is 3:1, with a magnetizing inductance referred to the low voltage side of 128 μH. In the case of server-to-virtual bus architecture, for 0.3% voltage ripple magnitude, the virtual bus capacitor should be greater than 4.6 mF, as calculated by (29), so a 6.6 mF capacitor is used. The system parameters are listed in Table 1.

It is worth mentioning that at higher switching frequency than the adopted 10-kHz operation, the virtual bus capacitance value can significantly be reduced. However, the practical investigation in this paper is restricted by the frequency of the selected switch and the hardware gate driver used.

5.1. PI controller tuning

The PI controller gains for all cases are tuned based on online trial and error technique. The values of the proportional component (K_P) and integral component (K_i) of the server-to-bus architecture (PI voltage control approach) are set as 5 and 20000, respectively. PI voltage control approach is only concerned with voltage equalization and there is no control over the string current, therefore; the integral component has to be increased to a notably high value to minimize the steady-state error, which consequently slackens the system response to the variations of the servers' currents. On the other hand, $K_P = 5, K_i = 2000$ are the defined gains for the remaining two control approaches, namely: server-to-bus architecture (PI optimal string current control approach) and server-to-virtual bus architecture. No need for high integral component value in these two latter cases because the string current is controlled either directly in the server-to-bus case or indirectly in the server-to-virtual bus case.

It is worth mentioning that the PI tuning optimization is within the group's future research framework which includes experimental investigation using actual servers.

5.2. Simulation

The objective of the following simulation study is to evaluate/-compare the server operation in the two architectures, namely: server-to-bus architecture (in which two control approaches

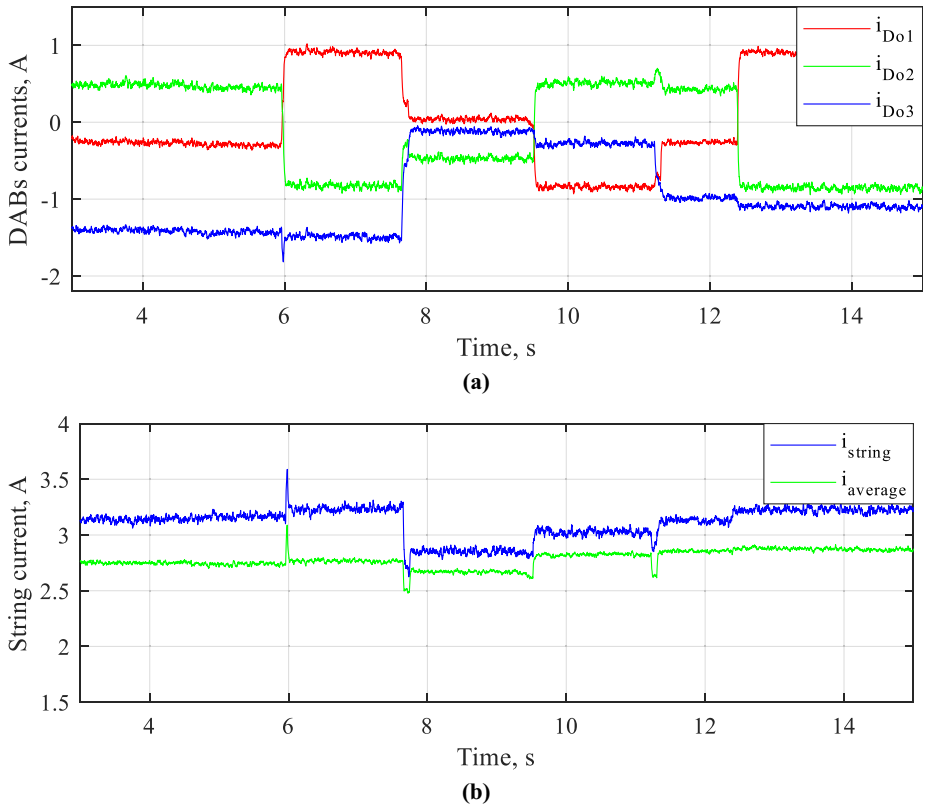


Fig. 24 Server-to-virtual bus architecture (PI independent voltage control approach) experimental results (Cont.). (a) Servers' currents. (b) String current.

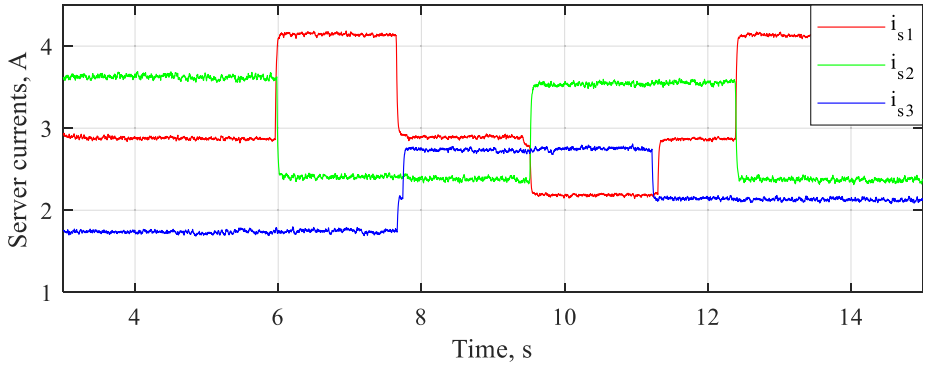


Fig. 25 Server-to-virtual bus architecture (PI independent voltage control approach) experimental results (Cont.) DABs output currents.

are employed) and server-to-virtual bus under the proposed voltage/current control. In the following simulations, servers are modeled as controlled current sources whose loading profiles are shown in Table 2.

5.2.1. Server-to-bus architecture (PI Voltage control approach)

The controller is designed to maintain the server voltages at reference values with a low level of loading mismatch. The goal is achieved using simpler PI control that generates the required duty cycle for the three DABs.

Server voltages V_{sk} and currents I_{sk} under PI voltage control approach are shown in Fig. 7(a) and (b) respectively. The simulation shows that each server can withdraw the required load current while successful voltage balancing is realized at the 12 V voltage level. As previously stated, the string current I_{string} under this approach is uncontrollable, and its profile is shown in Fig. 8. The shortcoming in this control is that the string current profile significantly depends on the parasitic resistance (R_p).

Fig. 8(a) shows the string current assuming an ideal case ($R_p = 0$), which equals the average value of the servers' currents. By assuming a parasitic resistance (R_p) of 0.001 Ω, the string current deviates from the average value of the servers' currents I_{sk}, as shown in Fig. 8(b). This parasitic effect can however be eliminated by applying the PI optimal string current control approach. The DAB converters are operated to compensate for the current mismatch between each server and the actual string current I_{string} throughout the operation.

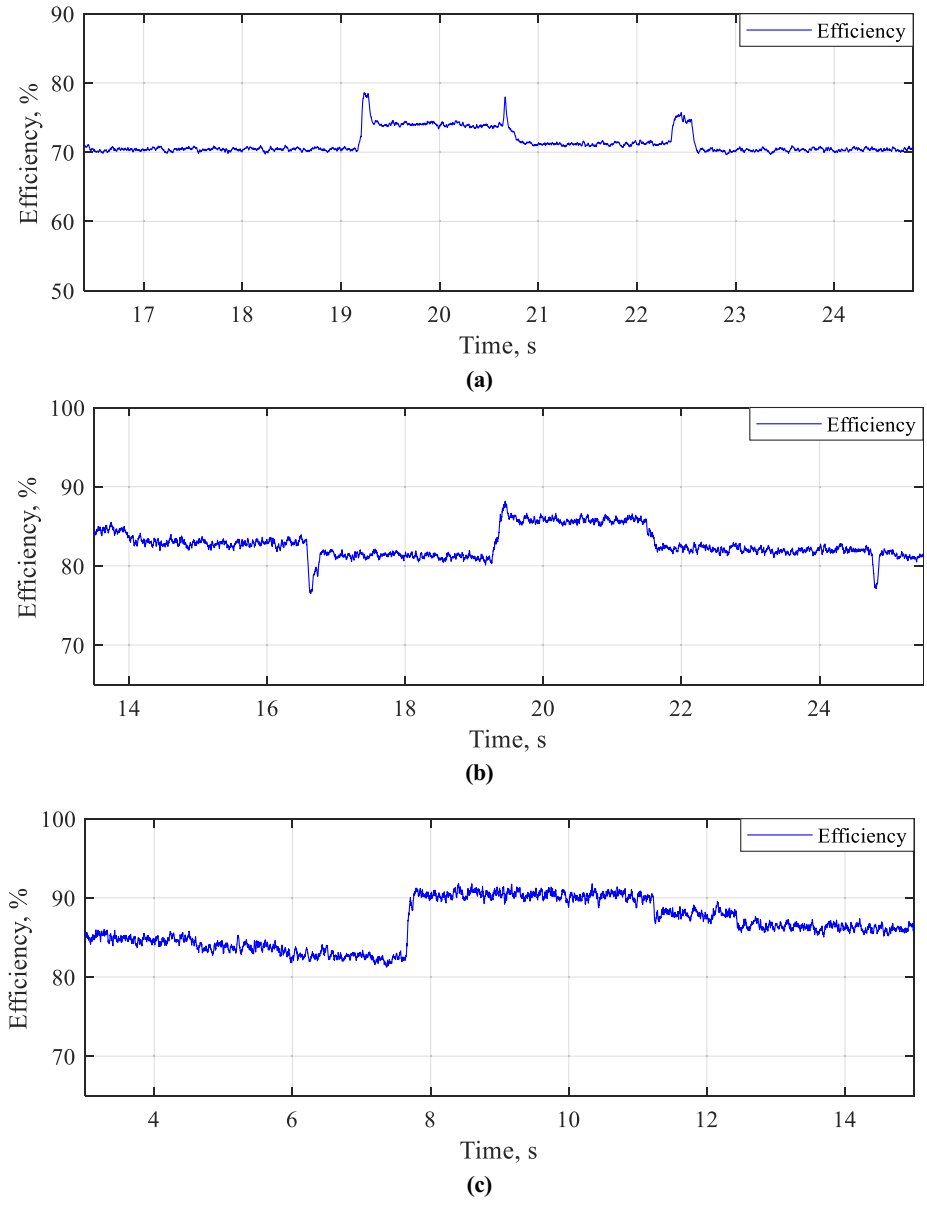


Fig. 26 Experimental efficiency of (a) Server-to-bus architecture (PI voltage control approach), (b) Server-to-bus architecture (PI optimal string current approach), and (c) Server-to-virtual bus architecture (PI independent voltage control approach).

The output currents I_{Dok} of the DABs (processed currents) are shown in Fig. 9(a) under the ideal case, which is minimized. While Fig. 9(b) shows the output currents I_{Dok} of the DABs when a parasitic resistance of 0.001 Ω has been introduced in the series connection loop. In this case, it is evident that the processed current is not minimized and highly susceptible to hardware deficiencies. Therefore, the efficiency of the system is considerably higher in the ideal case and decreases when inserting the parasitic resistance as seen in Fig. 10(a) and (b), respectively.

5.2.2. Server-to-bus architecture (PI optimal string current control approach)

PI optimal string current control approach is designed to maintain the servers' voltages V_{sk} balanced while forcing the average value of the servers' currents I_{sk} to flow through the string regardless of the value of R_P. The simulation results are taken with a parasitic resistance (R_P) of 0.001 Ω. Fig. 11(a) shows a perfect voltage balancing for all servers at 12 V, while the server currents I_{sk} are periodically changing as shown in Fig. 11(b). The string current I_{string} as shown in Fig. 12 is equal to the average value of all currents I_{sk} drawn by the three servers at any given instance of the whole operation period. This leads to minimizing the processed power P_{total} by each DAB converter as clear from the current values I_{Dok} of different DAB converter shown in Fig. 13(a). Resulting in a very high efficiency as seen in Fig. 13(b).

5.2.3. Server-to-virtual-bus architecture

In this architecture, the PI independent voltage control objective is to maintain the server voltages V_{sk} balanced while keep-

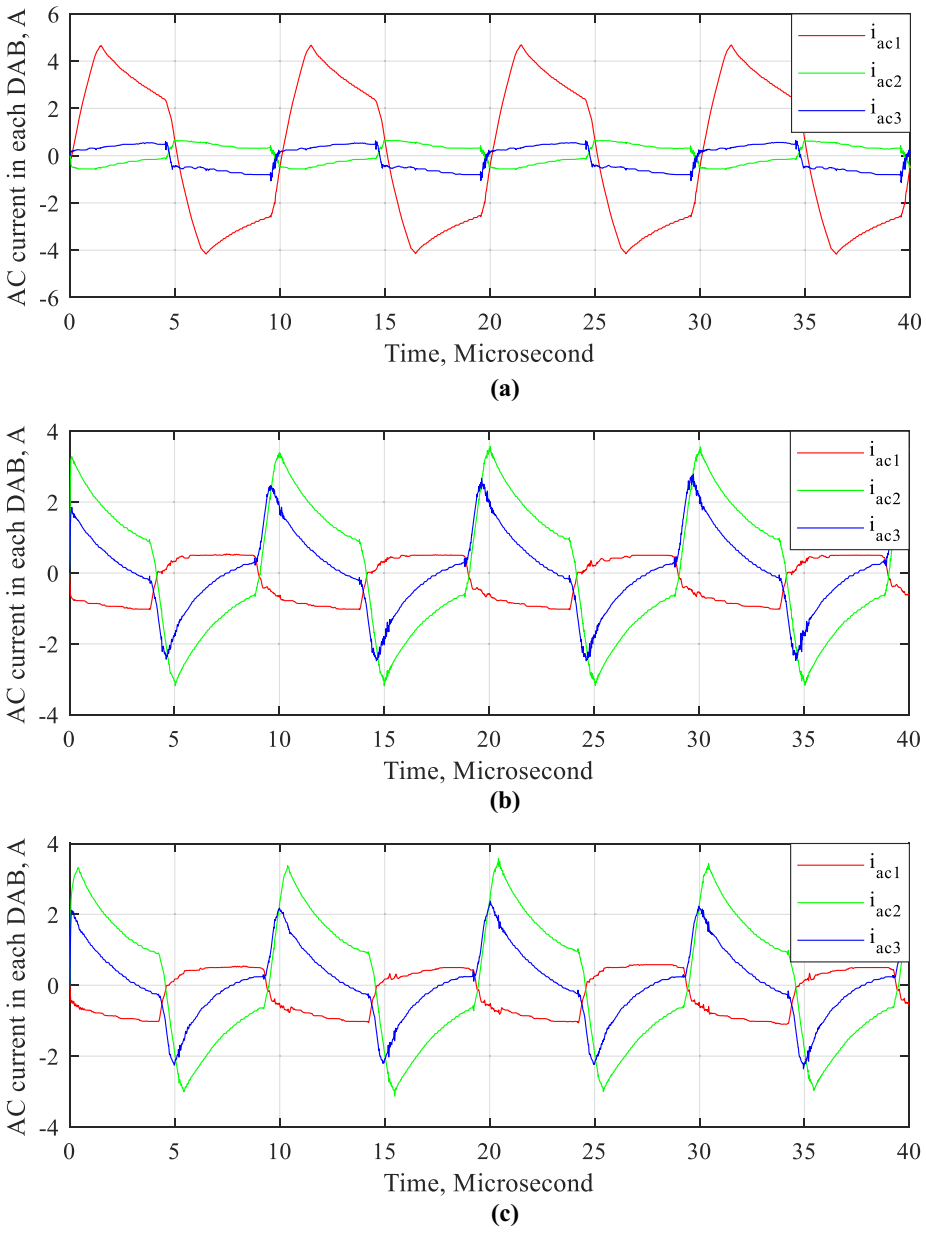


Fig. 27 AC currents in the server-side of the three DABs (a) server-to-bus architecture (PI voltage control approach), (b) server-to-bus architecture (PI optimal string current control approach), and (c) server-to-virtual bus architecture (PI independent voltage control approach).

ing the virtual bus voltage V_{Bus} constant at its reference value. The simulation results are also taken for $R_P = 0.001\ \Omega$. Since the same hardware structure is used for both architectures, the reference virtual bus voltage is set to 36 V.

Fig. 14(a) depicts that the server voltages V_{sk} are well-balanced around their reference value (12 V) regardless of the current variation shown in Fig. 14(b). The virtual bus voltage V_{VB} is successfully maintained constant at its reference value of 36 V, as shown in Fig. 15. Resulting in a string current I_{string} that is inherently equal to the average value of server currents I_{sk} as shown in Fig. 16, which is proved earlier in the mathematical modeling section. This minimizes the total processed power P_{total} shown in Fig. 17(a) and increases the efficiency as depicted in Fig. 17(b).

5.3. Experimental results

An experimental prototype system is constructed as shown in Fig. 18 to validate the simulation results. A real-time simulator (OPAL-RT) is used to control the whole system which offers online measurements and online tuning of the control system parameters. The servers are emulated by variable resistors, whose values are continuously varied to simulate the dynamic server loading. The server-to-bus and the server-to-virtual bus

architectures have been applied and tested with the proposed control approaches.

5.3.1. Server-to-bus architecture (PI voltage control approach)

The experimental test rig is connected as shown in Fig. 4 and the first control approach has been applied, where each DAB is responsible for controlling the voltage of the corresponding server. The control approach successfully maintains the voltage of each server at 12 V, as shown in Fig. 19(a), while the servers' currents I_{sk} are shown in Fig. 19(b). As depicted in Fig. 20(a), string current I_{string} is considerably below the average value of the server currents I_{sk}. Consequently, higher DAB output currents I_{Dok} (processed currents) flow, as shown in Fig. 20(b), due to parasitic resistances discussed earlier.

5.3.2. Server-to-bus architecture (PI optimal string current control approach)

The controller used in this case is shown in Fig. 5, such that one of the DABs is responsible for controlling the string current I_{string} and the rest are responsible for controlling the servers' voltages at 12 V, as shown in Fig. 21(a), regardless of the current variation shown in Fig. 21(b). With this controller, the string current I_{string} equals the average of all server currents, as shown in Fig. 22(a), resulting in the minimization of DAB

output currents I_{Dok} (processed current), as shown in Fig. 22(b). However, all server currents I_{sk} as well as the string current I_{string} need to be measured to apply this control approach.

5.3.3. Server-to-virtual-bus architecture

The experimental setup is reconnected as shown in Fig. 6 to test the server-to-bus architecture with the proposed PI independent voltage control approach. Fig. 23(a) and (b) show the servers' voltages V_{sk} and the virtual bus voltage V_{VB}, respectively, which are successfully maintained at the required values, while the servers' currents I_{sk} change continuously over the whole operation, as depicted in Fig. 24(a). Fig. 25(b) shows the string current I_{string}, which is slightly higher than the servers' average current by about 0.3 A, due to core losses and magnetization currents of transformers. Core losses and magnetization currents are notable in experimental results due to the limited power level of the prototype system. However, in higher power servers, core losses and magnetization currents may be negligible. Nevertheless, even with the notable increase in string current, the DAB differential operation is successfully achieved with low processed DABs output currents (I_{Dok}), as shown in Fig. 25.

The experimental efficiencies are depicted in Fig. 26, where the efficiency of the server-to-bus architecture (PI voltage control approach) shown in Fig. 26(a) is lower than the efficiencies of the server-to-bus architecture (PI optimal string current control approach) and the server-to-virtual bus architecture shown in Fig. 26(b) and (c), respectively. It is evident that the efficiencies in the simulation are nearly the same as that obtained from the experimental setup. Also, the efficiencies can significantly be increased by selecting a transformer with lower core losses.

To evaluate the performance of the DABs in each of the previously discussed architectures with their corresponding control approaches, the ac currents at the server side in each of the three DABs are measured and shown in Fig. 27. The measurements are recorded when the three servers draw 4A, 2A, 3A, respectively. Moreover, ac currents in the case of the server-to-bus architecture (PI voltage control approach), server-to-bus architecture (PI optimal string current control approach), and server-to-virtual bus, are illustrated in Fig. 27(a), (b), and (c), respectively. Obviously, the first case has the highest DAB current, which leads to a lower efficiency converter as mentioned earlier.

6. Conclusion

The operation of *n*-series-stacked servers employing differential power processing concept was investigated in this paper. A comparative study has been conducted to compare three control algorithms based on simple PI controllers. Two control approaches were introduced for the server-to-bus architecture and one control approach was suggested for server-to-virtual bus architecture. A comparative discussion of both architectures under the proposed control approaches based on the experimental investigation is summarized in Table 3.

Server-to-bus is presented with two novel control approaches:

1. The PI voltage control approach is intended to keep server voltage domains all balanced and controlled to operate at the desired reference voltage. Therefore, a voltage measurement is required to employ this control algorithm. This approach is advantageous in terms of reliability because the sustained operation is achieved even when one server

Table 3 Comparison of system performance.

Point of comparison	Server-to-bus (PI voltage control approach)	Server-to-bus (PI optimal string current control approach)	Server-to-virtual bus (PI voltage control approach)
String current	Uncontrollable	Average value of server currents	Average value of server currents
Susceptibility to voltage drop	Dependent	Independent	Independent
Total processed power as a percentage of the total power	High (60%)	Low (20%)	Low (20%)
Efficiency	Low (70%)	High (85%)	High (85%)
Reliability	High	High	Low
Switch voltage rating	Bus voltage and server voltage	Bus voltage and server voltage	Server voltage
Scalability	Not scalable	Not scalable	Scalable
Voltage measurement	Server voltages	Server voltages	Server & virtual bus voltages
Current measurements	None	Servers and string currents	None

is malfunctioning. However, the processed currents in the DABs are high as seen earlier resulting in lower overall efficiency.

2. The second control approach is employed to achieve two goals, namely: to balance the servers' voltages and to force the string current to be the average of all server currents. The processed currents by DABs are minimized, thus, higher overall efficiency is achieved. However, more sensing elements are required, namely: servers' voltage measurement as well as the current measurement of the servers and the string, are needed.

On the other hand, in server-to-virtual bus architecture, the PI independent voltage control aims to balance the server voltages as well as to maintain the virtual bus voltage constant. In this control approach, only voltage measurements for the servers as well as the virtual bus are needed. Merits of this control approach include high efficiency, simple control, and a more flexible transformer design. The turns ratio can be selected to be a 1:1 turns ratio, yielding a reduced voltage rating of the DAB secondary side. The major demerit of this system is its low reliability because when a single DAB is out of service, the whole system fails to operate correctly.

It has to be noted that the efficiencies in Table 3 are not absolute and vary with the system parameters. The efficiency can increase using switches with lower on-state resistance (lower switching losses) and/or using a better material for the transformer core. The merits and demerits of both architectures under different controllers have also been highlighted. One of the major findings of this work is that the switching delay issues in DPP converters' operation can be eliminated using the proposed PI control approach instead of hysteresis controllers, which counts as an advantage given the fast-changing nature of server loading mismatch. PI controller mainly depends on tuning the controller gains for a robust and fixed switching frequency operation. The study showed that the selection between different architectures and controllers involves trade-offs between overall efficiency, reliability, and cost.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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