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*Research Article*

# An Enhanced Space Vector PWM Strategies for Three Phase Asymmetric Multilevel Inverter

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This work presents the two space vector pulse width modulation (SVPWM-I and SVPWM-II) strategies for eleven-level (11L) asymmetric cascaded H-bridge (CHB) multilevel inverter (MLI). Depending on the isolated structure and nonappearance of capacitor voltage balancing issues, the CHB MLI structure is favoured. These days, the SVPWM control method is accomplished superior consideration among the diverse PWM methods. In common, the SVPWM strategy is realized based on deteriorating higher-level hexagons into a lower level hexagon (2-level). Compared to the classical SVPWM strategy, the proposed SVPWM-I strategy decreases the memory and mathematical burden necessity included within the demonstration of eleven-level SVPWM devoid of losing the inverter output voltage (AC) contour by diminution the number of two-level hexagons. Also, the SVPWM-II strategy is presented, which incredibly diminishes the mathematical endeavours. The presented two SVPWM methods performed on an eleven-level asymmetric CHB multilevel inverter (MLI) by utilizing SIMULINK/MATLAB program tool and are compared with conventional sinusoidal PWM and Third harmonic injection (THI) PWM methods to confirm the proposed SVPWM methods. The proposed SVPWM methods give higher AC RMS voltage and lower harmonic distortion when compared to SPWM and THIPWM methods. To validate the presented two SVPWM control schemes, hardware results are taken on asymmetric eleven-level CHB MLI.

## 1. Introduction

In a basic two-level inverter, a lower harmonic in output voltage is obtained by rising the switching frequency, which leads to higher voltage stresses and switching losses upon that switches are the result of a reduction in the step count in the output voltage. The disadvantages in two-level inverter motivate the intrigued on the multilevel inverters (MLIs). In 1991, MLI was presented and its development is quick over a long time [1].

MLIs find widespread use across a variety of sectors today, particularly for high-power and medium-voltage applications [2, 3]. MLIs make use of a greater amount of DC sources and switches to generate a staircase waveform that is more similar to a sinusoidal signal and has a lower level of harmonic distortion [4]. MLIs provide several advantages over classical two-level inverters, including a higher basic output voltage, a lower common mode voltage and switching loss, a reduction in EMI, and a reduction in THD [5]. As a result of these benefits, MLIs may be utilized in a diverse collection of contexts, such as in HVDC, FACTS, electric cars, and solar power systems [6–8]. The CHB inverter, which was discovered by Peng and Lai [9] the flying capacitor (FC) inverter, which was discovered by Meynard

and Foch [10] and the neutral point clamped (NPC) inverter, which was discovered by Nabae et al. [11] are the three established MLI topologies that are used the most frequently. The only difference between NPC and FC topologies is that NPC uses diodes in a ladder configuration while FC uses capacitors in a ladder configuration. To produce higher inverter levels, NPC, and FC both need a greater number of power components, and they both struggle with voltage imbalance [12, 13]. H-bridge cells are connected in series in the CHB topology, and the modular topology is created by the requirement that each cell has its own DC source. Both three-phase and single-phase power conversion can benefit from this CHB topology. CHB MLIs are one of the three fundamental MLI topologies and are ideal for PV applications [14, 15]. In this work, CHB inverter topology is considered and is operated in an asymmetric mode to realize an eleven-level inverter. Figure 1 depicts the three-phase asymmetric CHB 11L inverter. Table 1 depicts the switching logic of an asymmetric CHB eleven-level inverter.

The SVPWM [16] and the level-shifted multicarrier SPWM [17] are the two inverter modulation methods that are used most often for MLIs. To identify the switching states of an MLI in SPWM, a sinusoidal signal of the appropriate phase is compared to a high-frequency triangular carrier waveform. To create gate pulses in an 11-L inverter, ten carrier waveforms are compared with a single modulating signal. If a sinusoidal signal with a frequency three times that of the modulating signal is added to the modulating signal in the SPWM method, it is referred to as a third harmonic injection (THI) PWM. The THI signal's magnitude is determined by the modulating signal's amplitude. If $k$ is the amplitude of the modulating signal, then $k/4$ or $k/6$ is the magnitude of the common mode signal for better results. The magnitude of the reference signal ($k$) is changed to $1.154k$ in THIPWM to achieve high DC bus usage. Both SPWM and THIPWM schemes lack redundancy switching states, which are particularly helpful for a variety of applications [17].

The SVPWM approach, on the other hand, provides greater DC source utilization, reduced THD, and common mode voltage (CMV) [18–20]. In addition, it enables the balancing of capacitor voltage concerns through the assistance of a redundant switching state [21]. And also, the reliability of the MLIs can be improved with the use of redundancy switching states in the SVPWM technique [22]. SPWM technique is also simpler to implement for various applications [23]. SVPWM implementation via digital means is simpler. SVPWM is therefore the preferred PWM method for industrial applications [24, 25]. Finding the sector in which the reference voltage ($V_{ref}$) is located is the first step in implementing the SVPWM [26], which is then followed by choosing a triangle within that sector based on the location of $V_{ref}$, computing dwell times and choosing the best switching times to generate gate signals for power switches in an MLI. SVPWM implementation for an MLI is challenging for the reason that complexity rises as inverter levels rise [27].

Article [28] presents an SVPWM method for a 3L (level) inverter in which they split the 3L hexagon into six 2L

hexagons. To implement 3L SVM similarly to the 2L SVM approach, the center of the 3L hexagon is moved to the corresponding 2L hexagon. Euclidean vector approach is used in [29] to implement generalised SVM for an N-level inverter. According to [30], a fractal concept related SVPWM approach for MLI involves knowing the triangle where the $V_{ref}$ tip lies using a triangularization procedure. In [31], the initial 5L space vector diagram (SVD) was broken up into six 3L hexagons, and then each of those was split into six 2L hexagons prior to the standard procedure was used to acquire SVPWM for five-level inverters.

In [32], the 7L SVPWM was first disintegrated into six 4L hexagons, and the 4L hexagon was then divided into 2L hexagons. The usual conventional process was then used to realise the seven-level SVPWM. In [33], the nine-level SVPWM was first disintegrated into six 5L hexagons, and the 5L hexagon was then divided into 2L hexagons. Then, the conventional process was then used to realise the nine-level SVPWM. MLI output phase voltage levels range from $+P_5$ (equivalent +ve peak level) to $-N_5$ (equivalent -ve peak level) as shown in Figure 2, according to the SVD for eleven-level inverters. The switching instants for an N-level inverter is typically $N^3$. $3N^2 - 3N + 1$ are independent switching possibilities out of $N^3$, and the left behind switching instants are redundant switching possibilities. It consists of $(N-1)^3$ triangles and $(N-1)$ layers in N-level SVD. As a result, an inverter has $11^3 = 1331$ switching instants available for 11-level inverters. There are 331 independent switching instants and 1000 redundant switching instants out of the total 1331 switching instants. The space vector diagram contains 1000 triangles and has 10 layers.

In this work, presents the two SVPWM techniques, namely, SVPWM-I and SVPWM-II strategies for eleven-level asymmetric cascaded H-bridge MLI. Without sacrificing the AC voltage profile at the MLI output, the proposed two SVPWM technique drastically lessens the computational load associated with the SVPWM for an 11-level inverter. Reduced from 1331 to 222 counts, the number of 2L hexagons needed for an eleven-level inverter. It is also shown in the SVPWM-II technique, which significantly reduces computation time by switching from 222 to 1862-level hexagons. The proposed SVPWM methods that have been proposed are tested on an eleven-level inverter and evaluated against the widely used SPWM and THIPWM techniques. The proposed SVPWM schemes have undergone an experimental setup for validation.

## 2. Proposed SVPWM-I Technique

The lower level SVD is disintegrated into 2L hexagons as part of the SVPWM-I technique. Figure 2 displays the 11L SVD. As shown in Figure 2, the 11L SVD is first divided into six 6L hexagons. Hexagon-I is the first six-level hexagon, and its midpoint is by the side of the 0°axis. The midpoint of every subsequent 6L hexagon is then 60°off. To prevent overlap between adjacent hexagons, the appropriate hexagon is chosen by considering the $V_{ref}$ angle's value. Depending on the angle of the $V_{ref}$, Table 2 displays the selection of 6L hexagons from 11L SVD.
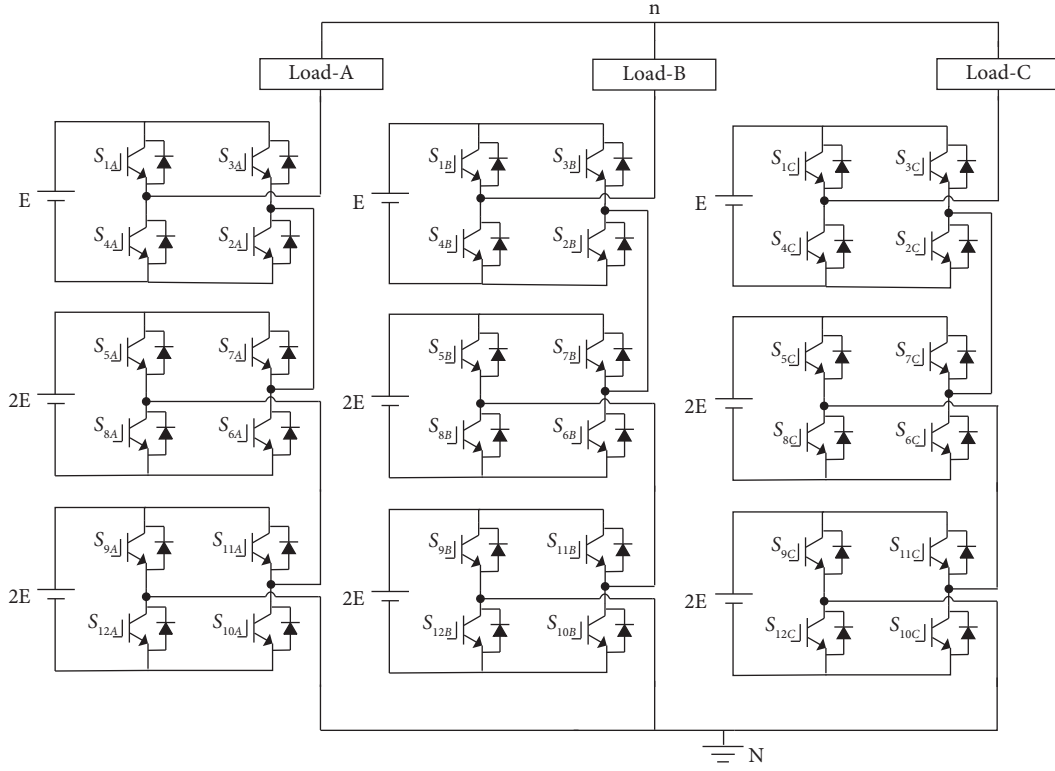
Figure 1: Three phase asymmetric 11L CHB inverter configuration.

Table 1: Switching states of eleven-level CHB inverter.

| Voltage level | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | $S_9$ | $S_{10}$ | $S_{11}$ | $S_{12}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $+5E$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $+4E$ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $+3E$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| $+2E$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| $+E$ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $-E$ | 0′ | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $-2E$ | 1 | 0 | 1 | 0 | 0′ | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| $-3E$ | 0′ | 1 | 0 | 1 | 0′ | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| $-4E$ | 1 | 0 | 1 | 0 | 0′ | 1 | 0 | 1 | 0′ | 1 | 0 | 1 |
| $-5E$ | 0′ | 1 | 0 | 1 | 0′ | 1 | 0 | 1 | 0′ | 1 | 0 | 1 |



Figure 2: 11L SVD with reference vector mapping and its disintegration to 6L SVDs.

Once a six-level hexagon is chosen, a new reference vector, $V_{ref6}$, that originates from the centre of the chosen six-level hexagon is needed to align the vector tips of $V_{ref}$ and $V_{ref6}$. Take as an illustration that the tip of $V_{ref}$ is located in Hexagon-I shown in Figure 2. Here, as shown in Figure 2, the reference signal $V_{ref}$ and the mapped reference vector $V_{ref6}$ from Hexagon-I are coincident with their tips. Precisely, the imaginary($\beta$-axis)and real ($\alpha$-axis) components of mapped vector $V_{ref}$ can be derived from $V_{ref}$ as follows:

$$V_{6\alpha} = V_{11\alpha} - 5E,$$
$$V_{6\beta} = V_{11\beta}. \tag{1}$$

Here, the components of $V_{ref6}$ and $V_{ref}$ along the $\alpha$-axis and $\beta$-axis, correspondingly, are $V_{6\alpha}$ and $V_{6\beta}$, and $V_{11\alpha}$ and $V_{11\beta}$. The reference vector ($V_{ref}$) mapping to other six-level hexagons can be examined similarly, as shown in Table 3. By calculating the $V_{ref6}$ vector, the 11L SVPWM problem is reduced to a 6L SVPWM problem.

The 6L is then disintegrated into 2L hexagons as the next step. Figure 3 illustrates how a 6L hexagon can be reduced to

TABLE 2: Selection of 6L hexagons from 11L SVD.

| Hexagon No | Range of $\theta$ |
| --- | --- |
| I | 330° to 30° |
| II | 30° to 90° |
| III | 90° to 150° |
| IV | 150° to 210° |
| V | 210° to 270° |
| VI | 270° to 330° |

TABLE 3: Mapping of $V_{\text{ref6}}$ from $V_{\text{ref11}}$.

| Hexagon No | $V_{6\alpha}$ | $V_{6\beta}$ |
| --- | --- | --- |
| I | $V_{11\alpha} - 5E$ | $V_{11\beta}$ |
| II | $V_{11\alpha} - 5E\cos(\pi/3)$ | $V_{11\beta} - 5E\sin(\pi/3)$ |
| III | $V_{11\alpha} - 5E\cos(2\pi/3)$ | $V_{11\beta} - 5E\sin(2\pi/3)$ |
| IV | $V_{11\alpha} + 5E$ | $V_{11\beta}$ |
| V | $V_{11\alpha} - 5E\cos(4\pi/3)$ | $V_{11\beta} - 5E\sin(4\pi/3)$ |
| VI | $V_{11\alpha} - 5E\cos(5\pi/3)$ | $V_{11\beta} - 5E\sin(5\pi/3)$ |



FIGURE 3: Disintegration of 6L SVD to lower-level hexagons.

a two-level one by having an inner 4L hexagon with thirteen 2L hexagons and an outer one with 24 two-level hexagons. Thus, there are thirty-seven 2L hexagons in total for each 6L hexagon. Depending on the angle and magnitude of $V_{\text{ref6}}$, outer and inner 2L hexagons are chosen. Assume that outer 2L hexagons are chosen if the magnitude value of the vector $V_{\text{ref6}}$ is greater than magnitude $3E$, and inner 2L hexagons are chosen if the magnitude value of the vector $V_{\text{ref6}}$ falls below the value of $3E$. The 6L SVD is then disintegrated into 2L hexagons as the next step. Table 4 displays the selection of the outer twenty-four 2L hexagons in a 6L SVD.

A new reference vector, let us call it $V_{\text{ref2O}}$, that comes from the centre of the chosen outer 2L hexagons is needed if any outer 2L hexagons is chosen. Here, the $V_{\text{ref6}}$ and $V_{\text{ref2O}}$ tips are in sync. Take the tip of $V_{\text{ref}}$ as an example; it is located in the outer 2L hexagon-3 (i.e., OH3) in Figure 4. The following diagram shows how to calculate the vector $V_{\text{ref2O}}$ mathematically from $V_{\text{ref6}}$.

$$
\begin{aligned}
V_{2\alpha O} &= v_{6\alpha} - 3.46E\cos\left(\frac{\pi}{6}\right), \\
V_{2\beta O} &= v_{6\alpha\beta} - 3.46E\cos\left(\frac{\pi}{6}\right).
\end{aligned}
\tag{2}
$$

Here, the components of $V_{\text{ref6}}$ and $V_{\text{ref2}}$ along the $\alpha$-axis and $\beta$- axis, correspondingly, are $V_{6\alpha}$ and $V_{6\beta}$, and $V_{2\alpha O}$ and $V_{2\beta O}$, respectively. Consequently, the mapping of $V_{\text{ref6}}$ to the remaining twenty-three outer 2L hexagons in a 6L SVD can be analysed similarly, as given in Table 4. The 6L hexagon-I is depicted in Figure 5 along with all potential switching instants. Figure 5 illustrates how the number of space vector redundancies rises beginning from the outer layer to the centre. The eleven-level SVD's centre has the most space vectors, ten of which are redundant.

A new reference vector, let us call it $V_{\text{ref2i}}$, that comes from the centre of the chosen inner 2L hexagons is needed if inner four-level hexagons, which are a grouping of thirteen 2L hexagons, are chosen. Here, the $V_{\text{ref6}}$ and $V_{\text{ref2i}}$ tips are identical is shown in Figure 6. Table 5 illustrates how a four-
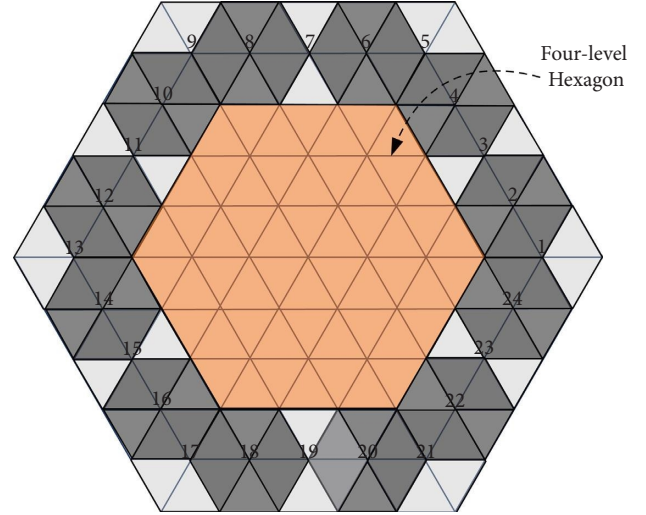
level hexagon's inner 2L hexagons are chosen depending on the magnitude of $V_{\text{ref6}}$. Consider the tip of $V_{\text{ref6}}$ as an example, which is located in the inner 2L hexagon-1 in Figure 6. The following diagram shows how to calculate the vector $V_{\text{ref2i}}$ mathematically from $V_{\text{ref6}}$.

$$
\begin{aligned}
V_{2\alpha i} &= V_{6\alpha} - 2E, \\
V_{2\beta i} &= V_{6\beta}.
\end{aligned}
\tag{3}
$$

Here, the components of $V_{\text{ref6}}$ and $V_{\text{ref2i}}$ along the $\alpha$-axis and $\beta$- axis, correspondingly, are $V_{6\alpha}$ and $V_{6\beta}$, and $V_{2\alpha}$ and $V_{2\beta}$, respectively. Consecutively in a 4-level SVD of a six-level SVD, $V_{\text{ref6}}$ mapping to the other 13 inner two-level hexagons can be analysed similarly is shown in Table 5. Thus, by locating the $V_{\text{ref2}}$ vector, the 11L SVM problem is reduced to a 2LSVM.

### 2.1. Calculation of Switching Sequence and Dwell times.

The switching times and dwell times are derived in a manner akin to the classical 2L hexagon. Every one of the six sectors in a two-level hexagon can be realised with a reference vector ($V_{\text{ref}}$) using one of the three switching states that are available. Based on the volt-sec-balancing method, the time spent in each switching state is determined. Consider the mapped reference vector $V_{\text{ref2O}}$, which is depicted in Figure 7 as being located in the outermost 2L hexagon (OH3) of the 6L hexagon-I.

Figure 7 shows $P_5N_3N_5$ as the active switching state ($V_1$), $P_5N_2N_5$ as the active switching state ($V_2$), and $P_5N_2N_4$ or $P_4N_3N_5$ as the zero switching states ($V_0$). For switching between states $V_1$, $V_2$, and $V_0$, the dwell times are $T_1$, $T_2$, and $T_0$, correspondingly.

The terms to derive the dwell times meant for $V_1$, $V_2$, and $V_0$ are as follows:

$$
\begin{aligned}
T_1 &= T_s \, x \, M \, x \, \sin(60 - \theta), \\
T_2 &= T_s \, x \, M \, x \, \sin(60), \\
T_0 &= T_s - T_1 - T_2.
\end{aligned}
\tag{4}
$$

TABLE 4: Selection of outer 2L hexagons from 6L SVD and mapping of $V_{ref2O}$ from $V_{ref6}$.

| Hexagon No | Range of $\theta$ | $V_{2\alpha o}$ | $V_{2\beta o}$ |
|---|---|---|---|
| OH1 | 348° to 12° | $V_{6\alpha} - 4E$ | $V_{6\beta}$ |
| OH2 | 12° to 24° | $V_{6\alpha} - 3.6E\cos(\pi/12)$ | $V_{6\beta} - 3.6E\sin(\pi/12)$ |
| OH3 | 24° to 36° | $V_{6\alpha} - 3.46E\cos(2\pi/12)$ | $V_{6\beta} - 3.46E\sin(2\pi/12)$ |
| OH4 | 36° to 48° | $V_{6\alpha} - 3.6E\cos(3\pi/12)$ | $V_{6\beta} - 3.6E\sin(3\pi/12)$ |
| OH5 | 48° to 72° | $V_{6\alpha} - 4E\cos(4\pi/12)$ | $V_{6\beta} - 4E\sin(4\pi/12)$ |
| OH6 | 72° to 84° | $V_{6\alpha} - 3.6E\cos(5\pi/12)$ | $V_{6\beta} - 3.6E\sin(5\pi/12)$ |
| OH7 | 84° to 96° | $V_{6\alpha} - 3.46E\cos(6\pi/12)$ | $V_{6\beta} - 3.46E\sin(6\pi/12)$ |
| OH8 | 96° to 108° | $V_{6\alpha} - 3.6E\cos(7\pi/12)$ | $V_{6\beta} - 3.6E\sin(7\pi/12)$ |
| OH9 | 108° to 132° | $V_{6\alpha} - 4E\cos(8\pi/12)$ | $V_{6\beta} - 4E\sin(8\pi/12)$ |
| OH10 | 132° to 144° | $V_{6\alpha} - 3.6E\cos(9\pi/12)$ | $V_{6\beta} - 3.6E\sin(9\pi/12)$ |
| OH11 | 144° to 156° | $V_{6\alpha} - 3.46E\cos(10\pi/12)$ | $V_{6\beta} - 3.46E\sin(10\pi/12)$ |
| OH12 | 156° to 168° | $V_{6\alpha} - 3.6E\cos(11\pi/12)$ | $V_{6\beta} - 3.6E\sin(11\pi/12)$ |
| OH13 | 168° to 192° | $V_{6\alpha} + 4E$ | $V_{6\beta}$ |
| OH14 | 192° to 204° | $V_{6\alpha} - 3.6E\cos(13\pi/3)$ | $V_{6\beta} - 3.6E\sin(13\pi/12)$ |
| OH15 | 204° to 216° | $V_{6\alpha} - 3.46E\cos(14\pi/12)$ | $V_{6\alpha} - 3.46E\sin(14\pi/12)$ |
| OH16 | 216° to 228° | $V_{6\alpha} - 3.6E\cos(15\pi/12)$ | $V_{6\beta} - 3.6E\sin(15\pi/12)$ |
| OH17 | 228° to 252° | $V_{6\alpha} - 4E\cos(16\pi/12)$ | $V_{6\beta} - 4E\sin(16\pi/12)$ |
| OH18 | 252° to 264° | $V_{6\alpha} - 3.6E\cos(17\pi/12)$ | $V_{6\beta} - 3.6E\sin(17\pi/12)$ |
| OH19 | 264° to 278° | $V_{6\alpha} - 3.46E\cos(18\pi/12)$ | $V_{6\beta} - 3.46E\sin(18\pi/12)$ |
| OH20 | 278° to 290° | $V_{6\alpha} - 3.6E\cos(19\pi/12)$ | $V_{6\beta} - 3.6E\sin(19\pi/12)$ |
| OH21 | 290° to 314° | $V_{6\alpha} - 4E\cos(20\pi/12)$ | $V_{6\beta} - 4E\sin(20\pi/12)$ |
| OH22 | 314° to 326° | $V_{6\alpha} - 3.6E\cos(21\pi/12)$ | $V_{6\beta} - 3.6E\sin(21\pi/12)$ |
| OH23 | 326° to 337° | $V_{6\alpha} - 3.46E\cos(22\pi/12)$ | $V_{6\beta} - 3.46E\sin(22\pi/12)$ |
| OH24 | 337° to 348° | $V_{6\alpha} - 3.6E\cos(23\pi/12)$ | $V_{6\beta} - 3.6E\sin(23\pi/12)$ |
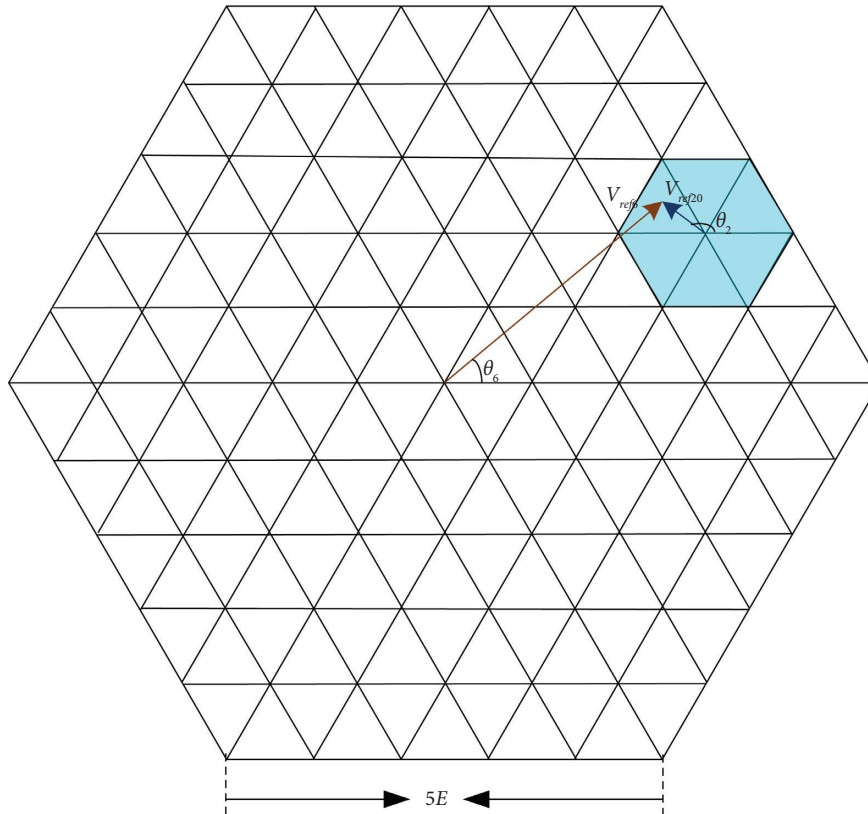


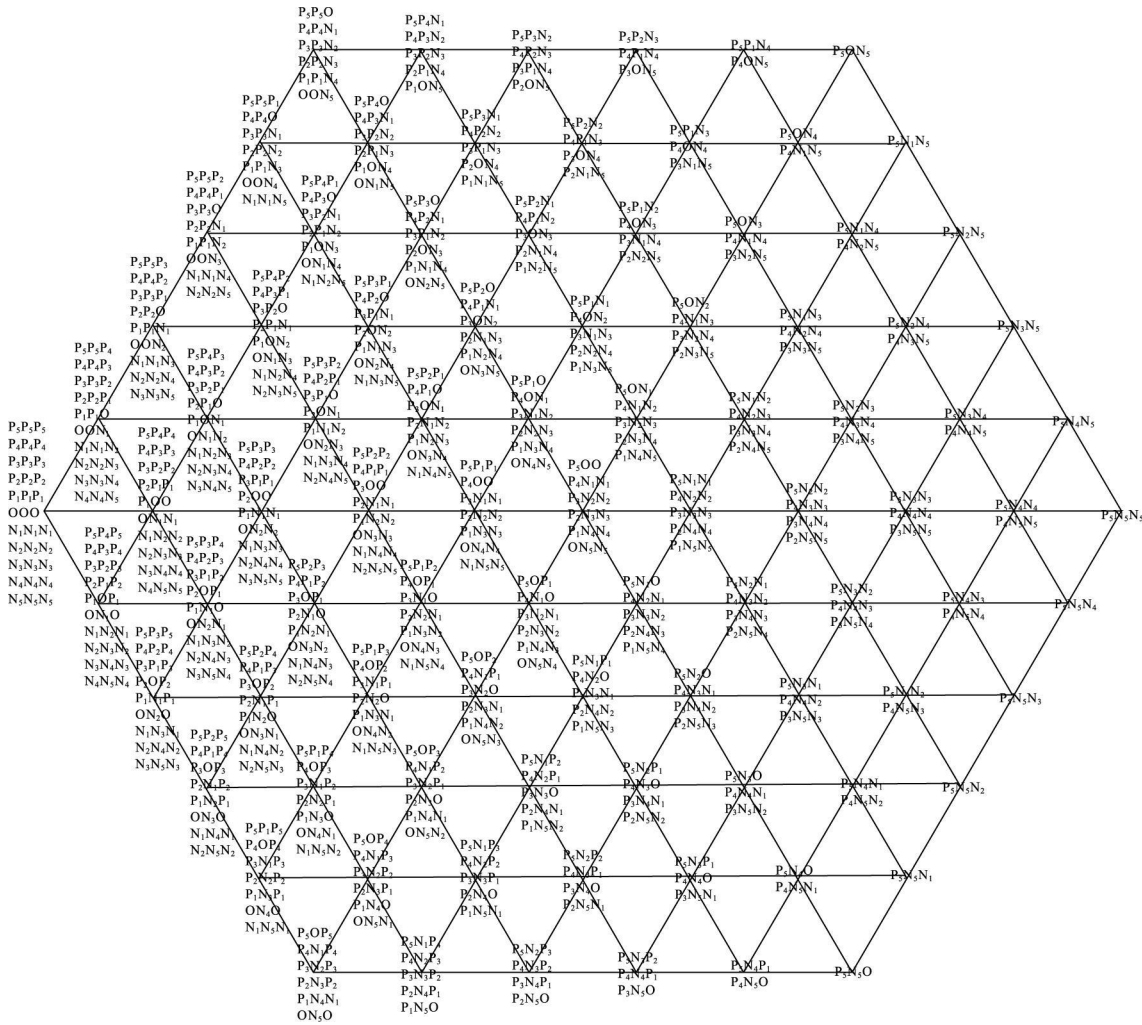FIGURE 4: Mapping of $V_{ref6}$ in outer 2L hexagon.

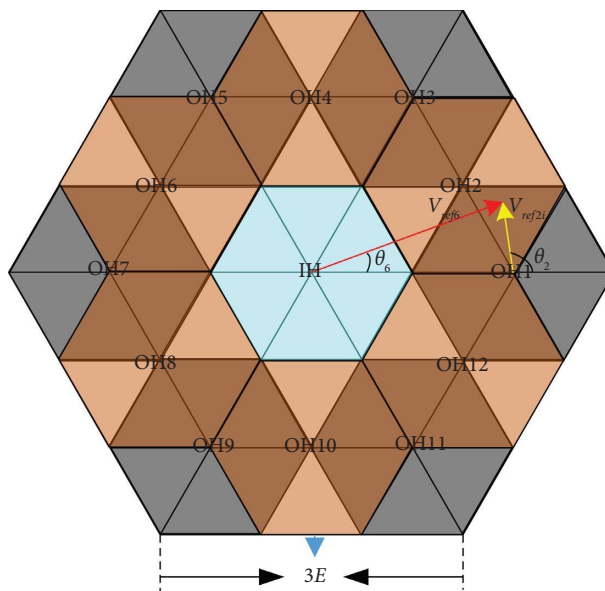Figure 5: Switching states of 6L hexagon-I.



Figure 6: Disintegration of 4L SVD to 2L hexagons.

TABLE 5: Selection of 2L hexagons from 4L SVD and mapping of $V_{ref2}$ from $V_{ref4}$.

| Hexagon No | Magnitude of $V_{ref4}$ | Range of $\theta$ | $V_{2\alpha i}$ | $V_{2\beta i}$ |
|---|---|---|---|---|
| IH | $\leq E$ | — | — | — |
| OH1 | | 340° to 20° | $V_{4\alpha} - 2E$ | $V_{4\beta}$ |
| OH2 | | 20° to 40° | $V_{4\alpha} - 1.73E \cos(\pi/6)$ | $V_{4\beta} - 1.73E \sin(\pi/6)$ |
| OH3 | | 40° to 80° | $V_{4\alpha} - 2E \cos(2\pi/6)$ | $V_{4\beta} - 2E \sin(2\pi/6)$ |
| OH4 | | 80° to 100° | $V_{4\alpha}$ | $V_{4\beta} - 1.73E$ |
| OH5 | | 100° to 140° | $V_{4\alpha} - 2E \cos(4\pi/6)$ | $V_{4\beta} - 2E \sin(4\pi/6)$ |
| OH6 | $> E$ | 140° to 160° | $V_{4\alpha} - 1.73E\cos(5\pi/6)$ | $V_{4\beta} - 1.73E\sin(5\pi/6)$ |
| OH7 | | 160° to 200° | $V_{4\alpha} + 2E$ | $V_{4\beta}$ |
| OH8 | | 200° to 220° | $V_{4\alpha} - 1.73E\cos(7\pi/6)$ | $V_{4\beta} - 1.73E \sin(7\pi/6)$ |
| OH9 | | 220° to 260° | $V_{4\alpha} - 2E\cos(8\pi/6)$ | $V_{4\beta} - 2E \sin(8\pi/6)$ |
| OH10 | | 260° to 280° | $V_{4\alpha} - 1.73E\cos(9\pi/6)$ | $V_{4\beta} - 1.73E\sin(9\pi/6)$ |
| OH11 | | 280° to 320° | $V_{4\alpha} - 2E\cos(10\pi/6)$ | $V_{4\beta} - 2E \sin(10\pi/6)$ |
| OH12 | | 320° to 340° | $V_{4\alpha} - 1.73E\cos(11\pi/6)$ | $V_{4\beta} - 1.73E \sin(11\pi/6)$ |
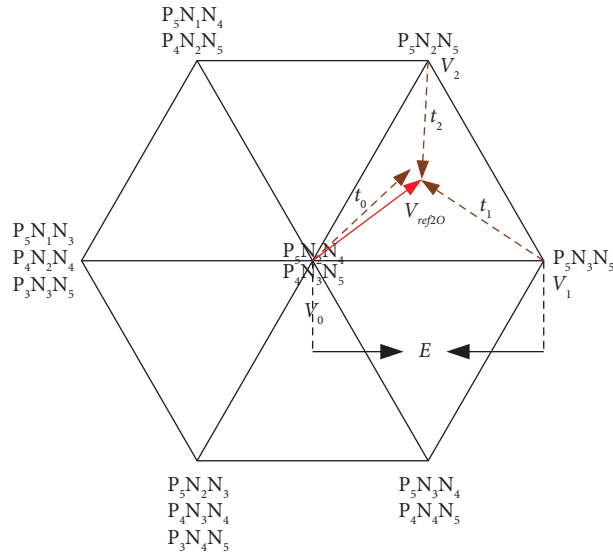


FIGURE 7: Outer 2L hexagon-3 with switching states.

Here $M$ stands for modulation index, and it is given as follows:

$$M = \frac{\sqrt{3}V_{ref}}{E}. \tag{5}$$

Here, $M$ value ranges from 0 to unity. Designing the switching time sequence using a single zero switching state and 2 active switching states is another crucial step. This technique switches between seven segments. When changing from one switching instant to another instant, there should be no more than individual leg change in the switching sequence.

The seven instants of segment switching through switching times sector-I is chosen if the $V_{ref2O}$ vector is present.

$$(P_4N_3N_5) * \frac{T_0}{4}, (P_5N_3N_5) * \frac{T_1}{2}, (P_5N_2N_5) * \frac{T_2}{2}, (P_5N_2N_4) * \frac{T_0}{2}, (P_5N_3N_5) * \frac{T_1}{2}, (P_5N_2N_5) * \frac{T_2}{2}, (P_3N_4N_4) * \frac{T_0}{4}. \tag{6}$$

Furthermore, if the $V_{ref2}$ vector lies within, sector-IV is chosen as

$$(P_4N_3N_5) * \frac{T_0}{4}, (P_4N_3N_4) * \frac{T_1}{2}, (P_4N_2N_4) * \frac{T_2}{2}, (P_4N_3N_5) * \frac{T_0}{2}, (P_4N_3N_4) * \frac{T_1}{2}, (P_4N_2N_4) * \frac{T_2}{2}, (P_4N_3N_5) * \frac{T_0}{4}. \tag{7}$$

## 3. Proposed SVPWM-II Technique

For the SVPWMM of a nine-level inverter, the SVPWM-II scheme is also suggested. The number of 2L hexagons required to realise the eleven-level SVD is once again reduced by this scheme. As in the SVPWM-II technique, the 9L SVD is first resolved into six 4L hexagons in this scheme, and each of those is then divided into thirty-one 2L hexagons. As a result, for eleven-level SVM, the number of 2L hexagons to be considered drops from 222 to 186. The largest circle that is encircled by a hexagon has a radius that corresponds to the value of $M$ is 1.0. Figure 8 displays the 6L SVD with a circle. Only 18 of the outer hexagons in the eleven-level SVD's darkly shaded region are excluded, even for the unity modulation index ($M$).

As a result, for the SVM of an eleven-level inverter, the number of 2L hexagons considered is diminished to 186. Consider selecting the adjacent outer hexagon depends on $V_{ref2O}$ and angle $\theta_2$ if the $V_{ref}$ vector is in the dark-shaded area. According to the value of $V_{ref6}$ and angle $\theta_6$, the outer eighteen 2L hexagons of a 6L SVD are chosen as shown in Table 6, and the inner 2L hexagons are chosen using the same criteria as in the SVPWM-I method (Table 5). When the $M$ value is greater than 0.91, the THD is slightly increased, which results in a reduction in complexity compared to the SVPWM-I scheme. Both SVPWM-I and SVPWM-II produce the same results if the value of $M$ is less than or equal to 0.92.

## 4. Simulation Results

Using the MATLAB/SIMULINK software tool, the SVPWM-I and SVPWM-II schemes are both applied to an 11L asymmetric CHB MLI. The three-phase CHB MLI is associated to a three-phase RL-load that is star connected. The inverter neutral and load neutral are not isolated to each other. With the SPWM and THIPWM techniques, simulation results for the presented two SVPWM schemes are validated. IPD multicarrier scheme is employed in the SPWM method. In the SPWM technique, the carrier frequency is 2.5 KHz. Table 7 displays the simulation's input parameters.

Figure 9 displays the output phase voltage of an 11L inverter for various control schemes (SPWM, THIPWM, SVPWM-I, and SVPWM-II) when the dynamic variation of $M$ is from 0.2 to 1.0. Figure 10 displays the eleven-level inverter AC line voltage waveform for various modulation indices ranging from 0.2 to unity.

Table 8 displays the line voltage THD for various values of $M$ and modulation techniques. The RMS voltage for various modulation strategies at various values of $M$ is shown in Table 9. Figure 11 depicts the 11L inverter load current waveforms at dynamic value of $M$ for various modulation techniques by using SPWM, THIPWM, SVPWM-I, and SVPWM-II schemes. The load voltage along with the load current for 1.0 as $M$ value is shown in Figure 12 by using the SVPWM-I technique. The three-phase line voltage of an 11L inverter for various control schemes (SPWM, THIPWM, SVPWM-I, and SVPWM-II) when the
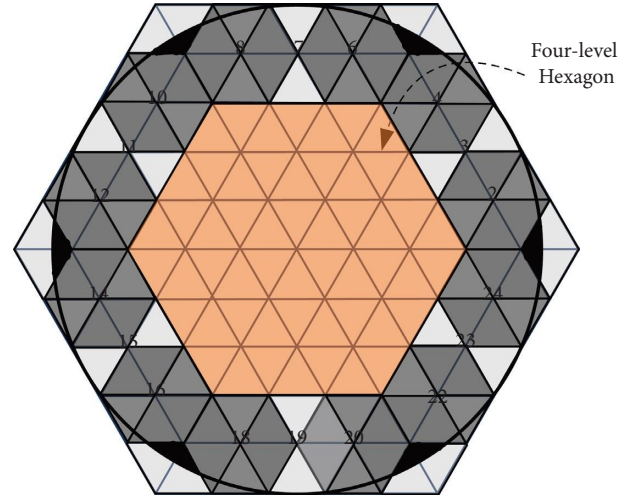


Figure 8: 6L SVD with inscribed circle at 1.0 $M$.

Table 6: Selection of 2L hexagons from 6L SVD.

| Hexagon No | Range of $\theta$ |
| --- | --- |
| OH2 | 0° to 24° |
| OH3 | 24° to 36° |
| OH4 | 36° to 60° |
| OH6 | 60° to 84° |
| OH7 | 84° to 96° |
| OH8 | 96° to 120° |
| OH10 | 120° to 144° |
| OH11 | 144° to 156° |
| OH12 | 156° to 180° |
| OH14 | 180° to 204° |
| OH15 | 204° to 216° |
| OH16 | 216° to 240° |
| OH18 | 240° to 264° |
| OH19 | 264° to 276° |
| OH20 | 276° to 300° |
| OH22 | 300° to 324° |
| OH23 | 324° to 336° |
| OH24 | 336° to 360° |

Table 7: Simulation parameters.

| Parameter | Value |
| --- | --- |
| Output frequency | 50 Hz |
| DC source ($E$) | 100 V |
| Inductive load | 110 mH/$ph$ |
| Resistive load | 100 $\Omega$/$ph$ |
| Sampling time ($T_S$) | 2100 s |

dynamic variation of $M$ from 0.2 to 1.0 is shown in Figure 13. The load voltage waveform for the dynamic variation of $M$ from 0.2 to 1.0 is shown in Figure 14 by using SVPWM-I and SVPWM-II techniques. The microscopic view of the 11L inverter line voltage waveform for 1.0 as $M$ value by using SVPWM-I and SVPWM-II is shown in Figure 15. From Figure 15, it is clear that the line voltage waveform has 21 levels. Table 10 shows the 11L inverter line output voltage
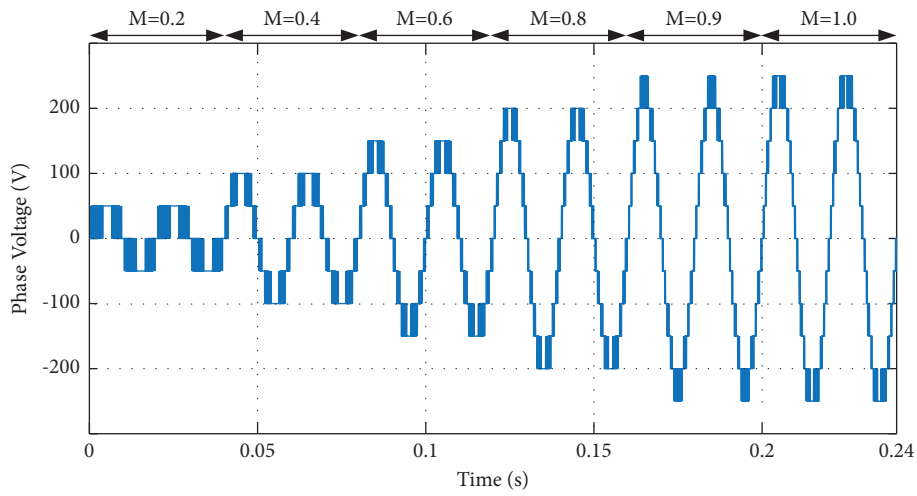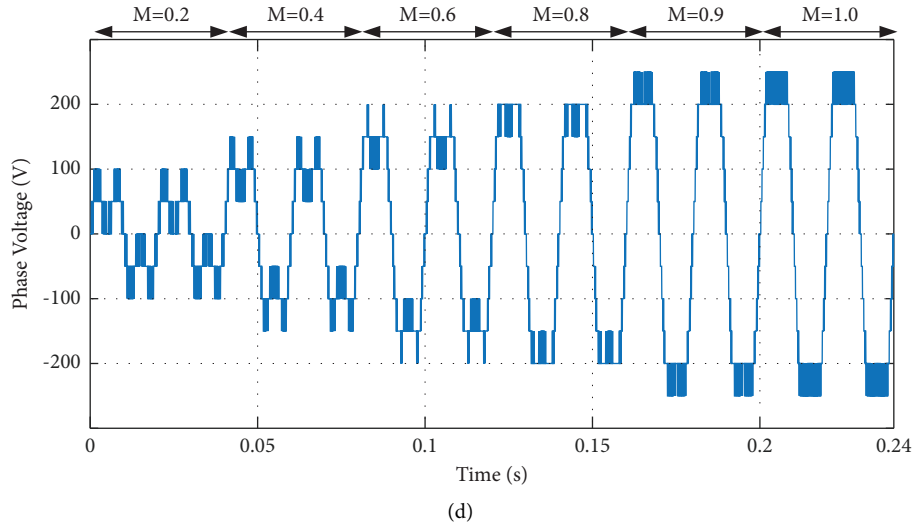
(a)
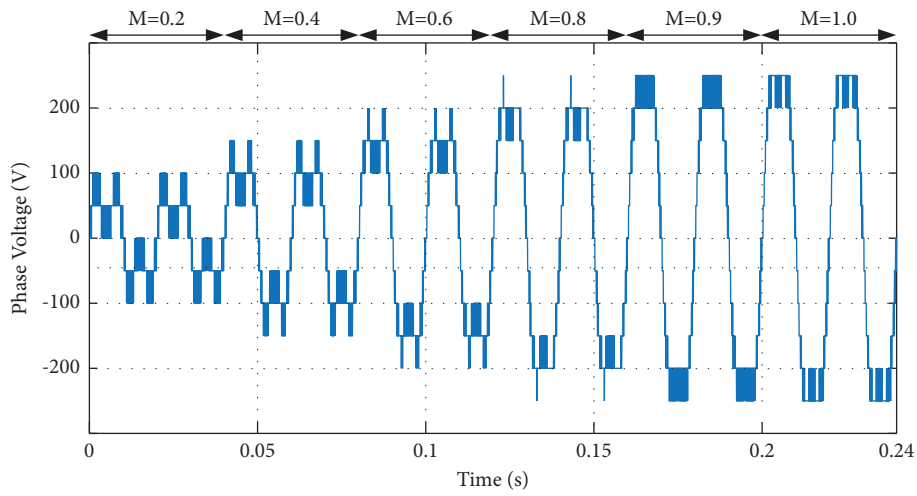
(b)
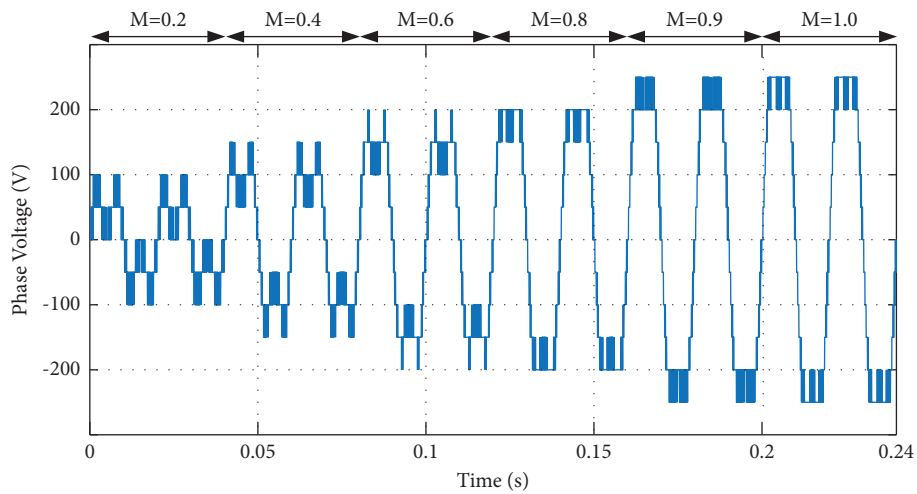
(c)

Figure 9: Continued.

(d)

FIGURE 9: 11L CHB inverter phase output voltage for dynamic values of M. (a) SPWM. (b) THIPWM. (c) SVPWM-I. (d) SVPWM-II.
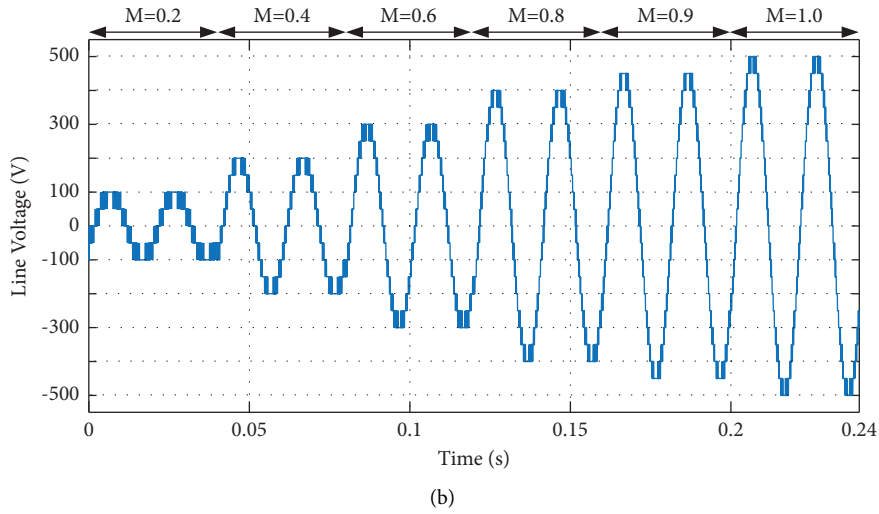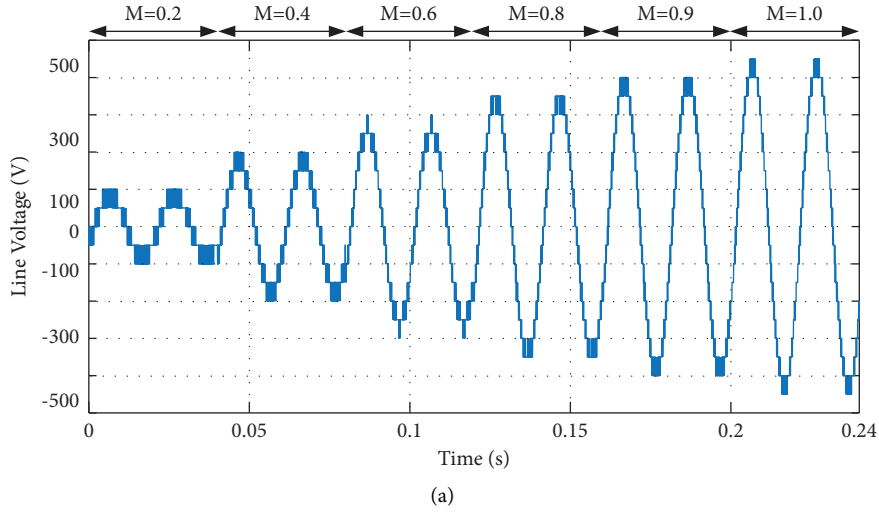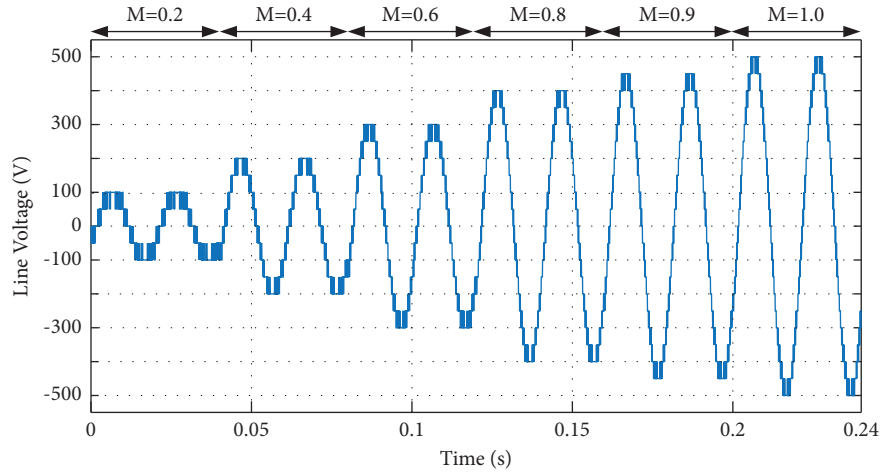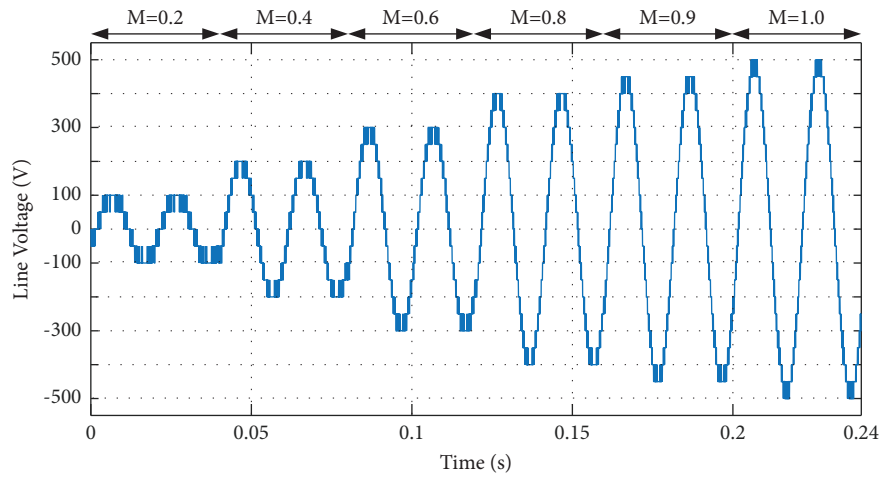


(a)



(b)

FIGURE 10: Continued.

(c)



(d)

FIGURE 10: 11L CHB inverter line voltage for dynamic values of *M*. (a) SPWM. (b) THIPWM. (c) SVPWM-I. (d) SVPWM-II.

TABLE 8: Line voltage THD at various values of *M*.

| M value | Line voltage THD (%) | | | |
|---|---|---|---|---|
| | SPWM | THIPWM | SVPWM-I | SVPWM-II |
| 1.0 | 6.75 | 6.69 | 6.06 | 6.12 |
| 0.9 | 7.88 | 8.06 | 6.17 | 6.17 |
| 0.8 | 8.23 | 8.82 | 6.78 | 6.78 |
| 0.6 | 10.4 | 9.21 | 8.65 | 8.65 |
| 0.4 | 17.4 | 12.69 | 12.48 | 12.48 |
| 0.2 | 33.22 | 27.14 | 25.55 | 25.55 |

TABLE 9: AC line voltage value at various values of *M*.

| M value | AC line voltage (V) | | | |
|---|---|---|---|---|
| | SPWM | THIPWM | SVPWM-I | SVPWM-II |
| 1.0 | 305.4 | 334.3 | 353.1 | 343.2 |
| 0.9 | 274.7 | 315.4 | 317.8 | 317.8 |
| 0.8 | 245 | 283.7 | 284.8 | 284.8 |
| 0.6 | 183.2 | 212.4 | 212.5 | 212.5 |
| 0.4 | 121.9 | 141 | 142.6 | 142.6 |
| 0.2 | 62.02 | 70.17 | 71.52 | 71.52 |

TABLE 10: Line output voltage levels for different modulation indices.

| Modulation index | Line output voltage levels |
|---|---|
| 0.1 | 3 |
| 0.2 | 5 |
| 0.3 | 7 |
| 0.4 | 9 |
| 0.5 | 11 |
| 0.6 | 13 |
| 0.7 | 15 |
| 0.8 | 17 |
| 0.9 | 19 |
| 1.0 | 21 |

levels for different modulation indices. The THD is calculated in MATLAB by considering the harmonic order of infinity; i.e., all the frequency components are considered in FFT analysis. The line voltage FFT at *M* value of 1.0 by using SVPWM-I and SVPWM-II is shown in Figure 16. Similarly, the load current harmonic spectra at *M* = 1.0 by using

TABLE 11: Switching losses for three different modulation schemes.

| Modulation scheme | Switching losses (W) |
| --- | --- |
| SPWM | 8.57 |
| SVPWM-I | 6.89 |
| SVPWM-II | 7.56 |
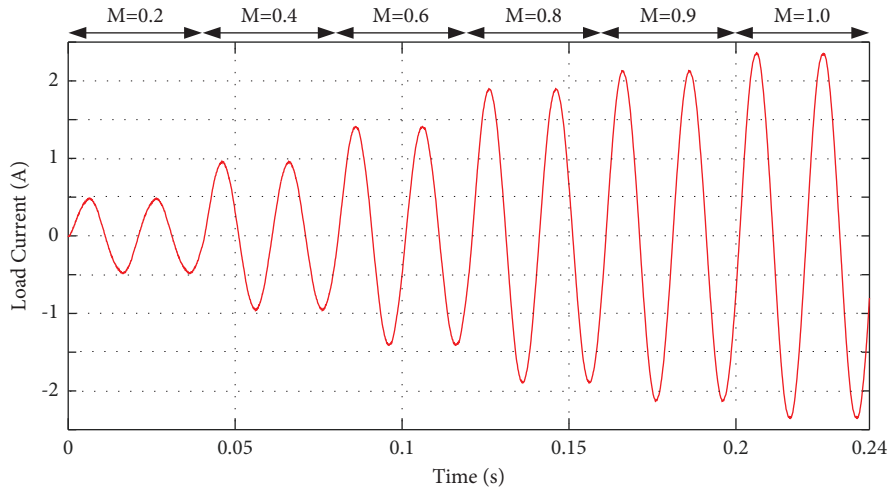

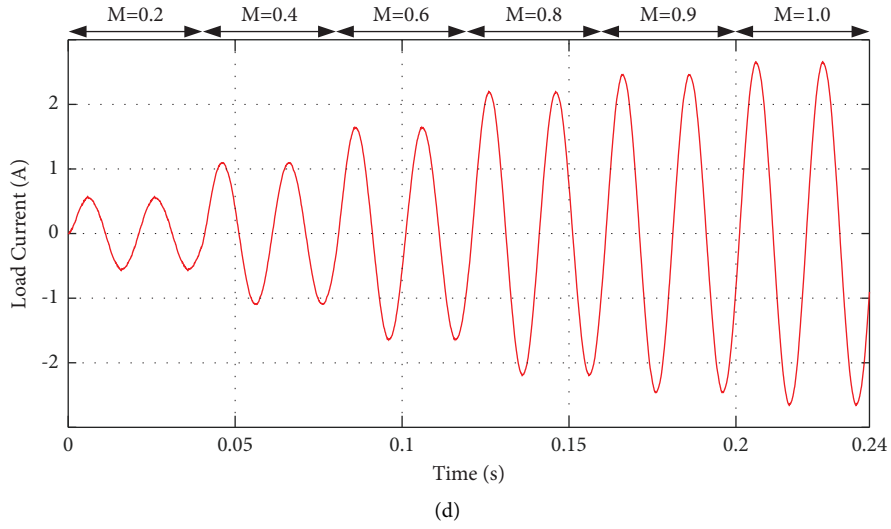
(a)
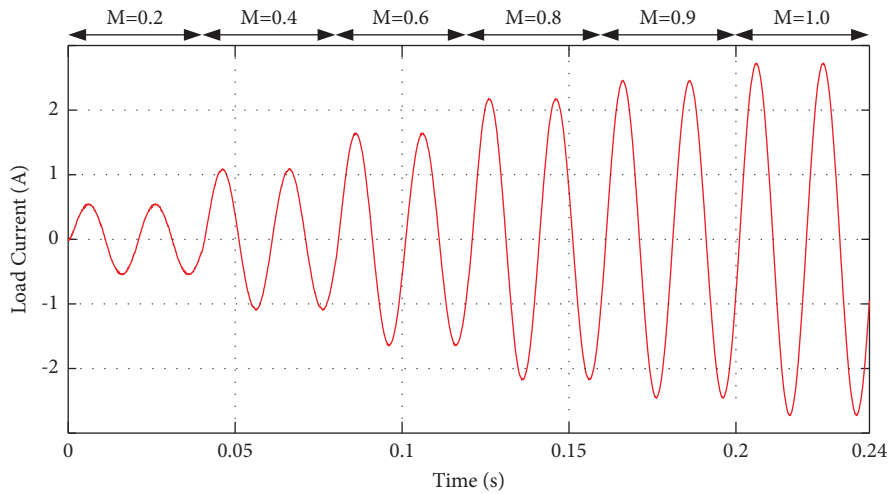


(b)
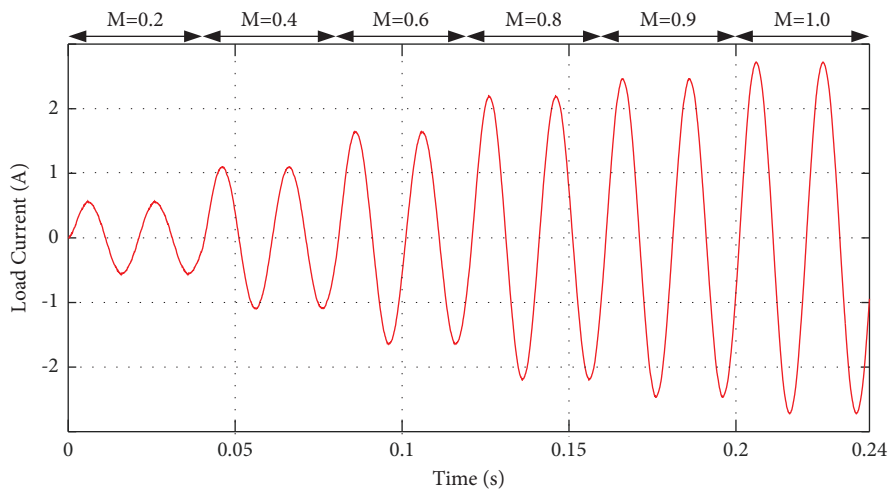


(c)

FIGURE 11: Continued.

(d)

FIGURE 11: 11L CHB inverter load current for dynamic values of *M*. (a) SPWM. (b) THIPWM. (c) SVPWM-I. (d) SVPWM-II.
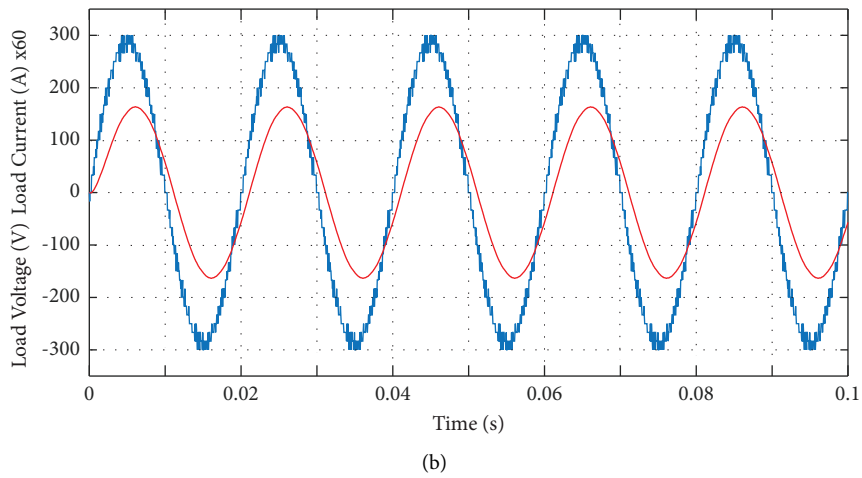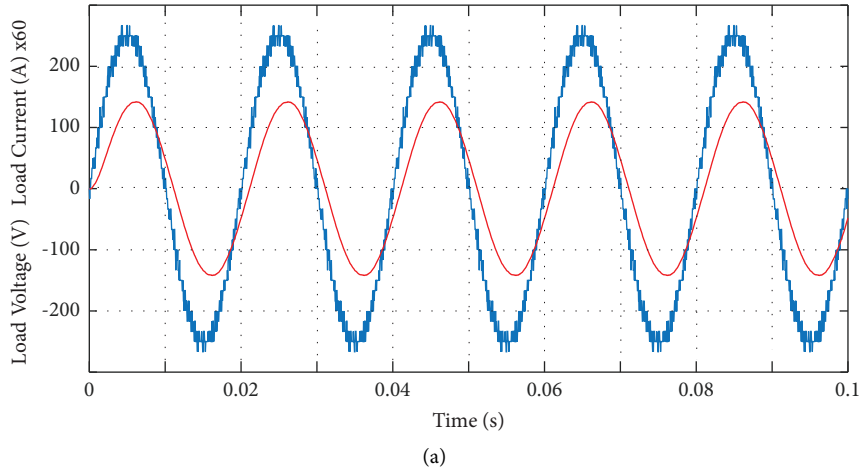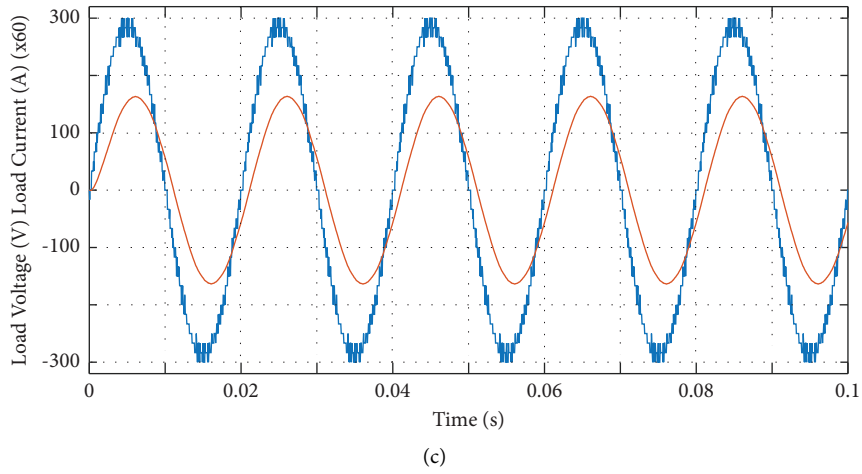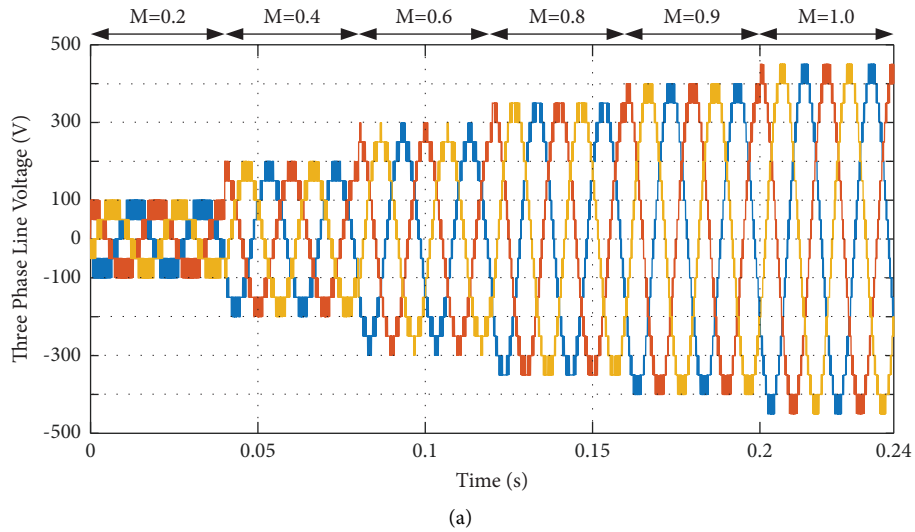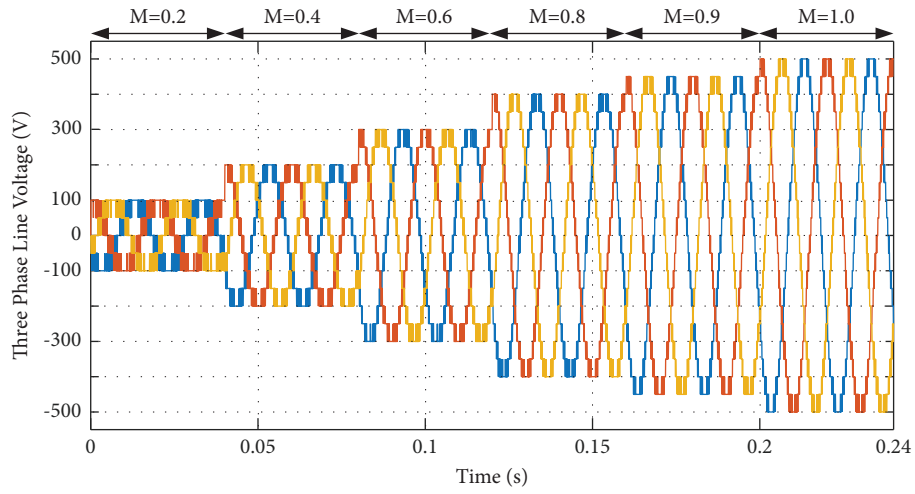


(a)



(b)

FIGURE 12: Continued.

(c)

FIGURE 12: 11L CHB inverter load voltage and current at $M = 1.0$. (a) SPWM. (b) THIPWM. (c) SVPWM-I.
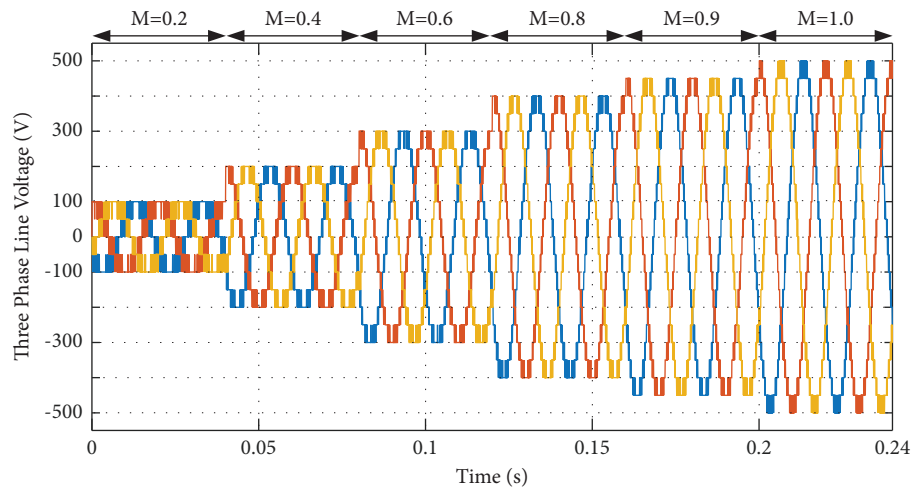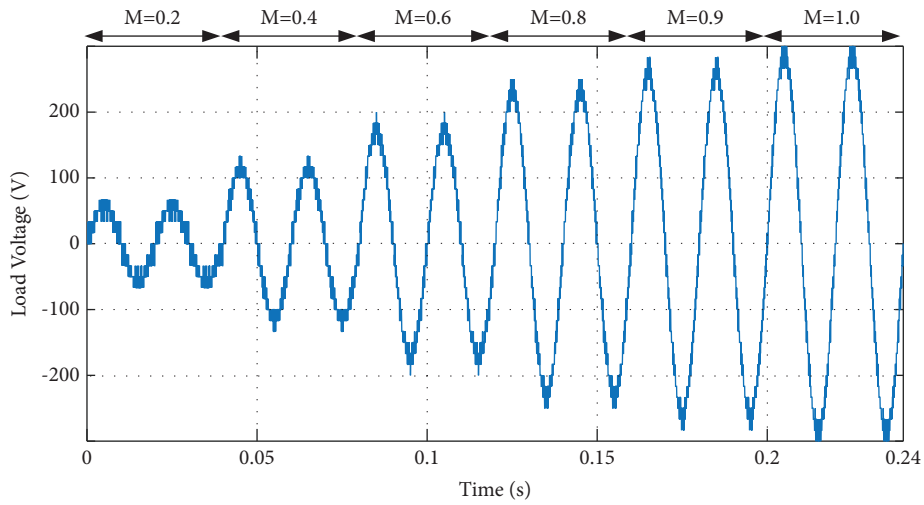


(a)



(b)
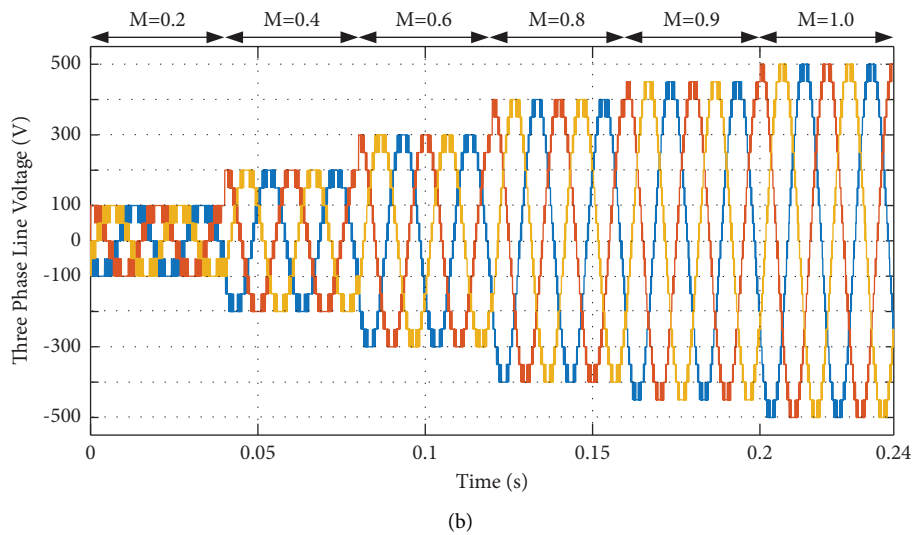
FIGURE 13: Continued.

(c)



(d)

FIGURE 13: 11L CHB inverter three phase line voltage for dynamic values of *M*. (a) SPWM. (b) THIPWM. (c) SVPWM-I. (d) SVPWM-II.
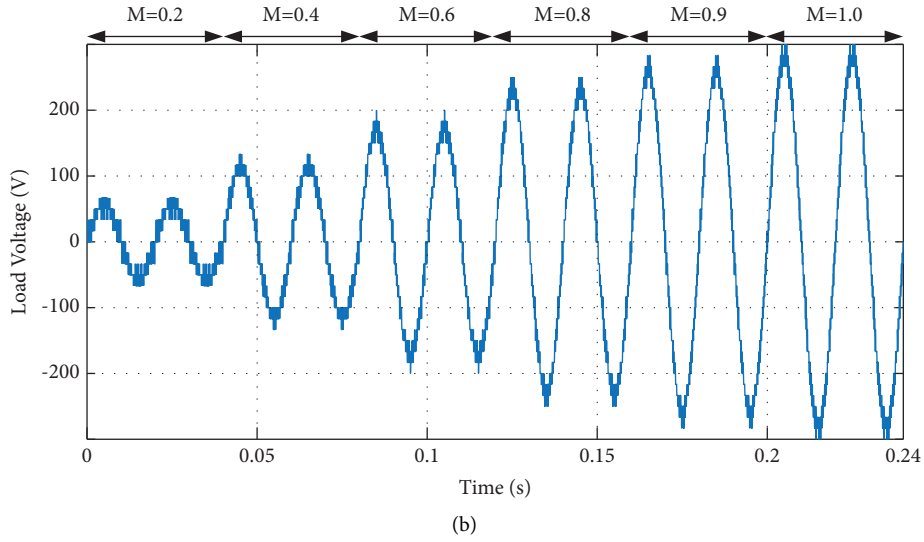


(a)

FIGURE 14: Continued.

(b)

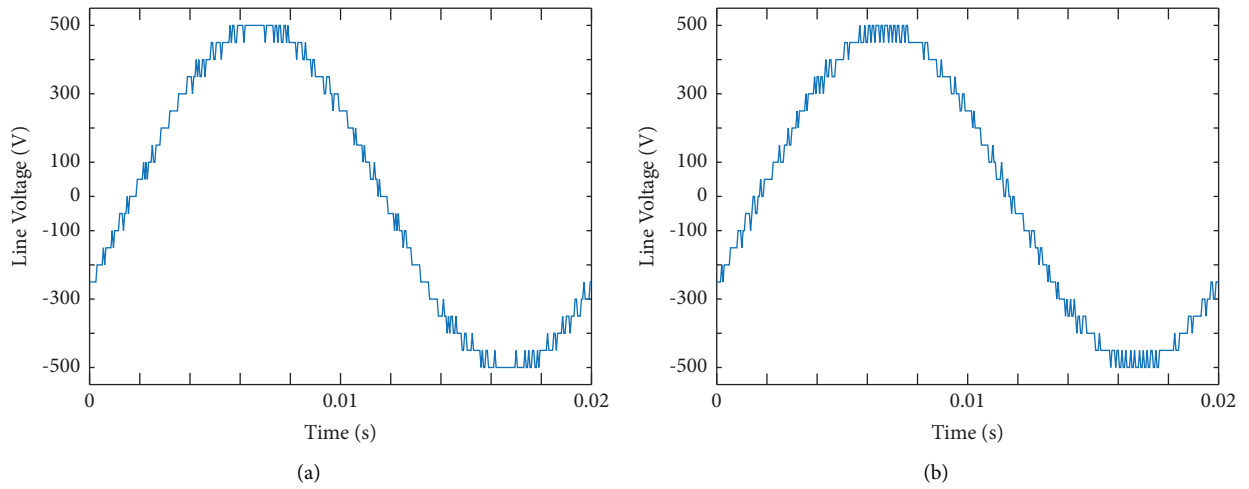FIGURE 14: 11L CHB inverter load voltage for dynamic values of *M*. (a) SVPWM-I. (b) SVPWM-II.



(a)

(b)

FIGURE 15: Microscopic view of line voltage at *M* = 1.0. (a) SVPWM-I. (b) SVPWM-II.



Fundamental (50 Hz) = 353.1 V *rms*, *THD*= 6.06%

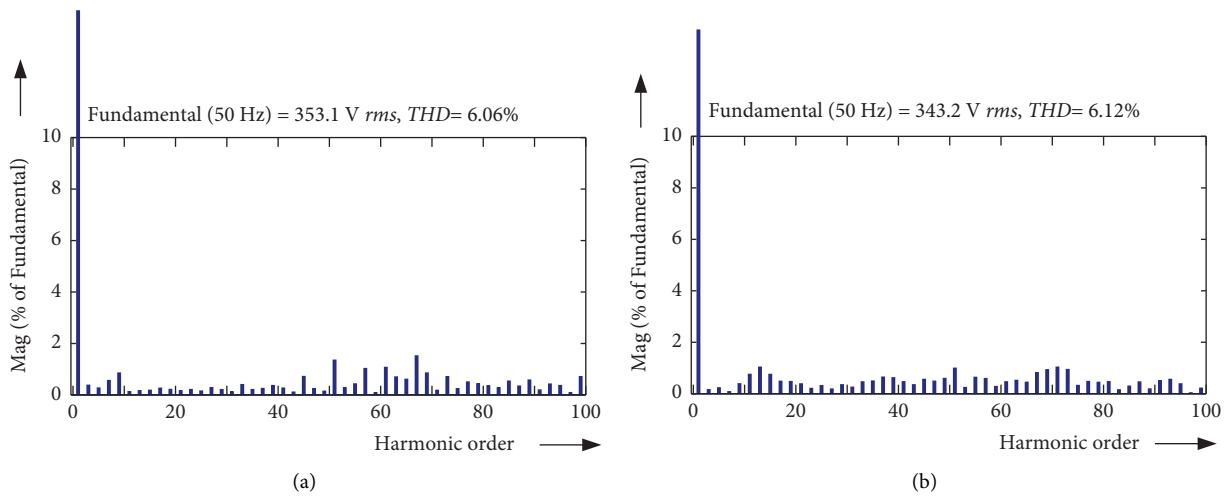Fundamental (50 Hz) = 343.2 V *rms*, *THD*= 6.12%

(a)

(b)

FIGURE 16: FFT spectra of line voltage at *M* = 1.0. (a) SVPWM-I. (b) SVPWM-II.
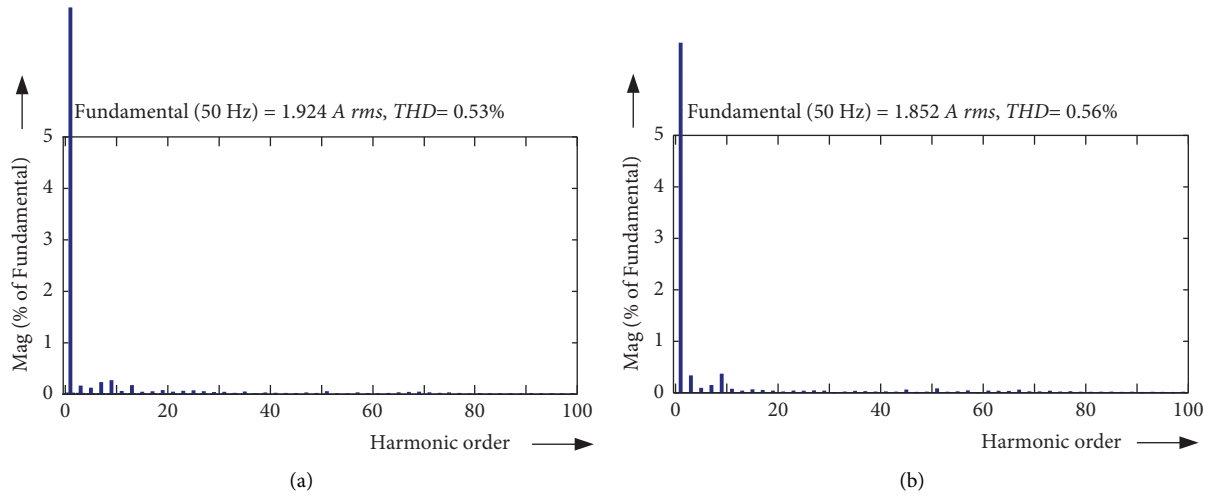
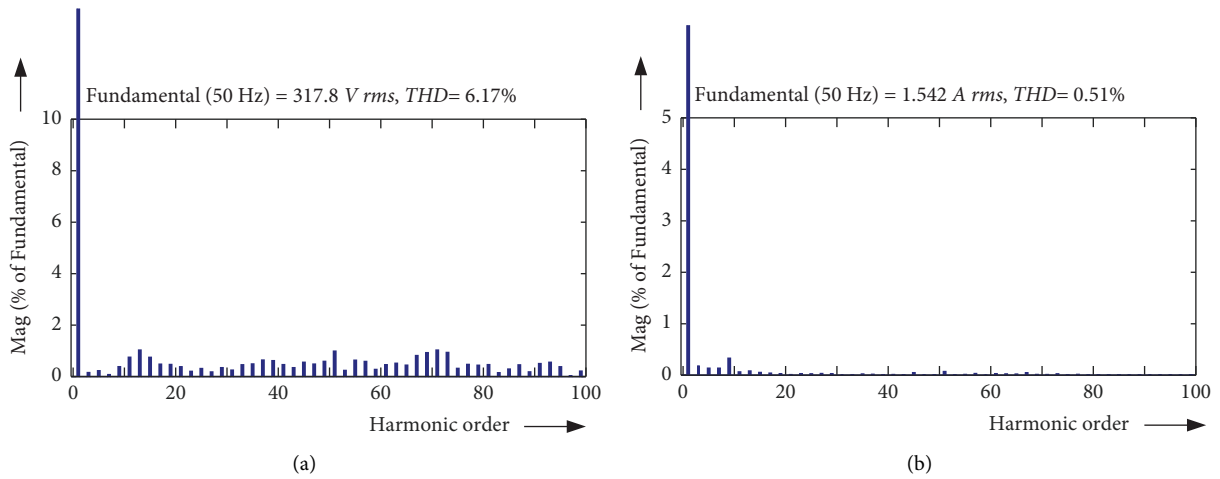Figure 17: FFT spectra of load current at $M = 1.0$. (a) SVPWM-I. (b) SVPWM-II.



Figure 18: FFT spectra at $M = 0.9$ by using SVPWM-I technique. (a) Line Voltage. (b) Load Current.
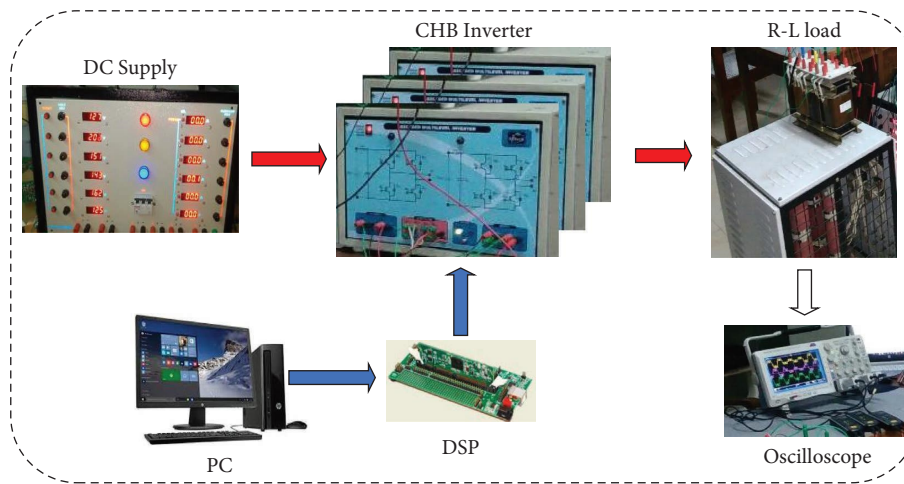


Figure 19: Hardware prototype.

FIGURE 20: Experimental 11L CHB inverter phase voltage for dynamic values of $M$. (a) SVPWM-I. (b) SVPWM-II.
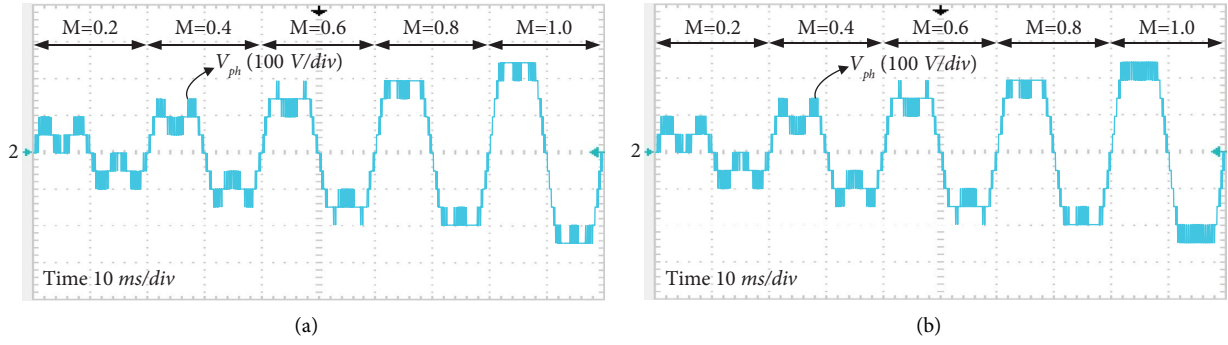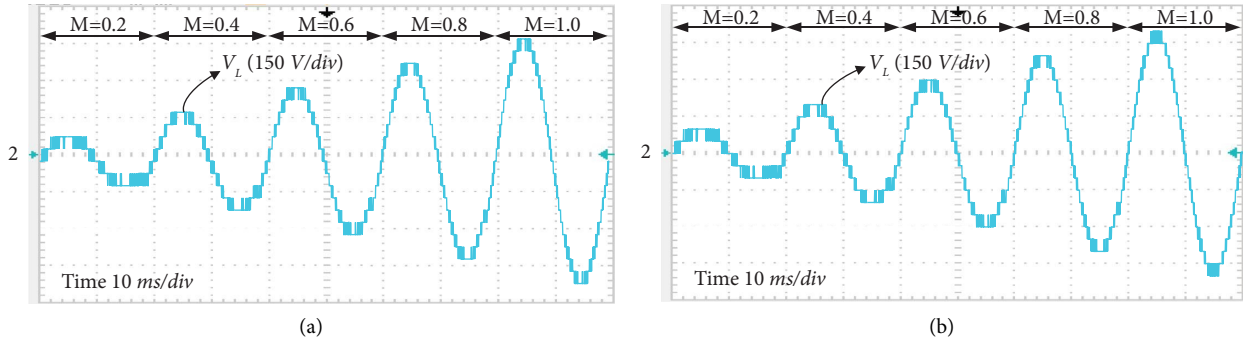


FIGURE 21: Experimental 11L CHB inverter line voltage for dynamic values of $M$. (a) SVPWM-I. (b) SVPWM-II.
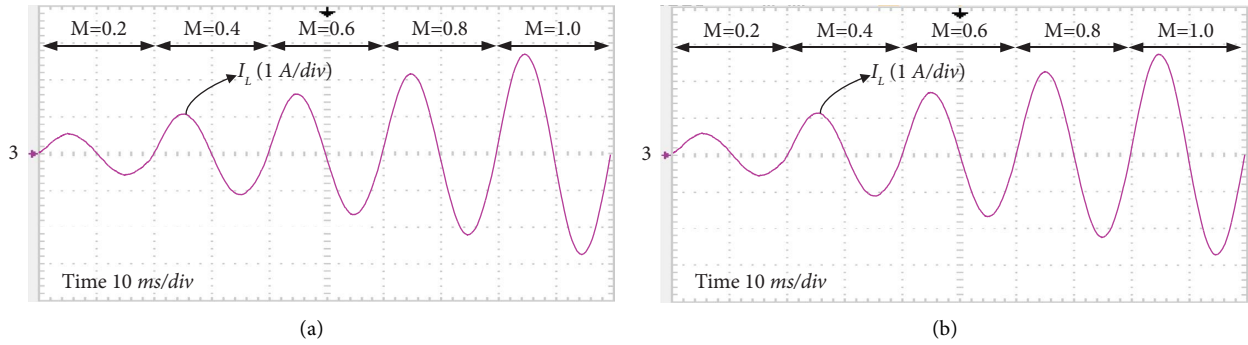


FIGURE 22: Experimental 11L CHB inverter load current for dynamic values of $M$. (a) SVPWM-I. (b) SVPWM-II.
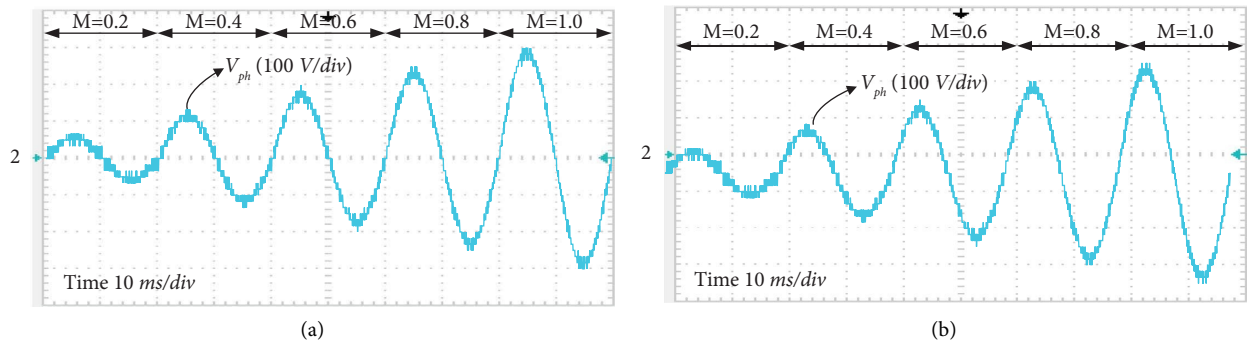


FIGURE 23: Experimental 11L CHB inverter load voltage for dynamic values of $M$. (a) SVPWM-I. (b) SVPWM-II.
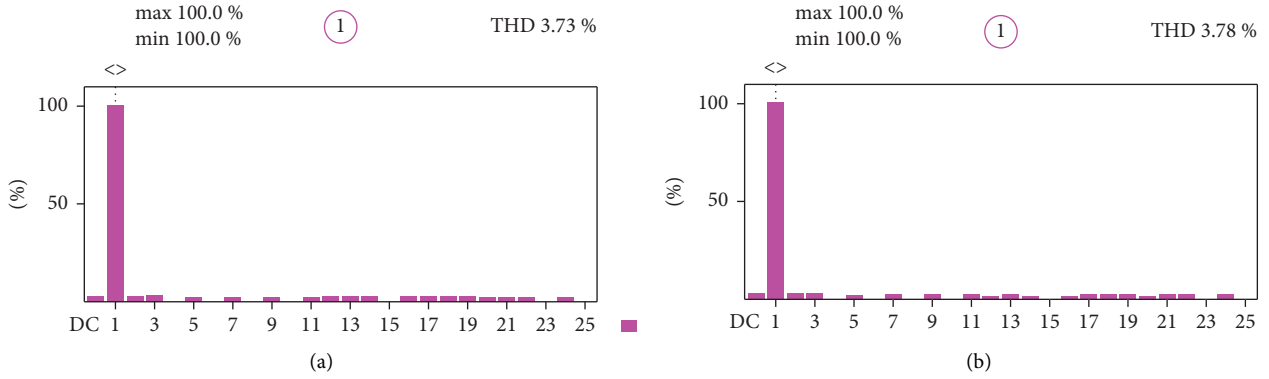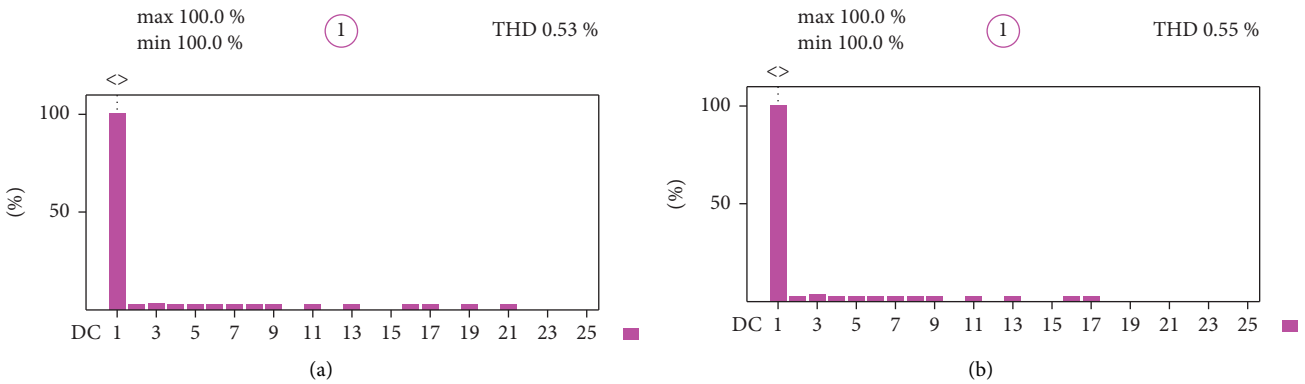
FIGURE 24: Experimental FFT of line voltage at $M = 1.0$. (a) SVPWM-I. (b) SVPWM-II.



FIGURE 25: Experimental FFT of load current at $M = 1.0$. (a) SVPWM-I. (b) SVPWM-II.

TABLE 12: Experimental line voltage THD for different modulation indices.

| Modulation index ($M$) | Harmonic distortion (%) | |
| --- | --- | --- |
| | SVPWM-I | SVPWM-II |
| 1.0 | 3.73 | 3.78 |
| 0.9 | 4.07 | 4.07 |
| 0.8 | 4.19 | 4.19 |
| 0.6 | 6.58 | 6.58 |
| 0.4 | 8.65 | 8.65 |
| 0.2 | 16.64 | 16.64 |

SVPWM-I and SVPWM-II is shown in Figure 17. The line voltage FFT and load current FFT at $M$ value of 0.9 by using SVPWM-I are shown in Figure 18. The two SVPWM techniques that have been suggested perform well at various modulation indices and are comparable to traditional SPWM and THIPWM schemes. Switching losses are computed for various modulation schemes by adding IGBT parameters from the datasheet [34] into the IGBT thermal model. At $M = 1.0$, Table 11 displays the switching losses for SPWM, MSVPWM, and FMSVPWM approaches. Because the switching sequence pattern is built in such a manner that there is only one leg change from one switching instant to the next, the switching frequency is reduced, which results in a decrease in switching losses. Table 11 shows that the suggested SVPWM strategies yield smaller switching losses than the SPWM method.

## 5. Hardware Results

Figure 19 depicts the practical setup for a $3 - \theta$, eleven-level CHB MLI to verify the suggested two SVPWM schemes. The same simulation's parameters were taken out for analysis. Texas DSP processor is used to implement the suggested SVPWM techniques.

Figures 20(a) and 20(b) respectively show the eleven-level output phase voltage at different modulation indices (0.2, 0.4, 0.6, 0.8, and 1.0) by using the SVPWM-I and SVPWM-II technique, respectively. The eleven-level output line voltage by different $M$ values using the SVPWM-I and SVPWM-II technique is shown in Figures 21(a) and 21(b) correspondingly. Figures 22(a) and 22(b) show the load current waveforms at dynamic modulation indices by using the SVPWM-I and SVPWM-II techniques correspondingly. Similarly, the load voltage waveforms at dynamic modulation indices by using the SVPWM-I and SVPWM-II techniques are shown in Figures 23(a) and 23(b) correspondingly.

Figures 24(a) and 24(b) display the frequency spectrum for the 11L phase voltage at 1.0 as $M$ by using the SVPWM-I and SVPWM-II techniques. Whereas the frequency

spectrum for the load current at $M = 1.0$ by using the SVPWM-I and SVPWM-II techniques is shown in Figures 25(a) and 25(b). Table 12 shows the experimental line voltage THD for different modulation indices for both SVPWM techniques. It is seen that the experimental THD value in lower when compared to THD obtained in simulation because the harmonic order of 100 is considered in digital storage oscilloscopes when calculating frequency spectra of any quantity, whereas during the simulation the entire frequency harmonic orders are contemplated in FFT analysis.

## 6. Conclusion

By reducing the number of 2L hexagons that must have been considered from 1331 to 222 in order to realise the space vector PWM of the 11L inverter, the proposed SVPWM-I schemes significantly diminish the mathematical burden and the system memory requirements. This method can be generalised for any inverter level and is applicable to any inverter topology. Also presented is the SVPWM-II scheme, which diminishes the number of 2L hexagons so as to be considered to realise a nine-level SVM from 222 to 186. Eleven-level CHB inverter simulation analyses at various modulation indices are compared through SPWM and THIPWM techniques. Reduced harmonic distortion and greater DC bus utilisation are provided by the presented SVPWM schemes. To support the suggested SVPWM control strategies, experimental results are also provided. Thus, by simplifying the process of realising SVPWM for MLIS, the suggested two SVPWM-I and SVPWM-II techniques yield satisfactory results.

## Data Availability

No underlying data was collected or produced in this study.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

## Acknowledgments

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