

A thorough investigation of the switching dynamics of TiN/Ti/10 nm-HfO₂/W resistive memories

D. Maldonado^a, G. Vinuesa^{b,*}, S. Aldana^a, F.L. Aguirre^c, A. Cantudo^a, H. García^b, M.B. González^d, F. Jiménez-Molinos^a, F. Campabadal^d, E. Miranda^c, S. Dueñas^b, H. Castán^b, J. B. Roldán^a

^a Departamento de Electrónica y Tecnología de Computadores, Universidad de Granada, Avd. Fuentenueva S/n, 18071, Granada, Spain

^b Departamento de Electrónica, Universidad de Valladolid, Paseo de Belén 15, 47011, Valladolid, Spain

^c Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona, Edifici Q, 08193, Cerdanyola del Vallès, Spain

^d Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Carrer dels Til·lers s/n, Campus UAB, 08193, Cerdanyola del Vallès, Spain

ARTICLE INFO

Keywords:

Resistive switching
RRAM
Operation dynamics
Characterization
Kinetic Monte Carlo
Compact modeling

ABSTRACT

The switching dynamics of TiN/Ti/HfO₂/W-based resistive memories is investigated. The analysis consisted in the systematic application of voltage sweeps with different ramp rates and temperatures. The obtained results give clear insight into the role played by transient and thermal effects on the device operation. Both kinetic Monte Carlo simulations and a compact modeling approach based on the Dynamic Memdiode Model are considered in this work with the aim of assessing, in terms of their respective scopes, the nature of the physical processes that characterize the formation and rupture of the filamentary conducting channel spanning the oxide film. As a result of this study, a better understanding of the different facets of the resistive switching dynamics is achieved. It is shown that the temperature and, mainly, the applied electric field, control the switching mechanism of our devices. The Dynamic Memdiode Model, being a behavioral analytic approach, is shown to be particularly suitable for reproducing the conduction characteristics of our devices using a single set of parameters for the different operation regimes.

1. Introduction

Among the wide variety of memristive devices, those based on the generation and rupture of a tiny filament spanning across the insulating layer of a MIM or MIS structure are gaining momentum both at academia and industrial research centers [1]. These devices are also referred to as Resistive Random-Access Memories (RRAMs) or, for short, resistive memories. Their operational principle relies on the alternate switching of the dielectric film resistance between two remarkably different values (the low resistance state, LRS, and the high resistance state, HRS). If no signal is applied, the device resistance does not change so that this kind of memory can be used for non-volatile information storage. In particular, in the industrial context, different companies offer resistive memories among their products, such as TSMC for its 40 nm [2], 28 nm [3] and 22 nm [4] nodes, as well as INTEL for its 22 nm [5] node. RRAMs allow building memory cells exhibiting multi-level resistance states, low power consumption, high endurance (above $>10^{10}$

cycles, high-speed operation (<10 ns), and CMOS technology compatibility [1,6–9].

From the analog viewpoint and within the neuromorphic engineering landscape, resistive memories offer in-memory computing capabilities that facilitate novel computing paradigms. In such a case, results are generated and stored on-site without shuffling data in and out, therefore avoiding the drawbacks associated with the so-called von Neumann's bottleneck [10]. This remarkable feature in combination with the improvements associated with the reduction of the memory wall (i.e., the steadily growing performance gap between the different types of memory and the microprocessors) [11] allow boosting the development of artificial intelligence techniques by supplying new hardware platforms to cope with the needs of machine learning, Internet of Things, 5G data management, etc. The role of memristors within this new computing paradigm [12–20] is essential to reduce computation time and energy consumption since the use of circuits based on conventional metal-oxide-semiconductor transistors to construct artificial

* Corresponding author.

E-mail address: guillermo.vinuesa@uva.es (G. Vinuesa).

<https://doi.org/10.1016/j.mssp.2023.107878>

Received 20 July 2023; Received in revised form 6 September 2023; Accepted 1 October 2023

Available online 18 October 2023

1369-8001/© 2023 The Authors. Published by Elsevier Ltd. This is an open access article under the CC BY license (<http://creativecommons.org/licenses/by/4.0/>).

neurons and synapses is far from being power and area-efficient. Moreover, memristive devices can successfully mimic biological synapses to help in the fabrication of hardware neural networks [10,20–23]. Last but not least, resistive switching (RS) devices have also been employed for cryptography in which physical unclonable functions and true random number generators are imperatively required [24–28].

RRAM dynamics has been tackled previously under ramped voltage stress (RVS) signals with different ramp rates, although many of the studies in the literature focus on conductive-bridge RAM (CBRAM) devices. For example, Schindler et al. [29] observed a logarithmic relationship between the set voltage and the input signal ramp rate (1 mV/s - 1 V/s range). They reported higher set voltages as the frequency increases. Similar results were obtained by Ghosh et al. with respect to the reset voltage [30]; again, a logarithmic relationship was found between the reset voltage and the ramp rate (in the 0.01V/s - 20V/s interval) for CBRAMs.

A detailed study on Pt/NiO/Pt unipolar devices [31], using a broad ramp rate range (1 mV/s – 10 MV/s), showed that both switching voltages increased with the ramp rate. Two other works on unipolar NiO-based devices [32,33] (ramp rate range: 0.5 mV/s - 1V/s and ramp rate range: 5 mV/s - 10 MV/s, respectively), along with an analysis on Ni-based devices [34] (ramp rate range: 35V/s - 1143V/s) showed results in line with the previous studies. Similar studies on this matter, but on valence change memories (VCM), are less common. In particular, a study on Cr-doped SZrO₃ based-devices found that if the ramp rate was too high (the study included a range of 0.5 V/s - 50V/s), resistive switching disappeared [35]. Ielmini et al. [36] studied reset transitions on HfO_x-based devices and observed increased reset voltages as ramp rates grow (their ramp rate range was limited to the 1 mV/s - 1V/s interval). They stated that the switching time depends on the power dissipated in the device. Additionally, Rodriguez-Fernandez et al. [37] demonstrated that in one transistor-one resistor (1T1R) structures with HfO₂-based RRAMs, there is an increase in both the set and reset voltages as the ramp rate is increased (ramp rate range: 10 V/s - 50 kV/s). From a different viewpoint, current-voltage characteristics simulated for 10 V/s and 2 V/s made by Marchewka et al. show increased set voltages as ramp rates rise [38]. Fleck et al. [39], also working on VCMs, analyzed set transitions for a wide ramp rate interval (30 mV/s - 6 MV/s). They found that, as in previous cases, higher set voltages are needed as the ramp rate increases. A preliminary study to the one presented here [40] also pointed out that, at room temperature, both set and reset voltages increased with the ramp rate (100 mV/s – 1 MV/s). Moreover, that investigation proved that the conductance change can be

indeed controlled by the voltage ramp rate.

Studies on resistive switching (RS) including modifications of the voltage signal ramp rate and temperature are an exception. Lin et al. studied BiFeO₃ perovskite-based RRAMs whose operation depends on the ferroelectric and polarization properties of the dielectric [41]. At lower temperatures and higher ramp rates (0.8 V/s - 5V/s) they measured higher currents, with an opposite trend occurring at high temperatures. Concerning the temporal dependences of RVS; e. g., series of voltage pulsed signals, Yu et al. [42] found that, for CBRAMs, as pulse widths increased, lower voltage amplitudes were needed to complete both the set and reset transitions.

In this work, we deal with VCM devices (consisting in TiN/Ti/HfO₂/W stacks) measured under RVS sweeping with a ramp rate range much wider than previously done. In addition, we analyze both the set and reset events as a function of the temperature. This thorough analysis of the experimental results is interpreted in first place considering kinetic Monte Carlo (kMC) simulations. The kinetic Monte–Carlo technique stands as a firmly established methodology that facilitates the comprehension of stochastic phenomena, such as random migration of ions or generation of vacancies. Its large adaptability enables the analysis of thermodynamic and kinetic behavior of fundamental transitions occurring even at complex spatial and temporal scales. Moreover, the inherent stochastic nature of kMC can effectively replicate ions diffusion, generation of vacancies, or other chemical reactions, establishing a link between the microscopic configuration and the macroscopic system behavior. Researchers have utilized kMC to study stochastic phenomena such as resistive switching processes [43,44], variability [45], data retention [46], endurance and device optimization [47] as well as the influence of different ambient temperatures on the filament creation and destruction during the SET and RESET processes [48]. Based on this analysis, the density of oxygen vacancies and the compactness of the conductive filaments (CF) during the switching process can be calculated. After a comprehensive fitting process of the experimental data, compact modeling results based on the Dynamic Memdiode Model (DMM) are also used to catch the essential dynamical aspects of our devices which are difficult to achieve solely using a microscopic approach. The similarities and differences between the microscopic (kMC) and behavioral (DMM) descriptions are also discussed.

2. Materials and methods

The devices investigated in this work are bipolar valence change memory structures based on the TiN/Ti/HfO₂/W stack. They were

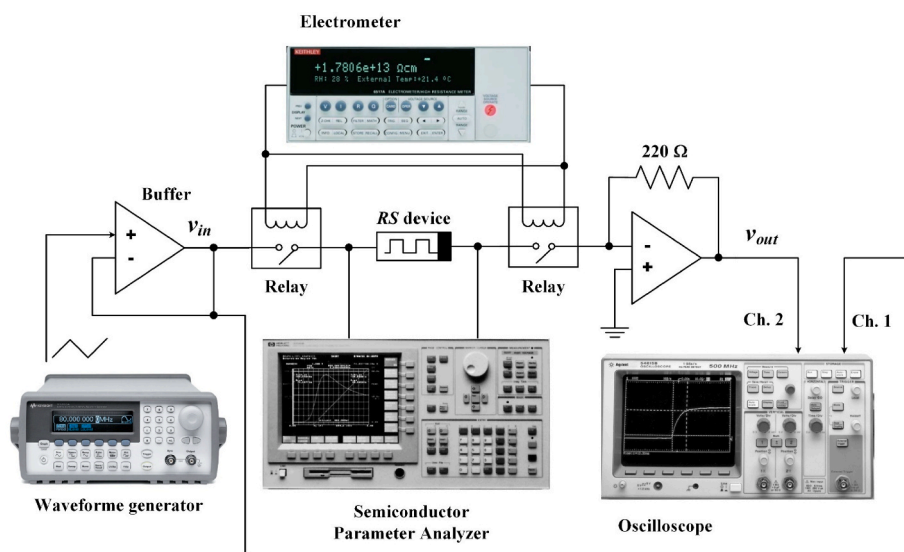


Fig. 1. Ad hoc electrical characterization set-up to obtain the ramp rate variable I-V characteristics.

fabricated using highly-doped N-type ($\rho = 4 \text{ m}\Omega\cdot\text{cm}$) silicon wafers including a 20 nm-thick Ti adherence layer onto which the bottom electrode, a 50 nm-thick W layer, was deposited by magnetron sputtering. The bottom electrode is contacted by an Al layer (500 nm thick) deposited on the back of the wafers. A 100 nm-thick SiO_2 field oxide layer was plasma enhanced chemical vapor deposited (PECVD) and then patterned to define the active area of the MIM devices. Then, a HfO_2 layer 10 nm-thick was grown by atomic layer deposition. The top electrode is formed by a 200 nm-thick TiN layer on a 10 nm-thick Ti layer grown by magnetron sputtering and patterned by a lift-off process. Measurements were performed on devices with an area of $1.44 \times 10^4 \mu\text{m}^2$. Further fabrication details about the devices investigated in this work can be found in a previous work [49].

In order to carry out the current-voltage (I-V) measurements, the devices were cooled down under darkness conditions in an Oxford DM1710 cryostat. An Oxford ITC 502 controller was used to keep the temperature constant during the measurements. Before cooling the devices, an electroforming process was performed with a current compliance of 0.1 mA at room temperature. We used an *ad hoc* electrical characterization set-up [40] (see Fig. 1) to obtain the current-voltage characteristics using different voltage ramp rates. First, the devices are settled in the high or low resistivity state using an HP 4155B Semiconductor Parameter Analyzer to perform the measurement starting from similar initial conditions. Then, a waveform generator (Keysight 33250A) produces a ramped voltage signal in order to change the device resistance state. The current flowing through is obtained using a transimpedance amplifier and is recorded by means of an HP 54615B oscilloscope. The measurement setup is connected to a computer using the GPIB interface and controlled via the Agilent VEE software.

Four different ambient temperatures were analyzed (130 K, 210 K, 290 K, and 350 K), and a wide range of ramp rates for the input voltage signal ($\sim 0.1 \text{ V/s}$ to $\sim 1 \text{ MV/s}$) was considered to characterize the set and reset dynamics of our devices (see Figs. 2 and 3).

3. Results and discussion

3.1. Experimental measurements

In order to study the set dynamics (Fig. 2), the device was first settled in HRS before applying the ramp rate variable voltage signal using a low ramp rate voltage (-1.25 V) from the HP4155B equipment. Similarly, when studying the reset dynamics (Fig. 3), the device was first settled in the LRS using a low ramp rate voltage signal ($+0.8 \text{ V}$ amplitude) to assure now an identical low resistance state before applying the ramp rate variable voltage signal.

As shown in Figs. 2 and 3, the I-V characteristics of our devices strongly depends on the voltage ramp rate. For the highest ramp rates, the set and reset processes are not fully completed due to the fast voltage changes that drive the RS operation. In other words, higher ramp rates require larger voltages to switch the device from HRS to LRS and vice versa [50].

The connection of the ramp rate effects with the two modeling approaches considered in this work will be discussed in Sections 3.4 and 3.5. To deepen into the physics behind RS and to shed light on the switching dynamics of our devices, an analysis of the most significant RS parameters is carried out next.

3.2. Extraction of the set and reset voltages

As illustrated in Figs. 2 and 3, the set and reset voltages notably change with the applied signal ramp rate. To qualitatively assess this dependence, the I-V curves described in the previous section were analyzed using a number of parameter extraction techniques already discussed in the literature [51,52]. In particular, the set voltage, V_{set} , was determined by means of three alternative methods: MS1, which consists in finding the maximum of the numerical derivative of the current (considering the interval between the 40% and 90% of the applied voltage range to avoid data fluctuations); MS2, which detects increments in the current complying with the condition $I_{t+1} \geq (1+a)I_t$ (a

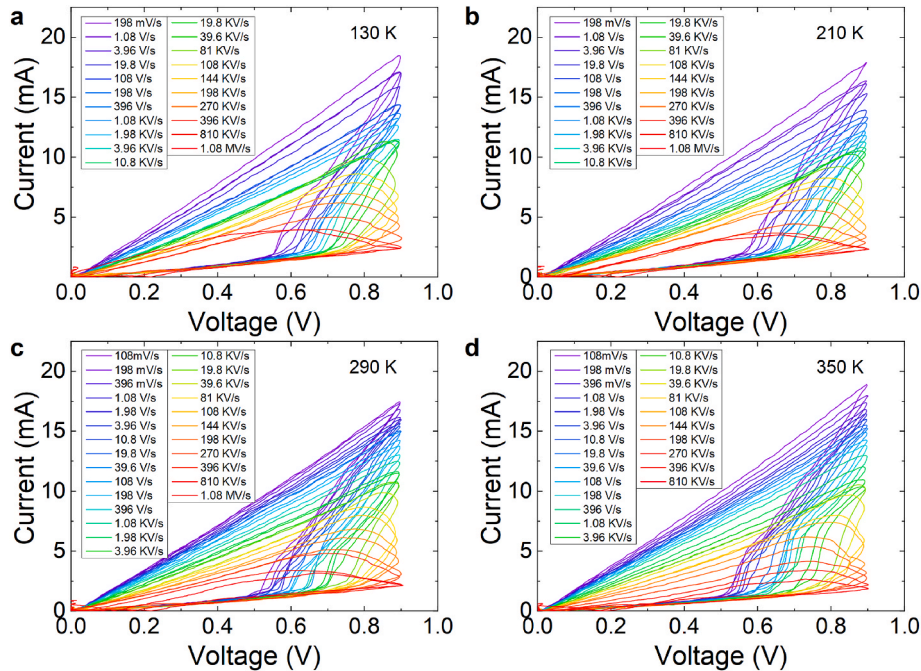


Fig. 2. Experimental set I-V curves for our devices under RVS for different temperatures: a 130 K, b 210 K, c 290 K, d 350 K. A wide range of ramp rates were employed for the input voltage signals.

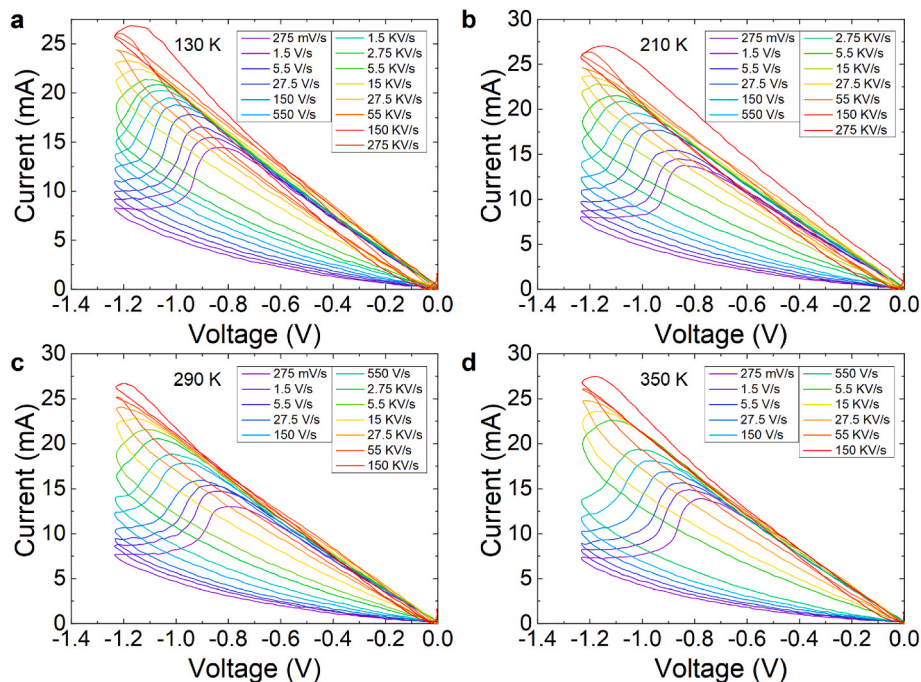


Fig. 3. Experimental reset I–V curves for our devices measured under RVS for different temperatures: **a** 130 K, **b** 210 K, **c** 290 K, **d** 350 K. A wide range of ramp rates were employed for the input voltage signals.

value of 0.1 is given for the fitting parameter [52]); and MS3, which looks for the maximum separation of the experimental curve to a virtual straight line joining its first and end points (in other words, it consists in finding the set curve “knee”) as illustrated in Fig. 4b.

The three methods described above yield almost similar results except for the highest ramp rates at which the shape of the I–V characteristics is remarkably different from the rest. We have also to account for variability effects, which are known to be typical of the RRAM technology [51,53,54]. As shown in Fig. 4a, the $I_{\text{on}}/I_{\text{off}}$ (LRS/HRS) ratio measured at 0.5 V decreases as the ramp rate increases. It is clear that the RS operation degrades (in terms of the resistive window) for high ramp rates regardless of the temperature value. The switching mechanism underpinning the behavior of TiN/Ti/10nm-HfO₂/W devices hinges upon the generation of oxygen vacancies and the diffusion of oxygen ions. These thermally activated processes [55–58] are linked to the application of an electric field. Upon applying an electric field, ions migrate and vacancies are formed within the material. The rate of these processes is determined by the magnitude of the electric field and the temperature, while the extent of generated vacancies and the diffusion of oxygen ions are tied to the duration of the electric field applied during the I–V measurements. Ultimately, these processes determine the device resistance state. Significantly, the application of electric fields with shorter durations (faster ramp rates) results in the diminished generation of vacancies and fewer diffusion of ions that recombine with these vacancies. Consequently, the efficiency of both set and reset processes is compromised, leading to a degradation in the device performance. We have also plotted the extracted set voltages as a function of the ramp rates for the different temperatures considered in our study (Fig. 4c–f). Despite the large fluctuations, it can be seen that the set voltage significantly increases with the ramp rate regardless of the temperature considered. This is expected since for higher ramp rates (assuming identical maximum voltages) the device exposure to thermal effects (and to the electric field), as explained above, is shorter; thus, higher transition voltages are required. Remarkably, all extraction methods provide similar results.

In the case of V_{reset} , four methodologies were considered in this work [52] (Fig. 5b): MR1, which consists in finding the minimum value of the numerical derivative (the interval considered in the X axis is [40%–90%] of the voltage signal to avoid data fluctuations); MR2 which looks for a current decrease complying with the condition $I_{(i+1)} \leq (1 + a)I_i$, in our case $a = 0.1$; MR3, which searches for the maximum current along the curve; and MR4, which corresponds to the first point in the curve with negative derivative.

As can be seen in Fig. 5a, the $I_{\text{on}}/I_{\text{off}}$ ratio at –0.5 V gradually decreases as the ramp rate increases as well. Notice that for high ramp rates, the ratio curves merge for all the temperatures considered, as it is the case illustrated in Fig. 4a.

Fig. 5c–f shows the extracted reset voltages as a function of the input signal ramp rates. See that, in general, the reset voltages obtained with the MR3 and MR4 methods are lower than those found with MR1 and MR2. This effect is a consequence of the numerical technique considered: the detection of the derivative minimum and the maximum current decrease are found at higher voltages than the current maximum or the first point with a current decrease along the reset I–V curve. However, notice that the difference mentioned above is systematic regardless of the device temperature.

3.3. Extraction of the series resistance

In this type of resistive memories, the role played by the series resistance cannot be overlooked [59]. The series resistance appears because of both the metal lines and the remnants of the conductive filament involved in the switching process. It was demonstrated that this parameter has a large influence on the shape of the I–V curves [59].

We have extracted the series resistance of our devices from the experimental curves shown in Figs. 2 and 3. The extraction methodology considers a correction to the applied voltage $V_N = V_{\text{Applied}} - I_{\text{Measured}} \cdot R_S$, where V_{Applied} stands for the external voltage and I_{Measured} is the measured current. If the experimental current is plotted as a function of V_N , sweeping R_S , we get the modified $I_{\text{Measured}} - V_N$ curves; if

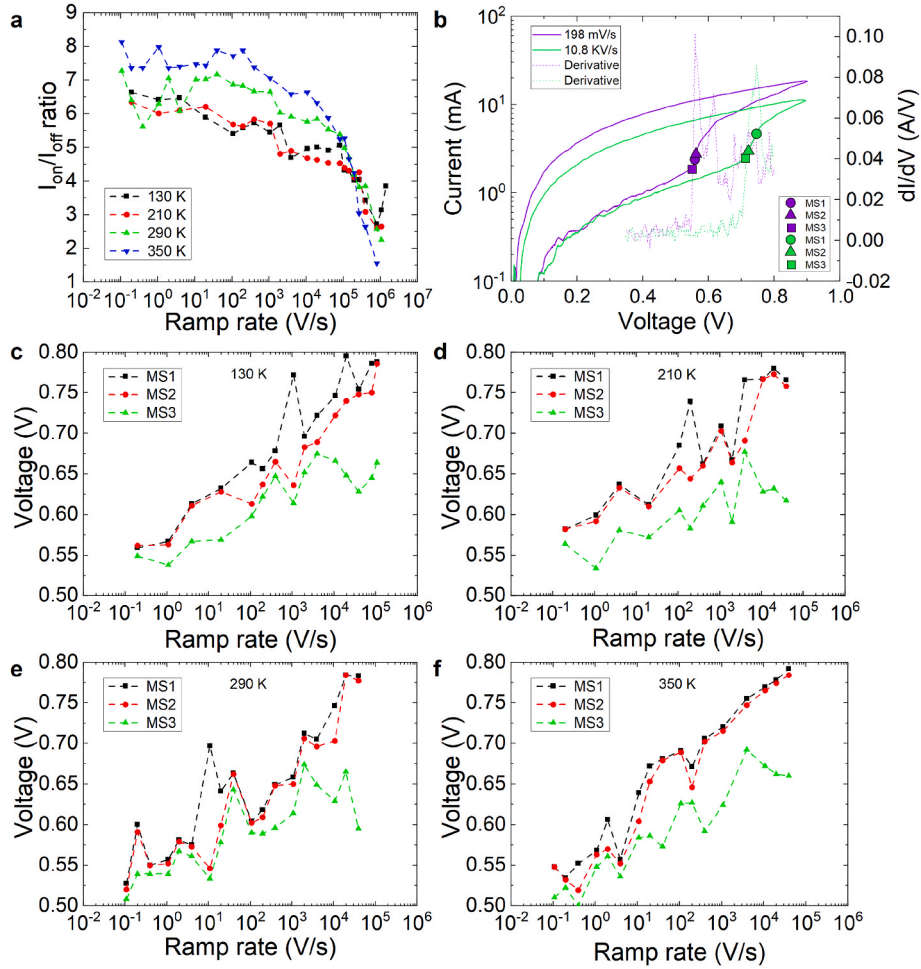


Fig. 4. **a** I_{on}/I_{off} ratio calculated at 0.5 V versus ramp rate of the input signal for the temperatures considered. **b** Experimental current versus voltage for two set of curves describing the extraction procedures employed in this work. The set voltage extraction techniques consists in (MS1) finding the maximum of the current numerical derivative, (MS2) finding the current points that fulfill $I_{i+1} \geq (1+a)I_i$ (where a value of $a = 0.1$ is used) and (MS3) finding the set curve knee. Set voltage versus the ramp rate of the input signal for different temperatures: **c** 130 K, **d** 210 K, **e** 290 K, **f** 350 K.

we select the curve with the steepest slope in the region after the curve knee [59], the value of the series resistance is then obtained. The voltage corresponding to the vertical current increase is often referred to as the set transition voltage (V_{TS}). The CDF for the series resistance is plotted in Fig. 6a. The reported values are in close agreement with previous results [59]. No clear dependence with the temperature was found.

For completeness, the evolution of these parameters is also plotted as a function of the input signal ramp rate. Fig. 7a illustrates the extracted series resistance values and Fig. 7b the set transition voltages as a function of the ramp rate for the different temperatures considered. Again, there seems to be no clear temperature dependence involved. However, an increase of V_{TS} with the ramp rate similar to the one observed for V_{set} is observed.

Importantly, notice that the determination of R_{series} at the highest ramp rates may not yield accurate results due to the significant distortion of the I–V curve under these circumstances. Therefore, this is a numerical issue linked to the procedure employed. As a consequence, the values of R_{series} for the highest ramp rates were disregarded in the above analysis.

3.4. Kinetic Monte Carlo study

In this section, the kinetic Monte Carlo physical simulator previously

reported [57] for the case of HfO_2 -based devices is considered. The most relevant RS processes for this technology were incorporated into the kMC algorithm, for instance: oxygen vacancy generation, oxygen ion diffusion and the recombination of oxygen ions and vacancies. The algorithm also considers the 3D electric field and temperature distributions by solving the corresponding charge and heat equations. The transition rates Γ for each physical mechanism are described by Arrhenius-type equations such as:

$$\Gamma = \nu \exp\left(-\frac{E_A}{\kappa_B T}\right) \quad (1)$$

where ν is the vibration constant of the particle, E_A the activation energy (i.e. the energy barrier height for the process involved), κ_B the Boltzmann constant and T the local temperature [60]. The inverse of the transition rate corresponds to the characteristic time needed for a given process to take place and they are taken into account for the simulator time step estimation. Importantly, as in the standard approach, the effective activation energies for the oxygen vacancies generation (formation of an oxygen vacancy and ion Frenkel pair) process ($E_G = E_G(F=0) - b \cdot F(x,y,z)$) and oxygen ion diffusion ($E_D = E_D(F=0) - k_D \cdot F(x,y,z)$) linearly reduce with the local electric field ($F(x,y,z)$); therefore, affecting the transition rates within the kMC algorithm. A thorough description of the kMC approach can be found in a previous work by

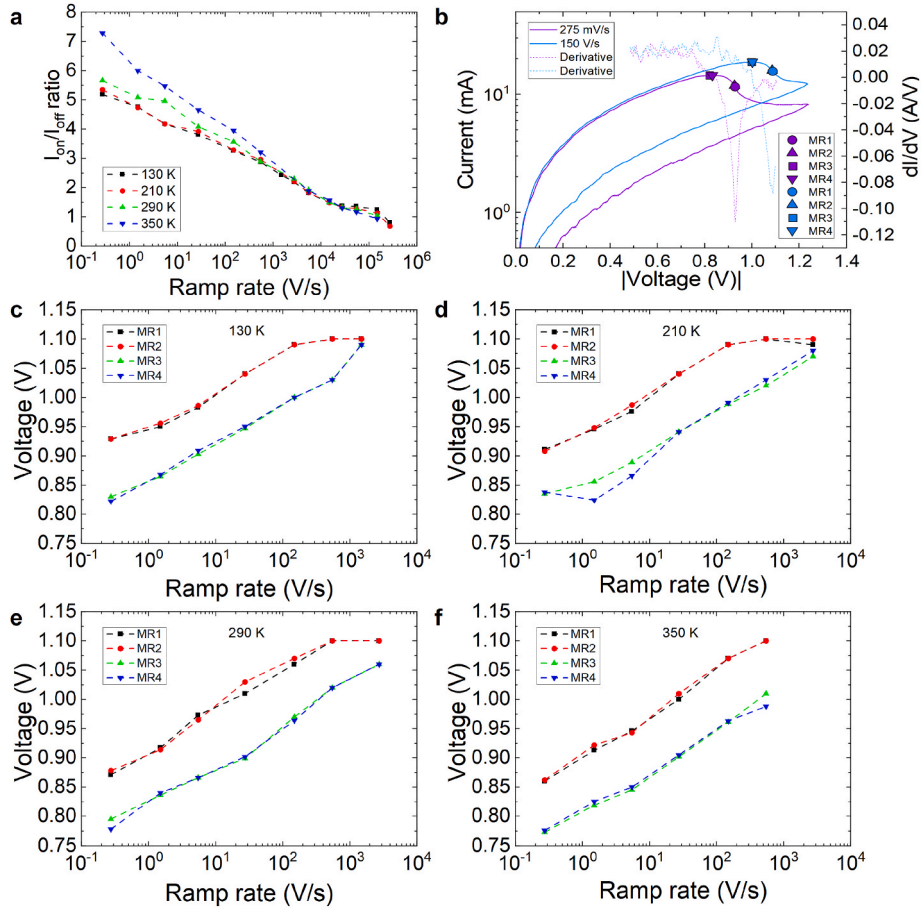


Fig. 5. **a** I_{on}/I_{off} ratio calculated at -0.5 V versus ramp rate of the input signal for the temperatures considered. **b** Experimental current versus voltage for two reset curves detailing the extraction procedures employed in this work. The reset voltage extraction algorithm consists in (MR1) finding the minimum of the current numerical derivative, (MR2) finding the current points that fulfill $I_{i+1} \leq (1 + a)I_i$, ($a = 0.1$ in our algorithm). (MR3) consists in finding the maximum current along the curve and (MR4) denotes the first point with negative derivative. Reset voltage versus the ramp rate of the input signal for different temperatures: **c** 130 K, **d** 210 K, **e** 290 K, **f** 350 K.

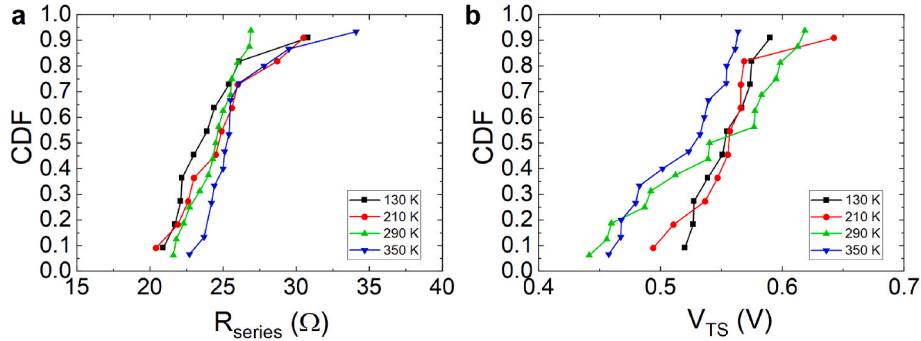


Fig. 6. Cumulative distribution functions for **a** the series resistance extracted for different temperatures employing the methodology described by Maldonado et al. [59], and for **b** the extracted transition voltage for different temperatures.

Aldana et al. [57].

In this work, we have analyzed the conductive filament dynamics that leads to a typical RS event in terms of growth and rupture. To do so, we reproduced the I–V curves during the set transition for different ramp rates using the kMC approach (Fig. 8). Notice that the voltage ramp rate affects the transition rate through the electric field dependence of the

effective activation energies. A close agreement between the simulated and the experimental curves is obtained as shown in Fig. 8.

In this regard, the well-known set voltage increase with the ramp rate is correctly addressed by simulations (see Fig. 8d). To complete the overall picture, Fig. 9 shows the number of oxygen vacancies in the simulation domain having 1 to 6 neighbors. As previously established,

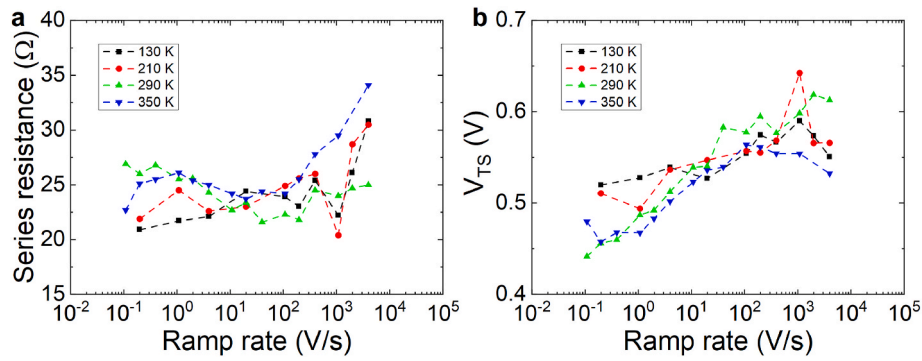


Fig. 7. a Series resistance and b set transition voltage versus voltage ramp rate for different temperatures.

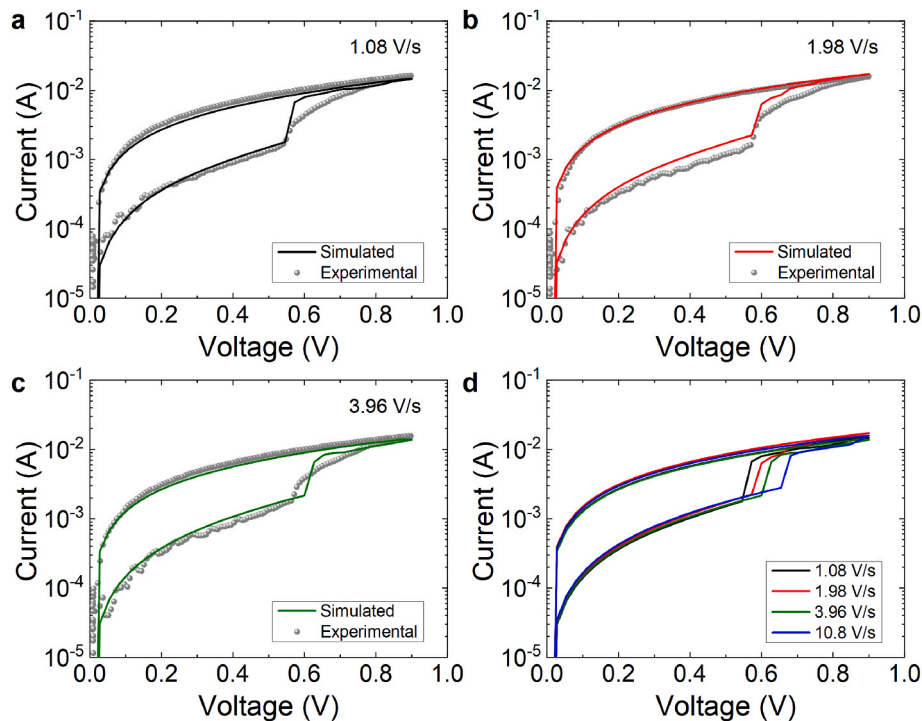


Fig. 8. Experimental and kMC simulated set curves for the devices under study at room temperature for three different ramped rates: a 1.08 V/s, b 1.98 V/s and c 3.96 V/s d I–V simulated curves at room temperature for four different voltage ramp rates (1.08 V/s, 1.98 V/s, 3.96 V/s and 10.8 V/s), notice the set voltage rises as the ramp rate increases, as seen in Fig. 3.

the rate of vacancy generation depends on the activation energy, which is influenced by the local electric field and temperature. According to the simulations, the ramp rate increase generates more oxygen vacancies with three or fewer neighbors, while the number of oxygen vacancies with four or more neighbors notably drops off.

As the vacancy generation decreases with faster ramp rates, a reduction of the CF density is therefore observed. Hence, for higher ramp rates, higher voltages are needed in order to generate the amount of oxygen vacancies necessary to trigger the formation of the conductive filament leading the device to LRS (a fully developed percolation path in the context of our simulation approach). This effect provides a microscopic explanation for the increment of the set voltage experimentally observed. Thermal effects are obviously intertwined with the physical mechanisms implemented in the kMC algorithm that ultimately led to this behavior since the vacancy movement is thermally activated.

In Fig. 10, we report data similar to those shown in Fig. 9, in this case in the time domain. Again, the results in terms of the oxygen vacancies with low number of neighbors are linked to the ramp rate as referred above. In this case we can interpret this behavior to be originated in the shorter time the electric field affects the atomic network in connection with the oxygen vacancies displacement.

3.5. Compact modeling approach

In this Section we make use of a compact model in order to provide an analytical description of the behavioral aspects behind the resistive switching effect. In general, for circuit simulations, models are required to reproduce the electrical characteristics of the devices (hysteresis phenomena, pinched I–V loop, resistive-like behavior at high frequencies, etc.) and these models must be defined in terms of a low

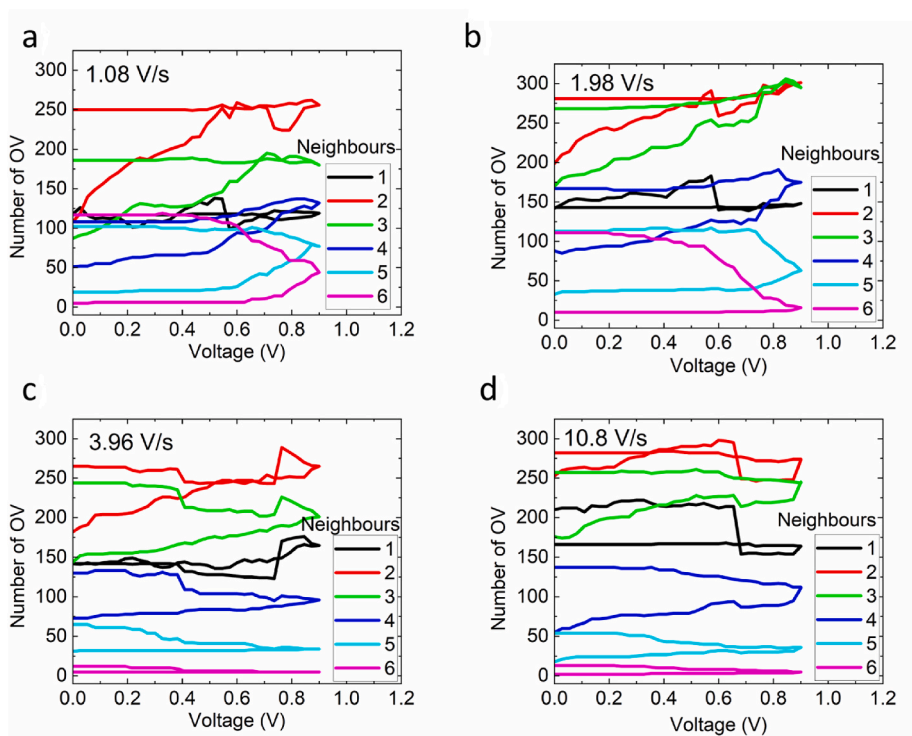


Fig. 9. Number of oxygen vacancies in the simulation domain versus applied voltage along a set process. We have separated the oxygen vacancies with 1–6 neighbors (the maximum allowed in the simulation) [61] in the simulation domain. The data shown correspond to the simulations described in Fig. 8d, the ramp rates are the following: a 1.08 V/s, b 1.98 V/s, c 3.96 V/s and d 10.8 V/s.

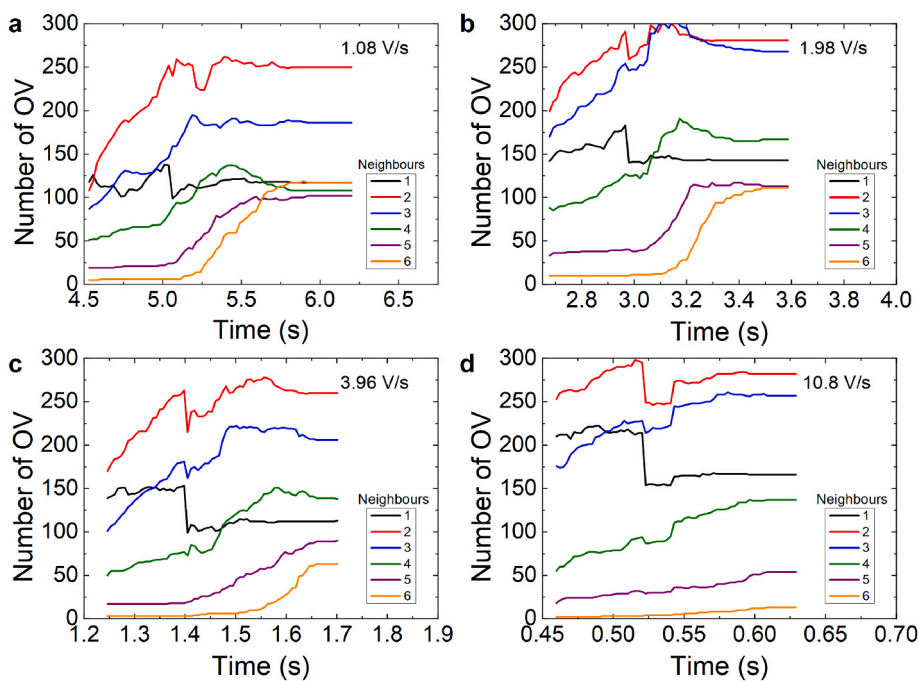


Fig. 10. Evolution of the number of oxygen vacancies in the simulation domain versus simulation time in a set process (different time windows were employed to adapt to the ramp rate). We have separated the oxygen vacancies with 1–6 neighbors in the simulation domain (the maximum allowed in the simulation). The data shown correspond to the simulations described in Fig. 8d, the ramp rates are the following: a 1.08 V/s, b 1.98 V/s, c 3.96 V/s and d 10.8 V/s.

number of well-behaved mathematical expressions driven by a reduced set of parameters with physical or electrical meaning. These are the so-called compact behavioral models and they can be developed from different perspectives; some of the most representatives (Yakopcic [62], TEAM [63], VTEAM [64], Eshraghian [65], etc.) have their foundations in Prof. Chua's theory for memristive devices [66]. In this Section, we consider the Dynamic Memdiode Model (DMM) [67–69] as it has been successfully used for simulating large memristor-based neural networks [70]. Succinctly, this model defines a memristor by a system of two coupled equations: i) the current-voltage (I–V) relationship and ii) the memory state equation (λ -t). In the framework of the DMM, the I–V is described by means of the charge that flows through a filamentary structure formed by ions or oxygen vacancies (this latter option holds valid for our devices) according to Equation (2),

$$I(V) = I_0(\lambda) \left[e^{\beta\alpha(V-R_S I)} - e^{-(1-\beta)\alpha(V-R_S I)} \right] \quad (2)$$

which can be derived from the finite-bias Landauer's formula for a monomode ballistic conductor [71–73]. I_0 and α are model parameters related to the effective shape and lateral size of the constriction. R_S is a series resistance required for the linearization of Equation (2) in the high-current regime which in turn can be linked to the series resistance previously extracted in Section 3.3. The double exponential dependence in Equation (2) can be electrically identified with the behavior of two opposite-biased diodes and that's why the name of the model, i.e. memdiode. β is a constant that accounts for the possible asymmetry in the potential drop at the filament-electrode connections. Regarding the memory state equation, the considered differential equation for the hysteretic evolution of $0 < \lambda < 1$ is given by:

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda, V)} - \frac{\lambda}{\tau_R(\lambda, V)} \quad (3)$$

where $\tau_{S,R}(\lambda, V)$ are characteristic times associated with the set ($V > 0$) and reset ($V < 0$) transitions, i.e. with the movement of oxygen ions and vacancies within the dielectric film in one or the opposite direction. In the framework of the DMM, these times are expressed as:

$$\tau_S(\lambda, V) = e^{-\eta_S(V-V_S)} \quad (4)$$

$$\tau_R(\lambda, V) = e^{\eta_R(V-V_R)} \quad (5)$$

where $\eta_{S,R}(\lambda, V)$ and $V_{S,R}(\lambda, V)$ are the transition rates ($\eta_S, \eta_R > 0$) and the reference switching voltages ($V_S > 0, V_R < 0$), respectively. The exponential dependences of Equations (4) and (5) on V are a consequence of the diffusive dynamics of the atomic species [74] and they have the same foundation as Equation (1). At the end, this is in line with the transition state theory (TST) which introduces the transition rate calculation used as part of the kMC algorithm [45]. In case of the compact modeling approach, the transition rates are considered as a behavioral rule rather than as a local prescription.

For the sake of simplicity, let us consider in the following analysis the set transition exclusively. A similar approach can be followed with the reset transition. In this case, the second term in Equation (3) can be dropped so that we have,

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S} \quad (6)$$

Equation (6) can be easily integrated for a voltage ramp $V(t) = RR \cdot t$ using expression 4. RR is the signal ramp rate. Notice that V_S in expression 4 is simply the voltage at which $\tau_S = 1$, and not the set voltage. Integrating the differential equation we have,

$$\lambda(V) = (\lambda_0 - 1) \exp\left\{ -\frac{\exp(-\eta_S V_S) [\exp(\eta_S V) - 1]}{\eta_S RR} \right\} + 1 \quad (7)$$

where λ_0 is the initial the memory state value. If, again, for the sake of simplicity, $\lambda_0 = 0$ and $\lambda = 1/2$ are assumed as the initial and reference conditions for the set voltage (V_{set}), respectively, making use of Equation (7), we have:

$$V_{set} \approx \frac{1}{\eta_S} \ln \left[\frac{\ln(2)\eta_S RR}{\exp(-\eta_S V_S)} \right] \quad (8)$$

That is,

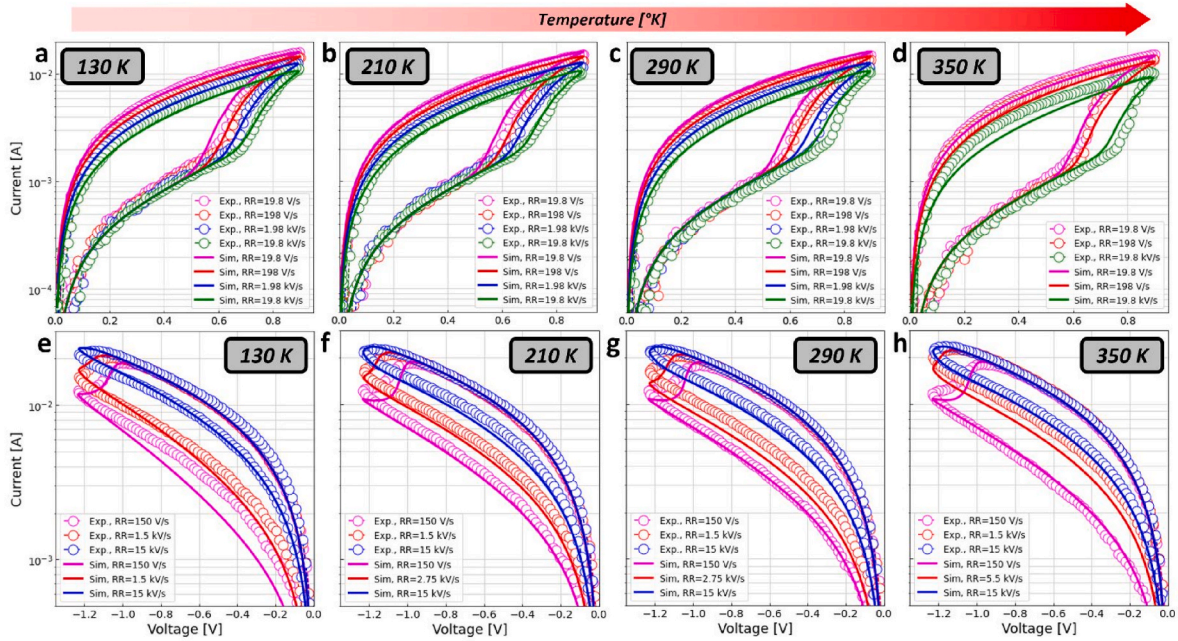


Fig. 11. Set (a–d) and reset (e–h) current versus voltage at 130 K, 210 K, 290 K and 350 K. Experimental and modeled data are plotted for different ramp rates (19.8 V/s, 198 V/s, 1.98 kV/s and 19.8 kV/s for the set loops, and 150 V/s, 1.5 V/s, 2.75 kV/s, 5.5 kV/s and 15 kV/s for the reset loops).

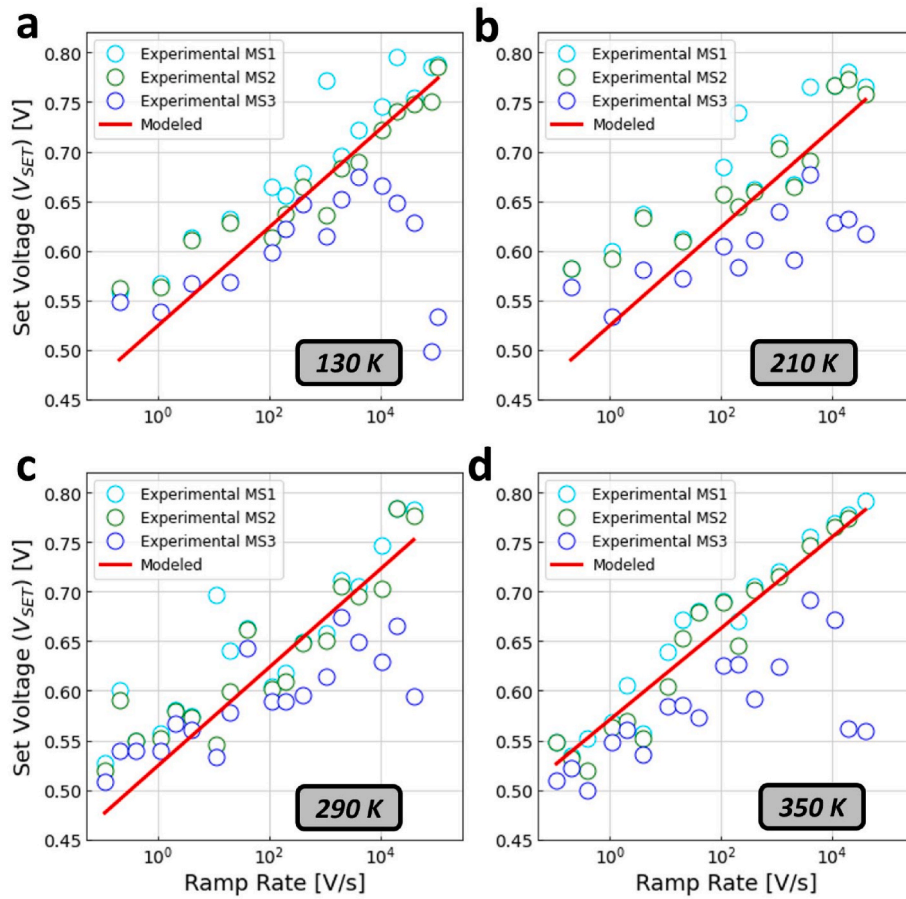


Fig. 12. Evolution of the set voltage (V_{SET}) as a function of the ramp rate. Experimental data obtained with the different numerical methods employed in this work are fitted considering Equation (6). a 130 K, b 210 K, c 290 K and d 350 K. In all cases the parameters for Equation (5) are $\eta_s = 46.5$ 1/V and $V_s = 0.45$ V.

$$V_{set} \approx \frac{1}{\eta_s} \ln(RR) + constant \quad (9)$$

as experimentally observed (see Figs. 4 and 5). This point is discussed below in terms of fitting results for the whole I–V curve.

Fig. 11 shows the fitting of the experimental I–V loops originally presented in Figs. 2 and 3 using the DMM for different ramp rates. See more details on the model parameters employed in the Appendix. The model parameters are almost the same for all the 4 temperatures and 8 ramp rates investigated.

The fitting results show that the DMM is capable of capturing the I–V characteristics, mainly in connection with the ramp rate (temperature is not included in the model) [37,75]. Note that the DMM simulations accurately reproduce the shift of the set and reset transitions towards higher absolute voltages as the ramp rates rise, consequently causing a change in the current levels after the set and reset events. This is shown for the case of the set transition in Fig. 12, in which the data shown in Fig. 4 were considered. The red solid lines correspond to the expected results from Equation (9). What is remarkable from the fitting results is that the external temperature seems to play a minor role in the overall behavior of our curves. This does not rule out the role played by the local temperature within the dielectric structure, but again, the obtained results indicate that this is not a significantly relevant parameter from a behavioral viewpoint. Of course, this cannot be considered as a general rule for all kind of memristors.

4. Conclusions

Resistive switching operation of TiN/Ti/HfO₂/W resistive memories has been studied in depth by means of extensive experimental characterization, kinetic Monte Carlo simulations and compact modeling. Ramped voltage stress for a wide range of ramp rates was employed. Measurements were also performed at different temperatures. The kinetic Monte Carlo simulations showed that the conductive filament compactness depends on the voltage time variation which can explain the increment of the set and reset voltages with the ramp rate increase. In addition, the Dynamic Memdiode Model allowed representing the conductive filament formation and rupture processes by means of a behavioral approach. In this case, the movement of oxygen ions and vacancies are described by means of simplified transition rates that allow to describe the device dynamics in terms of a single differential equation for the memory state of the device. The functional dependence of the set voltage on the input signal ramp rate is reproduced with the model by using the parameters tuned by means of experimental I–V curves. We have shown that both temperature and electric field influence the device resistive switching operation. Nevertheless, for these specific devices, the external temperature seems to play a minor role in comparison to the electric field.

CRedit authorship contribution statement

D. Maldonado: Writing – original draft, Software, Methodology, Investigation, Formal analysis, Data curation. **G. Vinuesa:** Writing –

review & editing, Visualization, Methodology, Investigation, Formal analysis, Data curation. **S. Aldana:** Software, Methodology, Investigation, Formal analysis, Data curation. **F.L. Aguirre:** Writing – review & editing, Visualization, Software, Methodology, Investigation, Formal analysis, Data curation. **A. Cantudo:** Software, Methodology, Investigation, Data curation. **H. García:** Supervision, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **M.B. González:** Resources, Project administration, Methodology, Funding acquisition. **F. Jiménez-Molinós:** Writing – review & editing, Validation, Software, Resources, Methodology, Investigation, Funding acquisition, Data curation, Conceptualization. **F. Campabadal:** Supervision, Resources, Methodology, Funding acquisition. **E. Miranda:** Writing – review & editing, Validation, Supervision, Software, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization. **S. Dueñas:** Validation, Supervision, Resources, Methodology, Funding acquisition. **H. Castán:** Validation, Supervision, Resources, Methodology, Funding acquisition. **J.B. Roldán:** Writing – review & editing, Writing – original draft, Validation, Supervision, Software, Resources, Methodology, Investigation, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial

APPENDIX

Memdiode model script adapted from Ref. [59]. The code corresponds to a subcircuit description in LTSPICE.

```
.subckt memdiode + - H
*Model parameters
.params
+ H0=0 ri=20 RPP=1E10
+ ion=15e-3 ioff=6e-04 ron=1 roff=1 aoff=2.95 aon=1.9
+ etas=46.5 vs=0.45 etar=53 vr=-0.45 gam=0.5
*Memory Equation
BV A 0 V=if(V(+,-)>=0,1,0)
RH H A R=if(V(+,-)>=0,TS(V(C,-)),TR(V(C,-)))
CH H 0 1 ic={H0}
*I-V
RI + C {ri}
RS C B R=K(ron,roff)
BF B - I=K(ion,ioff)*sinh(K(aon,aoff)*V(B,-))
RB + - {RPP}
*Auxiliary functions
.func K(on,off)=off+(on-off)*limit(0,1,V(H))
.func TS(x)=exp(-etas*(x- vs))
.func TR(x)=exp(etar*pow(x,gam)*(x-vr))
.ends
```

Model parameters for the different temperatures investigated:

	130 K	210 K	290 K	350 K
ion	15e-3	15e-3	15e-3	16e-3
ioff	6e-04	6e-04	6e-04	17.5e-04
aoff	2.95	2.95	2.95	2.15
etas	46.5	46.5	46.5	50
vs	0.45	0.45	0.45	0.50
etar	53	53	54	46
vr	-0.45	-0.45	-0.45	-0.43

interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

This work was supported by the Spanish Ministry of Science and Innovation and FEDER program [PID2022-139586NB-C41, PID2022-139586NB-C42, PID2022-139586NB-C43, PID2022-139586NB-C44], the Consejería de Conocimiento, Investigación y Universidad, Junta de Andalucía (Spain) [B-TIC-624-UGR20] and the Spanish Consejo Superior de Investigaciones Científicas (CSIC) [20225AT012], with support of FEDER funds. M. B. G. acknowledges the Ramón y Cajal grant number RYC2020-030150-I. E.M and F.A. acknowledge the support from the European project MEMQuD, code 20FUN06, which has received funding from the EMPIR programme co-financed by the Participating States and from the European Union's Horizon 2020 research and innovation programme.

References

- [1] M. Lanza, et al., Memristive technologies for data storage, computation, encryption, and radio-frequency communication, *Science* 376 (2022), eabj9979, <https://doi.org/10.1126/science.abj9979>.
- [2] C.-C. Chou, et al., "An N40 256K×44 embedded RRAM macro with SL-precharge SA and low-voltage current limiter to improve read and write performance", in: 2018 IEEE International Solid - State Circuits Conference (ISSCC), 2018, pp. 478–480, <https://doi.org/10.1109/ISSCC.2018.8310392>. San Francisco, CA, USA.
- [3] C.-F. Yang, et al., "Industrially applicable read disturb model and performance on mega-bit 28nm embedded RRAM", in: 2020 IEEE Symposium on VLSI Technology, 2020, pp. 1–2, <https://doi.org/10.1109/VLSITechnology18217.2020.9265060>. Honolulu, HI, USA.
- [4] C.-C. Chou, et al., "A 22nm 96KX144 RRAM macro with a self-tracking reference and a low ripple charge pump to achieve a configurable read window and a wide operating voltage range", in: 2020 IEEE Symposium on VLSI Circuits, 2020, pp. 1–2, <https://doi.org/10.1109/VLSICircuits18222.2020.9163014>. Honolulu, HI, USA.
- [5] P. Jain, et al., "13.2 A 3.6Mb 10.1Mb/mm² embedded non-volatile ReRAM macro in 22nm FinFET technology with adaptive forming/set/reset schemes yielding down to 0.5V with sensing time of 5ns at 0.7V", in: 2019 IEEE International Solid-State Circuits Conference - (ISSCC), 2019, pp. 212–214, <https://doi.org/10.1109/ISSCC.2019.8662393>. San Francisco, CA, USA.
- [6] H.-S.P. Wong, et al., Metal-oxide RRAM, in: *Proceedings of the IEEE*, 100, 2012, pp. 1951–1970, <https://doi.org/10.1109/JPROC.2012.2190369>, 6.
- [7] V. Gupta, et al., Resistive random access memory: a review of device challenges, *IETE Tech. Rev.* 37 (4) (2020) 377–390, <https://doi.org/10.1080/02564602.2019.1629341>.
- [8] A. Chen, A review of emerging non-volatile memory (NVM) technologies and applications, *Solid State Electron.* 125 (2016) 25–38, <https://doi.org/10.1016/j.sse.2016.07.006>.
- [9] M. Lanza, et al., Recommended methods to study resistive switching devices, *Advanced Electronics Materials* 5 (2019), 1800143, <https://doi.org/10.1002/aelm.201800143>.
- [10] A. Sebastian, et al., Memory devices and applications for in-memory computing, *Nat. Nanotechnol.* 15 (2020) 529–544, <https://doi.org/10.1038/s41565-020-0655-z>.
- [11] Tang, et al., Bridging biological and artificial neural networks with emerging neuromorphic devices: fundamentals, progress, and challenges, *Adv. Mater.* 31 (2019), 1902761, <https://doi.org/10.1002/adma.201902761>.
- [12] S. Yu, et al., An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation, *IEEE Trans. Electron. Dev.* 58 (8) (2011) 2729–2737, <https://doi.org/10.1109/TED.2011.2147791>.
- [13] E. Pérez-Bosch, et al., Toward reliable compact modeling of multilevel 1T-1R RRAM devices for neuromorphic systems, *Electronics* 10 (2021) 645, <https://doi.org/10.3390/electronics10060645>.
- [14] S. Ambrogio, et al., Equivalent-accuracy accelerated neural-network training using analogue memory, *Nature* 558 (2018) 60–67, <https://doi.org/10.1038/s41586-018-0180-5>.
- [15] P.A. Merolla, et al., A million spiking-neuron integrated circuit with a scalable communication network and interface, *Science* 345 (2014) 668–673, <https://doi.org/10.1126/science.1254642>.
- [16] F. Alibart, et al., Pattern classification by memristive crossbar circuits using ex situ and in situ training, *Nat. Commun.* 4 (2013) 2072, <https://doi.org/10.1038/ncomms3072>.
- [17] M. Prezioso, et al., Training and operation of an integrated neuromorphic network based on metal-oxide memristors, *Nature* 521 (2015) 61–64, <https://doi.org/10.1038/nature14441>.
- [18] M.A. Zidan, et al., The future of electronics based on memristive systems, *Nature Electronics* 1 (2018) 22–29, <https://doi.org/10.1038/s41928-017-0006-8>.
- [19] J.B. Roldán, et al., Spiking neural networks based on two-dimensional materials, *Npj 2D Materials and Applications* 6 (2022) 63, <https://doi.org/10.1038/s41699-022-00341-5>.
- [20] S. Yu, et al., Compute-in-Memory: from device innovation to 3D system integration, in: *ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference, 2021*, pp. 21–28, <https://doi.org/10.1109/ESSDERC53440.2021.9631765>. Grenoble, France.
- [21] C. Mahata, et al., Resistive switching and synaptic behaviors of an HfO₂/Al₂O₃ stack on ITO for neuromorphic systems, *J. Alloys Compd.* 826 (2020), 154434, <https://doi.org/10.1016/j.jallcom.2020.154434>.
- [22] C. Mahata, et al., Modified resistive switching performance by increasing Al concentration in HfO₂ on transparent indium tin oxide electrode, *Ceram. Int.* 47 (1) (2021) 1199–1207, <https://doi.org/10.1016/j.ceramint.2020.08.238>.
- [23] C. Mahata, et al., Quantized synaptic characteristics in HfO₂-nanocrystal based resistive switching memory, *J. Mater. Res. Technol.* 21 (2022) 981–991, <https://doi.org/10.1016/j.jmrt.2022.09.095>.
- [24] B. Yang, et al., RRAM random number generator based on train of pulses, *Electronics* 10 (2021) 1831, <https://doi.org/10.3390/electronics10151831>.
- [25] D. Arumí, et al., Unpredictable bits generation based on RRAM parallel configuration, *IEEE Electron. Device Lett.* 40 (2019) 341–344, <https://doi.org/10.1109/LED.2018.2886396>.
- [26] Z. Wei, et al., "True random number generator using current difference based on a fractional stochastic model in 40-nm embedded ReRAM", in: 2016 IEEE International Electron Devices Meeting (IEDM), 2016, <https://doi.org/10.1109/IEDM.2016.7838349>. San Francisco, CA, pp. 4.8.1–4.8.4.
- [27] M. Lanza, et al., Advanced data encryption using 2D materials, *Adv. Mater.* 33 (2021), 2100185, <https://doi.org/10.1002/adma.202100185>.
- [28] R. Carboni, et al., Stochastic memory devices for security and computing, *Advanced Electronic Materials* 5 (2019), 1900198, <https://doi.org/10.1002/aelm.201900198>.
- [29] C. Schindler, et al., Electrode kinetics of Cu–SiO₂-based resistive switching cells: overcoming the voltage-time dilemma of electrochemical metallization memories, *Appl. Phys. Lett.* 94 (2009), 072109, <https://doi.org/10.1063/1.3077310>.
- [30] G. Ghosh, et al., Write and erase threshold voltage interdependence in resistive switching memory cells, *IEEE Trans. Electron. Dev.* 62 (9) (2015) 2850–2856, <https://doi.org/10.1109/TED.2015.2452411>.
- [31] C. Cagli, et al., Modeling of set/reset operations in NiO-based resistive-switching memory devices, *IEEE Trans. Electron. Dev.* 56 (2009) 1712–1720, <https://doi.org/10.1109/TED.2009.2024046>.
- [32] U. Russo, et al., Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices, *IEEE Trans. Electron. Dev.* 56 (2) (2009) 186–192, <https://doi.org/10.1109/TED.2008.2010583>.
- [33] S. Larentis, et al., Filament diffusion model for simulating reset and retention processes in RRAM, *Microelectron. Eng.* 88 (2011) 1119–1123, <https://doi.org/10.1016/j.mee.2011.03.055>.
- [34] M. Maestro, et al., Analysis of Set and Reset mechanisms in Ni/HfO₂-based RRAM with fast ramped voltages, *Microelectron. Eng.* 147 (2015) 176–179, <https://doi.org/10.1016/j.mee.2015.04.057>.
- [35] J.-W. Park, et al., Effects of switching parameters on resistive switching behaviors of polycrystalline SrZrO₃:Cr-based metal-oxide-metal structures, *IEEE Trans. Electron. Dev.* 55 (7) (2008) 1782–1786, <https://doi.org/10.1109/TED.2008.924442>.
- [36] D. Ielmini, et al., Evidence for voltage-driven set/reset processes in bipolar switching RRAM, *IEEE Trans. Electron. Dev.* 59 (8) (2012) 2049–2056, <https://doi.org/10.1109/TED.2012.2199497>.
- [37] A. Rodríguez-Fernández, et al., Effect of the voltage ramp rate on the set and reset voltages of ReRAM devices, *Microelectron. Eng.* 178 (2017) 61–65, <https://doi.org/10.1016/j.mee.2017.04.039>.
- [38] A. Marchewka, et al., A 2D Axisymmetric Dynamic Drift-Diffusion Model for Numerical Simulation of Resistive Switching Phenomena in Metal Oxides", 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Nuremberg, Germany, 2016, pp. 145–148, <https://doi.org/10.1109/SISPAD.2016.7605168>.
- [39] K. Fleck, et al., Interrelation of sweep and pulse analysis of the SET process in SrTiO₃ resistive switching memories, *IEEE Electron. Device Lett.* 35 (9) (2014) 924–926, <https://doi.org/10.1109/LED.2014.2340016>.
- [40] H. García, et al., Effects of the voltage ramp rate on the conduction characteristics of HfO₂-based resistive switching devices, *J. Phys. D Appl. Phys.* 56 (2023), 365108, <https://doi.org/10.1088/1361-6463/acdae0>.
- [41] Y.B. Lin, et al., Temperature-dependent and polarization-tuned resistive switching in Au/BiFeO₃/SrRuO₃ junctions, *Appl. Phys. Lett.* 104 (14) (2014), 143503, <https://doi.org/10.1063/1.4870813>.
- [42] S. Yu, et al., Read/write schemes analysis for novel complementary resistive switches in passive crossbar memory arrays, *Nanotechnology* 21 (2010), 465202, <https://doi.org/10.1088/0957-4484/21/46/465202>.
- [43] D. Maldonado, et al., *Microelectron. Eng.* 257 (2022), 111736, <https://doi.org/10.1016/j.mee.2022.111736>.
- [44] S. Dirkmann, et al., Filament growth and resistive switching in hafnium oxide memristive devices, *ACS Appl. Mater. Interfaces* 10 (17) (2018) 14857–14868, <https://doi.org/10.1021/acsami.7b19836>.
- [45] S. Aldana, et al., Resistive switching in HfO₂ based valence change memories, a comprehensive 3D kinetic Monte Carlo approach, *J. Phys. Appl. Phys.* 53 (2020), 225106, <https://doi.org/10.1088/1361-6463/ab7bb6>.
- [46] S. Aldana, et al., Unravelling the data retention mechanisms under thermal stress on 2D memristors, *ACS Omega* 8 (30) (2023) 27543–27552.
- [47] S. Aldana, et al., On the switching mechanism and optimisation of ion irradiation enabled 2D MoS₂ memristors, *Nanoscale* 15 (2023) 6408–6416.
- [48] D. Maldonado, et al., An experimental and simulation study of the role of thermal effects on variability in TiN/Ti/HfO₂/W resistive switching nonlinear devices, *Chaos, Solit. Fractals* 160 (2022), 112247.
- [49] S. Poblador, et al., Methodology for the characterization and observation of filamentary spots in HfO_x-based memristor devices, *Microelectron. Eng.* 223 (2020), 111232, <https://doi.org/10.1016/j.mee.2020.111232>.
- [50] M.B. González, et al., Current transient response and role of the internal resistance in HfO_x-based memristors, *Appl. Phys. Lett.* 117 (2020), 262902, <https://doi.org/10.1063/5.0031575>.
- [51] D. Maldonado, et al., *Microelectron. Eng.* 257 (2022), 111736, <https://doi.org/10.1016/j.mee.2022.111736>.
- [52] D. Maldonado, et al., Variability estimation in resistive switching devices, a numerical and kinetic Monte Carlo perspective, *Microelectron. Eng.* 265 (2022), 111876, <https://doi.org/10.1016/j.mee.2022.111876>.
- [53] J.B. Roldán, et al., Variability in resistive memories, *Advanced Intelligent Systems* (2023), 2200338, <https://doi.org/10.1002/aisy.202200338>.
- [54] C. Acal, et al., Holistic variability analysis in resistive switching memories using a two-dimensional variability coefficient, *ACS Appl. Mater. Interfaces* 15 (15) (2023) 19102–19110, <https://doi.org/10.1021/acsami.2c22617>.
- [55] J.B. Roldán, et al., On the thermal models for resistive random access memory circuit simulation, *Nanomaterials* 11 (2021) 1261, <https://doi.org/10.3390/nano11051261>.

- [56] C. Funck, et al., Comprehensive model of electron conduction in oxide-based memristive devices, *ACS Appl. Electron. Mater.* 3 (2021) 3674–3692, <https://doi.org/10.1021/acsaem.1c00398>.
- [57] S. Aldana, et al., Resistive switching in HfO₂ based valence change memories, a comprehensive 3D kinetic Monte Carlo approach, *J. Phys. Appl. Phys.* 53 (2020), 225106, <https://doi.org/10.1088/1361-6463/ab7bb6>.
- [58] S. Dirkmann, et al., Filament growth and resistive switching in hafnium oxide memristive devices, *ACS Appl. Mater. Interfaces* 10 (17) (2018) 14857–14868, <https://doi.org/10.1021/acsaami.7b19836>.
- [59] D. Maldonado, et al., Experimental study of the series resistance effect and its impact on the compact modeling of the conduction characteristics of HfO₂-based resistive switching memories, *J. Appl. Phys.* 130 (2021), 054503, <https://doi.org/10.1063/5.0055982>.
- [60] J. Guy, et al., Investigation of forming, SET, and data retention of conductive-bridge random-access memory for stack optimization, *IEEE Trans. Electron. Dev.* 62 (11) (2015) 3482–3489, <https://doi.org/10.1109/TED.2015.2476825>.
- [61] S. Aldana, et al., Kinetic Monte Carlo analysis of data retention in Al:HfO₂-based resistive random access memories, *Semicond. Sci. Technol.* 35 (2020), 115012, <https://doi.org/10.1088/1361-6641/abb072>.
- [62] C. Yakopcic, et al., Generalized memristive device SPICE model and its application in circuit design, *IEEE Trans. Comput. Des. Integr. Circuits Syst.* 32 (8) (2013) 1201–1214, <https://doi.org/10.1109/TCAD.2013.2252057>.
- [63] S. Kvatinsky, et al., *IEEE Trans. Circuits Syst. I Regul. Pap.* 60 (1) (2013) 211–221, <https://doi.org/10.1109/TCSI.2012.2215714>.
- [64] S. Kvatinsky, et al., TEAM: ThrEshold adaptive memristor model, *IEEE Trans. Circuits Syst. II Express Briefs* 62 (8) (2015) 786–790, <https://doi.org/10.1109/TCSII.2015.2433536>.
- [65] K. Eshraghian, et al., Memristive device fundamentals and modeling: applications to circuits and systems simulation, *Proc. IEEE* 100 (6) (2012) 1991–2007, <https://doi.org/10.1109/JPROC.2012.2188770>.
- [66] L. Chua, Resistance switching memories are memristors, *Appl. Phys. A* 102 (2011) 765, <https://doi.org/10.1007/s00339-011-6264-9>.
- [67] E. Miranda, et al., Fundamentals and SPICE Implementation of the Dynamic Memdiode Model for Bipolar Resistive Switching Devices”, *Techrxiv*, 2020 <https://doi.org/10.36227/techrxiv.12479426.v1>.
- [68] F.L. Aguirre, et al., SPICE implementation of the dynamic memdiode model for bipolar resistive switching devices, *Micromachines* 13 (2022) 330, <https://doi.org/10.3390/mi13020330>.
- [69] F.L. Aguirre, et al., Fast fitting of the dynamic memdiode model to the conduction characteristics of RRAM devices using convolutional neural networks, *Micromachines* 13 (11) (2022) 2002, <https://doi.org/10.3390/mi13112002>.
- [70] F.L. Aguirre, et al., SPICE simulation of RRAM-based cross-point arrays using the dynamic memdiode model, *Front. Phys.* 9 (2021) 548, <https://doi.org/10.3389/fphy.2021.735021>.
- [71] J. Suñé, et al., Point contact conduction at the oxide breakdown of MOS devices, in: *International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, 1998, pp. 191–194, <https://doi.org/10.1109/IEDM.1998.746318>. San Francisco, CA, USA.
- [72] E. Miranda, et al., Model for the resistive switching effect in HfO₂ MIM structures based on the transmission properties of narrow constrictions, *IEEE Electron. Device Lett.* 31 (2010) 609, <https://doi.org/10.1109/LED.2010.2046310>.
- [73] S. Datta, *Electronic Transport in Mesoscopic Systems*, first ed., Cambridge University Press, 1997, 9780521599436.
- [74] A. Rodriguez-Fernandez, et al., Switching voltage and time statistics of filamentary conductive paths in HfO₂-based ReRAM devices, *IEEE Electron. Device Lett.* 39 (5) (2018) 656–659, <https://doi.org/10.1109/LED.2018.2822047>.
- [75] M. Maestro-Izquierdo, et al., A new perspective towards the understanding of the frequency-dependent behavior of memristive devices, *IEEE Electron. Device Lett.* 42 (2021) 565, <https://doi.org/10.1109/LED.2021.3063239>.