**Discover** Nano

Discover

Research

# Reconfigurable frequency multipliers based on graphene field-effect transistors

**A. Toral-Lopez[1] · E. G. Marin[1] · F. Pasadas[1] · M. D. Ganeriwala[1] · F. G. Ruiz[1] · D. Jiménez[2] · A. Godoy[1]**

Received: 15 June 2023 / Accepted: 4 August 2023
Published online: 05 October 2023


**Abstract**
Run-time device-level reconfigurability has the potential to boost the performance and functionality of numerous circuits beyond the limits imposed by the integration density. The key ingredient for the implementation of reconfigurable electronics lies in ambipolarity, which is easily accessible in a substantial number of two-dimensional materials, either by contact engineering or architecture device-level design. In this work, we showcase graphene as an optimal solution to implement high-frequency reconfigurable electronics. We propose and analyze a split-gate graphene field-effect transistor, demonstrating its capability to perform as a dynamically tunable frequency multiplier. The study is based on a physically based numerical simulator validated and tested against experiments. The proposed architecture is evaluated in terms of its performance as a tunable frequency multiplier, able to switch between doubler, tripler or quadrupler operation modes. Different material and device parameters are analyzed, and their impact is assessed in terms of the reconfigurable graphene frequency multiplier performance.

**Keywords** Graphene · Split gate · Frequency multiplier · Reconfigurable · Radio frequency · High frequency · Field-effect transistor

## Introduction

Leveraging ultra-high carrier mobility and saturation velocity, graphene has been, along the last two decades, extensively investigated as an outstanding alternative for high-frequency (HF) electronics, showing almost on par performance with cutting-edge III–V technologies [1]. Its striking transport properties are complemented by its inherent carrier ambipolarity, exhibited by a V-shaped transfer characteristics around the Dirac voltage. The combination of these features in the same material opens the path to the exploration and conception of novel HF designs able to greatly simplify and overcome conventional circuits.

One of the most suited and, at the same time, unexplored HF modules that could harness graphene properties are frequency multipliers. A frequency multiplier is a device/circuit that, under ideal operation, generates a single-frequency harmonic at a desired multiple of the frequency of an input signal. The physical implementation of this function is not straightforward and relies upon the nonlinear characteristic of a device which distorts the input signal, generating a

**Supplementary information** The online version contains supplementary material available at (https://doi.org/10.1186/s11671-023-03884-8).

✉ A. Toral-Lopez, atoral@ugr.es; A. Godoy, agodoy@ugr.es | [1]Dpto. Electrónica y Tecnología de Computadores, Facultad de Ciencias, Universidad de Granada, Granada, Spain. [2]Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona, Bellaterra, Spain.

spectrum of harmonics, which are later band-pass filtered. State-of-the-art frequency multipliers are mostly based on Schottky diodes with relatively high efficiencies but lacking amplification and with limited frequency selectivity [2]. Although the continuous technological optimization, both at the device architecture and at the III-V material quality, has pushed the operation of III-V diode-based frequency multipliers to the frontiers of the THz realm [3], novel concepts, exploiting distinct physics and designs, are susceptible to become game changers for the HF field in the hundreds of GHz [4] and THz ranges [5].

Graphene field-effect transistors (GFETs) exhibit the potential ingredients to break through the limitations of Schottky diodes and have indeed proved to be a good test bed to implement frequency doublers [6] reaching frequencies in the GHz range [7–9]. The series connection of two GFETs with conveniently tuned Dirac points has also been demonstrated as a powerful design to obtain higher harmonics such as triplers [10, 11] and quadruplers [12, 13] with notable conversion efficiencies. The main idea is to combine several V-shaped ambipolar transfer characteristics to attain a W-shaped response, which properly adjusted produces the required nonlinearity to generate the desired output harmonic. The physical implementation of this W-shaped characteristic can be achieved under different device architectures: (i) at the circuit-design level, connecting several independent GFETs, or (ii) more interestingly, at the device-design level, using independent gates to control the same channel and selectively adjust the device operation mode [14]. This latter case involves the additional appealing concept of extending the device functionality, i.e., reconfiguring the device beyond the implementation of a single function, aiming to get a higher functional density with a constant integration density [15].

In this regard, the combination of a back- and top-gate is the most employed configuration [12]. However, it has demonstrated a limited frequency performance due to the large parasitic capacitance originated by the global back-gate [13]. To overcome this serious drawback, we propose and analyze a split-gate GFET architecture able to perform as a reconfigurable frequency multiplier generating ×2, ×3 or ×4 harmonics of the input signal, with electrically controllable frequency reconfigurability under operating conditions. The analysis is carried out making use of a physically based simulator that includes a detailed description of the channel material through its density of states (DoS) integrated in the time-dependent transport equation [16–18], considering both, DC and transient analysis.

The rest of the paper is organized as follows: first, discusses the ideal response that can be expected from frequency multipliers, and its resemblance with the W-shaped transfer characteristic obtained in GFETs by tuning the Dirac voltage, is discussed; next, the numerical simulator is described and validated through comparison with experimental results; then, the main outcomes of this study are presented, followed by the conclusions extracted from them.

## Response of ideal frequency multipliers

The theoretical expression for ideal frequency multiplication, i.e., single-harmonic generation from a sinusoidal input, is a polynomial function where the eventual multiplication factor is determined by the order of the polynomial (see Supporting Information for details). For the case of frequency doubling, tripling and quadrupling, one can find a good resemblance in the shape of these ideal functions with different regions of a W-shaped function (see Fig. 1).

This W shape can, indeed, be achieved as the addition of two shifted quadratic responses, which is the ideal relationship between gate bias ($V_{gs}$) and drain current ($I_{ds}$) in GFETs, and a constant factor, which would correspond to a bias-independent conductive region or element connecting the two hypothetical GFETs. The resulting W-shaped response, and, to a good level of approximation, the series association of two GFETs (or any other architecture emulating this association), can thus be analytically described by the following expression:

$$w(x) = \left[\frac{1}{\beta_0(x-\alpha_0)^2+\gamma_0} + \frac{1}{\beta_1(x-\alpha_1)^2+\gamma_1} + \frac{1}{\gamma_2}\right]^{-1} \tag{1}$$

where $\alpha_0$ and $\alpha_1$ correspond to the position of the first and second minima (i.e., the Dirac voltages of the two GFETs ); $\beta_0$ and $\beta_1$ set the curvature of each parabola (i.e., the transconductance of the GFETs); and $\gamma_0$ and $\gamma_1$ are a vertical shift of each parabola (i.e., they set the minimum conductivity at the Dirac voltages), while $\gamma_2$ is a constant factor (i.e., the conductance of the element connecting both GFETs). Note that, from a circuit theory perspective, Eq. (1) just puts down a series association of three conductive regions, that would in principle correspond to two channels of graphene connected by a constant conductivity region.

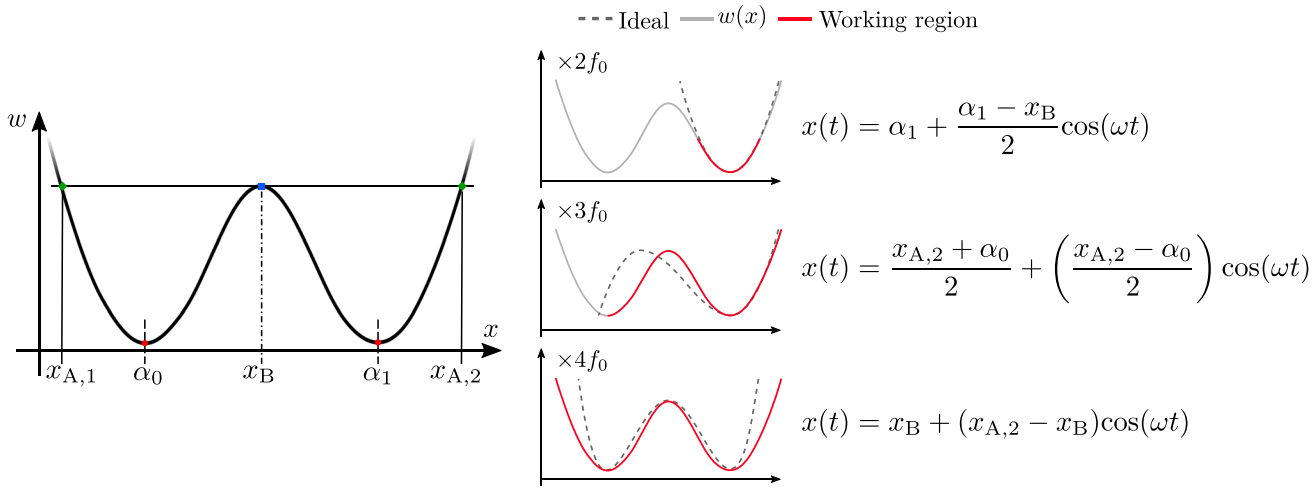


**Fig. 1** Comparison of the W-shaped profile of Eq. (1) (gray lines) and the ideal profiles (dashed lines) for the ×2, ×3 and ×4 frequency multiplication. The corresponding working regions of $w(x)$ to obtain each frequency multiplication factors are indicated in red, along with the corresponding input signals to operate in each region $x(t)$. These expressions for the input signals depend on the five main parameters of $w(x)$ indicated at the bottom part of the figure.

Figure 1 shows the comparison between the W-shaped function (solid light gray) in Eq. (1) and the ideal theoretical response for ×2, ×3 and ×4 frequency multiplication (dashed lines). Depending on the desired response, a different working region of $w(x)$ (solid red) must be selected by modifying the bias and amplitude of the input signal $x(t)$. The actual amplitude and bias values of the input signals for frequency doubling, tripling and quadrupling are defined in Fig. 1.

The frequency spectra (see Additional file 1) of the different curves demonstrate the appropriateness of $w(x)$ to generate the required frequency multiplication, with a slightly smaller amplitude than the ideal response and with some small-amplitude spurious at integer multiples of the input frequency.

## Numerical simulation scheme and validation

In order to move the theoretical discussion to a practical design, and more interestingly, to devise new concepts and architectures able to exploit graphene for frequency multiplication, it is necessary to determine to what extent the actual response of the GFETs is able to emulate the ideal W shape in Eq. (1). To this purpose, we exploit a simulation suite that encompasses the self-consistent solution of the Poisson equation along with the time-dependent continuity equation under a semiclassical dissipative umbrella, a reasonable approach considering typical device sizes. The range of applicability of the presented model is limited to the appearance of propagating electromagnetic waves in the device and the necessary consideration of the complete form of time-dependent coupled Maxwell equations. The electrostatic potential and the charge density profile in a 2D cross-section of the structure are related through the Poisson equation:

$$\nabla \cdot \left(\varepsilon \, \vec{\nabla} V\right) = -\rho \tag{2}$$

where $\varepsilon$, $V$ and $\rho$ are the permittivity, potential and charge distribution, respectively. All of them are defined in the XY plane, and the structure is considered invariant along the $z$-axis. The term $\rho$ includes the fixed charge associated with impurities as well as mobile carriers, i.e., electrons and holes. The time-dependent continuity equation is written as:

$$\nabla \cdot \left(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}\right) = 0 \tag{3}$$

where $\mathbf{D}$ is the electric displacement field and $\mathbf{J}$ the current density along the channel, expressed in terms of the Fermi-level gradient as [19]: $J = (\mu_n n + \mu_p p)\nabla E_F$, where $\mu_n$ ($\mu_p$) is the electron (hole) mobility dependent on the longitudinal electric field [20], and $n$ ($p$) the electron (hole) carrier densities. The Fermi level is solved using the continuity equation and combined with the conduction and valence band profiles to self-consistently evaluate the surface carrier densities as:

$$n(x) = \int \mathrm{DoS}_n(E) f_{FD}(E_D(x) - E_F(x)) dE$$
$$p(x) = \int \mathrm{DoS}_p(E) \left[1 - f_{FD}(E_D(x) - E_F(x))\right] dE \quad (4)$$

where $\mathrm{DoS}_n$ ($\mathrm{DoS}_p$) is the conduction (valence) band DoS, $f_{FD}$ the Fermi–Dirac function, and $E_D$ stands for the Dirac energy determined by the electrostatic potential obtained solving the Poisson equation. The DoS profiles can be provided by either external *ab-initio* calculations or theoretical expressions such as the graphene linear DoS profile: $\mathrm{DoS} = q^2 2|E|/\pi(\hbar v_F)^2$, where $v_F = 10^8$ cm/s is the Fermi velocity in graphene. The values for $E < 0$ correspond to $\mathrm{DoS}_p$, while $E > 0$ to $\mathrm{DoS}_n$. For stationary simulations, we solve the same self-consistent set of equations, neglecting the term $\frac{\partial D}{\partial t}$ in Eq. (3). A more detailed description of the iterative scheme and the integration of the equations can be found in the Additional file 1.

To validate the proposed numerical approach, we make use of the data provided in Ref. [6], where a graphene FET with a $L_{Ch} = 500$ nm-long gate and $L_{Acc,Sc} = L_{Acc,Dr} = 500$ nm-long source and drain access regions was fabricated (see Fig. 2), with the graphene layer deposited on a $SiO_2$ substrate and a $Y_2O_3$ layer as gate insulator, with $t_{ox} = 5$ nm. Notably, the experimental circuit is rather clear and simple, enabling the direct comparison with the measurements with minimal post-processing of the numerical simulation outputs, avoiding complex de-embedding procedures that could complicate the study of the single device response and thus impact in the soundness of the validation. The experimental topology included a series resistor ($R_o$), as shown in the upper section of Fig. 2, emulated in the numerical simulations with a $L_R = 500$ nm-long additional region of constant conductivity. The resistance value of this region is given by $R_o|_{Sim.} = \int_{L_R} \frac{dx}{q\mu_R(n+p)}$ where $\mu_R = 140$ cm$^2$/Vs was set to achieve a $R_o|_{Sim.} \approx 9$kΩ, mimicking the experimental resistance value.

We first focused on the experimental transfer characteristic, represented as a dashed line in Fig. 3a. We tuned the carrier mobilities in the channel ($\mu_n = \mu_p = 465$ cm$^2$/Vs), the residual carrier density due to puddles ($N_{puddles} = 11.8 \cdot 10^{11}$ cm$^{-2}$) and the carrier mobility in the resistive region. The dielectric constant of the gate insulator and the difference between the metal-gate and graphene work function $q(\phi_m - \chi_{gr})$ were set to 12.6 $\varepsilon_0$ and −0.375 eV, respectively. The result of the fitting is depicted as solid line in Fig. 3a, proving the capability of the numerical simulator to reproduce the electrical response of the device.

Once the DC behavior was assessed, we dealt with time-dependent simulations to reproduce the experiments carried out with a 10 kHz input signal and 400 mV of amplitude, employing the same tuned parameters. The experimentally obtained output waveform and its spectrum are depicted in Fig. 3b (red) jointly with the simulated signal (blue). A very good agreement is achieved between both signals, with the amplitude of the × 2 harmonic clearly outperforming the rest of components in the output spectra shown in Fig. 3c, stressing the capability of the approach here developed to reproduce the experimental response.

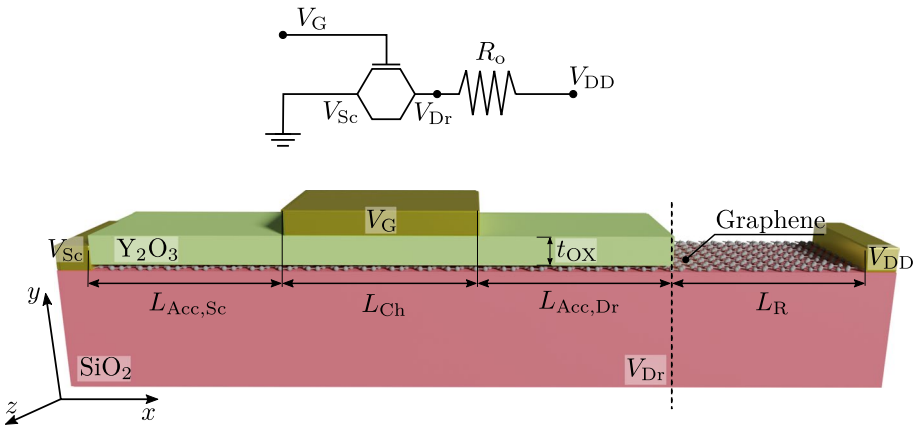


**Fig. 2** Device used to validate the simulator from the experimental data in Ref. [6]. An underlap graphene region has been included to model a series resistor $R_o$ with the aim of reproducing the same circuit used in its characterization (top panel)

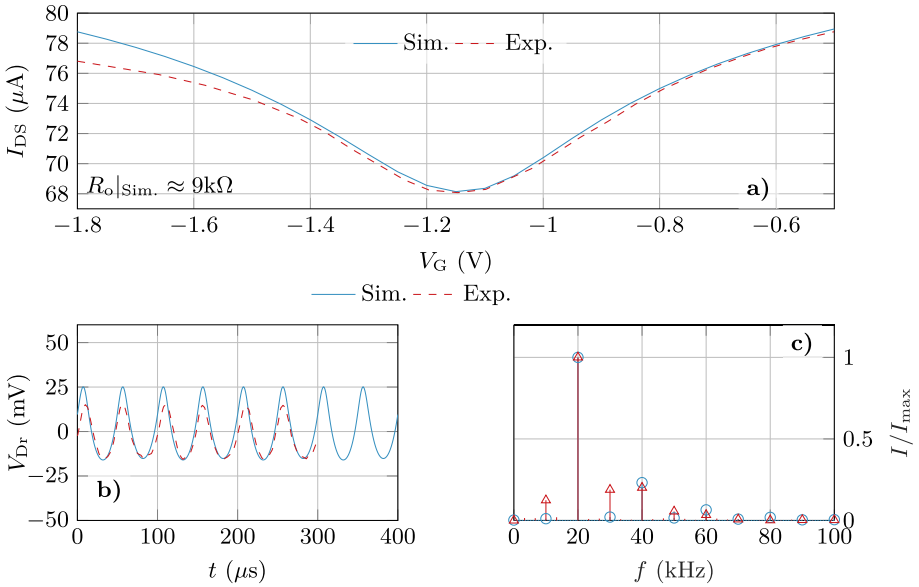


**Fig. 3** **a** Comparison of the experimental $I_{DS} - V_G$ characteristic [6] (dashed) with the numerical one (solid) for the device in Fig. 2. **b** Experimental (red) and computed (blue) output ($V_{Dr}$) obtained for a 10kHz input signal applied on the gate and **c** their spectra normalized by the maximum achieved at $f = 20$ kHz

## Results and discussion

Next, we assessed the capabilities of GFETs to emulate the ideal W-shaped transfer characteristic and therefore to perform as frequency multipliers. To this aim, we propose a novel architecture based on a split-gate configuration where the quadratic conductance of the GFETs is exploited in combination with a controlled Dirac voltage shift (DVS) [16].

The structure is depicted in Fig. 4, and it comprises a single graphene layer deposited on top of a $SiO_2$ substrate. The graphene is partially covered by a split gate with two contacts ($V_{G1}$ and $V_{G2}$), both with length $L_G = 115$ nm, each of them located at one edge of the graphene layer. The gate metals underlap a $Y_2O_3$ insulating layer of thickness $t_{OX} = 20$ nm and length 135 nm (resulting in two $L_{Acc}$= 10 nm long underlapped access regions at both sides of each gate). The split-gate configuration gives rise to two channels controlled by two independent gates and connected in series through an extended graphene layer of $L_R = 530$ nm. The conductivity of this region is not modulated by any gate (i.e., there is not back-gate in the proposed architecture), and it acts as a resistor causing a voltage drop between the drain of the first channel and the source of the second. This potential drop results in a distinct DVS at each graphene channel, determined by the corresponding drain and source biases [21], giving rise to the W shape.

Figure 5 depicts the transfer characteristic of the split-gate architecture for $V_{G1} = V_{G2} = V_{GS}$, and three values of $V_{DS}$: 0.5V (blue), 1V (red) and 1.5V (green). The $I_{DS} - V_{GS}$ characteristics depict two minima, indicating that the split-gate GFET results in distinct DVS in the two channels. In order to assess its resemblance with the theoretical W shape, the curves were fitted with the function $I_{DS} = w(V_{GS})$ in Eq. (1), with $\alpha_0 = V_{Dirac,1}$ and $\alpha_1 = V_{Dirac,2}$, and tuning $\beta_0$, $\beta_1$, $\gamma_0$, $\gamma_1$ and $\gamma_2$, for each $V_{DS}$. The resulting values are summarized in Table 1. The symmetry of both channels is evidenced by the similarity of $\beta_0$ and $\beta_1$ as well as $\gamma_0$ and $\gamma_1$. As can be observed, $V_{DS}$ directly affects the Dirac voltage values ($V_{Dirac,1}$ and $V_{Dirac,2}$) and their difference. The later can, indeed, be adjusted with $V_{DS}$, which sets an upper limit to $V_{Dirac,\,2} - V_{Dirac,\,1}$. Unfortunately,

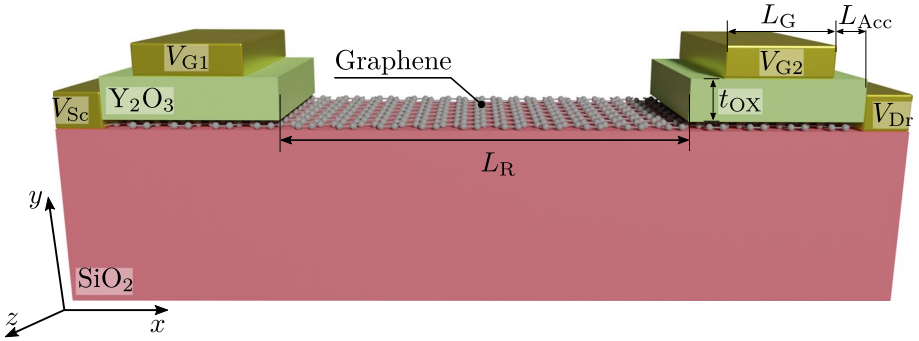


**Fig. 4** Structure used to implement the frequency multiplier defined by two channels serially connected by an intermediate uncontrolled region. The geometry of the device is defined by $L_R = 530$ nm, $L_G = 115$ nm, $L_{Acc} = 10$ nm and $t_{OX} = 20$ nm.

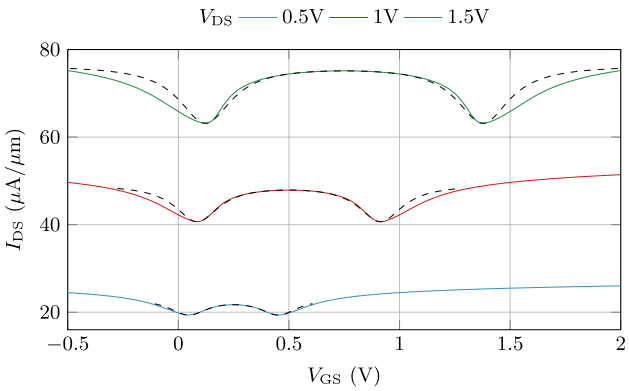


**Fig. 5** $I_{DS} - V_{GS}$ characteristics of the split gate device for three different $V_{DS}$ values and $V_{GS} = V_{G1} = V_{G2}$. The black dashed lines indicate the fitting with the function $w(V_{GS})$, with $\alpha_0 = V_{Dirac,1}$ and $\alpha_1 = V_{Dirac,2}$

**Table 1** Values of the parameters used to fit the transfer characteristics shown in Fig. 5 using the function $w(x)$

| $V_{DS}$ | $\beta_0$ | $\gamma_0$ | $V_{Dirac,1}$ | $\beta_1$ | $\gamma_1$ | $V_{Dirac,2}$ | $\gamma_2$ |
|---|---|---|---|---|---|---|---|
| 0.5V | 8.62 | 0.081 | 0.046V | 8.79 | 0.081 | 0.453V | 15.64 |
| 1V | 8.18 | 0.099 | 0.085V | 8.25 | 0.1 | 0.914V | 20.57 |
| 1.5V | 5.44 | 0.095 | 0.122V | 5.47 | 0.095 | 1.377V | 19.78 |

$V_{DS}$ also impacts in the shape of the W (as revealed by the variations in $\beta_i$ and $\gamma_i$) generating a notable change in the device output current. Figure 5 proves the limitations for a proper W-shaped generation by solely varying the DVS of both channels through $V_{DS}$.

An alternative method to control the position of both Dirac points (and to generate the W shape) with a lower impact in the output current is to independently bias each gate. A gate bias difference ($\Delta V_G = V_{G2} - V_{G1}$) directly translates into different DVS in both channels, as if they would have distinct metal work functions [21]. With this methodology, one can expect a controlled change in the position of both Dirac points with a lower impact in the output current. Indeed, $\Delta V_G$ can be interpreted as an electrically *operando* reconfiguration knob, converting the split-gate GFET architecture in a reconfigurable device able to implement different frequency multiplication factors as we will discuss in the following.

First, in order to assess the capability of $\Delta V_G$ to generate a W-shaped response in the split-gate GFET architecture, we have calculated the $I_{DS} - V_{G1}$ characteristics for different values of $\Delta V_G$, spanning in a range from −0.5 V to +0.5 V, and for three different $V_{DS}$ values: 0.5 V, 1 V and 1.5 V, respectively. The results are depicted in Fig. 6 indicating that for a fixed $V_{DS}$ value, $\Delta V_G$ provides a large tunable adjustment of the DVS without incurring in a substantial variation of the

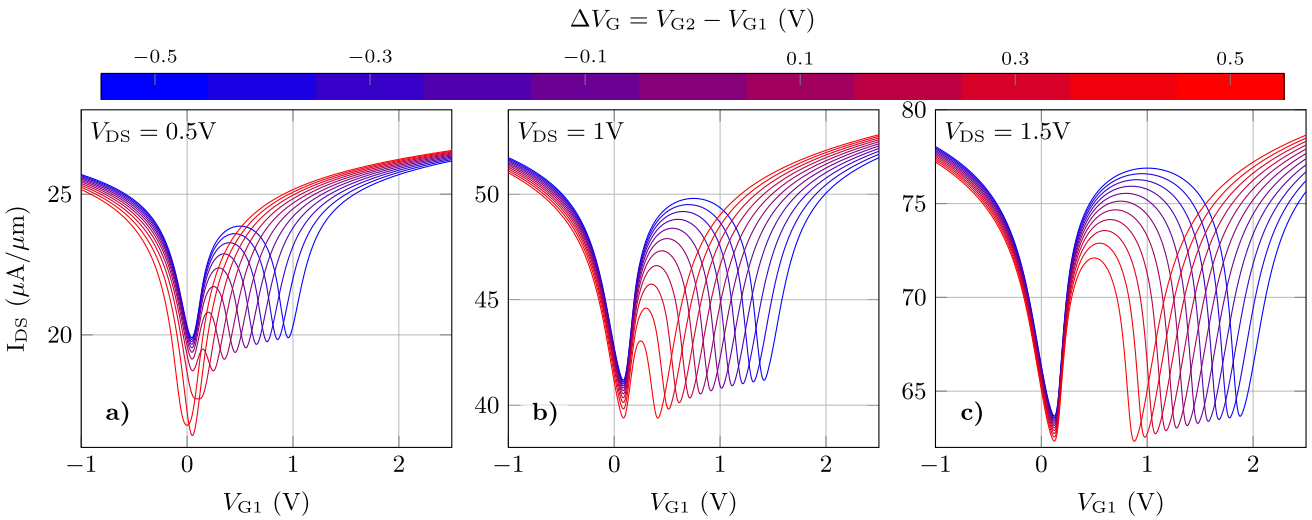


**Fig. 6** $I_{DS} - V_{G1}$ characteristics of the device for three different $V_{DS}$ values: **a** 0.5 V, **b** 1 V, **c** 1.5 V, as a function of the control bias $\Delta V_G$. For each curve, $V_{G2}$ corresponds to $V_{G1}$ plus a constant value $\Delta V_G$ according to the upper color bar

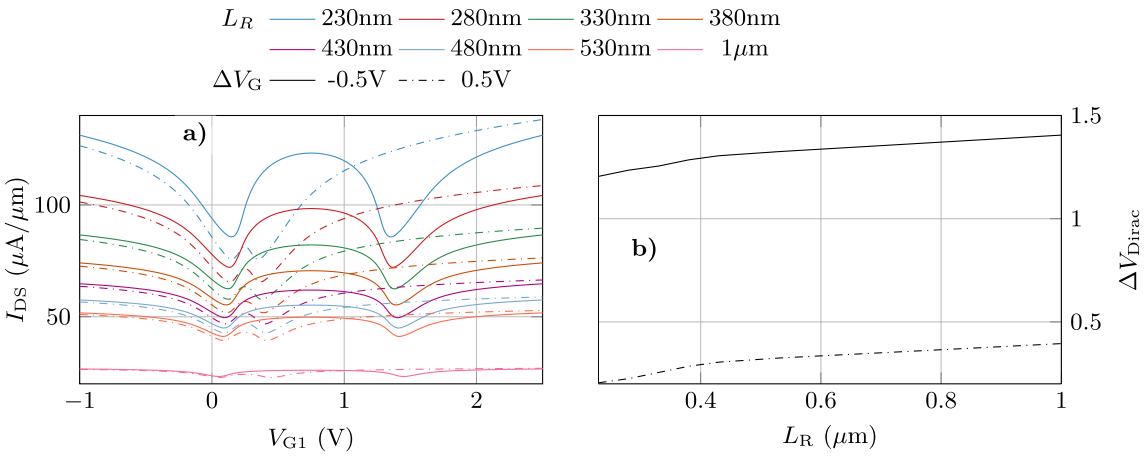


**Fig. 7** **a** $I_{DS} - V_{G1}$ for different lengths of the intermediate region $L_R$ for two different values of $\Delta V_G$, −0.5 V (solid) and 0.5 V (dot-dashed), and a constant $V_{DS} = 1$V. **b** $\Delta V_{Dirac} = V_{Dirac,1} - V_{Dirac,2}$ *vs* $L_R$

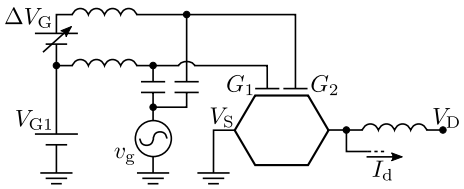


**Fig. 8** Setup employed to analyze the frequency performance of the split-gate GFET. Two independent DC voltage sources, $V_{G1}$ and $\Delta V_G$, are used to set the bias point and the $I - V$ characteristic, and a small-signal source $v_g$ feeds both gates

current. In more detail, $\Delta V_G$ is able to increase the distance between both minima well above the applied $V_{DS}$, which is the upper limit achieved in Fig. 5. The current values at both minima differ moderately for the lowest $V_{DS} = 0.5$ V, but they are almost equal for $V_{DS} = 1.5$ V. Interestingly, the Dirac voltages become closer when $\Delta V_G$ approaches to the applied $V_{DS}$ bias, and notably, it is even possible to merge both minima with an appropriate value of $\Delta V_G = V_{DS}$, as illustrated in the case $V_{DS} = 0.5$ V. This feature becomes attractive for switching from a W shape to V shape, namely the *operando* change of the frequency multiplication between $\times 4f_{in}$ and $\times 2f_{in}$.

The graphene region connecting both channels also plays a key role in the controlled separation between both Dirac points and the W shape generation. In order to gain insights into this point, we extend the analysis of the transfer function to assess the impact of $L_R$ on the device characteristics. Figure 7 shows $I_{DS} - V_{G1}$ for two $\Delta V_G$ values, −0.5 V (solid) and 0.5 V (dashed), and $V_{DS} = 1$V, for different values of $L_R$ in a range from 230 nm to 1 $\mu$m. The output current is clearly impacted by $L_R$, as the resistance of this intermediate region scales up with the length. In other words, a lower resistance in this region (lower $L_R$) improves the overall conductivity of the structure, enabling a higher output current. A slight variation in the separation of the minima ($\Delta V_{Dirac} = V_{Dirac,1} - V_{Dirac,2}$) as a function of $L_R$ is shown in Fig. 7b. This effect might be related to the impact of the diffusion length at the edge of the channels [22]. For $L_R < 0.4$ $\mu$m, the potential and charge distribution of the channels has a significant influence on the intermediate region. This in turn involves a higher modulation of the $V_{DS}$ bias of the channels, providing a large variation of their Dirac points.

*Time-dependent simulations*

Once the DC characteristics of the device have been analyzed, we perform time-dependent simulations to assess its AC response when a sinusoidal signal is used as input. This study is carried out making use of the setup depicted in Fig. 8, with two independent DC gate biases used to select the device working region and an AC input signal $v_g$ feeding both gates simultaneously.

We assume $V_{DS} = 1$V, while $\Delta V_G$ is swept from −0.5 V to +0.5 V, and $V_{G1}$ is tuned to be centered in the mid-point between $V_{Dirac,1}$ and $V_{Dirac,2}$, e.g., for $\Delta V_G = 0.5$ V, $V_{G1} \simeq 0.25$ V as shown in Fig. 6b. For that polarization, an AC input signal is applied to the gates with frequency $f_{in} = 1$MHz and the required amplitude to operate as a frequency quadrupler as indicated in Fig. 1. Figure 9a shows the drain current as a function of time for different $\Delta V_G$ biases, and Fig. 9b and c their corresponding frequency spectrum with the different normalized harmonic amplitudes. As expected, the device output shows a main harmonic at $\times 4f_{in}$. It must also be stressed the noticeable contribution of the $\times 2f_{in}$ harmonic, which lays < 5

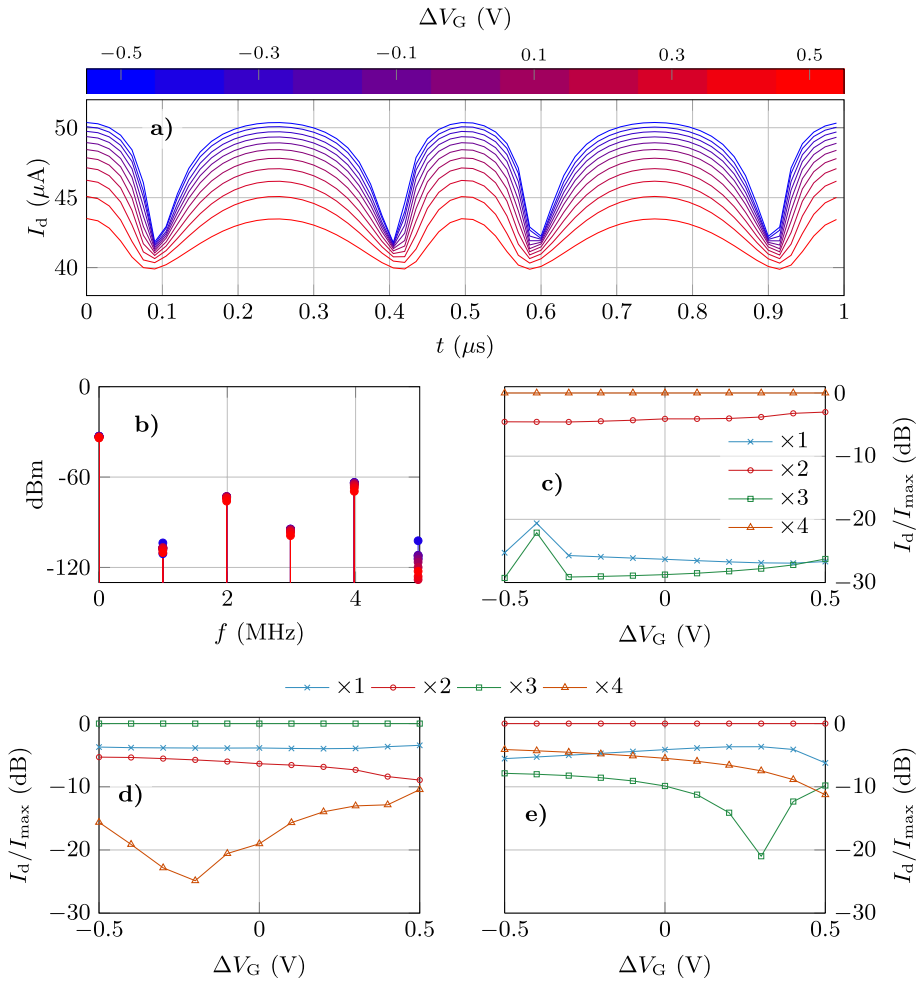


**Fig. 9** **a** Transient output current for a constant $V_{DS}$ = 1V, for ten different values of $\Delta V_G$ ranging from −0.5V to +0.5V and $V_{G1}$ at the mid-point between the Dirac points. **b** Output power spectrum for a 1MHz sinusoidal input ($v_g$) assuming a 50Ω load. **c** Normalized amplitude of the output harmonics as a function of $\Delta V_G$ when the device operates as a frequency tripler **d** and as a frequency doubler **e**

dB below the main tone (×4$f_{in}$). The device response agrees with the theoretical prediction (Additional file 1), and it is a result of the capability of the split-gate architecture to reproduce the ideal W behavior. Regarding the impact of $\Delta V_G$ on the spectral purity, the contribution of the ×2$f_{in}$ harmonic is slightly reduced as $\Delta V_G$ becomes more negative, while the odd harmonics (with a notable smaller amplitude) increase. Therefore, the $\Delta V_G$ makes possible to modify the weight of the different harmonics. This feature is shown in Fig. 9d and e, where the split-gate is configured to operate as a tripler (Fig. 9d) or as a doubler (Fig. 9d). In each case, the third and second harmonic, respectively, becomes dominant, with some modulation of the relative amplitudes of the rest of harmonics with $\Delta V_G$. The operation of the split-gate GFET as a frequency doubler and tripler is discussed in more detail in Additional file 1, proving that the device can be reconfigured to operate as an efficient doubler or tripler through the control of $V_{G1}$ and $\Delta V_G$.

*Operation frequency*

Once the AC operation of the split-gate GFET as a reconfigurable frequency multiplier has been assessed, we proceed with a prospective study of the maximum operation frequency achievable by the device. We focus on the quadrupler, as it is the scenario where the limitation would be more critical. We assume $V_{DS}$ = 1V and $\Delta V_G$ = 0.5 V, although similar conclusions could be drawn for different values of both biases. $V_{G1}$ is set at the mid-point between both Dirac points, and the frequency of $v_g$ is swept in a range from 1 MHz to 10 GHz, while its amplitude is kept as in Fig. 9. The obtained output spectrum is depicted in Fig. 10a, b for the first four harmonics normalized to the maximum for different frequencies.

While the ×4 harmonic is still dominant for sub-GHz frequencies, the contribution of the input frequency $f_{in}$ in the device output increases exponentially, reaching the ×4 harmonic at $f_{in}$ = 1GHz and becoming dominant for $f_{in}$ = 10 GHz. This is due to the capacitive leaking through the gate insulator of the AC signal and gives insights about the maximum input frequency for a proper operation of the frequency multiplier. It is worth to note that this limit is uniquely determined by the gate oxide stack and might be improved reducing the capacitive coupling. Moreover, the relative contribution of the displacement and diffusion current is also impacted by the carrier mobility. Figure 10c shows the frequency spectrum

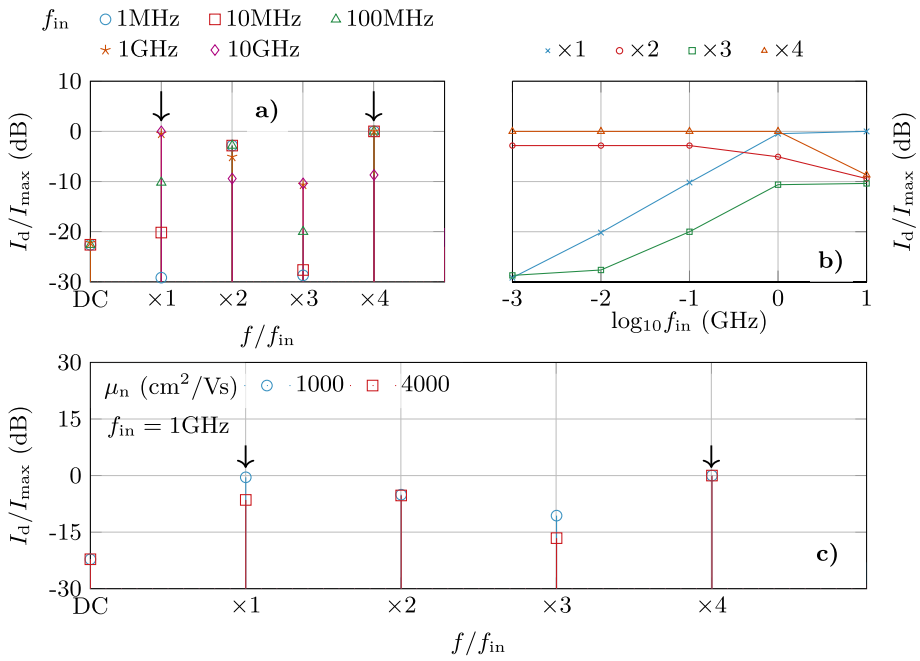


**Fig. 10** **a** and **b** Output spectrum for different $f_{in}$ and $\Delta V_G = 0.5$ V. **c** Variation of the first four harmonics when the electron mobility increases for $f_{in} = 1$GHz

at $f_{in} = 1$GHz for two different values of symmetrical electron/hole mobilities: 1000 cm$^2$/Vs and 4000 cm$^2$/Vs ($\mu_n = \mu_p$). The results demonstrate that the contribution of the $\times 4 f_{in}$component in the output is raised with an increasing mobility, resulting in 6.5 dB gain with respect to the $\times 1$harmonic that was similar in amplitude for the lower mobility of 1000 cm$^2$ /Vs. Notably, an improved mobility also reduces the $\times 3$ harmonic amplitude.

## Conclusions

A split-gate graphene FET architecture is presented as a reconfigurable frequency multiplier, leveraging the addition of two ambipolar quadratic $I - V$ characteristics. The split-gate GFET operation is thoroughly analyzed and its performance as reconfigurable frequency doubler, tripler and quadrupler is assessed in terms of the output spectra. It is demonstrated that the selection of the appropriate bias point on both independent gates results on the dynamic reconfiguration of the device operation. Moreover, the impact of the diffusive and displacement currents is discussed, proving the beneficial effect that an improved carrier mobility produces on the maximum operating frequency achievable by the device. The frequencies of these devices are still lower than the current off-the-shelf technologies. However, graphene is still a teenage material in a non-mature technological stage, with large potential for improvement and eventually overcome well-established semiconductors. This work adds to those demonstrating that beyond direct comparison of RF performance, graphene technology enables single-device implementation of complex nonlinear responses. The proposed architecture opens the path to the exploration of novel designs exploiting unmatched graphene ambipolarity and its inherent high-mobility in reconfigurable high-frequency electronics.

**Acknowledgements** Not applicable.

**Author contributions** ATL, EGM, FP, FGR and AG contributed to the conception of the study. ATL carried out the simulations, and MG and ATL contributed to the data analysis. ATL, EGM, FP, FGR, DJ and AG wrote the first draft of the manuscript, and all the authors contributed to writing the final document prior to the submission.

**Funding** This work is part of the research project P21_00149 ENERGHENE funded by Consejería de Universidad, Investigación e Innovación de la Junta de Andalucía. This work is also supported by FEDER/Junta de Andalucía - Consejería de Transformación Económica, Industria, Conocimiento y Universidades through the projects P20-00633 and A-TIC-646-UGR20, by Spanish Government through projects PID2020-116518GB-I00 funded by MCIN/AEI/10.13039/501100011033 and TED2021-129769B-I00 funded by MCIN/AEI/10.13039/501100011033 and the European Union NextGenerationEU/PRTR. F. Pasadas acknowledges funding from PAIDI 2020 and the European Social Fund Operational Programme 2014-2020 no. 20804. M. D. Ganeriwala acknowledges funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 101032701.

**Data availability** The output data of the simulations carried out on this work are available from the corresponding author under reasonable request.

## Declarations

**Competing interests** There are no conflicts of interest declared by any author of this work.

**Code availability** The source code is available upon reasonable request from the corresponding author.



## References

1. Norhakim N, Hawari HF, Burhanudin ZA. Assessing the figures of merit of graphene-based radio frequency electronics: a review of GFET in RF technology. IEEE Access. 2022;10:17030–42.
2. Wang H, Nezich D, Kong J, Palacios T. Graphene frequency multipliers. IEEE Electron Device Lett. 2009;30(5):547–9.
3. Mehdi I, Siles JV, Lee C, Schlecht E. THz diode technology: status, prospects, and applications. Proc IEEE. 2017;105(6):990–1007.
4. Ver Hoeye S, Hadarig A, Vazquez C, Fernandez M, Alonso L, Heras FL. Submillimeter wave high order frequency multiplier based on graphene. IEEE Access. 2019;7:26933–40.
5. Lerer AM, Makeeva GS, Cherepanov VV. Electronically tunable broadband THz frequency multipliers based on multilayer nonlinear graphene metasurfaces. In: 2020 international conference on actual problems of electron devices engineering (APEDE). IEEE, 2020.
6. Wang Z, Zhang Z, Huilong X, Ding L, Wang S, Peng L-M. A high-performance top-gate graphene field-effect transistor based frequency doubler. Appl Phys Lett. 2010;96(17): 173104.
7. Wang H, Hsu A, Kim KK, Kong J, Palacios T. Gigahertz ambipolar frequency multiplier based on CVD graphene. In 2010 international electron devices meeting. IEEE, 2010.
8. Ramón ME, Parrish KN, Chowdhury SF, Magnuson CW, Movva HCP, Ruoff RS, Banerjee SK, Akinwande D. Three-gigahertz graphene frequency doubler on quartz operating beyond the transit frequency. IEEE Trans Nanotechnol. 2012;11(5):877–83.
9. Lv H, Wu H, Liu J, Niu J, Yu J, Huang C, Li J, Xu Q, Wu X, Qian H. Monolithic graphene frequency multiplier working at 10ghz range. In Proceedings of Technical Program—2014 international symposium on vlsi technology, systems and application (VLSI-TSA). IEEE, 2014.
10. Chen H-Y, Appenzeller J. Graphene-based frequency tripler. Nano Lett. 2012;12(4):2067–70.
11. Cheng C, Huang B, Liu J, Zhang Z, Mao X, Xue P, Chen H. A pure frequency tripler based on CVD graphene. IEEE Electron Device Lett. 2016;37(6):785–8.
12. Cheng C, Huang B, Mao X, Zhang Z, Zhang Z, Geng Z, Xue P, Chen H. A graphene based frequency quadrupler. Sci Rep. 2017;7(1):46605.
13. Peng P, Tian Z, Li M, Wang Z, Ren L, Yunyi F. Frequency multiplier based on back-gated graphene FETs with m-shaped resistance characteristics. J Appl Phys. 2019;125(6): 064503.
14. Simon M, Mulaosmanovic H, Sessi V, Drescher M, Bhattacharjee N, Slesazeck S, Wiatr M, Mikolajick T, Trommer J. Three-to-one analog signal modulation with a single back-bias-controlled reconfigurable transistor. Nature Commun. 2022;13(1):7042.
15. Fei W, Trommer J, Lemme MC, Mikolajick T, Heinzig A. Emerging reconfigurable electronic devices based on two-dimensional materials: a review. InfoMat. 2022;4(10): e12355.
16. Toral-Lopez A, Marin EG, Medina A, Ruiz FG, Rodriguez N, Godoy A. GFET asymmetric transfer response analysis through access region resistances. Nanomaterials. 2019;9(7):1027.
17. Toral-Lopez A, Santos H, Marin EG, Ruiz FG, Palacios JJ, Godoy A. Multi-scale modeling of 2D GaSe FETs with strained channels. Nanotechnology. 2021;33(10): 105201.
18. Toral-Lopez A, Kokh DB, Marin EG, Wade RC, Godoy A. Graphene BioFET sensors for SARS-CoV-2 detection: a multiscale simulation approach. Nanoscale Adv. 2022;4(14):3065–72.
19. Champlain JG. A first principles theoretical examination of graphene-based field effect transistors. J Appl Phys. 2011;109(8): 084515.
20. Toral-Lopez A, Pasadas F, Marin EG, Medina-Rull A, Gonzalez-Medina JM, Garcia Ruiz FJ, Jiménez D, Godoy A. Multi-scale analysis of radio-frequency performance of 2D-material based field-effect transistors. Nanoscale Adv. 2021;3(8):2377–82.
21. Pasadas F, Medina-Rull A, Feijoo PC, Pacheco-Sanchez A, Marin EG, Ruiz FG, Rodriguez N, Godoy A, Jimenez D. Unveiling the impact of the bias-dependent charge neutrality point on graphene based multi-transistor applications. Nano Express. 2021;2(3): 036001.
22. Feijoo PC, Jimenez D, Cartoixa X. Short channel effects in graphene-based field effect transistors targeting radio-frequency applications. 2D Materials. 2016;3(2): 025036.