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WAFER BONDING TECHNOLOGIES FOR NANO-, MICRO- AND MACRO-SYSTEM REALIZATION AND INTEGRATION

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ABSTRACT

This paper is providing an overview about most common wafer bonding technologies used for the realization of nano-, micro,- and macro systems and for system integration. At first, the general aspects of wafer bonding applications are discussed. This is followed by the technological description of different wafer bonding processes, since for different bonding applications different processes are required related to process integration and the actual surface layers on the wafers which should be bonded. Finally, benefits and drawbacks as well as technology and application aspects are shown in an overview table, providing systematization and detailed comparison of the described bonding processes. This overview should help to choose the best suitable process for wafer level bonding and other applications.

Index Terms - direct, anodic, glass frit, adhesive, wafer bonding, process integration

1. INTRODUCTION

Wafer bonding is the stacking and joining of semiconductor substrates and is an essential process step in the development and production of MEMS (micro-electrical-mechanical systems) [1]. It provides the possibility to realize real three-dimensional structures, in this technology field where 2D-strutures with fixed thickness are still dominating. Since MEMS technologies are linked to general semiconductor developments towards smaller and smaller structures, wafer bonding processes are entering the nano scale as well. On the other hand, wafer bonding is used for devices, which are utilizing the full wafer area of 6” or 8” in diameter, so macroscopic applications can be addressed as well, for example X-Ray detectors. In addition, the wafer bonding methods can also be applied on bulkier, macro like structures such as optical elements. Actually, nano-, micro-, macro mechanical and electrical elements are required and possible to be bonded at wafer level, this finally allows system integration across functional and geometrical domains. This paper is intended to give a general introduction in various wafer bonding processes and their applications.

2. WAFER BONDING IN MEMS AND 3D INTEGRATION PROCESSES

As mentioned, the main purpose of wafer bonding is the realization of three-dimensional structures in the MEMS and related wafer process. This has two main aspects so far (see also figure 1):

1) Realization of special substrates with buried layers such as oxide and/or implanted layers in SOI wafers or buried structures such as sealed cavities in silicon: These special substrates provide advanced properties for device function and enable new features. For example, dielectrically insulated silicon areas can be realized in SOI wafers, which are important for high voltage applications, modern CMOS technologies in the nanometer nodes as well as for MEMS devices. On the other hand, these types of special substrate provide many technological advantages, and even enable new and efficient technologies. Examples include absolute pressure sensors based on substrates with sealed cavities or an etch stop at the buried oxide of SOI wafers.

2) Capping of MEMS [2] and micro fluidic devices at the end of the wafer process is the other important wafer bonding application. MEMS structures, particularly those of surface micromechanical devices must be protected at the wafer level to prevent destruction by mechanical or environmental influences. Hermetic sealing is also often required as an extra effective protection during dicing and assembly processing, as well as for device lifetime and application. This type of wafer bonding does not only provide protection, but also completes the functionality of the chips. Microfluidic channels must be sealed by caps in order to carry fluids, absolute pressure sensors and resonant structures, such as gyroscopes, require a vacuum in their cavity, while in other sensors, the cap is provided as an electrical shielding or counter electrode. Finally, the cap wafer can contain electrical structures as full application specific ICs (ASICs) for sensor signal conditioning - this allows full sensor system integration on chip level by wafer bonding.

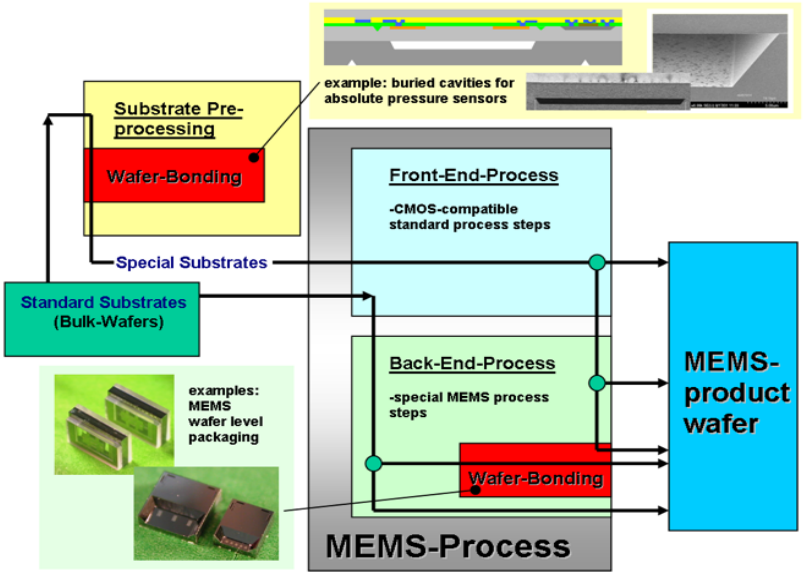

Figure 1: Application of wafer bonding in MEMS processing for substrate pre-processing and wafer level capping

Besides these very classical applications of wafer bonding in recent years it became very important for the 3D electronics integration in two different ways:

i) Ii)Temporary wafer bonding using special glues to join a wafer to a special carrier (often glass) is used to thin down wafers to thicknesses in the range of 100 µm or even below. This is indispensable to realize flexible electronic chips for smart cards and wearables, but also to prepare wafers or chips for 3D stacking. Still on the carrier wafers through silicon vias (TSVs) can be realized in the thinned silicon to get electrical contacts from the front to the backside and by that the possibility of vertical contacts through the vertical stack of electronics systems. Creating TSVs in thinned is accompanied by the positive effect, that processing is technologically easier – TSV holes are shorter and aspects ratios (TSV length = silicon thickness to diameter) can be more relaxed [3]. After wafer thinning and optimally after other processes like TSV creation are finished the thin wafer is removed from the carries, mostly by a laser release process (carrier wafer must be glass) or by a mechanical process. To allow a workable handling the thin wafers are either transferred to a tape on frame for dicing or to a second wafer, by a second wafer bonding process, to directly realize a vertical 3D-Integration.

ii) Hybrid wafer bonding is the simultaneous bonding of oxide layers for a strong and reliable joining and of embedded copper structures to realize electrical contacts in the bond interface. This is meanwhile the state-of-the-art method to bond wafers with electronics face to face and to form hundreds or thousands electrical contacts simultaneously, e.g. to equip computer processors with memories (both made in best suitable CMOS processes) at minimal signal path lengths [4]. The hybrid bonding is supported by wafer thinning and TSV processes to build up an electrical contact with the electronics which is in the bond interface.

3. REALIZATION OF WAFER BONDING

As shown in the first two paragraphs of the paper, wafer bonding is substantial technology for modern microelectronics and microsystems, however there exists not the one and only wafer bonding process. The term wafer bonding is rather describing a variety of technological solutions to stack and join substrates. Systemizations based on the bonded materials or regarding technological aspects are possible [5], but usually suffer from inconsistencies since one and the same bonding methods can be grouped in different categories. Thus, the methods are just listed, introduced, and explained to give an overview.

3.1 Semiconductor Direct Wafer Bonding

According to the name, semiconductor wafers are bonded directly, means without any intermediate layers for the actual bonding [6]. But this does not mean that there are necessarily no layers at all in the bond interface. Functional layers like silicon oxide as insulating layer can be coated on one or both semiconductor wafers before bonding. In that way Silicon on Insulator Wafers (SOI-Wafers) are produced during this bonding process and allows thin silicon layers for modern electronics insulated by a Silicon Oxide to the Carriere wafer below. The direct

wafer bonding process is rather characterized by an activation of the surface to be bonded (typically Silicon or Silicon Oxide). If the activated wafers are brought in contact, a bonding front is traveling along the bond interface, forming a weak pre-bond which is finally hardened to strength of the Silicon by thermal annealing. Mainly, the activation is a hydrophilization reaction, the saturation of dangling bonds of the substrate surface by OH-groups, which are connecting to each other in the pre-bond state. During annealing the rather weak OH-OH bonds are transferred to strong oxygen bonds. A perfect polished surface (Ra<1 nm) without any particles (perfect cleaning necessary) is crucial for the direct bonding. Figure 2 shows the traveling bond front and the direct wafer bonding principle.

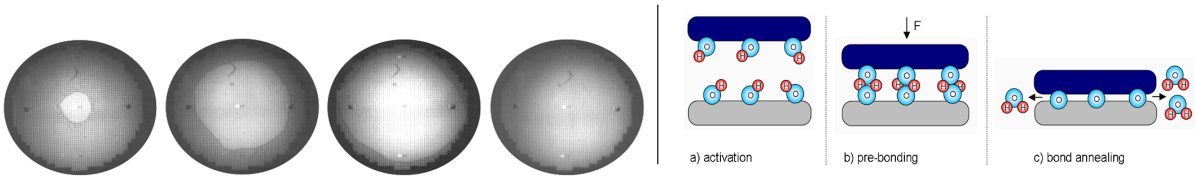

Figure 2: Bonding front traveling along the wafer interfaces (left) and formation of direct bond (right)

3.1.1 High Temperature Direct Wafer Bonding

For no or less processed Wafers (wafers with cavities or with just an oxide layer) the so-called high temperature wafer bonding can be used. High temperature means here an annealing temperature of 1000-1150°C. In this temperature range the transition of the OH-OH to Oxygen bonds is direct and no water is generated, the excessing water forms at the high temperatures a thermal oxide (like at thermal oxidation) and the Hydrogen can diffuse into and through the silicon crystal. The result is a very strong and void free bond. Since the high annealing temperatures can only applied to very stable materials like silicon and silicon oxide, very harsh chemicals like hot acids can be used for the activation. Hot acids provide both a perfect particle cleaning and hydrophilization and are the method of choice for activation wafer for the high temperature direct bonding. High temperature direct wafer bonding is mostly used for engineered substrates with buried layers (insulation) or cavities as MEMS functional elements.

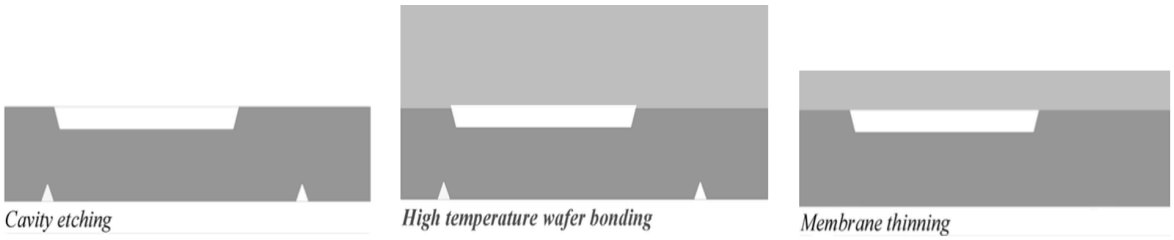

Figure 3: Example of high temperature direct wafer bonding for absolute pressure sensor substrates with buried cavities

3.1.2 Low Temperature Direct Wafer Bonding

Direct wafer bonding is also possible for wafers which were even more processed that are equipped with metal layers ore with finished MEMS and CMOS structures. However, the presence of metals is limiting both the annealing temperature to be lower 450°C (prevent alloying of the metal to the silicon) and the activation to non-acid based processes (not attacking the metals). For that purpose a low temperature variant of the direct wafer bonding was

developed, based on plasma activation prior to the bonding which allows annealing temperatures in the range of 200 to 400 °C achieving high bonding strengths without bubble generation in the bond interface during the thermal annealing [7]. With this method for example the backside of absolute pressure sensors can be sealed in vacuum. As received absolute pressure sensors are shown in figure 4.

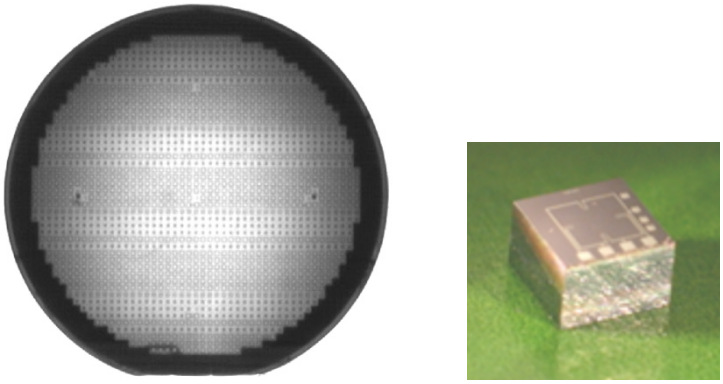

Figure 4: example of low temperature direct bonding of an absolute pressure sensor fabricated by back-side sealing of a relative pressure sensor wafer

3.2 Anodic Wafer Bonding

Anodic bonding of glass to silicon wafers is a widely used technique in microsystems technology. This is a relatively simple and safe process, in which a high bond strength and hermetic sealing is achieved. Typical applications of anodic bonding are sensor encapsulation and sealing of microfluidic systems. For anodic bonding, one of the two wafers to be bond have to be made of a sodium-containing glass which has its thermal expansion coefficient adjusted to match that of silicon, for example SCHOTT Borofloat33, Corning Pyrex #7740, or Hoya SD2. A bonding stack of one glass and one silicon wafer is heated up to a temperature of 300-500 °C. At these temperatures the sodium ions of the glass become mobile. By applying a negative voltage of some hundred volts to the glass wafers, the sodium ions drift away from the bonding interface, so that a depletion zone is created in the glass close to the silicon, in which most of the bonding voltage is dropped. As a result of the strong electrostatic field, the wafers are pressed together at the atomic level, and, by field-assisted oxygen diffusion and anodic oxidation, oxygen bonds are formed between the glass and silicon. Figure 5 illustrates this process and shows a typical application.

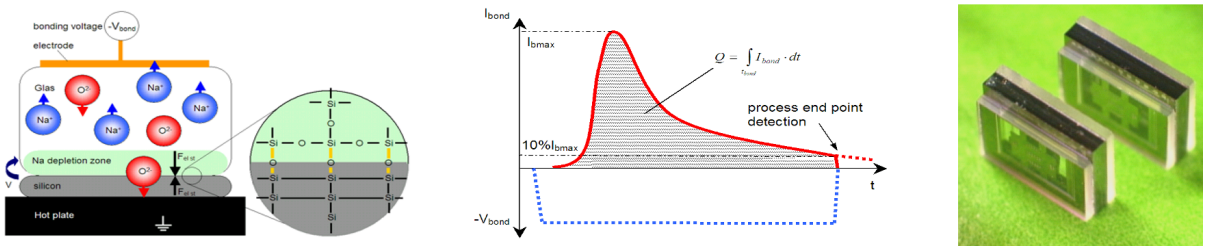

Figure 5: Principle of anodic bonding, Voltage and electrical current over time diagram of a typical anodic bonding process, and a typical application example

Anodic bonding is characterized by a very high yield, excellent hermetic sealing, and a very high bonding strength. The usage of glass can be a special benefit due to its optical transparency (optical applications, optical inspection of the bond interface), but is also a challenge since glass wafer structuring is still challenging and high in effort [8].

3.3 Glass Frit Wafer Bonding

For glass frit bonding a low melting point glass is necessary to join two or more wafers. This type of glass is commercially available (e.g. from Ferro Corporation) as a paste consisting of glass powder, organic binders and solvents. In the case of the widely used glass Paste FX 11-036 [9], the active melting glass compound is a lead-silicate glass with a wetting temperature of 425- 450 °C, which allows the bonding of wafers with aluminium structures. This glass is non-crystallising and contains zinc oxide as a wetting agent – both of these properties are advantageous for a high bonding performance. By adding high-melting barium-silicate filler particles, the thermal expansion behaviour of the glass frit is adjusted to match that of silicon to reduce thermo-mechanical stress at the bond interface. Meanwhile lead-free glass frit materials with processing temperatures of about 430°C are in development and under evaluation [10].

The glass frit bonding process consists of three main steps: screen printing, thermal conditioning of the glass paste, and the thermo-compressive bonding itself. These steps are shown principally in Figure 6 and described in the following.

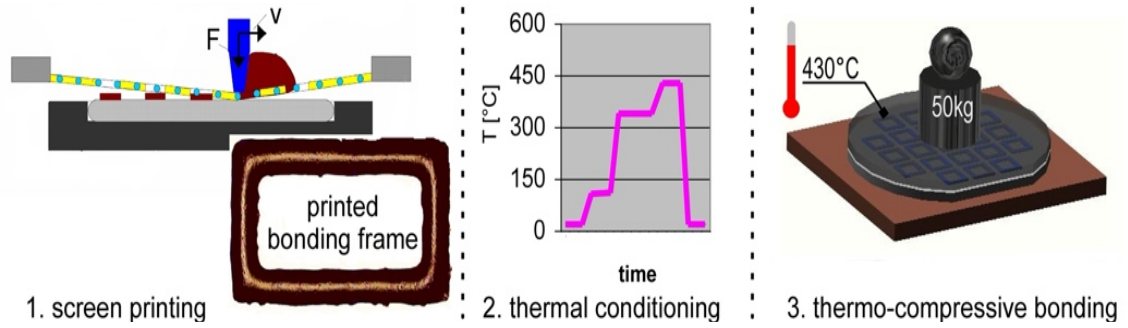

Figure 6: Principle process flow of glass frit bonding

Via screen printing, the paste can be deposited and structured in one step. The mesh openings are defined by the maximum paste particle size of 15 µm. The mesh thickness relates the printed structure maximum; 30 µm is recommended by the material manufacturer. The resulting bond frames have a minimum width of 190 µm, and a minimum distance of separated structures of 100 µm. To ensure a uniform glass thickness, all structures should have the same width, because the thickness increases with the print structure width. Due to the fact that screen printing does not give a particularly high accuracy of structural alignment, an area significantly larger than the required bond frame is necessary, and in addition, concave corners require more space. On the other hand, very precise screen printing is possible if the bond frame is limited by a cavity on both sides. For this, the screen opening has to be broader than the bond frame area defined in the silicon by the limiting cavities prior to bonding, a multistep thermal conditioning (Figure 7) is necessary in order to transform the paste into a real glass. During this pre-conditioning the solvent is burned out and the glass is pre-melted without internal voids.

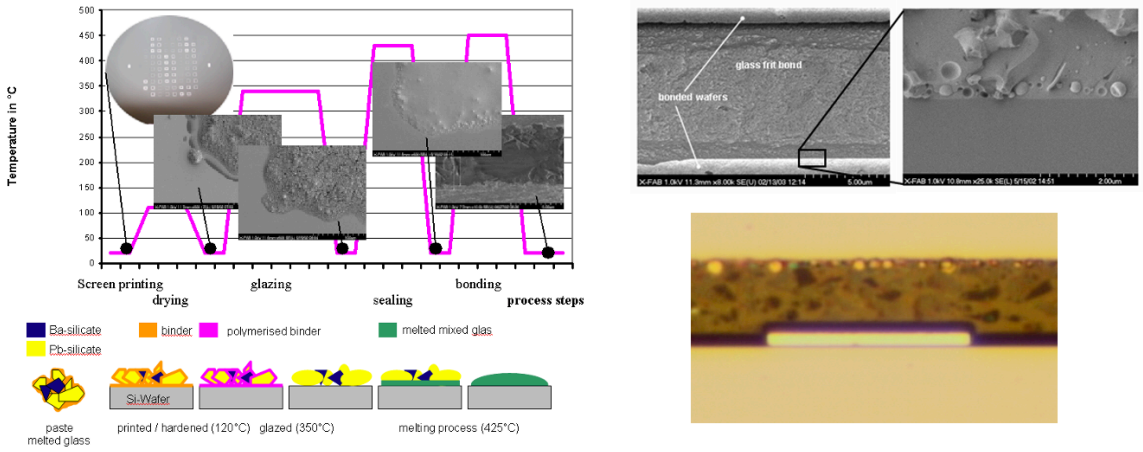

Figure 7: *thermal conditioning **glass** frit paste (left) and glass frit bond interface with (right) sealed metal line as electrical signal line through (right low)*

Bonding is a thermal process supported by slight pressure. By heating up the glass to the wetting temperature, its viscosity decreases to the point where it wets the bond surface. Material from the surface layer fuses into the glass on the atomic level, so that a strong bond is formed during cooling. The bonding temperature is the critical bonding parameter since it must be high enough to guarantee good wetting of the bond surface with the glass as the initial process for bond formation. The bond pressure gives only some support for the wetting, and equalises wafer geometry inadmissibility, such as bowing and warping. The cooling of the bonded wafer pair is only critical at higher temperatures where the bond is finally formed. However, to prevent thermal cracking of the wafers or the bonded interface by thermal shocks, the wafer stack has to be cooled down below 200°C before removing it from the bonding chamber.

By using a low melting point glass frit, it is possible to bond nearly all the surface of each material used in silicon microsystems: Silicon: (single and polycrystalline of any doping level) insulators and passivations (thermal or CVD silicon oxide, LP- and PE-CVD silicon nitride), metals (aluminium, aluminium-silicon, titanium, titanium-nitride, titanium-tungsten) special layers (polyimide, indium-tin oxide). Bonding wafers of different materials, such as silicon and Pyrex-type glass, is also possible if the thermal expansion coefficients are in the same range. Using Glass frit bonding, MEMS structures can be capped and sealed but also chips can be mounted in assembly processes (Figure 8).

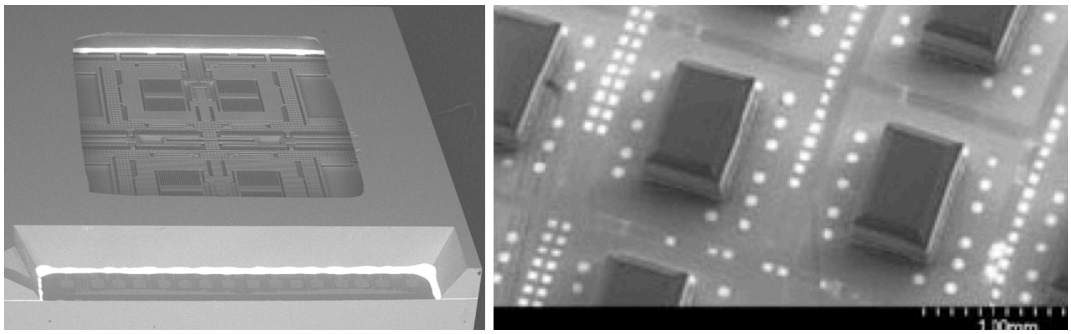

Figure 8: Application examples glass frit bonding: gyroscope capping (left) and optical glass windows on CMOS integrated Photodiodes (right)

3.4 Adhesive Wafer Bonding

During adhesive wafer bonding a glue as adhesive material is used to join the wafers. This joining can be either permanently or temporarily. Permanent wafer bonding methods and applications are described in the literature [11,12,13] and are used for capping, layer transfer or 3D Integration purposes. Here the adhesive material is spin coated, optional patterned and precured. Afterwards, the wafers are pressed together and the glue is thermally fully cured. The temporary adhesive wafer bonding follows the same process scheme, but usually without the patterning, because a homogenic support in the wafer thinning is required when the wafers are thinned down. This is the main application of the temporary wafer bonding as described above. In addition, the adhesive needs to be able to be released by laser or thermal decomposition demounting the wafer from the carrier.

A very interesting aspect of adhesive bonding is the usage of thick laminated dry films. Adhesive wafer bonding using laminated photosensitive dry-resist offers many advantages and can be used to realize advanced, CMOS integrated, lab-on-a-chip devices. The low bond-temperatures involved allow the hybrid integration of a range of substrates, e.g. CMOS wafers with structured MEMS glass wafers. The dry-film polymer acts as an adhesive interlayer and can be lithographically patterned to form sealed microfluidic fluid channels and chambers. This approach is well suited for low-cost R&D prototyping, and efforts reported in the past were often limited to proof-of-concept devices. However, all the process steps involved have the potential to be scaled up for industrial volume production. We report on our activities to implement a baseline 8″ process flow, using the ORDYL SY300 series of permanent dry-film resist, to enable the commercial manufacturing of microfluidic devices based on this technology at a MEMS foundry [14]. The described microfluidic application is illustrated in figure 9.

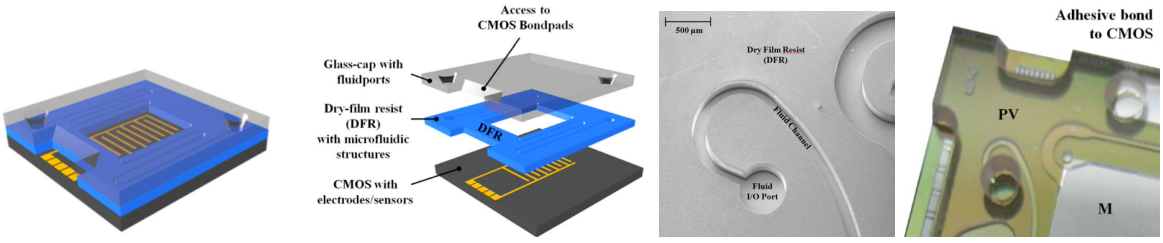

Figure 9: Microfluidic application using adhesive wafer bonding: schematics, structured adhesive dry film and bonded fully processed device

3.5 Further Wafer Bonding Processes

Regarding Wafer Bonding, there is wide variety of different processes, so not all approaches can be named or even described. However, some more should be named here:

For hermetic sealing of MEMS Sensor structures metal-based bonding technologies are emerging since they are providing lower vacuum levels at smaller bond frame widths compared to glass frit bonding. Eutectic bonding especially as Al-Ge Bonding in a CMOS compatible version [15] solder boding (the metal solder can be electroplated or screen printed) [16] and metal-metal-thermo compression bonding [17] should be named here. Regarding process integration and application related aspects they have specific advantages and drawbacks.

Surface activated bonding [18] is also a promising approach which is based on an ion bombardment of the bond surface, cleaning them from oxides and contaminations, leaving a very activated surface allowing strong and reliable wafer bond at room temperature without a need of later annealing. This is a process well suited to bond materials with very different coefficients of thermal extension since bonding is done on room temperature and technology wise no heating of the tack of substrates is required afterwards. The bonding strength his usually high enough to withstand thermal stress in the application temperature range (e.g. -45…175°C), just in the case of very different CTE the application temperature rage might be limited.

An alternative for bonding thermal sensitive constructions is the reactive wafer bonding. Here heat is still used to form the bond. The high temperature is generated just in the bond area by multilayers systems which are reacting exothermally after laser or electrical ignition. The multilayers can either form directly the bond or are melting solders. Due to this very local heating effect neighbouring areas are not affected thermally by the bonding process.

As already mentioned, hybrid wafer bonding is a rather new process for 3D wafer level integration of electronics. The process [19,20] is actually based on the low temperature direct bonding of oxide layers. Besides the bonding process a chemical mechanical polishing (CMP) step very important. During polishing of both wafers to be bonded copper pads laterally embedded in oxide layers are processed. Both the oxide and the copper pads are polished to an overall flat surface with a low roughness to allow the direct bonding of the oxide. In the CMP process there is a slight dishing effect at the copper pads, so that these are locally slightly lower compared to the oxide surface. This dishing effects come from different polishing rates of both materials and is utilized in the hybrid bonding process. In the pre-bond (mechanical contacting of the wafers to bond, at room temperature, traveling bond front) just the polished oxide layers are joined, at the copper pads there is a dishing related gap. In the thermal annealing process this oxide-oxide bond becomes mechanically strong, while the copper grains are growing and forming good low ohmic contacts. By this both strong bonding and electrical contacts are provided for different materials but in one wafer bonding process.

4. COMPARISON AND SYSTEMIZATION OF WAFER BONDING PROCESSES

As shown in the description of the wafer bonding processes, they are very different in the way the bond is formed and the processing is done. All wafer processes are having the common goal to provide a strong and reliable bond, related to the application – this is also true for the temporary adhesive bonding (bond needs to withstand the processing) even if it is finally released again. Typically, a second goal is a hermitic bond, especially if bonding has an encapsulation and protecting purpose which is typically for MEMS application, which requires mostly a defined working atmosphere (kind of gas, pressure, vacuum) in their cavities. With the stacked 3D-integration. Low ohmic contacts with perfect process yield are a further requirement which is getting more important in the recent years with the advancing of 3D wafer level integration. In addition, microsystems chips are getting smaller and smaller, this reduces the available bond frame area – a bond frame width of 100 µm and smaller are meanwhile sate of the art in all the mentioned wafer bonding processes. Beside these main requirements on the bonding results, there are many aspects in the field of technology integration important: available tools and materials in the wafer fabs, material compatibilities (prevention of cross contamination), wet or dry activation, protection of wafer bond frames in MEMS release processes, realization of the bond frames (glass frit screen printing, metal deposition and related structuring for eutectic or thermocompression bonding), wafer boding temperature (thermal

budget) and more. Beside the technological aspects also the economic side needs to be considered – bonding two wafers is per definition expensive, since two wafers are needed and must be processed up to the bonding. It can be concluded that the bonding process should be cost efficient (short bonding time, cost efficient bonding material, not too expensive bonding tools) and that process yield (ratio if correctly bonded wafers) and chip yield (bonding strengths, hermeticity) are very high. Therefore, it is very helpfully to have various wafer bonding processes available, to choose the overall most suitable one for each specific application. This can be done with related comparative studies of different bonding processes [22]. A high-level overview about the discussed wafer bonding processes in relation to potential application is shown in Table 1. It shows advances together withlimitations of existing wafer bonding approaches for different applications. With new materials and new wafer bonding tools there will be improvements in the bonding processes in the next years and by this more application fields will open up and we can expect even completely new wafer bonding methods.

Table 1: Comparison and systemisation of wafer bonding processes related to applications

Wafer Bonding Process	Engineered Substrates	MEMS Capping	MEMS CMOS Integration	Micro Fluidics	3D-Elelctronics Integration	Thin Wafer Processing
High Temperature direct bonding	++	--	--	+	--	--
Low Temperature direct bonding	+	+	+	+	+[1]	--
Glass Frit Wafer Bonding	--	++	++	-	-	--
Anodic Bonding of Glass Wafers	--	+	-	++	-	--
Eutectic Bonding	--	++	++	-	+	--
Solder Bonding	--	++	++	-	+	--
Metal Direct Bonding	--	++	++	-	+	--
Permanent Adhesive Bonding	--	+[2]	+	++	-	--
Temporary Adhesive Bonding	--	--	--	--	+[3]	++
Surface Activated Bonding	++	+	+	++	+	+
Reactive Wafer Bonding	--	+	+	-	+	--
Hybrid Bonding	--	-	+	--	++	--

++ typical application
\+ possible application
\- rather not possible application
-- impossible application

[1] as part of the hybrid bonding process
[2] if hermetic bonding is not required
[3] as part of layer transfer methods

5. SUMMARY AND CONCLUSIONS

Wafer bonding is a very substantial process in microelectronics and microsystems technologies. Actually it is opening the real 3rd dimension in originally mainly layer based CMOS and MEMS technologies and devices. This 3D-charater can be seen in in engineered substrates like SOI and cavity SOI wafers, the capping and completing of MEMS devices, MEMS-CMOS Integration (CMOS on cap wafers) and the 3D stacking of electronics by hybrid bonding. As diverse the applications are, as diverse are the technological methods to realize the wafer bonding. The mostly used wafer bonding technologies, low and high temperature direct, anodic, glass frit and adhesive wafer bonding are introduced in this paper regarding process flow, bond formation and the characteristics of the bond interface. Other, rather special or novel wafer processes such

as metal based, surface activated reactive, and hybrid bonding are rather shortly described to complete this overview of bonding processes. Regarding the application the most suitable wafer bond process needs to be chosen case by case requiring complete understanding of the potential bonding technologies. For some application like MEMS-CMOS integration there are quite some options, while for others (thin wafer processing) there exists just one suitable process. In table 1 the usability of the introduced wafer bonding processes for general application areas is shown. Which process is finally used for the specific application cannot not only be defined by this table, other aspects like process integration (available materials and tools, bond frame width, bonding temperatures, protection of bond frame structures and others) need to be considered in any special case as well. The importance of the wafer bonding technologies goes beyond joining wafers in microsystem technologies, it is also applicable for other substrates and even for bulky parts and may inspire other technology fields.

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