FLOATING AND GROUNDED IMPEDANCE SIMULATOR

BY

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This thesis is dedicated to

My parents for their love and endless care,

and my brothers for their encouragements,

and my friends for their support

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First for all, I thank ALLAH for his blessings and giving this opportunity to me to contribute in this field. And I thank him again for all his grace that made me able to overcome this challenge.

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LIST OF ABBREVIATIONS

IC : Integrated Circuit

MOSFET : Metal Oxide Semiconductor Field Effect Transistor

BJT : Bipolar Junction Transistor

VDTA : Voltage Differencing Transconductance Amplifiers

CCTA : Current Conveyor Transconductance Amplifier

DV-CCTA : Differential Voltage Current Conveyor Transconductance Amplifier

VDBA : Voltage Differencing Buffered Amplifier

OTA : Operational Transconductance Amplifier

VDCC : Voltage Differencing Current Conveyor

DVCC : Differential Voltage Current Conveyor

FB-VDBA : Full-Balanced Voltage Differencing Buffered Amplifiers

OTRA : Operational Transresistance Amplifier

VDIBA : Voltage Differencing Inverting Buffered Amplifier

VCVS : Voltage-Controlled Voltage Source

CCCS : Current-Controlled Current Source

DUA : Differential Unity Gain Amplifier

ABSTRACT

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Thesis Title : Floating and Grounded Capacitance Multiplier

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This thesis presents a CMOS floating and grounded tunable capacitance multiplier with high multiplication factor. The proposed design uses the translinear loop stage and two OTAs stage for the grounded capacitance and CCII and OTAs for the floating one. The MOS transistors are biased in Subthreshold region to provide low power consumption and high multiplication factor. The total multiplication factor is widely tunable and can be up to 1200 times of the value C with maximum error of 8.5% for the grounded capacitance designs and 3600 times with maximum error of 8.6% for the floating capacitance design. The designs are simulated using TANNER TSPICE with 0.18μm TSMC level 49 technology and powered using ± 0.75 supply voltage.

ملخص الرسالة

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تقدم هذه الرسالة لمكثف أرضي أو عائم بتقنية (CMOS)مع عامل ضرب عالي. يستخدم التصميم المقترح مرحلة طريقة الحلقة أو ما يعرف باسم (Translinear Loop). ومرحلتي OTAs للمكثف الأرضي و CCII و OTAsللمكثف العائم. الترانزستورات المستخدمة تم تشغيلها في منطقة Subthreshold للحصول على استهلاك منخفض للطاقة وتوفير عامل مضاعف عالي. إن عامل الضرب الكلي قابل للتحكم على نطاق واسع ويمكن أن يصل إلى 1200 مرة من قيمة المكثف الأصلية C مع خطأ أقصى قدره 8.5٪ لتصميم المكثف الأرضي و3600 مرة مع خطأ أقصى يبلغ 8.6٪ لتصميم المكثف العائم. يتم محاكاة التصاميم باستخدام TANNER TSPICE مع تقنية .CMOS 0.18µm TSMC يتم تشغيل التصاميم المقترحة باستخدام جهد التغذية قدره ± 0.75 فولت وتعمل التصاميم في الترددات المنخفضة تحت 1 كيلو هرتز الذي يفي بمتطلبات التطبيقات الطبية الحيوية ذات الترددات المنخفضة.

CHAPTER 1

INTRODUCTION

System integrability has been a common practice over the years to satisfy the appealing of reducing the size of the devices and to achieve portability. Meanwhile, the digital systems have progressed so far to have been able to integrate millions of transistors into a single die area. But on the other hand, the analog systems faced a severe issue in the same matter in certain applications such as filters that requires passive elements that are area hungry relative to their values. Another appealing feature of integrated systems is high accuracy, better performance, wide dynamic range and less power consumption.

In low frequency applications, such as biomedical circuits when high impedance values such as capacitors and resistors are needed which again is impractical to be implemented in the integrated circuits (ICs). The common approach for solving this issue is to use impedance multiplier circuit that uses less chip area. The idea here is to implement a small starting value of passive element and then scaling it up using a simple circuit that has less effect on the total impedance and uses small silicon area. Simulated impedances can be grounded or floating depending on the intended application.

There are several designs and techniques developed so far which introduced some key features to distinguish between them such as the multiplication factor, negative impedance, transistor type, tunability, power consumption and chip area. Some of these designs are built with active elements and a small passive element. These types of designs are usually

called impedance simulator, impedance multiplier, impedance emulator or impedance scaler.

1.1 Motivation

As the technology advances more transistors can be fabricated in a small area except for the passive elements. These impedance values are still directly proportional to the silicon area. On the top of that, if a high value of impedance is required for an example a capacitor in 0.18μm CMOS process has a related value of 1.0fF/μm^2 [1]. This means a 1.0nF capacitor it may take 1mm^2 of silicon area which becomes impractical to fabricated in an IC chip because of the area required to implement the capacitor is huge. The motivation of this thesis is to develop a circuit which simulates grounded and floating capacitance that has higher value, required small area compared to the actual impedance and its total impedance is electronically controllable via the bias currents or voltages.

The following key features should be considered when designing such circuits: multiplication factor, technology used, tunability, power consumption and silicon area.

1.1.1 Multiplication Factor

The total simulated impedance will require a base passive element in the design, then scaled up using various method. The multiplication factor needed to be high so that the base impedance can be very small which helps also in reducing the chip area and make the design possible to be fabricated in an IC.

1.1.2 Tunability

The multiplication factor can have a fixed value or range of values. This feature can be very helpful in designing circuits with tunable parameters like filters with tunable cut-off frequencies or in oscillators with tunable frequencies.

1.1.3 Power Consumption

The power consumption is a key parameter as it defines whether this circuit is suitable for portable applications such as implantable devices where replacing batteries is considered a big concern. It is also important to mention that higher power consumption will dissipate more heat which can be critical in some applications.

1.1.4 Silicon Area

The main target of the design, with replacing the actual impedance with a simulated one containing active elements will result in relatively less chip area. Passive components with high values are considered a critical disadvantage in the design or not preferred, so these components need to be as minimum as possible.

1.1.5 Technology used

As it is known from the technology advancements going toward reducing the size of the MOSFET transistor which is different from the bipolar junction transistors (BJT). So, to gain the advantage of less area, MOSFET are the preferred choice here.

1.2 Problem Statement

Many designs have been reported for the impedance simulator, and this will be shown in detail in the literature survey chapter. However, there were always some missing feature

from those designs. It is always a challenge to achieve all the feature perfectly, so one or more of them had to be suffered so that it can enhance the remaining ones. The problem here is in low frequency application like filters with low cut-off frequencies (mHz) which translates into large time constants that is directly proportional to the capacitance, these types of applications requires large capacitance that will take large silicon area rendering the designs to be impossible to fabricate in an IC chip.

1.3 Thesis Organization

This thesis will be divided into four chapters and the outline for each one is described below.

Chapter 1: Introduction.

This chapter presents the need of an impedance simulator circuit to overcome the issue of IC fabrication and lists the important feature that these circuits should have which motivates this thesis.

Chapter 2: Literature Review.

This chapter lists some of the previous designs and circuits used for impedance simulator in an organized way and summarize them with a discussion about this research goals.

Chapter 3: Proposed Designs and Simulation Results.

Here two proposed circuits for grounded and floating capacitance simulator will be presented with appealing features including the design of the sub-circuits that it requires to

yield better results. Simulation results and discussion and nonideal analysis are also presented.

Chapter 4: Conclusion.

This final chapter will provide the conclusion and future works.

CHAPTER 2

LITERATURE REVIEW

Impedance scaler is a useful technique when large time constant is needed for low frequency applications. Over the years, many circuits have been designed with different techniques, some of these will be described in this section while investigating the problems within.

The impedance to be scaled can be a resistor or capacitor. In this work, we will focus only on the capacitor simulator as it has many applications like filters, oscillators and compensators.

Impedance simulator attracts the attention of researchers in the last two decades. Consequently, a lot of research papers are presented in the open literature. Different approaches were used and can be classified as:

1- Voltage Differencing Transconductance Amplifiers (VDTA) based.
2- Current Conveyor Transconductance Amplifier (CCTA) and Differential Voltage Current Conveyor Transconductance Amplifier (DV-CCTA) based.
3- Voltage Differencing Buffered amplifier (VDBA) based.
4- Operational Transconductance Amplifier (OTA) based.
5- Voltage Differencing Current Conveyor (VDCC) based.
6- Other.

2.1 VDTA Based Capacitance Simulator

The VDTA has a relation between its input voltages and output currents as shown in Figure 2-1. The use of VDTA is that it has two values of tunable transconductance which is useful for different applications that require tunability such as capacitance simulator.

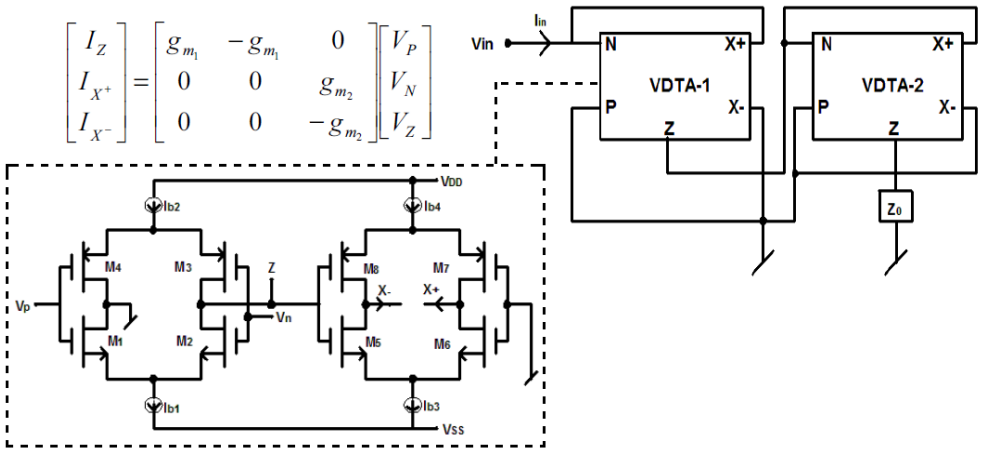

Figure 2-1 VDTA relation with a variable grounded capacitance simulator design.

A variable grounded capacitance simulator using VDTA presented in [2] and [3] with different configurations, using the VDTA model presented in [4]. The multiplication factor is the ratio between the bias currents of the two VDTA. One of them is biased with 150µA which is very high and will result in a high-power consumption, and due to the limits of the bias currents mentioned in the VDTA model, the maximum multiplication factor recorded is four times.

The design in [5] used three VDTA and two passive resistors. These designs suffer from high-power consumption because of bias currents in 150µA, with two extra passive resistors added there to enhance the multiplication factor range.

2.2 CCTA and DV-CCTA Based Capacitance Simulator

The CCTA first realized in 2005 [6], the relation between its currents and voltages are shown in Figure 2-2. The main advantage of this block is that its output current can be controlled electronically.

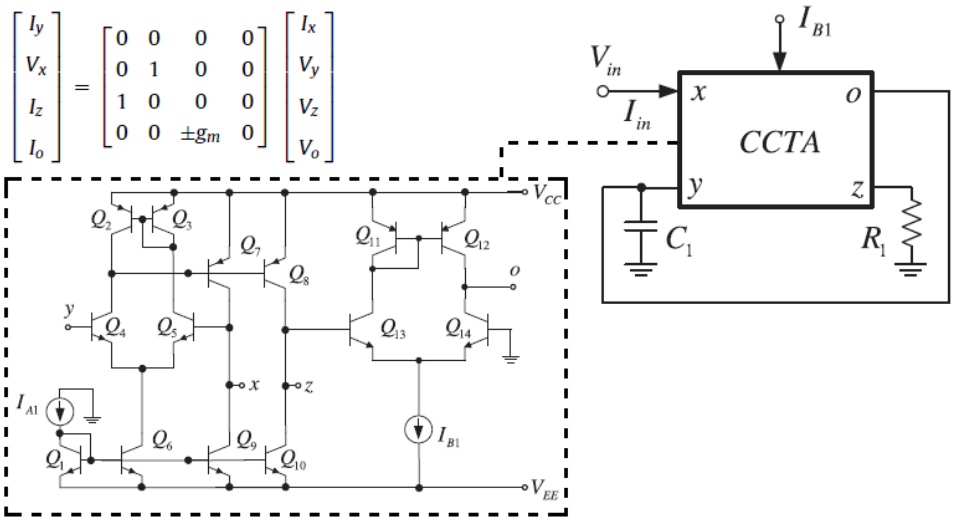

Figure 2-2 CCTA relation with a simple grounded capacitance simulator design.

A simple grounded capacitance simulator based-on CCTA is presented in [7], with a supply voltage ±1.5V and bias currents 50μA. The resulting power consumption is high, the circuit has a limited multiplication factor and it is constructed using bipolar junction transistor (BJT) which is not favorable in this era for integrated circuits. Temperature insensitive/electronically controllable floating simulators based on DV-CCTA presented in [8], but it uses two extra passive element and consumes large power. A current controlled CCTA based- novel grounded capacitance multiplier with temperature compensation is presented [9] the design has an extremely high multiplication factor and it is tunable, but the circuit is designed using BJT and the supply voltage is ±1.5V and high bias currents in

micro ampere range. A differential voltage current conveyor (DVCC) based floating capacitance multiplier designs are presented in [10] and [11]. These two designs are using CMOS transistors but still suffers from an extra passive element and high bias current (100μA) results in high power consumption and has limited scaling factor.

2.3 VDBA Based Capacitance Simulator

The VDBA has a relation between its input voltages and output currents as shown in Figure 2-3. A transconductance amplifier as an input stage and a unity buffered voltage gain as an output stage, thus the tunability can be achieved through the transconductance value which is suitable for capacitance simulator.

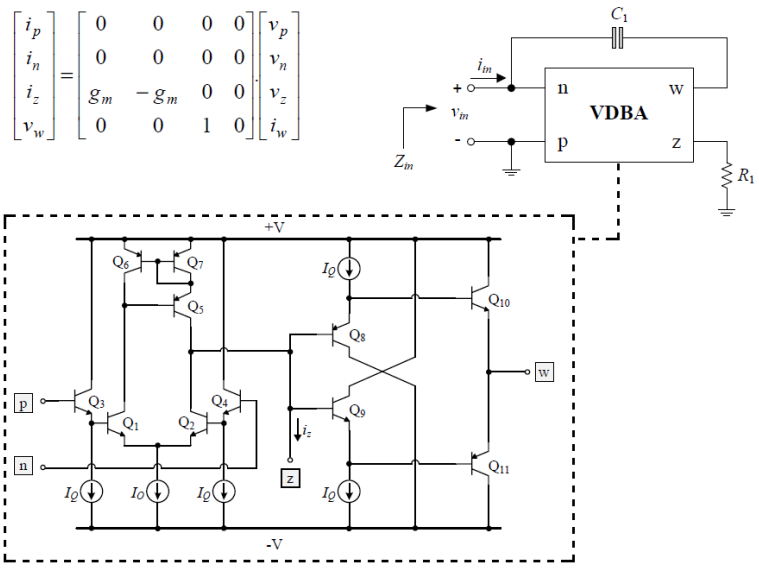

Figure 2-3 VDBA relation with a tunable capacitance multiplier design.

A tunable capacitance multiplier with a single voltage differencing buffered amplifier is presented in [12]. The design is, BJT based with limited scaling factor and high-power consumption. A similar VDBA based design is presented in [13] but it uses two VDBA`s

and extra two passive elements which still has the same disadvantages with even large silicon area. Another floating capacitance multiplier circuit using full-balanced voltage differencing buffered amplifiers (FB-VDBAs) is reported in [14] using BiCMOS realization. It requires high bias current (50μA) and have limited scaling factor.

2.4 OTA Based Capacitance Simulator

The OTA shown in Figure 2-4 has been employed and emphasized as a favorable building blocks for tunable applications and circuit realizations for capacitance multipliers.

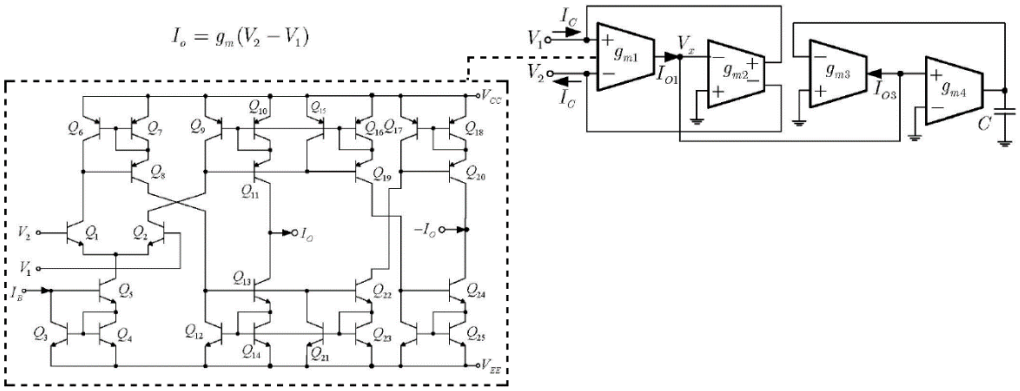

Figure 2-4 OTA relation with a an electronically controllable capacitance multiplier with temperature compensation.

An electronically controllable capacitance multiplier circuit with temperature compensation utilizing the OTA are presented in [15], [16], and [17]. These designs have high multiplication factor because of the wide linear range of the OTA designed using BJT. Other designs are presented in [18], [19] and [20]. The existence of an extra passive elements renders these designs to have large silicon area. Designs presented in [21] and [22] are using dual output OTAs. The bias currents are high and hence consumes high power and are not tunable.

Multiple stage capacitance multiplier using dual-output differential amplifiers is presented in [23]. The design used multiple stages such that the multiplication factor can be high, but the total power consumption is high. The design presented in [24] has high bias currents resulting in high power consumption and a limited scaling factor.

2.5 VDCC Based Capacitance Simulator

The VDCC is presented in [25] with its input and output relation is shown in Figure 2-5.

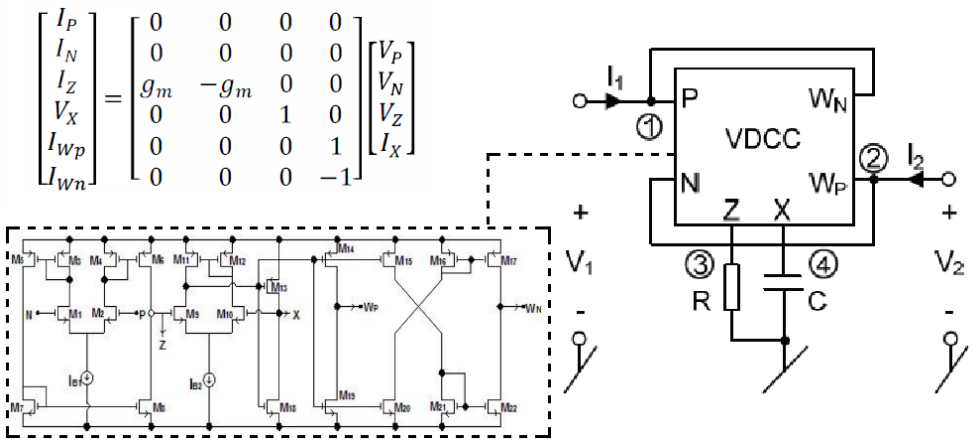

Figure 2-5 VDCC relation with a tunable floating capacitance simulator design.

Tunable capacitance simulators with VDCC are found in [26], [27], [28] and [29]. All these designs require extra passive elements which is not suitable in integrated circuits and the bias current is around 100μA which is considered high and hence high power consumption.

2.6 Other Capacitance Simulator designs

The design in [30] uses Operational transresistance amplifier (OTRA) and six passive elements which consumes a large chip area and it is not electrically tunable. Another design using voltage differencing inverting buffered amplifier (VDIBA) is presented in [31]. This

design uses less chip area but suffers from a very limited range of tuning. Another design uses differential unity gain amplifier to implement a floating impedance scaling circuit [32]. It is a simple design, but it lacks the tunability for the multiplication factor since it depends on transistor sizes. A complex design in [33] employing log and anti-log circuits plus two nonlinear transconductance. Since the log and anti-log circuits involving excessive number of active elements this affects the area and the power consumption of the circuit in addition to the complexity of the circuit itself. A grounded capacitance utilizing Dual-X second-generation current-conveyor DXCCII is presented in [34]. The problem in this circuit is the DXCCII itself since the implementation of this device requires large number of transistors with high bias currents which results in high power consumption and a large area on chip.

The designs presented in [35] – [42] have extra passive elements which will require large silicon area. Other designs in [43], [44] and [45] uses large bias currents increasing the power consumption. The circuit presented in [46] has a limited multiplication factor.

Another circuits for capacitance simulator are presented in [47] and [48], which has fixed scaling factor and lacks the tunability.

2.7 Summary

From the presented works in the literature survey, it is wise to compare between them to have a general understanding of the features for each design. We will be interested in the number of extra passive elements, power consumption, supply voltage, transistor type, technology used, electronically tunable and maximum multiplication factor. A summery

for the literature survey is in Table 2-1 where F means for floating, G for grounded and NA for not available.

Table 2-1 Summery of the literature survey

Reference	Building Block	Type	Supply Voltage	Power Consumption	Technology	# of passive elements	Tunable?	Scaling Factor
[2]	VDTA	G	±0.9V	NA	0.18µm	0	Yes	3
[3]	VDTA	G	±0.9V	NA	0.18µm	0	Yes	1.7
[5]	VDTA	G	NA	NA	NA	2	Yes	1.7
[7]	CCTA	G	±1.5V	542µW	BJT	1	Yes	10
[9]	CCTA	G	±1.5V	0.822mW	BJT	0	Yes	4
[12]	VDBA	G	±1.5V	0.89mW	BJT	1	Yes	20
[13]	VDBA	G	±1.5V	NA	BJT	2	Yes	10
[15]	OTA	G	NA	NA	BiCMOS	0	Yes	1000
[17]	OTA	G	NA	NA	BJT	0	Yes	100
[18]	OTA	G	±2.2V	1.32mW	0.5µm	1	Yes	28
[20]	OTA	G	±3V	1.815mW	0.5µm	2	Yes	10000
[21]	OTA	G	NA	NA	NA	2	NA	10
[22]	OTA	G	NA	NA	NA	2	Yes	100
[23]	OTA	G	±2V	6.72mW	0.5µm	0	Yes	28
[24]	OTA	G	NA	NA	NA	0	Yes	7
[26]	VDCC	G	±5V	NA	BJT	1	Yes	NA
[29]	VDCC	G	NA	NA	0.35µm	1	Yes	30
[30]	OTRA	G	NA	NA	BJT	6	No	NA
[31]	VDIBA	G	±0.75V	5.27mW	0.25µm	0	Yes	3
[34]	DXCCII	G	±0.1.65V	0.2mW	0.35µm	0	Yes	50
[35]	CCII	G	NA	NA	BJT	2	No	NA
[36]	NA	G	NA	NA	UMC130	3	No	NA
[38]	CMOS	G	1.8V	NA	0.18µm	4	No	NA
[39]	OTA CCII	G	NA	NA	NA	2	Yes	NA
[41]	CMOS	G	NA	NA	BiCMOS	0	No	40
[45]	VDIBA	G	±0.75V	5.27mW	0.25µm	0	Yes	3
[46]	CMOS	G	1.2V	175nW	65nm	0	Yes	140
[8]	DV-CCTA	F	±2.5V	NA	BJT	2	Yes	3
[10]	DVCC	F	±0.75V	1.29mW	0.13µm	2	Yes	20
[11]	DVCCTA	F	±2V	3mW	0.5µm	1	Yes	3
[14]	FB-VDBA	F	±1V	NA	BiCMOS	0	Yes	3
[16]	OTA	F	±2.5V	0.565mW	BJT	0	Yes	100000
[19]	OTA	F	NA	0.5µW	0.35µm	1	Yes	NA
[27]	VDCC	F	±0.45V	556µW	90nm	2	No	NA
[28]	VDCC	F	±0.9V	NA	0.18µm	2	Yes	NA
[32]	CMOS	F	±0.9V	53.2µW	0.18µm	0	No	50

Reference	Building Block	Type	Supply Voltage	Power Consumption	Technology	# of passive elements	Tunable?	Scaling Factor
[37]	CMOS	F	±3V	5.28mW	0.5µm	3	Yes	10
[40]	DVCC	F	±0.2.5V	NA	0.25µm	0	Yes	15
[43]	CBTA	F	±1.5V	43.3mW	0.25µm	2	NA	NA
[44]	FB-VDBA	F	±1V	NA	BiCMOS	0	Yes	3
[47]	CMOS	F	±0.9V	53.2µW	0.18µm	0	No	NA
[48]	CMOS	F	1.8V	5.94µW	0.18µm	0	No	50
[33]	NA	NA	0.5V	16.19nW	0.18µm	NA	NA	NA
[42]	NA	NA	1.28V	NA	BiCMOS	2	NA	NA

CHAPTER 3

PROPOSED DESIGN

By observing the previous designs; it appears that a design with tunability, low power consumption and without any extra passive elements is required. These are the main key feature of this thesis. In this chapter, a tunable grounded and floating capacitance simulator with high multiplication factor are realized utilizing translinear principle, OTAs and CCII. Both proposed designs are designed in weak inversion featuring low-power consumption, linearly tunable and requires small silicon area to make them suitable for portable implants applications.

3.1 Design Concept

The principle of designing a capacitance scaler is discussed in [49]. The scaling of a capacitance can be done in two methods as illustrated in Figure 3-1. In Figure 3-1a the scaling is done using voltage-controlled voltage source (VCVS) in series with a capacitor.

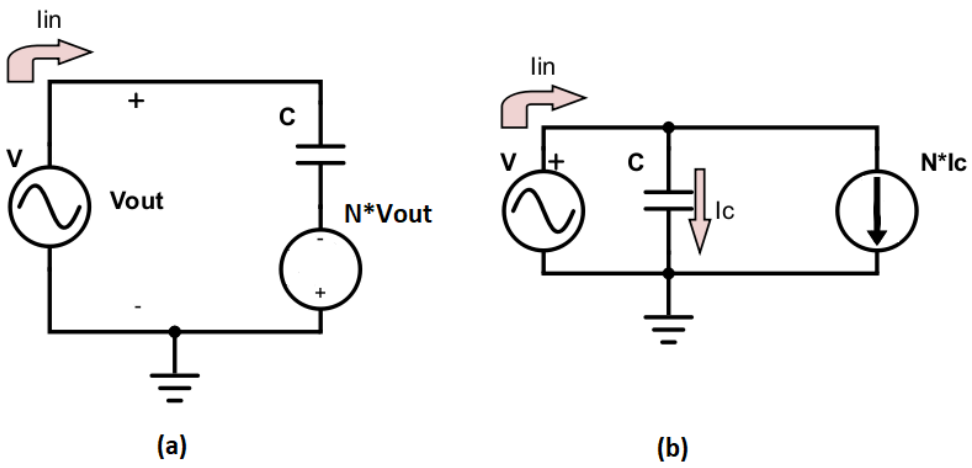

Figure 3-1 General design for floating capacitance simulator

The input current for the circuit is

$$I_{in} = \frac{V_{out} + N * V_{out}}{1/sC} = \frac{V_{out}(1+N)}{1/sC}$$

The total capacitance seen from the input voltage is.

$$Z_{eq} = \frac{1}{sC_{eq}} = \frac{V_{out}}{I_{in}} = \frac{V_{out}}{\frac{V_{out}(1+N)}{1/sC}} = \frac{1}{(1+N)*sC}$$

$$C_{eq} = (1+N) * sC$$

Figure 3-1b employs a current-controlled current source (CCCS) connected in parallel with the capacitor, the input current for the circuit is

$$I_{in} = I_C + N * I_C = \frac{V}{1/sC} + N * \frac{V}{1/sC} = V * sC(1+N)$$

The total capacitance seen from the input voltage is.

$$Z_{eq} = \frac{1}{sC_{eq}} = \frac{V}{I_{in}} = \frac{V}{V*sC(1+N)} = \frac{1}{sC(1+N)}$$

$$C_{eq} = (1 + N) * sC$$

It is clear that designs based on voltage controlled will require high voltage dynamic range for tunability and may need to generate voltages higher than the input voltage. The disadvantages here are the limitation in the dynamic range and are difficult to implement due to the advanced technology which utilizes low power supply. On the other hand, designs based on current controlled are preferable due to the wide dynamic range under low supply voltages.

After an extensive study of the literature survey and focusing on current controlled method, a proposed method is selected for designing a capacitance simulator in Figure 3-2 [46]. This method is used for floating capacitance simulator. However, grounded capacitance simulator is obtained if V_2 is grounded.

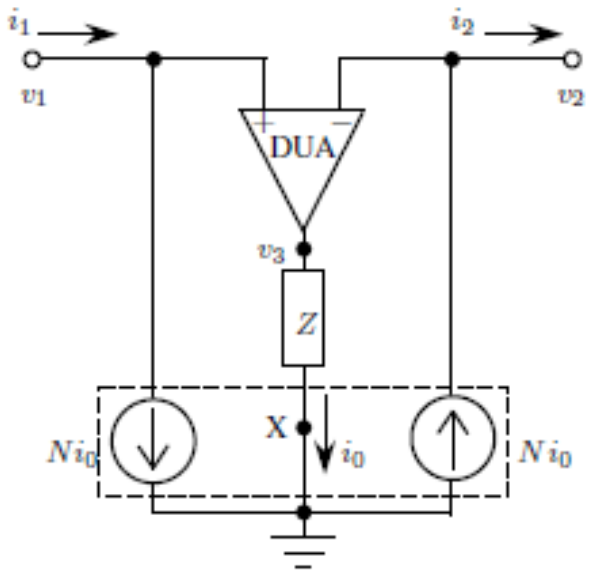

Figure 3-2 Proposed method for constructing floating capacitance simulator

With the differential unity gain amplifier (DUA) and neglecting the input impedance from the current scaler circuit, the voltage across the impedance Z, V_3 is given by:

$$V_3 = V_1 - V_2 \tag{3.1}$$

The current that flows through the impedance Z is given by:

$$I_Z = \frac{V_3}{Z} = \frac{V_1 - V_2}{Z} \tag{3.2}$$

By using the current scaling circuit that acts as a linear current amplifier with two outputs, one is drown from V_1, the other supplies to V_2. The equivalent impedance seen between V_1 and V_2 is.

$$Z_{eq} = \frac{V_1 - V_2}{I_1} = \frac{V_1 - V_2}{I_2} = \frac{V_1 - V_2}{N * I_Z} \tag{3.3}$$

Combining equations (3.2) and (3.3), the equivalent impedance is given by:

$$Z_{eq} = \frac{V_1 - V_2}{N\frac{V_1 - V_2}{Z}} = \frac{Z}{N}$$

If Z is replaced by a capacitor

$$Z_{eq} = \frac{I}{S * C * N}$$

And hence

$$C_{eq} = C * N \tag{3.4}$$

This relation gives us a suitable way for designing the proposed circuit for capacitance simulator.

To achieve low power consumption, it is desired to design the proposed circuit using MOSFET operating in weak inversion region.

As for the tunability, the current scaling circuits should be constructed with a linear electronically tunable design block with high accuracy.

Regarding the multiplication factor, a general fact is that if a circuit is designed to be operated in subthreshold region, it is expected that its dynamic range to be low which affects the multiplication factor. To overcome this problem, the multiplication can be done in two stages instead of one. With low scaling factors from both stages, the accumulated scaling factor will be high since both factors are multiplied.

3.2 Proposed Grounded Capacitance Multiplier

The proposed grounded capacitance multiplier is shown in Figure 3-3, it consists of two multiplication stage and a CCII as current buffer stage. The first stage of multiplication is the translinear loop formed using M1-M4, a current buffer formed using M5-M12 and lastly OTA1 and OTA2 (Operational Transconductance Amplifier) is for the second multiplication stage.

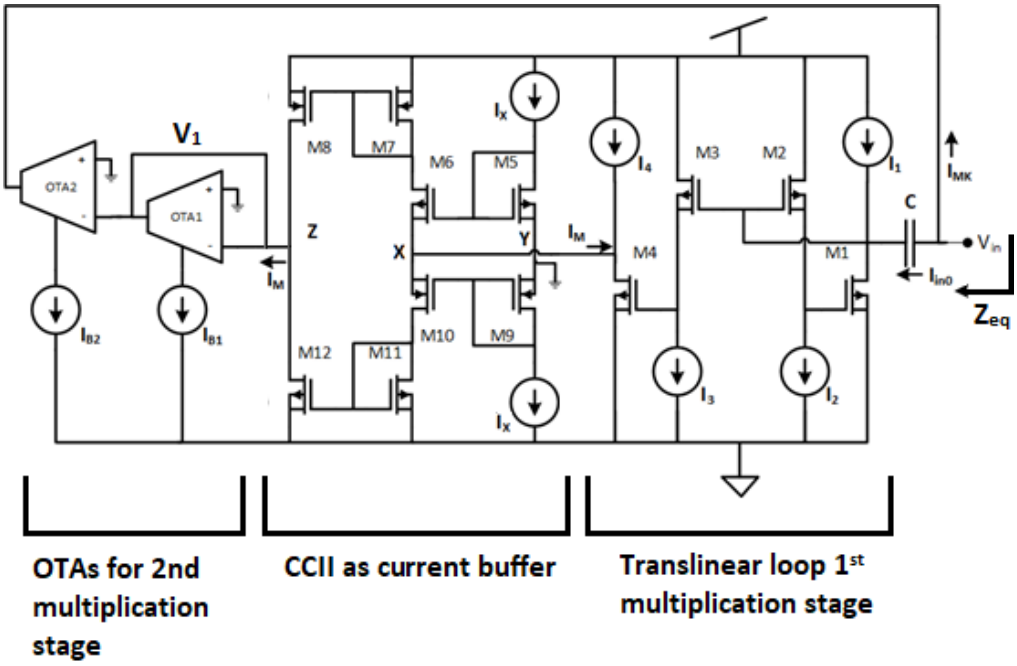

Figure 3-3 Proposed grounded capacitance simulator circuit

From the translinear loop, the well-known relation between the currents in subthreshold region is.

$$I_{\mathrm{D1}} * I_{\mathrm{D2}} = I_{\mathrm{D3}} * I_{\mathrm{D4}} \tag{3.5}$$

$$I_{\mathrm{D1}} = I_{\mathrm{in0}} + I_1$$

$$I_{\mathrm{D4}} = I_{\mathrm{M}} + I_4$$

Then equation (3.5) is written as

$$(I_1 + I_{in0}) * I_2 = I_3 * (I_4 + I_M)$$

$$I_1 * I_2 + I_{in0} * I_2 = I_3 * I_4 + I_M * I_3$$

If $I_1 * I_2 = I_3 * I_4$, then

$$I_M = M * I_{in0} \tag{3.6}$$

Where M = I_2/I_3, and voltage V_1 is given as.

$$V_1 = \frac{1}{g_{m1}} * I_M = \frac{2nV_T}{I_{B1}} * M * I_{in0}$$

The current I_{MK} is given as.

$$I_{MK} = g_{m2}V_1 = \frac{I_{B2}}{I_{B1}} * M * I_{in0} = M * K * I_{in0} \tag{3.7}$$

Where K = I_{B2}/I_{B1}.

The total impedance Z_{eq} looking into terminal V_{in}.

$$Z_{eq} = \frac{V_{\text{in}}}{I_{\text{in0}}+I_{MK}} = \frac{V_{\text{in}}}{I_{in0}(1+M*K)} \tag{3.8}$$

Since M*K >> 1, then equation (3.8) is written as

$$Z_{eq} = \frac{V_{\text{in}}}{I_{in0}*M*K} \tag{3.9}$$

The impedance of the capacitor is very large compared to the input impedance of the translinear loop [50] and $V_{in}/I_{in0} = Z_C$, then equation (3.9) is written as:

$$Z_{eq} = \frac{Z_C}{M*K} \tag{3.10}$$

Replacing the impedance by capacitance with Z = 1/sC

$$C_{eq} = C * M * K \tag{3.11}$$

Equation (3.11) shows that the equivalent capacitance can be controlled by two multiplying factors M and K. This will allow a multiplication factor up to 1200 times while keeping

the percentage of error lower than 10%. Another feature which is observed clearly from the equations that it is temperature insensitive, due to the cancelation of all temperature related parameter from all stages.

Negative equivalent capacitance can be achieved by swapping the connection of OTA2 inputs, which causes the current I_{MK} to be inverted, then the result of the total capacitance can be in negative values. The details of each stage is explained in the following sub chapters.

3.2.1 Translinear Loop

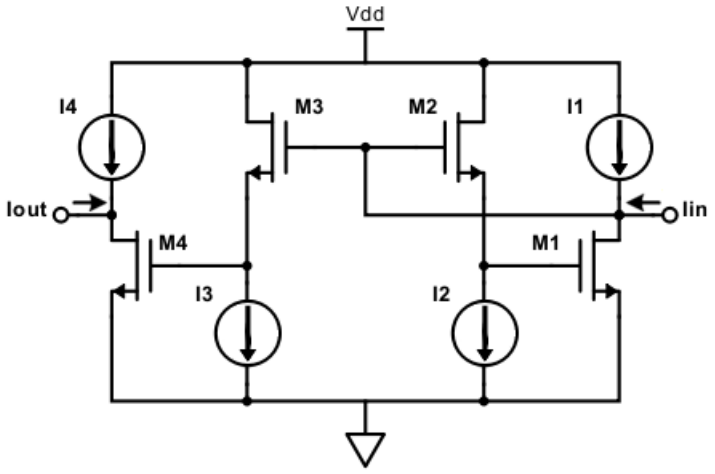

Figure 3-4 Translinear loop circuit

With to Figure 3-4, the translinear loop formed by M1-M4 relation is given by:

$$V_{GS1} + V_{GS2} = V_{GS3} = V_{GS4} \tag{3.12}$$

The drain current for the NMOS transistors operating in weak inversion region is given by:

$$I_D = I_{Do} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \left(1 - e^{\left(\frac{-V_{DS}}{V_T}\right)}\right) \tag{3.13}$$

Where I_{DO} is the saturation current, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage, n is the slope factor, V_T is the thermal voltage, V_{DS} is the drain-source voltage. For the NMOS to operate in forward saturation, the following conditions must be satisfied.

$$V_{DS} > 4V_T \tag{3.14}$$

$$I_D \ll I_{D0} \tag{3.15}$$

Equation (3.13) is rewritten as

$$I_D = I_{Do} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \tag{3.16}$$

Using the equation (3.16), V_{GS} is given.

$$V_{GS} = nV_T * \ln\left(\frac{I_D}{I_{Do}}\right) + V_{Th} \tag{3.17}$$

Assume M1-M4 are matched then combining equations (3.12) and (3.17). The following relation is generated.

$$I_{D1} * I_{D2} = I_{D3} * I_{D4}$$

Since the transistor current will be the same as their respective bias currents.

$$I_1 * I_2 = I_3 * I_4 \tag{3.18}$$

Equation (3.18) can be written as.

$$I_4 = I_{out} = I_{in} * M \tag{3.19}$$

Where M equals to I_2/I_3. Applying the relation (3.19) to the circuit in Figure 3-3

$$I_M = I_{in0} * M \tag{3.20}$$

This yields the first multiplied current I_M with a factor M.

3.2.2 Current Conveyor

Current conveyor can be used as a current buffer for their unique characteristic to copy the current from terminal X to terminal Z [51]. The circuit diagram of the CCII is shown in Figure 3-5 and has the matrix relation between its terminals shown in equation (3.21).

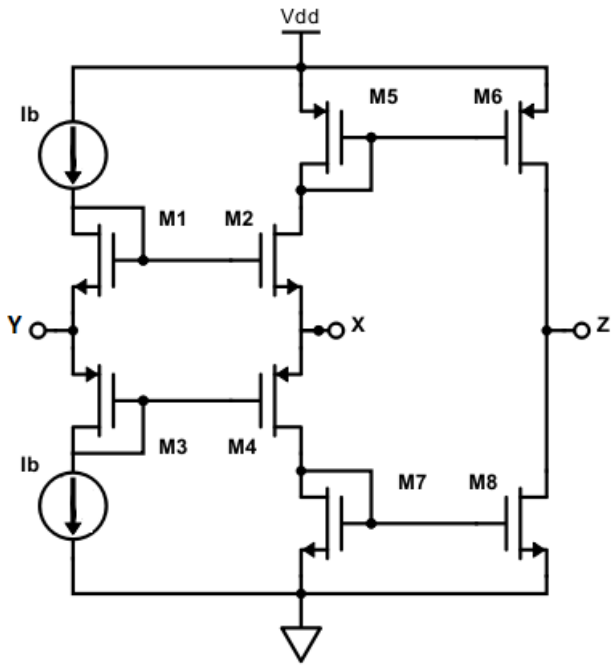

Figure 3-5 Circuit diagram for CCII

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.21}$$

This circuit consists a class AB voltage follower between terminal Y and X formed by transistors M1-M4, this provides a good control and high effectiveness and accuracy in the use of the quiescent current and has relatively low voltage offset which is determined mainly by transistor mismatch [51]. The transistors M5-M6 and M7-M8 are simple current mirrors to copy the current between terminal X and Z. These simple current mirrors can be replaced by cascode current mirrors to enhance the accuracy and increase the output impedance if needed. The two bias currents I_b will force the input current at terminal Y to be nearly zero and hence the input impedance at terminal Y is infinity.

3.2.3 OTA

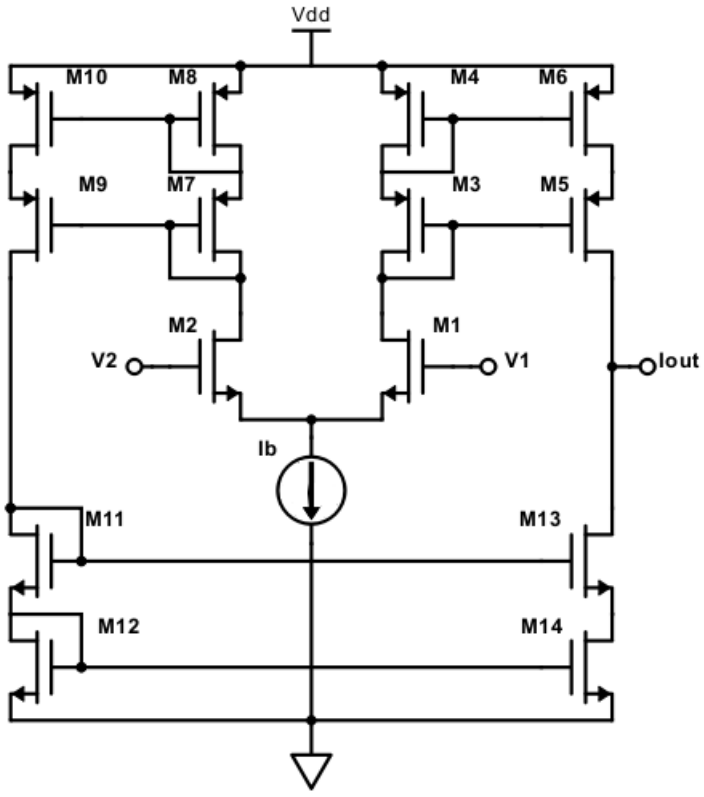

Figure 3-6 Circuit diagram for OTA

The OTA`s structure is balanced type with cascode current mirrors to provide high output impedance and better accuracy as shown in Figure 3-6. It has a simple differential pair operating in subthreshold with the following relation.

$$I_b = I_{DM1} + I_{DM2}$$

$$I_{out} = I_{DM1} - I_{DM2}$$

Using the current equation for MOS operating in subthreshold region, the relation between I_{out} and I_b is:

$$\frac{I_{out}}{I_b} = \frac{I_{DM1} - I_{DM2}}{I_{DM1} + I_{DM2}}$$

$$\frac{I_{out}}{I_b} = \frac{I_{Do}e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)}\left(1-e^{\left(\frac{-V_{DS}}{V_T}\right)}\right)_1 - I_{Do}e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)}\left(1-e^{\left(\frac{-V_{DS}}{V_T}\right)}\right)_2}{I_{Do}e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)}\left(1-e^{\left(\frac{-V_{DS}}{V_T}\right)}\right)_1 + I_{Do}e^{\left(\frac{V_{GS}-V_{th}}{nV_T}\right)}\left(1-e^{\left(\frac{-V_{DS}}{V_T}\right)}\right)_2} \quad (3.22)$$

The two transistors are matched and share the same source voltage V_S, the term $e^{-VDS/VT}$ will be neglected if $V_{DS} > 4V_T$. Equation (3.22) can be written as.

$$\frac{I_{out}}{I_b} = \frac{e^{\left(\frac{V_G}{nV_T}\right)_1} - e^{\left(\frac{V_G}{nV_T}\right)_2}}{e^{\left(\frac{V_G}{nV_T}\right)_1} + e^{\left(\frac{V_G}{nV_T}\right)_2}} \quad (3.23)$$

The gate voltage (V_G) of the two transistors M1 and M2 are inputs of the differential pair, then the differential voltage (V_{id}) will have this relation.

$$V_{id} = V_{G1} - V_{G2}$$

For simplifying the relation, both gate voltages will have this relation.

$$V_{G1} = \frac{V_{id}}{2} \; and \; V_{G2} = \frac{-V_{id}}{2}$$

Combining this relation to equation (3.23) results in.

$$\frac{I_{out}}{I_b} = \frac{e^{\left(\frac{V_{id}}{2nV_T}\right)} - e^{\left(\frac{-V_{id}}{2nV_T}\right)}}{e^{\left(\frac{V_{id}}{2nV_T}\right)} + e^{\left(\frac{-V_{id}}{2nV_T}\right)}} \tag{3.24}$$

The resulted equation gives a similar relation to the hyperbolic tan (*tanh*) function.

$$\tanh X = \frac{e^{(X)} - e^{(-X)}}{e^{(X)} + e^{(-X)}} \tag{3.25}$$

Assuming

$$X = \frac{V_{id}}{2nV_T} \tag{3.26}$$

Then

$$\frac{I_{out}}{I_B} = \tanh \frac{V_{id}}{2nV_T} \tag{3.27}$$

It is well known that in the *tanh* function, the output is almost equal to the input as shown from the *tanh* curve in Figure. 3-7, this implies that.

$$\tanh X \approx X \tag{3.28}$$

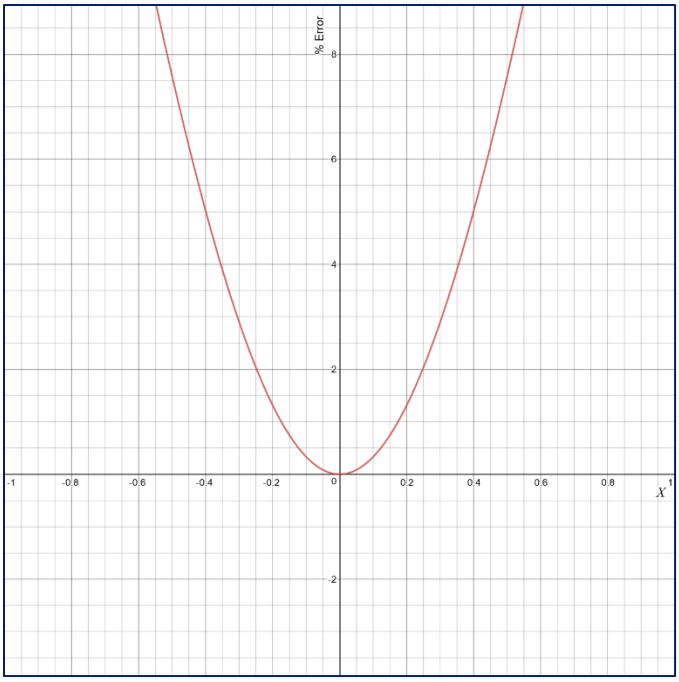

Figure 3-7 tanh function curve

From the curve, with X is less than 0.5, equation (3.27) can be written as.

$$\tanh \frac{V_{id}}{2nV_T} \approx \frac{V_{id}}{2nV_T} \tag{3.29}$$

$$\frac{V_{id}}{2nV_T} < 0.5 \tag{3.30}$$

$$V_{id} < nV_T \tag{3.31}$$

Combining equation (3.29) and equation (3.27), the output current is given by.

$$I_{out} = I_b * \frac{V_{id}}{2nV_T} = g_m V_{id} \tag{3.32}$$

Where g_m is equal to ($I_B/2nV_T$).

The bias current I_b has a limited range since the OTA is designed to work in subthreshold and need to be kept in this mode. As mentioned earlier, in equation (3.15), the bias current

should be ten times less than I_{DO} of the transistors to assure forward saturation in weak inversion operation.

Consider the two OTAs connected in a configuration shown in Figure 3-8. OTA1 acts as an active grounded resistor equals to $1/g_m$.

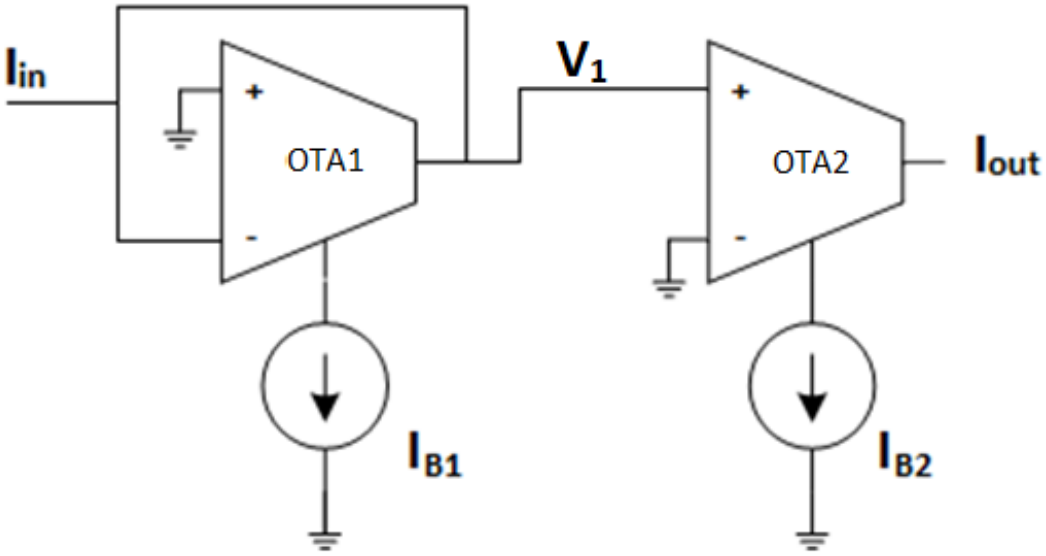

Figure 3-8 Two OTAs configuration for current amplifier

The voltage V_1 is given as.

$$V_1 = \frac{1}{g_{m1}} * I_{in} = \frac{2nV_T}{I_{B1}} * I_{in} \tag{3.33}$$

Then output current I_{out} is given as.

$$I_{out} = g_{m2}V_1 = \frac{I_{B2}}{I_{B1}} * I_{in} \tag{3.34}$$

3.2.4 Simulation Results

TANNER TSPICE simulator with 0.18µm TSMC CMOS processing technology and BSIM3V3 level 49 MOS model was used to simulate the proposed grounded capacitance simulator. The aspect ratio for all transistors is given in Table 3-1. The circuit was powered with voltage sources of ±0.75V. All bias currents have the initial value of 10nA, and the capacitor C value will be 10pF. The bias currents I_2 and I_4 are fixed to 200nA which make the value of M to be equal to 20. The current I_{B2} was swept from 10nA to 600nA so the value of K will be from 1 to 60, and the total multiplication factor will be in the range from 20 to 1200. From equation (3.11), the expected simulated capacitance will be from 0.2nF to 12nF.

Table 3-1 The aspect ratios of the transistors for the proposed grounded capacitance

Block	Transistor	W/L
Translinear	M1 – M4	20µm / 1µm
CCII	M1 – M8	10µm / 0.25µm
OTA	M1 – M2	20µm / 0.5µm
	M3 – M14	10µm / 1µm

Plot of the simulated impedance of the proposed grounded capacitor is shown in Figure 3-9. It is evident that the working frequency range is between 1Hz and 1KHz. The scaled capacitance values have been obtained for both the ideal and simulated results and were compared, the results are shown in Table 3-2 and Figure 3-10. It is seen that having a large total scaling factor of 1200 results in an error of less than 8.6%.

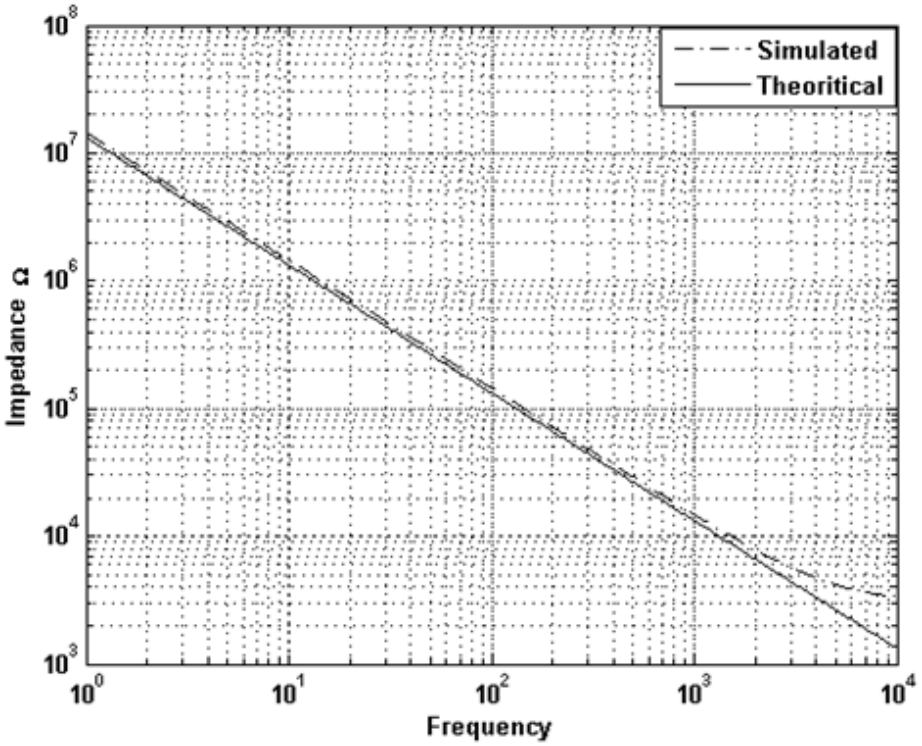

Figure 3-9 The impedance of the proposed grounded capacitance simulator for M=20 and K =60

Table 3-2 Comparison between the theoretical and simulated capacitance

M = 20		Expected value of Capacitance (nF)	Simulated value (nF)	% of Error
K	Multiplied Factor			
1	20	0.2	0.210	5.030
5	100	1.0	0.993	0.738
10	200	2.0	1.950	2.505
20	400	4.0	3.822	4.461
40	800	8.0	7.452	6.845
60	1200	12.0	10.978	8.515

As shown in Table 3-2, the percentage of error is increasing with the increase of factor K, this happens because the bias current of OTA1 is increasing which will become closer to the value of I_{DO} affecting the conditions in equation (3.15).

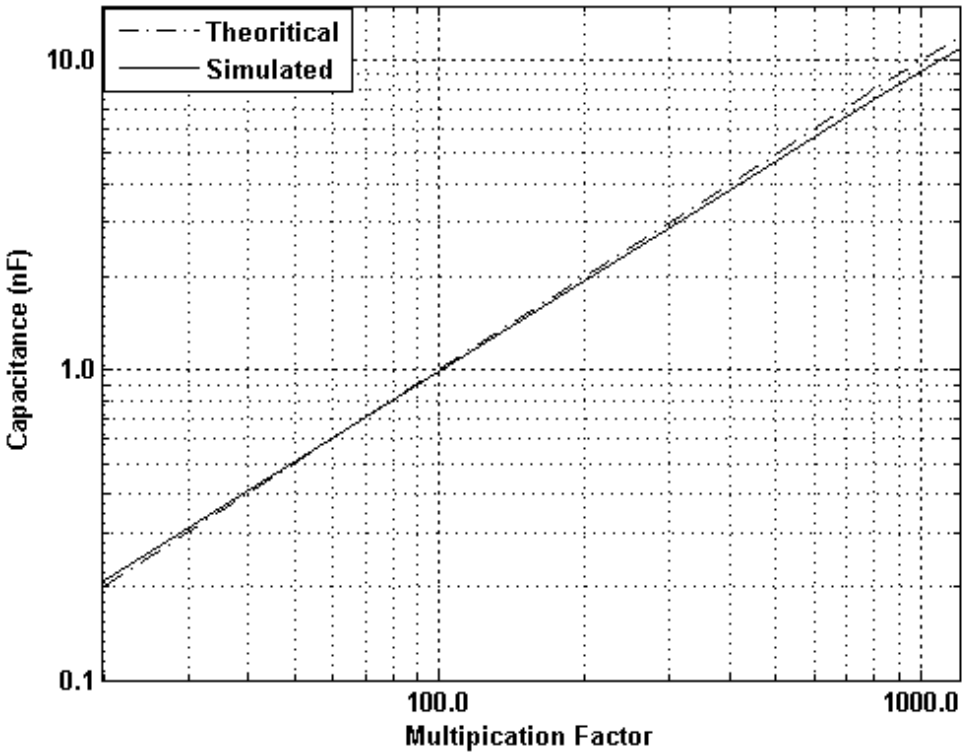

Figure 3-10 Variations between the simulated and expected values of the grounded capacitance through different multiplication factor

To study the temperature variation effect, the temperature analysis was carried out. The temperature has swept from 0C to 100C for the multiplication factor of 1200, which is shown in Figure 3-11. As expected, the design is almost insensitive to temperature variations.

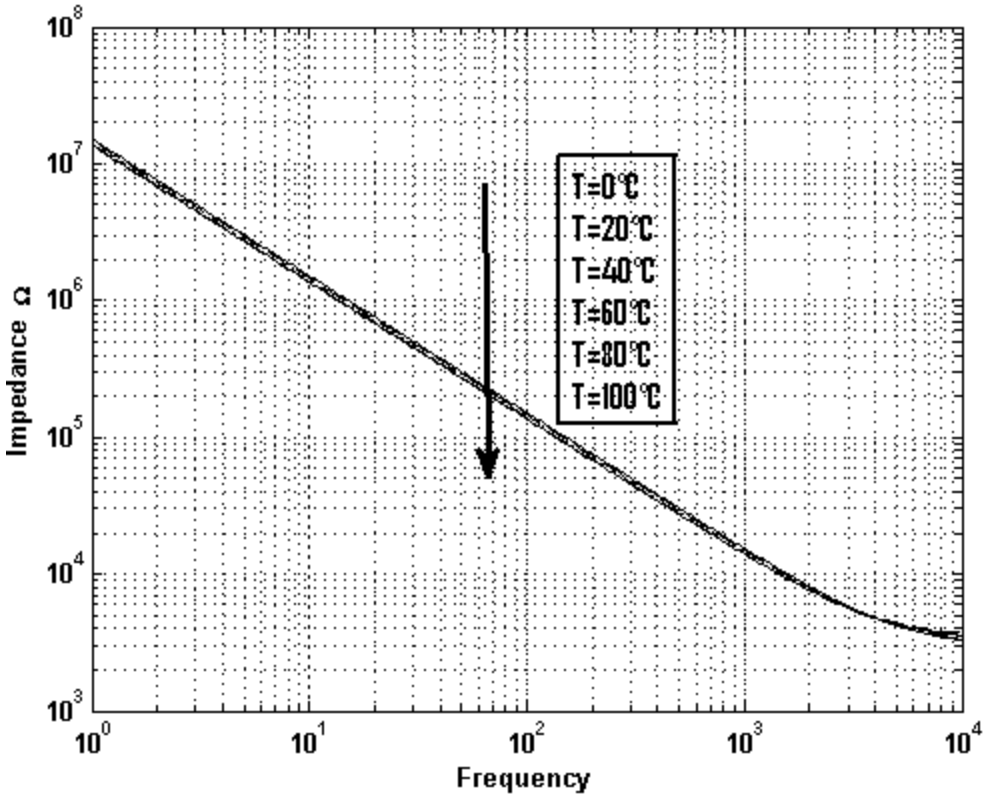

Figure 3-11 Simulation result of temperature analysis for scaling factor of 1200

The propose grounded capacitance simulator design is compared with the previous works and summarized in Table 3-3.

From Table 3-3, it is seen that the proposed work excelled the other designs in terms of low-power consumption and has high tunable range (up to 1200) compared with the others and doesn`t use passive elements.

Table 3-3 Performance comparison between the proposed circuit and previous ones

Reference	Building Block	Type	Supply Voltage	Power Consumption	Technology	# of passive elements	Tunable?	Scaling Factor
[2]	VDTA	G	±0.9V	NA	0.18µm	0	Yes	3
[3]	VDTA	G	±0.9V	NA	0.18µm	0	Yes	1.7
[5]	VDTA	G	NA	NA	NA	2	Yes	1.7
[7]	CCTA	G	±1.5V	542µW	BJT	1	Yes	10
[9]	CCTA	G	±1.5V	0.822mW	BJT	0	Yes	4
[12]	VDBA	G	±1.5V	0.89mW	BJT	1	Yes	20
[13]	VDBA	G	±1.5V	NA	BJT	2	Yes	10
[15]	OTA	G	NA	NA	BiCMOS	0	Yes	1000
[17]	OTA	G	NA	NA	BJT	0	Yes	100
[18]	OTA	G	±2.2V	1.32mW	0.5µm	1	Yes	28
[20]	OTA	G	±3V	1.815mW	0.5µm	2	Yes	10000
[21]	OTA	G	NA	NA	NA	2	NA	10
[22]	OTA	G	NA	NA	NA	2	Yes	100
[23]	OTA	G	±2V	6.72mW	0.5µm	0	Yes	28
[24]	OTA	G	NA	NA	NA	0	Yes	7
[26]	VDCC	G	±5V	NA	BJT	1	Yes	NA
[29]	VDCC	G	NA	NA	0.35µm	1	Yes	30
[30]	OTRA	G	NA	NA	BJT	6	No	NA
[31]	VDIBA	G	±0.75V	5.27mW	0.25µm	0	Yes	3
[34]	DXCCII	G	±0.1.65V	0.2mW	0.35µm	0	Yes	50
[35]	CCII	G	NA	NA	BJT	2	No	NA
[36]	NA	G	NA	NA	UMC130	3	No	NA
[38]	CMOS	G	1.8V	NA	0.18µm	4	No	NA
[39]	OTA CCII	G	NA	NA	NA	2	Yes	NA
[41]	CMOS	G	NA	NA	BiCMOS	0	No	40
[45]	VDIBA	G	±0.75V	5.27mW	0.25µm	0	Yes	3
[46]	CMOS	G	1.2V	175nW	65nm	0	Yes	140
Proposed Work	Translinear OTA CCII	G	±0.75V	1.545µW @1200 times	0.18µm	0	Yes	1200

3.3 Proposed Floating Capacitance Simulator

The block diagram of the proposed floating capacitance simulator is shown in Figure 3-12. It consists of a CCII+ and two multiplication stages. The first multiplication stage consists of OTA1 and OTA2 and the second multiplication stage is formed using OTA3 and OTA4.

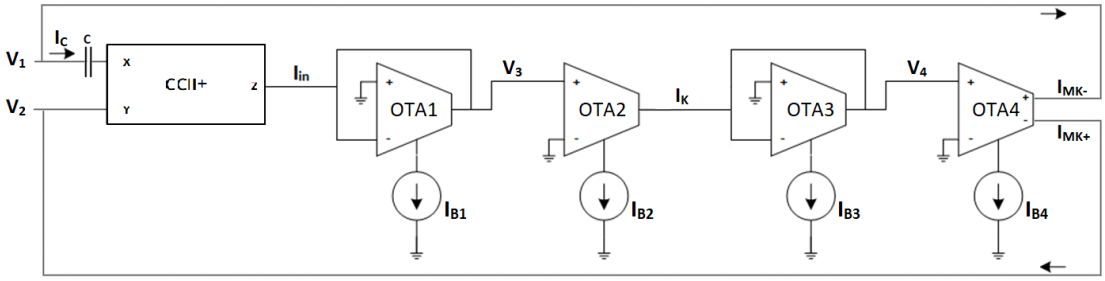

Figure 3-12 Proposed circuit for the floating capacitance simulator

With reference to Figure 3-12

$$I_{in} = I_C \tag{3.35}$$

The voltage V_3 is given by:

$$V_3 = \frac{1}{g_{m1}} * I_{in} = \frac{2nV_T}{I_{B1}} * I_C \tag{3.36}$$

The current I_K is given by:

$$I_K = g_{m2}V_3 = \frac{I_{B2}}{I_{B1}} * I_C = K * I_C \tag{3.37}$$

Where $K = I_{B2}/I_{B1}$.

The voltage V_4 is given by:

$$V_4 = \frac{1}{g_{m3}} * I_K = \frac{2nV_T}{I_{B3}} * K * I_C \quad (3.38)$$

Then output currents I_{MK+} and I_{MK-} are given by:

$$I_{MK+} = -I_{MK-} = g_{m4}V_4 = \frac{I_{B4}}{I_{B3}} * K * I_C = M * K * I_C \quad (3.39)$$

Where M = I_{B4}/I_{B3}.

The total impedance Z_{eq} seen between terminals V_1 and V_2 is given by:

$$Z_{eq} = \frac{V_1}{I_{MK-}+I_C} - \frac{V_2}{I_{MK-}} = \frac{V_1}{I_C(1+M*K)} - \frac{V_2}{I_C*M*K} \quad (3.40)$$

Since M*K >> 1, then equation (3.40) is rewritten as:

$$Z_{eq} = \frac{V_1-V_2}{I_C*M*K} \quad (3.41)$$

From the CCII+ function in equation (3.21), the current I_C is given by:

$$I_C = \frac{V_1-V_2}{Z_C} \quad (3.42)$$

Combining equation (3.41) with equation (3.42), the total equivalent impedance is given by:

$$Z_{eq} = \frac{V_1-V_2}{\frac{V_1-V_2}{Z_C}*M*K} = \frac{Z_C}{M*K} \quad (3.43)$$

Replacing the impedances with 1/sC, equation (3.43) is given by:

$$Z_{eq} = \frac{1}{sC*M*K} \rightarrow C_{eq} = C * M * K \quad (3.44)$$

The relation in equation (3.44) describes the functionality of the proposed floating capacitance simulator with two scaling factors M and K. Consequently, high scaling factor is achieved. The proposed design is electronically tunable through the bias currents of the OTAs. The design is passive-less to insure the ability to fabricate it using CMOS technology with less silicon area compared to designs with extra passive elements. All the transistors in the proposed design works in subthreshold region to assure low power consumption. The details for the sub-circuits will be discussed next.

The internal circuit for the CCII+ is shown in Figure 3-13.

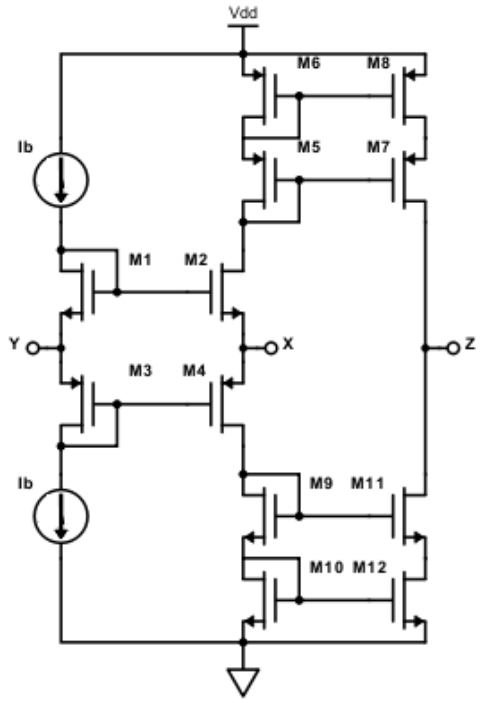

Figure 3-13 Circuit diagram for the enhanced CCII

The current conveyor used is a modified version of the CCII in Figure 3-5 with cascode current mirrors to enhance the output impedance.

The circuit design of the OTAs used (OTA1, OTA2, OTA3) is shown in Figure 3-6.

The OTA4 is a dual outputs OTA (DO-OTA) and the circuit design of it is shown in Figure 3-14.

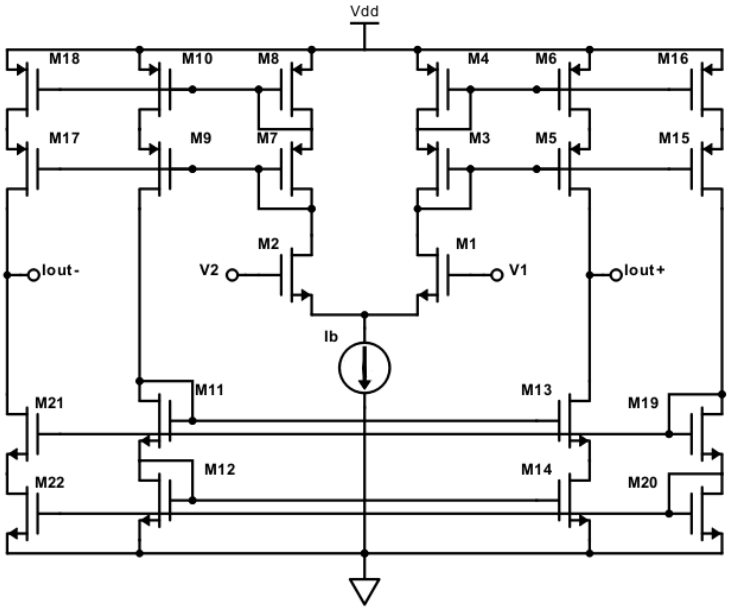

Figure 3-14 Circuit diagram for DO-OTA

The relationship between the output currents in the OTA4 is defined as follows.

$$I_{\text{out+}} = -I_{\text{out-}} = g_m V_{id} \tag{3.45}$$

It is important to find the range of the bias current such that M1 and M2 remains in subthreshold forward saturation with $I_D << I_{DO}$ and $V_{DS} \geq 4V_T$

Where I_{DO} is the saturation current and has this relation given by

$$I_{Do} = \frac{W}{L} * u * C_{ox} * V_t^2 * \frac{1-k_s}{k_s} * e^{\frac{-k_s * V_{th}}{V_t}} \tag{3.46}$$

Where V_{th} is the threshold voltage which is given on the file for every combination of length and width of the transistor, L is the transistor length, W is the width of the transistor,

k_S is the reciprocal of the slope factor equals 1/n , V_t is the thermal voltage, C_{ox} is the oxide capacitance and u is the carrier mobility which has this relation.

$$\mu = \mu_0 + \frac{L\mu 0}{L} + \frac{W\mu 0}{W} + \frac{P\mu 0}{L*W} \tag{3.47}$$

Where μ0, Lμ0, Wμ0 and Pμ0 are process parameters given from the BSIM3.3 level 49 0.18μm technology library file. There are 16 groups of parameters, each group depends on whether the length and width of the transistor falls into certain range. The range for NMOS transistor is shown in Table 3-4.

Table 3-4 NMOS transistor groups for each range of width and length

Group	Length Range		Width Range	
	Min (um)	Max (um)	Min (um)	Max (um)
1	10	20	10	900.001
2	1.2	10	10	900.001
3	0.5	1.2	10	900.001
4	0.18	0.5	10	900.001
5	10	20	1.2	10
6	1.2	10	1.2	10
7	0.5	1.2	1.2	10
8	0.18	0.5	1.2	10
9	10	20	0.5	1.2
10	1.2	10	0.5	1.2
11	0.5	1.2	0.5	1.2
12	0.18	0.5	0.5	1.2
13	10	20	0.22	0.5
14	1.2	10	0.22	0.5
15	0.5	1.2	0.22	0.5
16	0.18	0.5	0.22	0.5

Then, the parameters μ0, Lμ0, Wμ0, Pμ0 and V_{th0} which is the threshold voltage are collected from the library file and are shown in Table 3-5.

Table 3-5 Factory parameters for the MOS in 0.18µm technology

Group	Vth0	U0	pu0	wu0	lu0
1	0.4365561	0.04220339	0	0	0
2	0.4304705	0.04187289	0	0	3.291809e-09
3	0.4793240	0.04381358	0	0	1.0406079e-09
4	0.4752311	0.04335447	0	0	1.2517989e-09
5	0.4364873	0.04303590	0	-8.320099e-09	0
6	0.4303924	0.04273027	2.4756895e-15	-8.568663e-09	3.0440912e-09
7	0.4799949	0.04452649	8.0088650e-16	-7.124867e-09	9.604713e-10
8	0.4751966	0.04384084	-2.4055863e-16	-4.860856e-09	1.2758692e-09
9	0.4406337	0.03519972	0	1.0362965e-09	0
10	0.4340151	0.03482766	1.6856667e-15	8.670528e-10	3.705752e-09
11	0.4821278	0.03581186	-1.1138246e-15	3.280407e-09	2.5640821e-09
12	0.4891579	0.03980552	4.1479770e-16	-4.268465e-11	7.269945e-10
13	0.4632908	0.03533742	0	9.682726e-10	0
14	0.4576404	0.03434400	-1.3716021e-15	1.105983e-09	9.894555e-09
15	0.4985188	0.04437776	1.0146696e-15	-9.511471e-10	-1.7446106e-09
16	0.4862920	0.03710350	-1.7230291e-17	1.2921135e-09	1.6015452e-09

The thermal voltage V_t can be found using the equation below.

$$V_t = \frac{k*T}{q} \tag{3.48}$$

Where k is the Boltzmann constant equal to $1.38064852*10^{-23}$, T is the temperature in Kalvin, in room temperature it will be equal to 299.14 K and q is the electron charge equals to $1.60217662*10^{-19}$ C.

The oxide capacitance C_{ox} can be found using the given equation below.

$$C_{ox} = \frac{e_0*e_{0x}}{t_{0x}} \tag{3.49}$$

Where e_o is the vacuum permittivity equal to $8.8541878176*10^{-12}$, e_{ox} is the relative permittivity for the silicon-oxide equal to 3.9 and t_{ox} is the gate oxide thickness equal to $4.08*10^{-9}$.

The slope factor n can be found from the technology file, the NMOS has a slope factor of 1.3 and the PMOS has 1.33 for the 0.18um technology, so the reciprocal of the slope factor for NMOS is 0.77 and PMOS is 0.752

Using equation (3.47) for transistor with length of 0.3µm and width of 15µm the parameter group is number 4, the thermal voltage at room temperature is around 25.8mV. The carrier mobility can be found as below.

$$u = 0.04335447 + \frac{0.0012517989}{0.3} + \frac{0}{15} + \frac{0}{0.3*15} = 0.047527133 \qquad (3.50)$$

Combining equations (3.50) and (3.46), the saturation current I_{DO} is 2.8µA.

For transistors M1 and M2 in the OTA Figure 3-6, the transistor currents I_{D1} and I_{D2} will be halved the bias current. Then by determining the bias currents of the OTAs utilizing the ratio between the saturation current I_{DO} and the transistor current I_D in equation (3.15) to be more than 10 times.

$$\frac{I_D}{I_{DO}} \ll 1 \rightarrow \frac{I_{DO}}{I_D} > 10$$

$$\frac{I_{Do}}{I_D} > 10 \rightarrow \frac{2.8\mu A}{I_D} > 10 \rightarrow I_D < 0.28\mu A \qquad (3.52)$$

Since the bias current is double the transistor currents of M1 and M2, then the maximum bias current allowed should be less than 560nA. If the maximum multiplication factor to be around 60 times, then, the maximum bias current allowed should be around 9.3nA.

3.3.1 Simulation Results

The functionality of the proposed floating capacitance multiplier circuit in Figure 3-12 is confirmed using TANNER TSPICE simulator with 0.18µm TSMC CMOS processing

technology and BSIM3V3 level 49 MOS model. The bias currents I_b, I_{B1} and I_{B3} are 5nA. The bias current I_{B2} is kept at 300nA for the multiplication factor K of 60 and the bias current I_{B4} is swept from 5nA to 300nA for the multiplication factor M from 1 to 60, so the total multiplication factor will be swept from 60 to 3600. The circuit is operated from ±0.75V supply voltage. The capacitor C is 3pF. The expected capacitance range should be between 0.18nF to 10.8nF. The transistors aspect ratios are listed in Table 3-6.

Table 3-6 The aspect ratios of the transistors used in the proposed floating capacitance multiplier

Block	Transistor	W/L
CCII	M1 – M4	1µm / 0.5µm
	M5 – M8	1.2µm / 0.3µm
	M9 – M12	0.9µm / 0.45µm
OTA	M1 – M2	15.0µm / 0.3µm
	M3 – M10	4.0µm / 0.8µm
	M11 – M14	3.8µm / 0.9µm
OTA-D	M15 – M18	4.0µm / 0.8µm
	M19 – M22	3.8µm / 0.9µm

Plot of the simulated impedance of the proposed circuit is shown in Figure 3-15 for a total multiplication factor of 3600 compared with the theoretical value. It is seen that the working frequency is in the range between 1mHz and 5KHz, which shows that the proposed circuit is suitable for sub-hertz applications. The scaled total capacitance values have been calculated for both the ideal and simulated results and compared for observing the accuracy, the results are shown in Table 3-7 and Figure 3-16. It is seen that having a large total scaling factor of 3600 results in an error of less than 8.5%.

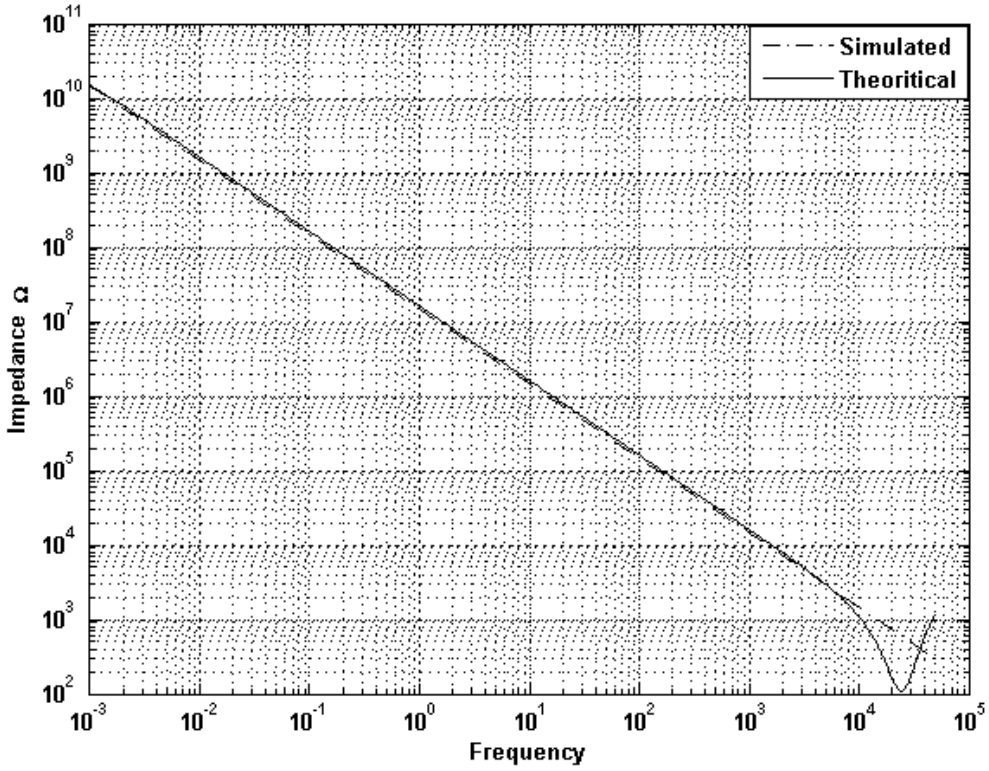

Figure 3-15 The impedance of the proposed floating capacitance simulator for M=60 and K =60

The power consumption recorded by the simulator is 2.301μW for a total multiplication factor of 3600 and 0.336μW for a total multiplication factor of 60. These values give an exquisite achievement to the proposed circuit for low power consumption, so it is suitable for low-power application especially for portable devices.

Table 3-7 Comparison between the theoretical and simulated capacitance

M = 60		Expected value of Capacitance (nF)	Simulated value (nF)	% of Error
K	Multiplied Factor			
1	60	0.18	0.176	2.453
2	120	0.36	0.347	3.661
4	240	0.72	0.687	4.555
8	480	1.44	1.363	5.357
16	960	2.88	2.701	6.220
32	1920	5.76	5.341	7.268
60	3600	10.8	9.885	8.475

The percentage of error is increasing with the increase of K because the bias current of the OTA4 is increasing which will make it closer to the saturation current of the transistors I_{DO} and hence affecting the condition in equation (3.15)

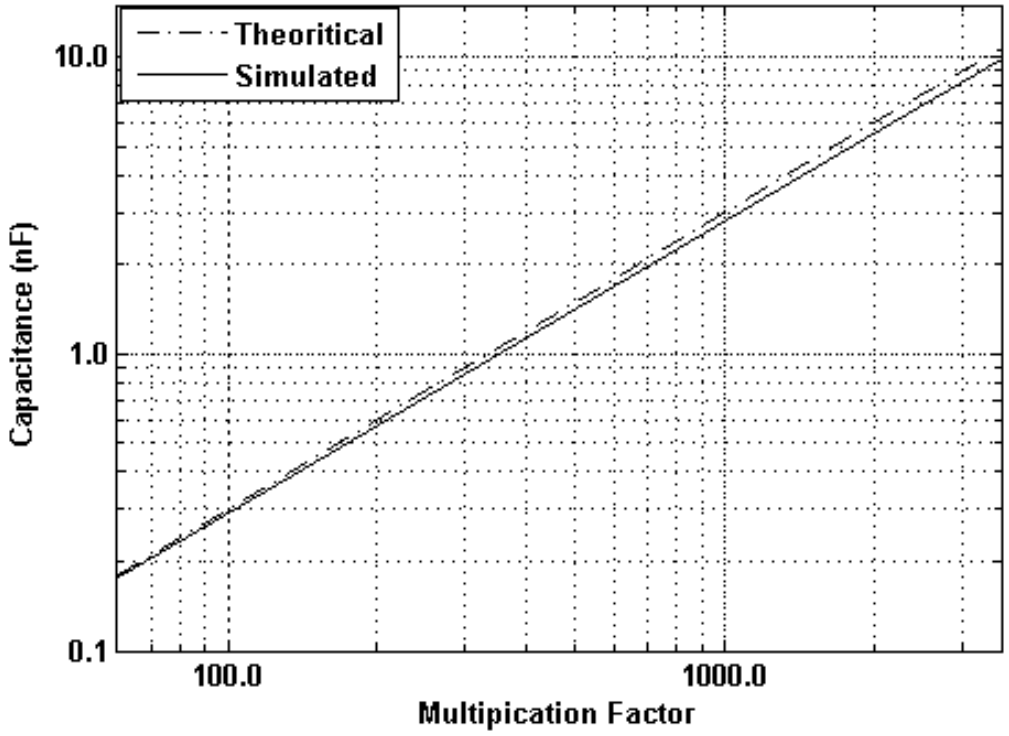

Figure 3-16 Variations between the simulated and expected values for the floating capacitance through different multiplication factor

Simulation results for temperature analysis was carried out. The temperature was swept from -25ºC to 80ºC in steps of 20ºC. The simulation result for the equivalent impedance with total multiplication factor of 3600 is shown in Figure 3-17.

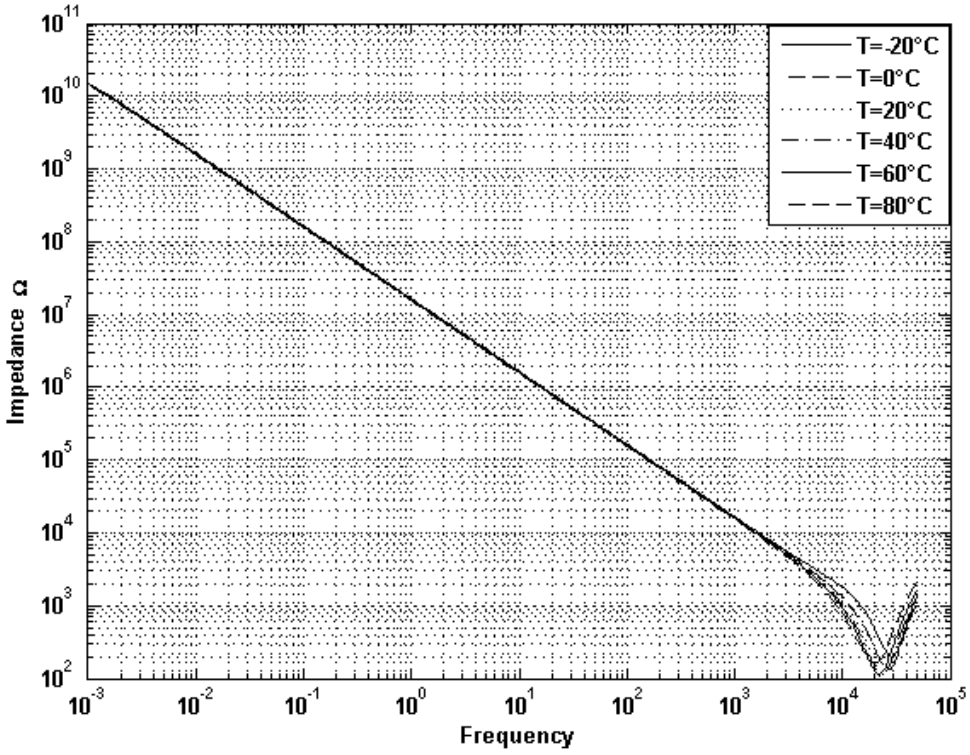

Figure 3-17 Simulation result of temperature analysis for scaling factor of 3600

It is evident that the total capacitance is insensitive to the temperature variation since all the temperature related parameters cancelled each other.

Since the design is based on the assumption of perfect matching, it is important to observe the effect of the mismatch between the transistor's parameters. Consequently, it is important to study the effect of mismatch in device dimension that may result during fabrication process. To do so, the 0.18µm BSIM3V3 level 49 technology file already supplied with all the variation in transistor parameters. To utilize these variation, Monte

Carlo analysis simulation is carried out in the TANNER T-SPICE with 100 samples. Monte Carlo simulation shown in Figure 3-18 for the equivalent total impedance where the multiplication factor of 900.

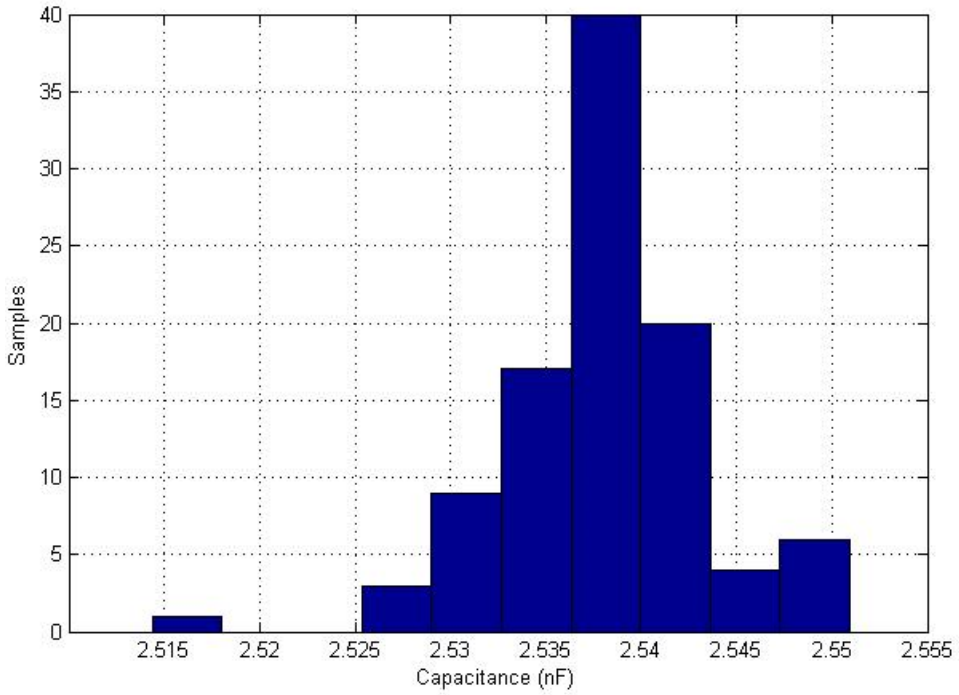

Figure 3-18 Monte Carlo simulation result for a total multiplication factor of 900

3.3.2 Non-Ideal Analysis

The previous analysis and resulted equations were carried out based on the assumption that the CCII and OTA are ideal. In this section, the effect of nonideality of these blocks will be analyzed.

For the CCII, the non-ideal relationship is shown in the following figure.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & R_X & 0 \\ 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.53}$$

Where α is the voltage coefficient and β is the current coefficient.

For the non-ideal voltage follower, the voltage at terminal X will be.

$$V_X = \alpha V_Y - I_X * R_X \tag{3.54}$$

From the circuit in Figure 3-12, since the equivalent impedance of the capacitor is much higher than R_X, hence the Z=1/sC with C is equal 3pF results in a very low current I_X, so the effect of the second term will be neglected and equation (3.54) is rewritten as:

$$V_X = \alpha V_Y \tag{3.55}$$

For the non-ideal current follower in the CCII, the current at terminal Z will be.

$$I_Z = \beta I_X \tag{3.56}$$

With this, I_{in} in the terminal Z will be equal to.

$$I_{in} = \beta \frac{V_1 - \alpha V_2}{Z_C} \tag{3.57}$$

The resulting equivalent total impedance including the non-ideal CCII parameters.

$$Z_{eq} = \frac{V_1 - V_2}{I_{\mathrm{MK+}}} = \frac{V_1 - V_2}{I_{\mathrm{MK-}}} = \frac{V_1 - V_2}{\beta \frac{V_1 - \alpha V_2}{Z_C} * M * K} = \left(\frac{V_1 - V_2}{V_1 - \alpha V_2}\right) \frac{Z_C}{\beta * M * K} \tag{3.58}$$

For OTA4, it is assumed that both the output currents are equal in magnitude, with the non-ideal case they have this relation between them.

$$I_{\mathrm{MK+}} = \gamma I_{\mathrm{MK-}} \tag{3.59}$$

The resulting equivalent total impedance including the non-ideal behavior of OTA4.

$$Z_{eq} = \frac{V_1}{\gamma I_{\mathrm{MK-}}} - \frac{V_2}{\gamma I_{\mathrm{MK+}}} = \frac{V_1}{\gamma \frac{V_1 - V_2}{Z_C} * M * K} - \frac{V_2}{\frac{V_1 - V_2}{Z_C} * M * K} = \frac{V_1 - \gamma V_2}{\gamma \frac{V_1 - V_2}{Z_C} * M * K} \quad (3.60)$$

The equivalent impedance including all the non-ideal parameters.

$$Z_{eq} = \left(\frac{V_1 - \gamma V_2}{V_1 - \alpha V_2}\right) \frac{Z_C}{\gamma * \beta * M * K} \quad (3.61)$$

The percentage of error is.

$$\%\mathrm{Error} = \left| \left(\frac{V_1/V_2 - \gamma}{V_1/V_2 - \alpha} \right) \beta - 1 \right| * 100 \quad (3.62)$$

As the modified CCII includes cascode current mirrors in the output stage, the current following error parameter β will be nearly 1.

A total error if 1.11% can be found if V_1=10mV, V_2=1mV, β=0.99 and γ=0.98 and α=0.97.

The propose floating capacitance simulator design is compared with the previous works for floating capacitance in Table 3-8.

Table 3-8 Performance comparison between the proposed circuit and previous ones

Reference	Building Block	Type	Supply Voltage	Power Consumption	Technology	# of passive elements	Tunable?	Scaling Factor
[8]	DV-CCTA	F	±2.5V	NA	BJT	2	Yes	3
[10]	DVCC	F	±0.75V	1.29mW	0.13µm	2	Yes	20
[11]	DVCCTA	F	±2V	3mW	0.5µm	1	Yes	3
[14]	FB-VDBA	F	±1V	NA	BiCMOS	0	Yes	3
[16]	OTA	F	±2.5V	0.565mW	BJT	0	Yes	100000
[19]	OTA	F	NA	0.5µW	0.35µm	1	Yes	NA
[27]	VDCC	F	±0.45V	556µW	90nm	2	No	NA
[28]	VDCC	F	±0.9V	NA	0.18µm	2	Yes	NA
[32]	CMOS	F	±0.9V	53.2µW	0.18µm	0	No	50
[37]	CMOS	F	±3V	5.28mW	0.5µm	3	Yes	10
[40]	DVCC	F	±0.2.5V	NA	0.25µm	0	Yes	15
[43]	CBTA	F	±1.5V	43.3mW	0.25µm	2	NA	NA
[44]	FB-VDBA	F	±1V	NA	BiCMOS	0	Yes	3
[47]	CMOS	F	±0.9V	53.2µW	0.18µm	0	No	NA
[48]	CMOS	F	1.8V	5.94µW	0.18µm	0	No	50
Proposed Work	OTA CCII	F	±0.75V	2.030µW @3600 times	0.18µm	0	Yes	3600

From Table 3-8, it is shown that the proposed work excelled the other designs in terms of low-power consumption except for work [27] as it consumes large silicon area and not tunable. Also, the proposed work uses less silicon area because of the absence of extra passive elements and has high tunable range (up to 3600) compared with the others except for [16] as it uses BJT which is known for their linearity.

3.3.3 Applications

The suitable applications for such tunable capacitors are biomedical ones, since biomedical signals are time records of biomedical events like heart movements or stimulated neuron.

When biomedical signals are produces, an electric potential is generated that can be measured such as Electroencephalogram (EEG) and Electrocardiogram (ECG). Large amplification for such signals is necessary since the electric potential generated from the body is in range of micro to millivolt range. Pre-filtering is needed using analog filters to attenuate undesired high frequency noise as ECG signals occupy a frequency bandwidth 1mHz -100Hz while EEG occupy 10mHz – 30Hz [52], hence the need of this work to design such filters.

The tunable capacitors are also needed in the amplification stage for controlling the gain of biomedical signals such as Chopper stabilization which is an established for suppressing offsets and drifts coming from neuro field potentials (NFP) and is shown in Figure 3-19 [53].

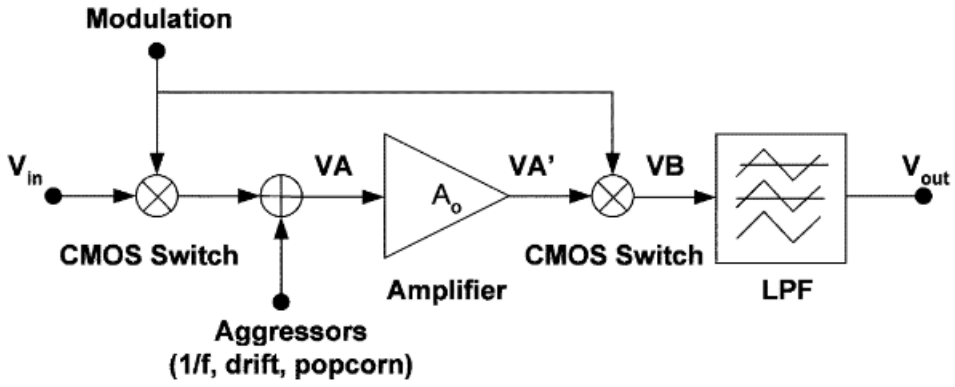

Figure 3-19 Chopper amplifier architecture

Tunable capacitors are also needed in biomedical sensor interface as implants to measure and process NFP. This interface is called analog front-end (AFE) and is shown in Figure 3-20 which consists of an instrumentation amplifier (IAMP) and an antialiasing filter, in

this case a sinc antialiasing filter (SAAF) is used [54]. The SAAF filter provides tunable gain due the tunable capacitors.

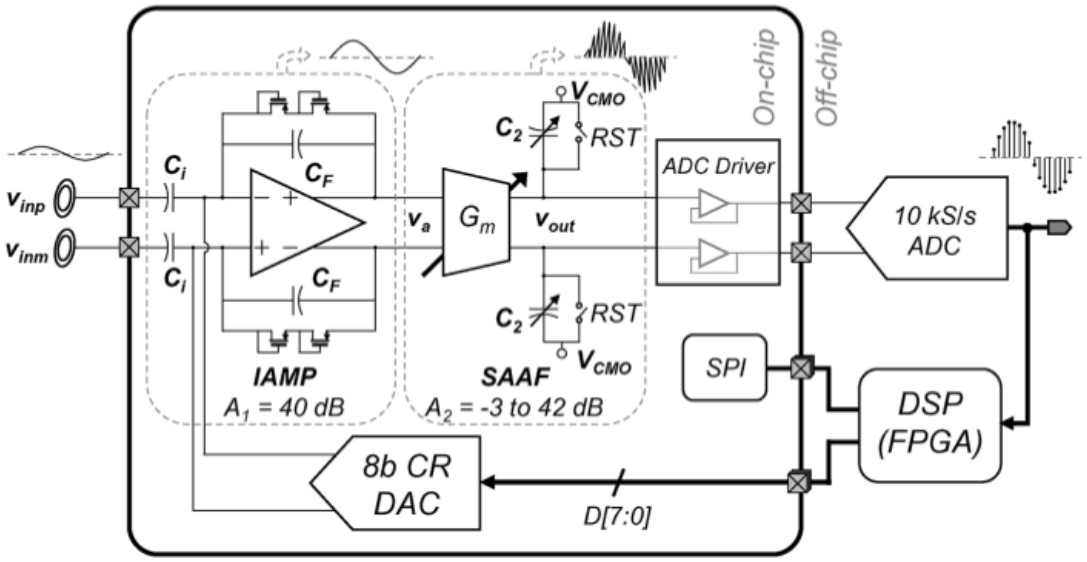

Figure 3-20 system block diagram of a biomedical sensor interface

Tunable filters are achieved with tunable capacitors and are generally used in any typical data acquisition for biomedical signals shown in Figure 3-21 [55].

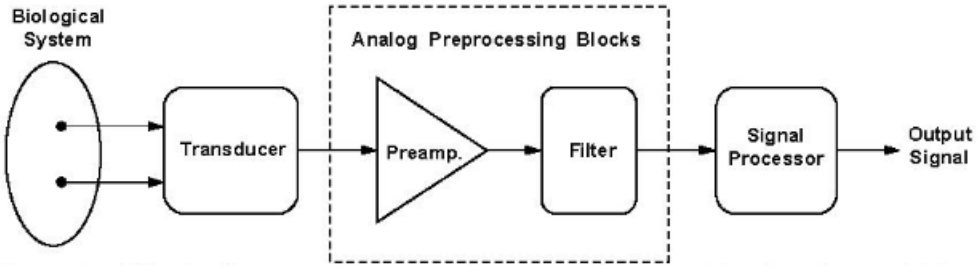

Figure 3-21 block diagram of a general-purpose bioelectric signal acquisition system

On-chip high capacitor values are used for generating low frequency on-board clock which is required for designing switched-capacitors (SC) filters that are preferred for high-performance low-frequency applications because of their high accuracy, low sensitivity to parasitic elements and has reduced harmonic distortion [55].

The performance of the floating capacitance simulator is very important in biomedical applications especially low frequency and low-power ones. To test the performance of the proposed tunable capacitance simulator, simple low-pass, high-pass and band-reject filters are used as illustrated in Figure 3-22. The resistance R_L for the low-pass filter circuit is 10MΩ, the resistance R_H from the high-pass filter is 1MΩ and the resistance R_B for the band-reject filter is 1MΩ with the inductor L equals to 100H. The frequency responses of the filters were recorded with total multiplication factor of 120, 1200 and 3600 for both simulated and expected values for the filters are shown in Figure 3-23, Figure 3-24 and Figure 3-25 respectively.

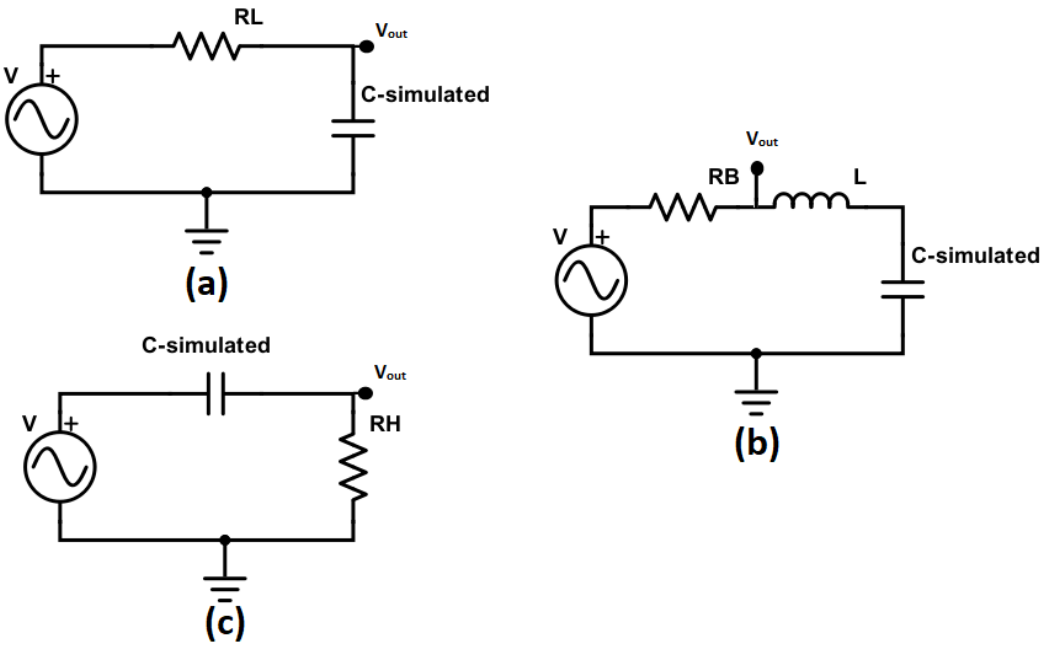

Figure 3-22 Simple filters (a) low-pass (b) band-reject (c) high-pass

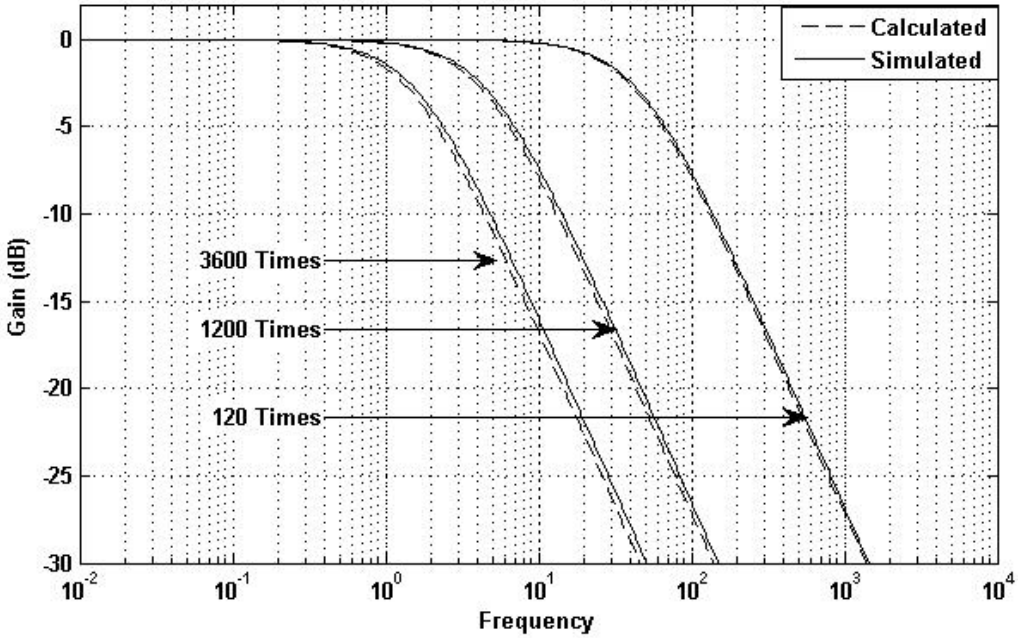

Figure 3-23 Simulation of the low-pass filter circuit with total scaling factor of 120, 1200 and 3600

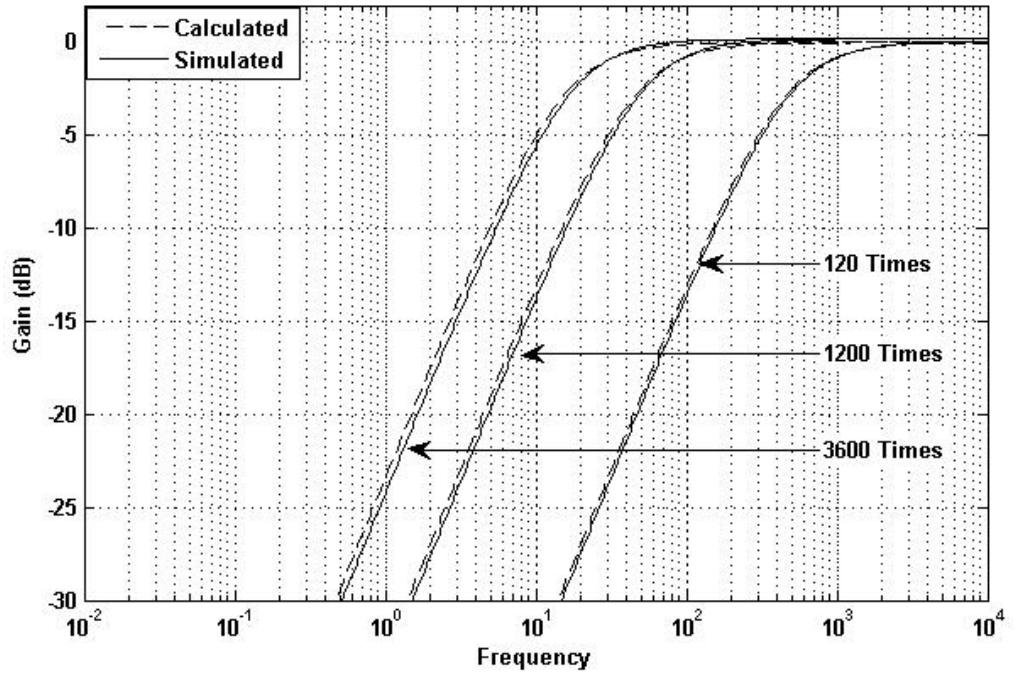

Figure 3-24 Simulation of the high-pass filter circuit with total scaling factor of 120, 1200 and 3600

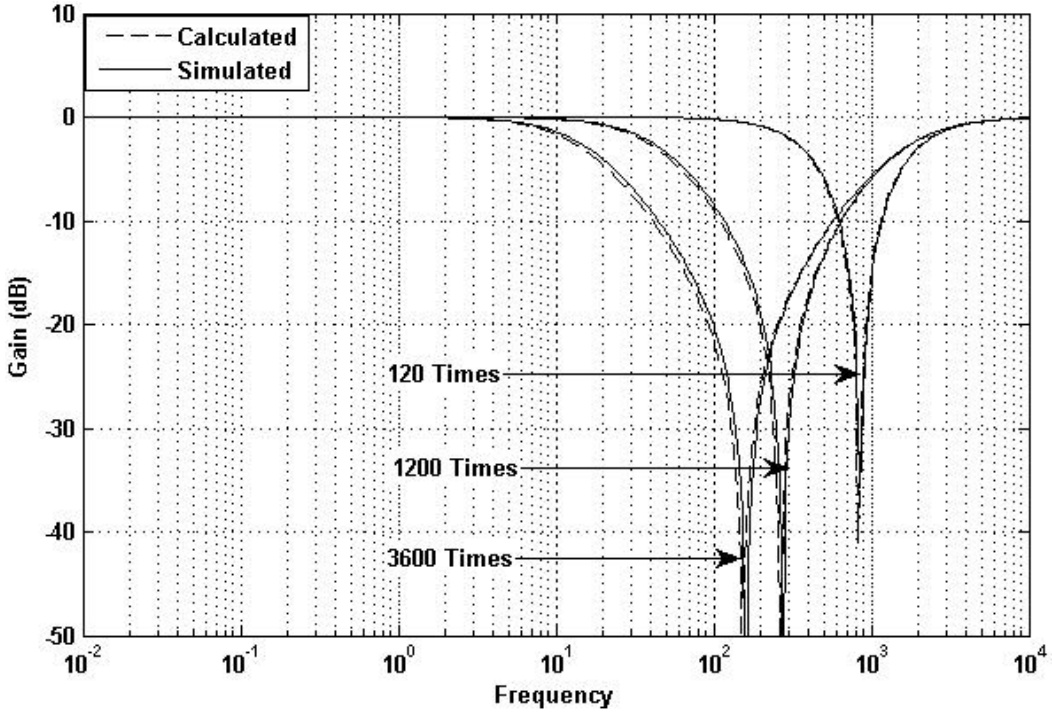

Figure 3-25 Simulation of the band-reject filter circuit with total scaling factor of 120, 1200 and 3600

It is shown that a filter with tunable cut-off frequencies can be achieved with low power consumption and good accuracy.

CHAPTER 4

CONCLUSION AND FUTUTRE WORK

4.1 Conclusions

In this thesis, a wide tunable floating and grounded capacitance multiplier design has been presented, utilizing two stages of multiplication. The design presented the ability of having a wide tuning range with maximum error less than 8.6% and is insensitive to temperature variations. The proposed design enjoys low power consumption, high accuracy, wide tunable range, high multiplication factor and small silicon area. The proposed design is designed to work in low frequency applications which suits the biomedical applications, low frequency filters and oscillators where large time constant is required.

4.2 Future Work

- Layout simulation for the proposed design if possible.
- Enhance the accuracy of the OTA design.
- Apply the proposed design in other low power application.

References

[1] P E Allen; Douglas R Holberg;, "CMOS analog circuit design" fourth edition New York : Oxford University Press, USA, 2011.

[2] Srivastava, M., Joshi, S., Srivastava, S., Goel, K., & Prasad, D. (2016). New Active Only Scaling Configuration for Grounded Passive Elements with Electronic Scaling Facility, 502–506.

[3] Engineering, T. (2016). Grounded Passive Elements, 561–565. https://doi.org/10.1109/ICMETE.2016.110

[4] Engineering, E., & Engineering, C. (n.d.). New Simple CMOS Realization of Voltage Differencing Transconductance Amplifier and Its RF Filter Application, (1), 632–637.

[5] Roy, A. (2018). A Generalized Grounded Impedance Simulator / Grounded Impedance Scaling Circuit with Electronic Tuning. 2018 5th International Conference on Signal Processing and Integrated Networks (SPIN), 771–776.

[6] Prokop, R., & Musil, V. (2014). New modern circuit block CCTA and some its applications, (January 2005).

[7] Jantakun, A. (2015). A simple grounded FDNR and capacitance simulator based-on CCTA. AEU - International Journal of Electronics and Communications, 69(6), 950–957. https://doi.org/10.1016/j.aeue.2015.03.002

[8] Jantakun, A., Pisutthipong, N., & Siripruchyanun, M. (2009). A Synthesis of Temperature Insensitive / Electronically Controllable Floating Simulators Based on DV-CCTAs, (2), 2–5.

[9] Silapan, P. (2008). Current Controlled CCTA Based- Novel Grounded Capacitance Multiplier with Temperature Compensation, 1490–1493.

[10] Alpaslan, H. (2017). DVCC-based floating capacitance multiplier design Z +, 1334–1345. https://doi.org/10.3906/elk-1509-112

[11] Tangsrirat, W. (2013). Floating simulator with a single DVCCTA, 20(April), 79–86.

[12] Unhavanich, S., Onjan, O., & Tangsrirat, W. (2016). Tunable Capacitance Multiplier with a Single Voltage Differencing Buffered Amplifier, II, 18–21.

[13] Mongkolwai, P., & Tangsrirat, W. (2016). Generalized Impedance Function Simulator Using Voltage Differencing Buffered Amplifiers (VDBAs), II, 16–19.

[14] Pimpol, J., Channumsin, O., & Tangsrirat, W. (2016). Floating Capacitance Multiplier Circuit Using Full-Balanced Voltage Differencing Buffered, II, 16–19.

[15] M. T. Ahmed, I. A. Khan and N. Minhaj, "Novel electronically tunable C-multipliers," in Electronics Letters, vol. 31, no. 1, pp. 9-11, 5 Jan. 1995.doi: 10.1049/el:19950018

[16] Jaikla, W., & Siripruchyanan, M. (2006). An electronically controllable capacitance multiplier with temperature compensation. 2006 International Symposium on Communications and Information Technologies, ISCIT, 356–359. https://doi.org/10.1109/ISCIT.2006.340064

[17] I. A. Khan and M. T. Ahmed, "OTA-based integrable voltage/current-controlled ideal C-multiplier," in Electronics Letters, vol. 22, no. 7, pp. 365-366, 27 March 1986.doi: 10.1049/el:19860248

[18] Padilla-cantoya, I., Furth, P. M., & Member, S. (2015). Enhanced Grounded Capacitor Multiplier and Its Floating Implementation for Analog Filters, 62(10), 962–966.

[19] Kulej, T. (2009). Regulated Capacitance Multiplier in CMOS Technology, (3), 4–7.

[20] Padilla-Cantoya, I. (2013). Capacitor multiplier with wide dynamic range and large multiplication factor for filter applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 60(3), 152–156. https://doi.org/10.1109/TCSII.2013.2240814

[21] D. V. Kamath, "Novel DO-OTA based current-mode grounded capacitor multiplier," 2018 2nd International Conference on Inventive Systems and Control (ICISC), Coimbatore, 2018, pp. 1187-1190.doi: 10.1109/ICISC.2018.8398992

[22] D. V. Kamat, "Novel large value grounded capacitor realizations using OTAs and small capacitors," 2017 International Conference On Smart Technologies For Smart Nation (SmartTechCon), Bangalore, 2017, pp. 1195-1200.doi: 10.1109/SmartTechCon.2017.8358557

[23] C. Rivera-Escobar, F. Silva-Del-Rosario, M. Silva and I. Padilla-Cantoya, "Multiple stage capacitor multiplier using dual-output differential amplifiers," 2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS), Cusco, 2013, pp. 1-3.doi: 10.1109/LASCAS.2013.6519076

[24] J. Aguado-Ruiz, J. Hernandez-Alvidrez, A. J. Lopez-Martin, R. G. Carvajal and J. Ramirez-Angulo, "Programmable capacitance scaling scheme based on operational transconductance amplifiers," in Electronics Letters, vol. 45, no. 3, pp. 159-161, 29 January 2009.doi: 10.1049/el:20093596

[25] Biolek, Dalibor & Senani, Raj & Biolkova, Viera & Kolka, Zdenek. (2008). Active Elements for Analog Signal Processing: Classification, Review, and New Proposals. Radioengineering. 17.

[26] A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek and K. Vrba, "Floating capacitance multiplier simulator for grounded RC colpitts oscillator design," 2015 International Conference on Applied Electronics (AE), Pilsen, 2015, pp. 93-96.

[27] A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek and K. Vrba, "Application possibilities of VDCC in general floating element simulator circuit," 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, 2015, pp. 1-4.doi: 10.1109/ECCTD.2015.7300064

[28] M. Srivastava, P. Bhanja and S. F. Mir, "A new configuration for simulating passive elements in floating state employing VDCCs and grounded passive elements," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, 2016, pp. 1-4.doi: 10.1109/ICPEICES.2016.7853402

[29] B. Metin, M. Atasoyu, E. Arslan, N. Herencsar and O. Cicekoglu, "A tunable immitance simulator with a voltage differential current conveyor," 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, 2017, pp. 739-742.doi: 10.1109/MWSCAS.2017.8053029

[30] Ashish Gupta, Raj Senani, D. R. Bhaskar, and A. K. Singh, “New OTRA-Based Generalized Impedance Simulator,” ISRN Electronics, vol. 2013, Article ID 907597, 10 pages, 2013. https://doi.org/10.1155/2013/907597.

[31] AMPLIFIER, I.B., & Tangsrirat, W. (2017). Resistorless Tunable Capacitance Multiplier Using Single Voltage Differencing Inverting Buffered Amplifier.

[32] F. Matsumoto, T. Fujii, S. Nishioka, T. Abe and T. Ohbuchi, "Design of a floating-type impedance scaling circuit for large capacitances," 2013 International Symposium on Intelligent Signal Processing and Communication Systems, Naha, 2013, pp. 391-396.doi: 10.1109/ISPACS.2013.6704581

[33] Kafe, F. & Psychalinos, C. Analog Integr Circ Sig Process (2014) 78: 217. https://doi.org/10.1007/s10470-013-0165-0

[34] Myderrizi, I., & Zeki, A. (2014). Electronically tunable DXCCII-based grounded capacitance multiplier. AEU - International Journal of Electronics and Communications, 68(9), 899–906. https://doi.org/10.1016/j.aeue.2014.04.013

[35] Khan, A. a., Bimal, S., Dey, K. K., & Roy, S. S. (2002). Current conveyor based R- and C- multiplier circuits. AEU - International Journal of Electronics and Communications, 56(5), 312–316. https://doi.org/10.1078/1434-8411-54100121

[36] Jelle Van Rethy, Georges Gielen, Capacitance-Controlled Oscillator with Enhanced Tuning Range using Negative Capacitance for Time-Based Sensor Interfaces, Procedia Engineering, Volume 47, 2012, Pages 21-24, ISSN 1877-7058, https://doi.org/10.1016/j.proeng.2012.09.074.

[37] I. Padilla-Cantoya, "Low-Power High Parallel Load Resistance Current-Mode Grounded and Floating Capacitor Multiplier," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 1, pp. 16-20, Jan. 2013. doi: 10.1109/TCSII.2012.2234923

[38] J. Choi, J. Park, W. Kim, K. Lim and J. Laskar, "High multiplication factor capacitor multiplier for an on-chip PLL loop filter," in Electronics Letters, vol. 45, no. 5, pp. 239-240, 26 February 2009. doi: 10.1049/el:20092874

[39] J. A. Ruiz, A. Lopez-Martin and J. Ramirez-Angulo, "Three novel improved CMOS capacitance scaling schemes," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, Paris, 2010, pp. 1304-1307. doi: 10.1109/ISCAS.2010.5537257

[40] Nahhas, A.M. (2013). Digitally Programmable Floating Impedance Converter using CMOS-DVCC.

[41] J. Silva-Martinez and A. Vazquez-Gonzalez, "Impedance scalers for IC active filters," ISCAS '98. Proceedings of the 1998 IEEE International Symposium on Circuits and Systems (Cat. No.98CH36187), Monterey, CA, 1998, pp. 151-154 vol.1. doi: 10.1109/ISCAS.1998.704211

[42] G. A. Rincon-Mora, "Active capacitor multiplier in Miller-compensated circuits," in IEEE Journal of Solid-State Circuits, vol. 35, no. 1, pp. 26-32, Jan. 2000. doi: 10.1109/4.818917

[43] Ayten, Umut & Sagbas, Mehmet & Herencsar, Norbert. (2012). Novel Floating General Element Simulators Using CBTA. Radioengineering. 21. 11-19.

[44] Channumsin, Orapin & Tangsrirat, Worapong. (2016). Electronically tunable floating capacitance multiplier using FB-VDBAs. Enginrring Letters. 24. 365-369.

[45] AMPLIFIER, I.B., & Tangsrirat, W. (2017). Resistorless Tunable Capacitance Multiplier Using Single Voltage Differencing Inverting Buffered Amplifier.

[46] W. Germanovix, E. Bonizzoni and F. Maloberti, "Capacitance Super Multiplier for Sub-Hertz Low-Pass Integrated Filters," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 3, pp. 301-305, March 2018. doi: 10.1109/TCSII.2017.2691010

[47] F. Matsumoto, T. Fujii, S. Nishioka, T. Abe and T. Ohbuchi, "Design of a floating-type impedance scaling circuit for large capacitances," 2013 International Symposium on Intelligent Signal Processing and Communication Systems, Naha, 2013, pp. 391-396. doi: 10.1109/ISPACS.2013.6704581

[48] Matsumoto, F., Nishioka, S., Ohbuchi, T. et al. Analog Integr Circ Sig Process (2015) 85: 253. https://doi.org/10.1007/s10470-015-0569-0

[49] L. J. Stotts, "Introduction to implantable biomedical IC design," in IEEE Circuits and Devices Magazine, vol. 5, no. 1, pp. 12-18, Jan. 1989. doi: 10.1109/101.17234

[50] M. A. Al-Absi, E. S. Al-Suhaibani and M. T. Abuelma'tti, "A new controllable CMOS impedance scaler," 2016 13th International Multi-Conference on Systems, Signals & Devices (SSD), Leipzig, 2016, pp. 695-698. doi: 10.1109/SSD.2016.7473774

[51] Moro-Frías D. “Design and Applications of CMOS Current Conveyors”, 2008-06, Instituto Nacional de Astrofísica, Óptica y Electrónica, http://inaoe.repositorioinstitucional.mx/jspui/handle/1009/543

[52] J. Webster, “Medical Instrumentation: Application and Design”, John Wiley, 3rd Edition, 1998.

[53] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley and A. Kelly, "A 2μW 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2934-2945, Dec. 2007. doi: 10.1109/JSSC.2007.908664

[54] J. L. Bohorquez, M. Yip, A. P. Chandrakasan and J. L. Dawson, "A Biomedical Sensor Interface With a sinc Filter and Interference Cancellation," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 746-756, April 2011. doi: 10.1109/JSSC.2011.2108128

[55] C. Hsu, M. Ho, Y. Wu and T. Chen, "Design of Low-Frequency Low-Pass Filters for Biomedical Applications," *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, 2006, pp. 690-695. doi: 10.1109/APCCAS.2006.342101

Vitae

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