BRIDGE TYPE FAULT CURRENT LIMITERS FOR FAULT RIDE THROUGH CAPABILITY ENHANCEMENT OF VSC-HVDC SYSTEMS

BY

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A Dissertation Presented to the

DEANSHIP OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

DOCTOR OF PHILOSOPHY

In

ELECTRICAL ENGINEERING

APRIL 2018

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN- 31261, SAUDI ARABIA

DEANSHIP OF GRADUATE STUDIES

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Dedicated To

My Parents

My Brothers

My Wife and Children

ACKNOWLEDGMENTS

First of all, I would like to thank my creator and sustainer almighty ALLAH for giving me chance to complete this thesis work. I am also highly grateful to my most beloved Prophet MOHAMMAD (peach be upon him) for giving message that nothing can come into exist without the mercy and blessing of ALLAH.

I would like to thank my supervisor Dr. M. A. Abido for his continuous support and motivation towards novel research work. He spent a lot of time in understanding my problems and driving me towards a finest solution. He always helped me in finding gaps in my field of study and filling those gaps through novel work. He supported me financially by the funded project. I could not have imagined having a better supervisor for my PhD thesis than him. The work done in this research could not have been possible without his continuous supervision and guidance.

I would like to thank my thesis co-adviser Dr. Z. M. Al-Hamouz for his guidance towards this thesis work.

I would like to thank Dr. Ibrahim Mohamed El-Amin, Dr. Ibrahim Omar Habiballah, and Dr. Salim Ibrir whose graduate courses helped me a lot to gain huge technical knowledge in solving research problems.

I would like to acknowledge all the supports like scholarship, well equipped labs, library facility, full furnished student housing, and free medical service provided by King Fahd University of Petroleum and Minerals.

I would like to thank all members of real time digital simulator (RTDS) support team for helping me to solve many problems related to RTDS simulation.

I would like to thank my all colleagues and friends for supporting me by encouraging and helping through all possible ways.

Last but not least, I am highly indebted to my parents, brothers, mother-in-law, and father-in-law and all relatives for their supports by all possible means. My acknowledgement will remain unfinished without thanking my wife Rebeka Sultana, my daughters Hafsa and Fatema and my son Muhammad Talha for giving me free will to do my work by sacrificing their valuable weekends.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

1LG	**:**	Single Line to Ground Fault
2LG	**:**	Double Line to Ground
3LG	**:**	Three Line to Ground Fault
AC	**:**	Alternating Current
BFCL	**:**	Bridge Type Fault Current Limiter
D	**:**	Duty cycle
DC	**:**	Direct Current
DFIG	**:**	Doubly Fed Induction Generator
DG	**:**	Distributed Generation
DLFCL	**:**	DC Link Fault Current Limiter
FACTS	**:**	Flexible AC Transmission System
FCL	**:**	Fault Current Limiter
FFF	**:**	Feed Forward Function
FRT	**:**	Fault Ride Through
GVSC	**:**	Grid Voltage Source Converter
HTS	**:**	High Temperature Superconductor
HVDC	**:**	High Voltage DC
IGBT	**:**	Insulated Gate Bipolar Transistor
LCC	**:**	Line Commutated Converter
LL	**:**	Line to Line
MBFCL	**:**	Modified Bridge Type Fault Current Limiter
MOPSO	**:**	Multi Objective Particle Swarm Optimization

MTDC	**:**	Multiterminal HVDC
ORC	**:**	Over Current Relay
PCC	**:**	Point of Common Coupling
PI	**:**	Proportional Integral
PLL	**:**	Phase Locked Loop
PMSG	**:**	Permanent Magnet Synchronous Generator
PRBFCL	**:**	Parallel Resonance Bridge Fault Current Limiter
RTDS	**:**	Real Time Digital Simulator
RVSC	**:**	Rotor Voltage Source Converter
SDBR	**:**	Series Dynamic Braking Resistor
SFCL	**:**	Superconducting Fault Current Limiter
SVSC	**:**	Stator Voltage Source Converter
VR-BFCL	**:**	Variable Resistive Bridge Type Fault Current Limiter
VSC	**:**	Voltage Source Converter
WTVSC	**:**	Wind Turbine Voltage Source Converter

ABSTRACT

Full Name : [Md Shafiul Alam]

Thesis Title : [Bridge Type Fault Current Limiters for Fault Ride Through Capability Enhancement of VSC-HVDC Systems]

Major Field : [Electrical Engineering]

Date of Degree : [April 2018]

In electric power industry, alternating-current (AC) system has been overwhelmingly dominant over the direct-current (DC) option for long time. However, this scenario is changing in recent years as DC systems are playing an ever increasing role in the overall power systems due to several potential benefits: long distance water crossing, lower losses, controllability, lesser corona loss, and less insulation. Voltage source converter (VSC) based high voltage direct current (HVDC) transmission is attracting research interests for several benefits such as self-regulating control of active and reactive power, improved power quality, comfortable integration of large-scale wind farm, and easy operation with weak AC grid, no reactive power demand, and less operational cost. However, regardless of the numerous advantages, VSC-HVDC systems face difficulties in dealing with different grid faults due to current flow through the antiparallel diodes as well as discharge of DC link capacitors. Fault ride through (FRT) capability enhancement is one of the main requirements for grids connected and wind farm integrated VSC-HVDC systems.

A prospective solution to the fault problems mentioned above is to employ fault current limiters. Different categories of fault current limiter such as resistive, inductive, superconducting, flux-lock, DC reactor, and resonance fault current limiter (FCL) have

been presented for limiting fault current as well as improving stability of power system. Among different types of FCLs non-superconducting bride-type fault current limiter (BFCL) is new technology having the capability of limiting fault current as well as improving dynamic performance of the power grid.

This research proposes BFCL-based control strategy for VSC-HVDC systems in order to limit fault current and enhance fault ride through capability as well as stability. Both grids connected and wind farms integrated VSC-HVDC systems are developed and designed with BFCL. BFCL controller is developed to limit the fault current during the inception of system disturbances with optimal design of BFCL parameters. Real and reactive power controllers for the VSC-HVDC are proposed based on current control mode. One of the voltage source converters in HVDC system controls DC link voltage by outer controller. Outer DC link voltage control is proposed by a feedback mechanism such that net power exchange with DC link capacitor is zero. Two grids connected VSC-HVDC system and several wind farms such as fixed speed wind farm and doubly fed induction generator (DFIG) wind farm integrated VSC-HVDC systems are considered. In the proposed control scheme of DFIG, constant capacitor voltage is maintained by the stator VSC (SVSC) controller while current extraction or injection is achieved by rotor VSC (RVSC) controller. Grids connected and wind farm integrated VSC-HVDC systems along with the proposed BFCL and associated controllers are implemented in real time digital simulator (RTDS). Symmetrical three phase as well as different types of unsymmetrical faults are applied in the systems in order to show the effectiveness of the proposed BFCL solution. DC link voltage fluctuation, fault current, machine speed and active power oscillations are greatly reduced with the proposed BFCL control technique.

Another significant feature of this work is that the performance of the proposed control strategy of VSC-HVDC systems with BFCL is compared with the traditional control techniques. Comparative results show that the proposed BFCL based control technique is superior over traditional techniques in limiting fault current as well as improving system FRT capability.

ملخص الرسالة

الاسم الكامل: مـد شفيع ال علام

عنوان الرسالة: التقنية الذكية للإرجاع الذكي للشبكات المصغرة

التخصص: الطاقة الكهربائية

تاريخ الدرجة العلمية: ابريل 2018

عالميا, كان نظام التيار المتردد هو المهيمن في الصناعات الكهربية اذا ما قورن بنظام التيار المستمر لعدة عقود. هذا السيناريو ما لبث ان تغير مع ظهور مزايا فريدة لنظام التيار المستمر متمثلة في: المفاقيد الاقل, التحكمية العالية و الاحتياج لعازلية اقل. جذب محول مصدر الجهد (VSC) المعتمد في طريقه عمله على التيار المستمر العالي الجهد (HVDC) انتباه الباحثين لعدة مزايا متضمنه في هذا النظام, مثل التحكم الذاتي في تنظيم الطاقة, جودة الطاقة العالية, سهولة استعمال انظمة الطاقة المعتمدة على الرياح, سهولة التشغيل في شبكات التيار المتردد الضعيفة و قلة التكلفة التشغيلية. و لكن مع كل هذه المزايا, تواجه هذه الانظمة عدة صعوبات في التعامل مع اخطاء الشبكه المختلفه. يعتبر تحسين الصدع من خلال تحسين القدرة (Fault Ride Through) أحد المتطلبات الرئيسية لأنظمة VSC-HVDC المتصلة بانظمة الرياح. احد الحلول المقترحة هو استخدام محددات تيار العطل (Fault Current Limiters). تم تقديم فئات مختلفة من هذه المحددات للحد من المشاكل الحالية وكذلك تحسين استقرارية نظام الطاقة. من بين الانواع المختلفة لهذه المحددات, هناك ما يعرف ب non-superconducting bride-type fault current limiter (BFCL), وهي تقنية جديدة تساعد في الحد من تيار العطل وكذلك تحسين الأداء الديناميكي لشبكة الطاقة.

يقترح هذا البحث إستراتيجية التحكم المعتمدة على BFCL لأنظمة VSC-HVDC من أجل تحسين استقرارية النظام مع وجود أنظمة الرياح. تم اقتراح وحدات تحكم طاقة حقيقية ومتفاعلة (Real and Reactive power) لـ VSC-HVDC بناءً على وضع التحكم الحالي(Current operation mode). يتحكم أحد محولات مصدر الجهد في نظام HVDC في جهد الوصلة المستمر (DC link voltage) بواسطة وحدة تحكم خارجية. تعمل وحدة التحكم الخارجية بواسطة آلية التغذية المرتدة بحيث يكون صافي تبادل الطاقة مع مكثف الوصلة (DC link capacitor) صفرًا. تم اعتبار شبكتين متصلتين بنظام VSC-HVDC والعديد من مزارع الرياح مثل مزرعة الرياح ذات السرعة الثابتة ومولد الرياح ذو التغذية المزدوجة (DFIG). تم تصميم الشبكات ومزرعة الرياح المزودة بأنظمة VSC-HVDC جنبا إلى جنب مع BFCL المقترح وأجهزة التحكم المرتبطة به في نظام المحاكاة الرقمية في الوقت الحقيقي (RTDS). تم تطبيق مجموعه من الاختبارات المختلفة من أجل اظهار فعالية النظام المقترح, حيث وجد أن تقلب الجهد الكهربي للتيار المستمر، تيار العطل، و التقلبات في سرعة الماكينة وتذبذبات الطاقة النشطة تقل بصورة كبيرة بتقنية التحكم BFCL المقترحة.

CHAPTER 1

INTRODUCTION

1.1 Background

Nowadays, transmission lines are being stressed to transfer larger amounts of power, much closer to thermal limit, than they were considered when built. Gradually and steadily, power resources are being limited and more uncertain and variable. Due to continuous depletion of fossil fuel as well as perpetual escalation of energy demand, research on renewable energy resources has been hot topic in recent years. Among the several renewable energy resources wind energy has drawn substantial attention of the researchers due to its maximum power point tracking capability, high efficiency, independent control of active and reactive power, and improved power quality. High voltage direct current (HVDC) system has been evolved as optimum solution for renewable energy integration and long-distance power transmission especially voltage source converter based HVDC (VSC-HVDC). Compared to traditional line commutated converter HVDC (LCC-HVDC), VSC-HVDC system has several potential benefits, for instance, independent control of active and reactive power, high power quality, lower losses and less insulation material for DC cable [1,2]. Additionally, nowadays, different problems faced by power networks such as network congestions and grid re-

enforcements are resolved by VSC-HVDC [3]. Mainly two-level and multi-level VSC topologies are presented in the literature [4,5] for VSC-HVDC transmission system.

Nevertheless, in spite of several potential benefits, a VSC-HVDC system is more defenceless to AC/DC faults than classic LCC-HVDC system. Level of fault current increases several times of normal current after the appearance of fault in VSC-HVDC system which may have serious impact on highly cost converters and other parts of the system. Designing protection scheme for VSC-HVDC is of utmost concern and researchers have proposed many possible solutions. To keep the fault current within the permissible limit, application of fault current limiters is considered as one of the prospective solutions. Fault current limiters can supress the excessive current during the response time of circuit breakers by dissipating substantial amount of fault energy. In this way, fault current limiters protect power electronic converters and other parts of the system from possible damage and reduce the current interruption stress on circuit breakers. Mostly, superconducting [6,7] and non-superconducting [8] fault current limiters have been employed in power systems.

Due to fast response superconducting fault current limiters have been proposed in HVDC system in the literature [9–12]. However, superconducting fault current limiters have several shortcomings such as big size, high cost and heavy weight, magnetic field interference with neighboring sensitive devices, high circulating and leakage current, long recovery time, and loss in normal mode [13,14] .

Application and feasibility analysis of different superconducting fault current limiters (SFCLs) have been widely examined and their operating performance has been fully

explored in AC grids [15–17]. Furthermore, some of SFCLs have been studied in VSC-HVDC system [18,19]. However, their detailed analysis and feasibility study in the VSC-HVDC networks has not been investigated thoroughly.

Another type of fault current limiter is non-superconducting one which has low implementation cost, low loss, and low voltage drop. Recently a new non-superconducting bridge type fault current limiter (BFCL) has been proposed to limit fault current as well as improve fault ride through (FRT) capability [15,20–24]. However, this new non-superconducting low cost BFCL technology has not been examined as yet in enhancing dynamic stability of VSC-HVDC system. Thus, BFCL presents a potential solution in reducing fault current, DC link voltage fluctuation, power oscillation and machine speed deviation as well as improving overall FRT operation of VSC-HVDC system with minimal cost.

Given this brief background, this dissertation proposes an efficient control technique for VSC-HVDC system with bridge type fault current limiter which limits fault current and improves FRT capability of the system. Two grids connected as well as fixed and variable speed doubly fed induction generator based wind farms integrated VSC-HVDC systems are considered. Control strategies are proposed and implemented to track maximum power for a wide range of wind speed variation. Control technique is also proposed for BFCL to insert resistance and inductance during the inception of fault in order to limit fault current within the permissible limit of converters. Active power flow between two grids or point of common coupling and wind farms has been considered to design the parameters of BFCL. The advantage of the proposed control is two-folds such as it is superior over traditional control and less complicated as well as easy execution.

To evaluate the performance of the proposed control for VSC-HVDC based on BFCL, its performance is compared with that of the conventional controllers. The proposed control techniques outperforms existing techniques in limiting fault current as well as improving FRT capability. Several index parameters are calculated and compared to show the improvement in system performance. Real time digital simulator (RTDS) has been used to implement BFCL, VSC-HVDC, wind farms and their associated controllers.

1.2 Dissertation Motivations

HVDC system has been evaluated as the optimum solution for the renewable energy integration especially winds energy to existing AC grid and long distance grid connection. HVDC system has several advantages that cannot be achieved in HVAC system such as independent control of active and reactive power, low transmission loss, and asynchronous operation. However, HVDC system faces serious problem in dealing with both AC and DC side faults compared to traditional HVAC system [25–27]. In case of fault condition, the converters are needed to trip off by AC circuit breakers; but, the fault current rise time of HVDC system is extremely faster than interrupting time of AC circuit breaker [1].

Taking all these issues in hand, this thesis proposes an efficient control technique for VSC-HVDC system with bridge type fault current limiter to reduce fault current, DC link voltage fluctuation, power oscillation and machine speed deviation. Control techniques are developed to insert optimum values of resistance and reactance to limit fault current within permissible limit of converters. Active power and reactive power are controlled independently based on current control mode. DC link voltage controller is designed so

that the net power exchange with DC capacitor is zero. VSC-HVDC controllers are designed for both grids connected mode and wind farms integrated mode. Several wind energy harvesting techniques are adopted and controllers for them are designed with VSC-HVDC such as fixed speed wind and doubly fed induction generator (DFIG) wind farms. Both balanced and unbalanced faults are applied on the most critical parts of this VSC-HVDC system to show the effectiveness of this BFCL based controller on transient stability and fault ride through (FRT) capability enhancement.

1.3 Dissertation Objectives

This dissertation aims at developing an efficient control strategy for voltage source converter-high voltage DC (VSC-HVDC) with non-superconducting fault current limiter placed in the system. VSC-HVDC system will be considered for two different modes: two grids connected mode and wind farms integrated mode. The developed controller will be implemented in real time digital simulator (RTDS).

The proposed control strategy augment transient stability and fault ride through (FRT) capability of VSC-HVDC system. DC link voltage fluctuation, fault current, machine speed, and power oscillation are reduced with the proposed control techniques. The specific objectives are as follows:

1. Developing a dynamic model of a VSC-HVDC system with bridge type fault current limiter.
2. Designing efficient control techniques for the VSC-HVDC systems.
3. Developing dynamic model for wind farm and designing controllers to integrate wind farms with VSC-HVDC system.

4. Designing parameters for bridge type fault current limiters.
5. Developing fault detection and fault current limiter activation techniques in order to augment FRT capability of grids connected and wind farms integrated VSC-HVDC systems.

1.4 Dissertation Methodology

The aim of this dissertation is to develop and implement efficient control strategies for VSC-HVDC system in both grids connected mode and wind farm integrated mode with bridge fault current limiter so that system dynamic performance and stability are improved. The HVDC plants and associated controllers are implemented in real time digital simulator (RTDS). The developed control technique is capable to reduce fault current and improve FRT capability of the VSC-HVDC systems. Different phases for execution of this thesis are listed below:

1. Conducting a comprehensive literature review on VSC-HVDC system and its control techniques, wind power integration techniques with VSC-HVDC system, existing methods to enhance fault ride through (FRT) capability of VSC-HVDC systems, feasibility analysis of fault current limiters on dynamic performance improvement of VSC-HVDC systems.
2. Developing dynamic models for VSC-HVDC systems, developing models for fixed speed wind farm, doubly fed induction generator based variable speed wind farms, fault current limiters, and integration of wind farms and VSC-HVDC with bridge type fault current limiters.

3. Designing controllers for VSC-HVDC systems to control active and reactive power independently based on the developed models with current control mode. Designing controllers to control DC link voltage of the HVDC systems. Designing controllers to track maximum power for the wind generation systems. Designing controllers to integrate wind farms with the VSC-HVDC systems. Designing the parameters for bridge type fault current limiters and developing control techniques for activation and deactivation of bridge type fault current limiters based on appearance of faults in the system.
4. Conducting real time simulation on the developed models and associated controllers with real time digital simulator (RTDS). Applying different faults such as single line to ground fault, line to line fault and double line to ground faults on the systems in order to show the effectiveness of the proposed control techniques. Comparing proposed control methods with existing technique to show the superiority of the proposed control techniques with bridge type fault current limiter.

1.5 Dissertation Contributions

The main contributions of this research is to develop an efficient controller for grids connected and wind farms integrated VSC-HVDC systems with non-superconducting low cost bridge type fault current limiters. The specific contributions are:

- A controller is developed to control bidirectional active power flow between two grids through HVDC link depending on reference command.
- A controller is developed to maintain DC link voltage to a pre-specified value.

- A controller is developed to track maximum power from wind turbine and deliver to the system.
- The parameters of the bridge type fault current limiters are determined based on pre-fault power flow through each phase.
- The controllers for wind farm side converters and grid side converters for wind farms systems are developed and designed to deliver power to the grid through HVDC link.
- A controller is developed to sense system faults and activate fault current limiters through insertion of desired resistance and reactance in order to reduce fault current within the permissible limit of voltage source converter and hence it increases systems fault ride through (FRT) capability by minimizing DC link voltage fluctuation, active power oscillation and machine speed deviation.

1.6 Dissertation Organization

This thesis contains several chapters. Summary of each chapter is outlined as below.

- The chapter 1 is an introduction chapter which provides background and motivations of this thesis. It also provides research methodology and main contributions of this research.
- Chapter 2 provides detailed literature review on existing control techniques of VSC-HVDC systems. The advantages and disadvantages of these control techniques are highlighted. Different fault current limiters in power systems are discussed. The fault ride through (FRT) operation of VSC-HVDC system is

discussed with different fault current limiters. Finally, several gaps are pointed out those are to be filled by this research work.

- Chapter 3 presents fault current limiting capability of VSC-HVDC system in two grid connected mode with model predictive control approach of bridge type fault current limiter. Dynamic model for VSC-HVDC system is developed and bridge type fault current limiters are proposed for VSC-HVDC system with finite control set model predictive control technique. Real time digital implementation results are presented at the end of this chapter.
- Chapter 4 presents FRT capability enhancement of VSC-HVDC systems in grids connected mode and fixed speed wind farm integrated mode with proposed bridge type fault current limiter. Different faults are applied in the systems in order to show the improvement in FRT capability with proposed control techniques.
- Chapter 5 presents the doubly fed induction generator (DFIG) based variable speed wind power integration of VSC-HVDC system. Dynamic model for DFIG is provided. Maximum power point tracking is developed to harness power from variable speed wind turbine. Constant capacitor voltage is maintained by the stator VSC (SVSC) controller while current extraction or injection is achieved by rotor VSC (RVSC) controller. BFCL controller is developed to insert an impedance during the inception of system disturbances in order to limit the fault current and augment FRT capability. RTDS implementation results are provided and discussed at the end of this chapter.
- Chapter 6 deals with an efficient non-linear control based variable resistive bridge type fault current limiter in order to enhance FRT capability and dynamic stability

of VSC-HVDC systems. Fault detection technique and fault current limiter control technique are developed. In this chapter, the proposed non-linear control technique is compared with traditional fixed duty control technique by real time digital simulation results.

- Finally, chapter 7 summarizes this dissertation by pointing out the main contributions of this work. Also, future research scopes are provided in this chapter.

CHAPTER 2

LITERATURE REVIEW

This chapter provides a comprehensive literature review in the area of control of classic HVDC, VSC-HVDC, two terminal and multiterminal HVDC, hybrid HVDC, renewable energy resources, and fault current limiters to depict the current status of the technology. Furthermore, the chapter clearly depicts several aspects of fault current limiters in power system and finds several gaps in the current study which are to be filled by this research work.

2.1 Overview

Power systems are becoming more and more complex in nature due to integration of several power electronic devices. Transmission lines are being loaded closer to thermal limit due to increased electric power demand as result of global population growth and industrialization. Several renewable energy such as solar, tidal, wave, biomass, geothermal and wind are being integrated to the existing grid due to perpetual growth in electricity demand. All these factor increases the complexity of the electric networks with inherently high short circuit rate. Protection of such systems and augmentation of reliability as well as stability highly depend on limiting the fault currents. Several fault current limiters (FCLs) have been applied in power systems as they provide rapid and efficient fault current limitation. This chapter presents a comprehensive literature review on different control strategies of for both line commutated converter (LCC) and voltage source converter (VSC) based HVDC systems and application of different types of FCLs

in power systems. Applications of superconducting and non-superconducting FCLs are categorized as: 1) application in generation, transmission, and distribution networks; 2) application in AC/DC systems; 3) application in renewable energy resources integration; 4) application in distributed generation (DG); and 5) application for reliability, stability, and fault ride through (FRT) capability enhancement. Modeling, impact, and control strategies of several FCLs in power systems are presented with practical implementation cases in different countries. Several drawbacks and gaps are identified in the current study of fault current limiters in power system which are filled and improved in this research. Recommendations are provided to improve the performance of the FCLs in power systems with modification of its structures, optimal placement, and proper control design.

2.2 Classic and VSC-HVDC systems

HVDC is traditionally used to transfer large amount of power over long distances. But, reactive power cannot be controlled independently in classic HVDC system [28]. Classic HVDC system is based on thyristor valves [29–31]. In [29], the authors proposed new type of DC reactor using high temperature superconducting (HTS) wire in order to reduce electrical losses in line commutated converter based classic HVDC system. The proposed reactor operated well without any adverse effect on the LCC-HVDC system. Earth return path is necessary in line-commutated converter HVDC circuit. Many of conventional LCC HVDC systems use earth electrode as return path which simply help flowing current into the ground located near or few kilometers away from the valve station. Submarine cable and sea electrode are commonly used in LCC-HVDC system that cross sea or interconnect island regions. Those sea electrodes located on the sea floor have been

facing challenges because of the environmental concerns made by DC current injected into the ocean. Application of different faults on such LCC-HVDC system and their effects are analyzed and counter measures are proposed to protect metallic return [30].

LCC-HVDC is appropriate for high voltage bulk power and long distance transmission projects without the effect of capacitance along the long transmission line [32]. The typical example is the Ultra LCC-HVDC projects commissioned in China having power transmission capacity of about 6000MW from hydro plants to the load area about 2000 km away through two overhead DC transmission lines with ±800 kV DC voltage rating.

Due to independent control of active and reactive power, power reversal without voltage polarity change, less corona loss and better controllability, voltage source converter high voltage DC (VSC-HVDC) has been dominant over classic LCC-HVDC in recent years [3,32,33].

Moreover, VSC-HVDC presents a solution for many problems faced nowadays by power networks, such as, network congestions, grid re-enforcements, renewable energy source integration, multi-terminal DC (MTDC) operation and asynchronous operations of two different grids [3]. Different types of VSC topologies are proposed in literatures [4]-[5] including two level, three level and multilevel for HVDC transmission. Multilevel means more than two voltage levels can be gained in one phase leg, which decreases the switching times of valve and makes the voltage wave form closer to sinusoidal curve. Line to neutral voltage waveforms of both two-level and three-level converters with pulse width modulation (PWM) are discussed and compared [5]. Table **2**:**1** shows the comparison between classic and VSC-HVDC.

Table 2:1 Comparison of Classic HVDC and VSC-HVDC

Function	Classic HVDC	VSC- HVDC
Converter valves	Thyristor	IGBT
Connection valve - AC grid	Converter transformer	Series reactor (+ transformer)
Filtering and reactive compensation	50% in filters and shunt capacitors	Only small filter
DC current smoothing	Smoothing reactor and DC filter	DC capacitor
Telecom between converter station controls	Needed	Not needed

2.3 Two terminal and Multiterminal HVDC

Two terminal VSC-HVDC consists of a rectifier and an inverter whereas multi-terminal VSC-HVDC consists of several rectifiers and inverters [34]-[35] forming DC grid. In two terminal topology, sending end and receiving end of VSC-HVDC have the similar configuration where sending end converter acts as rectifier and receiving end acts as inverter. Phase reactors connected between grid and converter control current through it and hence active and reactive power flow. AC filters block harmonic components to enter in AC grid. Converters are usually connected to AC grid through transformer. DC side capacitor helps controlling DC link voltage.

Vector current control is the most popular control method used for VSC-based HVDC [36], [37],[38]. The basic principle of the vector current controlled VSC is to control

instantaneous active and reactive grid currents independent of each other [39]. Vector control consists of a fast inner current control loop controlling the AC current and the outer control loop [40]. Outer controllers supply the AC current references for the inner current controller. Several outer controllers are included in HVDC control system depending upon the applications.

In multi-terminal HVDC system, more than two converters are connected together to form high voltage DC grid. Hierarchical power control of multi-terminal high voltage direct current (MT-HVDC) has been proposed in [41]. The proposed controller has primary, secondary and tertiary controls as classical AC transmission system. The proposed methodology provides separation among different control actions like classical AC power system. Primary, secondary and tertiary control actions involve voltage stability, power set points after contingency and power scheduling respectively. Power reference change and converter disconnection have been simulated to validate proposed controller.

A new control strategy is proposed for voltage source converter (VSC) in MTDC system [42] for the connection of offshore windfarms to the grid incorporating voltage-current characteristics of VSC and power reduction of windfarms during fault. The proposed control technique does not require fast communication between wind farms and VSC. In normal operation condition, grid side converters take over DC voltage control and coordinate power sharing to the terrestrial grid. In fault condition, windfarm side converters control DC voltage and coordinate power reduction between windfarms.

Fault location in DC line of MTDC may not be determined accurately due to the fact that fault current flows through the whole line. A novel fault location and protection technique on DC line is proposed in [43] by analyzing characteristics harmonics of DC filter. Complex wavelet transform is used for determining fault location criterion from the differences of harmonics at the characteristic frequency and at the other frequency.

Voltage current-characteristic of each converter and equilibrium point of MTDC system are analyzed in [44]. Either voltage droop mode or maximum AC current mode is used for grid connected inverter whereas wind firm rectifiers can operate in constant AC voltage mode, maximum DC current mode, and voltage droop mode. HVDC grid conductance matrix and converter equations are used to find out equilibrium points for several cases like converter loss, voltage sag in AC grid, and different wind power conditions.

Majority of the literatures presented MTDC system with one slack bus whose function is to control DC voltage and set of others DC busses performing power regulation to the AC grid. However, this system will ensure stable operation until the slack bus converter power rating is greater than the power required to keep DC network voltage within the limit. If not, transient in the system will put huge stress on the slack bus. To solve this problem distributed DC voltage control method has been proposed [45] considering a slack bus that controls DC voltage and droop control on other DC busses.

2.4 Hybrid HVDC

Bridge type fault current limiter (BFCL) and parallel-resonance bridge type fault current limiter (PRBFCL) have been applied to a hybrid power system consisting of a photovoltaic (PV) power generation source, a doubly-fed induction generator (DFIG)-

based wind energy system, and a synchronous generator (SG) to augment the transient stability and PRBFCL has been shown superior to BFCL [46]. Rotating machines such as synchronous generator (SG), doubly fed induction generator (DFIG) in hybrid system can be stabilized with the proposed protection scheme.

A hybrid power system consisting LLC-HVDC and static VAR compensator (SVC) is proposed to connect grids having no synchronous generator in literature [47]. Combination of robust performance, low capital cost and power loss of a LCC converter, with the fast dynamic performance of a VSC converter is observed in the proposed system. Different operating scenarios like black-start, variations of load or generation, and AC fault conditions are simulated for validating proposed controller of such hybrid HVDC system.

Operation with weak AC system, no reactive power demand, excellent control performances are the advantages of VSC-HVDC system; however, due to inherent defect in fault ride through (FRT) for DC fault, this is not still optimal choice. A line commutated converter (LCC) and modular multilevel converter (MMC) hybrid HVDC topology with high power diode installed in the overhead line is proposed [48] with DC fault clearance capability. Bulk power transmission, improved AC FRT capability are the main advantages of the proposed technique. Besides, low cost and operational losses are observed in the proposed technique for DC fault clearing capability compared to other techniques proposed in [49], [50]; however, power flow is not bidirectional in this technique.

One of the major applications of VSC-HVDC system is integration of renewable energy especially wind energy. Over a wide range of wind speed, variable-speed wind turbines (WTs) offer increased efficiency in harvesting the energy from wind with better power quality [51], [52]. Nowadays, the best option for integrating variable speed wind turbine is doubly fed induction generator (DFIG) [53]. DFIG based wind power integration offers lower converter cost as well as lower power loss with better power quality compared to fully fed synchronous generator with full rated speed [54], [55]. In [56], the authors proposed a new control strategy for low voltage ride through capability enhancement of DFIG based wind energy system under unbalanced voltage dips. A combined control of rotor-side converter and three-phase stator damping resistor (SDR) placed in series with the stator windings is used to achieve low voltage ride through capability improvement of DFIG. SDRs are activated only for those phases experiencing low voltage whereas rotor current controller is controlled in such a way that stator winding does not experience low voltage.

Detailed dynamic model and improved control strategies of a grid-connected DFIG with series grid side converter (SGSC) is presented in [57] under unbalance network conditions and harmonic voltage distortions. The parallel grid side converter (PGSC) is controlled in a way that eliminates pulsations and keeps total current symmetrical and undistorted. In addition, PGSC provides transient maximum average reactive power to support the power grid during transient fault conditions.

2.5 Fault Current Limiters in Power Systems

Fault current limiters have been extensively applied in power systems for improving stability and dynamic performance of the systems by limiting fault current. Following

subsections summarizes different aspects of both superconducting and non-superconducting types fault current limiters.

2.5.1 Superconducting and Non-superconducting FCLS in power system

Fault current limiters (FCLs) are considered as main candidates to be inserted into the electrical grids in order to prevent the short-circuit damages and inevitable upgrading of the system equipment. Mainly, two types of fault current limiters (FCLs) are extensively applied in power systems: non-superconducting [15,24,58–62] and superconducting [63–68]. The tree diagram shown in Figure **2.1** summarizes the applications of superconducting and non-superconducting FCLs in power systems.

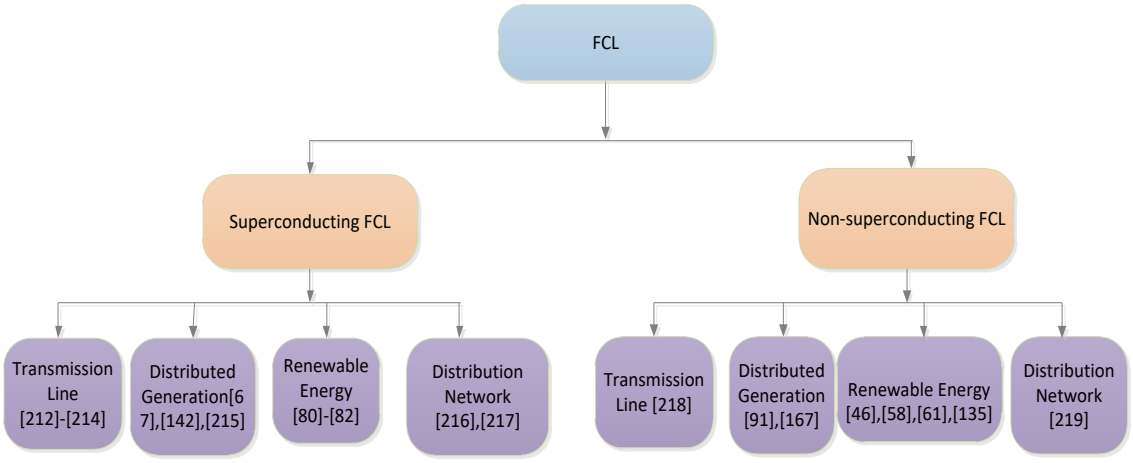

Figure 2.1 Superconducting and Non-superconducting FCLs in Different Applications of Power System

Both superconducting FCL and non-superconducting FCL have been extensively applied in transmission and distribution networks and renewable energy systems for different purposes such as stability enhancement, protection improvement, fault current reduction, and fault ride through (FRT) capability enhancement. Main advantages and disadvantages of superconducting and non-superconducting FCLs are summarized in the following table.

Table 2:2 Comparisons of Superconducting and Non-superconducting FCLs

Items	**Superconducting FCL**	**Non-Superconducting FCL**	**References**
Size and weight	Big size and heavy weight.	Small in size and less weight.	[69,70]
Cost	As the required inductor and resistor are superconducting nature, it has high implantation cost.	Less cost due to non-superconducting nature of required inductor and resistor.	[8,14,71,72]
Loss	It has loss in normal operating condition.	It has negligible loss in normal operation of the system.	[73–75]
Implementation status	Practically implemented in power system in many countries.	Not yet implemented. Detailed feasibility analysis is needed to be done for practical implementation.	[76–79]
Interference with neighboring communication line	It has interference with communication line.	No interference with communication line.	[79],[80], [81]
Fault detection and control systems	Most of them does not require additional fault detection and control system.	Most of the non-superconducting FCL needs additional fault detection and control circuit.	[79–82]
Topology complexity	Most of them has highly complex circuit topology.	Structure is very simple for most of them.	[83–91]

2.5.2 Superconducting FCLs

Depending on the structure and operating principle, superconducting fault current limiters (SFCLs) can be categorized into different types: Non-inductive reactor, inductive, transformer, resistive, hybrid, flux-lock, and magnetic-shield.

i) Non-inductive type SFCL

A schematic diagram of non-inductive type SFCL is shown in Figure **2.2** which is made of two superconducting coils [92].

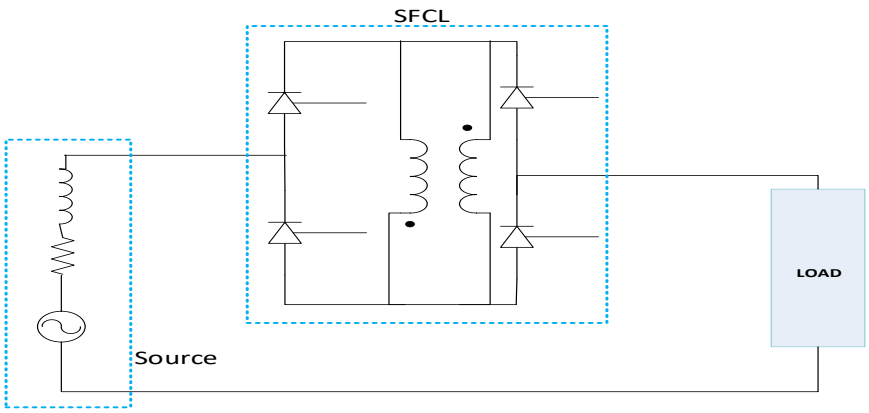

Figure 2.2 Basic Circuit Diagram of Non-inductive SFCL with Single Phase Circuit.

A current limiting coil and a trigger coil are connected in anti-parallel and are magnetically coupled well. Different types of configurations like coaxial coil arrangement and bifilar winding arrangement were compared. Bifilar winding arrangement was superior to have high impedance ratio [92].

ii) Inductive type SFCL

Inductive type SFCL has two coaxial windings and an optional magnetic core [93]. Primary winding is made up of copper (Cu) whereas secondary winding is made up of a high temperature superconductor (HTS). The SFCL is cooled in the liquid nitrogen bath. Electrical connection diagram of inductive SFCL is shown in Figure **2.3**.

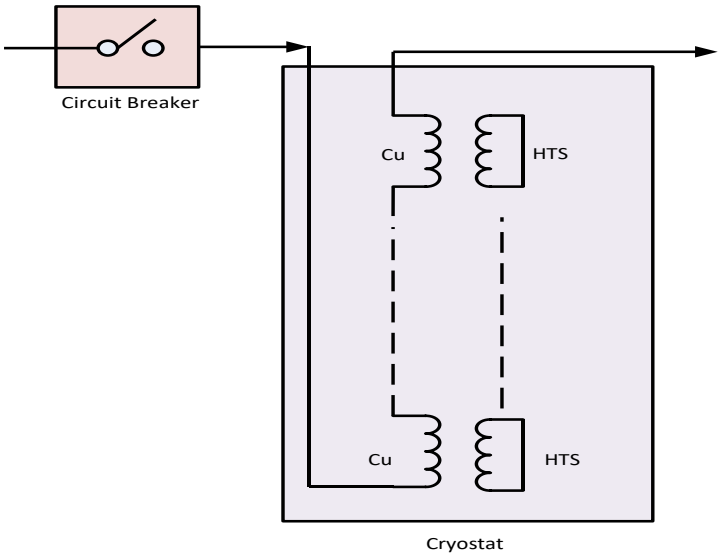

Figure 2.3 3. 15 kV Class Inductive SFCL

During steady state mode of the power system, zero impedance is shown by inductive SFCL as the zero impedance of the secondary superconducting winding is reflected to the primary. However, during system contingencies, resistance in the secondary is reflected into the primary circuits to limit the fault currents.

iii) Transformer type SFCL

Enhancement of supply reliability and power system stability have been observed with transformer type SFCL [83,94–100]. Primary side of the transformer type SFCL is connected in series with the load whereas secondary side is connected in series with superconductors. Transformer type fault current limiter with vacuum interrupter is shown in the Figure **2.4**. In Figure **2.4**, L_1 and L_2 are the inductance in primary and secondary respectively. M is the mutual inductance between primary and secondary coil of the transformer.

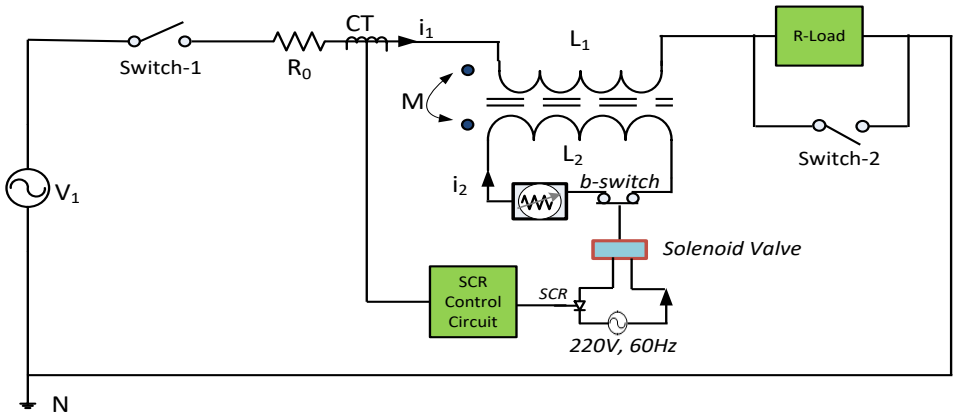

Figure 2.4 Transformer Type SFCL with Load in Single Phase Circuit [83].

Upon the occurrence of the faults, superconductors in the secondary side of the transformer is quenched, consequently, fault current in secondary is limited to lower value. Due to the current limiting in the secondary, fault current in the primary side is limited as well.

iv) Resistive type SFCL

Resistive type SFCL can improve the transient stability of the power system by suppressing the level of fault currents in a quick and efficient manner [101–112]. A very simple structure of resistive SFCL is shown in Figure **2.5** consisting n^{th} units of stabilizing and superconducting resistances in parallel [109]. Coil inductance with n^{th} units is connected in series with the parallel resistive branch.

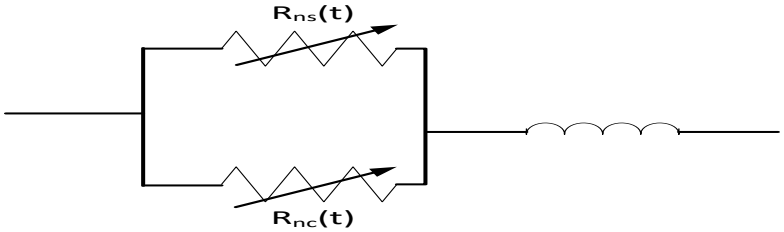

Figure 2.5 A Simple Structure of Resistive SFCL

In normal steady state condition, the values of stabilizing (R_{ns}) and superconducting (R_{nc}) resistances are zero. However, during fault conditions, these resistances become nonzero time-varying parameters to maintain superconducting states according to their unique characteristics. The value of the coil inductance is kept as small as possible in order to have minimal AC loss during normal operation. Therefore, the effect of the inductor during steady state operation is ignored.

Long length of superconductor is needed to make a high voltage and high current system in case of resistive and inductive type SFCL. However, this required length is significantly reduced in hybrid SFCL which makes it commercially applicable [113].

v) Hybrid SFCL

Due to the slight critical current differences between the several units, resistive SFCL faces difficulty in quenching simultaneously between the units; however, this problem can be solved with hybrid SFCL [114]. Hybrid SFCL is proposed for limiting fault current and improving dynamic performance of power system [113–116]. A hybrid type SFCL has a primary winding and several secondary windings as shown in Figure **2.6** [114]. Each of the secondary windings is connected in series with superconducting resistive unit. In Figure **2.6** , L_P is inductance in the primary winding of the transformer, and L_{SA}, L_{SB}, L_{SC} and I_{SA}, I_{SB}, I_{SB} are the inductances and currents of secondary winding *A*, *B*, and *C* respectively.

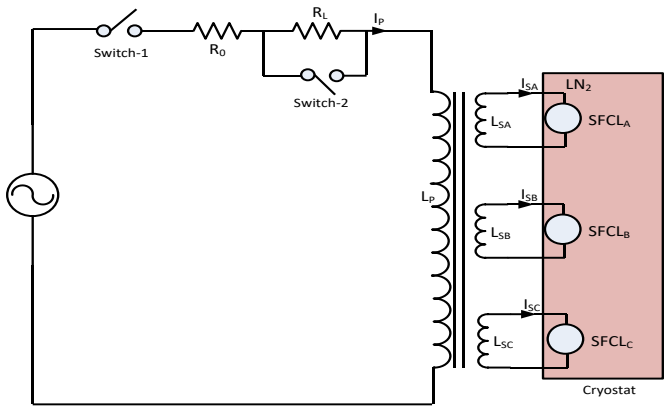

Figure 2.6 Structure of Hybrid SFCL [114]

During normal operation, resistance of the superconducting units connected in series with the secondary windings is zero. Therefore, current (I_P) flows through the power system without any loss. When fault appears on the system, superconducting unit is quenched and fault current is limited. In this way, hybrid SFCL has almost no effect on the system performance during normal operation and limits fault current during contingencies.

vi) Flux-lock type SFCL

Among the several SFCLs, the flux-lock type SFCL has less power burden of the high temperature superconducting (HTSC) element [84]. Short circuit current in power system can be limited with flux-lock type fault current limiter during different contingencies [13,14,69,84,117–120]. Configuration of flux-lock type SFCL with over current relay is shown in the Figure **2.7** where N_1, N_2, N_3 and i_1, i_2, i_3 represent coil-1, coil-2, and coil-3 with their currents, respectively. *ORC* stands for over current relay.

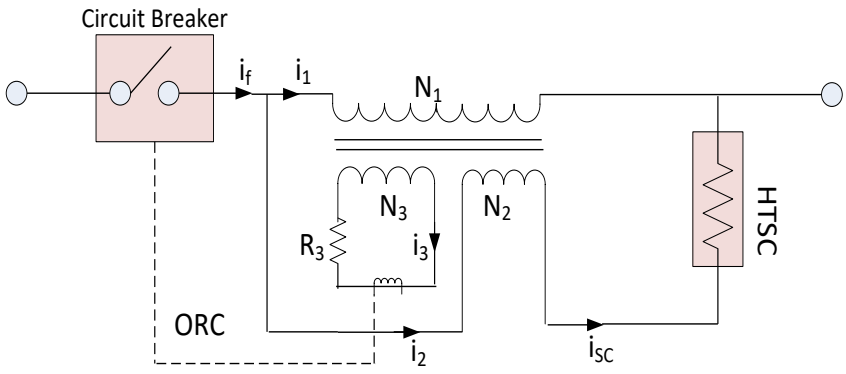

Figure 2.7 Configuration of the Flux-lock Type SFCL

As shown in Figure **2.7**, flux-lock type SFCL has mainly two parts: current limiting part and current interrupting part. The current limiting part consists of two parallel-connected coils and a high temperature superconducting (HTSC) connected in series with one of the coils. The current interrupting part consists of an over current relay driven by one of the parallel coils and a circuit breaker. During normal operation, zero voltage is induced across the coil as the magnetic fluxes generated in two coils are cancelled out. In faulty conditions, fault current is limited by the voltage generations across the coils.

vii) Magnetic Shield SFCL

Magnetic shield type SFCLs have been reported in [121–128]. It consists of a primary copper coil and secondary high temperature superconductor (HTS) tube wound around a magnetic iron core [127] as shown in Figure **2.8**. In magnetic shield SFCL, screen currents thwart flux penetration into the iron core during standard operation as HTS tube is fixed between primary copper winding and magnetic core.

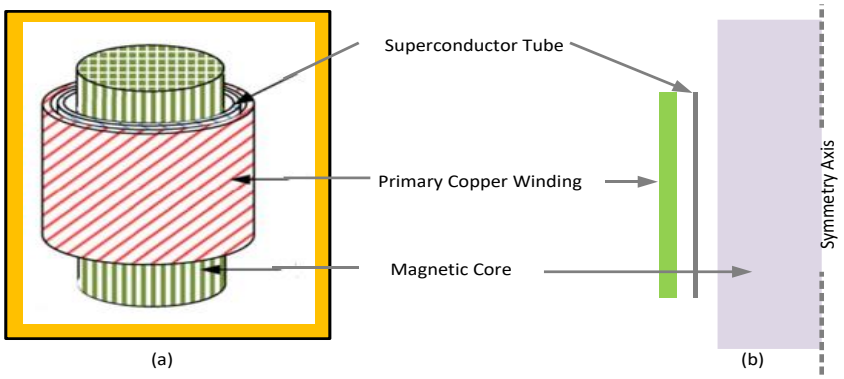

Figure 2.8 Magnetic Shield SFCL a) Full structural view b) Cross sectional view [127]

During fault conditions, superconducting to normal transition value is increased as the current exceeds critical value of HTS elements. Therefore, the resistance of the HTS tube is replicated in the primary circuit and magnetic flux infiltrates into the iron core augmenting impedance of the limiter.

Table **2:3** summarizes superconducting FCLs in terms of cost, advantages, limitation and applications etc.

Table 2:3 Comparisons of Different SFCLs in Terms Application, Cost, Pros and Cons

SFCL Types	**Advantages**	**Disadvantages**	**References**
Non-inductive	❖ Low cost ❖ Less recovery time ❖ Less AC losses ❖ It can withstand high voltage	❖ Volume of cryogenic is higher ❖ Higher leakage inductance and circulating current	[92,129,130]
Inductive	❖ Weight and device size can be significantly reduced due to coreless construction	❖ Loss in stand-by mode due to leakage reactance ❖ Conventional circuit breaker must needed in order to switch off short circuit to avoid maximum HTS winding temperature.	[73–75]
Transformer	❖ It can regulate fault current limiting range according to impedance ratio of transformer and hence applicable in the cases of wide range of current limiting ❖ Shortest recovery time could be achieved with neutral lines	❖ Current limiting time is higher ❖ Power burden of SFCL is higher	[97]

Resistive	❖ Automatic recovering and faster excessive current limiting capability ❖ Smaller in size, less costly and very simple structure	❖ Long length of superconductor is required for high voltage application ❖ Large dissipated power and long recovery time ❖ Shortest recovery time could not be achieved even with neutral lines ❖ Simultaneous quenching is not possible due to critical current difference between several units	[23,101–113]
Hybrid	❖ Simultaneous quenching is possible which is not possible in resistive SFCL ❖ Less superconductor is required for high voltage and current applications	❖ Replenishment of liquid nitrogen is needed if outage period is relatively long.	[113–116,131]
Flux-lock	❖ Operational current could be varied ❖ Less power burden on superconducting modules	❖ Big size, heavy weight and high cost.	[13,14,69,132]
Magnetic Shield	❖ Magnetic shielding body is automatically heated when fault occurs and hence does not require additional fault detection circuit ❖ It has greater design flexibility due to turn ratio ❖ It provides isolation between SFCL and power network	❖ It experiences undesirable voltage drop during normal operation ❖ It has magnetic field interference which affects the operation of nearby sensitive devices	[125,127,133,134]

2.5.3 Non-superconducting FCLs

Generally, superconducting fault current limiters have been extensively used in power system. However, non-superconducting fault current limiters could play an important role in reducing fault current and improving dynamic stability of power system with minimal cost compared to superconducting fault current limiters [23,46,58,135]. There are several types of non-superconducting fault current limiters as follows.

i) Series dynamic braking resistor (SDBR)

SDBR is non-superconducting FCL which has been extensively used in power system especially for fault ride through (FRT) capability enhancement of wind farm [85–90]. SDBR consists a resistor in parallel with a switch. The switch is turned on and off based on the occurrence of fault in the system. Due to fast response, IGBT is used as a switch as shown in Figure **2.9**.

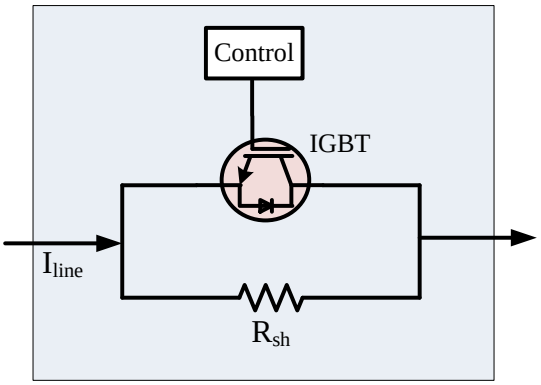

Figure 2.9 SDBR Configuration

During normal operation, IGBT is turned on and the braking resistor is bypassed. Therefore, the SDBR has no effect on the system during normal condition of the grid. At the inception of grid fault, voltage at point of common coupling (V_{pcc}) decreases and becomes lower than the predefined reference voltage (V_{ref}). IGBT is turned off at this condition and braking resistor comes in series with the line to limit the sharp increase in line current. Braking resistor continues to be in series with the line until V_{pcc} becomes greater than V_{ref}. When V_{pcc} surpasses V_{ref}, IGBT is turned on and system returns to its normal operation.

ii) Bridge type fault current limiter (BFCL)

BFCL has two main parts: bridge part and shunt branch [136,137] as shown in Figure **2.10**.

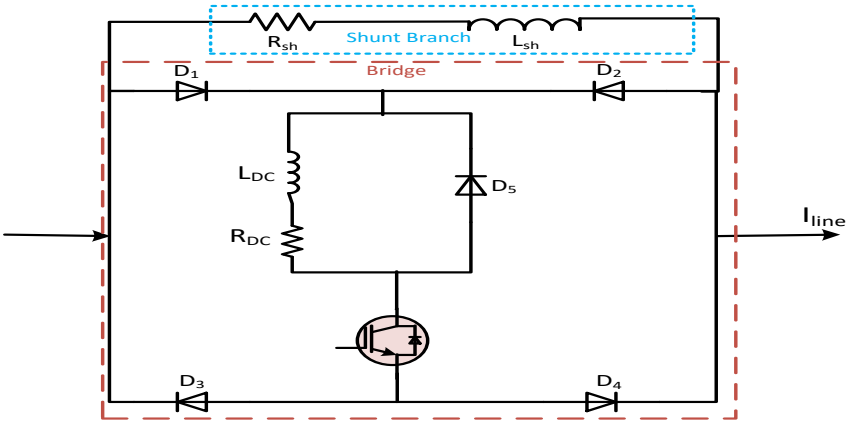

Figure 2.10 Bridge Type Fault Current Limiter

The main function of BFCL is to insert resistance and induction at the inception of fault. It does not require superconductive characteristic for its operation thus it has less application cost compared to other fault current limiting devices. The bridge part is composed of diode rectifier, a very small DC limiting reactor (L_{DC}), a small DC resistance (R_{DC}), commercially available semiconductor (IGBT) switch (CM200HG-130H) and a freewheeling diode. The main shunt branch is connected in parallel with the bridge part. It consists of a series connected resistance and reactance ($R_{sh}+j\omega L_{sh}$).

During normal operation, IGBT switch is turned on and current flows through the path D_1- L_{DC}- R_{DC}-D_4 for positive half cycle of the signal. Then, current conducts through the path D_2- L_{DC}- R_{DC} -D_3 for negative half cycle of the signal. As the current through the L_{DC} has unified direction during this normal operating condition L_{DC} is charged to the peak of the line current and essentially behaves like short circuit and it has negligible voltage drop. Consequently, BFCL has no impact on the system at normal operating condition. During contingencies, IGBT switch is turned off and essentially bridge behaves like open circuit. So, the shunt path of the BFCL comes into operation and limits the fault current.

At the same time, freewheeling diode provide discharge path for reactor (L_{DC}). It is worth mentioning that during fault initiation L_{DC} line current tends to increase drastically; however, L_{DC} limits this current. Therefore, IGBT switch is saved from high *di/dt*.

iii) Modified bridge type fault current limiter (MBFCL)

The structure of the bridge of the fault current limiter is rearranged to enhance low voltage ride through capability of fixed speed and variable speed wind farms [138,139]. This new topology is named as modified bridge type fault current limiter (MBFCL). In BFCL shunt path consists series connected resistor and inductor. However, inductor is omitted in MBFCL because it discharges when the shunt path is disconnected. During normal operation, MBFCL bridge is short-circuited as IGBT gate signal is high, thus shunt branch resistance is bypassed. When fault appears on the system, IGBT gate signal becomes low by proper control action, the bridge part of the MBFCL is eventually open and shunt resistance is inserted in the line to limit the fault current.

iv) DC link fault current limiter (DLFCL):

DC link fault current limiter is proposed for FRT capability enhancement of inverter based distributed generation system [91]. The non-superconducting DLFCL module is composed of a diode bridge and inductive coil having inductor L_d and very small resistance R_d as shown in Figure **2.11**.

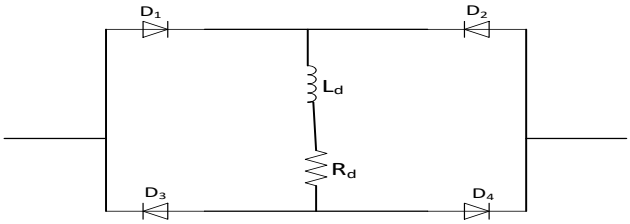

Figure 2.11 DC Link Fault Current Limiter

In normal operation, DC reactor has negligible impact. However, the reactor can effectively suppress severe *di/dt* and it can limit fault current successfully over the fault duration.

v) Transformer coupled BFCL:

Transformer coupled bridge type fault current limiter is presented [140] for low voltage ride through (LVRT) capability enhancement of doubly fed induction generator (DFIG). The schematic diagram of the fault current limiter is shown in Figure **2.12**. Bypass resistor (R_b) is used to absorb majority of the current harmonics during normal operation and reduce voltage spikes.

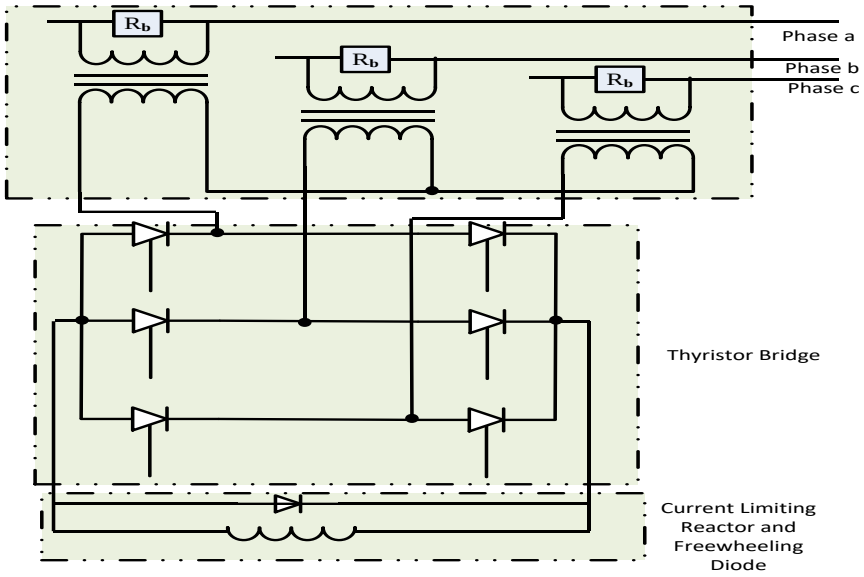

Figure 2.12 Transformer Coupled BFCL

In steady state system, all the thyristors are kept turned on and limiting reactors are bypassed. During system disturbances, gate signals of the thyristors are removed and limiting reactor is inserted to limit fault current.

Table **2**:**4** summarizes different types of non-superconducting fault current limiters.

Table 2:4 Non-superconducting Fault Current Limiter Summary.

FCL Type	FCL position	Required number of units	Transformer	Semiconductor devices	Controller circuit
SDBR	AC side	3 units	Not needed	IGBT	Needed
BFCL	AC side	3 units	Not needed	IGBT plus diodes	Needed
MBFCL	AC side	3 units	Not needed	IGBT plus diodes	Needed
DLFCL	DC side	1 unit	Not needed	Only diodes	Not Needed
Transformer coupled BFCL	AC side	3 units	Needed	Thyristors and diode	Needed

2.5.4 Optimal parameters and Placement of Fault Current Limiters

Optimal location of FCLs in power network has several potential benefits. These include enhancing the system reliability and security, reducing fault current and voltage sag, improving fault ride through (FRT) capability, and increasing the interconnection of renewable energy. Several optimal placement techniques have been reported in the literature [63,67,141–149]. Number of FCLs units, optimal parameters, and optimal positions are considered for the placement of the FCLs in power system with several objectives like fault current reduction, reliability and stability improvement, FCL cost reduction, and optimization of operating time of the over current relays. Some of the works focused on optimal placement mainly with single objective function as either fault current reduction [150,151] or stability enhancement [149]. Since there is the tradeoff among several objectives, enhancing one of them might lead to the deterioration of the

others. Multiobjective optimization techniques [67,142,143,152] have been reported to solve above mentioned problem. However, most of the optimal placement techniques do not take into account uncertainties in power systems, especially the unpredictable variations in the status of a DG, wind, and PV systems when determining the best location for SFCL [63]. New placement algorithms can be developed considering several networks uncertainties for better performance. Table **2:5** summarizes optimal placement parameter selection techniques for different superconducting FCLs.

Table 2:5 Optimization Techniques for the Placement of Superconducting FCLs

Objective Function	**Used Method/Algorithm**	**FCL Types**	**Considered Network**	**Features**	**References**
Minimization of main-backup overcurrent relay (OCR)-pairs coordination maintenance index and the total cost of required FCLs.	Multi objective Particle Swarm Optimization (MOPSO)	Impedance SFCL	IEEE 30-bus meshed system and IEEE 33-bus radial system	❖ Location and size can be obtained without any pre-assumptions. ❖ Applicable for both radial and meshed network	[142]
Minimization of number of SFCLs, fault current, and optimal relay operating time	scenario optimization	Hybrid resistive SFCL	17-bus power system with DGs	❖ Optimal placement of SFCLs keeps the fault current within breaking capacity of the protective devices ❖ No change in the coordination of relays are need while installing new DGs in the system	[67]
Maximizing reliability, Minimizing fault current and FCLs cost	Pareto algorithms	Impedance SFCL	IEEE 39-bus and 57 bus systems	❖ Penalty factor is introduced in the optimization problem to keep fault current within maximum allowable range	[152]

Minimization of total installed cost, including a fixed cost of installation and incremental cost of impedance	Iterative mixed integer nonlinear Programming	Impedance SFCL	The IEEE 9-bus, IEEE 30-bus, and a real North American 395-bus transmission system	❖ FCLs installing cost is minimized while reducing the fault current ❖ Location sensitivity indexed in not required for the proposed method ❖ Method is restricted by pre-determined locations and random searching techniques ❖ Method is Straightforward and can be applied for any mesh network	[143]
Minimization of angular deviations between the rotors of the synchronous machines	Transient stability index method	Resistive SFCL	IEEE benchmarked four-machine two-area test system	❖ The optimal location of SFCL determined by the method is capable of limiting fault current for the three phase fault at any location in the network	[149]
Minimization of power loss	Sensitivity index method	Resistive SFCL	IEEE benchmarked four-machine two-area test system	❖ Improve system damping more effectively ❖ Short circuit current is significantly reduced even if fault occurs at a point far from the optimal location of SFCL ❖ Drawback of the method is it does not consider protection co-ordination problem	[147]
Minimization of FCLs unit and parameters	Genetic algorithm	Impedance SFCL	Six-bus test system and IEEE 30-bus system	❖ Fault current is kept within CB interrupting ratings with minimum FCLs units and parameters ❖ Sensitivity factor is introduced in the proposed method to reduce search space	[146]

Some of the non-superconducting FCLs parameters design techniques have been presented in the literatures [20,139] . However, to the best of authors' knowledge, no

optimization technique has been applied for either optimal parameter selection or optimal placement of non-superconducting FCLs.

2.5.5 Real Grid Operations and Field Tests of FCLs

Although short circuit tests can be conducted to demonstrate current limiting capability of any developed SFCL, a field test is necessary to validate the performance and reliability. SFCL practical installing issues and field tests have been reported [16,66,76–78,153–157]. In many countries FCLs have been practically installed and field tests have been done with results and recommendations for further study. Table **2**:**6** below shows field test results from different countries.

Table 2:6 Summary of Field Tests of Superconducting FCLs

Country	FCL Type	FCL rating	Test Names	Test results	References
China	Saturated iron-core superconducting fault current limiter (SI-SFCL)	220 kV/300 MVA	✓ Lightning impulse and AC voltage withstanding tests ✓ Lightning partial discharge tests ✓ Partial temperature rise tests ✓ DC resistances and insulation resistances of the coils ✓ The AC coil impedance test	AC coil deformation, oil tank pressure, insulation resistance of AC/DC coil, AC voltage withstanding capability were as expected in the test result.	[76]
Korea	Hybrid superconducting fault current limiter (SFCL)	25.8 kV/630 A and 22.9 kV/630 A	✓ Long term operational test ✓ Fault tests (short circuit) ✓ Minimum limiting current test ✓ Temperature test ✓ Dielectric test	Cryostat suspension has been experienced during test for several times due to blackouts and false alarms. Most of the problem were solved during tests. Temperatures, liquid nitrogen level, and internal pressure remained within ±0.1K, ±0.5 cm, and ±0.3 bar range respectively under	[77],[78]

				all load conditions, Proving stability in cooling superconducting elements Finally, it has been stated that SFCL is capable of functioning reliably under repeated faults.	
Italy	Resistive-type SFCL	9kV/ 3.4 MVA	✓ Critical current test ✓ Partial discharge test, short-duration power-frequency withstand voltage test ✓ Basic impulse insulation level test ✓ short circuit current test	SFCL behavior for 24 hours test duration in grid shows promising results	[155,157]

Long term operational tests have been performed in majority of the field tests to guarantee the reliability and performance of the SFCL devices. For example, the device temperature test to check whether it is within or above the tolerance value [77]. Determination of operational cost by measuring power consumption is one of the main requirements during long term operation tests of SFCL. However, only operational cost of hybrid SFCL [77,158] has been determined and compared with circuit breaker replacement cost and other damages to the power system equipment due to high fault currents. More discussion and feasibility analysis of other types of SFCLs are required with rigorous filed tests. Furthermore, non-superconducting solid state FCLs grid operation and field tests with feasibility analysis should be done in future work before real time grid integration.

2.5.6 FCLs in Stability and Fault Ride Through Capability Enhancement

Due to the increased electrical power demand the fault levels in power systems increase causing severe damage to power system equipment. One of the main ways of enhancing power system stability and reliability is to interconnect the power systems for exchanging power among each other. However, when fault occurs in the system, fault current is contributed to the fault point from all the interconnected parts which restrict interconnection to a certain extent so that the fault current could be kept within the breaking capability of the circuit breakers. Another feasible way is to employ fault current limiters in order to enhance reliability and stability of the interconnected power systems [21,46,68,85,135,139,159–175] . Stability enhancement of microgrid, smart grid, multimachine system, PV system, HVDC, and wind system has been observed with different fault current limiters like SFCL, BFCL, DC link FCL, super capacitor switch FCL and standard iron core FCL as shown in Figure **2.13**. As clearly visualized in the Figure **2.13**, the superconducting FCLs have been examined with many branches of power system. However, non-superconducting FCL have been applied in few branches of power system.

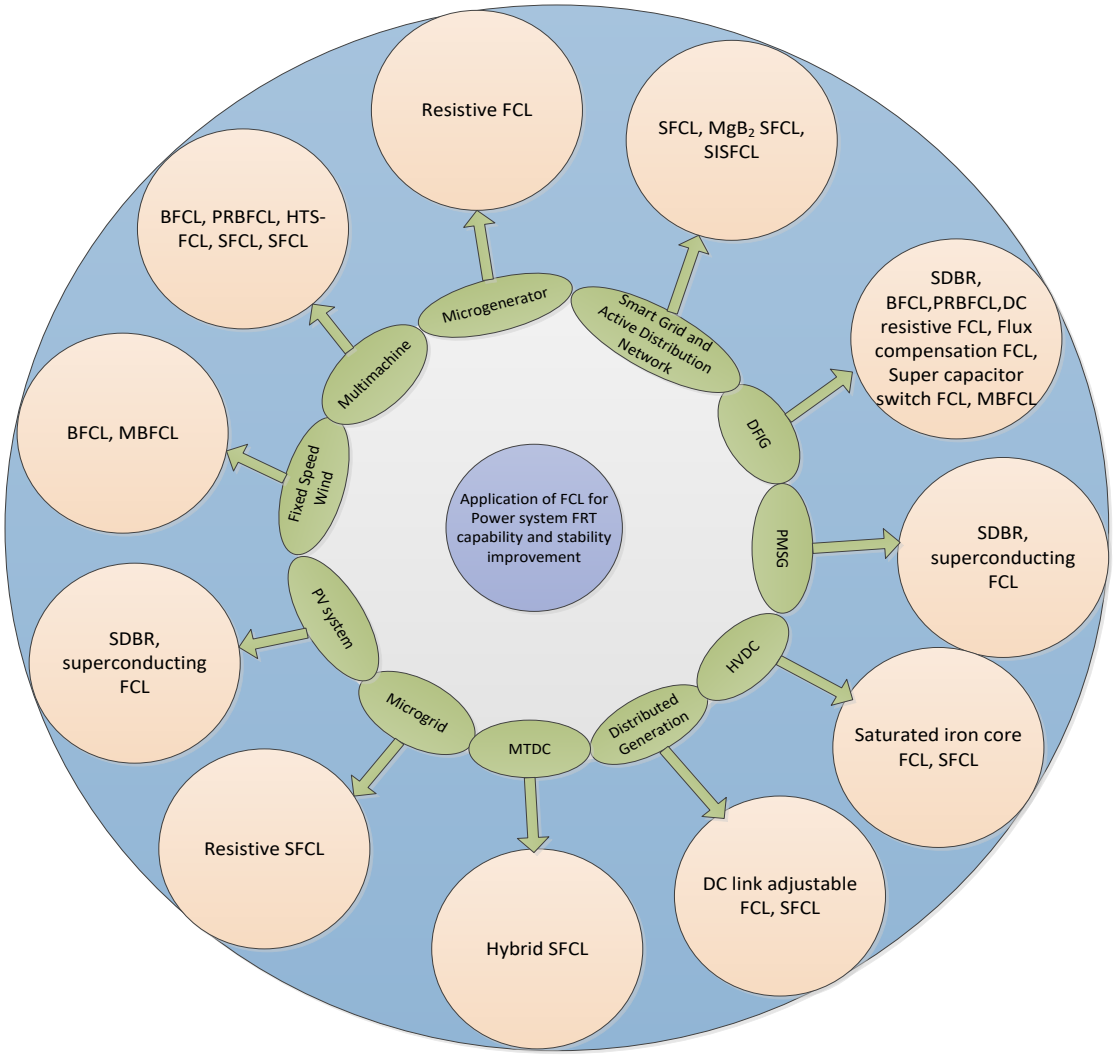

Figure 2.13 Stability Enhancement with Fault Current Limiters

Different types of non-superconducting FCLs like bridge type fault current limiter (BFCL), parallel resonance bridge type fault current limiter (PRBFCL) have been examined in DFIG based wind integration, multimachine system, and fixed speed wind system. Application of these non-superconducting FCL could be investigated in HVDC, smart grid, microgrid, and multi-terminal HVDC (MTDC). Till date, some of the SFCLs have been practically implemented in some power systems in the world. However, non-superconducting fault current are yet to be implemented in real power system. Diodes and IGBT switches are mainly required for non-superconducting FCLs which can be

implemented easily [139]. Moreover, required inductor and resistor for current limiting part are non-superconducting in nature which will reduce implementation cost excessively compared to superconducting fault current limiter for future in power system.

2.5.7 Current Challenges and Future Works

Nowadays, high penetration of distributed generation in the form of PV, wind, and energy storage interfaced with power electronic converters causes several technical issues especially high level of fault current. Moreover, power system are becoming more complex as it is advancing towards smart grid consisting control, computers, automation, and new technology and equipment working together. It is a great challenge for power system researcher to secure stability of such system from high level of fault current. In order to reduce the stress on circuit breaker and other protective devices, fault current limiters are to be installed to keep fault current within permissible limit. However, their application, control, placement, field test, optimal parameter design are important and need further research. Although FCLs have been extensively studied and applied in AC system; their applications are quite limited in systems with HVDC. Multiterminal HVDC (MTDC) is evolving where several converters are connected together to form high voltage DC grid. Such system is more vulnerable to AC/DC faults. Coordination of superconducting and non-superconducting FCLs can be a better solution for MTDC. Still, a lot of challenges are there in developing and testing of non-superconducting FCLs in power system. So, the challenges in application of FCLs are summarized as below from this comprehensive review.

- ✓ Economic analysis of FCLs.
- ✓ Optimal placement and design of FCLs considering network uncertainties.

- ✓ Analysis, application, and feasibility studies of non-superconducting FCLs in HVDC and MTDC systems in order to reduce vulnerability of system with AC/DC faults.
- ✓ Examining application FCLs for DFIG and or PMSG based large scale wind integrated VSC-HVDC system.
- ✓ Comparative studies of superconducting and non-superconducting FCLs in terms of economic aspects and performance analysis.
- ✓ Development of non-superconducting FCLs and conducting their field tests for real grid integration.
- ✓ Coordinated control strategy can be developed between flexible AC transmission systems (FACTS) devices and FCLs.
- ✓ Linearized model can be developed for the system comprising FCLs to conduct small signal stability analysis and design FCLs parameters.

2.6 Conclusions

The aim of this chapter is to offer a detailed and in-depth review of classic LCC-HVDC and VSC-HVDC systems and their existing control strategies with several fault current limiters. Application of FCLs in different branches of power systems like generation, transmission, and distribution networks, AC/DC systems, renewable energy resources integration, distributed generation is reviewed and documented. The key discussion are divided into several parts such as existing control strategies of LCC and VSC based HVDC systems, application of FCLs in several branches of power system, categorizing and discussing structure of several FCLs, pros and cons of different FCLs, real grid operation and testing of FCLs, optimal placement and parameter design, and stability and

fault ride through capability augmentation employing different FCLs. It is realized from the literature review that the FCLs placement is important in limiting fault current and augmenting stability of power system. However, a lot of challenges still are there in applying FCLs in power system such as minimizing interference with neighboring communication line, minimizing loss in normal operation, designing optimal parameters, coordinated control design between FCL and other protective devices, feasibility analysis, field test and real grid operation. Several gaps presented as a current challenges in FCLs applications and controls in power system in this review can be interested topics for the power system researchers.

This review clearly shows that different types of superconducting FCLs have been applied in VSC-HVDC system to limit fault current and enhance fault ride through capability. It is also notable that most of the SFCLs are of high cost. Recently low cost non-superconducting FCLs have been presented in many literature as a potential solution to fault problems of power system, especially bridge type fault current limiter. However, this low cost non-superconducting BFCL has not been investigated yet in VSC-HVDC systems. So, this thesis investigates the control strategy of VSC-HVDC systems with BFCL to enhance FRT capability. The proposed BFCL based control strategy of VSC-HVDC systems shows positive effect in reducing DC link voltage fluctuation, power oscillation, and machine speed deviation by limiting fault current during several disturbances.

CHAPTER 3

MODEL PREDICTIVE CONTROL APPROACH FOR BRIDGE TYPE FAULT CURRENT LIMITER (BFCL)

3.1 Introduction

Currently, transmission lines are being stressed to transfer larger amounts of power due to high electric power demand. Power resources are being limited and increasingly more uncertain and variable. Integration of several renewable energy resources including large scale wind farm to the existing grid is a great challenge for power system researchers. Among the several integration techniques, voltage source converter high voltage DC (VSC-HVDC) system has great flexibility and potential to integrate renewable resources to the existing grid. Due to greater flexibility in control especially independent control of active and reactive power, VSC-HVDC is considered superior over classic line commutated converter HVDC (LCC-HVDC) [1,2,28,176]. Moreover, VSC-HVDC with IGBTs or GTOs could avert commutation failure caused by the grid fault [5].

However, regardless of the numerous advantages, HVDC systems still have flaw in dealing with fault problems compared to AC systems [177]. During disturbances, HVDC systems must be kept energized to avoid bulk power interruption that may cause serious instability. Fault ride through (FRT) capability as well as transient stability improvement have been reported by applying various control techniques of VSCs in [178,179]. Different techniques have been presented in [180] to dissipate DC link power so as to

maintain DC voltage within permissible limit. All techniques presented in the literature except DC chopper resistors protective solution depend on fast communication channel among the converters. It involves different control actions like active power reduction, adjustment of wind turbine power etc. All these control actions are characterized by slow response and large grid power delivery reduction which may lead to system instability. In [181], power oscillations minimization and DC link ripples reduction have been proposed with negative sequence current controller for VSC-HVDC system with two-level converter. However, power from sending end wind power plant is reduced to zero which results in serious stresses in the mechanical system.

Nowadays, model predictive control (MPC) is one of the utmost front-line technologies having ability to include system constraints implicitly. As a result of this advantage, MPC has been extensively used in power systems [182–184]. Power fluctuation reduction and damping improvement of power system having HVDC link have been proposed with generalized predictive control in [185]. In MPC, system model is used for predicting future behavior of the controlled variables. An optimization criterion is used for selecting proper control input [186–188]. First optimum control input is applied as the input to the plant through initialization of a future input trajectory and at each sequential instant optimization problem is solved. Power converters are hybrid nonlinear in nature having linear and nonlinear parts. Turn-on and turn-off commands of such converters are applied with input digital signal which is discrete in nature. Control of such devices requires several restrictions and constraints. Classic control of power converters shows slow response due to dynamics of closed loop whereas MPC shows very fast dynamic response [189,190].

Improvement of stability power system is an important task. This becomes more important when several power electronic devices are integrated with power system. HVDC system is highly non-linear system with power converters. It is required to protect costly converters from high current by employing fault current limiters. This chapter deals with the low cost non-superconducting bridge type fault current limiter in VSC-HVDC system with model predictive control approach.

As the VSC-HVDC system is vulnerable to AC/DC fault and classic control of VSC shows slow dynamic response, so the work proposed in this chapter harnesses the benefits of model predictive control approach with BFCL. The main contributions of the work proposed in this chapter are as follows:

- The proposed MPC-BFCL has been found as very effective solution in limiting fault current of VSC-HVDC system for symmetrical and different unsymmetrical faults.
- Dynamic performance of the system has been improved with the proposed MPC-BFCL.
- MPC-BFCL performance in VSC-HVDC system is compared with its counterpart series dynamic braking resistor (SDBR) where significant improvement is observed.

3.2 BFCL Connection and Operation

BFCL is composed of a bridge with a parallel shunt branch [136,137] as shown in Figure 3.1.

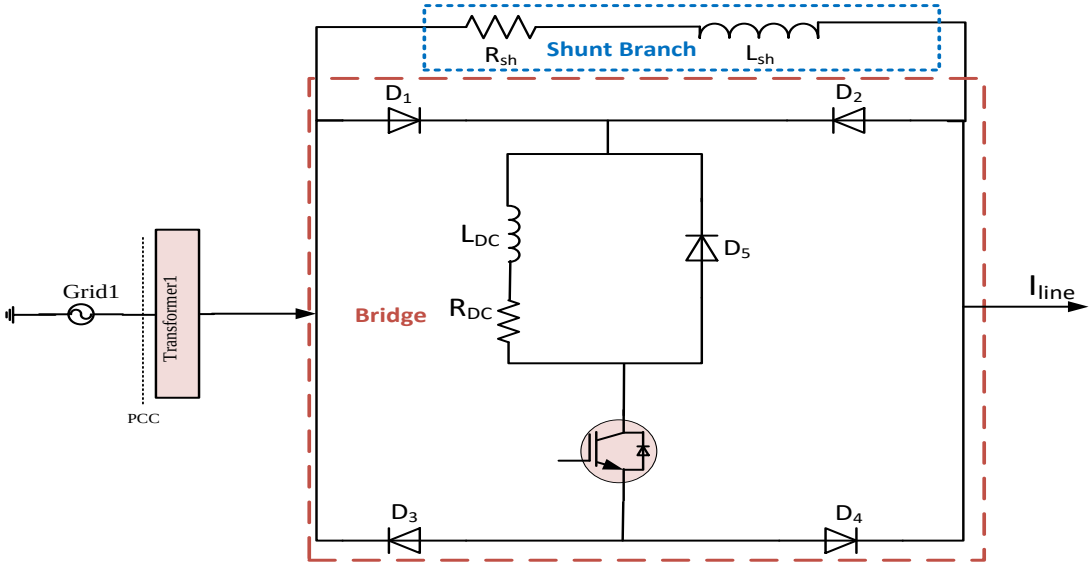

Figure 3.1 Bridge Type Fault Current Limiter Connection with Grid

Bridge part consists a diode rectifier, very small DC resistor and inductor with antiparallel diode, and an IGBT switch. The shunt branch consists of a series resistance and reactance. The main function of BFCL is to insert resistance and reactance by connecting its shunt branch with the line.

During normal operating conditions of the system, IGBT switch is turned on by its controller. So, for positive half cycle, current conducts thorough the path D_1-L_{DC}-R_{DC}-*IGBT*-D_4. During negative half cycle, current passes thorough the path D_2-L_{DC}-R_{DC}-*IGBT*-D_3. Therefore, for both the cycles, current has a unified direction through L_{DC} and R_{DC}. Consequently, L_{DC} is charged to the peak value of the line current and acts like short circuit. Since the values of R_{DC} and L_{DC} are very small, insignificant voltage drops across them. Eventually, the bridge is short circuited during normal system operation and it has no effect on this operating condition. On the other hand, during system disturbances, IGBT switch is turned off by BFCL controller. As a result, the shunt branch is connected to the line by considering the open circuit of the bridge part. Insertion of this resistance

and reactance during system disturbances limits fault current and improves dynamic stability of VSC-HVDC system.

3.3 Design of BFCL Parameters

In this work, BFCL parameters are designed based on the pre-fault power flow through each line. During normal operation, each line of three phase system carries equal amount of power. In order to have least effect of the fault on the system, BFCL should consume equal or higher amount of active power of pre-fault value. Now, the power consumption of BFCL at post-fault is given as below.

$$P_{BFCL} \geq \frac{P_G}{3} \tag{3.1}$$

$$P_{BFCL} = \frac{V_{PCC}^2 R_{sh}}{R_{sh}^2 + X_{sh}^2} \tag{3.2}$$

where P_G, $V_{PCC,}$ $R_{sh,}$ and X_{sh} are power delivered by the grid or wind farm, voltage at point of common coupling (PCC), shunt resistance, and shunt reactance, respectively. The above two equations give the following expression.

$$P_G R_{sh}^2 - 3V_{PCC}^2 R_{sh} + P_G X_{sh}^2 \leq 0 \tag{3.3}$$

From the above equation, we get R_{sh} as follows.

$$R_{sh} \leq \frac{3V_{PCC}^2 \pm \sqrt{9V_{PCC}^4 - 4P_G^2 X_{sh}^2}}{2P_G} \tag{3.4}$$

The necessary condition for the R_{sh} to be the real value is that the term inside root must be greater than zero and which gives following equation.

$$X_{sh} < 1.5\frac{V_{PCC}^2}{P_G} \tag{3.5}$$

The same approach is used to find the value of R_{sh}. For the BFCL to be practical, small values of L_{DC} and R_{DC} are chosen so that the voltage drop across them is negligible and the DC current flowing through them is well smooth.

3.4 BFCL Control Strategy

Disturbances in AC/DC system can be detected either by voltage dip or by over current at the point of common coupling (PCC) [191]. Voltage dip at PCC has been used in this work to sense fault and generate IGBT gate control pulses as shown in Figure **3.2**

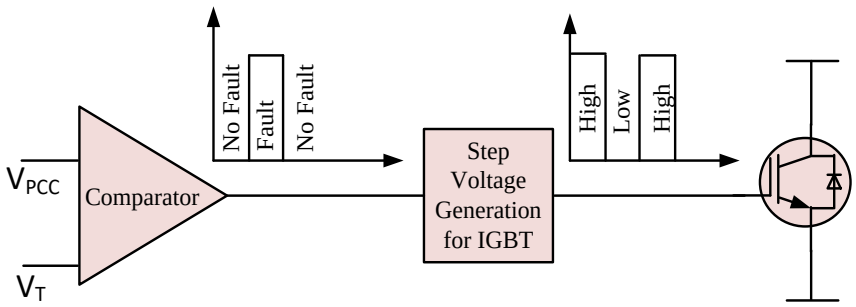

Figure 3.2 BFCL Control Strategy

PCC voltage (V_{PCC}) is compared with a predefined threshold voltage (V_T) which is considered to be 95% of the nominal V_{PCC}. At grid contingencies, PCC voltage goes on decreasing and becomes almost zero. The BFCL control scheme makes the gate signal to IGBT to go low and eventually makes the IGBT turn off. As a result, the bridge part of BFCL becomes open circuit and the parallel branch of bridge comes into effect to control fault current and to augment transient stability of the VSC-HVDC system. Afterwards, when the grid voltage increases and becomes greater than V_T due to fault clearance or by any grid voltage compensation technique, BFCL control system enables the IGBT gate signal to go high and consequently it turns on. Thus, the bridge part of BFCL becomes short circuit and parallel part is bypassed. In this way, BFCL has no impact on the system when there is no grid abnormality or voltage dip in the system. Depending on the gate signal of IGBT, shunt branch resistance or reactance of BFCL is either included or not included to control current through inner MPC. Proposed BFCL for VSC-HVDC system

is compared with series dynamic braking resistor (SDBR) in order to show the effectiveness of BFCL to reduce fault current and improve transient stability.

3.5 Proposed Voltage Source Converter-High Voltage DC (VSC-HVDC) Control Strategy

For transient stability and dynamic performance analysis, VSC-HVDC system shown in Figure 3.3 is modeled in this work.

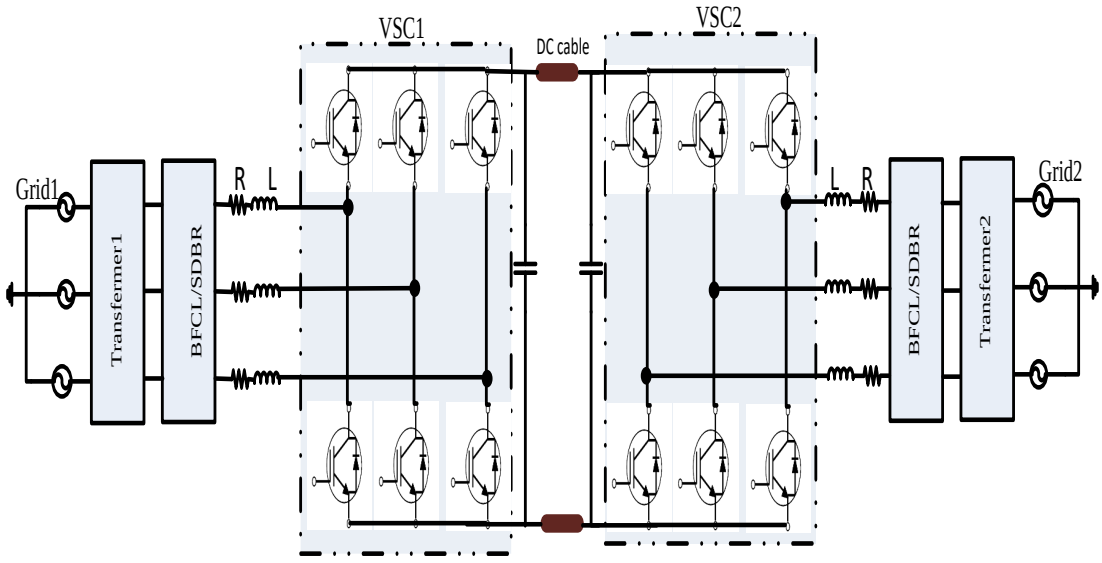

Figure 3.3 Schematic Diagram of VSC-HVDC System

The HVDC system allows bidirectional power flow between two grids depending on the reference power. For HVDC system, DC link voltage must be regulated at a prespecified value. Converter used in this work is 2-level VSC. Controller of VSC2 regulates the DC bus voltage. The power transfer between the grids must be equal (excluding converter loss) to keep the power exchange with the DC bus capacitor at zero. Proposed control technique with BFCL is described in the following subsections.

3.6 Control of Voltage Source Converter 1 (VSC1)

The function of VSC1 controller is to regulate active power exchange between the grids. According to instantaneous power theory active power and reactive power in terms of *d-q* quantities are given as follows:

$$P = \frac{3}{2}[V_d I_d + V_q I_q] \tag{3.6}$$

$$Q = \frac{3}{2}[-V_d I_q + V_q I_d] \tag{3.7}$$

The function of phase locked loop (PLL) is to regulate V_q at zero. So, putting $V_q = 0$ in above equations, the following equations can be written.

$$P = \frac{3}{2}V_d I_d \tag{3.8}$$

$$Q = -\frac{3}{2}V_d I_q \tag{3.9}$$

So, direct axis current controls the active power and quadrature axis current controls the reactive power independently given as:

$$I_{dref} = \frac{2}{3V_d} P_{ref} \tag{3.10}$$

$$I_{qref} = -\frac{2}{3V_d} Q_{ref} \tag{3.11}$$

Current from *d-q* is converted to *α-β* quantities and is used in finite model predictive control as shown in Figure **3.4**. This reference currents are considered as constant and not measured. So, this is a tracking problem in which object is to design controller which tracks the reference command.

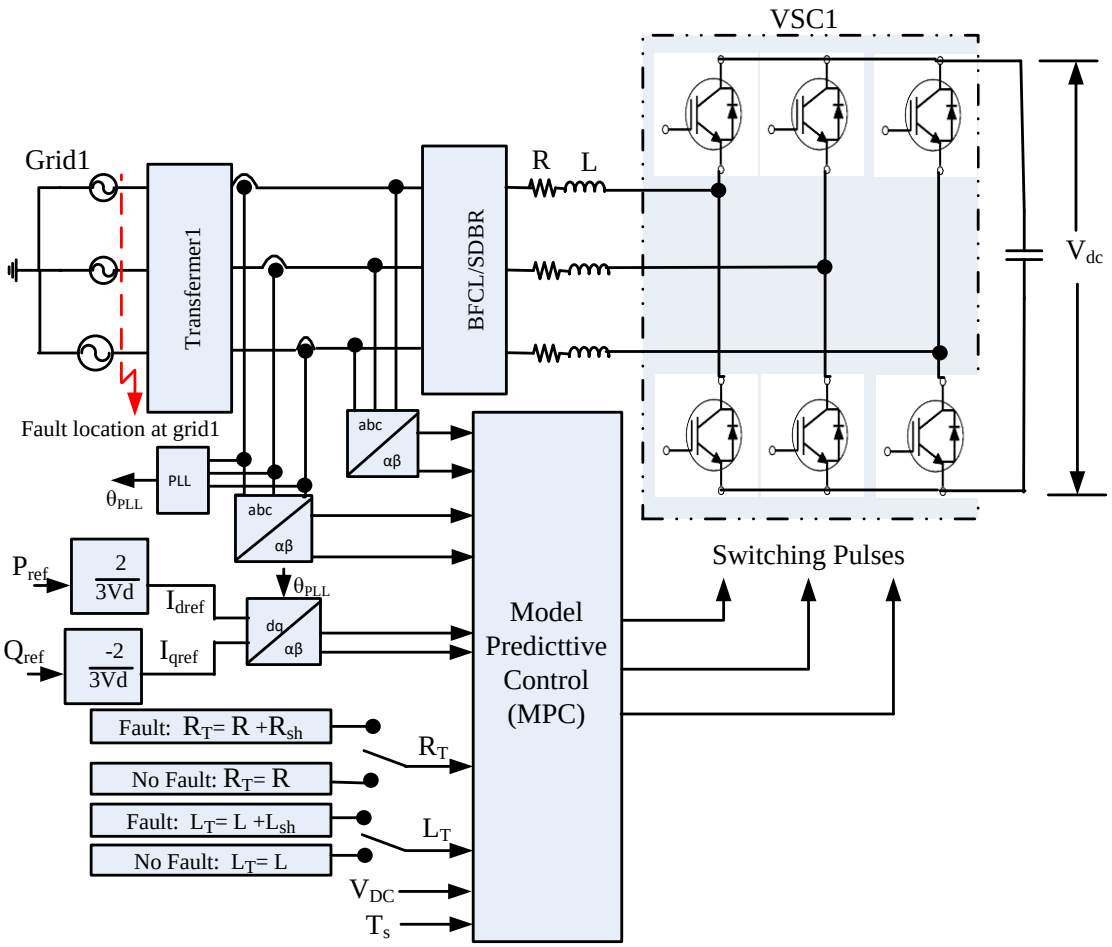

Figure 3.4 VSC1 Model Predictive Control Strategy with BFCL

In normal operating condition, bridge type fault current limiter (BFCL) or series dynamic braking resistor (SDBR) is short circuited by their controls and impedance of BFCL/SDBR is not included in inner model predictive controller (MPC) for determining optimal switching states to follow the reference power. However, during system fault, impedance of BFCL/SDBR is added with interface impedance as shown in Figure **3.4**.

Inner controller of VSC1 is MPC to regulate the current. In order to develop inner current controller for the proposed BFCL in VSC-HVDC system, it is first useful to write differential equation for the voltage source converters. VSC1 has six switches (SW_1 to SW_6) and its DC side is connected to DC link of the HVDC transmission system. AC side

of VSC1 is connected to the grid through interface reactor and resister. As shown in the simplified diagram of Figure **3.5**, the resistance and inductance are considered as total resistance and reactance including interface and BFCL/SDBR resistance and reactance. Power flow between AC and DC side of VSC1 is controlled by proper control of switching of semiconductor switches. In order to avoid short circuit of VSC1, the switches of each leg are controlled in complementary fashion. The switching signals for VSC1 are related to the several switching states in the following manner.

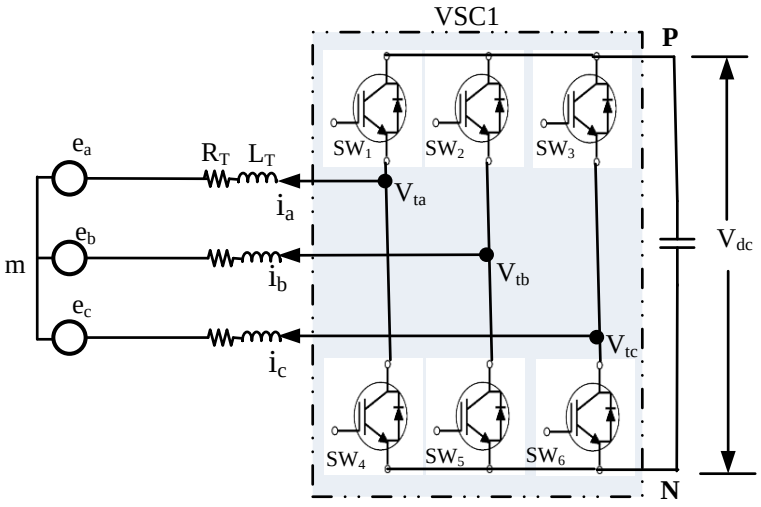

Figure 3.5 VSC1 Connection with Equivalent AC Side

$$SW_a = \begin{cases} 1 \text{ When } SW_1 \text{ is ON and } SW_4 \text{ is OFF} \\ 0 \text{ When } SW_1 \text{ is OFF and } SW_4 \text{ is ON} \end{cases} \tag{3.12}$$

$$SW_b = \begin{cases} 1 \text{ When } SW_2 \text{ is ON and } SW_5 \text{ is OFF} \\ 0 \text{ When } SW_2 \text{ is OFF and } SW_5 \text{ is ON} \end{cases} \tag{3.13}$$

$$SW_c = \begin{cases} 1 \text{ When } SW_3 \text{ is ON and } SW_6 \text{ is OFF} \\ 0 \text{ When } SW_3 \text{ is OFF and } SW_6 \text{ is ON} \end{cases} \tag{3.14}$$

The AC side terminal voltages of VSC1 is dependent of the switching signals which are described by the following relations.

$$V_{ta} = SW_a V_{dc} \tag{3.15}$$

$$V_{tb} = SW_b V_{dc} \tag{3.16}$$

$$V_{tc} = SW_c V_{dc} \tag{3.17}$$

Where V_{ta}, V_{tb}, and V_{tc} are the AC terminal to neutral (N) voltages and V_{dc} is the DC link voltage. Now, these voltages can be represented in compact form using space phasor theory [192–195].

$$V = \frac{2}{3}(V_{ta} + pV_{tb} + p^2 V_{tc}) \tag{3.18}$$

where $p = 1\angle 120 = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ is a unitary vector which provides 120^o phase displacement between phases. There are total eight possible switching states for VSC1. Depending on theses switching signals, following voltage vectors are obtained.

Table 3:1 Different Switching States and Voltage Vectors

Switching States			Space Voltage Vector for VSC1
SW_a	SW_b	SW_c	V
0	0	0	$V_0 = 0$
0	0	1	$V_1 = (-\frac{1}{3} - j\frac{\sqrt{3}}{3})V_{dc}$
0	1	0	$V_2 = (-\frac{1}{3} + j\frac{\sqrt{3}}{3})V_{dc}$
0	1	1	$V_3 = -\frac{2}{3}V_{dc}$
1	0	0	$V_4 = \frac{2}{3}V_{dc}$
1	0	1	$V_5 = (\frac{1}{3} - j\frac{\sqrt{3}}{3})V_{dc}$
1	1	0	$V_6 = (\frac{1}{3} + j\frac{\sqrt{3}}{3})V_{dc}$
1	1	1	$V_7 = 0$

With the reference to Figure **3.5**, following differential equations are written.

$$V_{ta} = L_T \frac{di_a}{dt} + R_T i_a + e_a + V_{mN} \tag{3.19}$$

$$V_{tb} = L_T \frac{di_b}{dt} + R_T i_b + e_b + V_{mN} \tag{3.20}$$

$$V_{tc} = L_T \frac{di_c}{dt} + R_T i_c + e_c + V_{mN} \tag{3.21}$$

Now according to space vector definition, the voltage and currents can be expressed as follows.

$$e = \frac{2}{3}(e_a + pe_b + p^2 e_c) \tag{3.22}$$

$$i = \frac{2}{3}(i_a + pi_b + p^2 i_c) \tag{3.23}$$

Now, putting Eq. (3.19)-(3.21) in Eq. (3.18) and using above set of equations following equations are obtained.

$$V = L_T \frac{di}{dt} + R_T i + e \tag{3.24}$$

Now, the derivative of current in above expression can be replaced by Euler approximation for a sampling time (T_s) as follows.

$$\frac{di}{dt} \approx \frac{i(k+1) - i(k)}{T_s} \tag{3.25}$$

Putting above expression in Eq. (3.24) and transforming voltage and current vectors in α-β reference frame, the predicted input current can be written in the α-β co-ordinate as below.

$$i_\alpha^{predict}(k+1) = (1 - \frac{R_T T_S}{L_T}) i_\alpha(k) + \frac{T_s}{L}[V_\alpha(k) - e_\alpha(k)] \tag{3.26}$$

$$i_\beta^{predict}(k+1) = (1 - \frac{R_T T_S}{L_T}) i_\beta(k) + \frac{T_s}{L}[V_\beta(k) - e_\beta(k)] \tag{3.27}$$

In MPC implementation, if the computation time is greater than the sampling time, a delay will be occurred between the time of current measurement and actuation of new switching states. Due to this delay converter load current oscillates around its reference value. Delay compensation has been included to mitigate this problem which predicts the current by shifting load model one step forward in time as represented by the following equations.

$$i_{\alpha}^{predict}(k+2) = (1-\frac{R_T T_S}{L_T})i_{\alpha}(k+1) + \frac{T_s}{L}[V_{\alpha}(k+1) - e_{\alpha}(k+1)] \quad (3.28)$$

$$i_{\beta}^{predict}(k+2) = (1-\frac{R_T T_S}{L_T})i_{\beta}(k+1) + \frac{T_s}{L}[V_{\beta}(k+1) - e_{\beta}(k+1)] \quad (3.29)$$

Now, the base of selecting optimum switching state in MPC is to minimize the error between reference variables and predicted variables. Therefore, a cost function '*J*' incorporating the predictive current in *α-β* reference frame is proposed. The cost function is expressed as the absolute error between reference and predicted current as follows:

$$J = \left| i_{\alpha}^{ref} - i_{\alpha}^{predict}(k+2) \right| + \left| i_{\beta}^{ref} - i_{\beta}^{predict}(k+2) \right| \quad (3.30)$$

Since there are total eight possible switching states, eight values of cost function are calculated. Afterwards, all these eight values are compared and minimum one is selected for optimal switching state application if there exist minimum. If several switching states show same minimum value, then any of them are considered as optimal switching state.

The flow chart of MPC is shown in Figure **3.6** for 2-level VSC.

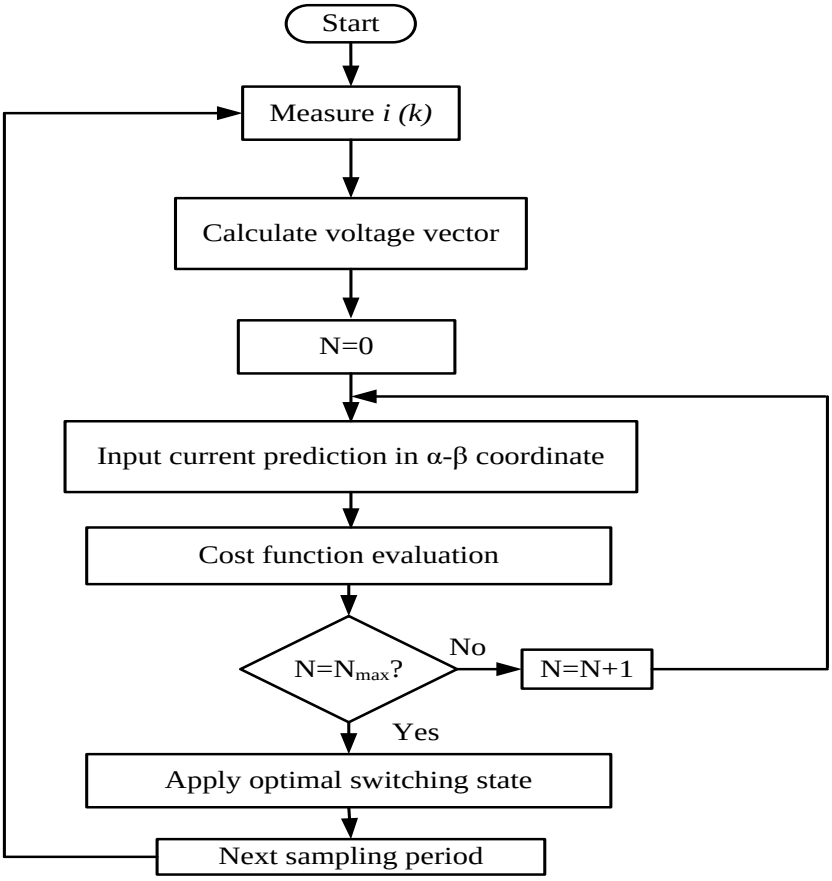

Figure 3.6 Flow Chart for MPC of the Proposed BFCL in VSC-HVDC

Two level voltage source converter is used in this work which has maximum eight different switching states (N_{max}). Inner MPC measures the current and calculates voltage vector. From the calculated voltage vector, input current is predicted in α-β coordinates. Cost function is evaluated from the reference current and predicted current. Then, optimal switching state is selected based on minimum value of the cost function.

3.7 Control of Voltage Source Converter 2 (VSC2)

Among several control strategies, DC voltage control is the main aspect of VSC-HVDC system analogous to the frequency control in classic AC power system. The system stability is directly affected by the performance of the DC voltage controller [196]. VSC2 has two controllers: outer controller for controlling DC link voltage and inner model

predictive control (MPC) for controlling current. VSC2 has similar inner MPC controller as shown in Figure **3.4** except that the reference active power (P_{ref}) for VSC2 controller is provided by outer DC link voltage controller. Outer DC link controller for VSC2 is shown in Figure **3.7**.

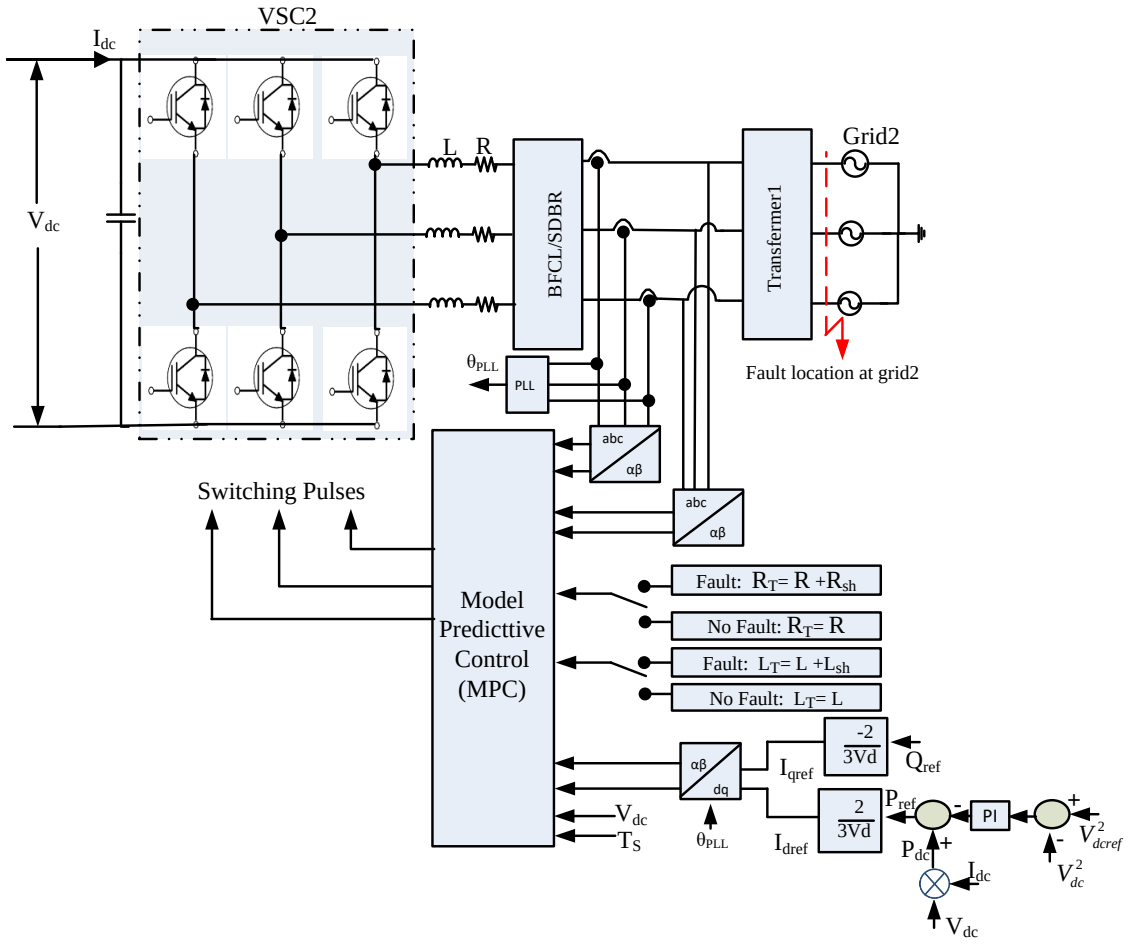

Figure 3.7 VSC2 Model Predictive Control Strategy with BFCL

Outer voltage controller is designed based on the DC voltage dynamics derived from the following power balance equation [197] .

$$P_{dc} - P_{loss} - \frac{1}{2} C \frac{dV_{dc}^2}{dt} = P_{ref} \tag{3.31}$$

where P_{dc} is the DC link power (power exchange between two grids), P_{loss} is the power loss in the DC link, and P_{ref} is the power reference for the VSC2. In outer DC link voltage

controller, square of measured DC link voltage is compared with square of reference DC link voltage and the error is controlled by proportional-integral (PI) controller. PI controller output is added with power exchange between two grids (P_{dc}) to generate reference active power for VSC2. The parameters of the outer PI controller have been tuned with the symmetrical optimum method [198].

3.8 RTDS Implementation Results and Discussions

3.8.1 RTDS Implementation

Test system of Figure 3.3 is implemented with real time digital simulator (RTDS) to validate the effectiveness of proposed MPC based BFCL solution. MPC-BFCL is also compared with SDBR to show the improvement of system performance in limiting fault current. Detail system parameters are listed in Table 3:**2**.

Table 3:2 Detailed System Parameters

Parameter	Value
HVDC system power rating	30 MVA
Grid voltage	140 kV (L-L rms)
Frequency	60 Hz
Transfer power rating	30 MVA
Voltage ratio of the transformer	140/18 kV (Delta/Y)
Interface resistor (R)	50 mΩ
Interface reactor (L)	3 mH
Equivalent DC bus capacitor	500 µF
Reference DC bus voltage	35 kV
DC cable length	25 km
DC cable resistance, inductance, and capacitance	6 mΩ/km, 0.8 mH/km, 0.20 µF/km
BFCL shunt resistor	70 mΩ

BFCL shunt inductor	7 mH
SDBR resistor	70 mΩ
Outer voltage controller K_p	0.1036
Outer voltage controller K_i	17.77

RTDS operates in real time and is a fully digital power system simulator [199]. It continuously produces output conditions that accurately characterize conditions in the real network by solving the power system equations. Thus, the RTDS has widely been recognized as an ideal tool for the design, development, and testing of power control and protection schemes.

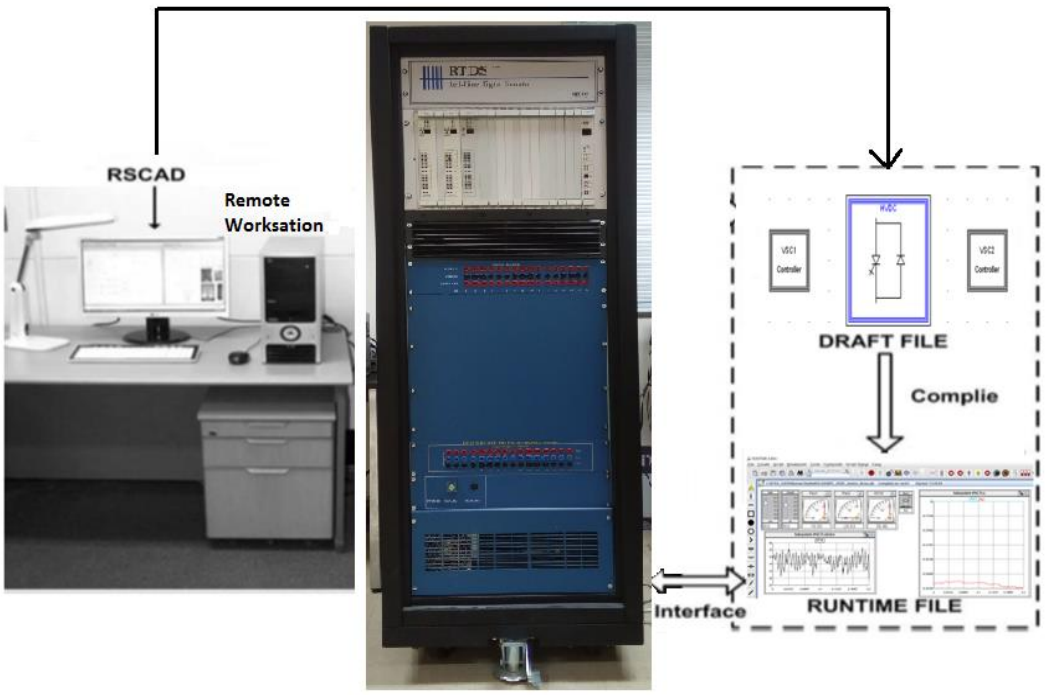

Figure 3.8 Laboratory Setup of Real Time Digital Simulator

As shown in Figure **3.8**, RTDS is connected to workstation computer via a network hub. System network is created in RSCAD software and saved as draft file. Afterwards, this file is compiled and downloaded in RTDS. In addition to draft module, RSCAD provides

runtime module for monitoring network behavior in real time. Following subsequent sections present detailed RTDS implementation results.

3.8.2 Simulation Considerations

Initially, the system is considered to be operated in its normal condition. Then symmetrical three line to ground (*3LG*) fault and different unsymmetrical faults: single line to ground (*1LG*) fault, line to line (*LL*) fault, double line to ground (*2LG*) fault are applied at both grids. The simulation time step (T_S) used in RTDS is 50 μs. Three different simulation cases are considered: without FCL, with SDBR, with proposed MPC-BFCL.

3.8.3 Symmetrical Fault Applications

Initially, DC capacitors are discharged by disconnecting HVDC system from both grids. And, getting pulses of VSC1 and VSC2 are blocked with all controllers at inactive conditions. Then, HVDC system is connected to the grids through the transformers. So, capacitors are charged gradually to a voltage level of around 25 kV through the antiparallel diodes of VSCs. Afterwards, DC link reference voltage is set to 35 kV. As a result, DC link voltage reaches to 35 kV by the control action of outer DC link voltage controller of VSC2 as shown in Figure **3.9**.

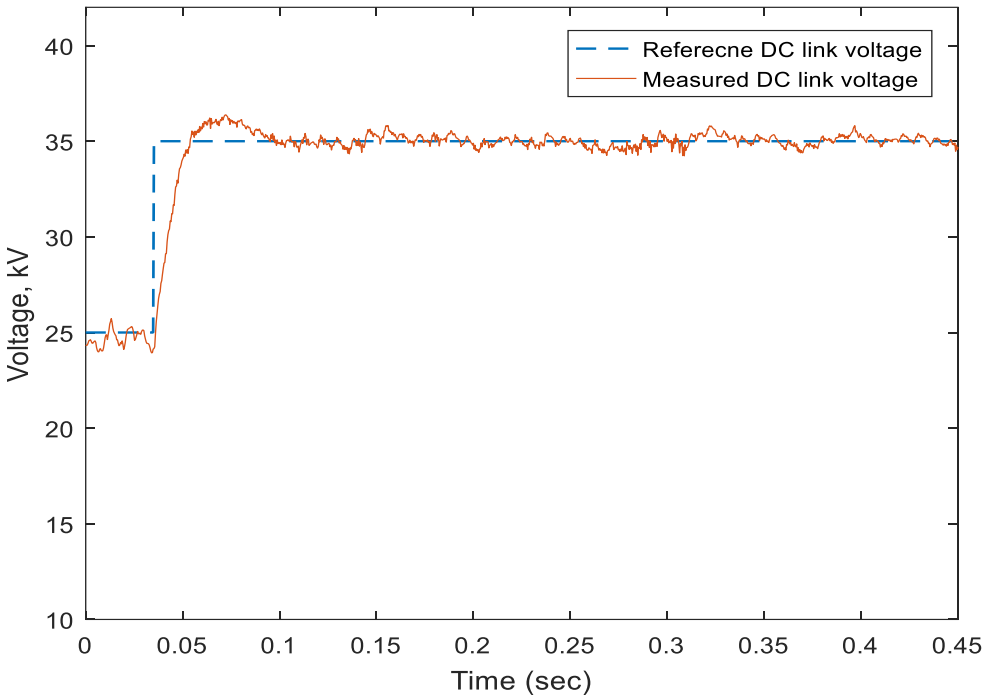

Figure 3.9 Control of DC Link Voltage

Now, 20 MW power is transferred from grid1 to grid2 by changing reference power command of VSC1 from 0 to 20 MW as shown in Figure **3.10**.

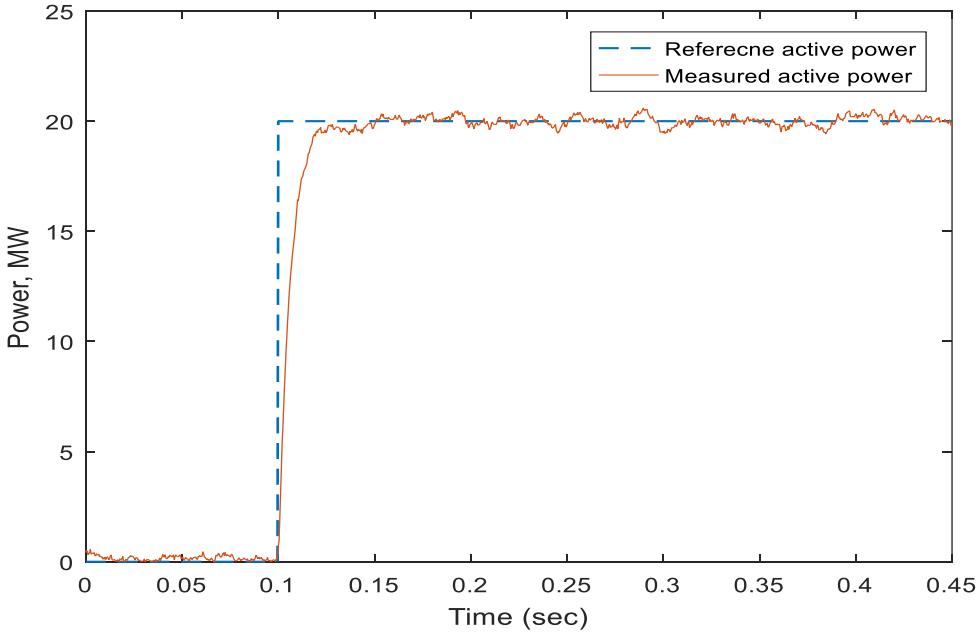

Figure 3.10 Control of Power Transfer between Two Grids

Different types of faults are now applied in the system at grid1 and grid2. Fault currents are presented and compared for both cases of SDBR and proposed MPC-BFCL. All faults have been applied for 6 cycles. Figure **3.11** shows the root-mean-square (RMS) value of current of phase 'a' of grid1 for three phase symmetrical fault applied at point of common coupling of grid1. Without fault current limiter during fault period, current of phase 'a' has a maximum RMS value of 5.013 kA. Application of SDBR reduces fault current by only 25.85%. However, proposed MPC-BFCL reduces fault current by 32.92%.

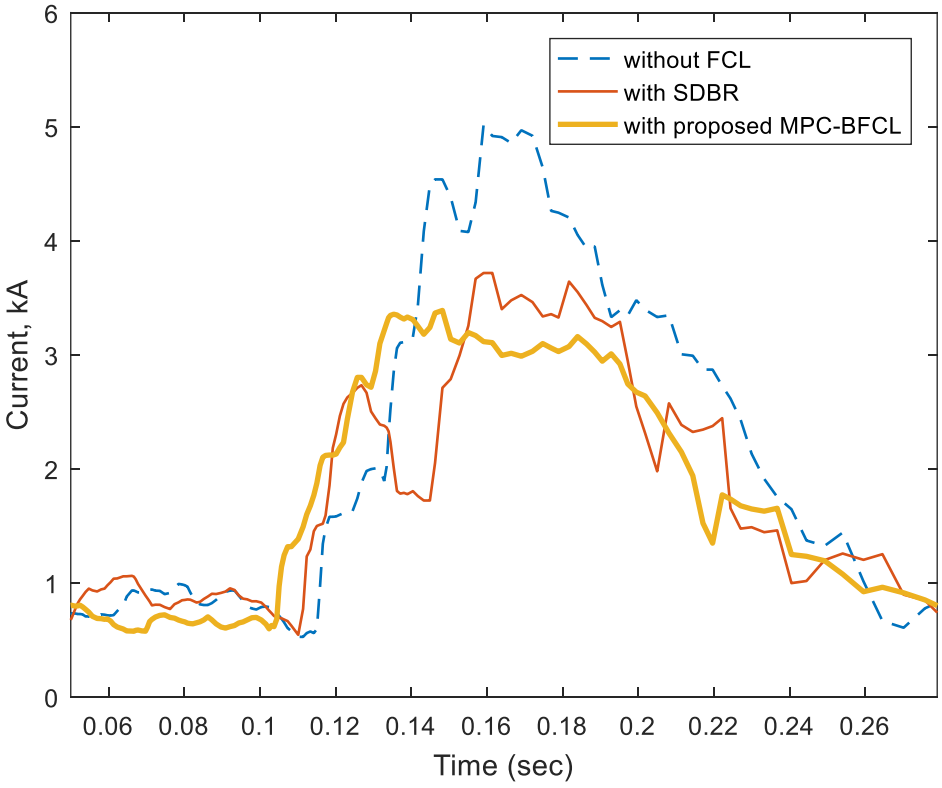

Figure 3.11 Comparative Simulation Results for Symmetrical Fault at Grid1 (Phase a Current of Grid1)

Figure **3.12** shows the current of phase 'a' of grid2 during three phase fault applied at PCC of grid2. Fault current is excessively higher without any auxiliary controller. With

the application of SDBR fault current is slightly reduced. Furthermore, proposed MPC-BFCL reduces fault current to a level that a converter can withstand easily.

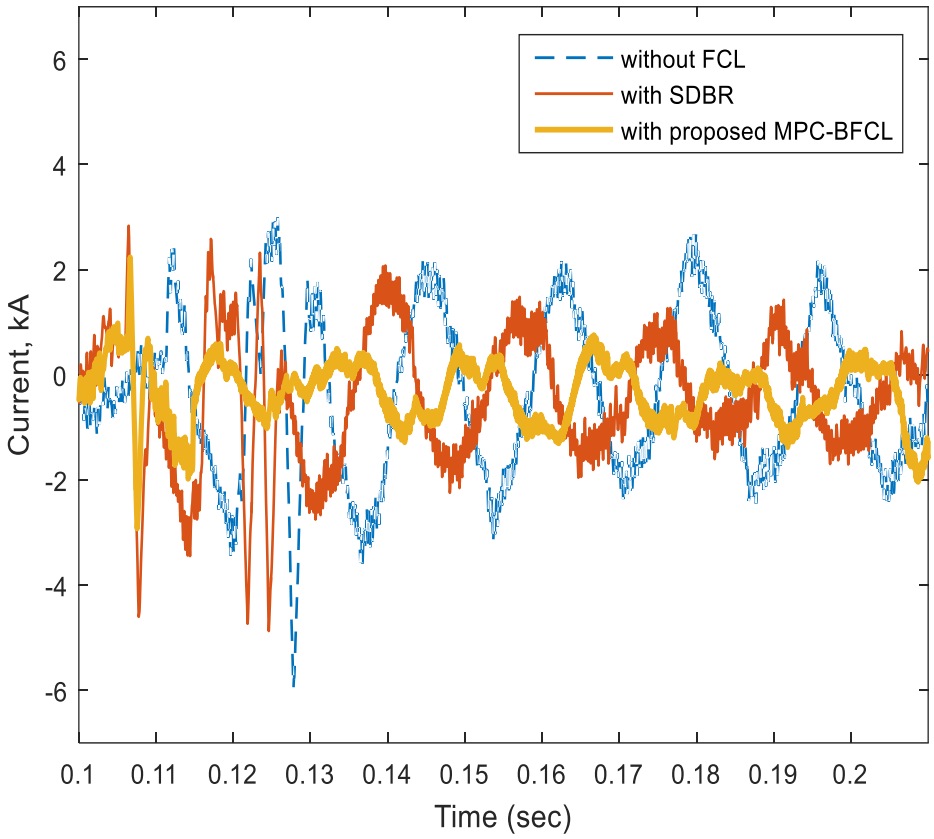

Figure 3.12 Comparative Simulation Results for Symmetrical Fault at Grid2 (Phase a Current of Grid2)

3.8.4 Unsymmetrical Fault Application

Different types of unsymmetrical faults have been applied in grid1. Real time simulation shows positive effect to reduce the fault current with the proposed MPC-BFCL. Table 3:3 shows the current of phase ‘a’ during fault period for single line to ground fault, line to line fault and double line to ground fault, and three phase fault.

Table 3:3 Peak Fault Current with Symmetrical and Different Unsymmetrical Faults

Type of faults	Positive Peak Current, kA			Negative Peak Current, kA		
	Without FCL	SDBR	Proposed MPC-BFCL	Without FCL	SDBR	Proposed MPC-BFCL
SLG	3.95	3.85	3.43	4.74	4.48	2.89
LL	6.72	6.26	4.97	8.17	5.14	4.92
LLG	8.36	6.45	5.03	7.81	7.62	5.96
Symmetrical 3-phase fault at grid1	7.61	6.91	5.20	11.81	8.88	6.00
Symmetrical 3-phase fault at grid2	3.2	3.00	2.50	6.01	4.91	3.01

It is clear from real time simulation that the current without and with SDBR is almost same for single line to ground fault. However, proposed MPC-BFCL limits the fault current very well compared to SDBR. Now, for line to line fault, proposed MPC-BFCL limits the fault current effectively compared to SDBR as presented in the above Table 3:3.

Finally, improvement of VSC-HVDC system performance in limiting fault current with proposed MPC-BFCL over SDBR for double line to ground fault application at grid1 is also presented in the Table 3:3. Without any auxiliary controller positive peak current is 8.36 kA and negative peak current is 7.81 kA. SDBR application in system reduces the positive peak current by 22.84% and negative peak current by 2.43%. Fault current reduction is further achieved by proposed MPC-BFCL, where positive peak current is reduced by 39.83% and negative peak current is reduced by 23.68%. The summary of

system performance improvement in limiting fault current with proposed MPC-BFCL for both symmetrical and unsymmetrical fault is presented in Table 3:4.

Table 3:4 Summary of Fault Current Limiting Capability of the Proposed MPC-BFCL

Type of faults	Percentage Fault Current Reduction (Positive peak)		Percentage Fault Current Reduction (Negative Peak)	
	SDBR	Proposed MPC-BFCL	SDBR	Proposed MPC-BFCL
Symmetrical Fault	9.10	29.80	27.31	49.80
SLG Fault	2.53	13.16	5.48	39.02
LL Fault	6.84	26.04	37.08	39.77
2LG Fault	22.84	39.83	2.43	22.68

3.9 Conclusions

In this chapter, model predictive control approach based BFCL is proposed to limit fault current of VSC-HVDC system. Real time digital simulation of plant and proposed controllers are developed in RTDS. From real time implementation results, MPC-BFCL is found as very effective way of limiting fault current of VSC-HVDC system. Also, approximately there is no effect of BFCL on normal operation of HVDC system. The performance of the proposed MPC-BFCL is compared with SDBR with symmetrical and different unsymmetrical faults. MPC-BFCL has been obtained as a very efficient way in limiting fault current as well as improving dynamic stability of VSC-HVDC system over SDBR as presented in literature.

CHAPTER 4

FAULT RIDE THROUGH (FRT) CAPABILITY AUGMENTATION OF FIXED SPEED WIND INTEGRATED VSC-HVDC SYSTEMS

4.1 Introduction

The power transmission by high voltage direct current (HVDC) lines shows an ever increasing trend in recent years. This technology is considered to be economic for power transmission and suitable for asynchronous operation of two AC networks. Most of the installed HVDC transmissions is based on line commutated converter (LCC). However, this converter faces problems related to commutations. A prospective solution to the commutation failure problem of HVDC system is to employ voltage source converter (VSC) which is based on insulated gate bipolar transistor (IGBT) or gate turn-off thyristor (GTO). However, VSC based HVDC system is vulnerable to faults compared to LCC based HVDC system.

Furthermore, electrical energy has been harnessed from mechanical energy using windmills for many years. In order to reduce price volatility of electricity marker and impact of fossil fuels, wind turbine is gaining more attention for harnessing electric energy. The wind turbine consists of rotor which converters kinetic energy of wind to mechanical energy. Then, induction generator is used to convert this mechanical energy

into electrical energy. Till date, most of the installed wind energy conversion system is based on fixed speed induction generator. However, fixed speed wind generator draws significant amount of reactive power and it is vulnerable to grid faults. This chapter deals with fault ride through (FRT) capability enhancement of VSC-HVDC systems with bridge type fault current limiter controller in two different mode: two grid connected mode and fixed speed wind farm mode.

4.2 System Modeling and Controller Design

For transient stability and dynamic performance analysis, two grids connected VSC-HVDC system and fixed speed induction generators based wind farm integrated VSC-HVDC system are considered. Fixed speed induction generator based wind integrated VSC-HVDC system is shown in Figure **4.1**.

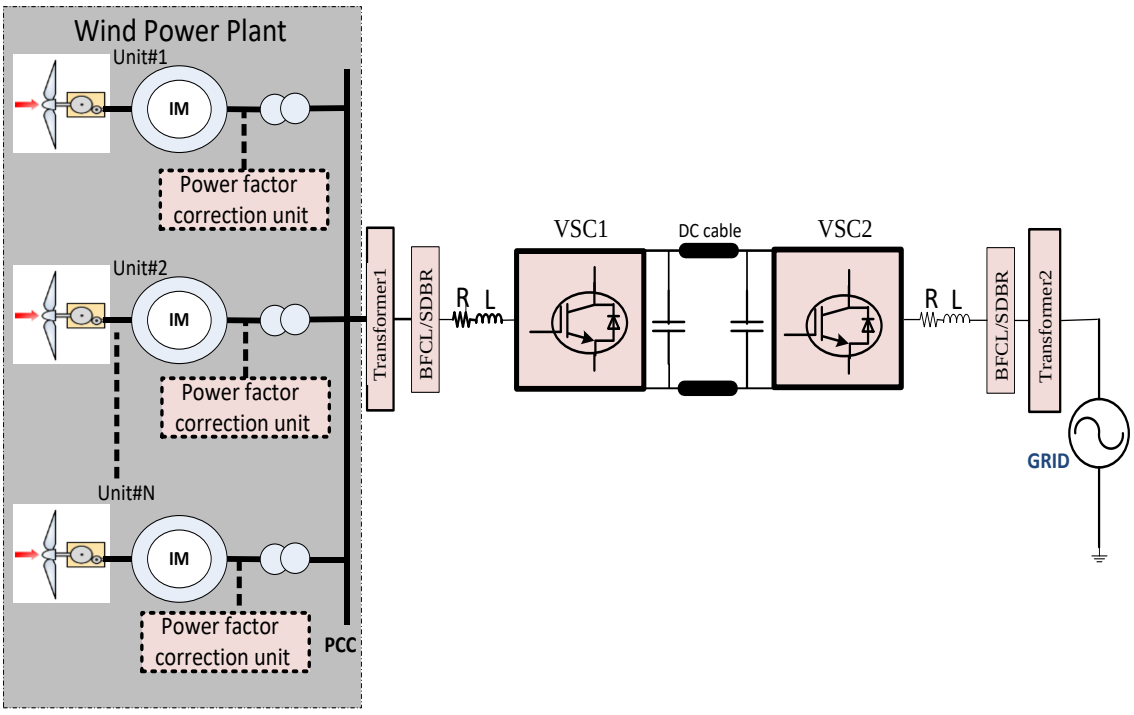

Figure 4.1 Fixed Speed Wind Integrated VSC-HVDC System.

Two grids connected VSC-HVDC system allows bidirectional power flow between the grids depending on the reference power. The direction of power flow depends system planning or power trading agreement between two grids. Whereas, power transfer is unidirectional from wind farm to the grid for wind farm integrated VSC-HVDC system. For HVDC system, DC link voltage must be regulated at a prespecified value. Converter used in this work is 2-level VSC. Controller of VSC2 regulates the DC bus voltage. Proposed control technique with BFCL is described in the following subsections.

4.2.1 Wind Power Plant Modeling

Wind power plant consists of wind turbine, gearbox, induction machine, power factor correction capacitor unit, interface transformer.

Wind turbine model consists two major parts one of which computes the energy available in the wind and other calculates efficiency of the turbine in converting wind energy to torque. Available kinetic energy from wind speed is given by the following formula.

$$KE = 0.5\rho\pi r^2 V_w^3 t \text{ Joules} \tag{4.1}$$

Where ρ is density of air in kg/m^3, r is the radius of the wind turbine in meter, V_w is wind speed in m/s, t the time in second. Energy divided by time gives the power which is represented in the following equation.

$$P = 0.5\rho\pi r^2 V_w^3 \text{Watts} \tag{4.2}$$

The amount of power extracted from wind turbine highly depends on wind turbine efficiency. The maximum efficiency of wind turbine is around 59.3 percent which is known as Betz's limit [89]. So, taking into consideration of Betz's limit available power extracted from wind turbine is given by the following equation.

$$P = 0.5\rho\pi r^2 V_w^3 C_p(\lambda, \beta) \text{ Watts} \quad (4.3)$$

In order to model the wind turbine, the power coefficient (C_p) must be known to compute the amount of power produced by the turbine for a given wind speed. C_p is highly nonlinear function of pitch angle (β) and tip speed ratio (λ). Power coefficient with wind is shown in Figure **4.2**.

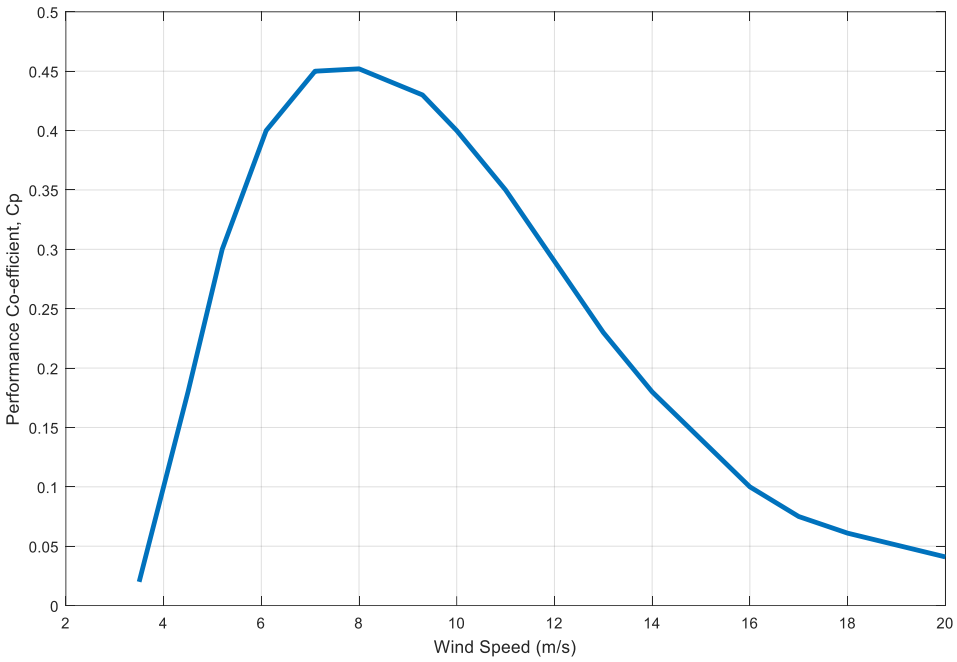

Figure 4.2 Wind Speed versus Performance Co-Efficient Curve

The amount of power generated by wind turbine for different speed is shown in Figure 4.3

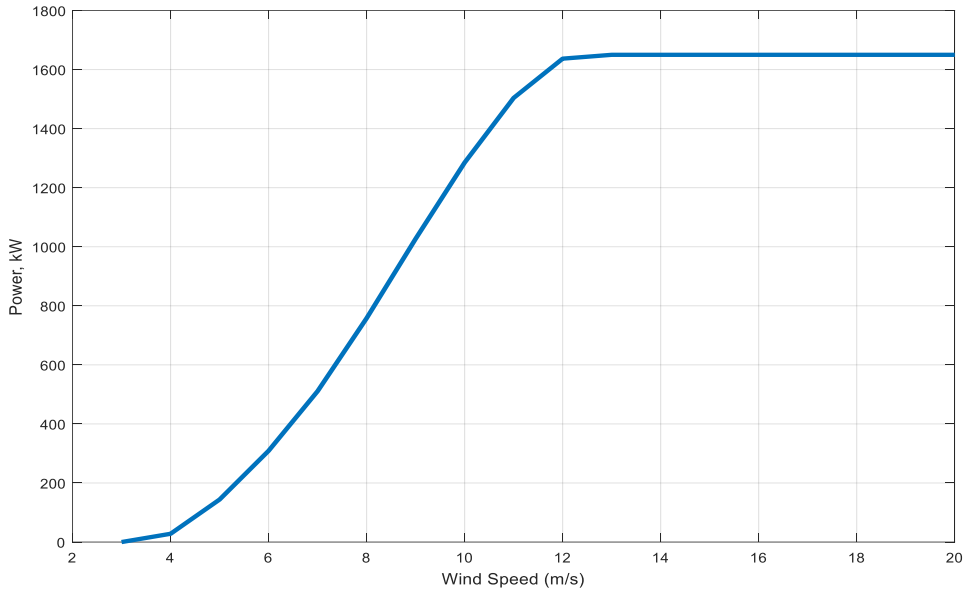

Figure 4.3 Wind Speed versus Power

Turbine blades are designed to stall if the wind speed exceeds a designed maximum. Active stall blades have the features that their pitch angle can be adapted dynamically to adjust efficiency. Wind turbine is connected to the induction machine through gear box as shown in Figure 4.1 *a*. Torque is provided from the wind turbine model as input to the induction machine and induction machine provides shaft speed back to the turbine model. A number of capacitor banks equipped with switches are connected at the terminal of the induction machine. A control loop is designed among the switches in order to maintain power factor within a set-point range. Several wind generating units are connected at the point of common coupling (PCC) to achieve a desired power delivery to the grid through the HVDC link.

4.2.2 Control of VSC1

The active power exchange between the grids is controlled by the controller of VSC1. Additionally, reactive power interchange between grid and point of common coupling

(PCC) can be controlled by VSC1 in order to control AC voltage at PCC. Active (P_s) and reactive power (Q_s) exchange in terms of direct and quadrature axis quantities, according to instantaneous power theory, can be represented as follows.

$$P_s = \frac{3}{2}[V_d I_d + V_q I_q] \tag{4.4}$$

$$Q_s = \frac{3}{2}[-V_d I_q + V_q I_d] \tag{4.5}$$

Where V_d and I_d are direct axis voltage and current respectively and V_q and I_q are quadrature axis voltage and current respectively. V_q can be regulated at zero by employing phase locked loop (PLL). The structure of PLL is given in Figure **4.4**.

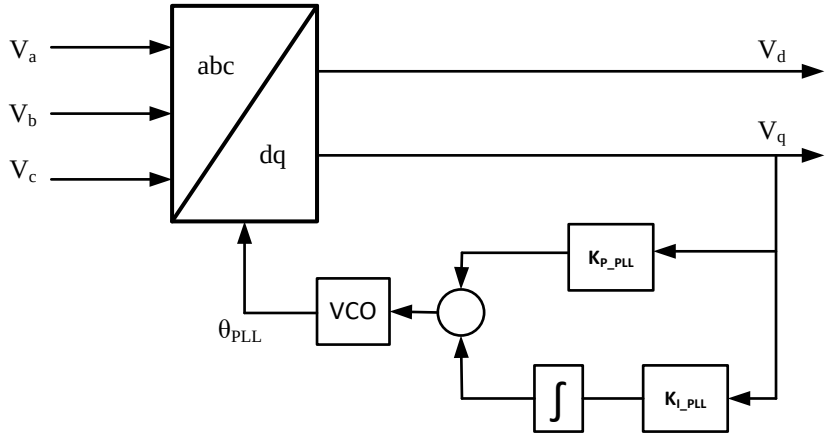

Figure 4.4 Structure of PLL

So, the PLL model is employed and based on aligning the angle of *dq* transformation system such that *q*-axis component of voltage is zero. Now, following two equations can be written for active and reactive power by putting $V_q = 0$ in above equations.

$$P_s = \frac{3}{2} V_d I_d \tag{4.6}$$

$$Q_s = -\frac{3}{2} V_d I_q \tag{4.7}$$

So, active and reactive power can be regulated by controlling direct and quadrature axis currents respectively given as:

$$I_{dref} = \frac{2}{3V_d} P_{sref} \tag{4.8}$$

$$I_{qref} = -\frac{2}{3V_d} Q_{sref} \tag{4.9}$$

So the block diagram for reference current generation in d-q frame is shown in Figure **4.5**.

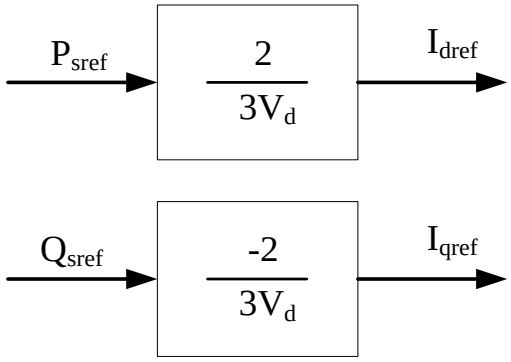

Figure 4.5 Direct and Quadrature Reference Current Generation from Active and Reactive Power

Now, following set of equations can be written for VSCs of Figure **4.1** using transformation technique (*a-b-c* to *d-q*) and considering steady state operating condition of the VSC-HVDC system.

$$L\frac{dI_d}{dt} = L\omega_0 I_q - RI_d + V_{td} - V_d \tag{4.10}$$

$$L\frac{dI_q}{dt} = -L\omega_0 I_d - RI_q + V_{tq} - V_q \tag{4.11}$$

$$V_{td} = \frac{V_{DC}}{2} m_d \tag{4.12}$$

$$V_{tq} = \frac{V_{DC}}{2} m_q \tag{4.13}$$

Where, *abc* to *dq* transformation matrix is given as follows.

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & sin(\theta - \frac{2\pi}{3}) & -sin(\theta - \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (4.14)$$

Using above set of equations and third harmonic injected PWM technique, VSC1 controller has been developed as shown in Figure 4.6 to control active and reactive power.

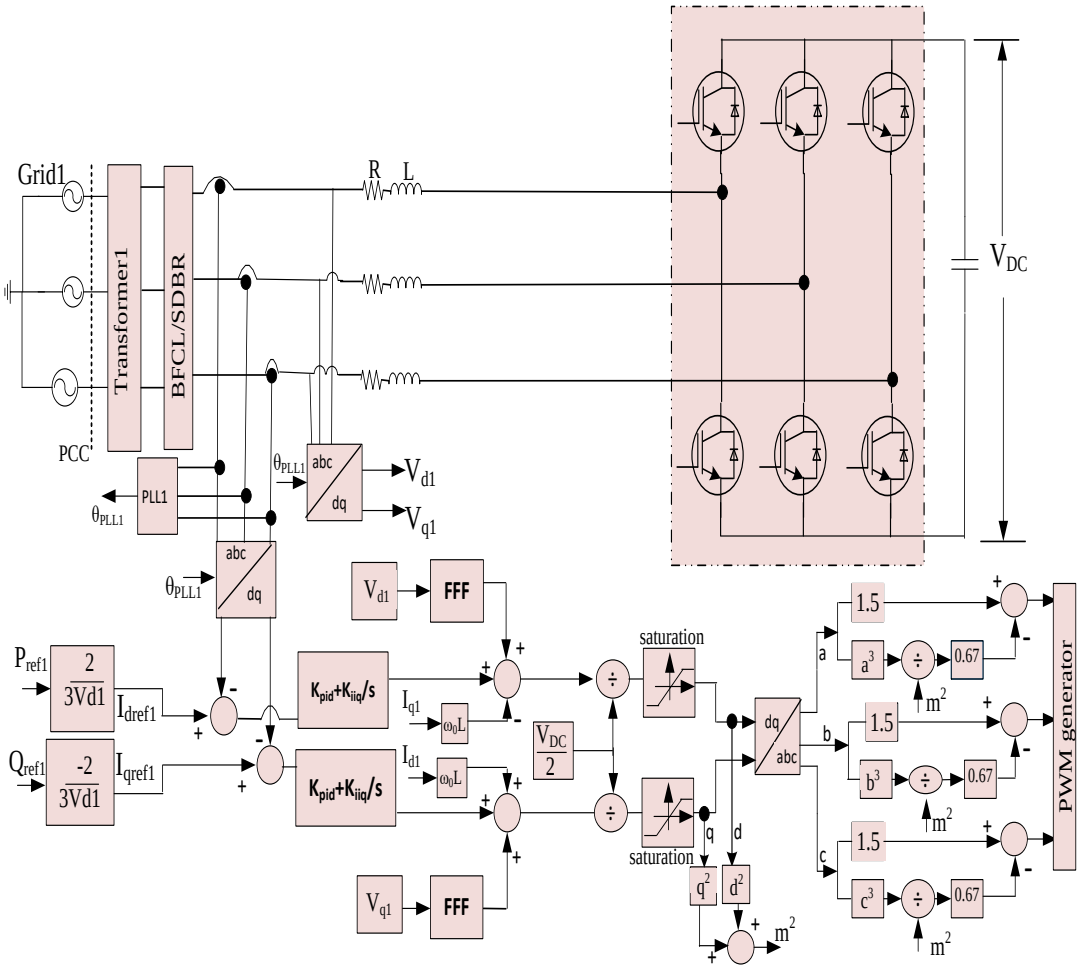

Figure 4.6 Control Strategy of VSC1 with BFCL

As shown in Figure 4.6 active and reactive power are controlled by inner current controller with corresponding direct and quadrature current controlling. PI controllers are

employed for both direct axis and quadrature axis currents. Pole-zero cancellation technique has been used to tune inner current controller parameters. Undesirable start-up transient has been avoided by augmenting the control scheme with a feed forward filter (FFF). Third harmonic injected PWM technique is used to make the VSC voltage within permissible limit.

4.2.3 Control of VSC2

Among several control strategies, DC voltage control is the main aspect of VSC-HVDC system analogous to the frequency control in classic AC power system. The system stability is greatly influenced by DC link capacitance [200] and control of voltage across DC link [196,201]. VSC2 has two controllers: outer controller for regulating the DC link voltage and inner controller for regulating the current. VSC2 has similar inner current controller as shown in Figure 4.6 except that the P_{ref} for VSC2 controller is provided by outer DC link voltage controller. Outer DC link voltage controller for VSC2 is shown in Figure **4.7**.

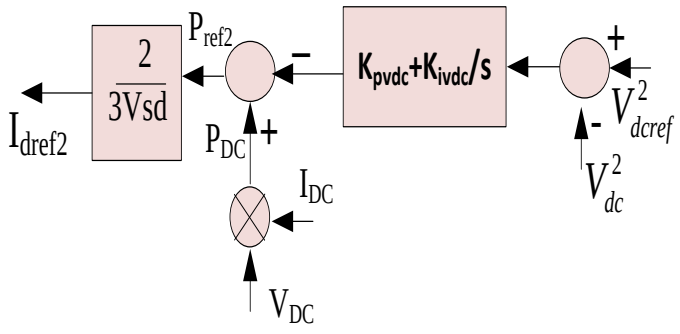

Figure 4.7 Outer DC Link Voltage Controller for VSC2

In outer DC link voltage controller, square measured DC link voltage is compared with square of reference DC link voltage and the error is controlled by proportional-integral (PI) controller. PI parameters have been tuned with symmetrical optimum method [198]. PI controller output is added with power exchange between two grids or wind farm and grid (P_{DC}) to generate reference active power for VSC2. It is worth mention that any other controller can be employed instead of PI controller.

4.2.4 Inner and Outer PI Parameters Tuning

As discussed in the previous sections, VSC1 has one control loop which controls current. On the other hand, VSC2 has both inner current control loop and outer voltage control loop. PI controllers are employed in both inner current control loop and outer voltage control loop. Methods for determining PI parameters are presented in the following sections.

A. PI parameter tuning for inner current controller

The transfer functions for direct and quadrature axis inner current control is shown Figure 4.8.

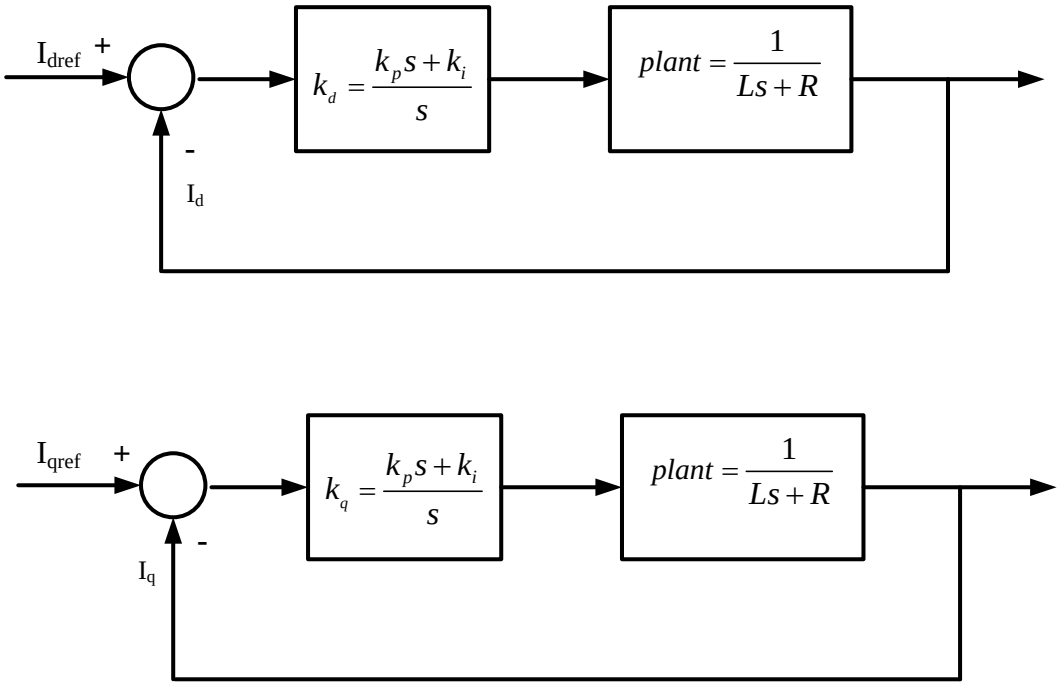

Figure 4.8 Control Block of Inner Current Controller

We have following transfer function for PI controller.

$$k_d = \frac{k_p s + k_i}{s} \tag{4.15}$$

Where, k_p and k_i are the proportional and integral gains respectively.

Open loop transfer function is given by the following equation.

$$G_{op} = (\frac{k_p}{Ls}) \frac{s + \frac{k_i}{k_p}}{s + \frac{R}{L}} \tag{4.16}$$

Open loop transfer function has pole -R/L. Normally, this pole is close to origin and shows slow natural response. So, this pole can be cancelled by zeros at $-k_i/k_p$.

So, after pole zero cancellation, we have open loop transfer function.

$$G_{op} = \frac{k_p}{Ls} \tag{4.17}$$

Now, close loop transfer function is given as follows.

$$G_{cl} = \frac{\frac{k_p}{Ls}}{1+\frac{k_p}{Ls}} \tag{4.18}$$

After simplifying above equation, we get following equation for closed loop transfer function.

$$G_{cl} = \frac{1}{\tau_i s+1} \tag{4.19}$$

Where τ_i is the desired time constant of the close loop system, and normally lies in the range 0.5ms to 5 *ms*. So, in the design process, first τ_i is chosen. Then, proportional gain is calculated using the following rule.

$$k_p = \frac{L}{\tau_i} \tag{4.20}$$

Then, integral gain is calculated using following equation.

$$k_i = k_p(\frac{R}{L}) \tag{4.21}$$

B. PI parameter tuning for outer voltage controller

The transfer function block diagram of the system outer voltage controller is shown in Figure 4.9.

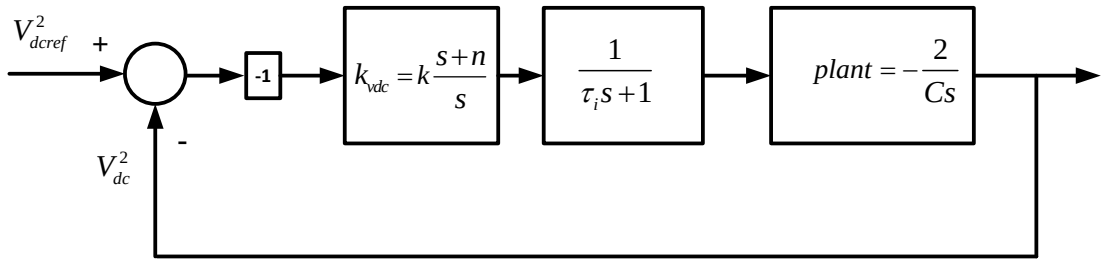

Figure 4.9 Control Block of Outer Voltage Controller

System transfer function is given in the following equation.

$$G_{sys} = -\frac{1}{\tau_i s + 1}\frac{2}{Cs} \tag{4.22}$$

The system has a pole at zero (s=0) and one real pole at s=-1/ τ_i. Such system can be stabilized with zero steady state error employing PI controller.

Open loop transfer function is given by following transfer function.

$$G_{op} = \frac{2k}{C\tau_i}\frac{s+n}{s+\tau_i^{-1}}\frac{1}{s^2} \tag{4.23}$$

In the following steps, symmetrical optimum method is employed to design PI parameters for the outer voltage controller from the above transfer function.

Step 1: Find *n* for specific phase margin (δ_m) using following rule.

$$\delta_m = sin^{-1}(\frac{1-\tau_i n}{1+\tau_i n}) \tag{4.24}$$

Step 2: Find cross over frequency ω_c using following rule.

$$\omega_c = \sqrt{n\tau_i^{-1}} \tag{4.25}$$

Step 3: Finally, find *k* to make $\left|G_{op}(j\omega_c)\right| = 1$

4.3 RTDS Implementation Results and Discussions

4.3.1 Systems and Controllers Data

Test system of Figure 4.1 are implemented in real time digital simulator (RTDS) to validate the effectiveness of proposed BFCL solution. BFCL is also compared with SDBR to show the improvement of systems performance in limiting fault current. Same value of resistors is used for both BFCL and SDBR for fair comparison. Detailed VSC-HVDC system (with controllers) and wind system data are listed in Table 4:1 and Table 4:2 respectively.

Table 4:1 HVDC System and Controller Parameters

Parameter	Value
HVDC system power rating	30 MVA
Grid voltage	140 kV (l-l rms)
Frequency	60 Hz
Transfer power rating	30 MVA
Voltage ratio of the transformer	140/18 kV (Delta/Y)
Leakage inductance of transformer referred to delta side	110 mH
Interface resistor (R) and reactor (L)	88 mΩ and 8.5 mH
DC cable length	25 km
DC cable resistance, inductance, and capacitance	6 mΩ/km, 0.8 mH/km, 0.20 µF/km
DC capacitance	500 µF
Reference DC bus voltage	35 kV
BFCL shunt resistor and inductor	10 mΩ and 2 mH
R_{DC} and L_{DC} of BFCL	0.1 mΩ and 0.1 mH
SDBR resistor	10 mΩ
Inner current controller K_{pid}	8.5
Inner current controller K_{iiq}	88
Outer voltage controller K_{pvdc}	0.1036
Outer voltage controller K_{ivdc}	17.77
Feed forward function (FFF)	$1/(1+7\times10^{-6}s)$

Table 4:2 Wind Power Plants Parameters

Parameter	Value
Rotor blade radius	41 m
Wind speed (cut-in/nominal/cut-out)	3.5 / 13 / 20 m/s
Nominal turbine speed	14.4 rpm
Rated power	1.65 MW
Induction machine	6 pole, 1200 rpm
Induction machine speed at rated power	1207 rpm

Rated slip	0.00167
Gear box ratio	84.5
Power factor correction capacitors	499.4 kVAR
Stator resistance	0.0077 Ω
Rotor resistance	0.0062 Ω
Stator reactance	0.0697 Ω
Magnetizing reactance	3.454 Ω
Rotor reactance	0.0834 Ω

4.3.2 Symmetrical Faults in Grids Connected VSC-HVDC Systems.

At the beginning, controllers for VSC1 and VSC2 are kept inactive conditions and the DC capacitors are discharged by disconnecting HVDC system from both grid. Afterwards, capacitors are charged gradually charged by connecting HVDC system to the grid through the transformers. Now, all controllers are activated and reference voltage of DC link is step changed to regulated DC voltage at 35 kV. Different types of faults are then applied in the system at grid1. DC link voltage, line active power, and line current are presented and compared for both cases of SDBR and proposed BFCL. All faults have been applied for 6 cycles. Figure 4.10 shows the transient response improvement of VSC-HVDC system with symmetrical three phase fault applied in grid1. Figure **4.10** shows that DC link voltage fluctuates between 0.552 p.u. to 1.736 p.u. without any auxiliary controller. This fluctuation is reduced with SDBR controller to the range of 0.6344 p.u. to 1.488 p.u. However, DC link voltage oscillation is greatly suppressed with the proposed BFCL controller keeping the voltage fluctuation between 0.8714 p.u. to 1.129 p.u. Moreover, DC link voltage reaches to its reference value of 35 kV at 0.8 second whereas it takes 2 seconds with SDBR and 2.4 seconds without any FCL.

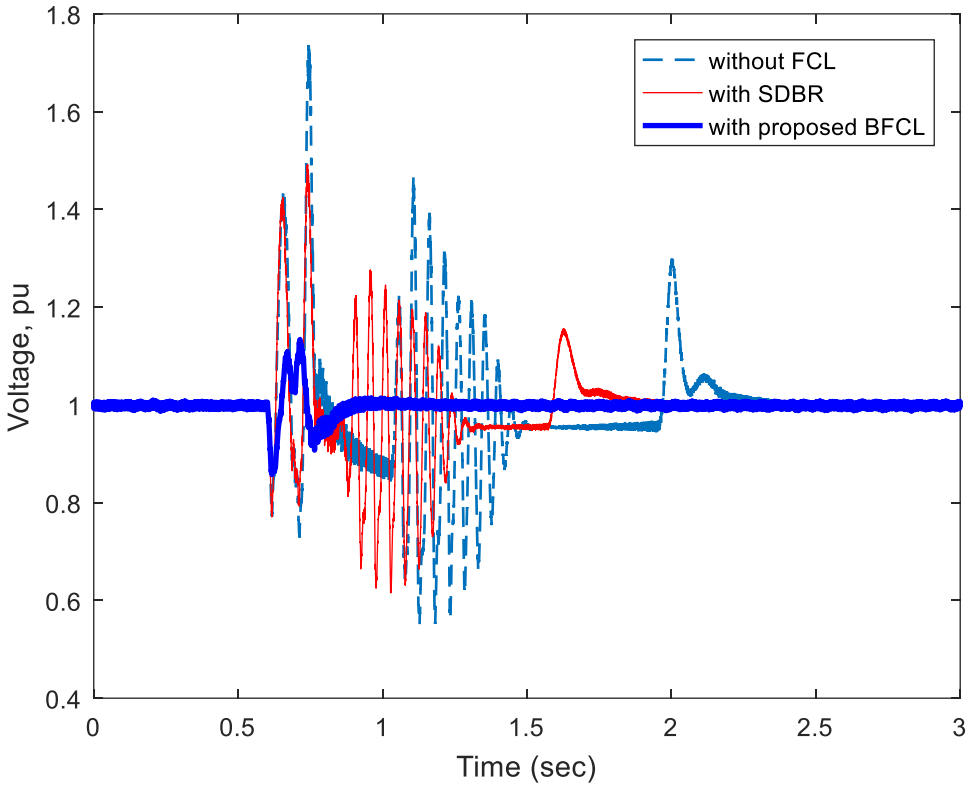

Figure 4.10 DC Link Voltage Response for Symmetrical Fault

Power oscillation minimization and fault current limiting capability of the proposed BFCL solution have been clearly visualized in Figure 4.11 and Figure 4.12 respectively for 3LG fault at grid1.

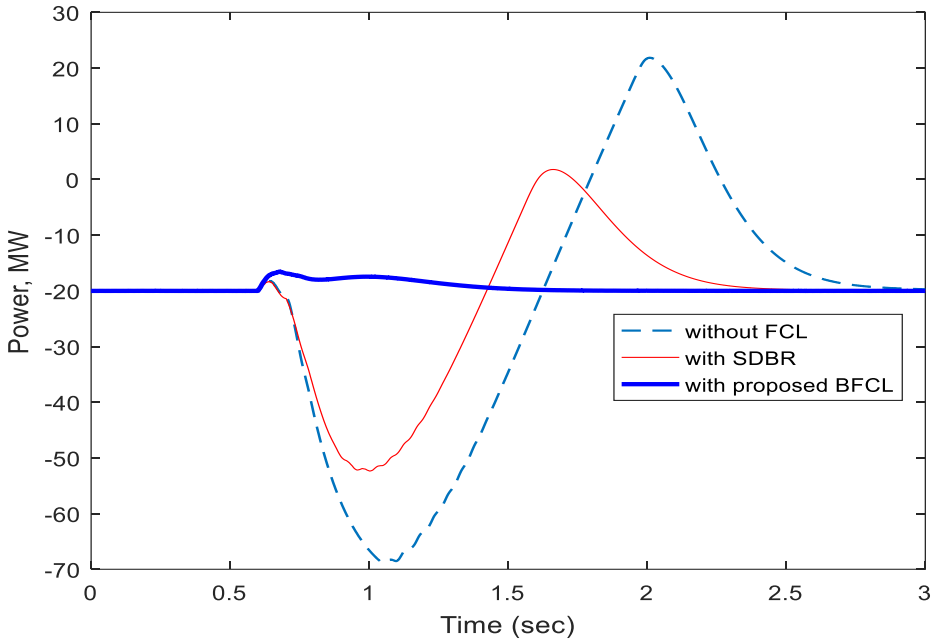

Figure 4.11 Active Power Response for Symmetrical Fault

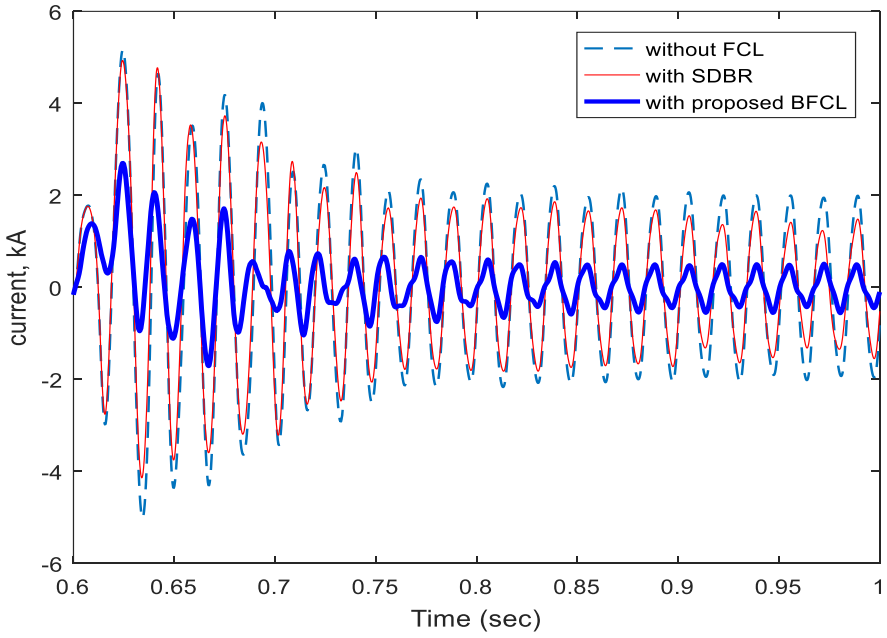

Figure 4.12 Response in Line Current for Symmetrical Fault

Performance of the proposed BFCL based control strategies is also in VSC-HVDC System is also investigated with different fault resistance. DC link voltage fluctuations with different fault resistances are visualized in Figure 4.13.

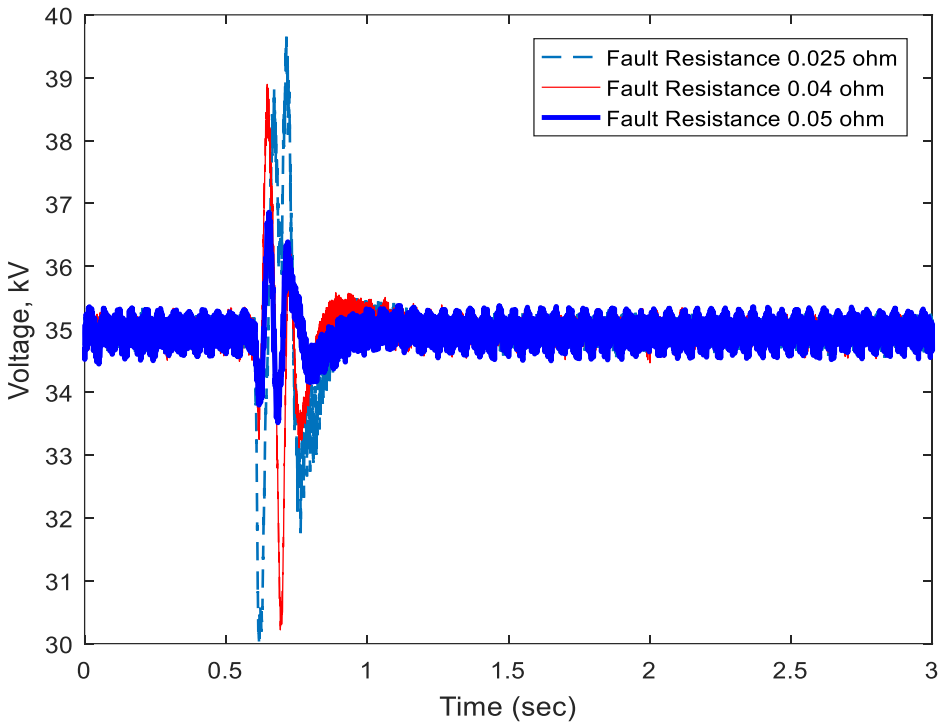

Figure 4.13 DC Link Voltage Variations with Different Fault Resistances

Oscillation in active power for symmetrical fault with different fault resistances is shown in Figure **4.14**.

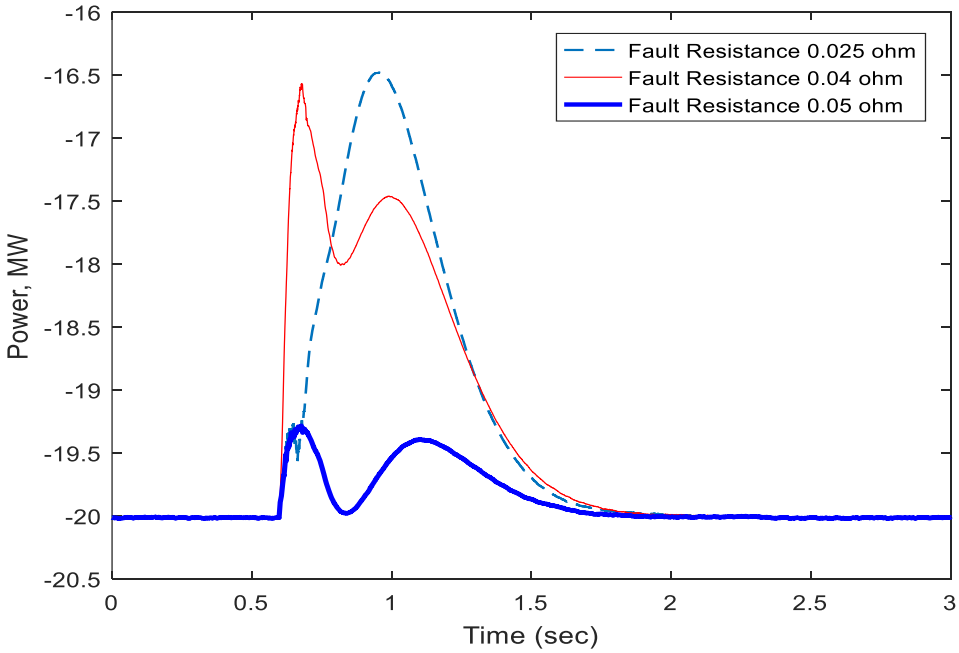

Figure 4.14 Active Power Oscillation with Different Fault Resistances

Robustness of the proposed BFCL based control strategy is investigated by system parameter variation. The leakage inductance of the interface transformer is changed to check the robustness. Performance in tracking reference DC link voltage with leakage inductance variation is shown in Figure **4.15**.

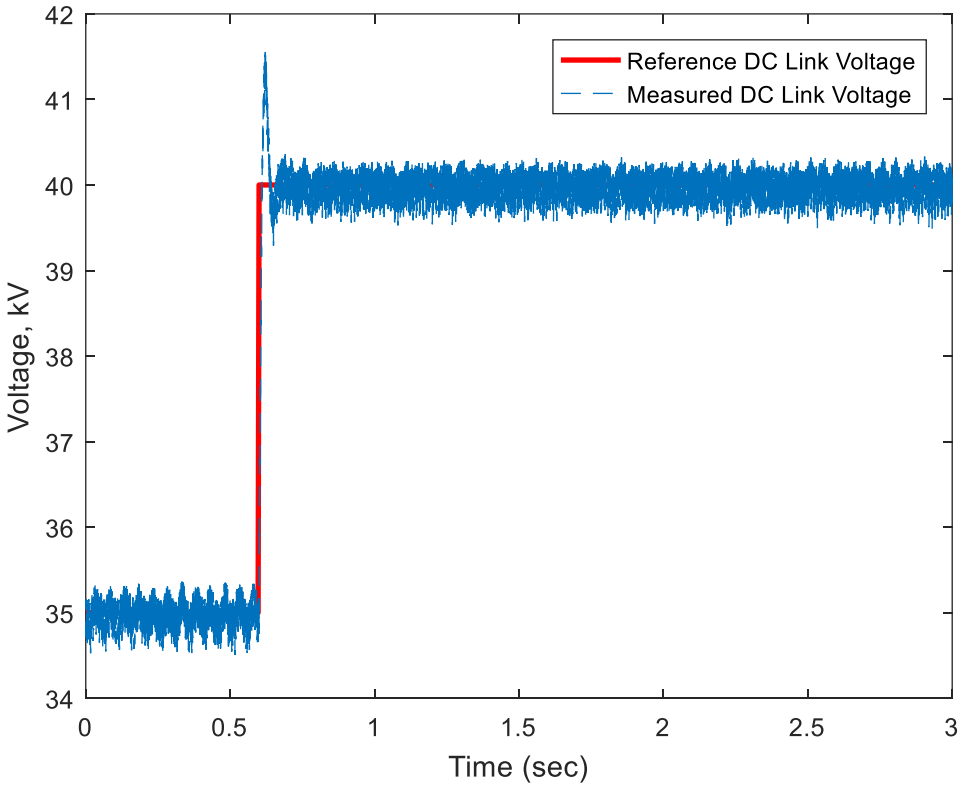

Figure 4.15 Robustness of Controller with Leakage Inductance Variation

4.3.3 Symmetrical Faults in Wind Farm Integrated VSC-HVDC Systems.

Three phase symmetrical fault is applied to wind farm integrated VSC-HVDC system. Figure 4.16 shows that induction machine speed fluctuates over a wide range of 1205 RPM to 1218 RPM without any auxiliary controller for symmetrical fault applied at PCC. System performance improvement is observed by slight speed fluctuation reduction with SDBR. However, machine speed oscillation is greatly damped with proposed BFCL

controller. Moreover, machine speed reaches to its steady state value at 0.9 seconds with BFCL whereas it takes 1.5 seconds with SDBR. Without any controller machine speed reaches to its steady state value at around 2.3 seconds. Machine stator fault current reduction and DC link voltage oscillation minimization with the proposed BFCL solution have been clearly visualized in Figure 4.17 and Figure 4.18 respectively for 3LG fault at PCC.

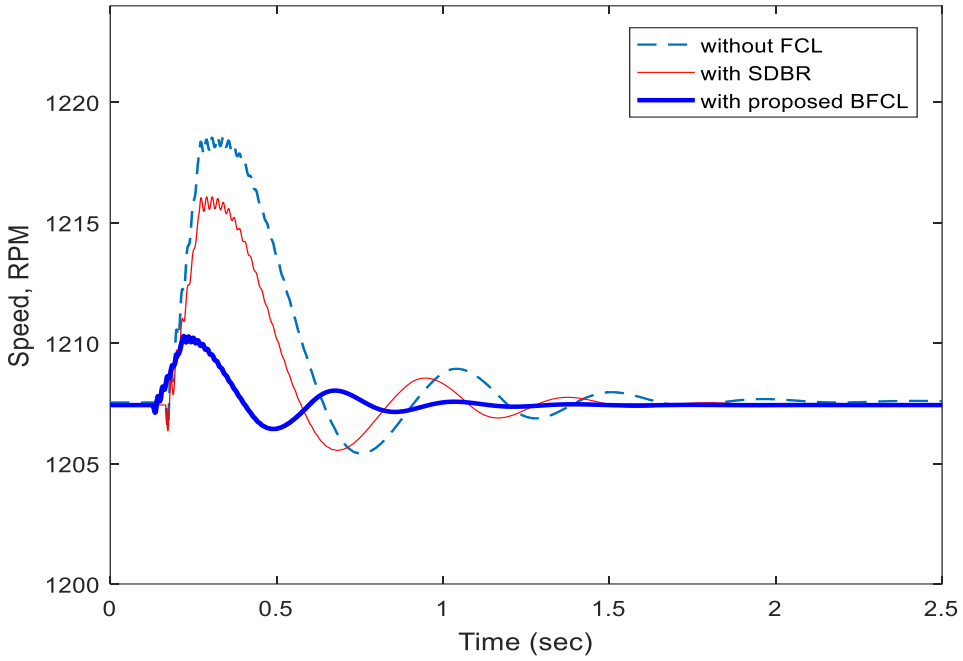

Figure 4.16 Machine Speed of Fixed Speed Wind Integrated VSC-HVDC

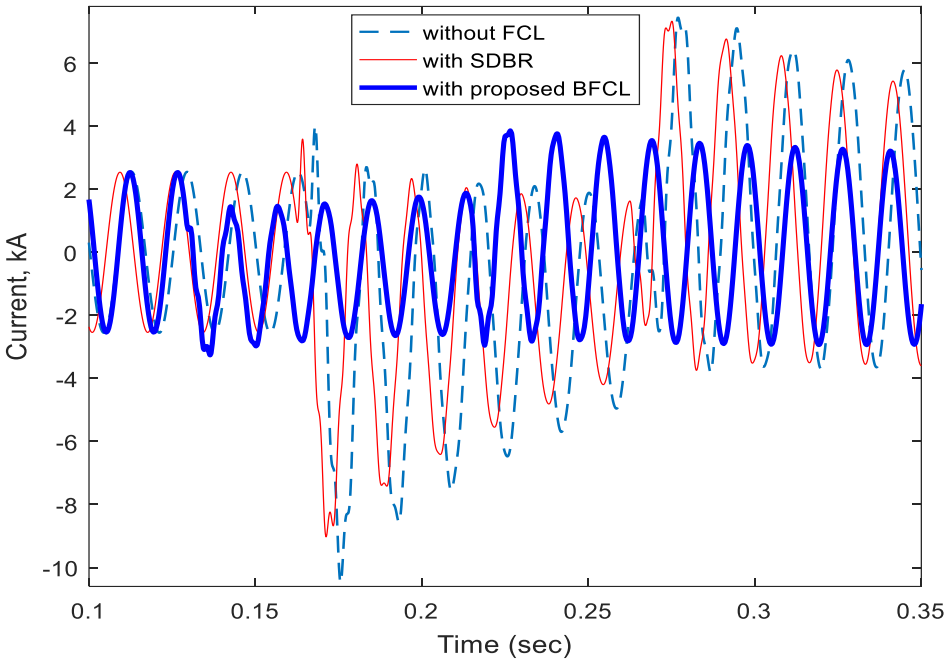

Figure 4.17 Line Current of Fixed Speed Wind Integrated VSC-HVDC

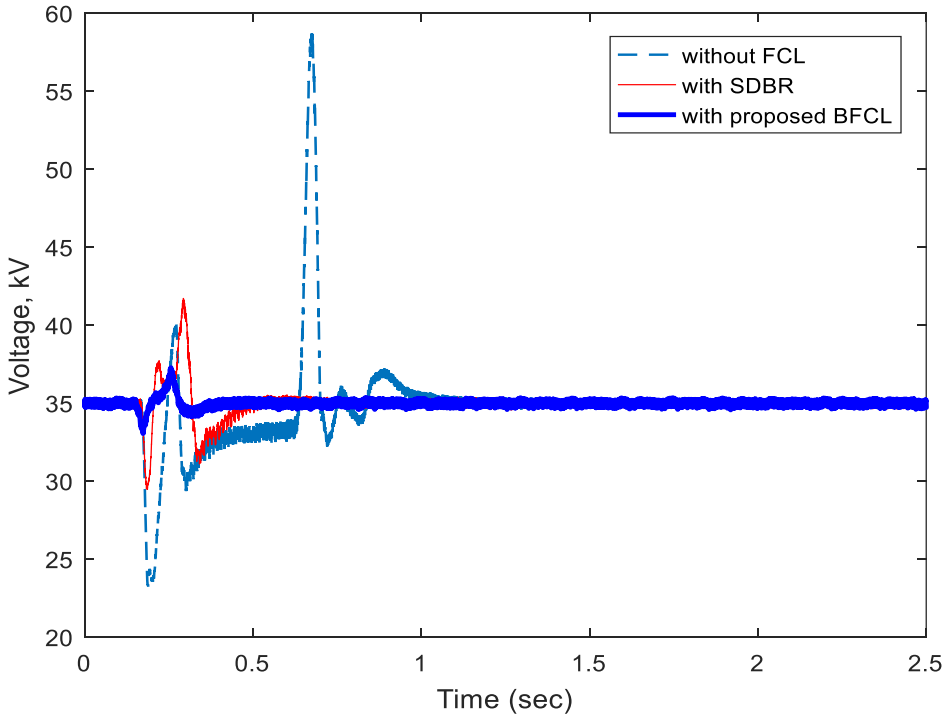

Figure 4.18 DC Link Voltage of Fixed Speed Wind Integrated VSC-HVDC

4.3.4 Single Line to Ground Faults in Grids Connected VSC-HVDC Systems.

Different types of unsymmetrical faults have been applied in grid1 for two grids connected VSC-HVDC system. Real time simulation shows positive effect to reduce DC link voltage oscillation, power oscillation and the fault current with the proposed BFCL.

Figure 4.19 shows the DC link voltage response with 1LG fault applied at grid1 for two grids connected VSC-HVDC system. Without FCL, the system has height DC link voltage overshoot. Application of SDBR reduces overshoot by 31.03%. However, a great reduction in DC link voltage overshoot is observed with the proposed BFCL which corresponds to 72.14% reduction. Moreover, settling time for DC link voltage is higher for the system without any auxiliary controller. A very slight reduction in settling time is achieved by SDBR. However, the proposed BFCL reduces settling time for the DC link voltage by 14.7%. Significant reduction in power oscillation and fault current is observed as shown in Figure 4.20 and Figure 4.21 respectively.

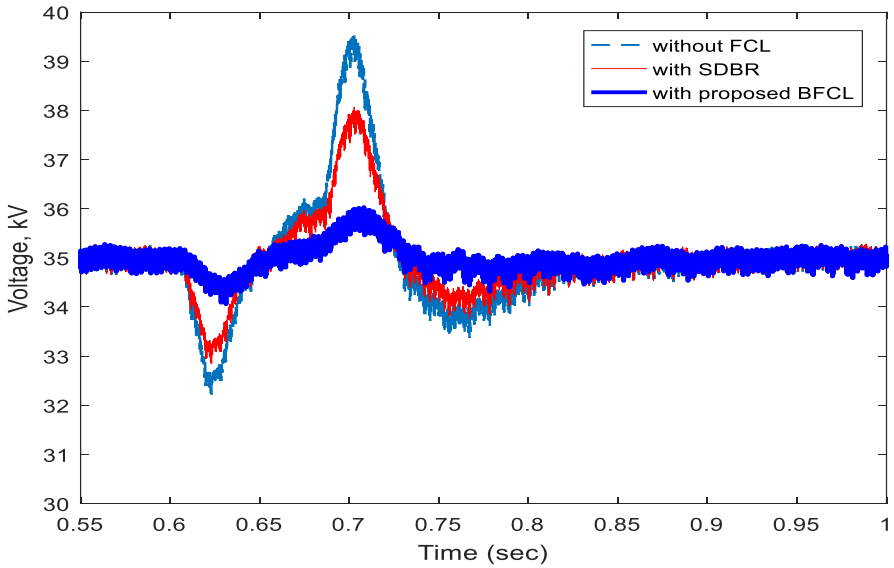

Figure 4.19 DC Link Voltage in Grids Connected VSC-HVDC for SLG Fault

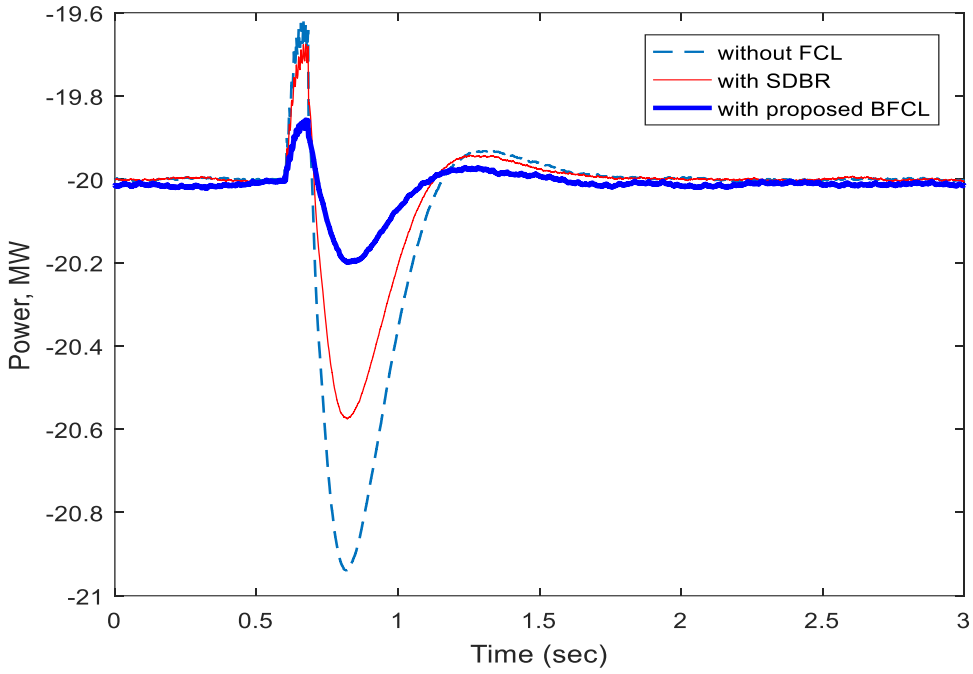

Figure 4.20 Grid1 Active Power in Grids Connected VSC-HVDC for SLG Fault

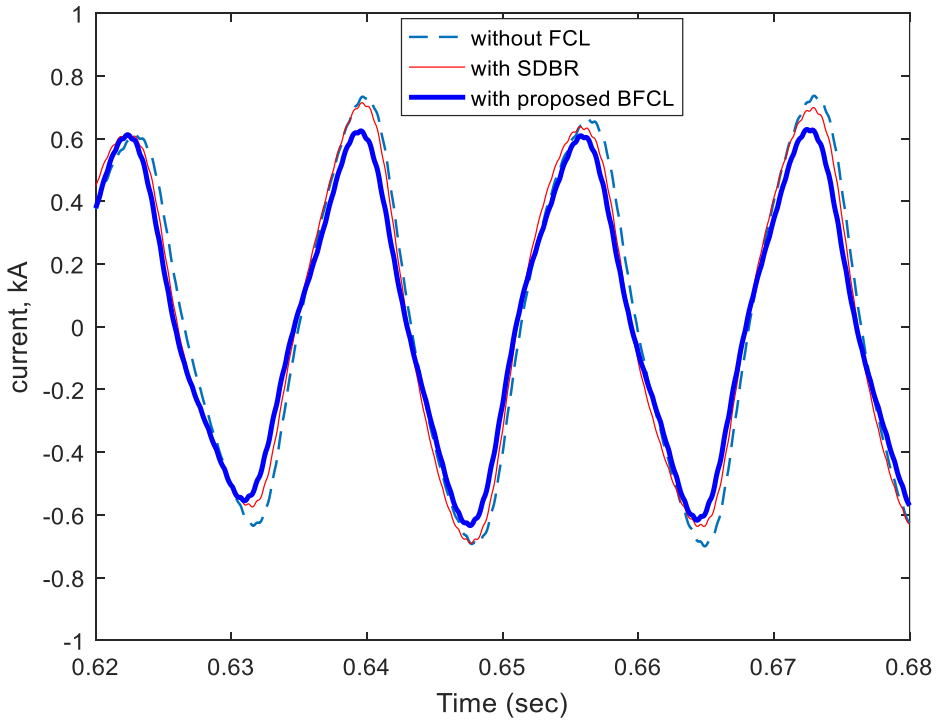

Figure 4.21 Line Current in Grids Connected VSC-HVDC for SLG Fault

4.3.5 Double Line to Ground Faults in Grids Connected VSC-HVDC Systems.

Fault current limiting capability of BFCL helps maintain DC link voltage of VSC-HVDC system as shown in Figure 4.22 for double line to ground (2LG) fault. Without FCL and with SDBR DC link voltage fluctuates widely between the range of 27 kV to 49 kV as shown in Figure **4.22**. However, voltage fluctuation is greatly reduced with the BFCL. DC link voltage lies within the range of 32 kV to 38 kV during 2LG fault at grid1. Time taken by the system to bring DC link voltage to its steady state value is 0.75 second with the proposed BFCL controller; whereas, this time is as long as 0.958 second without FCL and with SDBR. Figure 4.23 and Figure 4.24 demonstrate the capability of proposed BFCL control strategy in improving system power damping and reducing fault current during 2LG fault at grid1.

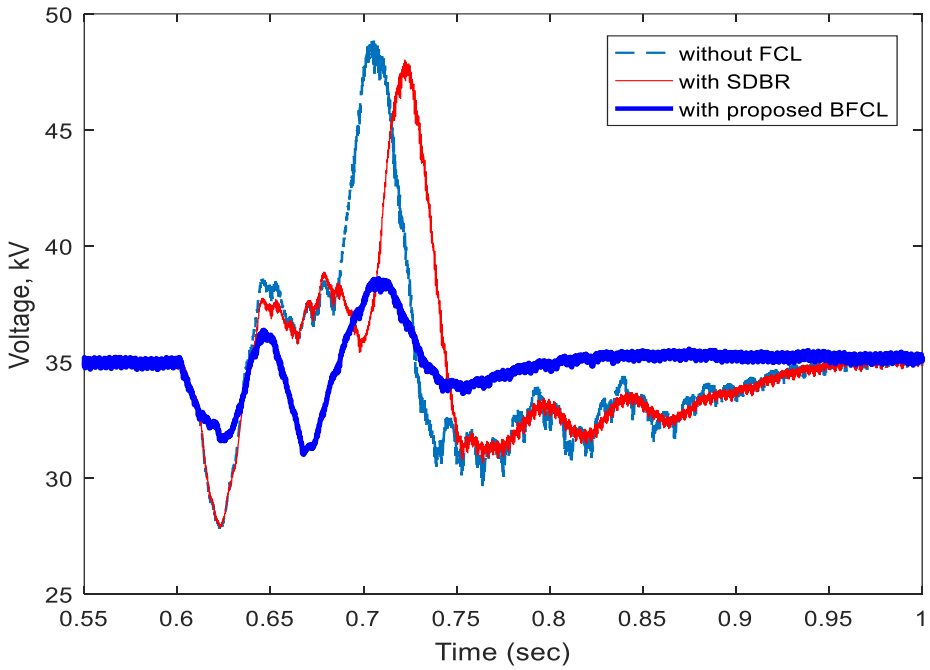

Figure 4.22 DC Link Voltage in Grids Connected VSC-HVDC for 2LG Fault

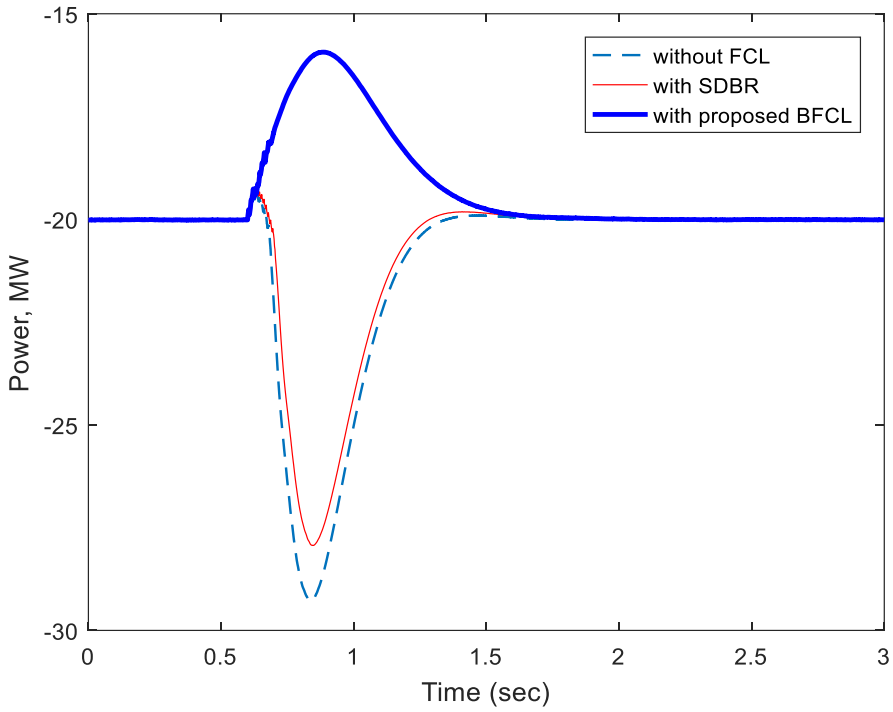

Figure 4.23 Grid1 Active Power in Grids Connected VSC-HVDC for 2LG Fault

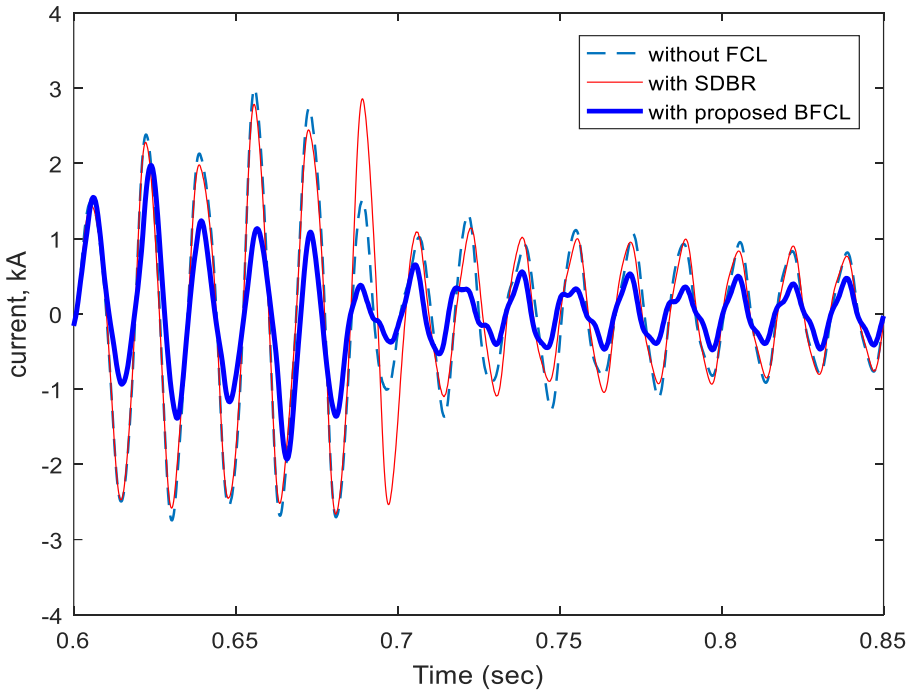

Figure 4.24 Line Current in Grids Connected VSC-HVDC for 2LG Fault

4.4 Index-Based Comparison

Besides graphical representations, index-based performance comparison is conducted to get more clear perception of VSC-HVDC systems performance improvement with proposed BFCL controller. Several performance indices are considered for example dc_{volt}, ac_{pow}, $line_{curr}$, and MAC_{speed}. Mathematical expressions for the above mentioned indices can be defined as follows:

$$DC_{volt} = \int_0^T |\Delta V_{DC}| dt \tag{4.26}$$

$$AC_{pow} = \int_0^T |\Delta P| dt \tag{4.27}$$

$$line_{curr} = \int_0^T |\Delta i| dt \tag{4.28}$$

$$MAC_{speed} = \int_0^T |\Delta N| dt \tag{4.29}$$

where ΔV_{dc}, ΔP, Δi and ΔN represent deviations of dc link voltage, active power flow, line current, and machine speed respectively.

Performance indices for symmetrical and different unsymmetrical faults are listed in the Table 4:3 to Table 4:6.

Table 4:3 Performance Index Improvement with Proposed BFCL for Symmetrical Fault (Grids Connected System)

Index parameters	**Values of indices**		
	Without FCL	**SDBR**	**Proposed BFCL**
DC_{volt}	3.1883	2.1935	0.35573
AC_{pow} [grid1]	19.2779	9.5683	0.69532
$line_{curr}$ [grid1]	1.0323	0.73188	0.22665

Table 4:4 Performance Index Improvement with Proposed BFCL for Symmetrical Fault (Wind Farm Integrated System)

	Values of indices		
Index parameters	**Without FCL**	**SDBR**	**Proposed BFCL**
DC_{volt}	1.3456	0.30726	0.16663
MAC_{speed}	2.0075	2.0069	2.0063
$line_{curr}$ [stator]	1.0242	0.94548	0.8011

Table 4:5 Performance Index Improvement with Proposed BFCL for 1LG Fault

	Values of indices		
Index parameters	**Without FCL**	**SDBR**	**Proposed BFCL**
DC_{volt}	0.21688	0.17779	0.12088
ac_{pow} [grid1]	0.11024	0.069492	0.030914
$line_{curr}$ [grid1]	0.17433	0.17193	0.16587

Table 4:6 Performance Index Improvement with Proposed BFCL for 2LG Fault

	Values of indices		
Index parameters	**Without FCL**	**SDBR**	**Proposed BFCL**
DC_{volt}	0.61458	0.57893	0.25341
ac_{pow} [grid1]	2.7937	2.2805	1.9214
$line_{curr}$ [grid1]	0.25032	0.24543	0.13371

Based on the performance indices values of DC link voltage, active power flow, line current, and machine speed listed above, it can be concluded that the proposed BFCL performance is better in two grid connected and fixed speed wind farm integrated VSC-HVDC systems during different faults.

4.5 MATLAB Simulations of the Proposed Controllers

In addition to real time digital simulation using RTDS, reference tracking performance of the proposed controllers in grid connected mode is simulated in MATLAB Simulink environment. HVDC system is built in Simulink as shown in Figure 4.25.

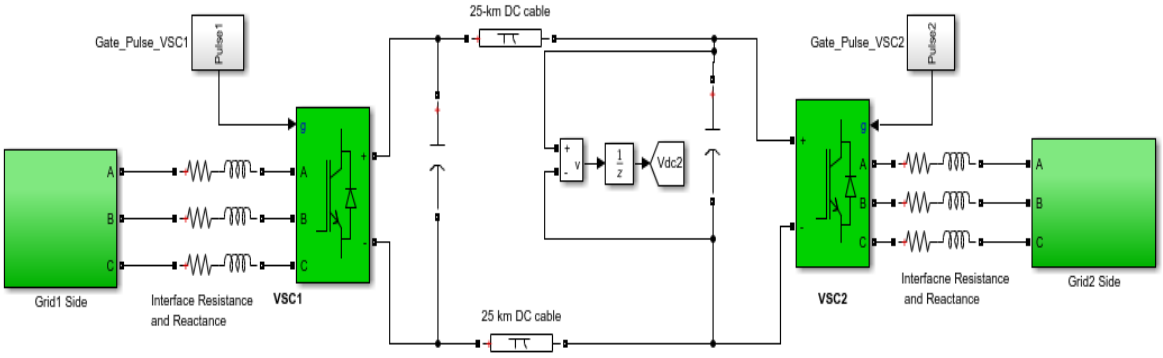

Figure 4.25 HVDC System built in MATLAB Simulink

VSC1 controller is designed to control active power exchange between two grids. Outer voltage controller loop is added for VSC2 controllers. So, VSC2 controls both DC link voltage and active power by outer DC link voltage controller and inner current controller respectively. VSC1 and VSC2 controllers are developed in MATLAB Simulink as shown in Figure 4.26.

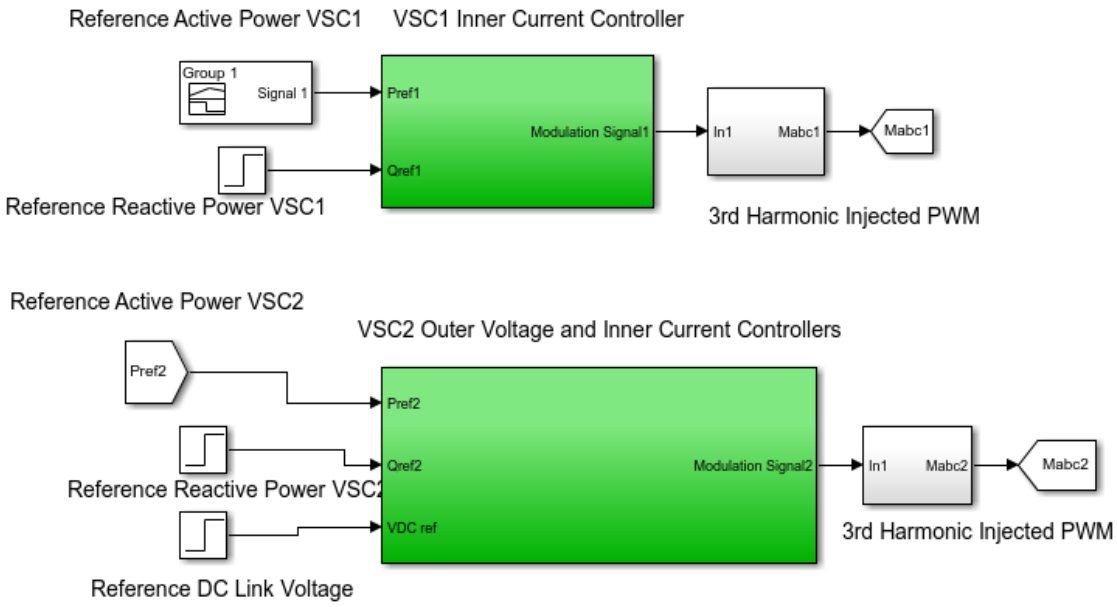

Figure 4.26 VSC1 and VSC2 controllers developed in MATLAB Simulink

During MATLAB simulation all the controllers are blocked initially. So, the DC link capacitor is initially charge through the antiparallel diode of VSC1 and VSC2. Then, DC link voltage is step changed to 35 kV. Performance of the controller in tracking reference DC link voltage is shown in Figure 4.27.

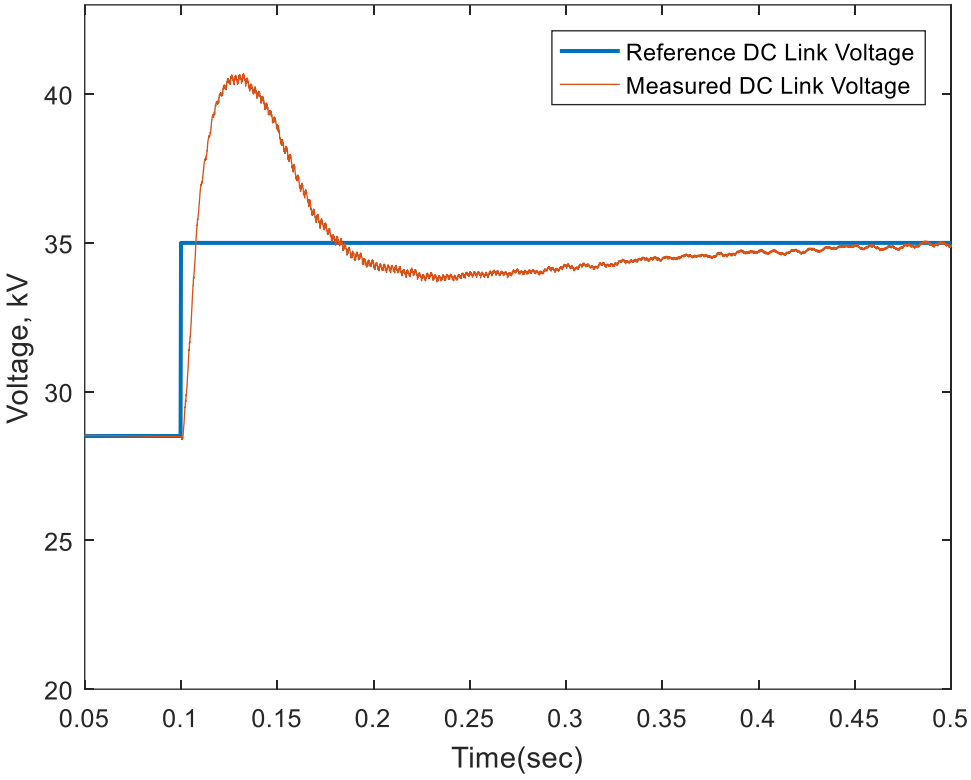

Figure 4.27 DC Link Voltage Tracking Performance of the Proposed Controllers

When DC link voltage reaches its reference steady state value, reference power for VSC1 is step changed to 20 MW to transfer this amount from grid1 to grid2. Reference power tracking performance of the controllers is visualized in Figure 4.28.

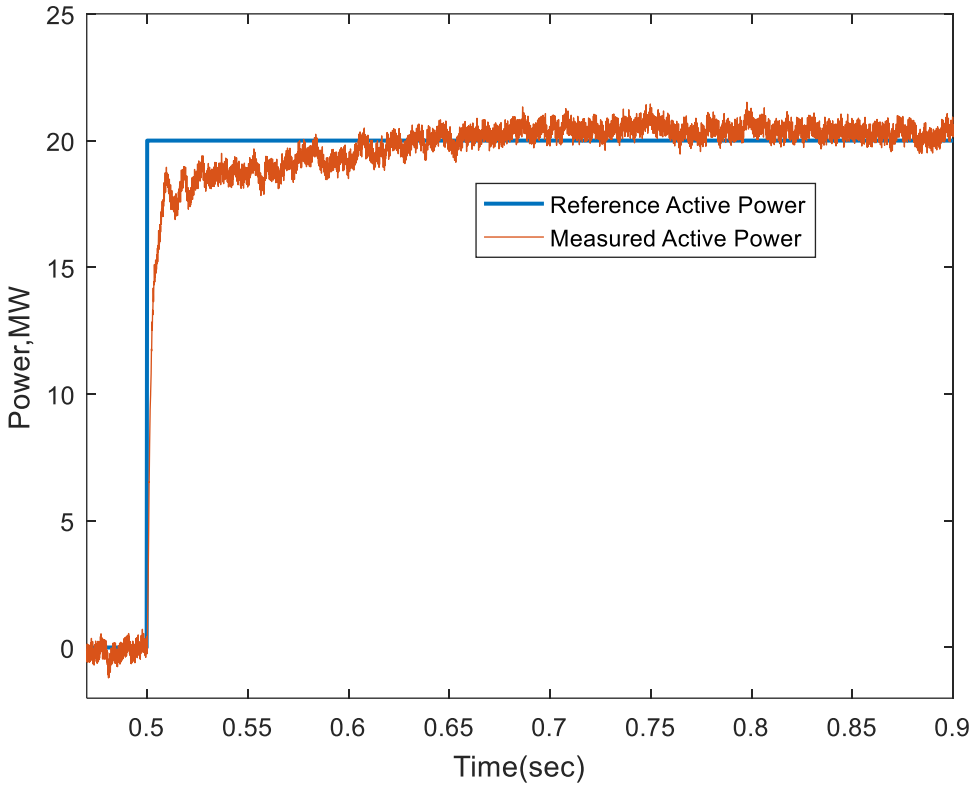

Figure 4.28 Active Power Tracking Performance of the Proposed Controllers

4.6 Conclusions

This chapter proposed BFCL-based efficient controllers to augment fault ride through capability of two grids connected and fixed speed wind farm integrated VSC-HVDC systems. Real and reactive power controllers, and DC voltage controller are designed. Real time digital simulation of HVDC plant, wind system, BFCL and their controllers are developed in RTDS. The effectiveness of the proposed BFCL is examined though the application of balanced and unbalanced faults. From real time implementation results, BFCL is found as very effective way of limiting fault current and enhancing dynamic performance of VSC-HVDC systems. The results demonstrate that the DC link voltage, power, fault current, and wind generator speed fluctuations have been substantially

reduced with the proposed BFCL and associated controllers. The results also show that the proposed BFCL based control technique outperforms SDBR in terms of response overshoots and settling times under all disturbances considered.

CHAPTER 5

FRT CAPABILITY ENHANCEMENT DFIG BASED VSC-HVDC SYSTEM WITH BFCL

5.1 Introduction

Industrialization and technological advancement have raised the increase in power demand all around the world. Due to limited reserve of fossil fuels, it is urgent to investigate alternative energy resource and to develop new methodology for harvesting energy from renewable sources. Among different renewable sources wind is fastest growing and most promising for generating electric power due to its zero fuel cost, no carbon emission, and lesser maintenance. However, wind is intermittent in nature. Integration of wind energy with variable speed wind generators requires complicated control techniques. Among different generators doubly fed induction generator (DFIG) is the best option of wind energy integration due to possibility to cover wide range of wind speed. Fault ride through (FRT) capability and transient stability are major concerns of doubly fed induction generator (DFIG) based wind energy integration with voltage source converter high voltage DC (VSC-HVDC) system. Since the stator of DFIG is directly connected to grid, it is readily affected by different types of fault at grid side. However, according to grid code requirements, wind generator should be connected and continued its operation during grid side fault. Fault current limiters (FCLs) are extensively applied in power system to suppress fault current and improve transient

stability as well as FRT capability of power system. However, their feasibility in VSC-HVDC system needs to investigate comprehensively. In this chapter, bridge type fault current limiter (BFCL) based efficient control technique is proposed to suppress fault current of DFIG based VSC-HVDC system and hence to improve transient stability as well as FRT capability.

5.2 System Modeling

For transient stability and dynamic performance analysis, DFIG wind integrated VSC-HVDC system shown in Figure **5.1** is modeled in this work. The HVDC system allows power flow from the wind farm to utility grid. For HVDC system, DC link voltage must be regulated at a predefined value. The converters used in this work are 2-level VSCs. The proposed controller of grid voltage source converter (GVSC) regulates the DC bus voltage. The power transfer between the wind farm and grid must be equal (excluding converter loss) to keep the power exchange with the DC bus capacitor at zero. The system components are modeled as follows.

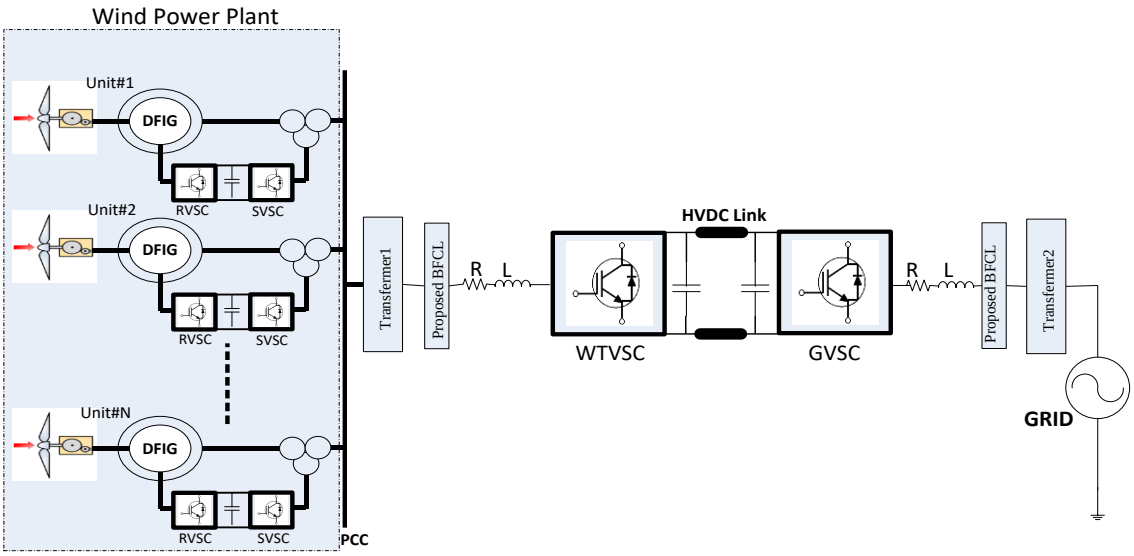

Figure 5.1 Schematic Diagram of DFIG Wind Integrated VSC-HVDC System

5.2.1 Wind Turbine Modeling

Generally, operating principle of wind turbine is characterized by its mechanical power [202,203]. Analytical expression for mechanical power is given by eq. (4.3) as presented in chapter 4.

Where ρ is air mass density in kg/m^3, A is turbine swept area= πr^2 , r is turbine radius, V_w is turbine speed in m/s, C_p The performance coefficient, β is blade pitch angle, and λ is tip speed ratio.

Tip speed ratio is given by the following equation.

$$\lambda = \frac{r\omega_{tur}}{V_w} \tag{5.1}$$

Where ω_{tur} is the turbine angular speed in rad/s. Power delivered by the wind turbine (P_{tur}) can be controlled by varying performance coefficient. Variation of C_p is achieved by varying ω_{tur} and β since wind speed V_w can not be controlled.

5.2.2 Doubly Fed Induction Generator (DFIG) Modeling

Wind energy is extracted and integrated to the grid with doubly fed induction generator which is basically three phase wound-rotor induction machine. The wind-power system utilizes wind turbine which is mechanically coupled through a gearbox to the DFIG. Stator side of DFIG is directly connected to the point of common coupling (PCC) as shown in Figure **5.1**. Rotor of the machine is connected to the PCC with AC/DC/AC conversion system with voltage source converters (VSCs). Common DC bus of the VSCs contains a capacitor. Rotor voltage in *d-q* frame is given as [204].

$$V_{dr} = R_r i_{dr} + \sigma L_r \frac{di_{dr}}{dt} - \omega_{slip}(\sigma L_r i_{qr}) \quad (5.2)$$

$$V_{qr} = R_r i_{qr} + \sigma L_r \frac{di_{qr}}{dt} + \omega_{slip}(\sigma L_r i_{dr} + L_m i_{ms}) \quad (5.3)$$

where mutual inductance, $L_m = \frac{(L_o)^2}{L_s}$; leakage factor, $\sigma = 1 - \frac{(L_o)^2}{L_r L_s}$; R_r is the rotor resistance; L_r is the rotor inductance; L_s is the stator inductance; L_o is the magnetizing inductance, ω_{slip} is the slip frequency which is the difference between stator and rotor frequency.

The main reason of using DFIG for harnessing wind energy is that it has better performance in variable speed wind system. Another advantage of DFIG is that only small amount of power usually 25 to 40% of the machine rated power is controlled by converters. So, the power loss is relatively low in the converters compared to the cases where converters have to exchange whole amount of power.

5.3 Controller Design

The following subsections describe stator voltage source converter (SVSC), rotor voltage source converter (RVSC), wind turbine voltage source converter (WTVSC), and grid voltage source converter (GVSC) controllers design process in details.

5.3.1 Control of Stator Voltage Source Converter (SVSC)

Stator side converter consists of a 2-level, 6 pulses AC/DC VSC whose AC side is connected to PCC and DC side is connected to a capacitor. To design control strategy for SVSC simplified diagram as shown in Figure **5.2** is considered.

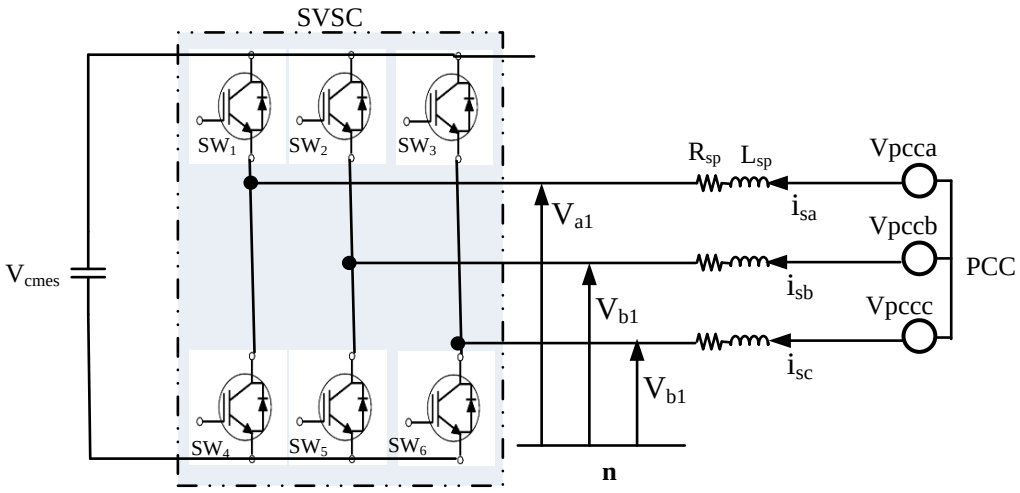

Figure 5.2 Simplified Diagram of SVSC with PCC

To develop control strategy for SVSC, it is first useful to write the equations for the voltages across the series resistors and reactors. So, we get following differential equations.

$$V_{pcca} = i_{sa}R_{sp} + L\frac{di_{sa}}{dt} + V_{a1} \tag{5.4}$$

$$V_{pccb} = i_{sb}R_{sp} + L\frac{di_{sb}}{dt} + V_{b1} \tag{5.5}$$

$$V_{pccc} = i_{sc}R_{sp} + L\frac{di_{sc}}{dt} + V_{c1} \tag{5.6}$$

Using *abc* to *dq* transformation, we have following two equations in a rotating reference frame.

$$V_{pccd} = i_{sd}R_{sp} + L\frac{di_{sd}}{dt} - \omega_0 L i_{sq} + V_{d1} \tag{5.7}$$

$$V_{pccq} = i_{sq}R_{sp} + L\frac{di_{sq}}{dt} - \omega_0 L i_{sq} + V_{q1} \tag{5.8}$$

From the above set of equations, SVSC controller as shown in Figure **5.3** is developed. SVSC has two control loops: outer control loop which maintains a constant DC link voltage and inner current control loop to control the active and reactive powers.

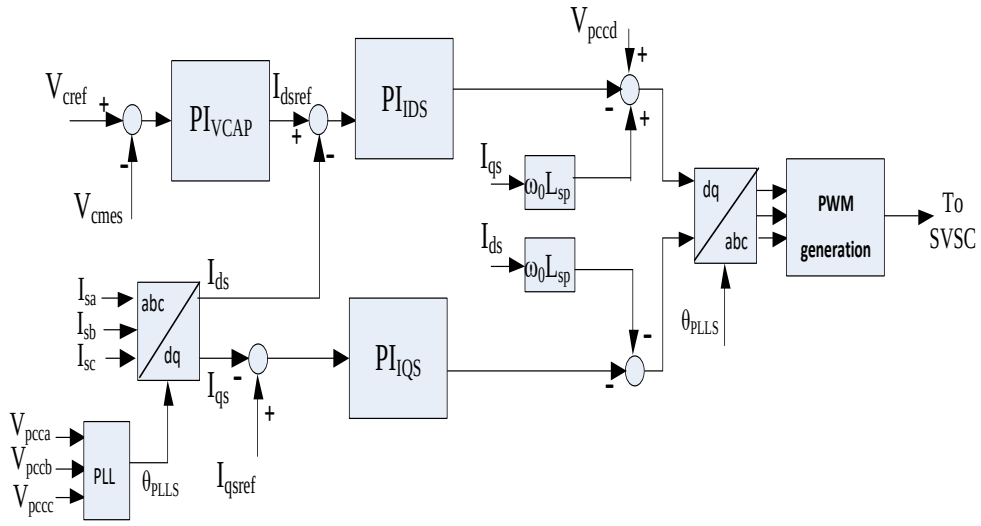

Figure 5.3 Schematic Diagram of Controller of SVSC

Measured DC link voltage (V_{cmes}) is compared with reference voltage (V_{cref}) and the error is processed by PI regulator. The output of PI regulator provides reference direct axis current (I_{dsref}) to inner current controller. The measured three phase stator current is converted to *d-q* components using Park's transformation and compared with corresponding reference currents and then processed by inner PI current regulators. Output of the inner PI controllers is added with decoupling terms ($I_{qs}\omega_0 L_{sp}$ and $I_{ds}\omega_0 L_{sp}$) in which L_{sp} is the reactance between SVSC terminal and PCC.

5.3.2 Control of Rotor Voltage Source Converter (RVSC)

The following RVSC controller is developed in *d-q* frame to control the active and reactive powers with corresponding *d*-axis and *q*-axis current components respectively as shown in Figure **5.4**. The base equations and symbol descriptions for the following controller are given in section 5.2.2.

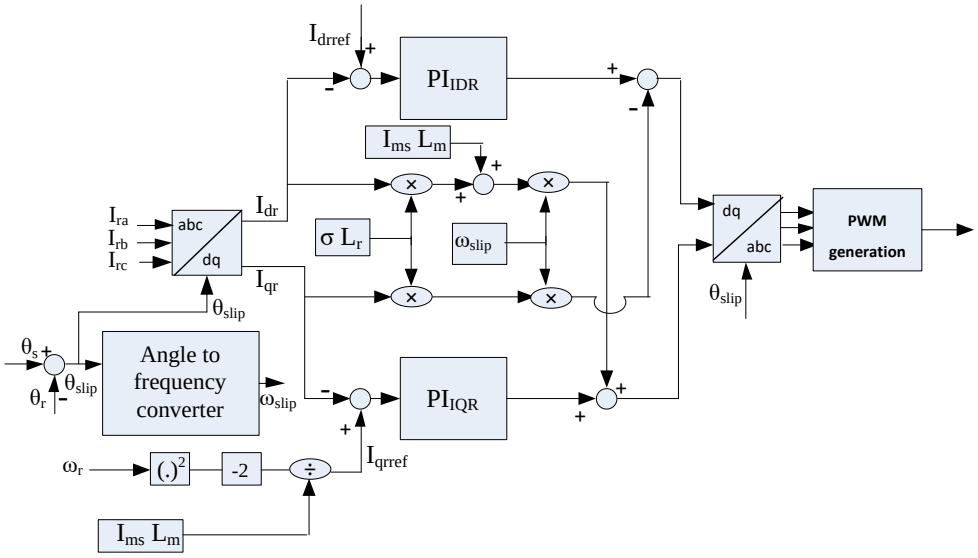

Figure 5.4 Schematic Diagram of Controller of RVSC

Figure **5.4** depicts that the measured three phase rotor current is converted to *d-q* components with a rotating reference frame (θ_{slip}) which is computed from the difference between the position of the stator flux (θ_s) and rotor flux (θ_r) vector. Reactive reference rotor current (I_{qrref}) is provided by the optimal power point tracker as shown in the above schematic diagram.

5.3.3 Control of Wind Turbine Voltage Source Converter (WTVSC)

Wind turbine voltage source converter (WTVSC) is controlled to regulate active power exchange between wind farm and DC link. Current control model controller is developed where active power is controlled by direct axis current and reactive power is controlled by quadrature axis current. PI controllers are employed in both direct and quadrature axis current regulators.

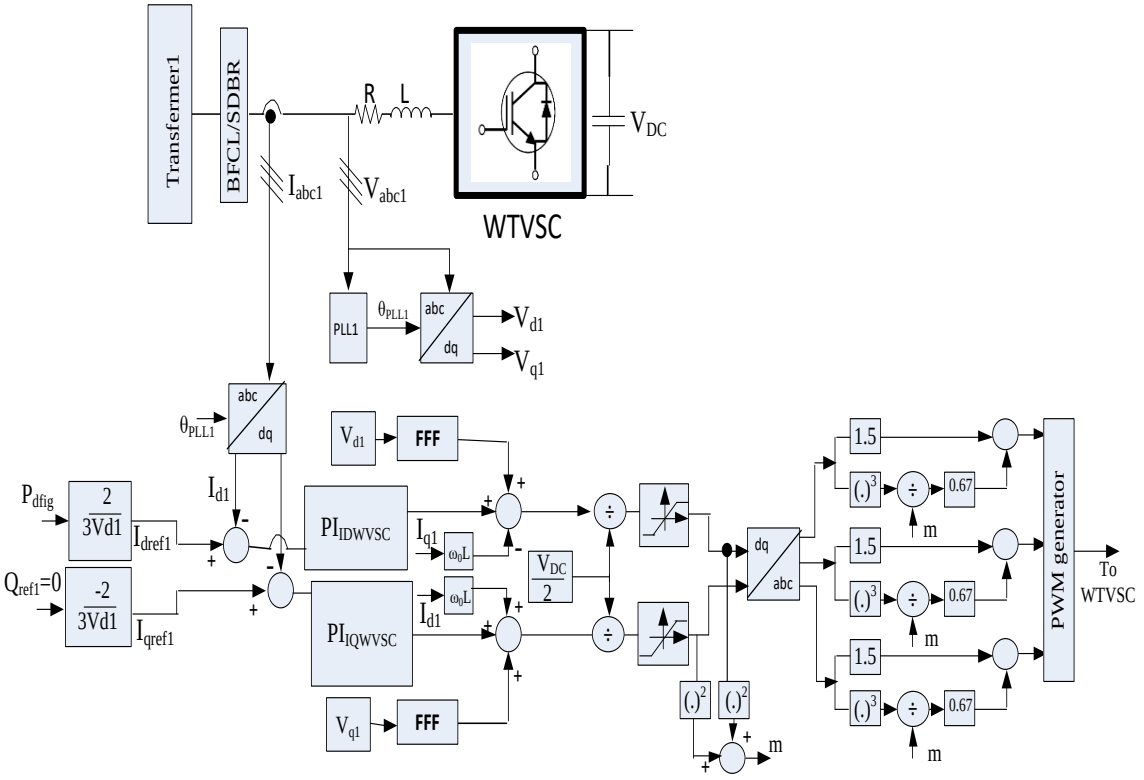

Figure 5.5 Schematic Diagram of Controller of WTVSC

As shown in Figure **5.5**, the active and reactive powers are controlled by inner current controller with corresponding direct and quadrature current respectively. PI controllers are used for both direct axis and quadrature axis currents. Undesirable start-up transient is avoided by augmenting the control scheme with a feed forward filter (FFF) as represented in Figure **5.5**. Third harmonic injected PWM technique is used as the required minimum DC bus voltage level is lower than classical PWM generation which, in turn, increases system stability in worst case scenario [197]. In the third harmonic injected PWM technique, square of *d*-axis and *q*-axis signals are added together to generate the modulating signal (*m*).

5.3.4 Control of Grid Voltage Source Converter (WTVSC)

The WTVSC controller is developed to perform two control actions: control of active power exchange between DC link and AC grid and control of DC link voltage. Outer controlled is employed to control DC link voltage and inner control is developed to control active power by current control mode. Overall control diagram is shown in Figure **5.6** below.

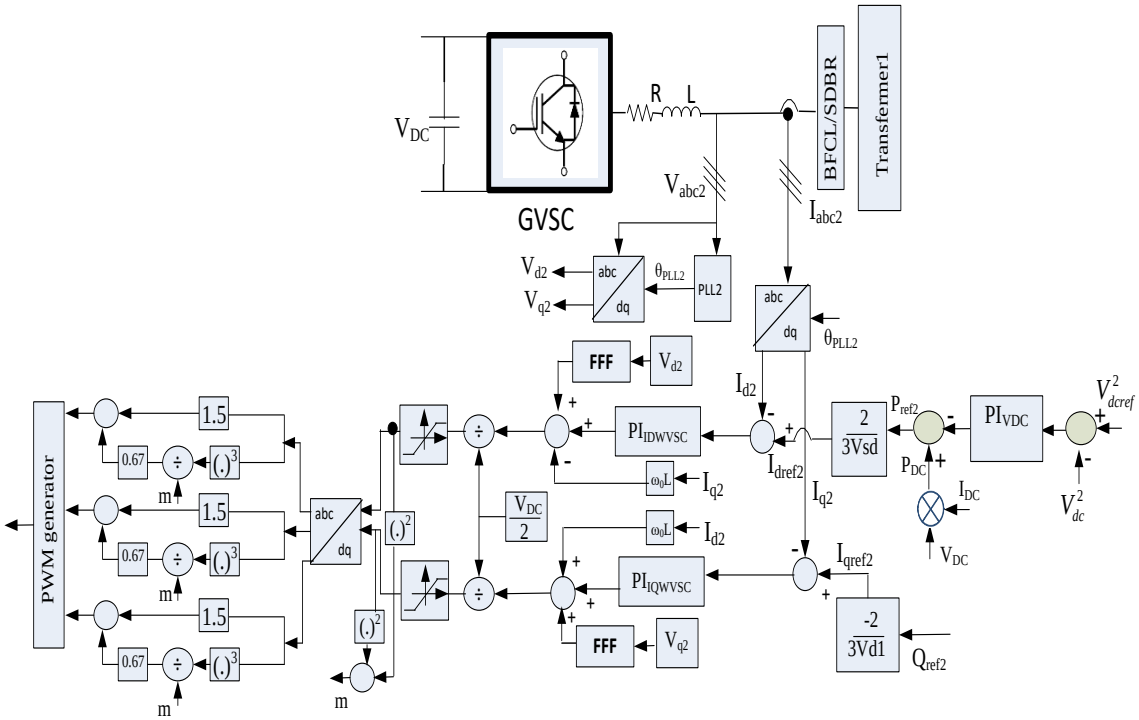

Figure 5.6 Schematic Diagram of WTVSC Controller

In outer voltage controller, error between square of measured DC voltage and reference DC voltage is processed by proportional integral (PI) controller. Power exchange between DC link and grid (P_{DC}) is added with PI controller output to generate reference active power (P_{ref2}) for VSC2 as shown in Figure **5.6**. Then, *d*-axis reference current is generated and processed by inner current control loop.

5.4 Results and Discussions

5.4.1 System and Controller Data

DFIG wind integrated VSC-HVDC with BFCL system as shown in Figure **5.4** is considered in this work to validate the proposed control strategies. Several DFIG units are connected at the point of common coupling (PCC). The proposed fault current limiting device, BFCL, is connected with both wind power plant and grid sides of the system considered. Detailed DFIG data are listed Table **5**:**1**.

Table 5:1 DFIG Wind System Parameters

Parameter	Value
Power rating	2 MW
Machine pole	6
Nominal speed	2225 RPM
Stator voltage	0.69 kV
Stator resistance	0.001 Ω
Rotor resistance	0.0013 Ω
Stator reactance	0.0022 Ω
Magnetizing reactance	0.941 Ω
Rotor reactance	0.024 Ω
Rotor/stator turn ratio	2.6377

Pole zero cancellation technique is used to tune the parameters of the inner current controllers. In addition, the symmetrical optimum method is used for parameters tuning of outer voltage controllers. Controller parameters obtained are listed in Table **5**:**2** for all PI controllers.

Table 5:2 Parameters of PI Controllers

Name	K_p	K_i
PI_{IDS}	0.3	10
PI_{IQS}	0.3	10
PI_{IDR}	1.387	35.6
PI_{IQR}	1.387	35.6
PI_{IDWVSC}	8.5	88
PI_{IQWVSC}	8.5	88
PI_{VDC}	0.1036	17.77

5.4.2 RTDS Implementation

This section presents detailed results by RTDS implementation of DFIG and HVDC plants and their controllers. The results are presented and compared in the following subsections for different faults. Initially, the system operates in its normal condition. Then symmetrical three-line-to-ground (3LG) and unsymmetrical single-line-to-ground (1LG) faults are applied at point of common coupling separately. The duration of these faults is 6 cycles. Under each fault, three different simulation conditions are tested to show the effectiveness of the proposed BFCL control technique. These conditions are:

i) without FCL;

ii) with SDBR;

iii) with proposed BFCL.

Case A: Symmetrical Fault Application

Initially, DC capacitors are discharged by disconnecting HVDC system where pulses of all the VSCs are blocked and all controllers are inactive. Then, HVDC system is connected to the grid through the transformer and BFCL. As a result, capacitors gradually

get charges to through the antiparallel diodes of GVSC. Afterwards, DC link voltage is regulated at 35 kV by unblocking gating pulses of GVSC. Now, the effectiveness of the proposed control strategy in capturing power from varying wind speed is tested. Total power delivery from the DFIG system is around 30 MW for nominal wind speed of 15 m/s. Wind speed is step changed from 15 m/s to 18 m/s and DFIG power delivery for this wind speed variation is plotted in Figure **5.7**.

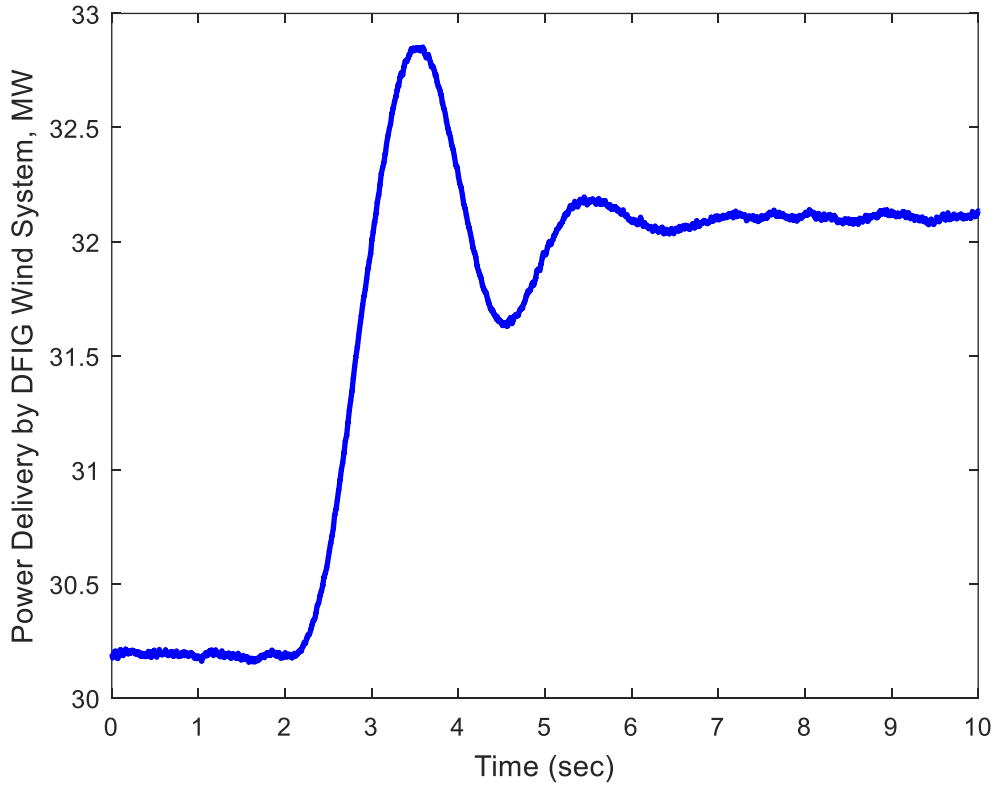

Figure 5.7 DFIG Power Variation for Wind Speed Variation (15m/s to 18m/s)

DC link voltage, line active power, line current, stator current, rotor current, and DFIG speed are presented and compared for both cases of SDBR and proposed BFCL for symmetrical fault as presented below.

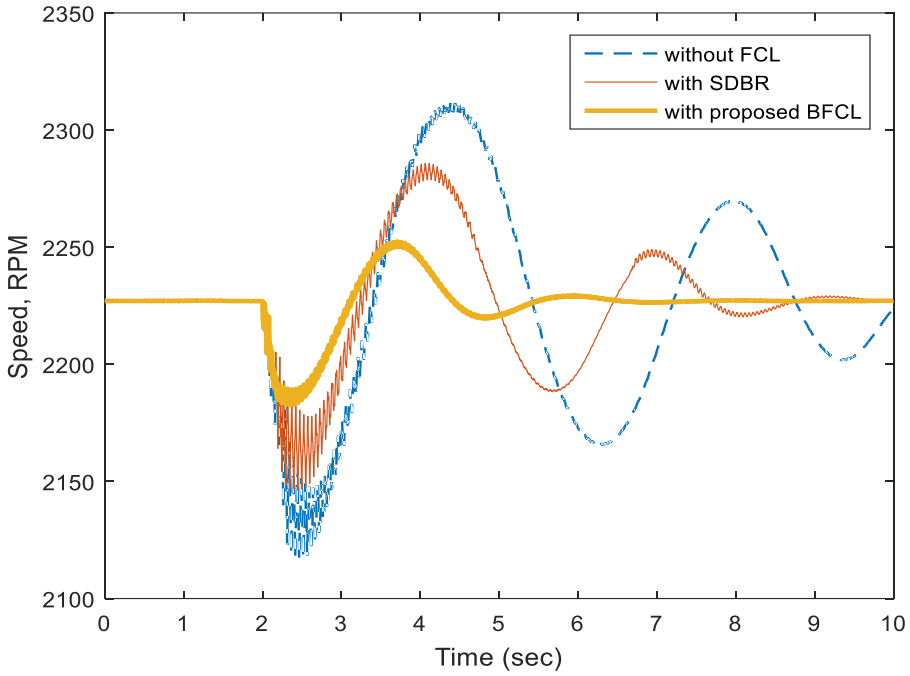

Figure 5.8 Improvement in DFIG Speed Response with Proposed BFCL Strategy

Figure **5.8** shows that the speed of DFIG fluctuates between 2120 RPM to 2310 RPM without any auxiliary controller. Although this fluctuation is damped one, it has detrimental effect on machine performance. Now, system performance improvement is observed by 40% speed fluctuation reduction with SDBR. However, DFIG speed oscillation is greatly damped with proposed BFCL controller by a fluctuation reduction of 65%. Moreover, DFIG speed reaches to its steady state value at 5.8 seconds whereas it takes 9.5 seconds with SDBR. Without a controller, DFIG speed oscillates during the entire simulation period. In addition, the effectiveness of the proposed BFCL solution has been clearly visualized from Figure **5.9** to Figure **5.11** for 3LG fault at PCC as the DFIG power oscillations, stator fault current, and DC link voltage fluctuations have been greatly reduced.

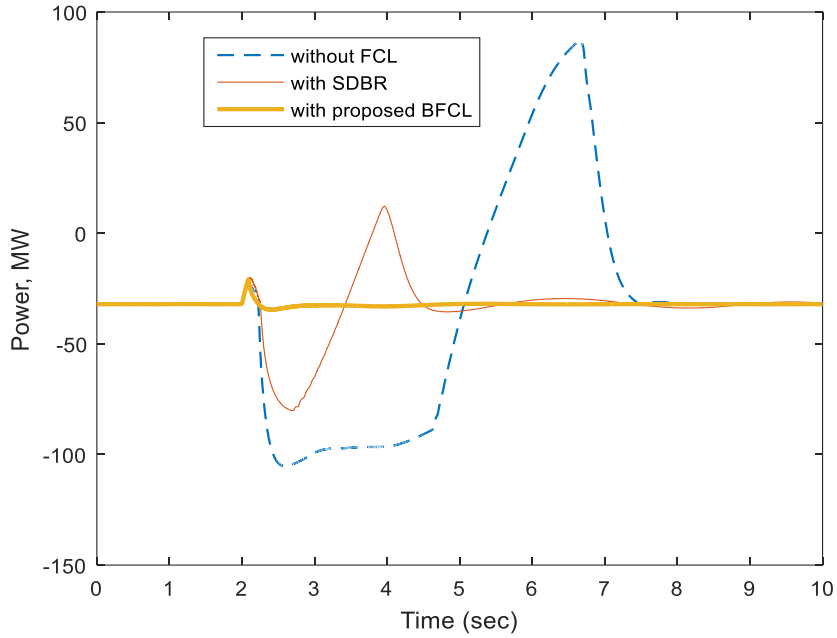

Figure 5.9 Improvement in Wind Farm Active Power Response with Proposed BFCL Strategy

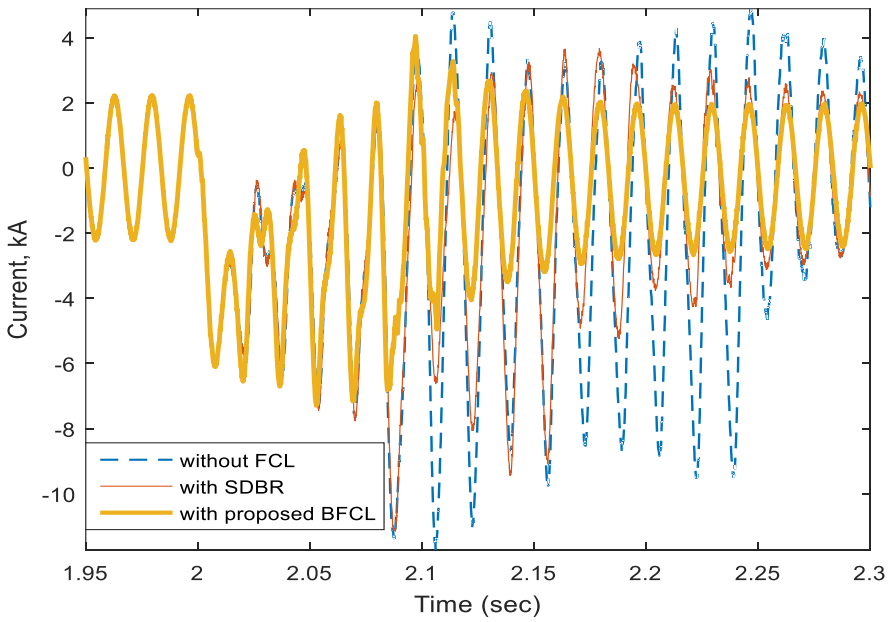

Figure 5.10 Improvement in DFIG Stator Current Response with Proposed BFCL Strategy

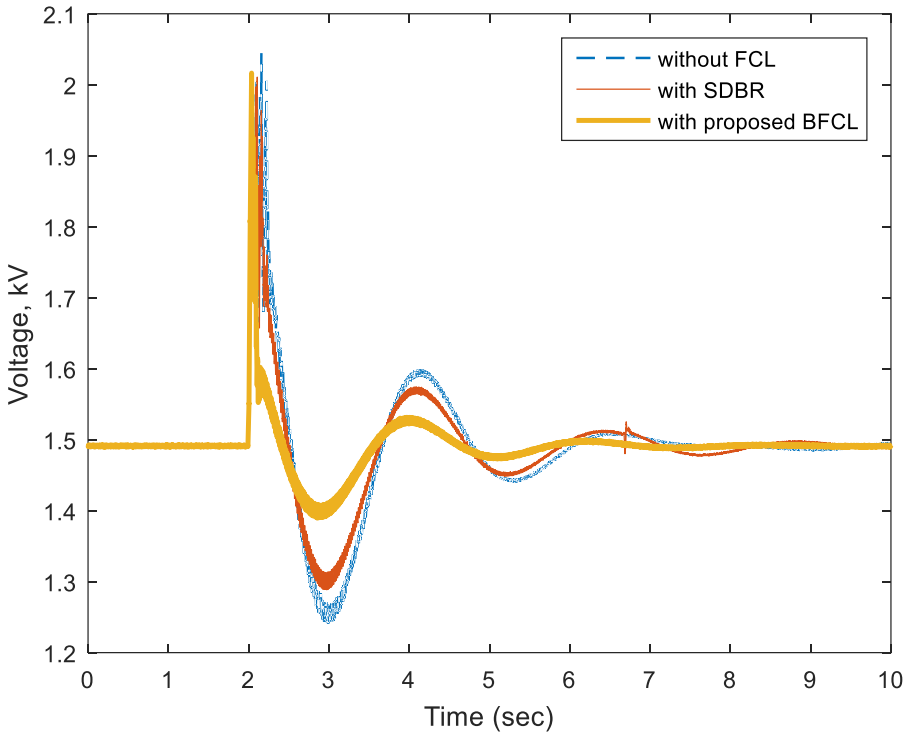

Figure 5.11 Improvement in Wind Farm DC Link Voltage Response with Proposed BFCL Strategy

Improvement in HVDC system response with the proposed BFCL has been also observed. Under the fault condition, the DC link voltage is shown in Figure **5.12**. Figure **5.12** shows that the DC link voltage of HVDC is oscillating over the entire simulation period. SDBR based controller reduces voltage fluctuation by 26.6% while the fluctuation has been reduced greatly with the proposed BFCL based controller by 41.6% as observed in the Figure **5.12**. Reduction in grid power oscillation and fault current has been shown in Figure **5.13** and Figure **5.14** respectively where the superiority of the proposed BFCL controller is evident.

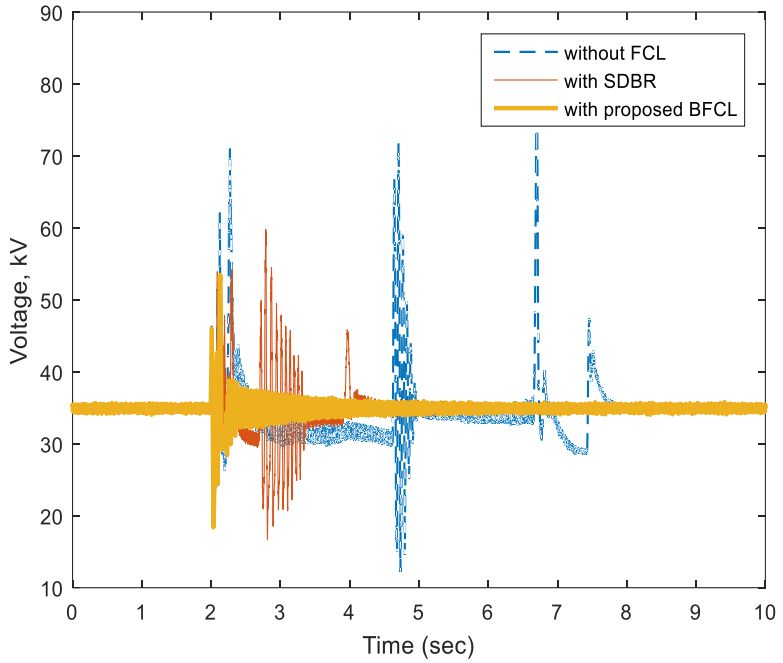

Figure 5.12 Improvement in HVDC DC Link Voltage Response with Proposed BFCL Strategy

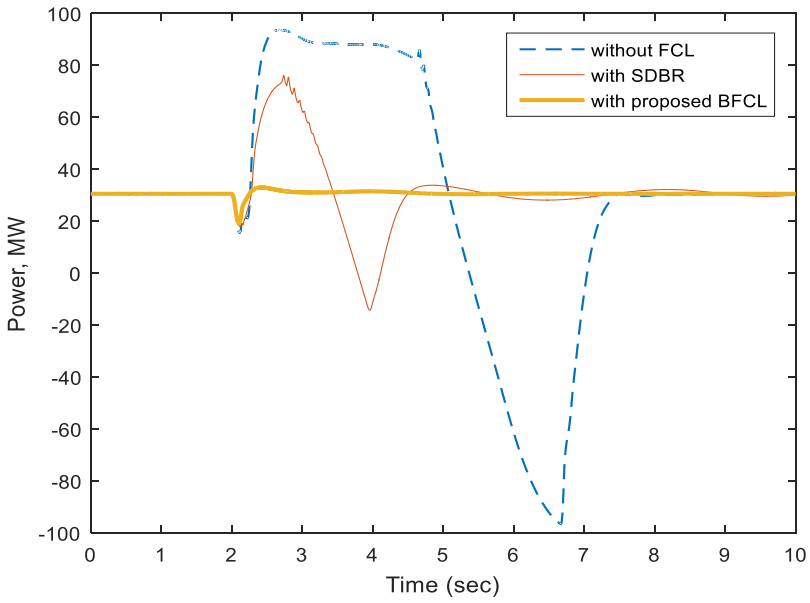

Figure 5.13 Improvement in Grid Active Power Response with Proposed BFCL Strategy

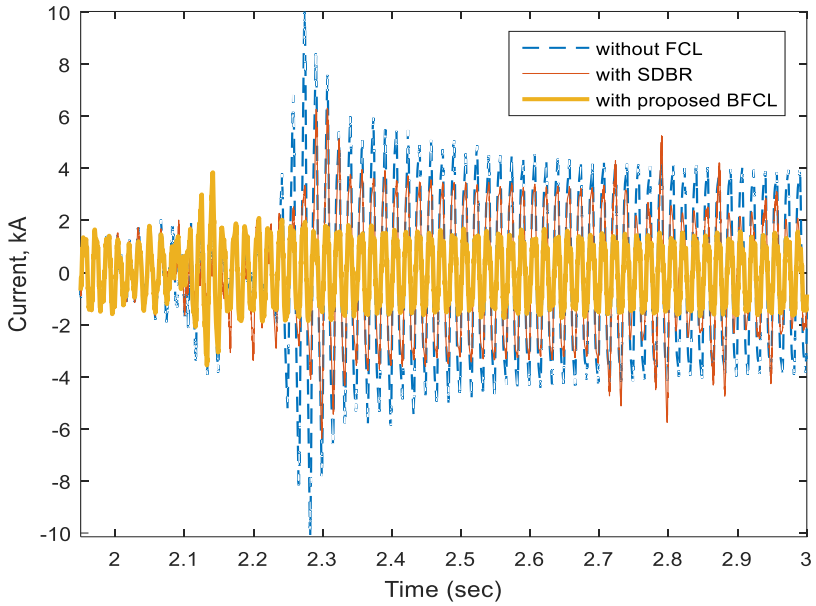

Figure 5.14 Improvement in Grid Current Response with Proposed BFCL Strategy

Case B: Unsymmetrical Fault Application

Unsymmetrical single-line-to-ground (1LG) fault has been applied at PCC. Real time simulation in Figure **5.15** shows clearly the positive effect of the proposed BFCL to reduce DFIG speed fluctuation. Without FCL, DFIG oscillates over a wide range and it does not reach to the steady state value within the entire simulation period. System performance is slightly improved with SDBR. However, the proposed BFCL controller greatly improves the system dynamic performance by keeping the DFIG speed within a narrow range during the fault. Time taken by DFIG speed to reach its reference value is also small for the proposed BFCL compared to without FCL and with SDBR cases. Significant reduction in power oscillation, fault current, and capacitor voltage fluctuation is observed as shown from Figure **5.16** to Figure **5.18**.

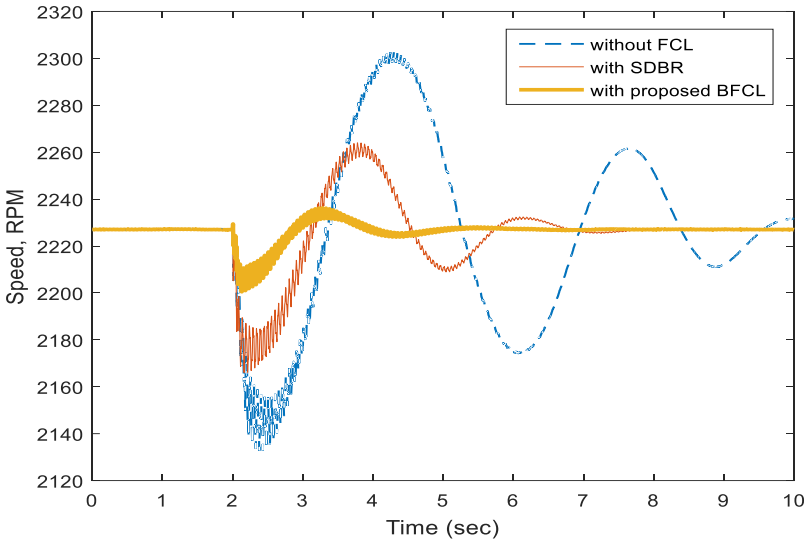

Figure 5.15 Improvement in DFIG Speed Response with Proposed BFCL Strategy for Unsymmetrical Fault

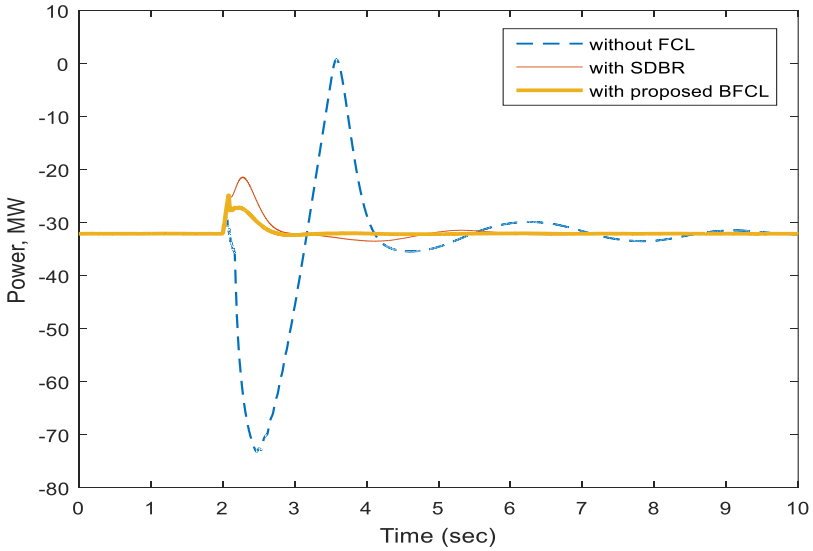

Figure 5.16 Improvement in Wind Farm Active Power Response with Proposed BFCL Strategy for Unsymmetrical Fault

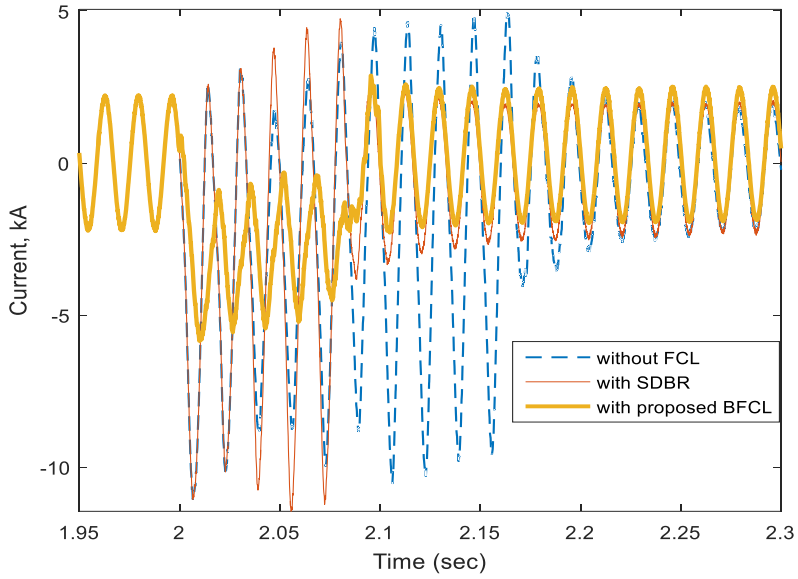

Figure 5.17 Improvement in DFIG Stator Current Response with Proposed BFCL Strategy for Unsymmetrical Fault

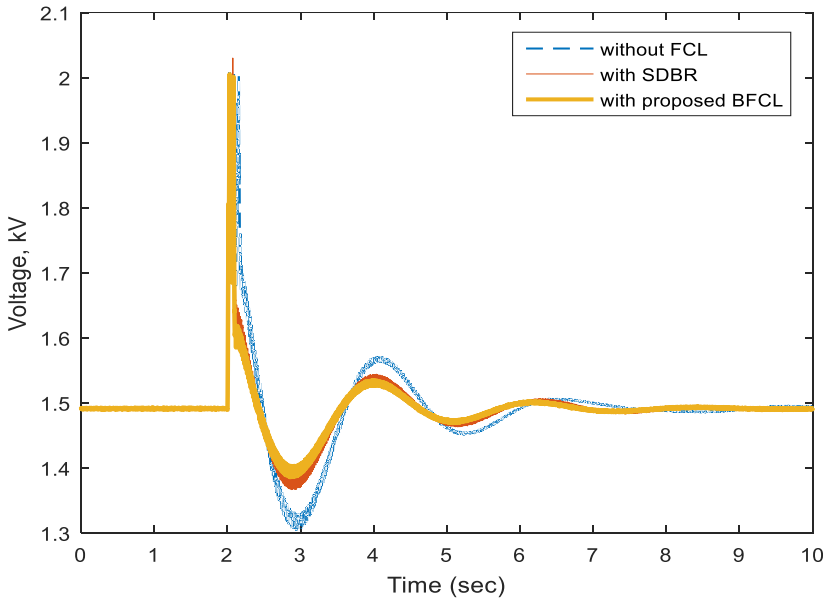

Figure 5.18 Improvement in Wind Farm DC Link Voltage Response with Proposed BFCL Strategy for Unsymmetrical Fault

Fault ride through capability of HVDC with proposed BFCL is shown Figure **5.19**. Without any fault current limiter, DC link voltage of HVDC fluctuates over a wide range. With the application of SDBR, DC link voltage fluctuation is reduced by 17.5%. Throughout the entire simulation period, proposed BFCL keeps DC link voltage within

the permissible limit compared to SDBR and without auxiliary controller. Active power oscillation damping and fault current reduction capability of the proposed BFCL based control strategy are shown in Figure **5.20** and Figure **5.21** respectively.

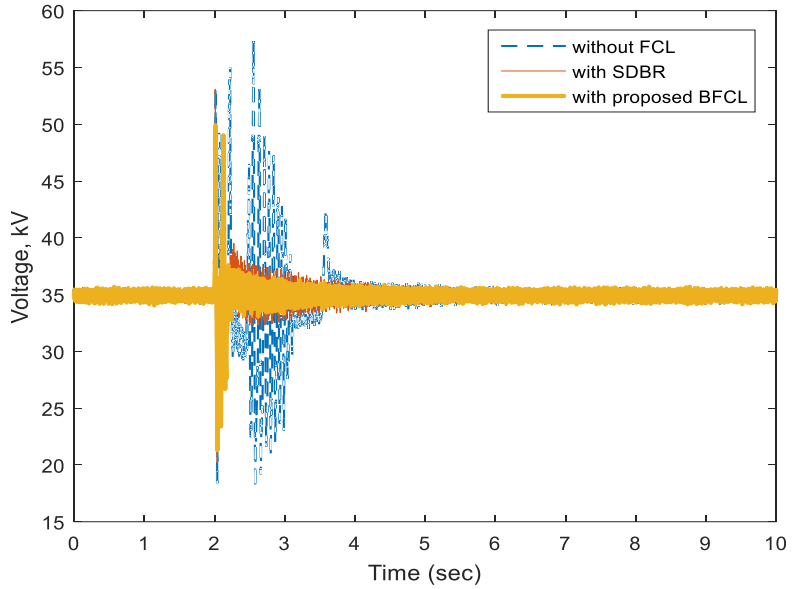

Figure 5.19 Improvement in HVDC DC Link Voltage Response with Proposed BFCL Strategy for Unsymmetrical Fault

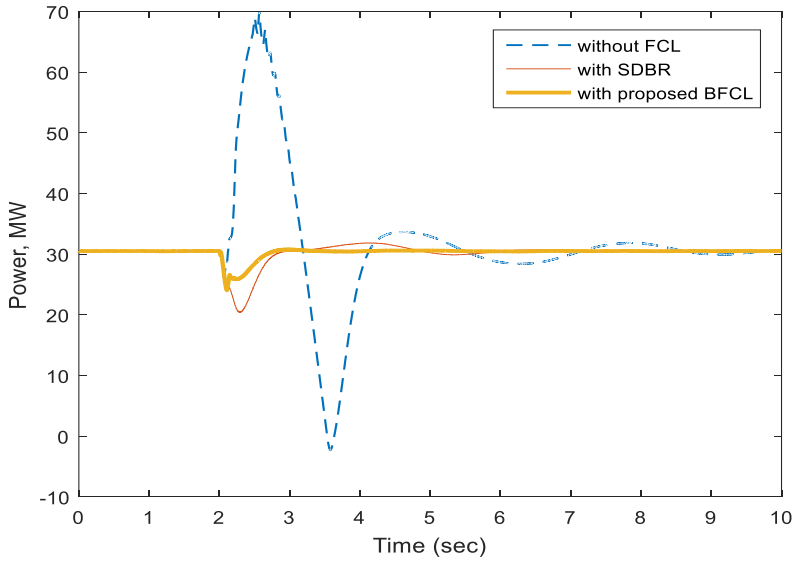

Figure 5.20 Improvement in Grid Active Power Response with Proposed BFCL Strategy for Unsymmetrical Fault

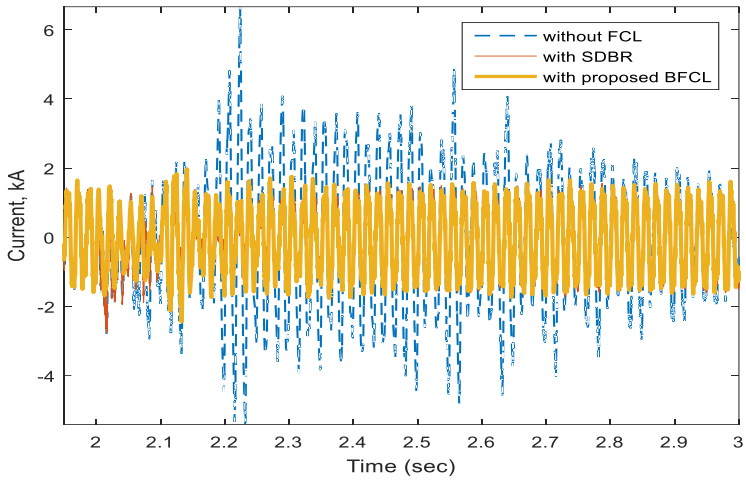

Figure 5.21 Improvement in Grid Current Response with Proposed BFCL Strategy for Unsymmetrical Fault

Case C: Index-Based Comparison

To get more clear perception of fault ride through capability enhancement similar indices as presented in chapter 4 are calculated for several parameters of the system. Performance indices values are presented in the following tables.

Performance indices for symmetrical and unsymmetrical faults are listed in the Table 5:**3** and

Table 5:**4** respectively.

Table 5:3 Performance Index Improvement with Proposed BFCL for Symmetrical 3LG Fault

Index Parameters	Without FCL	SDBR	Proposed BFCL
MAC_{speed}	80.8175	42.3763	14.2806
DC_{volt} [DFIG]	0.068902	0.05728	0.026487
DC_{volt} [HVDC]	3.586	1.7927	0.68626
AC_{pow} [DFIG]	52.1791	11.119	0.6223
AC_{pow} [GRID]	49.975	10.4877	1.0446
$line_{curr}$ [Stator]	0.73031	0.68826	0.63546

$line_{curr}$ [Grid]	1.3788	0.55428	0.38678

Table 5:4 Performance Index Improvement with Proposed BFCL for Unsymmetrical 1LG Fault

Index Parameters	Without FCL	SDBR	Proposed BFCL
MAC_{speed}	66.561	21.6401	4.9367
DC_{volt} [DFIG]	0.052067	0.035011	0.02854
DC_{volt} [HVDC]	1.5677	0.56259	0.46095
AC_{pow} [DFIG]	8.0379	1.1163	0.43776
AC_{pow} [GRID]	7.6162	1.2649	0.76578
$line_{curr}$ [Stator]	0.73031	0.68826	0.63546
$line_{curr}$ [Grid]	1.3788	0.55428	0.38678

The results in Tables 5.3 and 5.4 show that the deviations in all indices considered are much smaller with the proposed BFCL based control strategy. It can be concluded that the performance of DFIG wind integrated VSC-HVDC system is substantially improved with the proposed BFCL.

5.5 Conclusions

This chapter proposed an efficient control strategy for DFIG wind integrated VSC-HVDC system with bridge type fault current limiter to limit fault current as well as augment fault ride through capability. Depending on fault detection based on PCC voltage, BFCL controller is designed to insert resistance and inductance during system contingencies in order to limit fault current. Stator VSC and rotor VSC controllers are proposed to control DC link capacitor voltage and power respectively. VSC-HVDC transmission system controllers are developed based on current control mode to transfer active power from wind power plant to grid. Real time digital simulation of wind turbine,

DFIG, HVDC plant, BFCL and their controllers has been developed in RTDS. The effectiveness of the proposed control strategy is examined through the application of symmetrical as well as different unsymmetrical faults. From real time implementation results, BFCL control strategy is found as very effective way of limiting fault current and enhancing dynamic performance of VSC-HVDC system. The main contributions of this chapter can be summarized as:

a) The impact of proposed BFCL solution is substantial in suppressing DC link voltage fluctuation.
b) Reduction in fault current, DFIG speed and active power oscillations is achieved with the proposed BFCL control scheme.
c) The proposed BFCL solution is superior over SDBR in all aspects as evident from the graphical plots and index based results.

CHAPTER 6

VARIABLE RESISTIVE BRIDGE TYPE FAULT CURRENT LIMITER

6.1 Introduction

Despite of several potential benefits, VSC-HVDC system is more vulnerable to AC/DC faults than LCC-HVDC system. Upon the occurrence of short circuit faults, the level of fault current surges tenfold within several milliseconds feeding very high fault current into the DC cable through the freewheel diode which may cause severe damage to the voltage source converters [9,205–207]. A prospective solution to the fault problems of VSC-HVDC system is to employ fault current limiters. During the response time of circuit breaker, fault current limiter can suppress the large fault current in VSC-HVDC system. Thus, fault current limiter can evidently mitigate the current interruption stress on circuit breakers and reduces possible serious damage to the power electronic converters.

DC reactor type superconducting FCL is presented [208] to limit the fault current which has high implementation and maintenance costs. This structure also has a resistor to reduce the current rating of superconducting coil. However, this resistance cannot be varied to control the fault current level. In [62], a similar type of FCL is introduced with non-superconducting DC coil. This structure is more practical and keeps fault current level within pre-specified value than one presented in [208]; however, it has considerable voltage drop in large non-superconducting coil.

Till date, VSC-HVDC system's stability has been examined with the application of different types of superconducting fault current limiters (SFCLs) [1,9,12,169]. However, superconducting fault current limiters have several drawbacks such as big size, heavy weight and cost, magnetic field interference with nearby sensitive devices, higher leakage and circulating currents, long recovery time, and loss in stand-by mode [13,14,69,74,92,125,127,132] compared to non-superconducting fault current limiter. Non-superconducting variable resistive bridge type fault current limiter (VR-BFCL) can limit the fault current as well as augment transient stability with low implementation cost, low loss, and low voltage drop [15,22–24]. However, this new non-superconducting low cost VR-BFCL technology has not been examined as yet in enhancing dynamic stability of VSC-HVDC system.

With such background, variable resistive bridge type fault current limiter (VR-BFCL) is proposed in this chapter to enhance VSC-HVDC system FRT capability. A simple non-linear control has been proposed to control VR-BFCL. The advantage of the proposed non-linear control is two-folds such as it is superior over traditional fixed duty control and less complicated as well as easy implementation. To evaluate the performance of the proposed non-linear control based VR-BFCL, its performance is compared with that of the conventional fixed duty controlled VR-BFCL. Real time digital simulator (RTDS) has been used to conduct the simulations.

6.2 Variable Resistive Bridge Type Fault Current Limiter

In this chapter, non-linear control based VR-BFCL is proposed to resolve the fault issues in VSC-HVDC system. Its construction, operating principle and the proposed non-linear control method are described in the succeeding subsections.

6.2.1 VR-BFCL Structure and Operation

VR-BFCL is composed of an isolation transformer, a diode bridge, and series connected resistance and reactance in the DC side of the diode bridge [22,23,174,209] as shown in Figure **6.1**. An IGBT switch is connected in parallel with the resistance, the main current limiting part of VR-BFCL. IGBT switch is kept turned on during normal operation of the system without any fault and hence evacuating resistance is bypassed. In this operating condition, L_{DC} acts like short circuit as it gains maximum charge corresponding to the maximum value of the line current. Eventually, VR-BFCL has approximately no effect on normal operation of the power system. The benefit of the L_{DC} is that during system disturbance it protects drastic increase of current. As a result, L_{DC} protects IGBT switch from high *di/dt*.

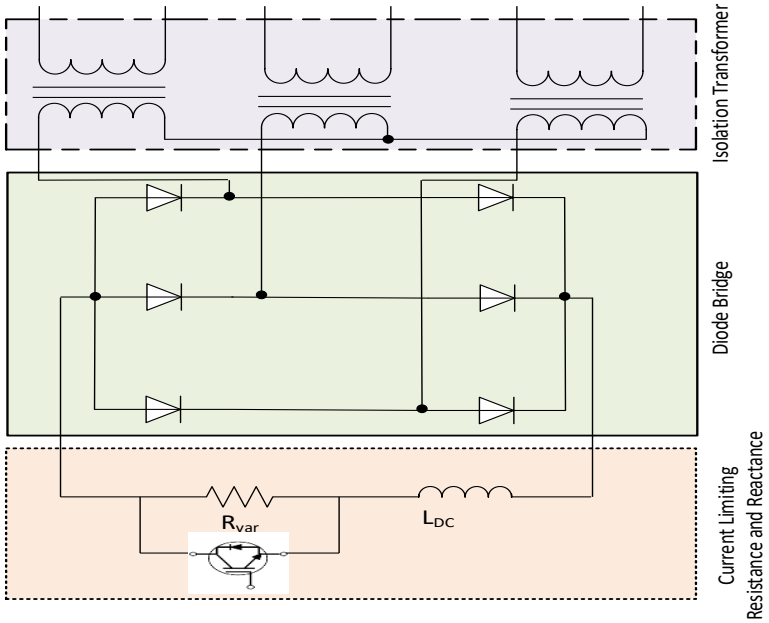

Figure 6.1 Variable Resistive Bridge Type Fault Current Limiter

The DC side voltage of the VR-BFCL is given by the following equation [22].

$$V_{DC} = \frac{6}{\pi}\sin(\frac{\pi}{3})aV_m \tag{6.1}$$

where a the isolation transformer turn ratio and V_m is the peak voltage in the primary side of the isolation transformer. The effective resistance appeared in the DC side of the bridge can be made adaptable by applying the proper control signal to the IGBT gate as following.

$$R_{DC} = (1 - D)R_{\text{var}} \tag{6.2}$$

where R_{DC}, D and R_{var} are the effective DC resistance, duty ratio, and variable resistance respectively. The effective resistance appeared in the AC side of the bridge can be computed by employing the concept of equal power in the AC and DC sides of the bridge while neglecting the power loss in isolation transformer, bridge rectifier and IGBT switch as follows [22].

$$\frac{3(V_m / \sqrt{2})^2}{R_{aceff}} = \frac{(\frac{6}{\pi}\sin(\frac{\pi}{3})aV_m)^2}{R_{DC}} \tag{6.3}$$

where R_{aceff} is the AC side effective resistance. This gives the following effective AC resistance.

$$R_{aceff} = \frac{\pi^2}{18a^2} R_{DC} \tag{6.4}$$

This effective resistance is inserted with the line during system faults to limit the severe fault current and eventually improve system FRT capability as well as dynamic stability. In this study, non-linear controller is proposed to generate variable duty cycle during the inception of severe faults in order to insert dynamic effective resistance for limiting fault current and augmenting transient stability of VSC-HVDC system.

6.2.2 Non-Linear Control of VR-BFCL

Since the power system is highly non-linear, a non-controller is proposed in this work to control VR-BFCL. The control block takes the deviation of reference DC link voltage (V_{DCref}) and measured DC link voltage (V_{DCmes}) of the HVDC link. As the HVDC system stability is directly affected by the performance of the DC voltage control [71,72,196,210,211] non-linear controller takes the amount of DC link voltage deviation as its input and provides variable duty (D) to emulate variable effective resistance during fault governed by the following non-linear equation.

$$D = \frac{1}{\sqrt{K\left|\Delta V_{DC}\right|}} \tag{6.5}$$

where K is the gain whose proper value is to be determined. This non-linear equation is proposed to generate variable duty depending on the total DC link voltage deviation. As seen in the above equation, with the increase of voltage deviation duty decreases. And, with the decrease of duty, effective AC resistance increases which reduces fault current and hence improves dynamic performance. Duty (D) versus voltage deviation is plotted for different values of gain (K) as shown in Figure **6.2**.

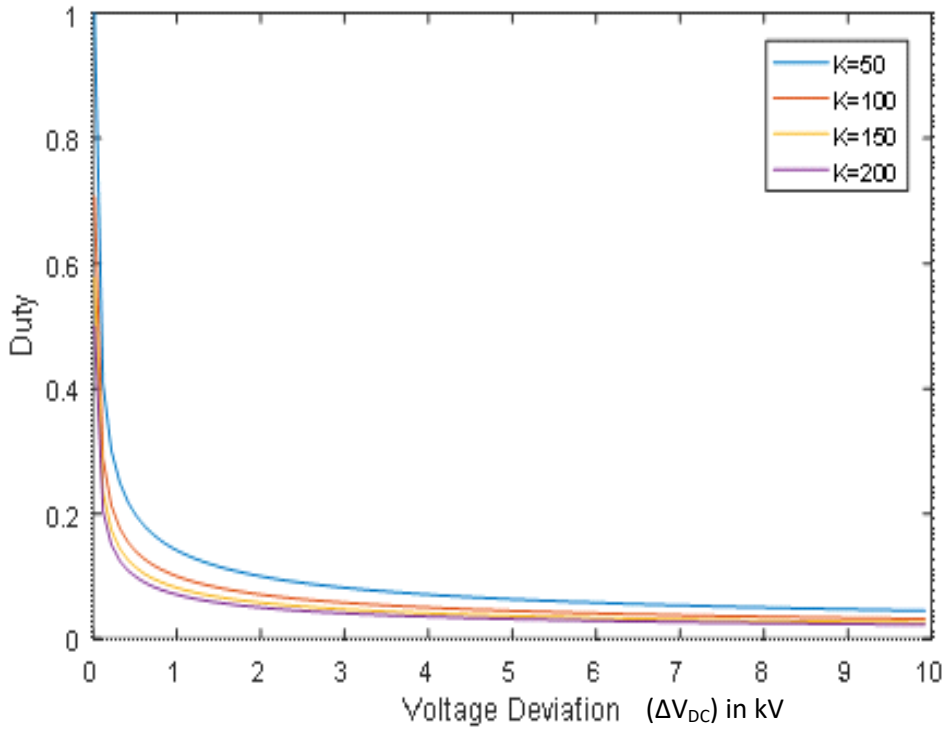

Figure 6.2 Duty Verses Voltage Deviation for Different Gains

In order to determine optimum value of gain (*K*) different types of faults with different intensities have been applied in the VSC-HVDC system. It was found that k=100 gives best performance during severe faults. This is evident from Figure **6**.**3**. Performance index value for voltage deviation defined as $dc_{volt} = \int_{T_0}^{T} |\Delta V_{DC}| dt$ is plotted for different values of gain (*K*) in Fig. 3. Here, *T* is the transient period after the application of fault. As this index measures deviation in DC link voltage of VSC-HVDC system, so a lower value is indicative of better performance of the system. It is evident from the Figure **6**.**3**, values of performance indices increase for gain *K*>100. Also for *K*<100, index values are higher which means that *K*=100 gives the better performance of the system during three phase faults. A gain value higher than this gives overcompensation whereas a value lesser than this provides insufficient compensation.

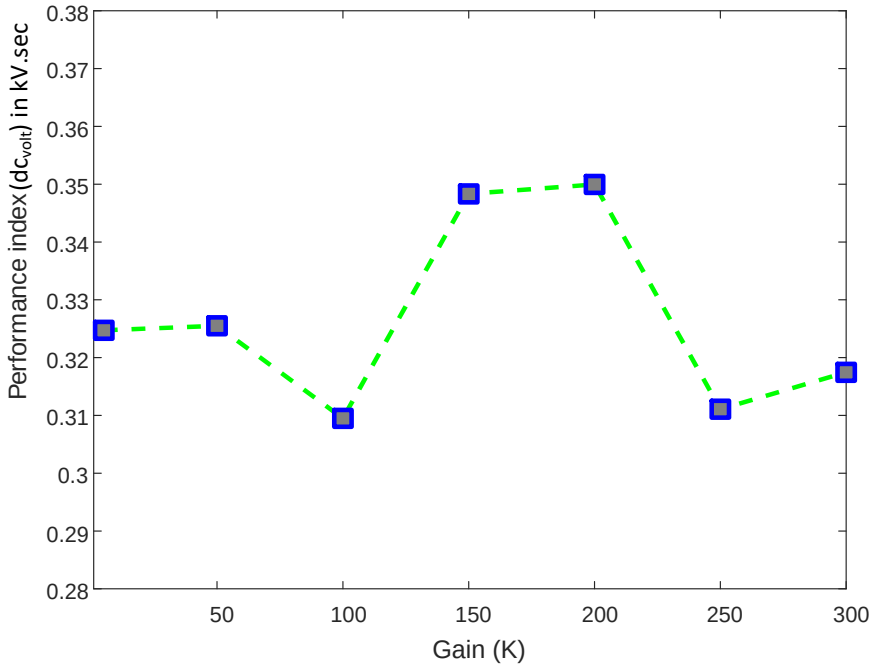

Figure 6.3 Performance Index versus Gain for Three Phase Fault

It is worth mentioning that other nonlinear equations for duty generation such as exponential, quadratic, cubic, and logarithmic were tried. However, those nonlinear equations failed to provide better performance. Over current or voltage sag at the point of common coupling (PCC) may be employed to detect fault in AC/DC systems [191]. Over current at PCC has been used in this study to detect fault for the proposed non-linear controller as shown in Figure **6.4**.

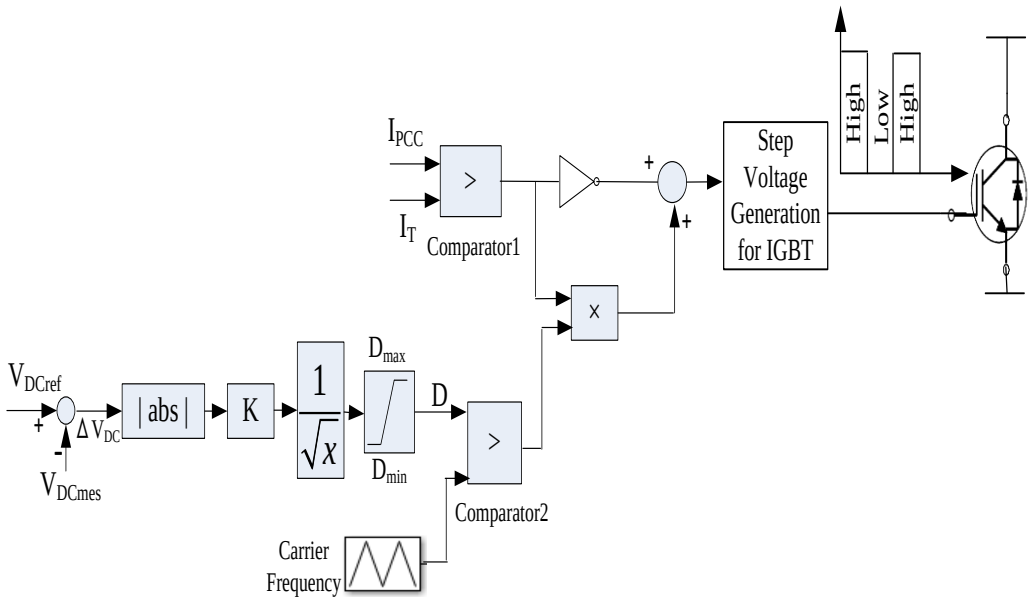

Figure 6.4 Overall Non-linear Control Strategy

Measured PCC current (I_{PCC}) is compared with a predefined threshold current (I_T) by comparator1. During normal operation when I_{PCC} is lower than the I_T, output of comparator1 becomes low. The output of this comparator1 is inverted and added with the product of the comparator2 output. Thus, output of summation block is high during normal operating condition of the system. Consequently, output of step voltage generation block becomes high to keep IGBT turn on. Therefore, evacuating resistance is bypassed and VR-BFCL has negligible impact on system in this condition. However, during grid abnormalities I_{PCC} goes on increasing and becomes higher than I_T, as a result comparator1 output becomes high. So, the low and high voltage signals are provided by the block of step voltage generation to turn on and turn off IGBT in dynamic fashion for providing varying compensation depending on the duty (D) provided by non-linear equation during system disturbances. Another noteworthy features of this work is that the proposed non-linear controller performance is compared with fixed duty control [22]

where a fixed duty is applied corresponding to average value of the *D* during severe disturbance.

6.3 Connection of VR-VFCL with VSC-HVDC System

For fault ride through (FRT) capability and dynamic performance analysis, VSC-HVDC system as shown in Figure **6.5** is demonstrated in this chapter.

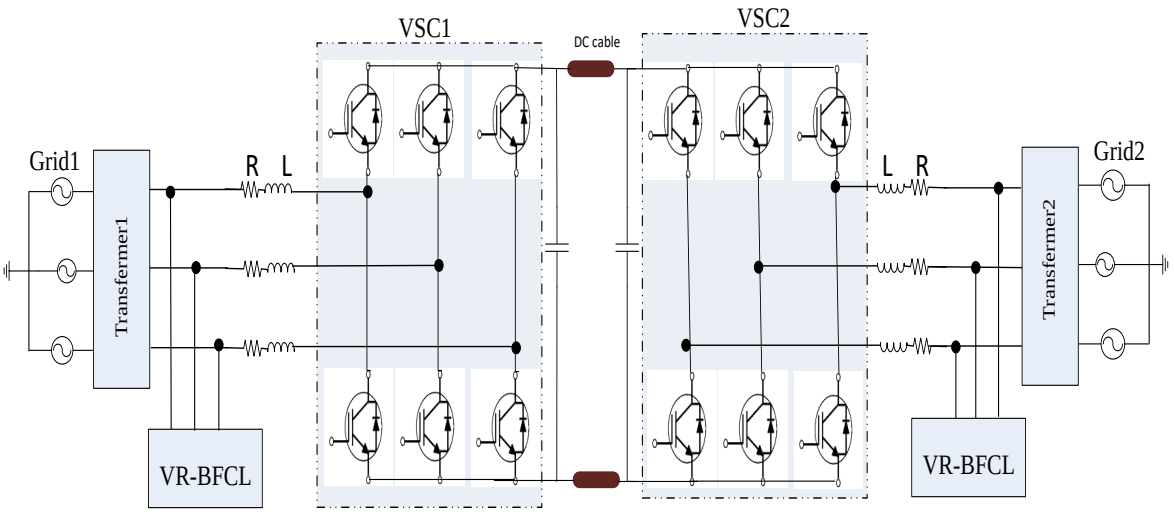

Figure 6.5 Connection of Proposed VR-BFCL with VSC-HVDC

Depending on reference power command, VSC-HVDC system permits power flow in both directions between two grids. For HVDC system, controlling of DC link voltage at a predefined value is vital task. In two-terminal VSC-HVDC systems, one of the VSCs controls DC link voltage. In this work, controller of VSC2 controls the DC bus voltage. Similar control strategy proposed in chapter 5 is used to control active power, reactive power, and DC link voltage.

6.4 Results and Discussion

Both symmetrical and unsymmetrical faults are applied in the system without FCL, with fixed duty control and with the proposed non-liner control of VR-BFCL. The system data and results are presented in the following subsections.

6.4.1 Simulation Considerations

Test system of Figure **6.5** is implemented with real time digital simulator (RTDS) to confirm the efficacy of proposed non-linear control based VR-BFCL solution. Furthermore, non-linear controller is equated with fixed duty control to demonstrate the enhancement of system performance in regulating fault current.

At the starting, VSC-HVDC system is considered to be operated in its steady state condition. Then, two different faults are applied at the PCC of the network: balanced-3LG and unbalanced-1LG fault. The following cases are considered and compared to show the efficacy of the proposed control technique.

i) without FCL

ii) with fixed duty controller VR-BFCL

iii) with proposed non-linear controller VR-BFCL

6.4.2 Symmetrical Fault Applications

Initially, both the grids are disconnected from voltage source converters (VSCs) connection and DC link capacitors are discharged. Also, all the controllers are kept inactive by blocking getting pulses of VSC1 and VSC2. Afterwards, both the grids are connected with HVDC converters through interface resistor, inductor and transformer, consequently DC link capacitor is gradually charged through the antiparallel diodes of

VSCs to a voltage level of around 25 kV. DC reference voltage is then set to 35 kV and outer controller regulates the DC link voltage to this set value. Now, reference active power (P_{ref1}) is set to 20 MW for VSC1 controller to deliver this power to grid2 from grid1. Symmetrical and unsymmetrical faults are now applied in the system at this steady state condition. All the faults have been applied for 6 cycles for three different conditions: without FCL, with fixed duty controller, and with proposed non-linear controller. Figure **6.6** demonstrates the dynamic performance improvement of VSC-HVDC system with the proposed non-linear control based VR-BFCL for symmetrical three phase fault applied in grid1. DC link voltage varies from 23.56 kV to 50.05 kV without any supplementary controller. This higher voltage fluctuation is slightly reduced with fixed duty controller based VR-BFCL in which voltage fluctuates from 30.88 kV to 45.47 kV. However, the proposed non-linear control based VR-BFCL suppresses voltage fluctuation greatly keeping the voltage variation from 31.5 kV to 41.8 KV. Furthermore, settling time for DC link voltage is significantly reduced with the proposed control technique which takes 0.906 second only whereas it takes 1.04 seconds with fixed duty controller and 1.669 seconds without any FCL.

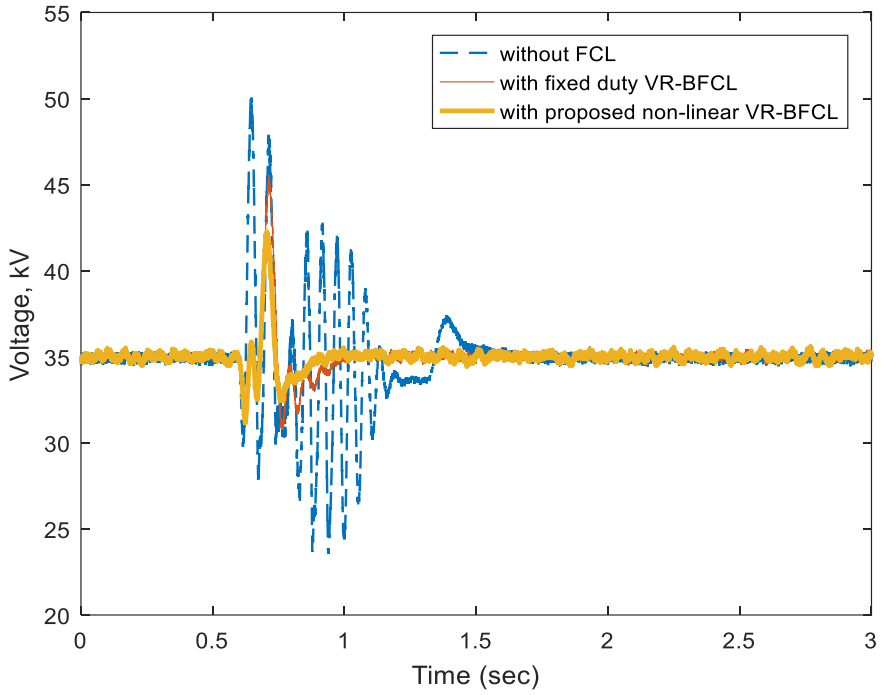

Figure 6.6 DC Link Voltage Response for 3LG Fault

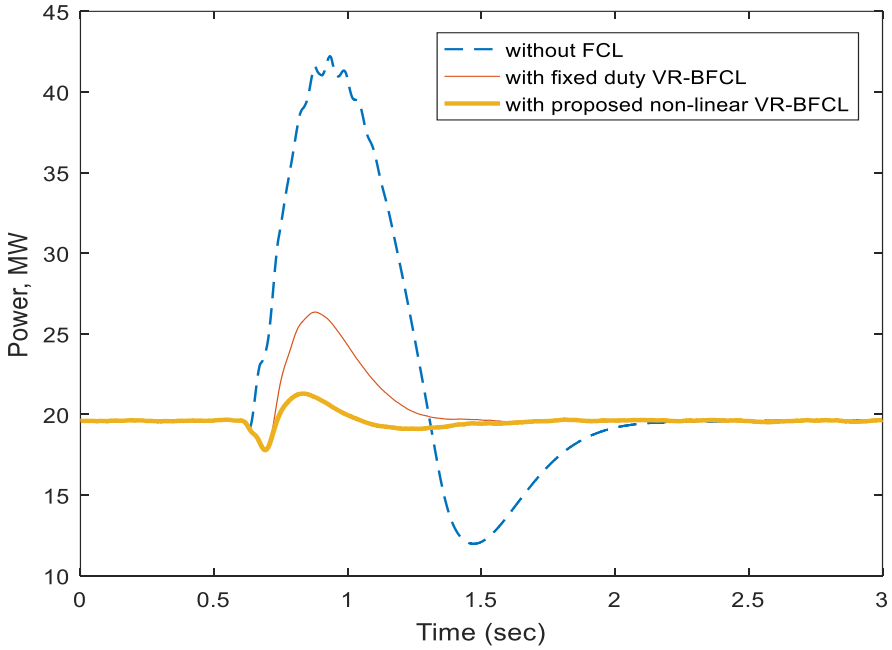

Figure 6.7 Response of Active Power Exchange between Two Grids for 3LG Fault

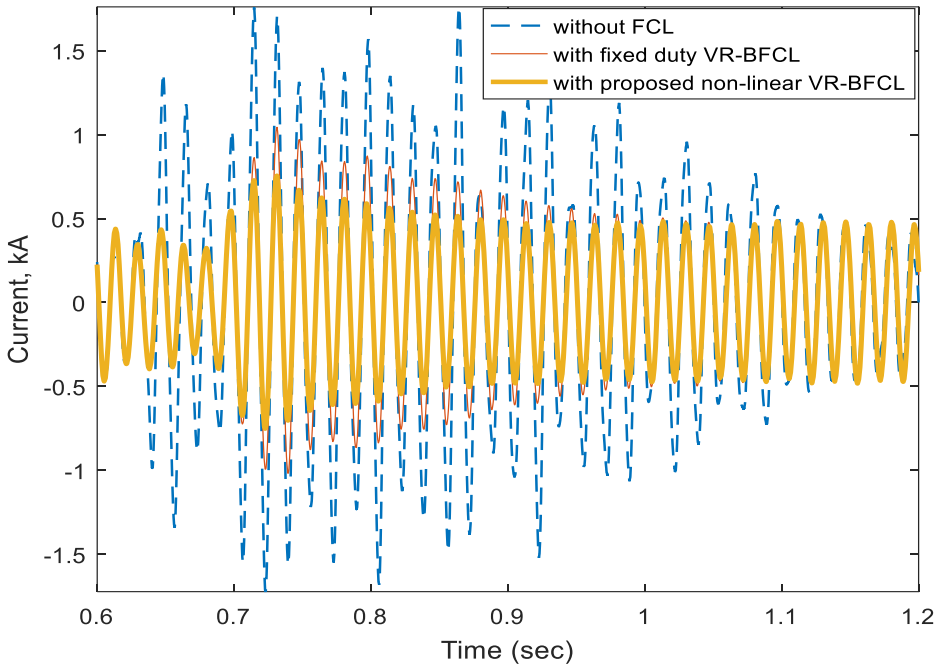

Figure 6.8 Response of Phase 'A' Current of Grid1 for 3LG Fault

Figure **6.7** clearly depicts that the oscillation in power exchange between two grids through the HVDC link is higher without any auxiliary controller. Active power oscillates between 5MW to 42MW without any fault current limiter controller. Fixed duty controller based VR-BFCL reduces oscillation by 74.3%. However, the proposed non-linear controller based VR-BFCL significantly reduces the power oscillation in the system for 3LG fault applied in grid1 which is around 87.8% reduction. Current limiting capability of the non-linear control based VR-BFCL is clearly visualized in Figure **6.8**.

6.4.3 Unsymmetrical Fault Applications

Unsymmetrical single line to ground (1LG) fault has been applied in grid1 of the VSC-HVDC system. DC link voltage fluctuation, power oscillation and the fault current have been reduced with the proposed non-linear control based VR-BFCL as visualized by the real time simulation results. DC link voltage response is shown in Figure **6.9** with 1LG

fault applied at grid1 for all the considered cases. Without FCL, DC link voltage fluctuates between 32.56 kV to 39.75 kV. A DC link voltage fluctuation reduction of 9.87% has been observed with fixed duty control. However, the proposed non-linear control based VR-BFCL reduces the DC link voltage fluctuation by 24.6%.

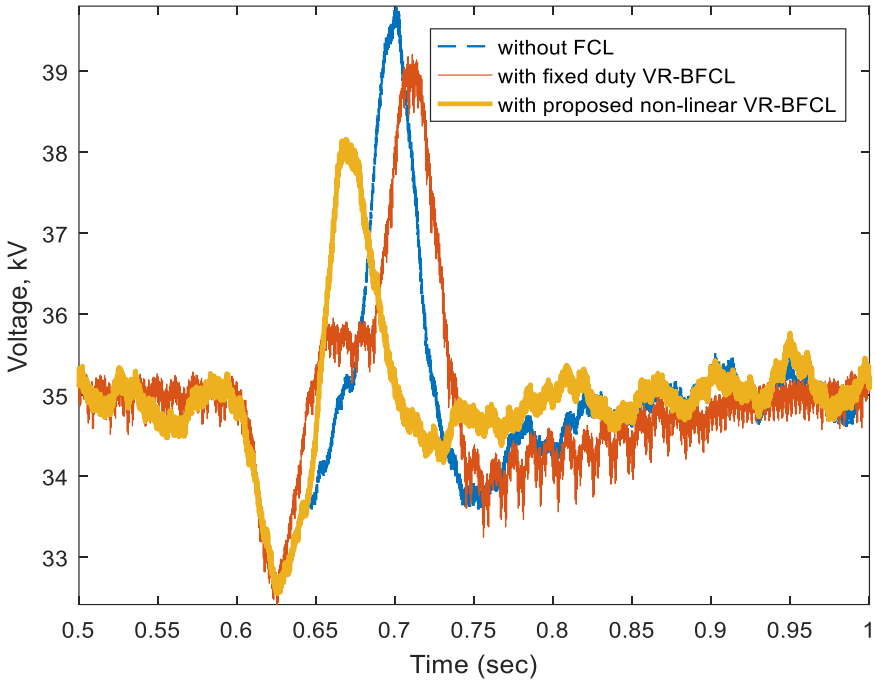

Figure 6.9 DC Link Voltage Response for 1LG Fault

As shown in Figure **6.10**, power exchange between grid1 and grid2 oscillates over a wide range without any auxiliary controller. Applications of fixed duty control based VR-BFCL damps power oscillation by 30.8%. However, the proposed non-linear controller for VR-BFCL gives best power oscillation damping performance of 50.5%. Maximum level of fault current limiting capability is observed with the proposed non-linear control based VR-BFCL over without FCL and with fixed duty VR-BFCL controller for 1LG fault as shown in Figure **6.11**.

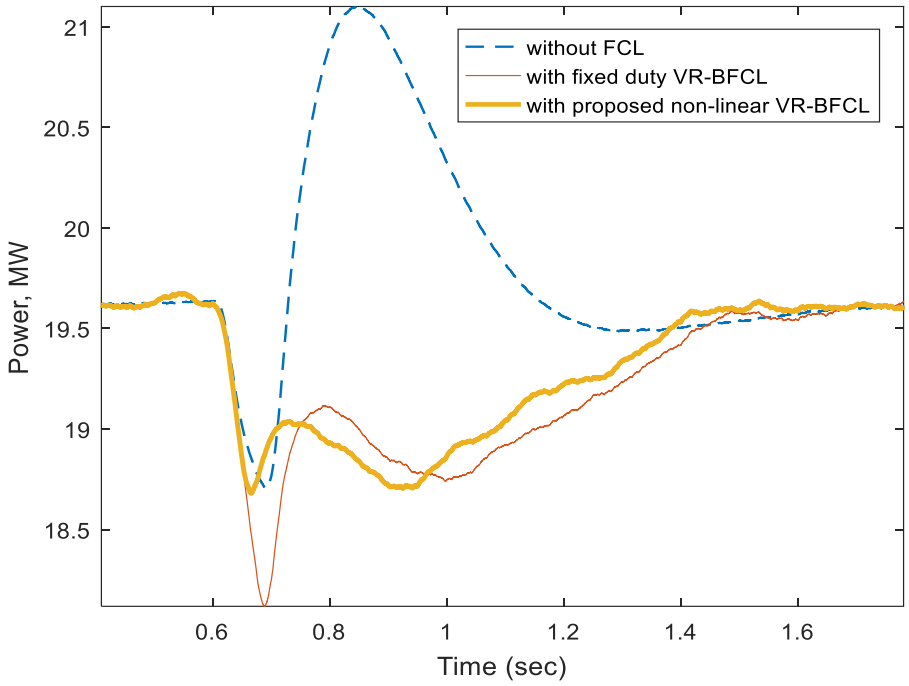

Figure 6.10 Response of Active Power Exchange between Two Grids for 1LG Fault

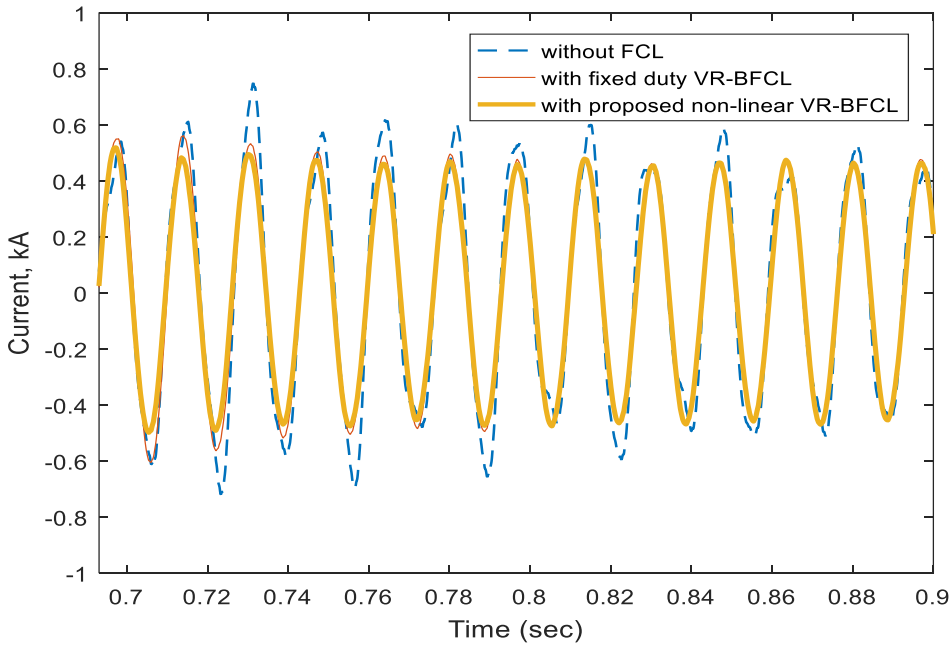

Figure 6.11 Response of Phase 'A' Current of Grid1 for 1LG Fault

6.4.4 Index-based Comparison

Index-based comparison is conducted in order to get more clear perception of fault ride through and transient stability enhancement with the proposed non-linear control based VR-BFCL. Similar performance indices as resented in chapter 4 are calculated for several parameters of the system. Values of performance indices for different symmetrical and unsymmetrical faults are presented in Table **6**:**1** and Table **6**:**2** respectively.

Table 6:1 Values of Indices with Proposed Non-Linear VR-BFCL for Symmetrical 3LG Fault

Index parameters	Values of indices in percent		
	Without FCL	With fixed duty VR-BFCL	With Proposed nonlinear VR-BFCL
$dclink_{volt}$	2.0276	0.6452	0.4623
ac_{pow}	7.8727	1.4493	0.6301
$line_{curr}$	0.3948	0.3360	0.3159

Table 6:2 Values of Indices with Proposed Non-Linear VR-BFCL for Unsymmetrical 1LG Fault

Index parameters	Values of indices in percent		
	Without FCL	With fixed duty VR-BFCL	With Proposed nonlinear VR-BFCL
$dclink_{volt}$	0.5321	0.4835	0.3831
ac_{pow}	0.6653	0.5155	0.4485
$line_{curr}$	0.3532	0.3029	0.3013

Performance of VSC-HVDC system is worst without any supplementary controller as evident form the index values of several performance indices presented in Table **6**:**1** and Table **6**:**2**. A slight improvement is observed with traditional fixed duty control. However, a notable improvement in FRT capability as well as stability is observed with the proposed non-linear control based VR-BFCL. Non-linear VR-BFCL shows smaller values for all indices which means it shows better performance for stabilization of the VSC-HVDC system.

6.5 Conclusion

In this chapter, non-linear control based VR-BFCL is proposed for limiting fault current and augmenting fault ride through capability of VSC-HVDC system connecting two grids. Depending on fault detection based on PCC current, VR-BFCL non-linear controller is designed. The proposed non-linear controller takes the amount of DC link voltage deviation as its input and provides variable duty to generate and insert effective resistance in order to limit fault current as well as improve FRT capability. VSC-HVDC plant, VR-BFCL and their controllers have been developed in RTDS. Both balanced and unbalanced faults are applied in the system so as to show the proficiency of the proposed controller in improving FRT capability of VSC-HVDC system. From real time implementation results, non-linear control based VR-BFCL is found as very efficient way of restricting fault current and augmenting transient response of VSC-HVDC systems. Also, approximately there is no effect of VR-BFCL on normal operation of HVDC systems. Active power oscillation, DC link voltage fluctuation, and fault current are reduced significantly and system stability is guaranteed with the proposed non-linear control based BR-BFCL. Furthermore, proposed non-linear control based VR-BFCL is

compared with traditional fixed duty control where the proposed control technique outperforms the fixed duty control in all aspects as evident from the graphical plots and index based results.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

In this chapter, the conclusions and implications of this thesis are summarized. In the following subsections proposed control methodologies for fault ride through capability enhancement of voltage source converter-high voltage DC (VSC-HVDC) systems with bridge type fault current limiters are summarized with analysis of implementation results. Furthermore, several possibilities to extend this work is provided as a future work.

7.1 Conclusions

In this dissertation, efficient controllers are proposed for grids connected and wind farm integrated VSC-HVDC systems with non-superconducting bridge type fault current limiter (BFCL) to limit fault current as well as augment fault ride through (FRT) capability. The proposed control techniques are able to reduce fault current and minimize fluctuation in DC link voltage, machine speed and active power. Fixed speed wind and doubly fed induction generator (DFIG) based wind based wind farms are integrated and their FRT capability is tested with proposed bridge type fault current limiter controllers. The conclusions of this dissertation are summarized in different subsections.

MODEL PREDICTIVE CONTROL BASED BRIDGE TYPE FAULT CURRENT LIMITER

1- Bridge type fault current limiters are connected with the VSC-HVDC systems and controllers are developed to activate and deactivate them depending on appearance of disturbances on the system where BFCL bridge part is short

circuited by its controller during normal operation and open circuited during faulty conditions to add resistance and reactance for limiting fault current.

2- Finite control set model predictive controller (MPC) is developed for controlling active and reactive power independently as inner current controller.

3- Optimum switching states are selected for MPC based on objective function which minimizes error between reference and predictive currents.

4- A delay compensation is included to mitigate oscillation in load current around its refernce value which predicts the current by shifting load model one step forward in time.

5- The resistance and reactance of BFCL are included in inner MPC for determining optimal switching states to follow the reference power during system contingencies by its controller.

6- One of the voltage source converters controller is designed to control the HVDC DC link voltage to its predefined valule as a outer controller.

7- The proposed control technique is tested by applying various disturbanes: single line to ground fault, line to line fault and double line to ground fault.

8- The proposed control techne is found as very effective solution in limiting fault current of VSC-HVDC system for different faults.

9- Another significant feature of the proposed technique is that the MPC-BFCL performance in VSC-HVDC system is compared with its counterpart series dynamic braking resistor where MPC-BFCL outperforms SDBR.

FAULT RIDE THROUGH OPERATION WITH BFCL FOR GRIDS CONNECTED MODE AND FIXED SPEED WIND INTEGRATED MODE

1- A BFCL-based approach for fault current reduction and fault ride through capability enhancement as well as stability improvement of VSC-HVDC systems in different configurations of two-grids connected mode and wind farm integrated mode is investigated.

2- Terminal one of the voltage source converter control active and reactive power independently based on current control mode where direct axis current controls active power and quadrature axis current controls reactive power.

3- Terminal two converter regulates DC link voltage by employing proportional integral (PI) controllers as an outer loop. Power exchange between two grids or between grid and wind farm is added with the outer DC link PI output to generate active power reference for this converter.

4- The amount of power flow through each phase is considered in designing the resistance and reactance values of BFCL.

5- A fixed speed wind turbine is connected to the induction machine through gear box. Turbine blades are designed to stall if the wind speed exceeds a designed maximum. A number of capacitor banks equipped with switches are connected at the terminal of the induction machine. A control loop is designed among the switches in order to maintain power factor within a set-point range.

6- Pole zero cancellation technique and symmetrical optimum technique are used to tune inner and out PI parameters respectively.

7- The performance of the proposed control technique in augmenting FRT capability is evaluated by applying symmetrical and unsymmetrical faults. The obtained results from real time digital simulation clearly depict the efficacy of the proposed control technique.

DOUBLY FED INDUCTION GENERATOR BASED WIND FARMS INTEGRATION TO VSC-HVDC SYTEM WITH BFCL

1- Wind energy is extracted and integrated to the VSC-HVDC systems with doubly fed induction generator which is basically three phase wound-rotor induction machine. The wind-power system is modeled by wind turbine which is mechanically coupled through a gearbox to the DFIG. Stator side of DFIG is directly connected to the point of common coupling (PCC) and rotor of the machine is connected to the PCC with AC/DC/AC conversion system with two VSCs: stator side VSC (SVSC) and rotor side VSC (RVSC).

2- BFCL is designed based on total amount of power delivery from the wind farms and connected between PCC and wind farm side voltage source converter (WFVSC).

3- Two control loops are designed and implemented for SVSC: outer control loop which maintains a constant DC link voltage and inner current control loop to control the active and reactive powers.

4- RVSC controller is designed to track maximum power point. In optimal power point tracker, reactive rotor current reference is calculated from the optimal torque. Furthermore, RVSC controls active and reactive power by inner current

controllers in which currents are converted with a rotating reference frame to quasi DC quantities and controlled by PI controllers.

5- The proposed control technique is evaluated by performing real time digital simulator simulation. Different balanced and unbalanced faults are applied in the PCC. The main contributions of the proposed control technique are that the DC link voltage fluctuation, fault current and active power and machine speed oscillations are significantly reduced.

NON-LINEAR CONTROL BASED VARIABLE RESISTIVE BFCL

1- Non-linear control based variable resistive BFCL (VR-BFCL) is proposed to resolve the fault issues in VSC-HVDC system.

2- The effective resistance inserted by VR-BFCL is controlled by controlling gate pulses of IGBT switch which is in parallel with VR-BFCL.

3- Non-linear controller takes the amount of DC link voltage deviation as its input and provides variable duty to emulate variable effective resistance during fault.

4- Optimum gain for non-linear controller is designed by applying severe faults and calculating total voltage deviation.

5- Overcurrent at point of common coupling is employed to sense faults.

6- Performance of the proposed non-linear control based VR-BFCL is evaluated by RTDS implementation. Several performance indices are also considered and compared. A notable improvement in fault ride through capability is observed with the proposed control technique over traditional fixed duty control.

7.2 Future Works

Based on the research presented in this dissertation, it is recommended that further research should be conducted to fill up the following gaps as a future work.

- Detailed economic analysis of fault current limiters can be conducted.
- BFCL parameters can be tuned with optimization techniques such as GA, PSO, and DE for better performance.
- Different control technique such as robust control, optimal control and sliding mode control can be implemented and compared with PI control.
- Linearized model of the system can be used to design parameters for fault current limiters by using different optimization techniques.
- Analysis, application, and feasibility studies of non-superconducting FCLs can be conducted for multiterminal HVDC systems in order to reduce vulnerability of system with AC/DC faults.
- Practical implementation of fault current limiters can be done by conducting their field tests.
- Optimal placement of fault current limiters can be found out by considering network uncertainties.

APPENDIX

IMPLEMENTATION OF SYSTEMS AND CONTROLLERS IN RTDS

This appendix briefly explains the components used in this work for building the system and its controllers with RSCAD software of RTDS. Real time implementation and monitoring of the system are achieved with different components of RSCAD software.

Figure A.1 shows VSC-HVDC system and its controllers developed in RSCAD. HVDC system, fault current limiter, and converters are placed in small time steps box named HVDC_box1 and HVDC_box2. Controller for VSC1 and VSC2 are placed in two hierarchical boxes.

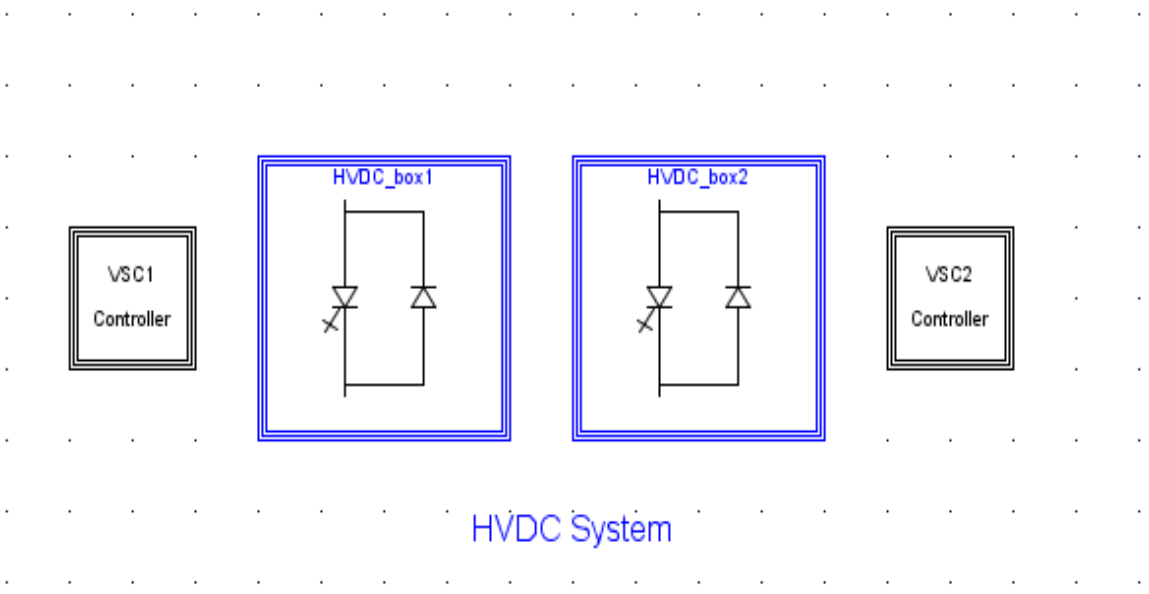

Figure A.1 VSC-HVDC System and its Controllers

Grid voltage generation, active and reactive power measurement, and integrator reset signal generation with RSCAD are shown in Figure A.2, Figure A. **3**, and Figure A. **4** respectively.

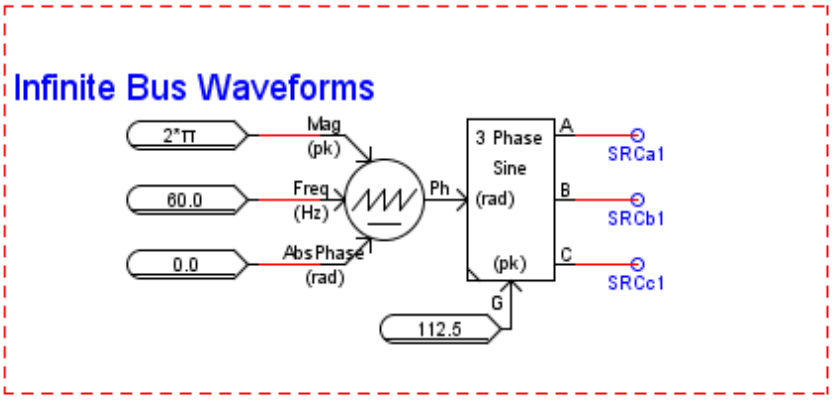

Figure A.2 Grid Voltage Generation

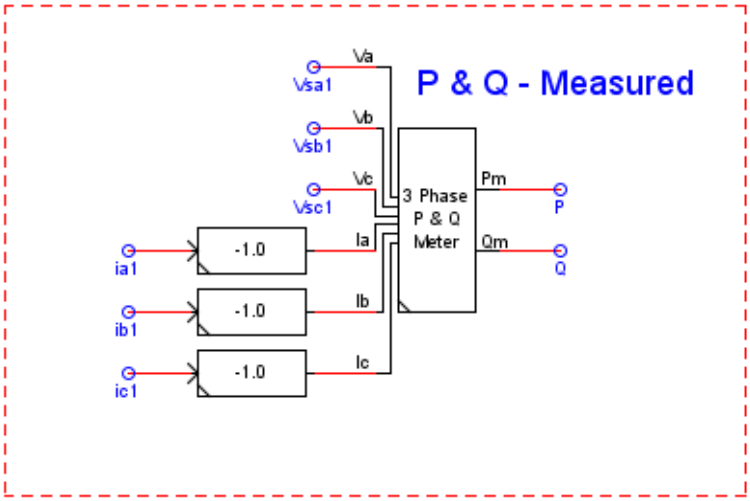

Figure A. 3 Active and Reactive Power Measurement

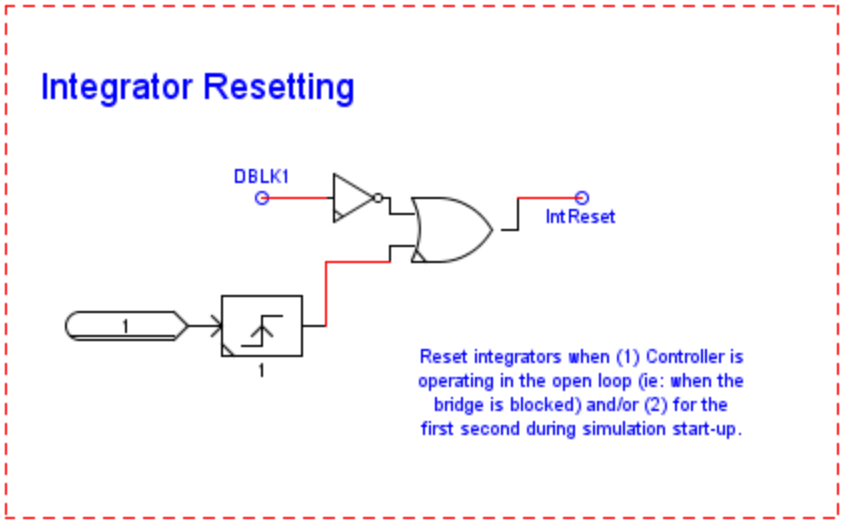

Figure A. 4 Integrator Reset Signal Generation

Control logic for application of symmetrical and different unsymmetrical fault is developed as shown in Figure A. **5**. Zero crossing detector, flip-flop, reset button are used to apply faults.

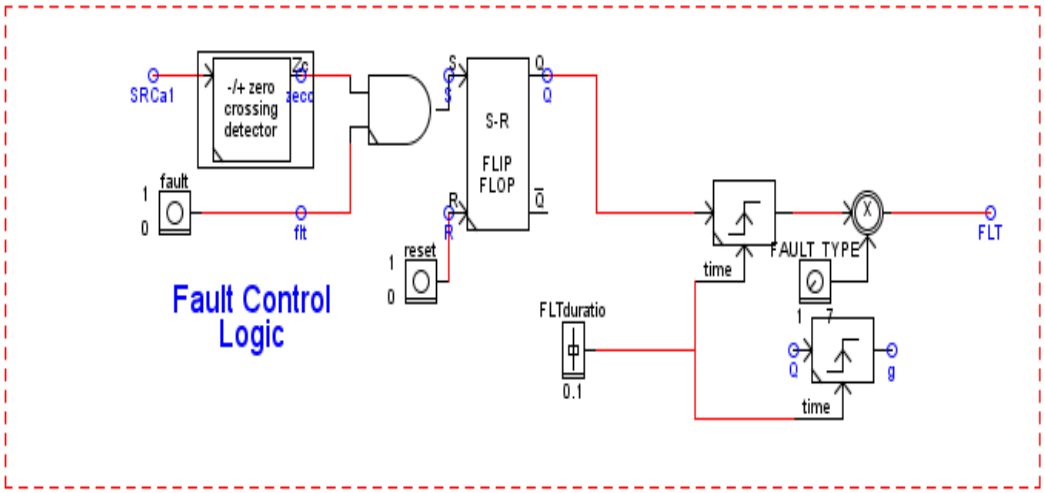

Figure A. 5 Control Logic for Symmetrical/Unsymmetrical Fault

Register, diode, inductor, and IGBT switch are used to develop bridge type fault current model in RSCAD as shown in Figure A.6.

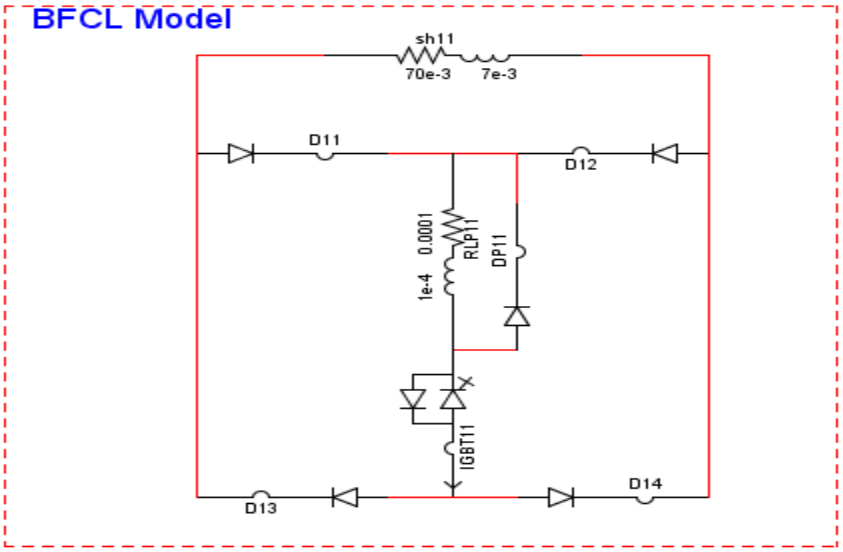

Figure A.6 Implementation of BFCL

Phase locked loop (PLL) is implemented in to synchronize voltage source converters (VSC) with grid or point of common coupling (PCC). Implementation diagram for PLL is shown Figure A. 7.

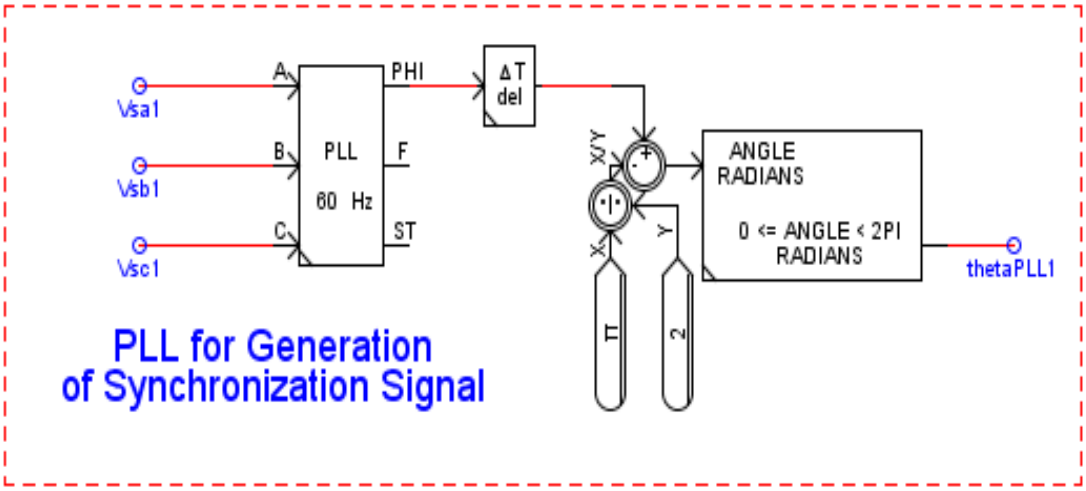

Figure A. 7 Internal Structure of PLL

Model predictive control approach for bridge type fault current limiter is implemented in alfa-beta reference frame. So, the reference current in alfa-beta reference frame is

generated with *dq* to *abc* and *abc* to alfa-beta transformations system as shown in Figure A.8.

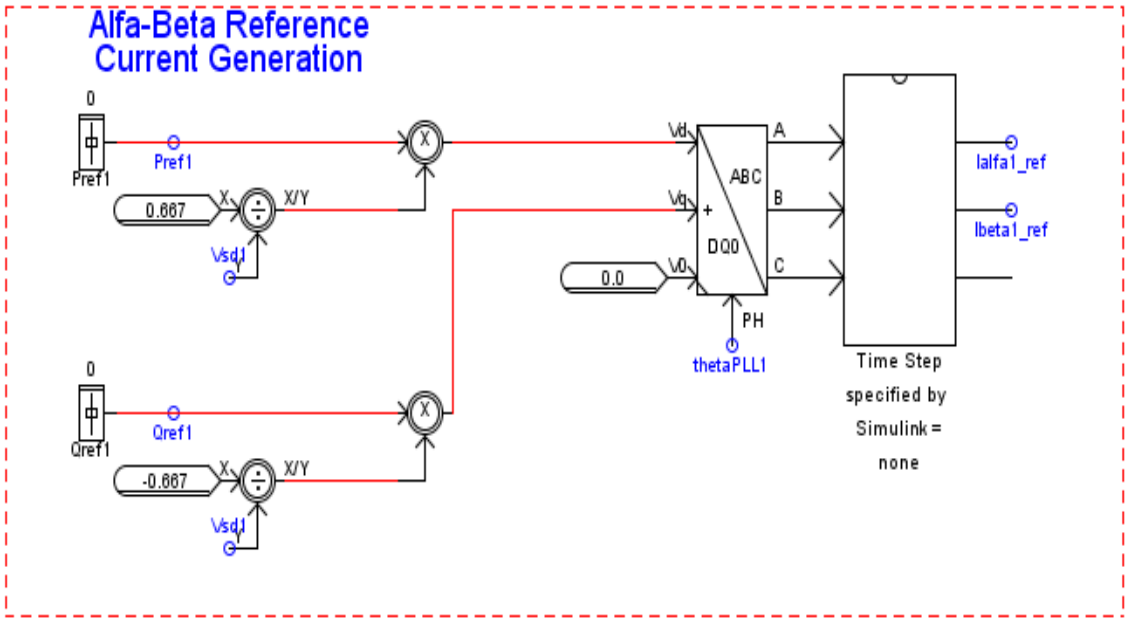

Figure A.8 Reference Current Generation from Active/Reactive Power

Different signals are transformed in alfa-beta and d-q frames as shown in Figure **A. 9** which are used in inner model predictive control approach.

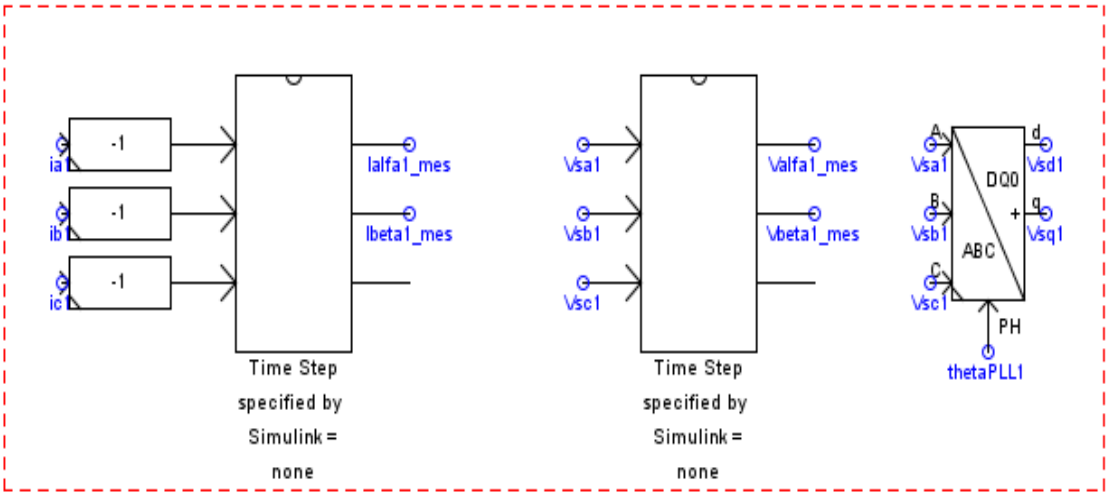

Figure A. 9 Transformation of Different Signals

The model predictive control algorithm is first developed in MATLAB environment. Then, the C-code is generated from this MATLAB code. The control block named MPC as shown in Figure A. **10** and Figure A. **11** is then built using 'component builder' feature of RSCAD which enables Simulink to RSCAD conversion.

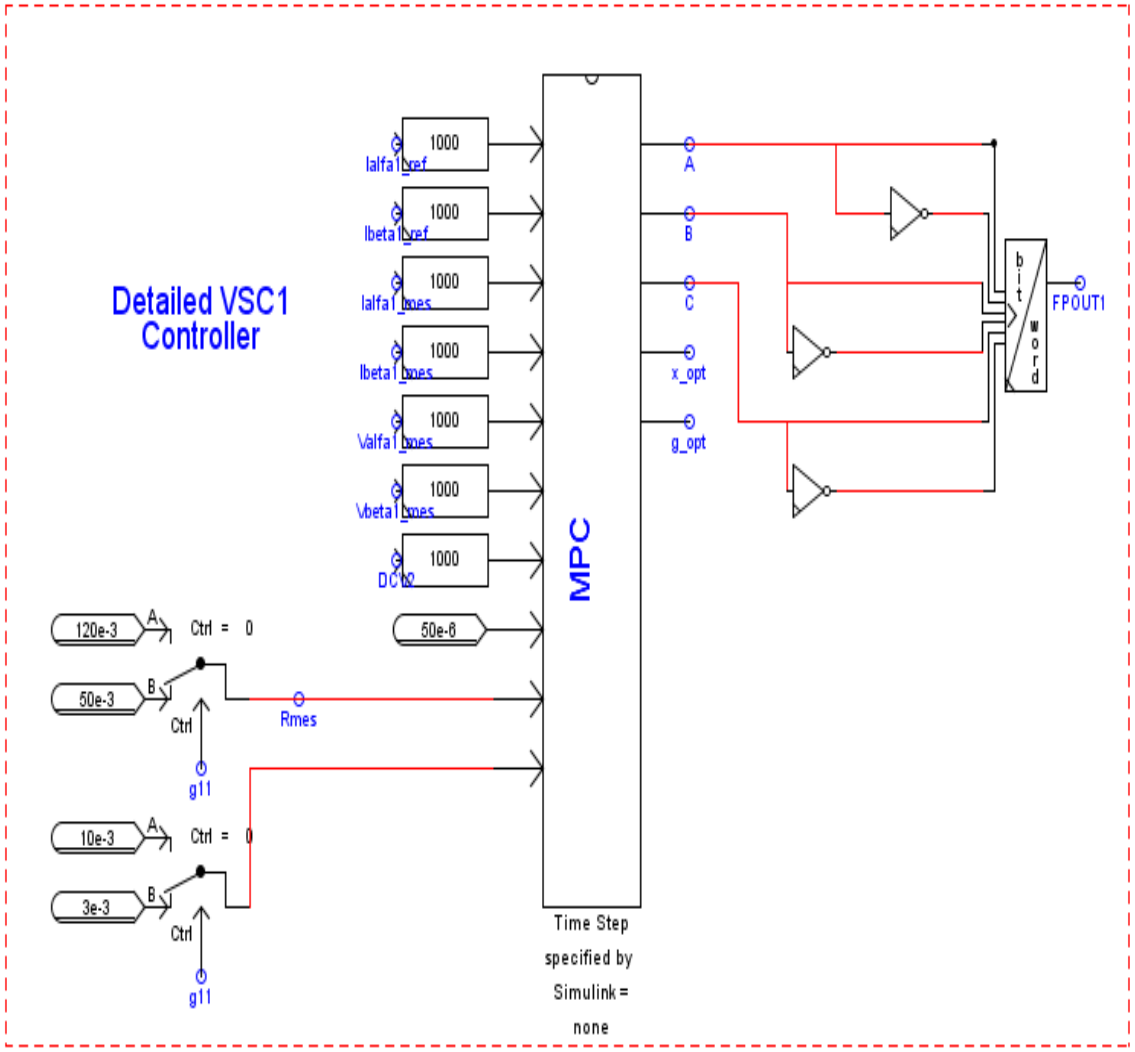

Figure A. 10 MPC Control of VSC1

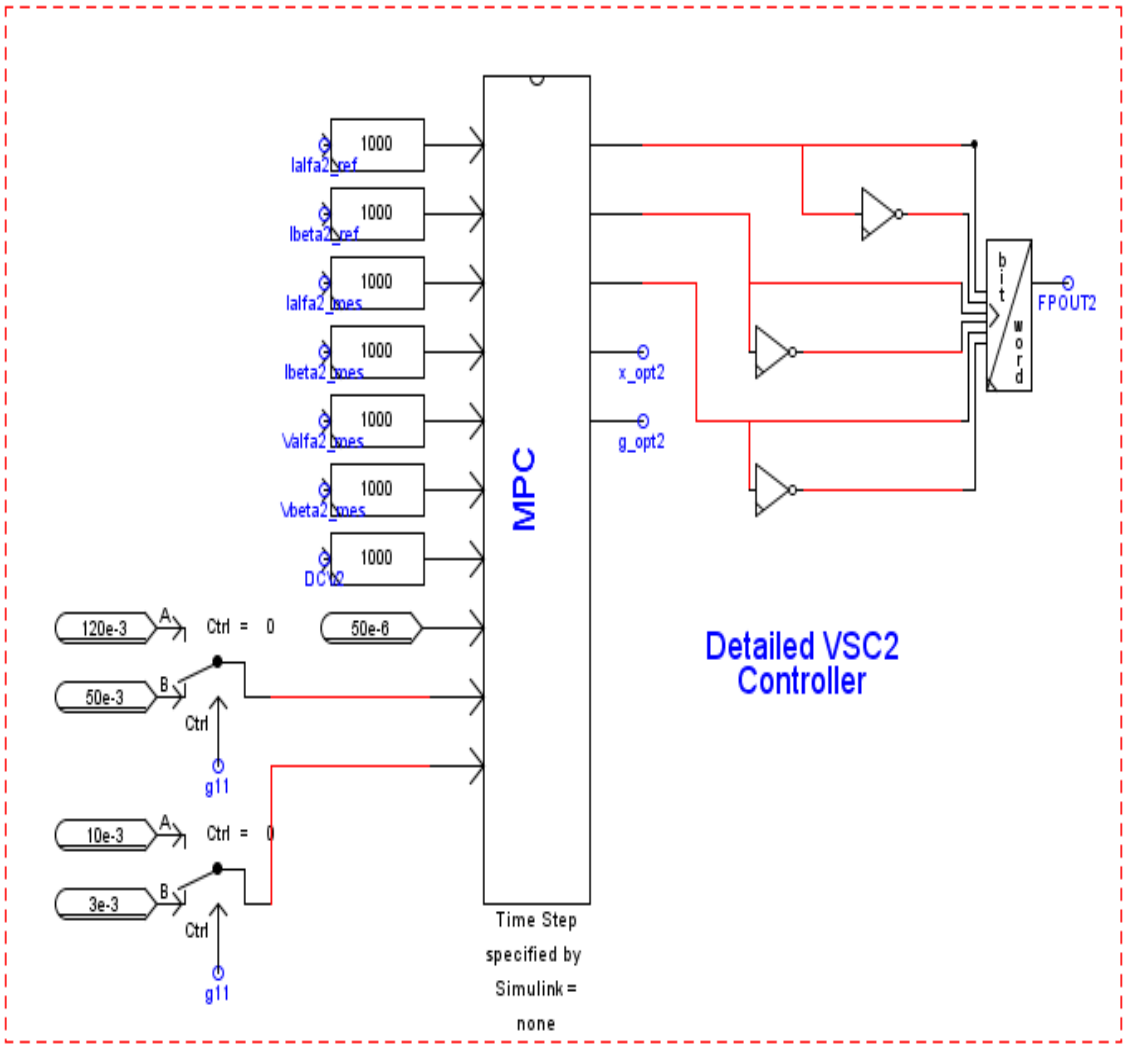

Figure A. 11 MPC Control of VSC2

Fixed speed wind farm is integrated with VSC-HVDC system as shown in Figure A. **12**. Wind turbine and wind generator are modeled in large time step hierarchical box. Then, generated power from wind farm is integrated to VSC-HVDC system built in small time step simulation box.

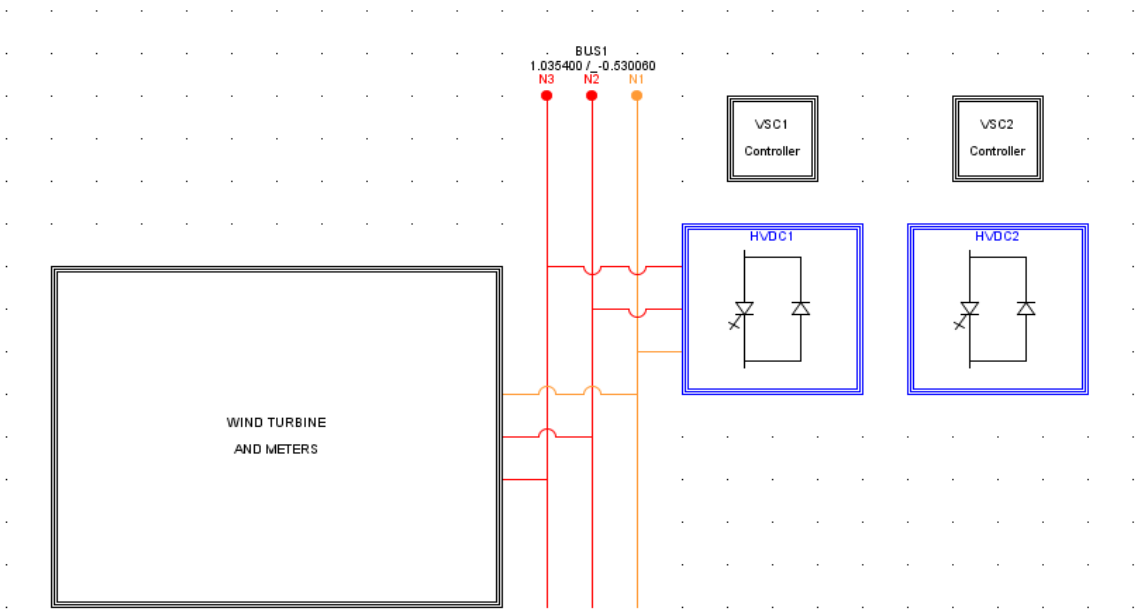

Figure A. 12 Development of Fixed speed Wind Integrated VSC-HVDC

The wind turbine and wind generator of the hierarchical box are shown in the Figure A. **13** below.

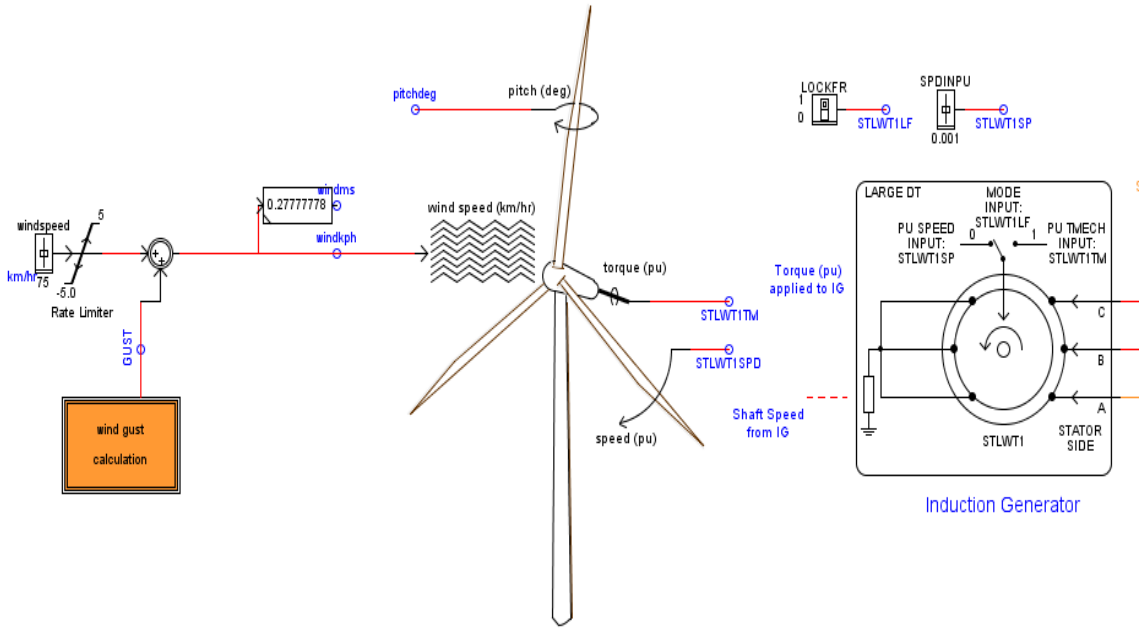

Figure A. 13 Wind Turbine and Generator Model

Capacitors are added and removed continuously to keep power factor within 0.95 to 1.05. Control circuit for connection and disconnection of capacitors is shown Figure A. **14**.

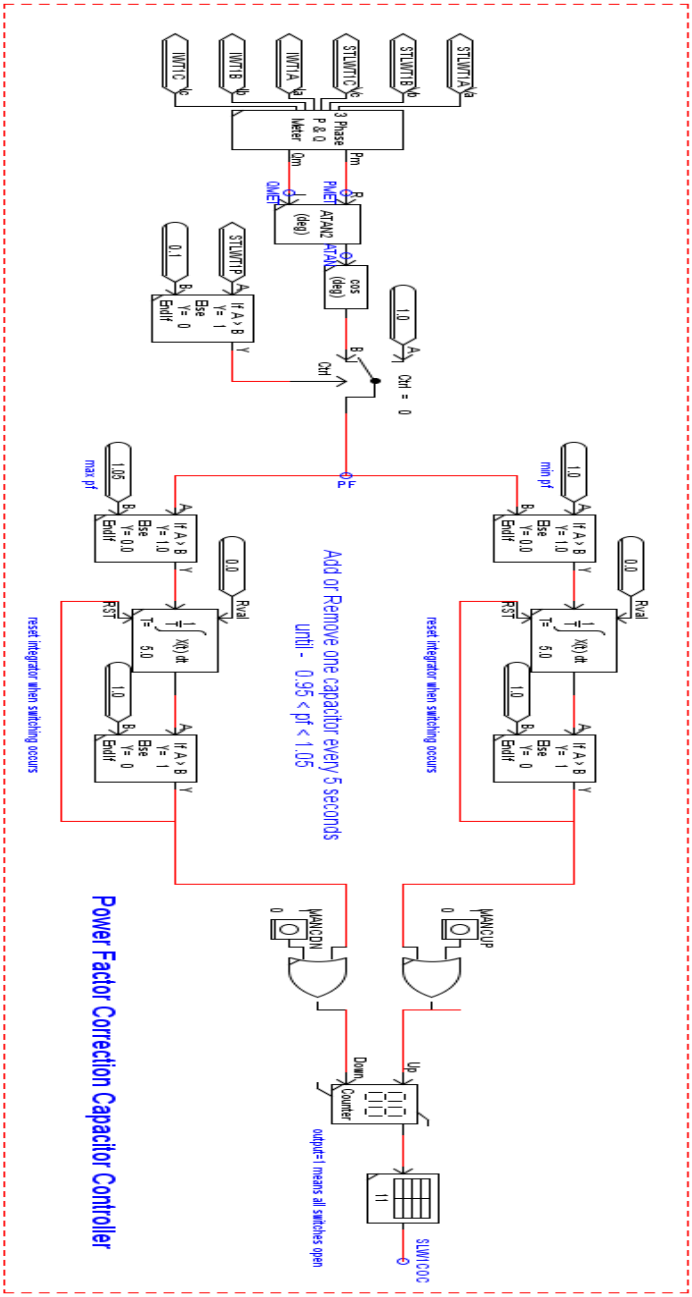

Figure A. 14 Capacitor Bank controller

RSCAD implementation diagram for active and reactive power control with VSC1 is shown Figure A. **15**. Reference active and reactive currents are generated from active and reactive

power. Measured three phase current is converted to *d*-axis and *q*-axis current with *abc* to *dq* transformation block. Proportional integral controllers are implemented for controlling both active and reactive components of current.

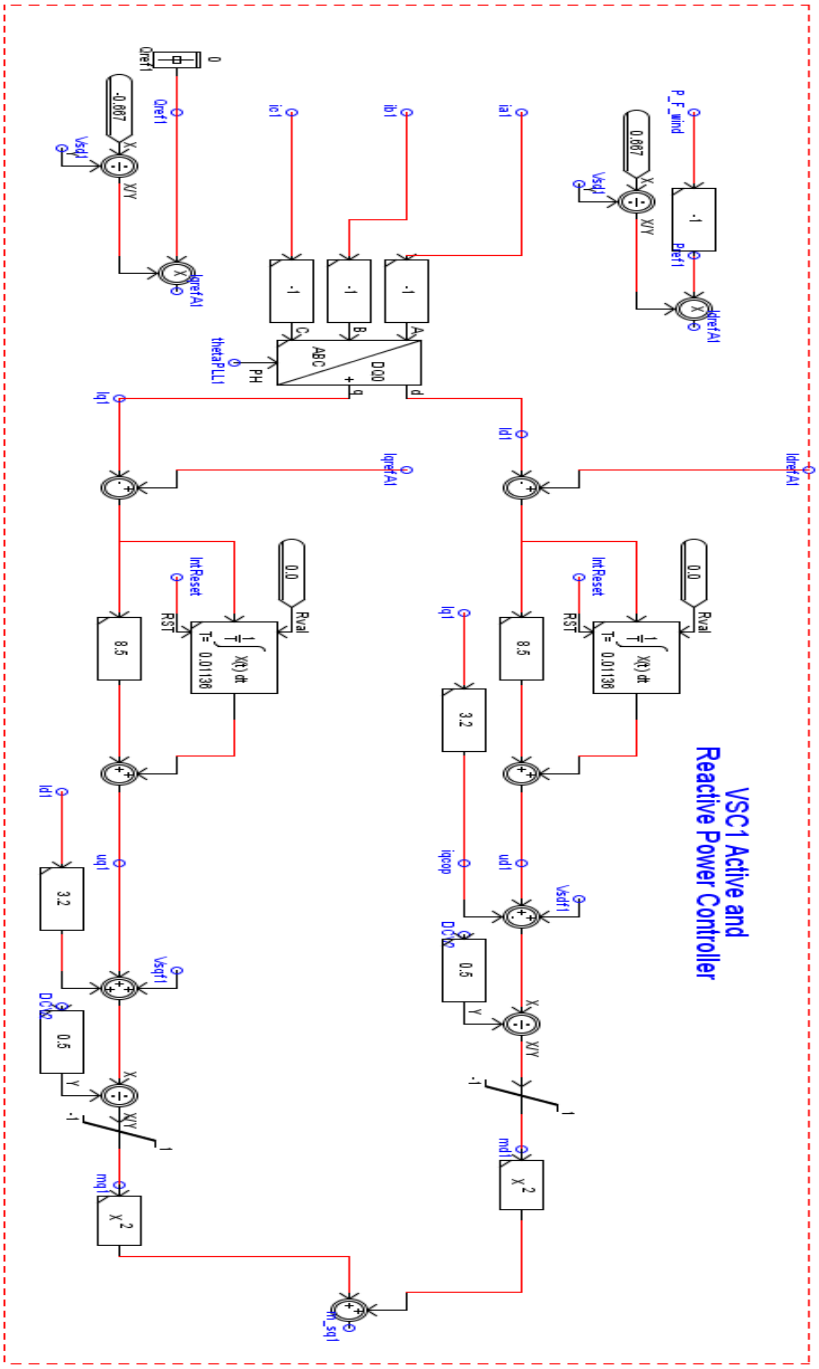

Figure A. 15 Active and Reactive Power Control with VSC1

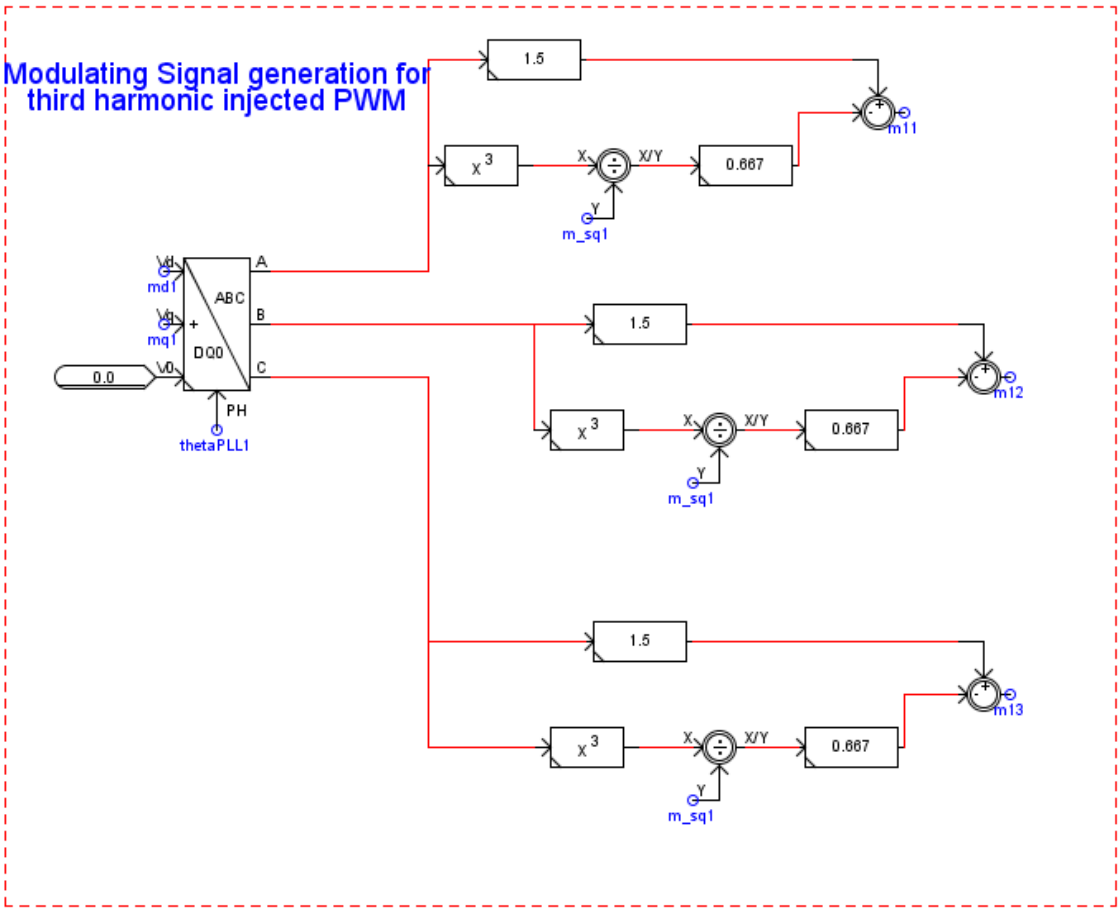

Figure A. 16 Third Harmonic Injective PWM Technique

Modulation signals is transformed to *abc* component from *dq* component as shown in Figure A. **16**. These signals are then used to generated third harmonic injected pulse width modulation signals.

Control diagram for controlling VSC2 is shown in Figure A. **17** using different RSCAD blocks like *abc* to *dq* transformation, slider, gain, integrator, summation, subtraction, multiplication and division.

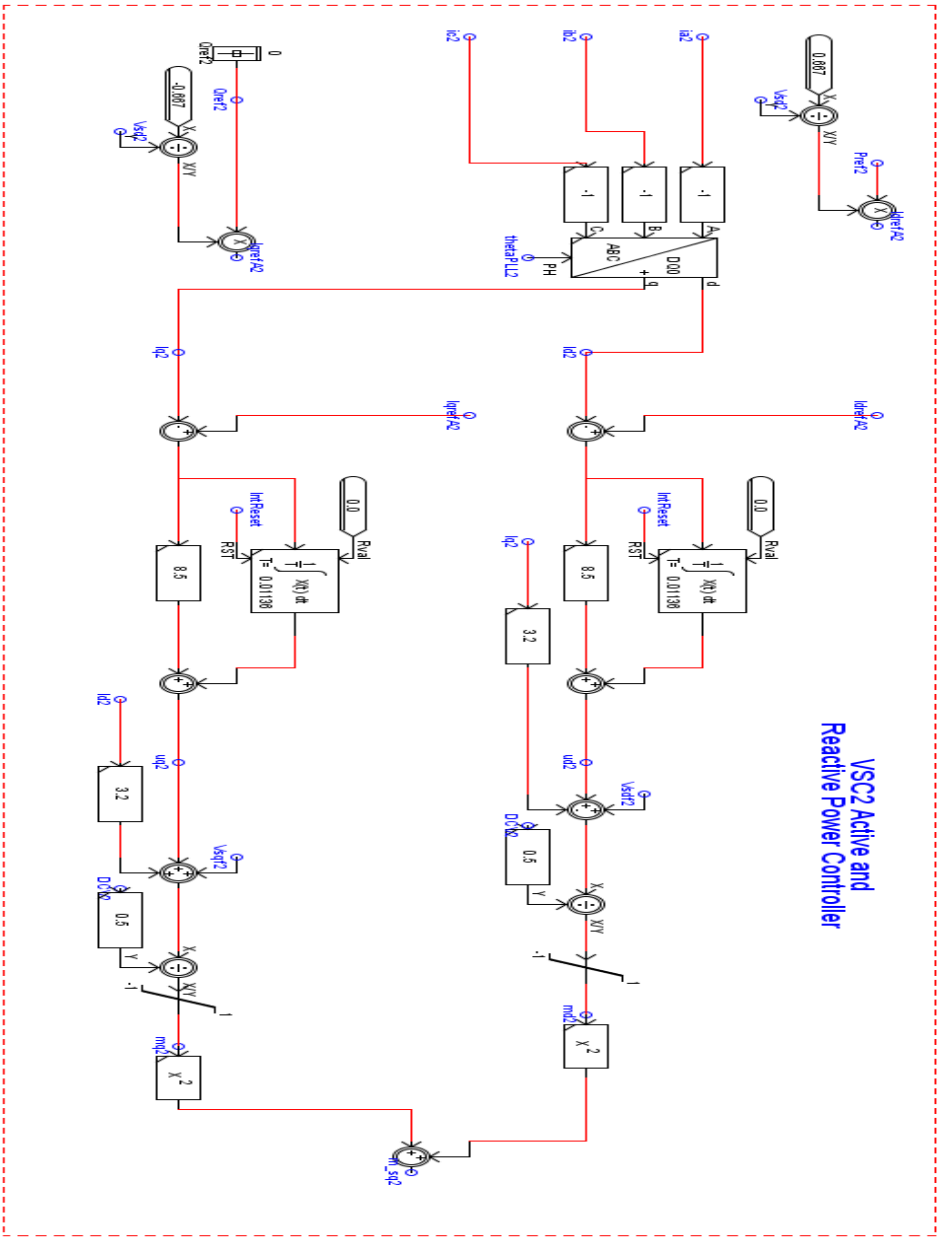

Figure A. 17 VSC2 controller for Active/Reactive Power Control

Implementation of DC link voltage controller for HVDC link is shown in Figure A. **18**

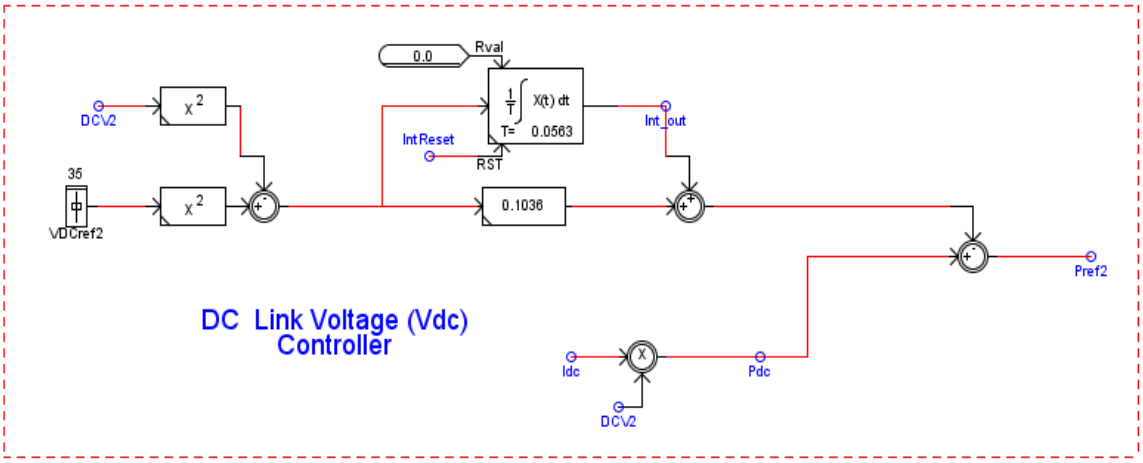

Figure A. 18 DC Link Voltage Control Strategy

Doubly fed induction generator based variable speed wind system is integrated VSC-HVDC as shown in Figure A. **19**. Stator of the induction machine is directly connected to the three winding transformer. Rotor of the machine is connected to the transformer through back to back voltage source converters. All these components of the wind system is implemented in small time step simulation box of RSCAD.

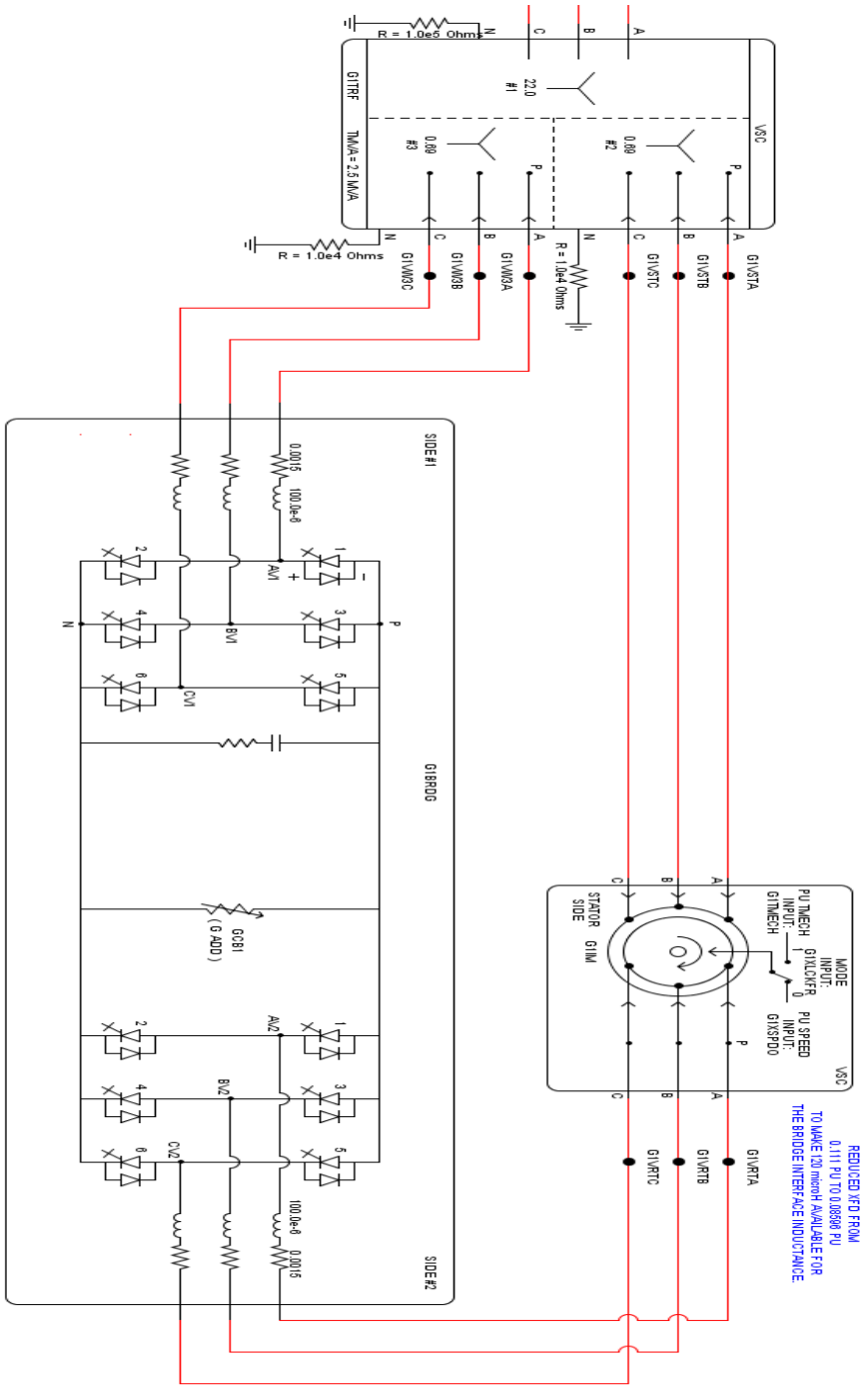

Figure A. 19 DFIG System with Back to Back Converters

Control diagram for stator side voltage source converter is presented in Figure A.20. Measured stator current is transformed from *abc* to *dq*. Voltage at across DC link of wind system and current in *dq* frame is controlled with PI controllers as presented in Figure A.20 below.

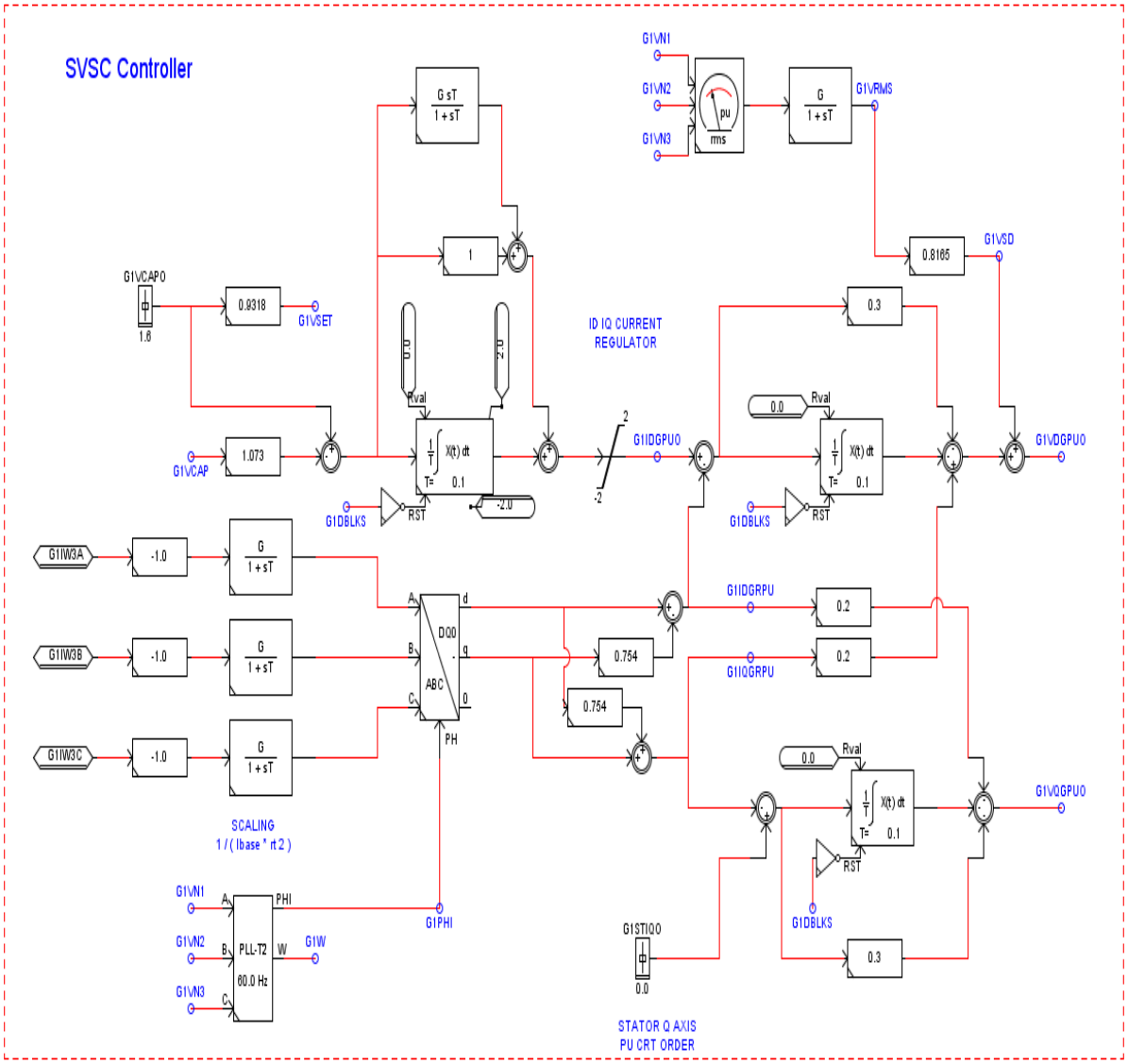

Figure A.20 Development of Controller for SVSC

Rotor side voltage source converter controller is presented in Figure A. **21** with RSCAD.

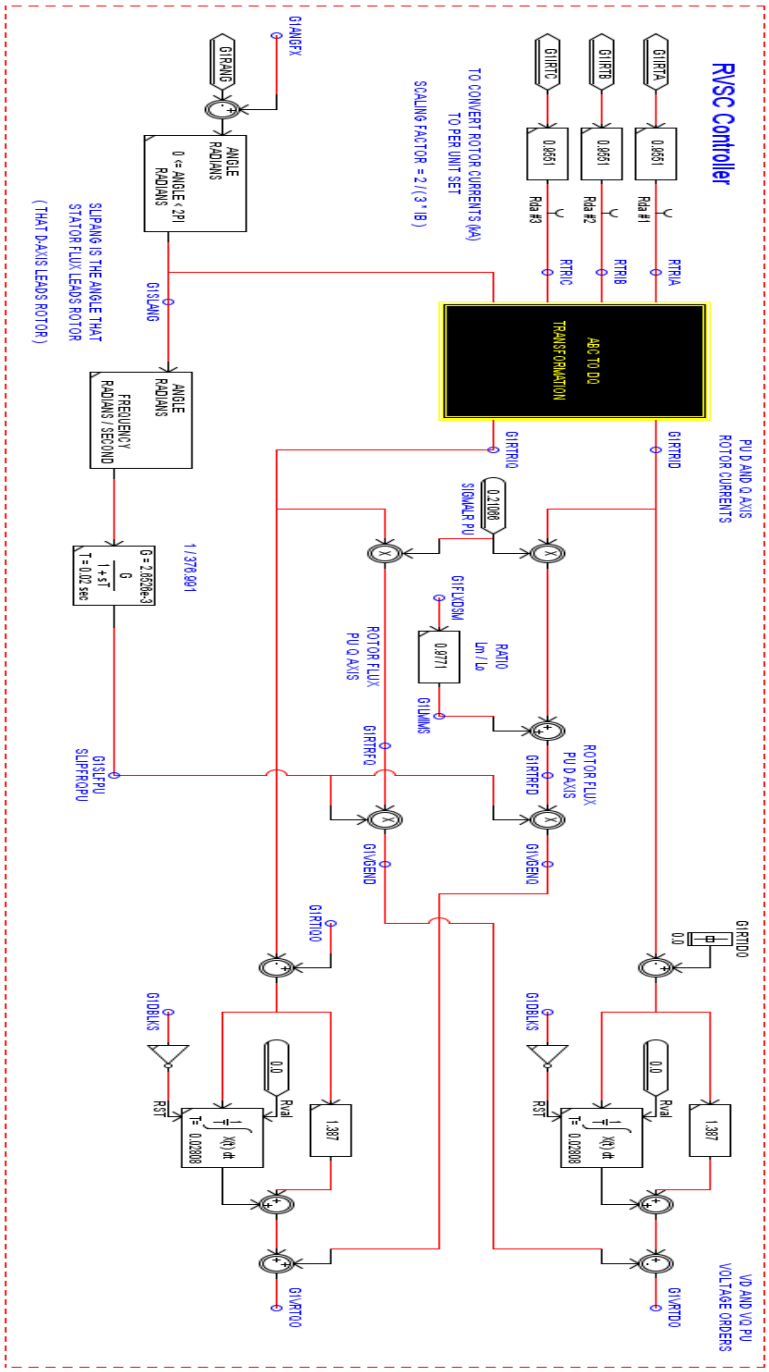

Figure A. 21 Development of Controller for RVSC

Modeling and control of DFIG system wind turbine is shown in Figure A. **22**. Pitch, speed, and torque controllers for wind turbine are developed with several blocks in RSCAD.

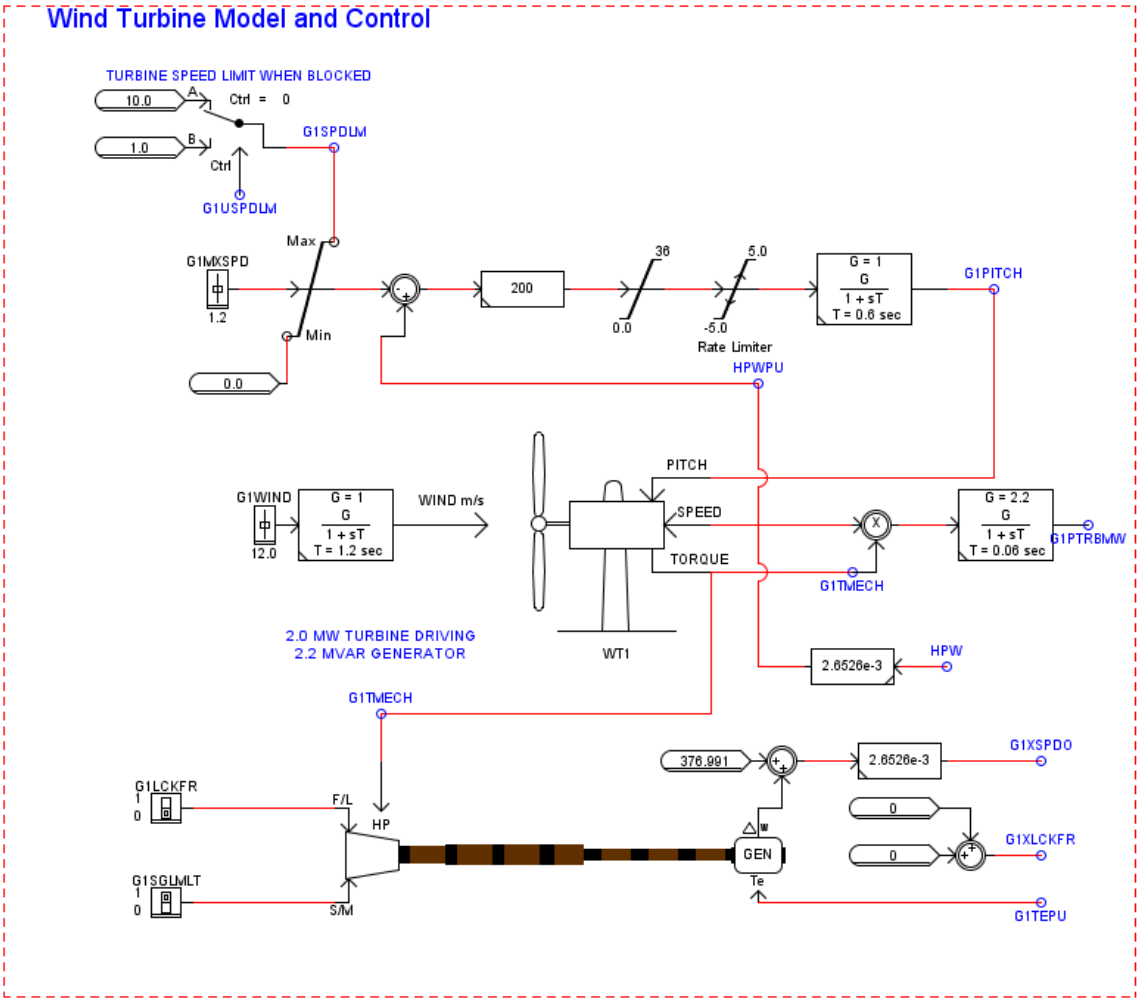

Figure A. 22 DFIG Wind Turbine and Control

Active power and reactive power measurement and filtering blocks are presented in the Figure A. **23**.

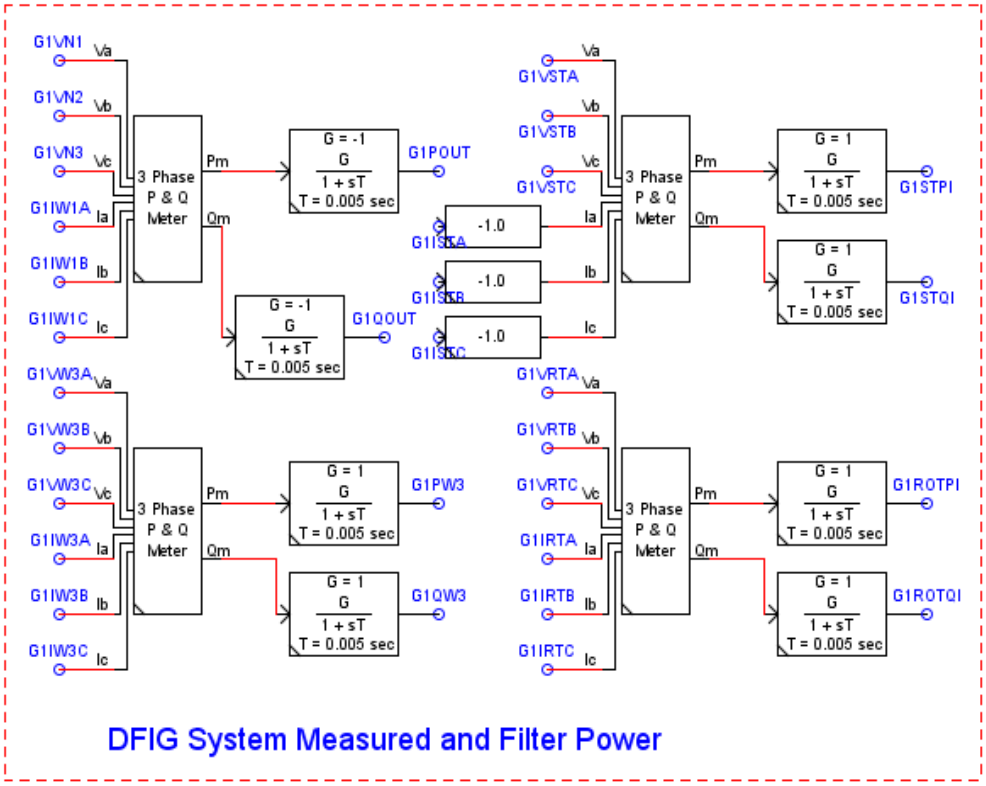

Figure A. 23 Active and Reactive Power Measurement for DFIG System

Variable resistive bridge type fault current limiter is implemented in RSCAD using single phase transformer, three phase diode-bridge, switch, resister and inductor as shown in Figure A. **24**.

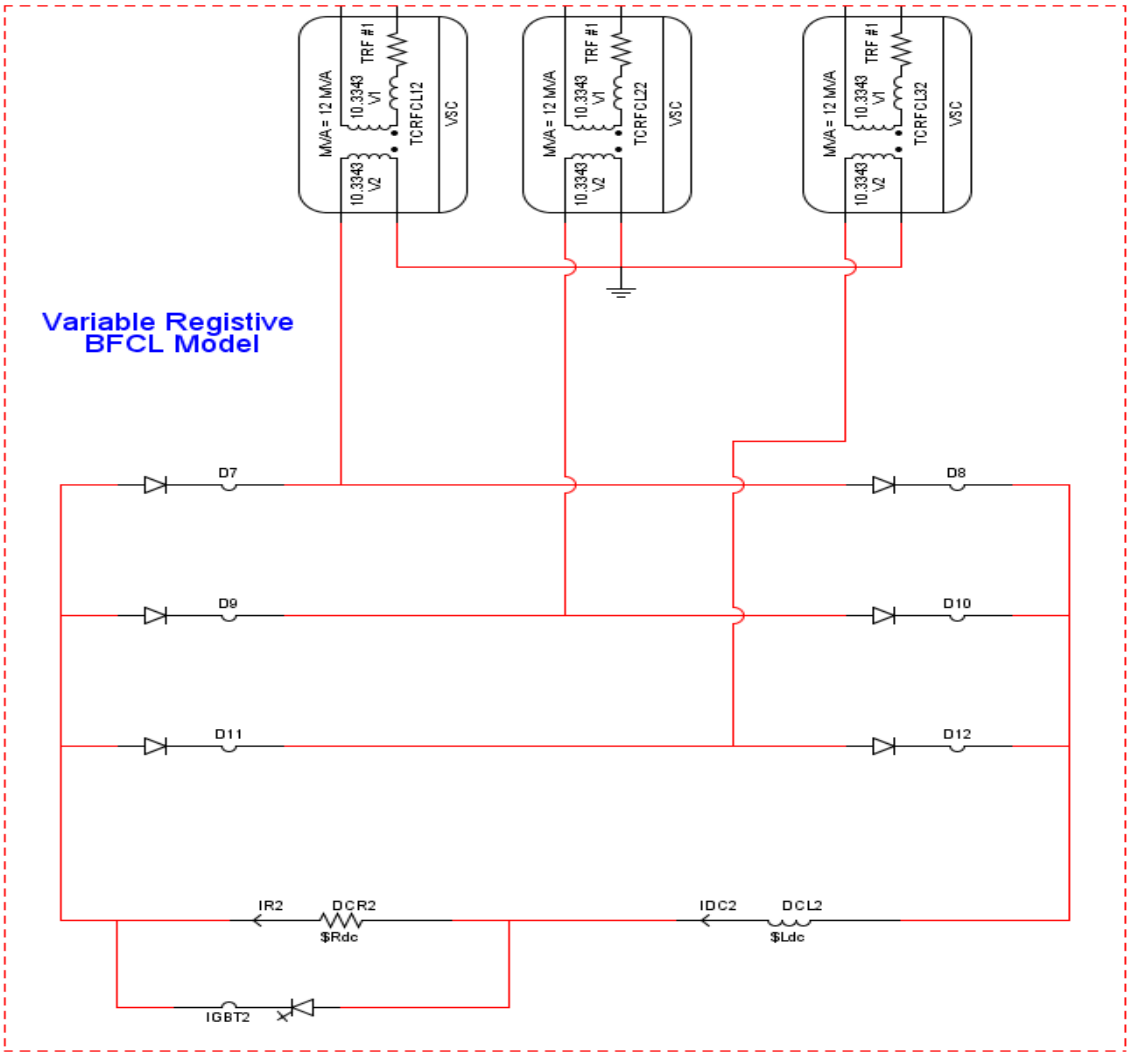

Figure A. 24 Development of VR-BFCL

Overall control structure for non-linear control of VRBFCL based on non-linear equation and point of common coupling current sensing is presented in Figure A. **25**.

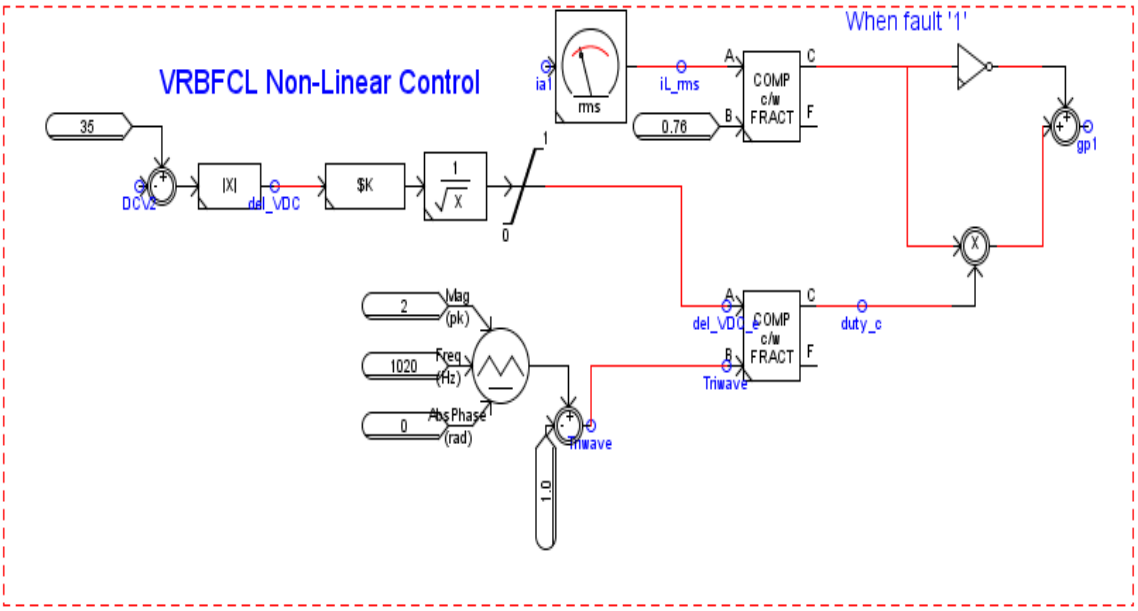

Figure A. 25 Non-linear Control for VR-BFCL

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PUBLICATIONS:

Journal Publications

1. **Md Shafiul Alam**, M. A. Y. Abido, I. El-Amin "Fault Current Limiters in Power Systems: A Comprehensive Review," Energies, vol. 11, no. 5, pp. 1–24, 2018. **ISI** index, **Impact Factor: 2.676**

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