ANFIS-PID HYBRID DIGITAL CONTROLLERS FOR BUCK CONVERTERS

BY

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To my parents, for always supporting me through this.

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LIST OF ABBREVIATIONS

ADC	:	Analog to Digital Converter
ANFIS	:	Adaptive Neuro-Fuzzy Inference System
CMC	:	Current Mode Control
DAC	:	Digital to Analog Converter
DC	:	Direct Current
DPFM	:	Digital Pulse Frequency Modulator
DPWM	:	Digital Pulse Width Modulator
FPGA	:	Field Programmable Gate Array
HDL	:	Hardware Description Language
PID	:	Proportional–Integral–Derivative
SoC	:	System on Chip
VMC	:	Voltage Mode Control

ABSTRACT

Full Name : Umair Ahmad Shaikh

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This dissertation proposes and tests ANFIS- PID hybrid controllers for DC-DC Buck converter for microprocessor applications which require accurate power supplies with low power consumption and fast response. Currently, PIDs are the most common type of control technique associated with buck converters but due to them being tuned towards a specific operating point, they inherently are not able to maintain constant performance across varying loads. ANFIS is a new and upcoming type of control technique based on artificial neural networks and fuzzy control systems. It has proven to be especially effective with varying loads and unpredicted conditions. In this thesis, three classes of ANFIS-PID hybrid voltage mode digital control techniques are proposed: Logical Hybrids, Arithmetic Hybrids, and ANFIS-Driven-PIDs, which are then implemented and tested experimentally on FPGA. The novel Product type arithmetic hybrid is among the proposed controllers. It is shown that utilizing these hybrid techniques can provide various improvements over traditional PID controllers, ranging from better rise time to better light and heavy load operation. Additionally, the use Delta-Sigma converters to alleviate high power consumption issues during low load due to use of high frequency DPWMs is investigated.

ملخص الرسالة

الاسم الكامل: عمير أحمد شيخ

عنوان الرسالة: وحدة تحكم رقمي هجين (ANFIS-PID) للمحول العكسي

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هذه الرسالة تقترح وتختبر وحدات التحكم الرقمية الهجينة (أنفيس) للمحول العكسي (تيار ثابت – تيار ثابت) لتطبيقات المعالجات الدقيقة التي تتطلب إمدادات طاقة دقيقة مع استهلاك طاقة منخفض والاستجابة السريعة. حاليا، وحدة التحكم التناسبية التكاملية التفاضلية هي النوع الأكثر شيوعا للتحكم بالمحولات العكسية لكن نظرا لضبطها نحو نقطة تشغيل محددة، فإنها بطبيعتها ليست قادرة على الحفاظ على أداء ثابت عبر الأحمال المتفاوتة. أنفيس هو نوع جديد وقادم من تقنية التحكم الذي يعتمد على الشبكات العصبية الاصطناعية وأنظمة التحكم المضببة. قد تم إثبات أن هذه التقنية فعالة خاصة مع الأحمال المتفاوتة والظروف الغير متوقعة. في هذه الرسالة، تم اقتراح ثلاث فئات من تقنيات التحكم الرقمي الهجين للجهد عن طريق وحدة تحكم أنفيس: التقنية الهجينة المنطقية، التقنية الهجينة الرياضية، ووحدة تحكم تناسبية تكاملية تفاضلية يتم التحكم بها عن طريق أنفيس. هذه التقنيات تم اختبارها وتطبيقها عملياً على مصفوفة البوابات المنطقية القابلة للبرمجة. تشير الرسالة أن استعمال هذه التقنيات تعطي نتائج وأداء أفضل من وحدات التحكم التقليدية بدءاً من سرعة الأداء إلى تحمل الأحمال المختلفة. وبالإضافة إلى ذلك، يتم التحقيق في استخدام محولات دلتا سيغما للتخفيف من ارتفاع استهلاك الطاقة القضايا أثناء الحمل المنخفض بسبب استخدام تقنية النبض الرقمي متغيرة العرض عالية التردد.

CHAPTER 1

INTRODUCTION

1.1 Motivation

With the invention of the transistor, equipment size started to greatly reduce in size. Large and bulky vacuum tubes could be replaced now with small, lightweight, and highly efficient transistors. Additionally, these transistors could be integrated together in a single circuit to further miniaturize technology. Starting with bipolar junction transistors to field effect transistors; metal-oxide field effect transistors reducing from being several micrometers in length to currently only tens of nanometer long, technology has continued to reduce in size with a rapid pace, thus requiring continuous innovation in the numerous associated fields of study.

With technology becoming smaller as lower process nodes are achieved, it has become required for entire computers or other advanced and sophisticated electronic circuits to be integrated into a single chip. This integrated circuit is referred to as a system on a chip. Manufacturing system-on-chip designs is cheaper than having separate components [1]. Such tight integration also allows for lower power consumption and more optimized designs. System-on-chips are highly popular in mobile electronics applications. They typically consist of a processing core, memory, clock modules, digital and analog interfaces and power circuitry as seen in Figure 1.1 [2]. The focus of this thesis is the voltage regulator in the power module.

Voltage regulation is required on system-on-chips since the board voltage, typically 3.3 V, is always higher than the internal operating voltage, typically 1.2 V, for CMOS technology ranging between 55 to 90 nm [3]. The type of regulators employed in system-on-chips are switching DC-DC converters due to their very high efficiency and lack of power loss as heat, in comparison to linear regulators [4]. Buck, Boost, and Buck-boost are the three most common types of switching DC-DC converters. In system-on-chips, Buck-type switching regulators are used to convert the high board power to lower on-chip power.

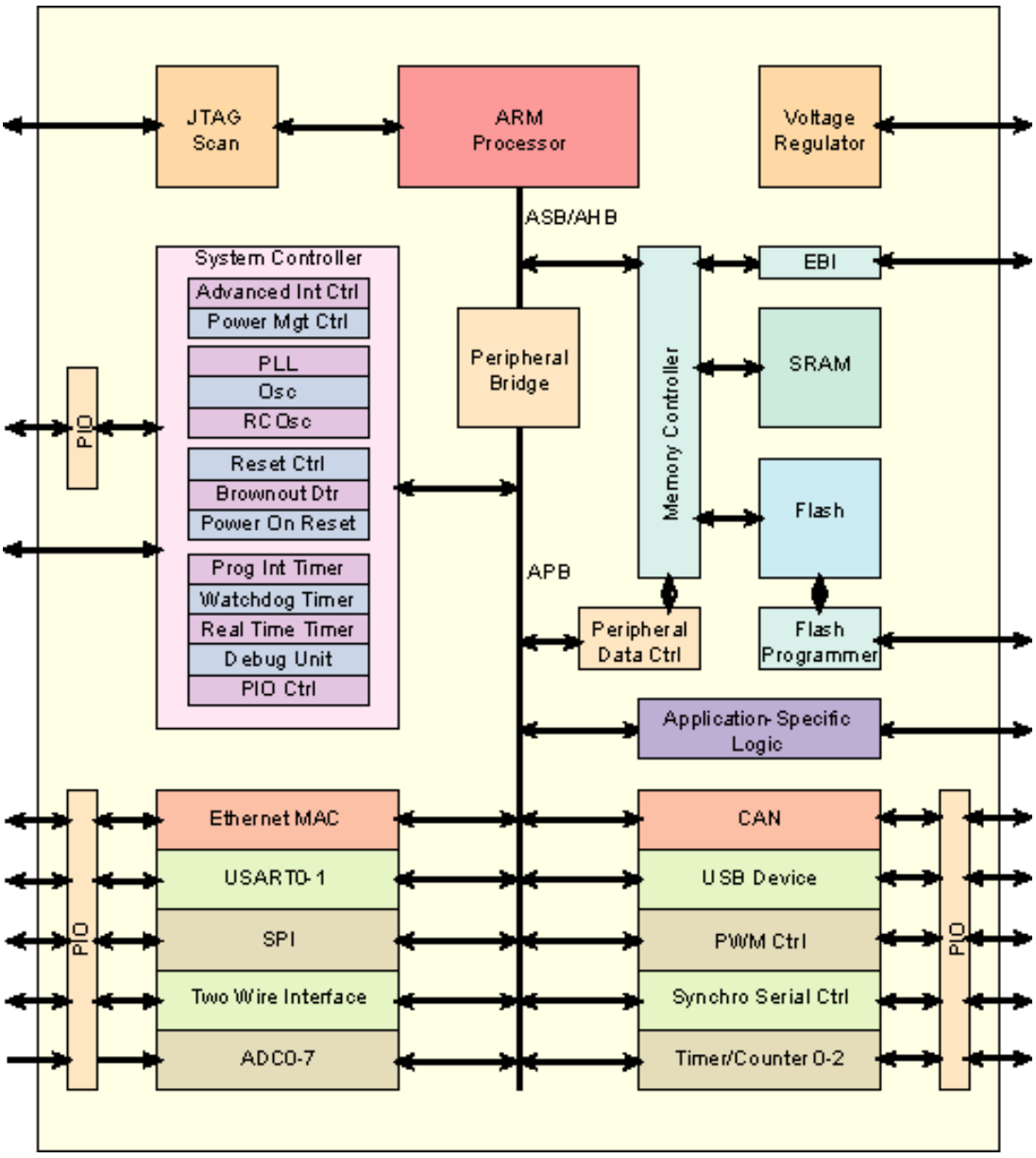


Figure 1.1: Typical block diagram for System-on-Chips

1.2 Research Goals

A typical System-on-Chip (SoC) requires a high efficiency buck-type DC-DC Converter with fast and accurate response. The converter should be able to handle variable current draw to different load conditions of the in-system microcontroller or microprocessor. High efficiency is required so that the buck converter can be utilized for low power applications.

This thesis proposes new hybrid ANFIS-PID digital designs for buck control based on various arithmetic and logical operations. A hybrid controller with adaptive PID coefficients is also put forward. These new controllers are optimized for SoC applications and thus provide fast and accurate response while consuming relatively small power compared to conventional control methods. The controllers are also verified with various Digital-to-Analog converter types to optimize the buck converter's overall power consumption.

1.3 Thesis Overview

This chapter, INTRODUCTION, presents the motivations behind this research, the objectives and the organization of the thesis. Chapter 2. LITERATURE REVIEW, provides background on buck-type DC-DC converters, their typical architecture, and the various control techniques currently used. Novel hybrid control techniques based on ANFIS and PID controllers are presented and described in Chapter 3, HYBRID ANFIF-PID CONTROL FOR BUCK CONVERTERS. Chapter 4, SIMULATION AND EXPERIMENTAL RESULTS, presents simulation and experimental results for the presented novel controllers. The results are also compared against conventional controllers. Finally, in Chapter 5, CONCLUSION AND FUTURE WORK, a summary of the thesis is provided along with the recommended future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Switching power supplies usually consist of the power stage and the controller. The controller switches on the power stage at a certain frequency to increase or decrease the output voltage. Depending on the configuration of the power stage, boost, buck, or buck-boost converters can be obtained. A boost converter steps up the input voltage to a higher level. A buck converter steps down the voltage to a lower level. A buck-boost converts to either a higher or lower voltage level. Buck converters are the focus of this thesis.

The following sections in this chapter will describe the structure of a typical buck converter and gives a brief overview and comparison of the various digital control techniques and the digital to analog converters used with them present in literature.

2.2 Buck Type (Step-Down) DC-DC Converters

The buck converter's operation is dependent on two switches. These switches are connected to an inductor and a capacitor. The switches allow the inductor to be active and store energy which is then discharged into the capacitor and the load. When the inductor is charging, the capacitor discharges to supply the load [5]. The switching is governed by a

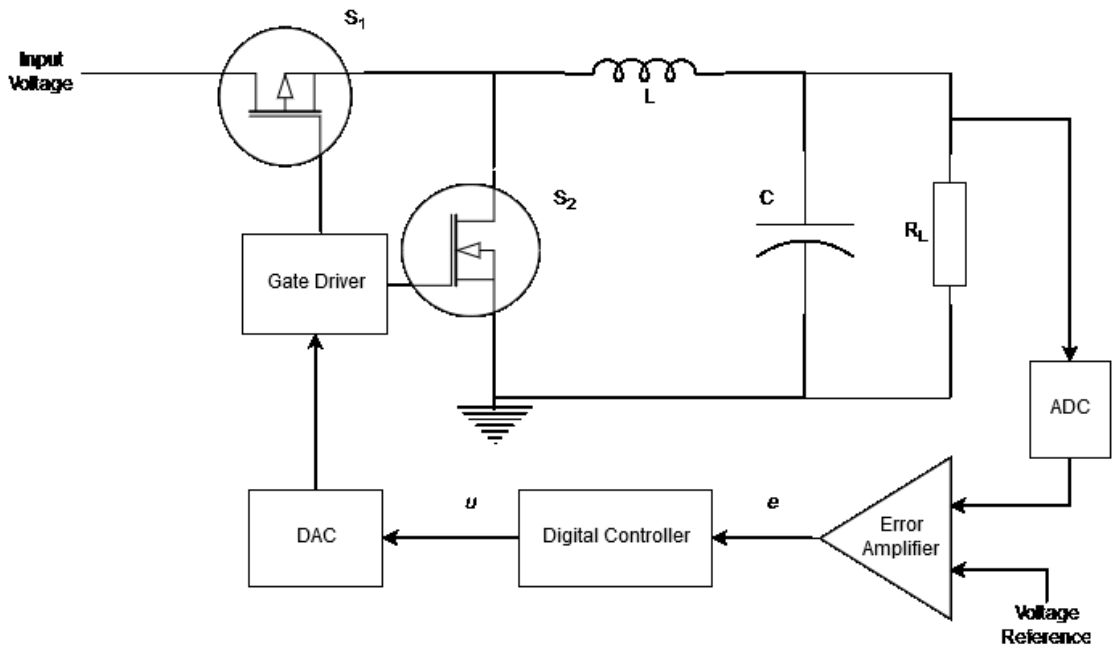


Figure 2.1: Typical structure of a digitally controlled buck converter

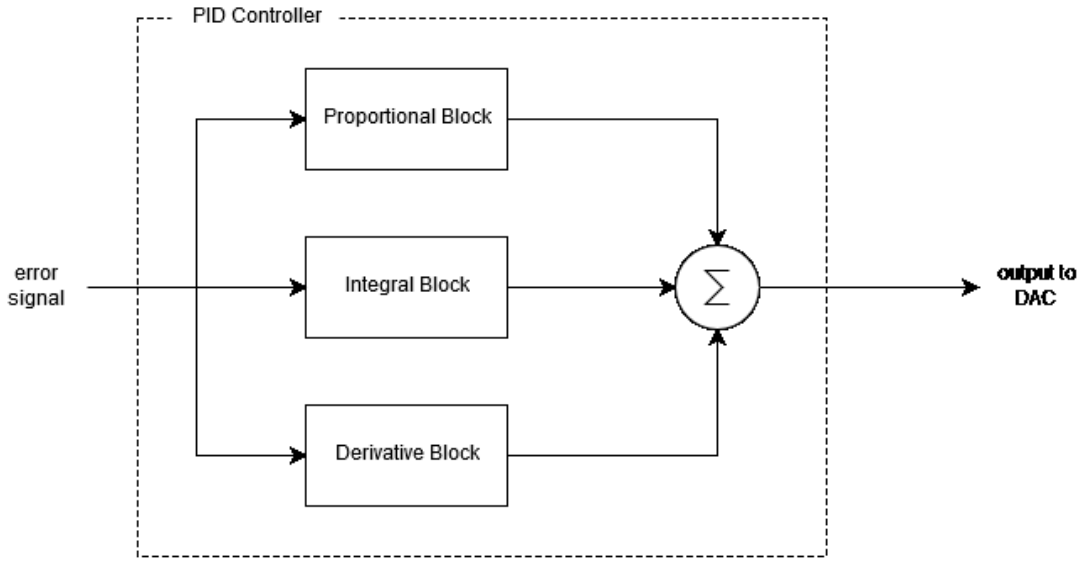
controller. The controller varies the length of the charge and discharge cycles thus varying the output voltage level based on the current output reading. The typical structure of a buck converter is given in Figure 2.1. In the diagram, S_1 and S_2 are the high and low side switches respectively, L the inductor, C the capacitor, and R_L the load.

Analog buck converters utilize an error amplifier and an analog controller to generate the switching signal. For digital buck converters, analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are used by the digital controller to sense the output voltage and generate the switching signal respectively. This is basically a negative feedback loop for voltage mode control (VMC). When using current mode control (CMC) is used to control the switching, a sensing element is used to sense the inductor current and is used instead. [6] This thesis focuses on VMC.

2.3 Digital Control Techniques for Buck Converters

Digital controllers have become extremely popular and have garnered widespread attention of researchers. This is due to the advantages digital controllers present over analog controllers, such as, ease of programmability, component variation immunity, lower complexity for complex control techniques, etc. [7]. A digital controller in a buck converter for voltage-mode control typically takes the output voltage reading of the buck converter from an ADC and changes the switching signal outputted to the DAC accordingly.

(a)



(b)

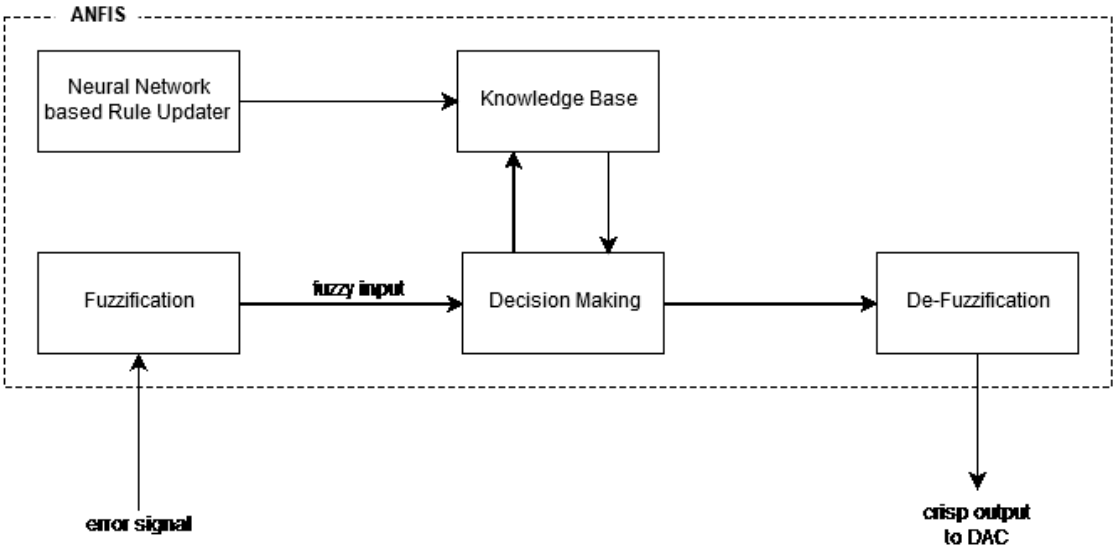


Figure 2.2 Typical structure of a (a) PID controller (b) ANFIS controller

Conventional controllers using type-II compensators are quite limiting in their performance [7]. More recently, they have been replaced with the popular discrete-PID (Proportional-Integrative-Derivative) controllers due to their robustness, simplicity, and performance. Extensive work has been done into PIDs which determines the degree of the proportional, integrative, and derivative gains for the controller which are tuned to obtain the required response from the controller. The typical structure of the PID controller is given in Figure 2.2 (a).

An alternative to PID controllers are Fuzzy controllers. When linked to artificial neural networks, we get Adaptive Neuro-Fuzzy Inference System (ANFIS) controllers. These controllers automatically adjust their parameters in real time for optimum control and are preferred for their performance under variable conditions. The typical structure of a ANFIS controller is given in Figure 2.2 (b).

Table 2.1. compares these two alternative control techniques. As can be seen, the PID controller displays a better settling time by 14% and a better rise time by 25%. On the other hand, the ANFIS exhibits absolutely no overshoot compared to the PIDs 12.5 %.

Table 2.1: Comparison between simple digital control techniques in [8], 2013

Controller Type	Overshoot (%)	Settling Time (s)	Rise Time (s)	Error (%)
PID Controller	12.5	0.6	0.3	0
ANFIS Controller	0	0.7	0.4	0

2.4 Digital Hybrid ANFIS-PID Controllers

Hybrid controllers combine the advantages of the PID and ANFIS controllers. Such hybrids controllers found in literature can be divided into three types. The first type consists of the output of the two-individual controller being combined through way of an adder. This hybrid control technique is covered in [8] and [9] for motor speed control and has yet to be brought to buck converters. Similarly, the second type does the same through use of a selection block. As with the summing controller type, this hybrid is covered in [8] and [9] for motor speed control and has yet to be brought to buck converters. The third and last hybrid controller uses the ANFIS as an auto-tuning module for the PID. Similar hybrids using ANFIS and PD controllers and Fuzzy and PID controllers are shown in [10] and [11] respectively. [12] utilizes a Fuzzy with PID hybrid for the same.

Table 2.2 compares between the hybrids found in literature. As can be seen from the table, ANFIS driven PD hybrids typically show better transient performance but lag in steady-state performance when compared to their summing and selecting hybrid counterparts.

Table 2.2: Comparison between hybrid control techniques found in literature

Reference	Controller Type	Overshoot (%)	Settling Time (s)	Rise Time (s)	Error (%)
[10], 2013	Summing Hybrid	75	1.40	0.20	0
[10], 2013	Selecting Hybrid	5	0.55	0.30	0
[11], 2014	ANFIS driven PD	0	0.007	0.005	1
[12], 2008	Fuzzy driven PID	50	0.016	0.002	0

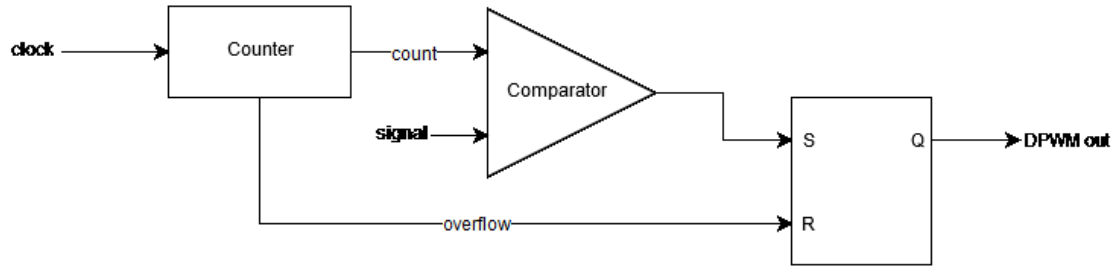
2.5 DPWM, DPFM, and Delta-Sigma Converters

The output of any digital controller in a buck converter is required to be passed through a single bit digital-to-analog converter before it can be utilized to control the switches as described in Section 2.2. This DAC can be one of many types. The most commonly used converter is the Digital Pulse Width Modulator (DPWM). It is preferred due to its fast-transient response, high efficiency at low load, and ability to operate at high frequencies, thus requiring smaller inductors and capacitors [13] [14]. All the controllers mentioned in Section 2.4 utilize this type of DAC. A few recent controllers also utilize DPWM in conjunction with Pulse Frequency Modulation (PFM) for low load or low power applications [15] [16]. Digital-PFM (DPFM) are used for the digital domain [17].

Current DPWM structures that can operate at high frequencies, have undesirable harmonic spike dues their power spectra concentrated around their switching frequency. [18] Solving this issue give rise to high switching losses and consume a lot of current thus lowering the buck converter efficiency [19]. Utilizing DPFM causes supply integrity issues due to changing output spectrum [20]. Using Delta-Sigma ($\Delta\Sigma$) modulators reduces non-idealities and errors associated with DPWMs and reduces power consumption [21]. Moreover, it has been seen that using Delta-Sigma modulators can give to improved controller performance compared to DPWMs [22].

Conventional DPWM, and $\Delta\Sigma$ modulator structures are shown in Figure 2.3.

(a)



(b)

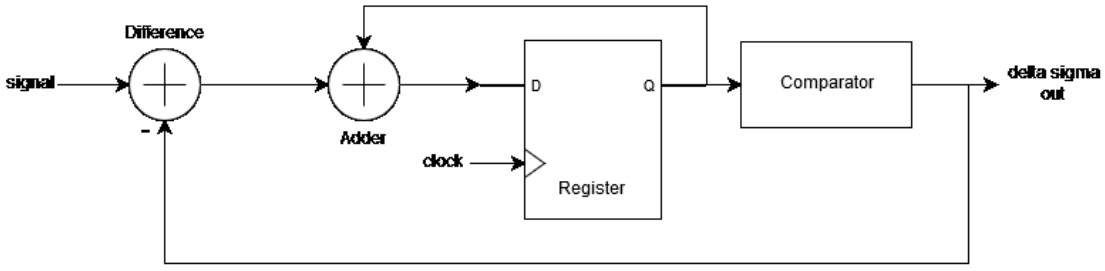


Figure 2.3: Conventional digital architectures for (a) DPWM (b) ΔΣ Modulator

CHAPTER 3

HYBRID ANFIS-PID CONTROL FOR BUCK CONVERTERS

3.1 Introduction

In theory, hybrid control techniques allow for the benefits of individual controllers to be taken advantage of without the drawbacks. This thesis focuses on hybrids between the two most promising control techniques, PID and ANFIS. The objective is to leverage the PID's robustness and the ANFIS's flexibility for a low power buck converter. The following sections will give an overview on these two control techniques and then cover existing and propose new hybrid controllers.

Most hybrid controllers can be divided into two branches:

- Logical Hybrids
- Arithmetic Hybrids

As their names suggest, these hybrid controllers simply perform the respective type of operation involving the outputs of the two individual controllers. Based on the operation, certain response characteristics can be boosted or even suppressed.

3.1.1. PID Control

As mentioned in the previous section, nowadays Discrete PIDs are the most commonly used digital control technique when dealing with buck converters. They can offer robustness and easy implementation.

Like most controllers, PID's input consists of an error signal which is used to generate proportional, integral, and derivate signals. These are summed to generate the switching signal. The PID controller works using the relation given in (3.1).

$$u = K_p e + K_i \int e dt + K_d \frac{de}{dt} \tag{3.1}$$

where:

u: controller output

e: controller input

K_p, K_i, K_d: PID constants (proportional, integral, derivative)

To discretize the above relationship for implementation of a digital PID: [23]

$$\frac{du}{dt} = K_p \frac{de}{dt} + K_i \frac{d}{dt}\left(\int e dt\right) + K_d \frac{d^2 e}{dt^2} \tag{3.2}$$

$$\frac{du}{dt} = K_p \frac{de}{dt} + K_i e + K_d \frac{d}{dt}\left(\frac{de}{dt}\right) \tag{3.3}$$

Replacing the $\frac{d}{dt}$ with its discretized equivalent $\frac{\Delta}{T_S}$:

$$\frac{\Delta U}{T_S} = K_p \frac{\Delta e}{T_S} + K_i e + K_d \frac{\Delta}{T_S}\left(\frac{\Delta e}{T_S}\right) \tag{3.4}$$

$$\Delta U = K_p \Delta e + K_i e T_S + K_d \Delta\left(\frac{\Delta e}{T_S}\right) \tag{3.5}$$

Given that the change in error samples can be represented as:

$$\Delta e = e_n - e_{n-1} \tag{3.6}$$

$$\Delta(e_n - e_{n-1}) = (e_n - e_{n-1}) - (e_{n-1} - e_{n-2}) \tag{3.7}$$

$$= e_n - 2e_{n-1} + e_{n-2}$$

and that the change in the output samples can be represented as:

$$\Delta U = U_n - U_{n-1} \tag{3.8}$$

Substituting (3.6) and (3.8) into (3.5):

$$U_n - U_{n-1} = K_p(e_n - e_{n-1}) + K_i e T_S + K_d \Delta(e_n - e_{n-1}) \tag{3.9}$$

Further substituting (3.7) into (3.9):

$$U_n - U_{n-1} = K_p(e_n - e_{n-1}) + K_i e T_S + K_d(e_n - 2e_{n-1} + e_{n-2}) \tag{3.10}$$

Note that T_S is the sampling time.

PID controller's parameters are typically regulated using Zeigler-Nichols method. This method allows for rapid gain and controller response tuning while remaining in the acceptable range. [23] Although quick, the Zeigler-Nichols method does not return optimal coefficients. Determination of optimal parameters is quite difficult [24]. Additionally, PID controllers are inherently linear and their performance with non-linear system varies.

Due to the simplicity of the discrete PID controller's equation, it can be implemented quite easily using HDL (Verilog or VHDL). MathWorks MATLAB offers a ready-made block of Discrete PIDs for simulation purposes.

3.1.2. ANFIS Control

As mentioned in the previous sections, ANFIS controllers are essentially fuzzy logic controllers linked to neural networks. Due to the learning capabilities of the neural network, controller parameters are adjusted in real time for optimum control. This control technique is quite general and can be applied to more than one type of DC-DC converter.

The architecture of the ANFIS utilized is based on the Sugeno Model consisting of five layers, two inputs, and one output. The inputs are first fuzzified and then using an internal rule knowledgebase, are defuzzified. Each rule has a weight determining its priority. With training, the rules and weights can be determined and adjusted to obtain the desired controller response and minimize the error. A first order Sugeno model can be expressed as follows: [25]

If inputs e is A_1, e is B_1; then output is u_1,

If inputs e is A_2, e is B_2; then output is u_2,

Then output $u = w_1u_1 + w_2u_2$

Where A and B are the fuzzified inputs and w is the determined weight. The function of each of the Sugeno layers is given below. [8][10][26]

Layer 1

Every node in this layer uses membership functions which uses the Sugeno input directly and is evaluated at that point. The membership functions utilized are triangular-shaped membership functions. The triangular curve depends on three scalar parameters a, b, and c and can be expressed using the following piecewise expression:

$$f(x;a,b,c,) = \begin{Bmatrix} 0, & x \leq a \\ \frac{x-a}{b-a}, & a \leq x \leq b \\ \frac{c-x}{c-b}, & b \leq x \leq c \\ 0, & c \leq x \end{Bmatrix} \tag{3.11}$$

A typical set of triangular membership functions can be seen in Figure 3.1 [27].

Layer 2

In this layer, the product of every membership function output from the previous layer is taken. This layer gives a fuzzified output for each input to the Sugeno-type ANFIS system.

Layer 3

This layer determines the applicable normalized weight of each rule for the outputs from Layer 2. Essentially, this layer is comparing the rules from the ANFIS's knowledgebase for the current input set.

Layer 4

Here, the weights from the previous layer are taken in as parameter. If the previous layer was comparing the rules, this layer can be said to apply the determined rules.

Layer 5

This layer is a summation layer. The outputs of the previous layer are summed and passed through membership functions hence defuzzifying them. The output membership function utilized here are again triangular membership functions. The output of this layer is the output of the Sugeno-type ANFIS controller.

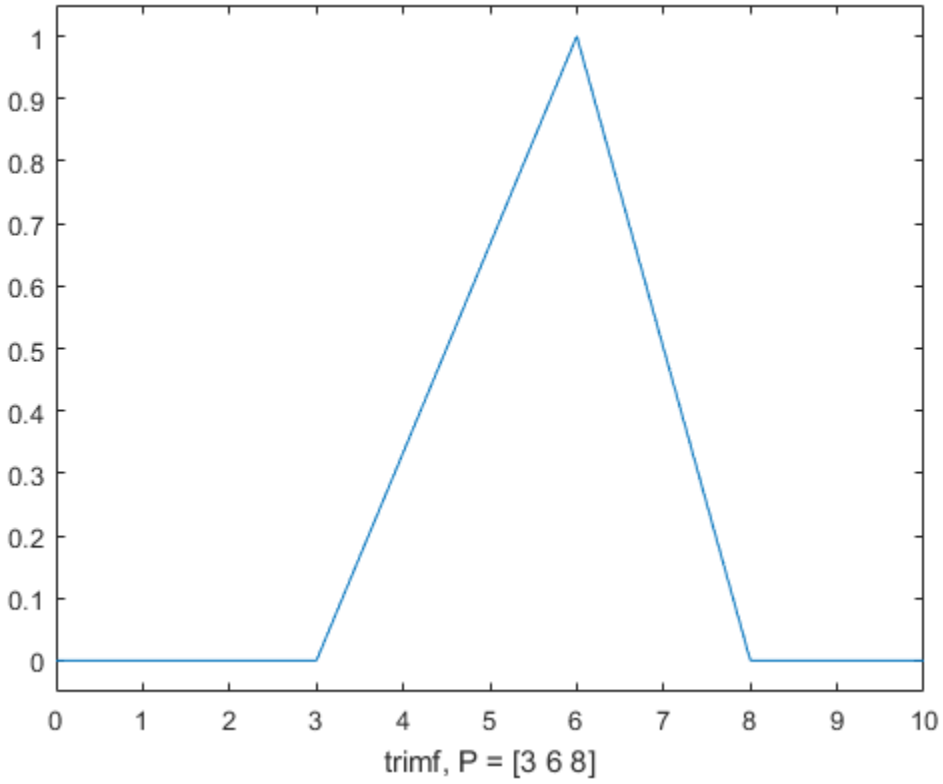


Figure 3.1: Sample of a Triangular Shaped membership function

The ANFIS controller used for buck converters takes two inputs: the error signal and its rate of change and output the required rate of change of the output (duty) to obtained the required voltage regulation. The training data for the ANFIS is obtained from the buck-converters open loop response. The training is used to determine the rules, weights and the membership function parameters. The training is repeated (iterated) till the response error is sufficiently small.

MathWorks MATLAB offers a ready-made block of the Sugeno-type ANFIS controller for simulation purposes. It also allows for training. For experimental implementation on FPGA, a Verilog model with only offline training can be implemented. This can be as simple as implementing a look-up table based knowledgebase with preset data and comparators based input processing.

3.2. Logical ANFIS-PID Hybrid Control

As the name of this class of hybrids suggests, these hybrids use Boolean logic operations to determine the output response of the controller. Each Boolean variable in this calculation could be the output of a more complex calculation. For example, Is inductor current less than i_0?, or Is error less than e_0?

There are two logical hybrid controllers considered as part of this thesis. These are switching controllers that select a single controller's response and output it only. The decision is made based on the magnitude of the error signal. The two logical hybrids are referred to as:

- Switching ANFIS-PID Hybrid Type I
- Switching ANFIS-PID Hybrid Type II

3.2.1. Switching ANFIS-PID Hybrid Type I

This hybrid outputs either one of the two controller outputs depending on the magnitude of the error signal. Its logical operation can be expressed in the Boolean expression given in (3.12) or by a piecewise expression in (3.13). The input C is true if the error signal is below a certain threshold or false otherwise. This threshold can be determined iteratively. The best response was found to be with the threshold at 10% if the steady desired voltage level.

$$U_{HYBRID} = (U_{PID} \wedge C) \vee (U_{ANFIS} \wedge \overline{C}) \tag{3.12}$$

$$U_{HYBRID} = \begin{cases} U_{ANFIS}, & for \quad error > \Delta E_{Error} \\ U_{PID}, & for \quad error \leq \Delta E_{Error} \end{cases} \tag{3.13}$$

This controller leverages the ANFIS's superior response during transient operation of the controller and the PID's during the steady-state. In other words, this hybrid controller should have fast rise times, approximately no overshoot, and robust steady state response but performance with minor disturbances at the input might cause the response to degrade at steady state.

A simple flowchart illustrating the flow of events based on which the controller selects the controller output is shown in Figure 3.2. The block diagram of the controller can be seen in Figure 3.3.

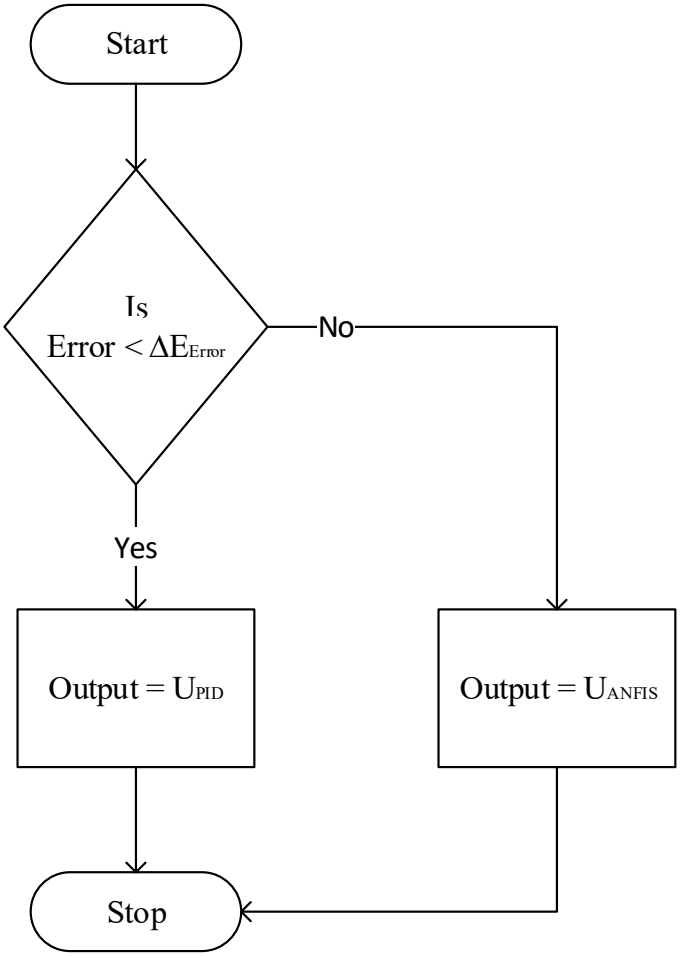


Figure 3.2: Flow chart for Switching ANFIS-PID Hybrid Type I

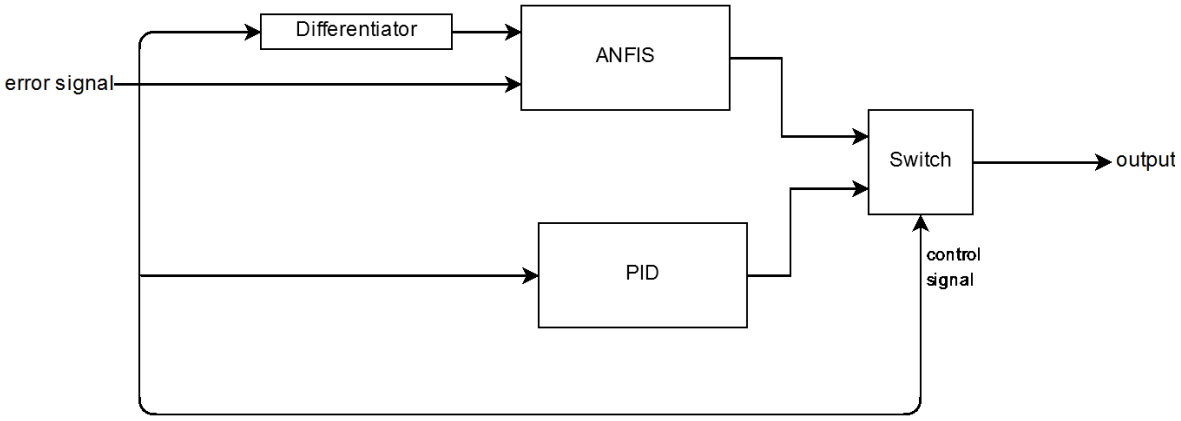


Figure 3.3: Block diagram for the Switching ANFIS-PID Hybrid Type I

3.2.2. Switching ANFIS-PID Hybrid Type II

Like the previously discussed controller, this hybrid outputs either one of the two controller outputs depending on the magnitude of the error signal. Its logical operation can be expressed in the Boolean expression given in (3.14) or by a piecewise expression in (3.15). The input C is true if the error signal is below a certain threshold or false otherwise. This threshold can be determined iteratively. The best response was found to be with the threshold at 10% if the steady desired voltage level. The main difference between this and the hybrid discussed in Section 3.2.1. is that this controller signal reverses the priority that was given in the Type I controller.

$$U_{HYBRID} = (U_{PID} \wedge \overline{C}) \vee (U_{ANFIS} \wedge C) \tag{3.14}$$

$$U_{HYBRID} = \begin{cases} U_{PID}, & for \quad error > \Delta E_{Error} \\ U_{ANFIS}, & for \quad error \leq \Delta E_{Error} \end{cases} \tag{3.15}$$

This controller applies the PID during transient operation and the ANFIS during the steady-state. In other words, this hybrid controller should have much superior steady state performance and disturbance rejection and negligible overshoot during the transient stage.

A simple flowchart illustrating the flow of events based on which the controller selects the controller output is shown in Figure 3.4. The block diagram of the controller is like the Type I illustration which can be seen in Figure 3.3. The only difference is what the control signal would constitute of here.

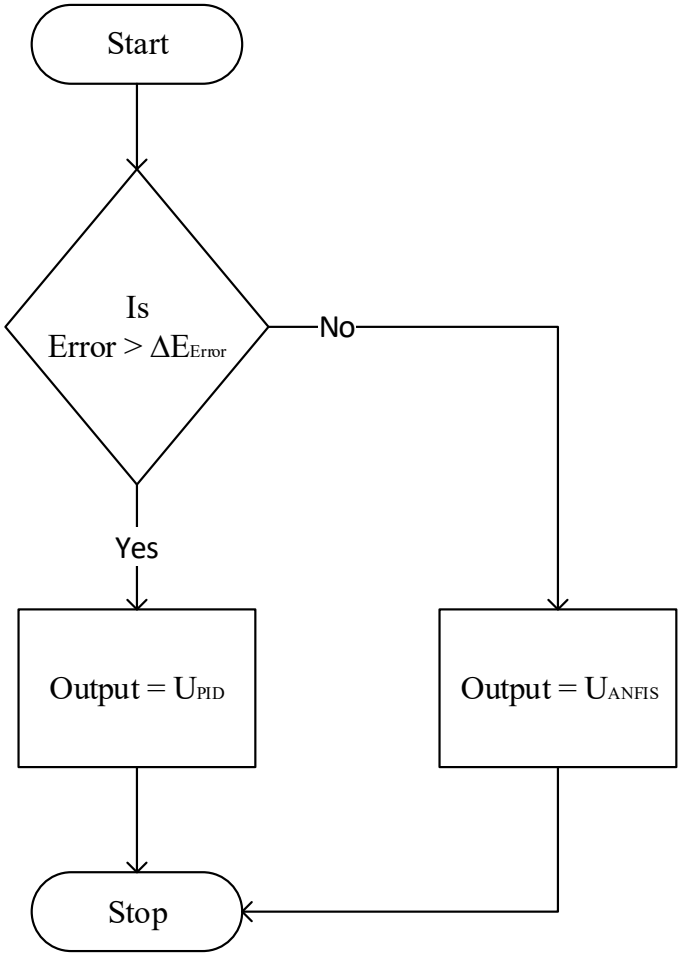


Figure 3.4: Flow chart for Switching ANFIS-PID Hybrid Type II

3.2.3. Theory of Operation

Breaking the desired response of a controller into two pieces, i.e. for large and small error magnitude, allows for a single controller to be optimized for a certain region of operation.

For the PID tuning, the Ziegler-Nichols method is used. For the Switching Type I hybrid, the PID is focused on the steady state operation. Hence, the tuning does not need to consider Overshoot and can be done to maximize disturbance rejection. This can be done by the classical Ziegler-Nichols rule: Kp=0.6Ku, Ki=2Kp/Tu, and Kd=KpTu/8, where Tu is the period of oscillation and Ku is the ultimate gain.

For the Switching Type II hybrid, the PID is focused on transient operation. Hence, the tuning does not need to consider disturbance rejection and can be done to minimize overshoot and optimize settling and rise times. This can be done by the *"Some Overshoot"* Ziegler-Nichols rule: Kp=0.33Ku, Ki=2Kp/Tu, and Kd=KpTu/3.

The ANFIS training remains consistent in either case. The open loop response of the target buck converter setup is used for the training.

3.2.4. Design and Implementation

The controller setups were designed and implemented in two environments for simulation and experimental verification purposes. These are:

- MATLAB Simulink (for Simulation)
- Verilog HDL for FPGA (Cadence IC Suite for Simulation and Experimental)

For MATLAB Simulink, a full buck converter implementation is required which includes the power stage. Therefore, the following structure and blocks were used:

1. The state equations of the converter were used to model an ideal power stage of the buck-converter using Simulink blocks. This model can be seen in Figure 3.5.
2. A Flash-ADC was modelled using the quantizer block set to the respective number of ADC bits and introducing appropriate delays.
3. The controller utilized a Fuzzy-Logic controller block using a pre-trained Sugeno ANFIS system and a parallel Discrete PID. The two controller were combined using a switch block, configured depending on the controller type.
4. Finally, the DAC was based either on a trailing-edge pulse width modulator design, or a second order delta-sigma model.

The entire Simulink model for the buck converter is given in Figure 3.6.

For the Verilog-HDL implementation, the following blocks were used:

1. The controller was implemented using a prioritized decision tree (comparator-based) using offline training data fed into a knowledgebase. The discrete PID was simply the Verilog representation of the PID equation previously mentioned in equation (3.10). The selecting switch was implemented as nested if-else statements. The differentiator was integrated into the ANFIS block.
2. To calculate the error signal, a simple signed adder was used.
3. For the DAC, the DPWM was implemented based on a counter based architecture. A delta-sigma converter was also implemented based on registers and D flip-flops.

The Verilog-HDL schematic block diagram implementation is given in Figure 3.7.

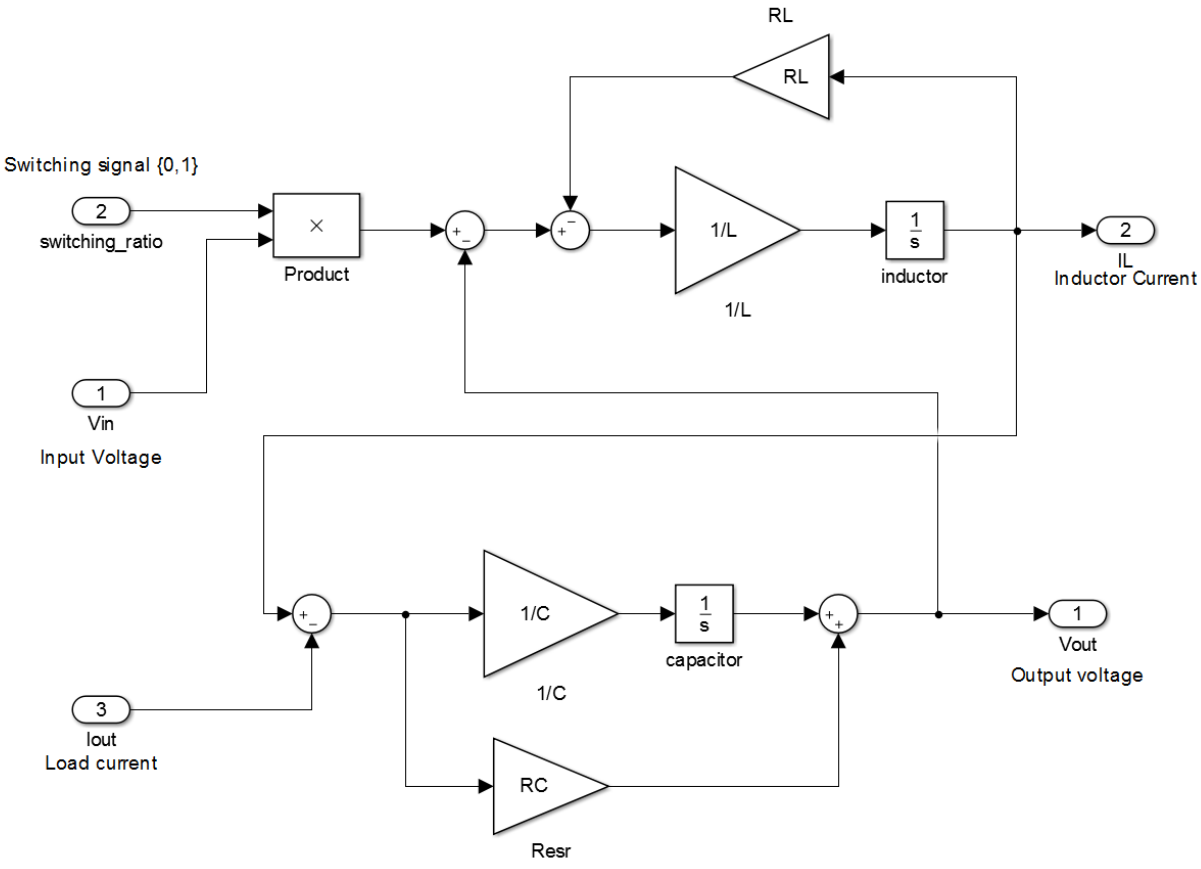


Figure 3.5: Ideal synchronous buck converter model

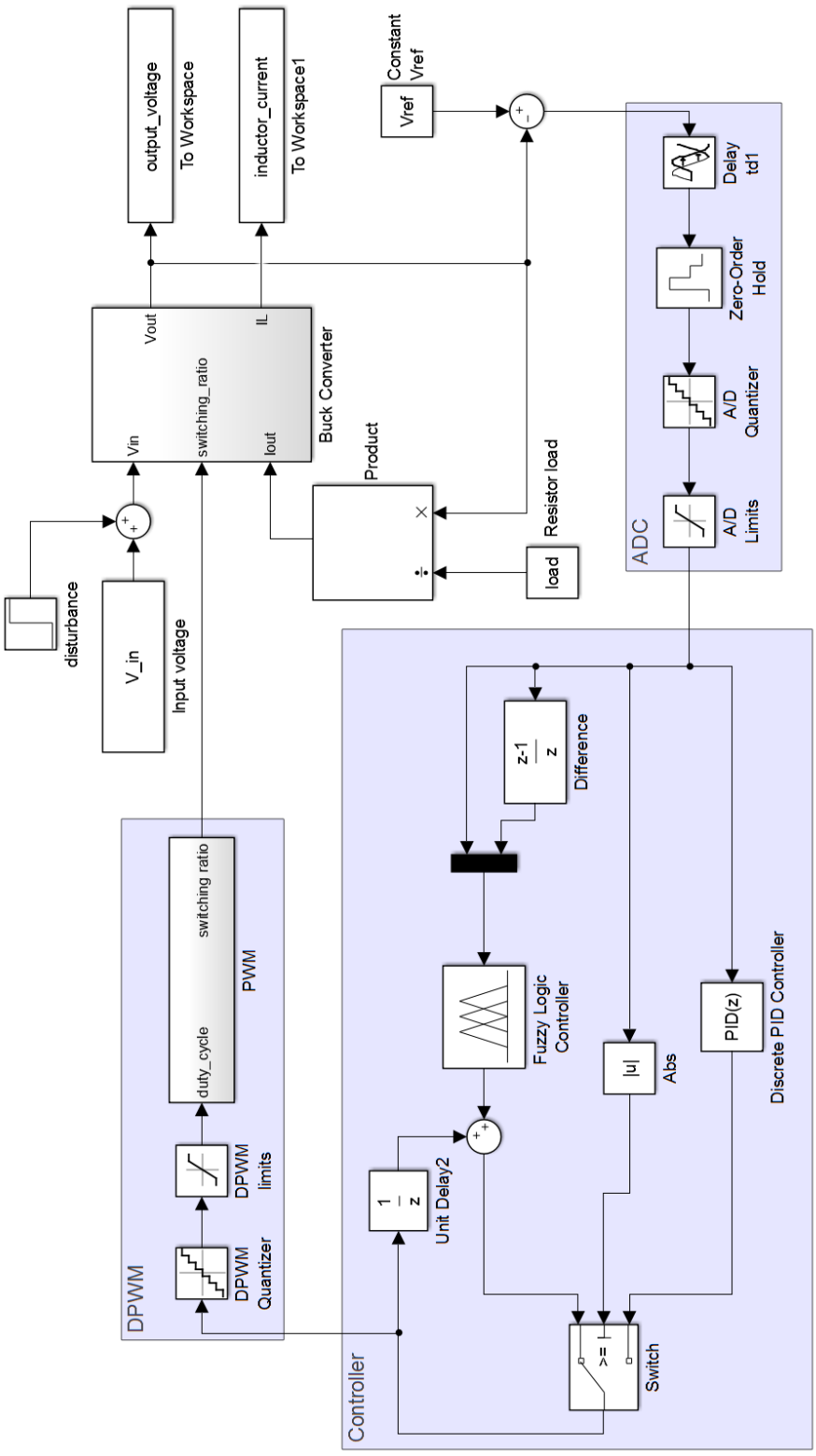


Figure 3.6: Simulink model for the synchronous buck converter with the Selecting ANFIS-PID Hybrid Type I Controller

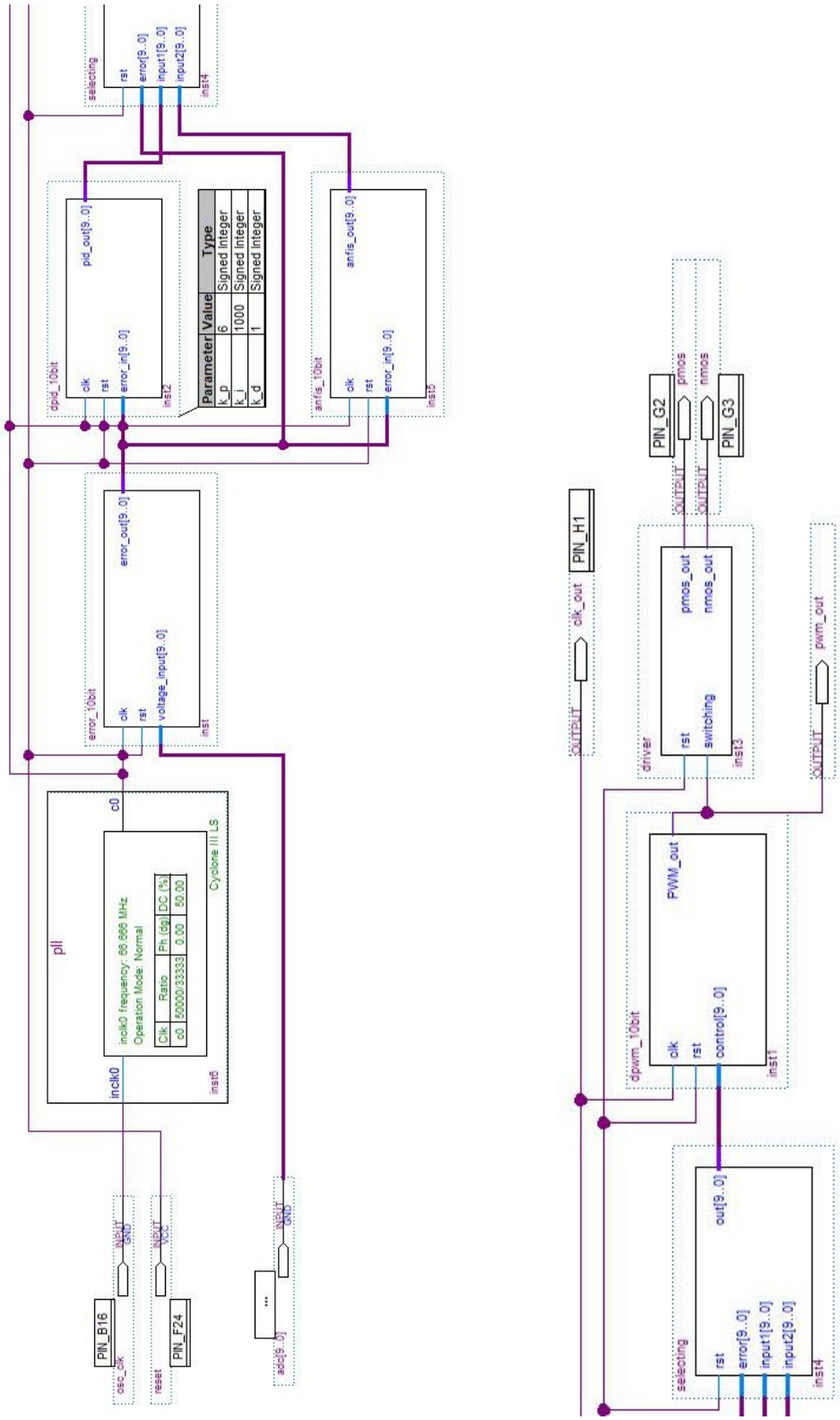


Figure 3.7: Verilog-HDL schematic for the synchronous buck converter with the Selecting ANFIS-PID Hybrid Type I Controller

3.3. Arithmetic ANFIS-PID Hybrid Control

As the name of this class of hybrids suggests, these hybrids use arithmetic operations to determine the output response of the controller. These include but are not limited to additions, multiplications, etc. Simple hybrids can be based on a single calculation as will be seen in this section. More complex hybrids can utilize entire polynomial outputs to obtain a specific response depending on application.

There are two arithmetic hybrid controllers considered as part of this thesis. These are summing and product hybrid controllers. The arithmetic operation is performed on the entire response of the individual controllers. The product controller is a novel controller proposed as part of this thesis and is a simpler and more efficient approach to the driven hybrid that will be covered in Section 3.4. The two arithmetic hybrids are referred to as:

- Summing ANFIS-PID Hybrid
- Product ANFIS-PID Hybrid

3.3.1. Summing ANFIS-PID Hybrid

This hybrid outputs the sum of the two controller outputs. Since the controller output is signed, the summing operation is signed. Its operation can be expressed in the expression given in (3.16). If the individual responses of the controller are substituted in, we get the expression in (3.17).

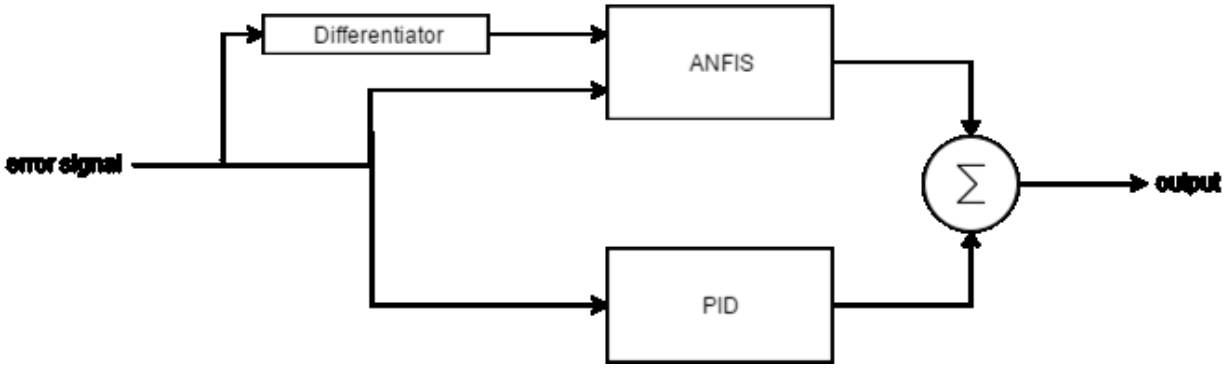


Figure 3.8: Block diagram for the Summing ANFIS-PID Hybrid

$$U_{HYBRID} = U_{ANFIS} + U_{PID} \tag{3.16}$$

$$u_{HYBRID} = u_{ANFIS}\left(e, \frac{de}{dt}\right) + K_p e + K_i \int e dt + K_d \frac{de}{dt} \tag{3.17}$$

As can be seen from equation (3.17), the hybrid is equivalent to a PID with additional proportional and integral constants. The magnitude of these constants are determined by the ANFIS's training. Generally, if the PID's operation is simplified, increasing the proportional parameter of the PID decreases the rise time and increases the overshoot. Similarly, increasing the integral parameter decreases the rise time, increases the overshoot and the settling time.

As such, since the summing hybrid can only add the effect of the constants (amplify only and not attenuate), it is expected that the summing hybrid would have a better (faster) rise time than the individual controllers but worse (larger) overshoot and (longer) settling time.

The block diagram of the controller can be seen in Figure 3.8.

3.3.2. Product ANFIS-PID Hybrid

This hybrid outputs the product of the two controller outputs. Since the controller output is signed, the multiplication operation is also required to be signed. Its operation can be expressed in the expression given in (3.18). If the individual responses of the controller are substituted in, we get the expression in (3.19).

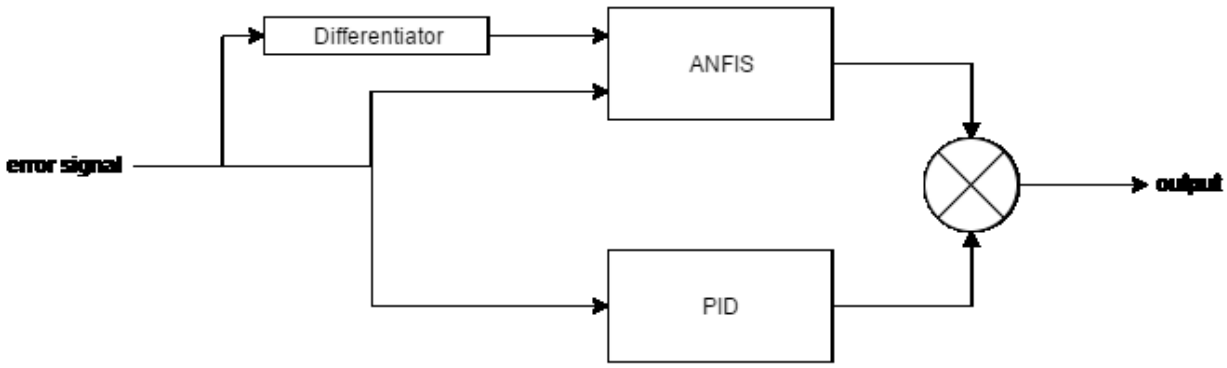


Figure 3.9: Block diagram for the Product ANFIS-PID Hybrid

$$U_{HYBRID} = U_{ANFIS} \cdot U_{PID} \tag{3.18}$$

$$u_{HYBRID} = u_{ANFIS}\left(e, \frac{de}{dt}\right) \cdot \left(K_p e + K_i \int e dt + K_d \frac{de}{dt}\right) \tag{3.19}$$

As can be seen from equation (3.17), ANFIS acts as an amplifier or as an attenuator for the PID controller depending on the input error signal and its rate of change. The magnitude of the attenuation or amplification of the PID's constants are determined by the ANFIS's training.

Generally, if the operation is simplified, increasing the proportional coefficient of the PID decreases the rise time and increases the overshoot. Similarly, increasing the integral coefficient decreases the rise time, increases the overshoot and the settling time. Increasing the derivative coefficient decreases the overshoot and settling time.

As such it is expected that the product hybrid will give better rise times compared to the stand-alone controllers but reduced overshoot and settling time (better) compared to the summing hybrid. The block diagram of the controller can be seen in Figure 3.9.

3.3.3. Theory of Operation

From the description of the arithmetic hybrids mentioned in Sections 3.3.1 and 3.3.2, the hybrid boosts both the advantages and disadvantages of the individual controllers. This should be especially true for the overshoot being larger in these hybrids. Due to the specific arithmetic operation performed, the product hybrid should provide a more desirable response.

For the PID tuning, the Ziegler-Nichols method is used. For either of the hybrids to minimize the overshoot, the "no overshoot" Ziegler-Nichols rule is utilized: Kp=0.2Ku, Ki=2Kp/Tu, and Kd=KpTu/3, where Tu is the period of oscillation and Ku is the ultimate gain.

As with the logical hybrids, the ANFIS training remains consistent in either controller. The open loop response of the target buck converter setup is used for the training.

3.3.4. Design and Implementation

As with the logical hybrid controllers, the controller setups were designed and implemented in two environments for simulation and experimental verification purposes. These are:

- MATLAB Simulink (for Simulation)
- Verilog HDL for FPGA (Cadence IC Suite for Simulation and Experimental)

For MATLAB Simulink, a full buck converter implementation is required which includes the power stage. Therefore, the following structure and blocks were used:

1. The state equations of the converter were used to model an ideal power stage of the buck-converter using Simulink blocks. This model can be seen in Figure 3.5.
2. A Flash-ADC was modelled using the quantizer block set to the respective number of ADC bits and introducing appropriate delays.

3. The controller utilized a Fuzzy-Logic controller block using a pre-trained Sugeno ANFIS system and a parallel Discrete PID. The two controllers were combined using a multiplier or summation block, configured depending on the controller type.
4. Finally, the DAC was based either on a trailing-edge pulse width modulator design, or a second order delta-sigma model.

The entire Simulink model for the buck converter with the product hybrid is given in Figure 3.10.

For the Verilog-HDL implementation, the following blocks were used:

1. The controller was implemented using a prioritized decision tree (comparator-based) using offline training data fed into a knowledgebase. The discrete PID was simply the Verilog representation of the PID equation previously mentioned in equation (3.10).
2. To calculate the error signal, a simple signed adder was used.
3. The multiplier and adders were implemented as signed blocks from the Altera MegaCore IP library.
4. For the DAC, the DPWM was implemented based on a counter based architecture. A delta-sigma converter was also implemented based on registers and D flip-flops.

The entire Verilog-HDL schematic block diagram implementation of the product hybrid is given in Figure 3.11. The summing hybrid simply had the multiplication block replaced by a summing one.

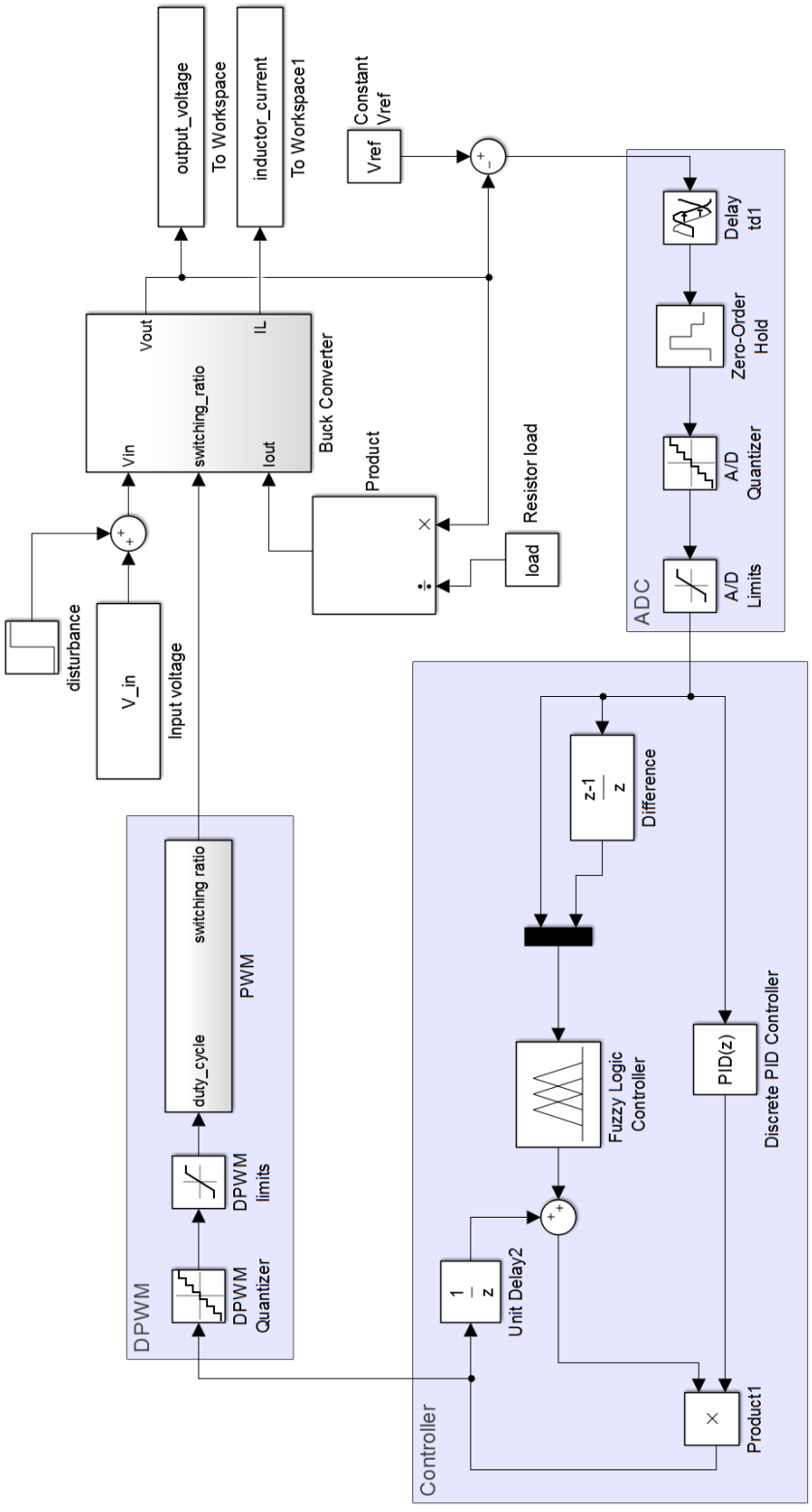


Figure 3.10: Simulink model for the synchronous buck converter with the Product ANFIS-PID Hybrid Controller

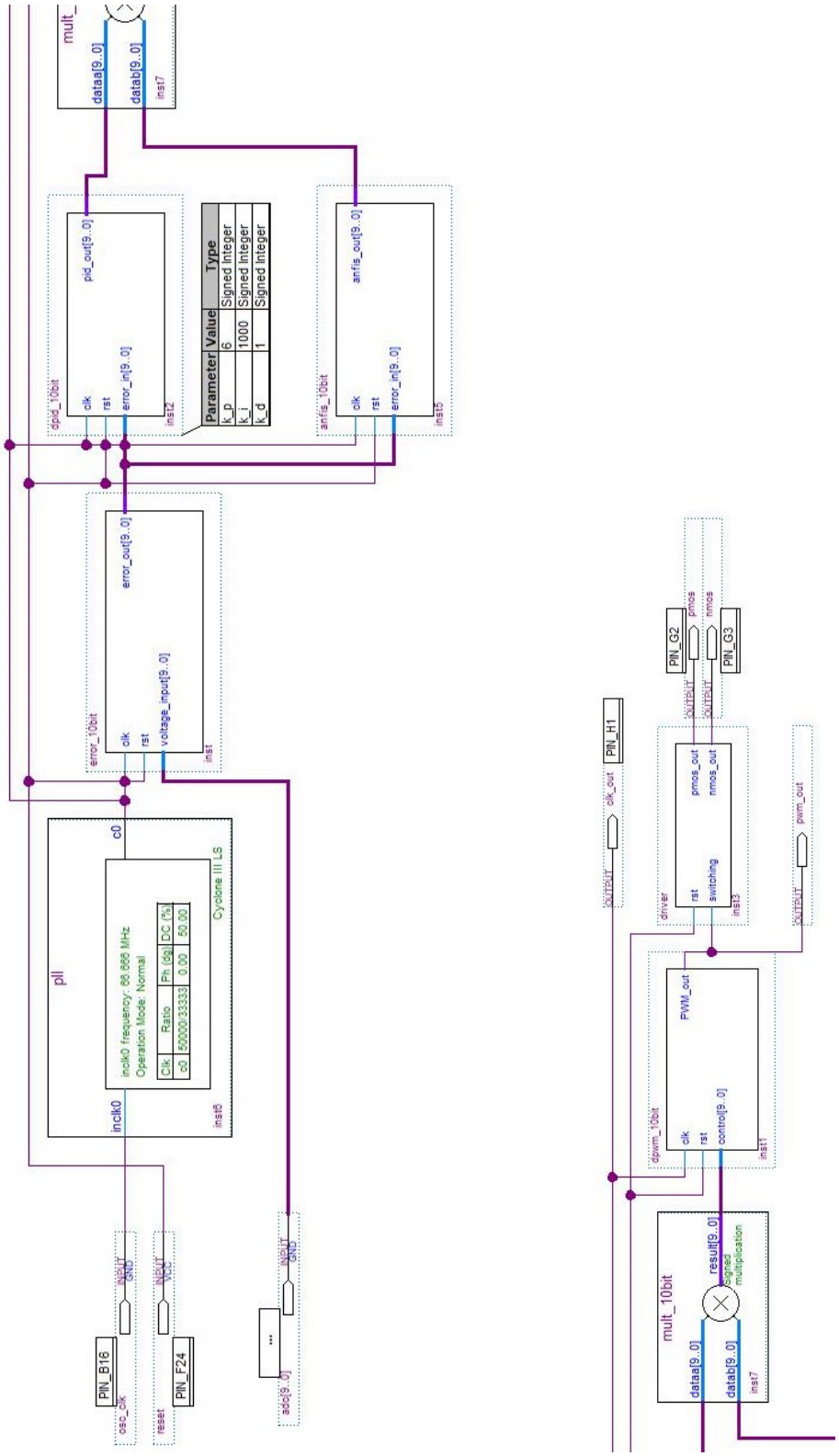


Figure 3.11: Verilog-HDL schematic for the synchronous buck converter with the Product ANFIS-PID Hybrid Controller

3.4. ANFIS Driven PID Hybrid Control

3.4.1. Introduction & Theory of Operation

ANFIS Driven PID, also known as Adaptive-Fuzzy driven PID, are PID controllers where the control coefficients are variable and set by an ANFIS controller output. Since there are three parameters for the PID, an ANFIS controller architecture was modified to have three outputs. Each output represents the change required in the PID coefficient for a more optimized output. The hybrid's overall operation can be expressed in the expression given in (3.20), where $\Delta K_{ANFIS,p}$, $\Delta K_{ANFIS,i}$, and $\Delta K_{ANFIS,d}$ are the ANFIS outputs. These outputs are signed and therefore can increase or decrease the coefficient as per the magnitude of the error signal.

$$u_{HYBRID} = (K_p + \Delta K_{ANFIS,p})e + (K_i + \Delta K_{ANFIS,i}) \int edt \ + (K_d + \Delta K_{ANFIS,d}) \frac{de}{dt} \quad (3.20)$$

The block diagram of the controller can be seen in Figure 3.12.

For the base PID tuning, the Ziegler-Nichols method is used. This can be done by the classical Ziegler-Nichols rule: Kp=0.6Ku, Ki=2Kp/Tu, and Kd=KpTu/8, where Tu is the period of oscillation and Ku is the ultimate gain.

PID controllers are inherently linear and tuned around a fixed operating point of the buck converter. Therefore, they do not offer the most optimized solution for non-linear system such as buck converters. Having variable parameters allows the PID to be always optimized to the buck converter's operating mode hence offering amore optimized controller.

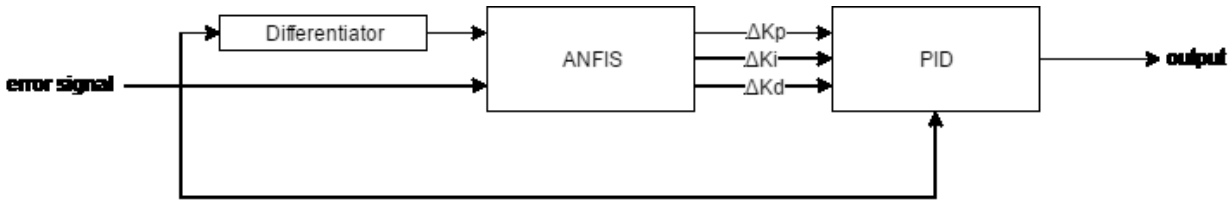


Figure 3.12: Block diagram for the ANFIS Driven PID Hybrid

3.4.2. Design and Implementation

The controller setup was designed and implemented in MATLAB (Simulink) for simulation based testing and verification.

For MATLAB Simulink, as in the previous hybrid controller simulations, a full buck converter implementation is required which includes the power stage. Therefore, the following structure and blocks were used:

1. The state equations of the converter were used to model an ideal power stage of the buck-converter using Simulink blocks. This model can be seen in Figure 3.5.
2. A Flash-ADC was modelled using the quantizer block set to the respective number of ADC bits and introducing appropriate delays.
3. The controller utilized a Fuzzy-Logic controller block using a pre-trained Sugeno ANFIS system and a custom implementation of a parallel Discrete PID to allow for coefficient variation.
4. Finally, the DAC was based either on a trailing-edge pulse width modulator design, or a second order delta-sigma model.

The entire Simulink model for the buck converter is given in Figure 3.13.

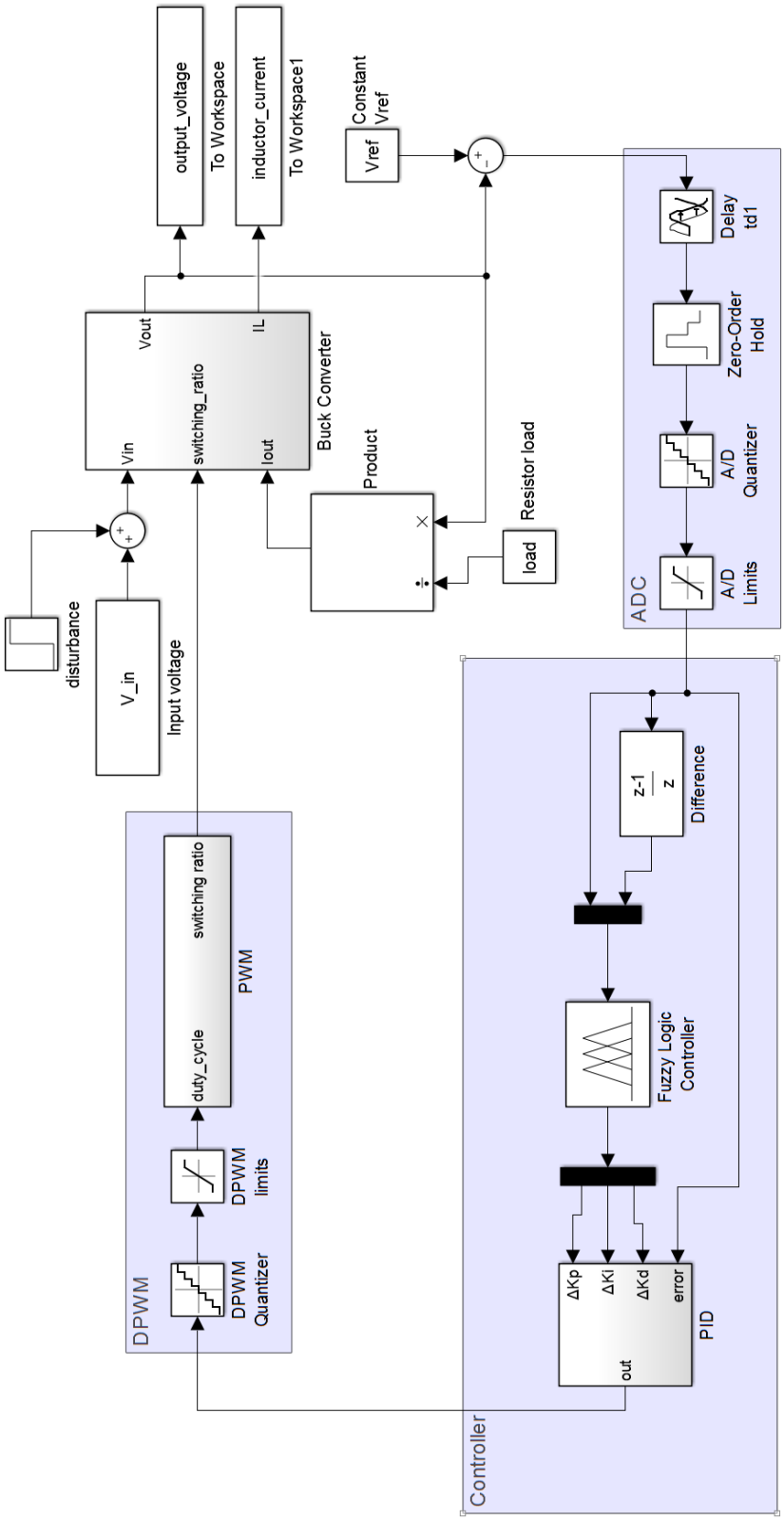


Figure 3.13: Simulink model for the synchronous buck converter with the ANFIS Driven PID Hybrid Controller

CHAPTER 4

SIMULATION AND EXPERIMENTAL RESULTS

4.1. Simulation with Digital Pulse Width Modulators (DPWM)

As covered in Section 2.5, there are a variety of Digital-to-Analog converters that can be utilized with buck converters. The most commonly used type is the Digital Pulse Width Modulator (DPWM).

In this section, simulation results for each of the ANFIS-PID hybrid buck controllers covered in Chapter 3 with a DPWM will be presented and analyzed and their performance will be compared against a traditional buck controller.

The buck converter was designed to operate with regulated output set at 1.2 V and the input voltage of 3.3 V. The system specification used for the simulation are given in Table 4.1.

Table 4.1: System specifications used for Simulation

Parameter	Value
Input Voltage	3.3 V
Target Output Voltage	1.2 V
Inductor Value	1μH
Inductor ESR Value	20 mΩ
Capacitor Value	2 μF
Capacitor ESR Value	20 mΩ

ADC Frequency	10 MHz
ADC Resolution	8-bit
DPWM Frequency	100 MHz
DPWM Resolution	9-bit

The circuit simulations were done using LFoundry's 150nm process libraries in Cadence. Layouts were generated for the Verilog-HDL controllers using Cadence Encounter over a silicon area of 170 by 155 micron for each.

4.1.1. Logical Hybrid: Switching Type I

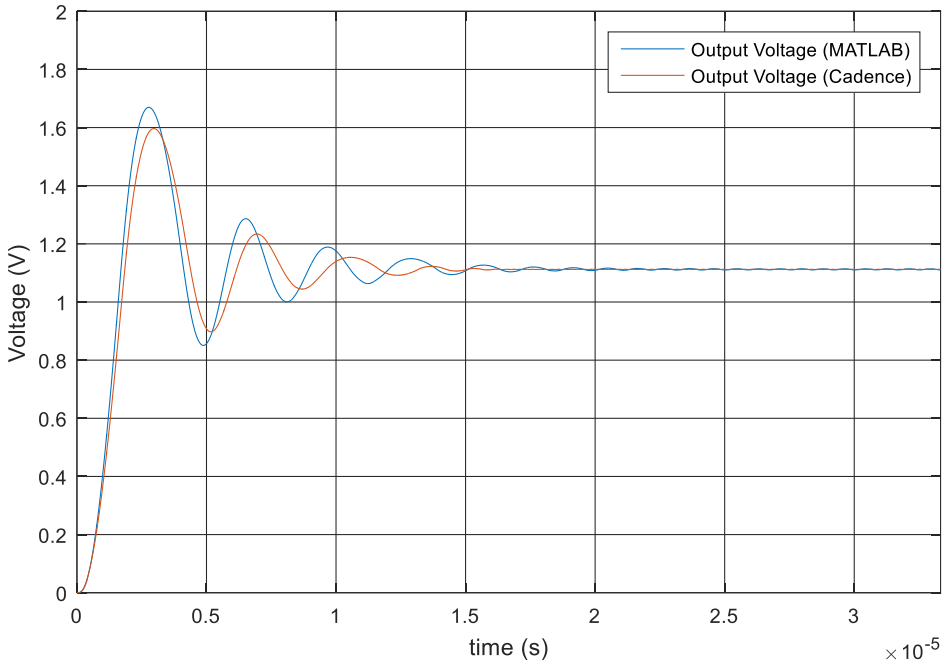
The controller with the specified DPWM was simulated in MATLAB and in Cadence. The output voltage waveform is given in Figure 4.1. The inductor current waveform and the switching duty value is given in Figure 4.2 (a) and (b) respectively.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Table 4.2.

Table 4.2: The various parameters extracted from the simulation of the Switching Type I hybrid buck converter

Parameter	MATLAB Simulation	Circuit Simulation
Steady State Error (V)	0.095	0.095
Overshoot (%)	49.7	43.4
Rise Time (µs)	1.04	1.16
Settling Time (µs)	13.79	11.38
Output Voltage Ripple (V)	0.004	0.0011

(a)



(b)

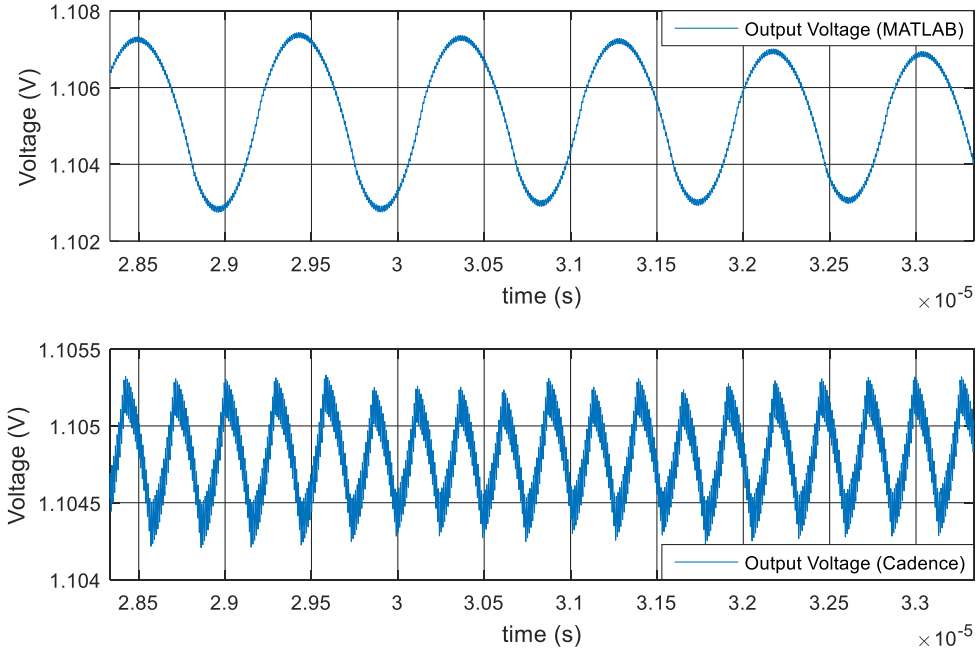
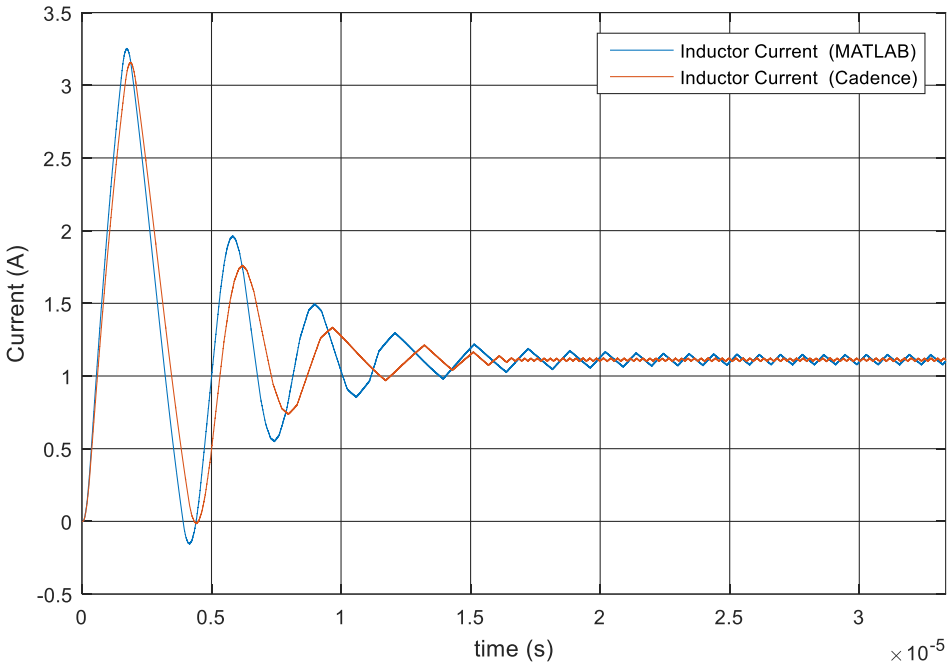


Figure 4.1: Simulated Switching Type I Hybrid (a) Output Voltage (b) Output voltage ripple

(a)



(b)

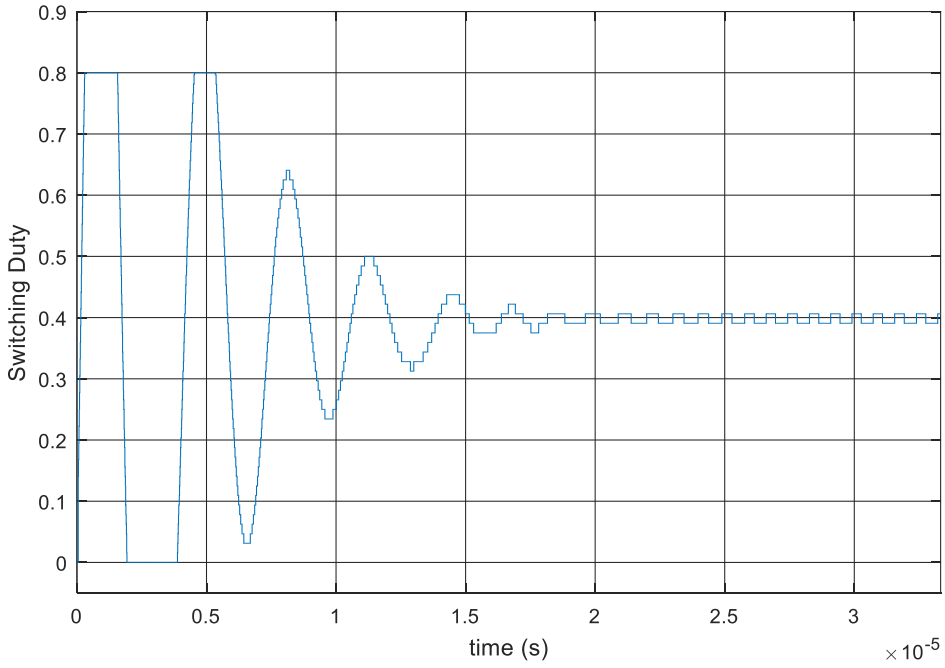


Figure 4.2: Simulated Switching Type I Hybrid (a) Inductor Current (b) Switching Duty (MATLAB)

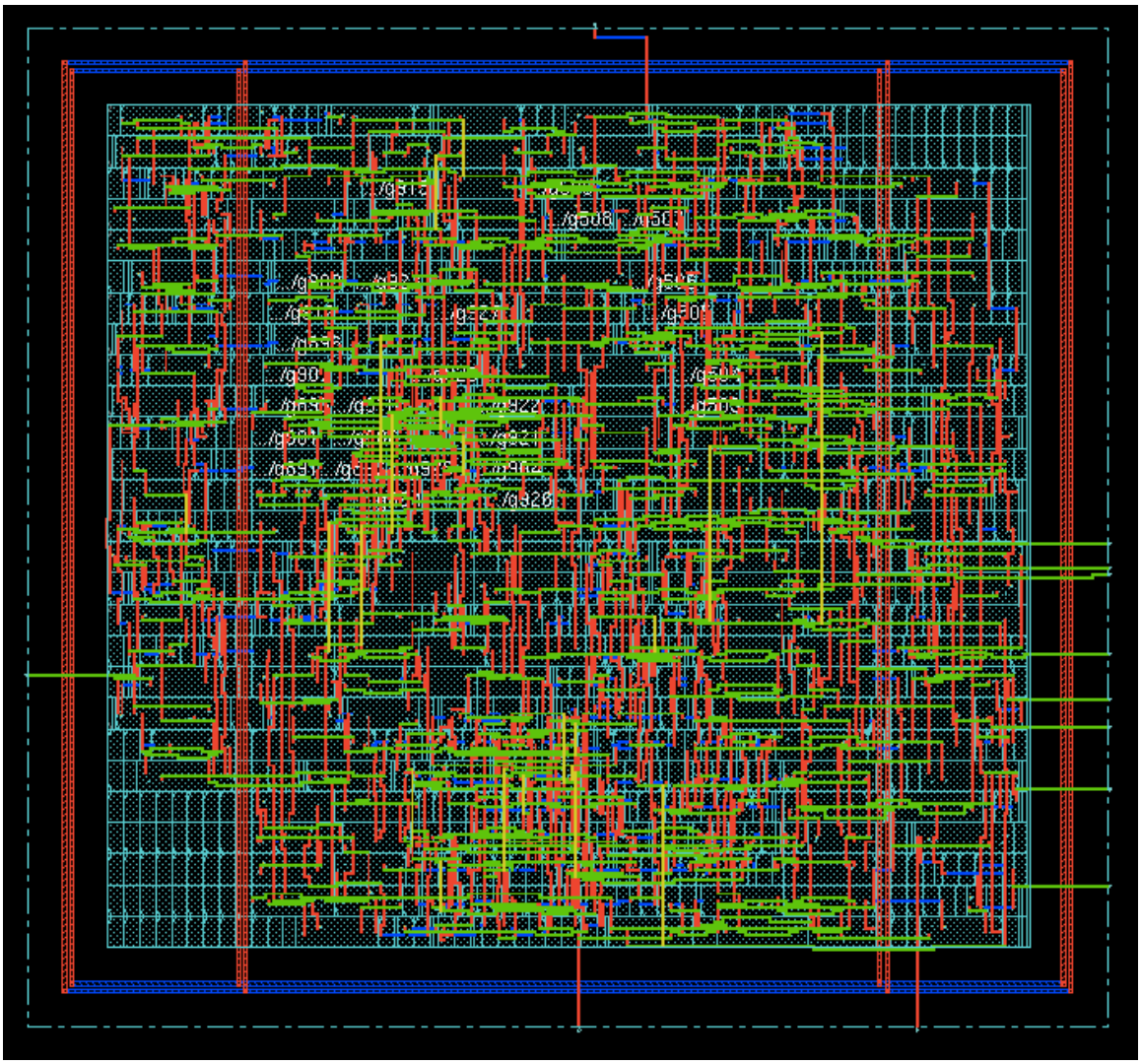


Figure 4.3: Switching Type I Hybrid Cadence Layout used for post-layout simulations

The layout generated in Cadence is given in Figure 4.3. Any subsequent layout images will not be added to this thesis due to their lack of legibility.

4.1.2. Logical Hybrid: Switching Type II

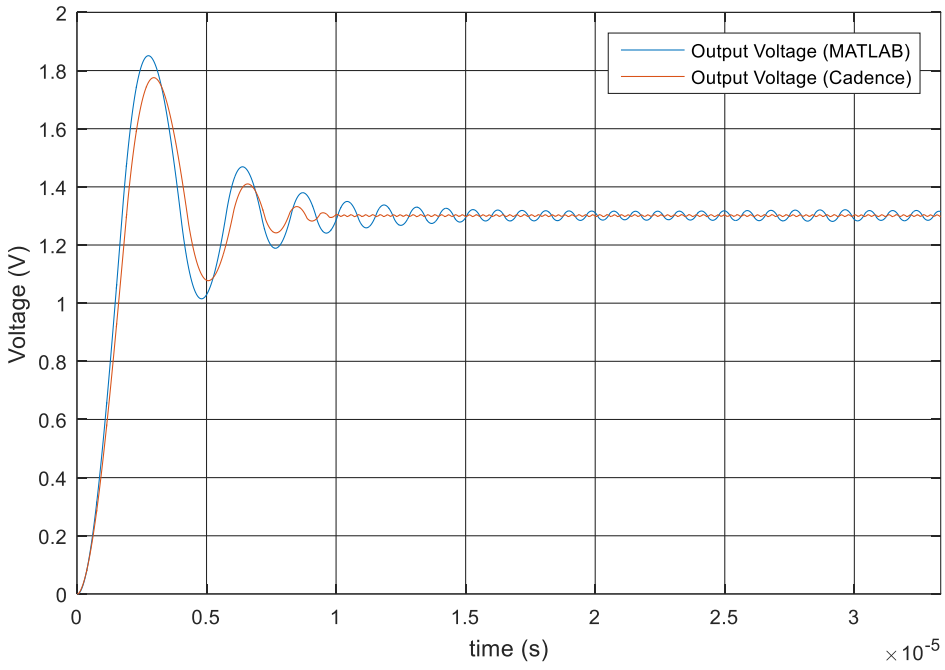
The controller with the specified DPWM was simulated in MATLAB and in Cadence. The output voltage waveform is given in Figure 4.4. The inductor current waveform and the switching duty value is given in Figure 4.5 (a) and (b) respectively.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Table 4.3.

Table 4.3: The various parameters extracted from the simulation of the Switching Type II hybrid buck converter

Parameter	MATLAB Simulation	Circuit Simulation
Steady State Error (V)	0.099	0.099
Overshoot (%)	40.7	36.6
Rise Time (μs)	1.16	1.29
Settling Time (μs)	99.74	8.58
Output Voltage Ripple (V)	0.033	0.099

(a)



(b)

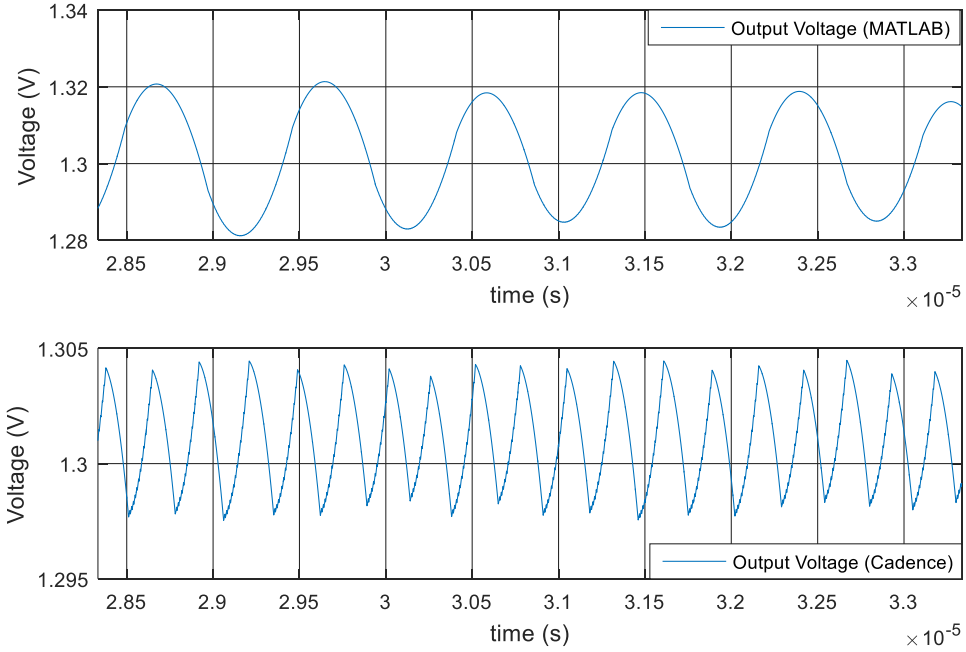
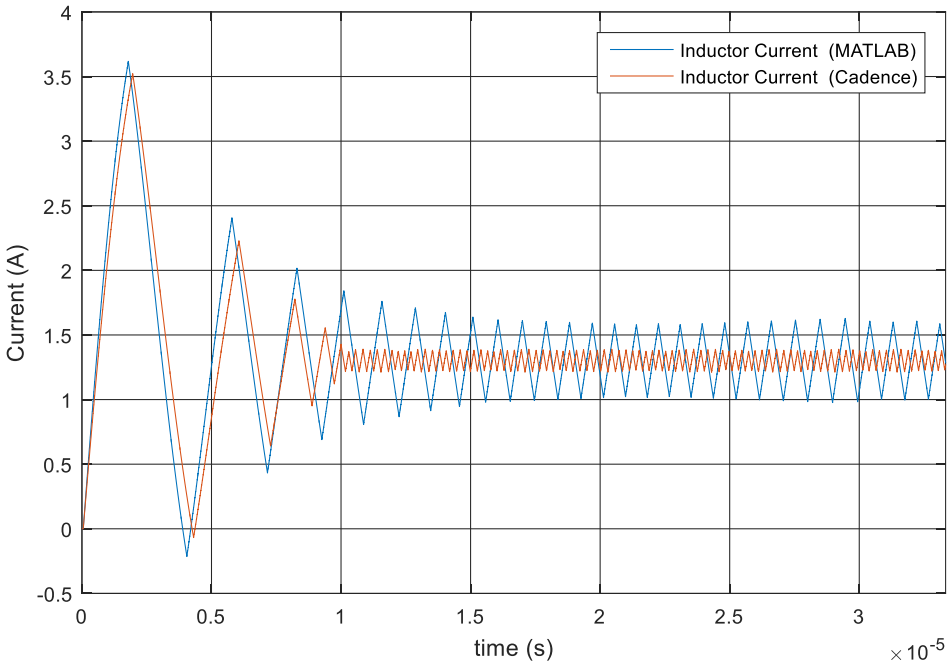


Figure 4.4: Simulated Switching Type II Hybrid (a) Output Voltage (b) Output voltage ripple

(a)



(b)

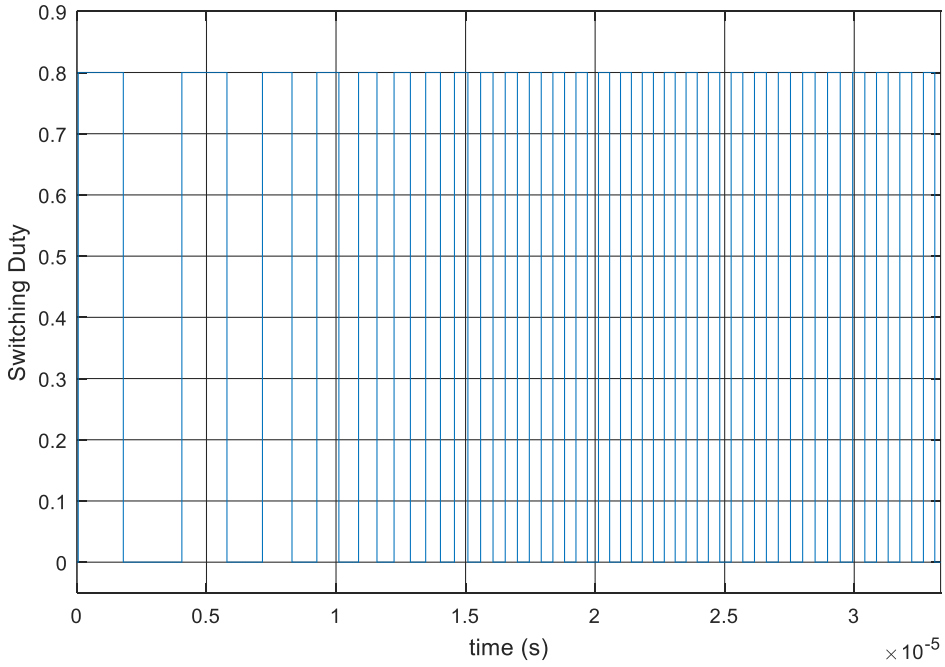


Figure 4.5: Simulated Switching Type II Hybrid (a) Inductor Current (b) Switching Duty (MATLAB)

4.1.3. Arithmetic Hybrid: Summing

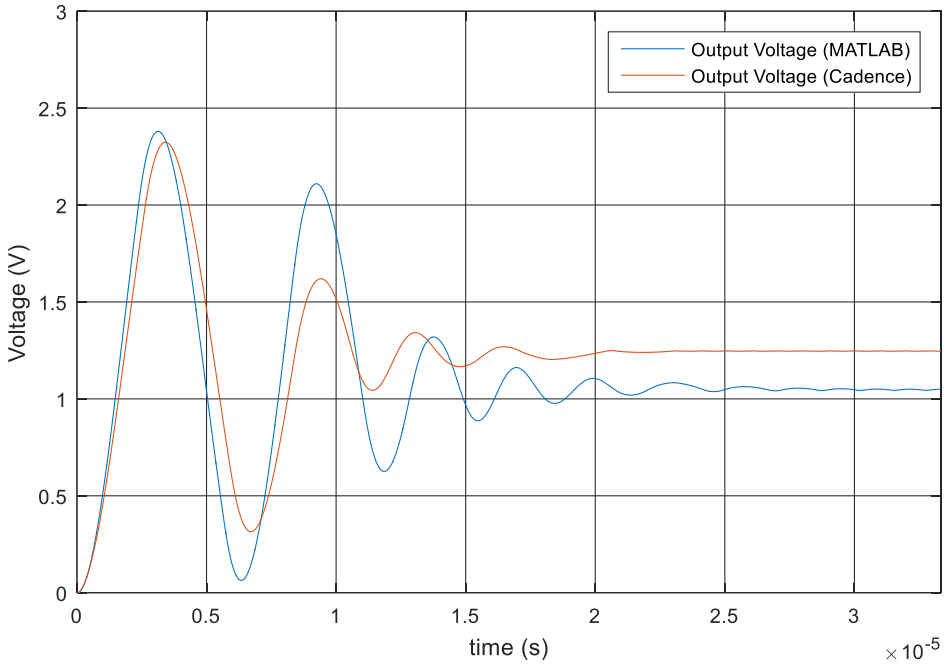
The controller with the specified DPWM was simulated in MATLAB and in Cadence. The output voltage waveform is given in Figure 4.6. The inductor current waveform and the switching duty value is given in Figure 4.7 (a) and (b) respectively.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Table 4.4.

Table 4.4: The various parameters extracted from the simulation of the Summing hybrid buck converter

Parameter	MATLAB Simulation	Circuit Simulation
Steady State Error (V)	0.13	0.044
Overshoot (%)	120	88.8
Rise Time (µs)	1.02	1.24
Settling Time (µs)	43.9	87.7
Output Voltage Ripple (V)	0.01	0.0015

(a)



(b)

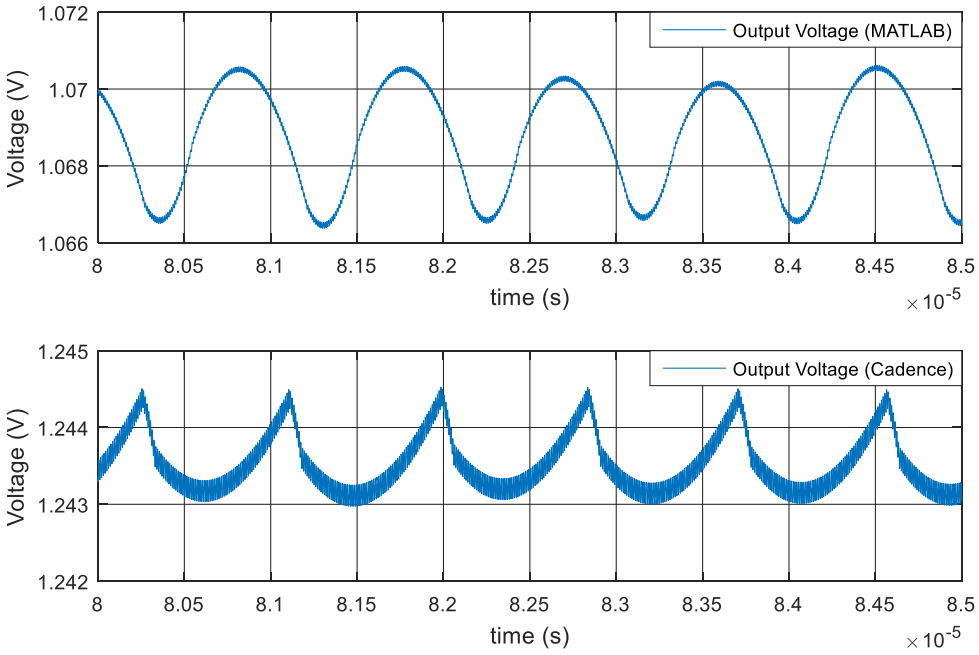
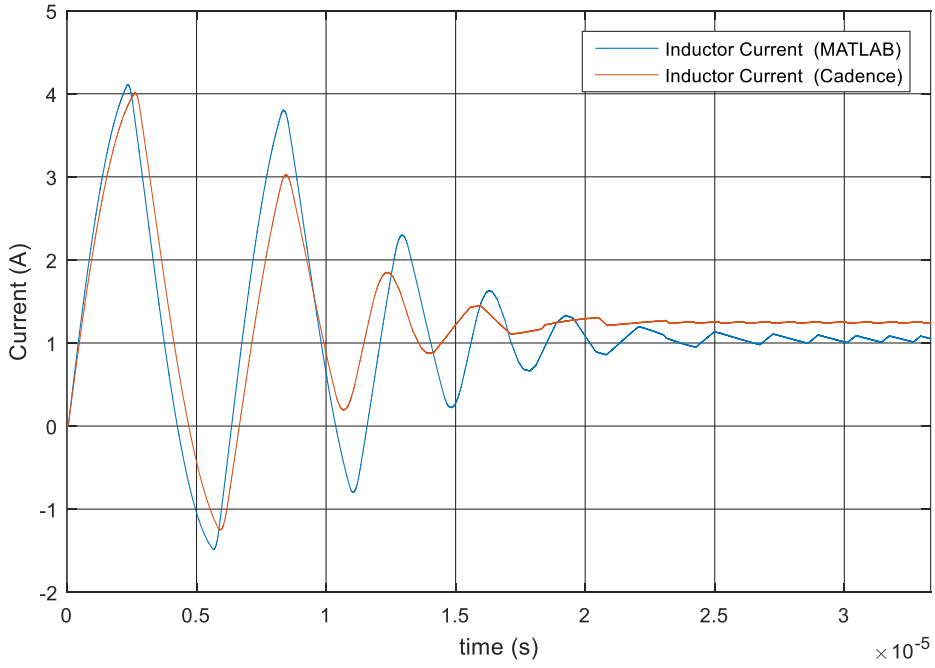


Figure 4.6: Simulated Summing Hybrid (a) Output Voltage (b) Output voltage ripple

(a)



(b)

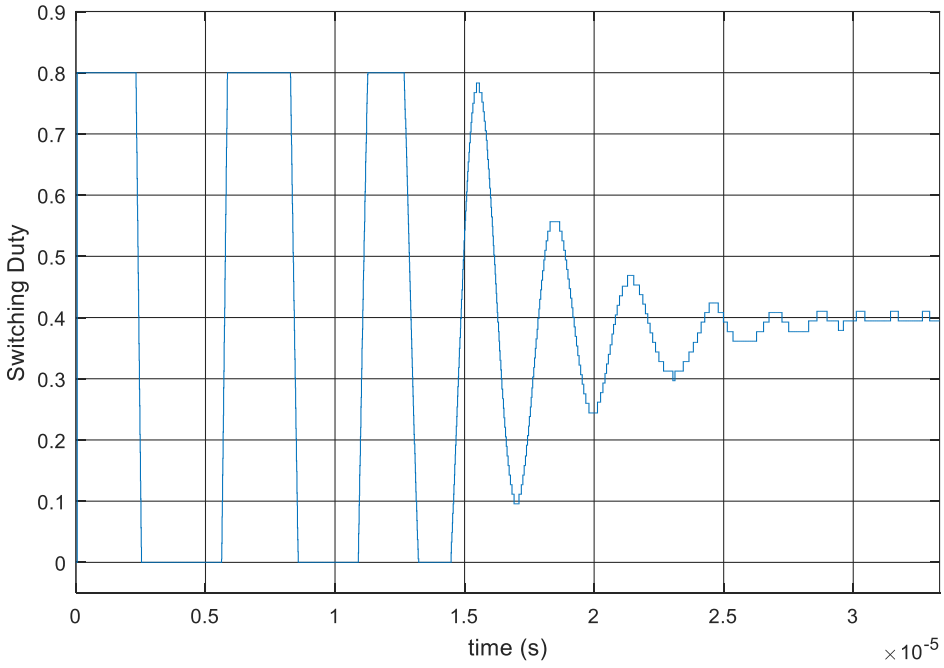


Figure 4.7:Simulated Summing Hybrid (a) Inductor Current (b) Switching Duty (MATLAB)

4.1.4. Arithmetic Hybrid: Product

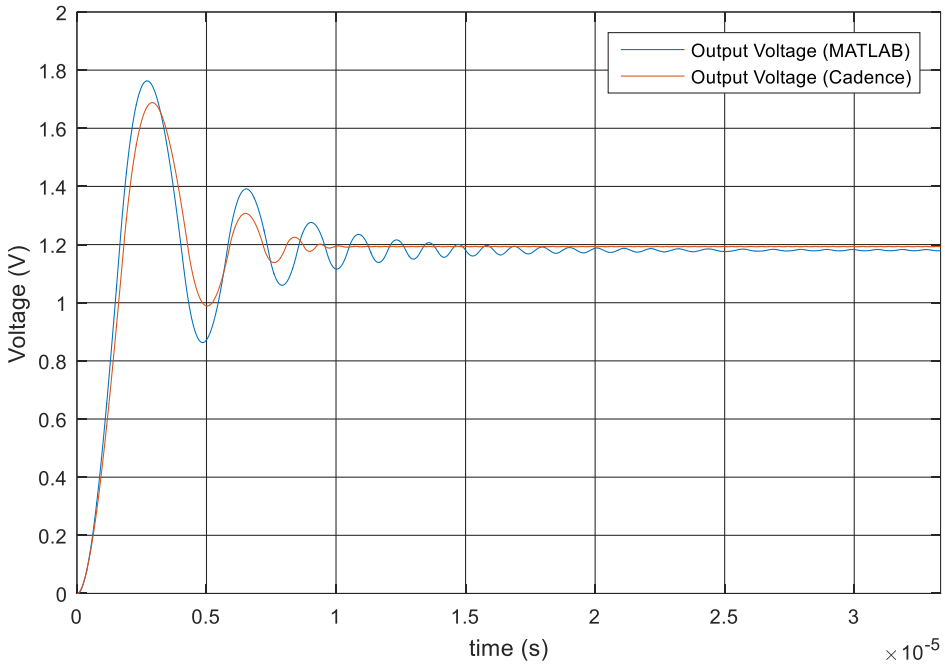
The controller with the specified DPWM was simulated in MATLAB and in Cadence. The output voltage waveform is given in Figure 4.8. The inductor current waveform and the switching duty value is given in Figure 4.9 (a) and (b) respectively.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Table 4.5.

Table 4.5: The various parameters extracted from the simulation of the Product hybrid buck converter

Parameter	MATLAB Simulation	Circuit Simulation
Steady State Error (V)	0.019	0.007
Overshoot (%)	49.3	41.5
Rise Time (μs)	1.07	1.21
Settling Time (μs)	14.2	8.58
Output Voltage Ripple (V)	0.0041	0.0012

(a)



(b)

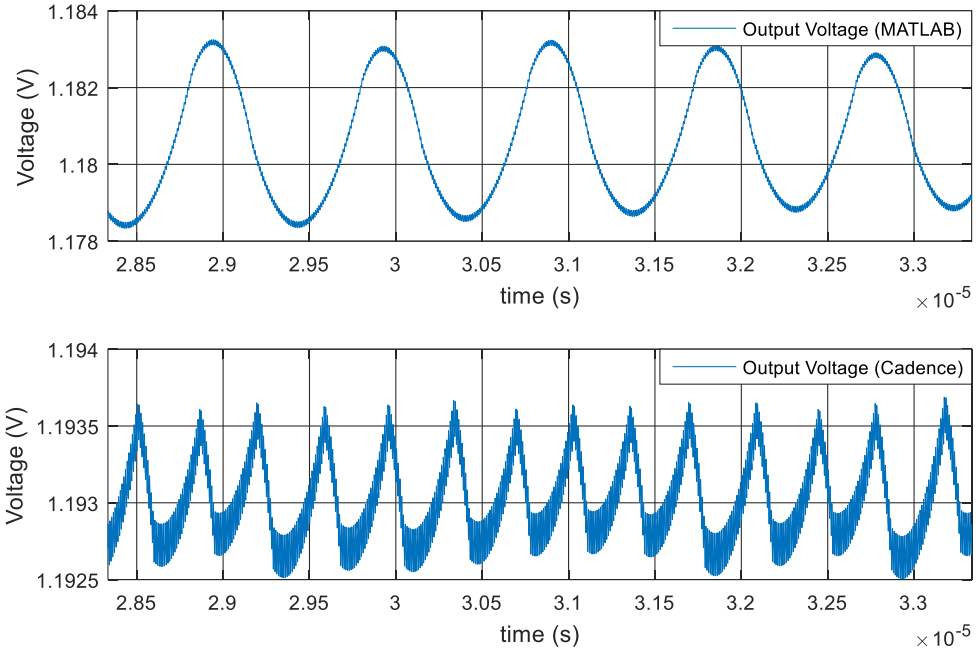
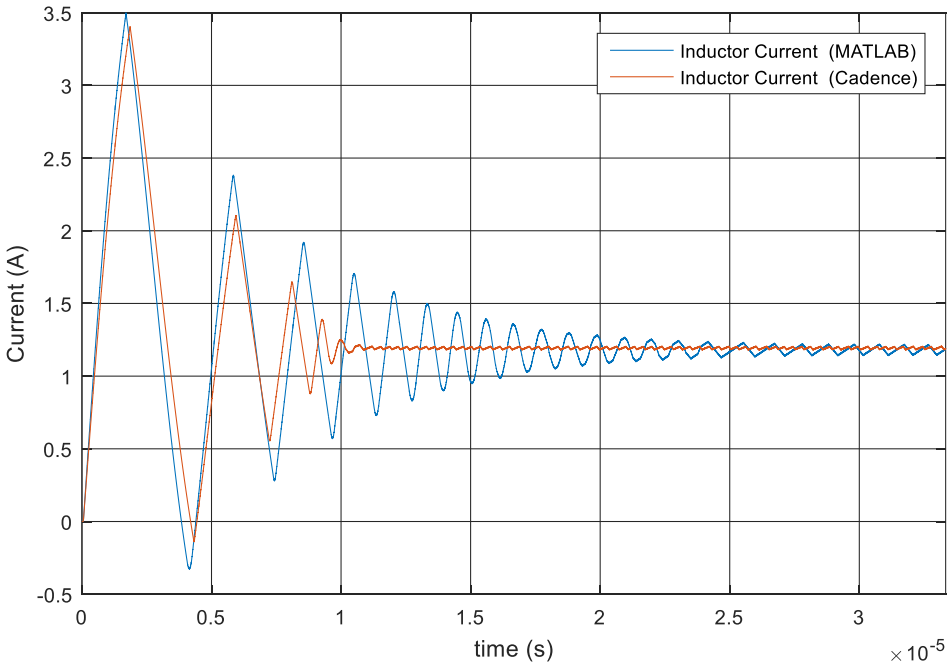


Figure 4.8: Simulated Product Hybrid (a) Output Voltage (b) Output voltage ripple

(a)



(b)

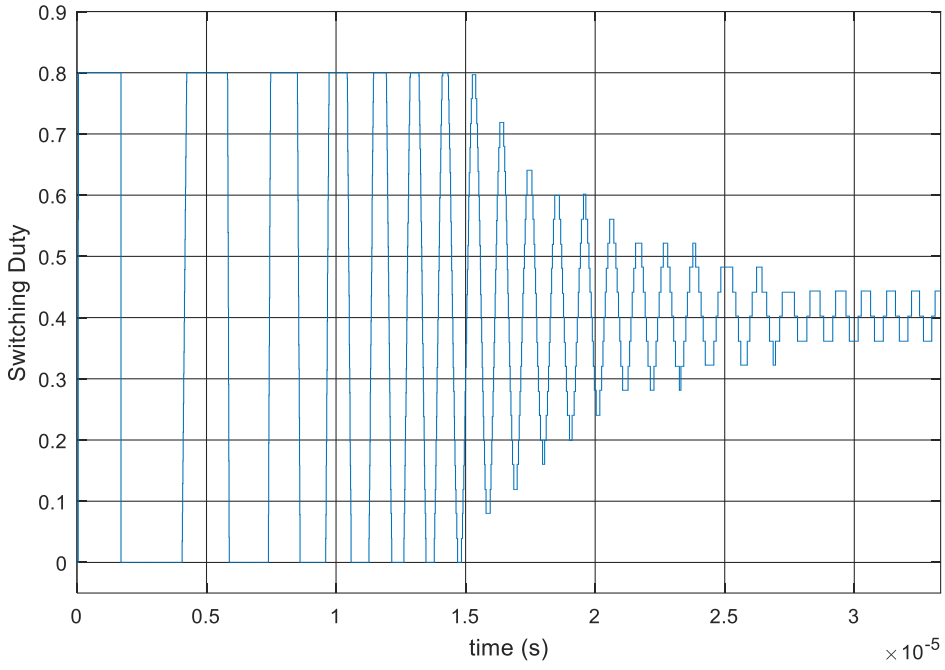


Figure 4.9: Simulated Product Hybrid (a) Inductor Current (b) Switching Duty (MATLAB)

4.1.5. ANFIS Driven PID

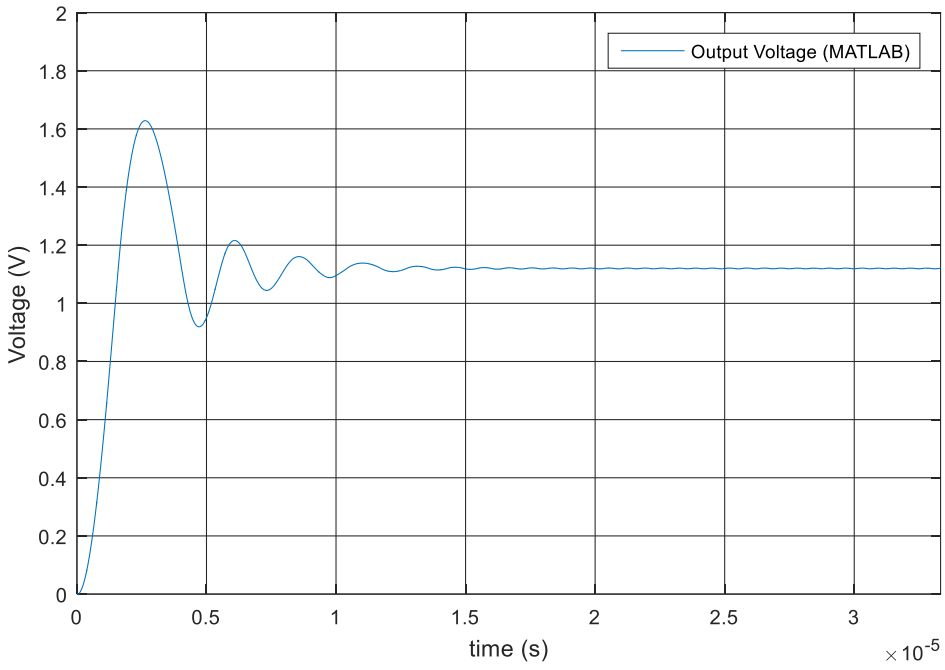
The controller with the specified DPWM was simulated in MATLAB. The output voltage waveform is given in Figure 4.10. The inductor current waveform and the switching duty value is given in Figure 4.11 (a) and (b) respectively.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Table 4.6.

Table 4.6: The various parameters extracted from the simulation of the ANFIS-Driven-PID buck converter

Parameter	MATLAB Simulation
Steady State Error (V)	0.08
Overshoot (%)	45.3
Rise Time (µs)	1.04
Settling Time (µs)	10.1
Output Voltage Ripple (V)	0.0023

(a)



(b)

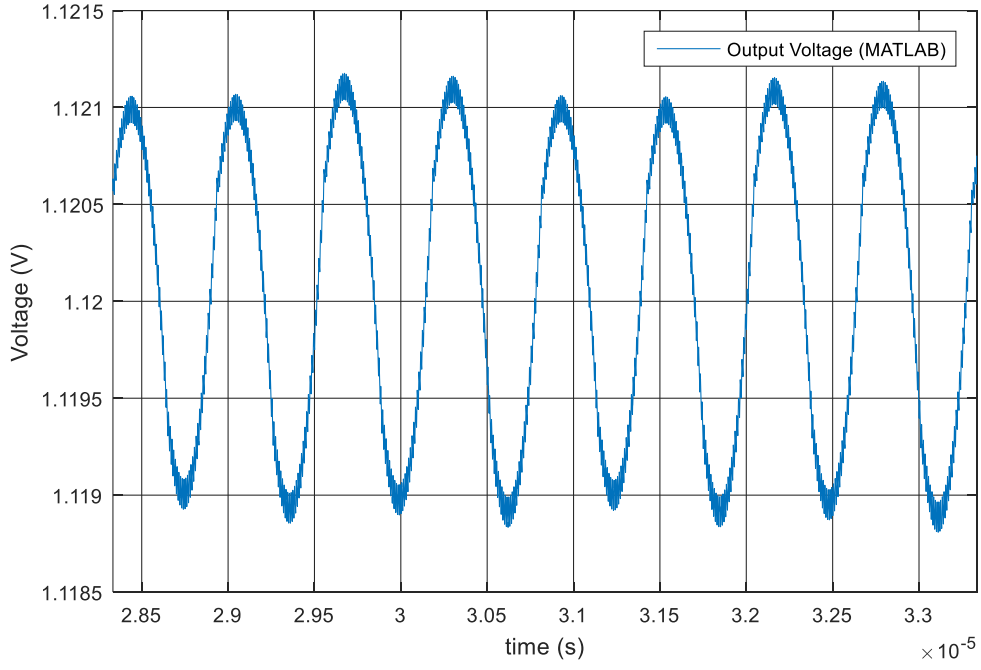
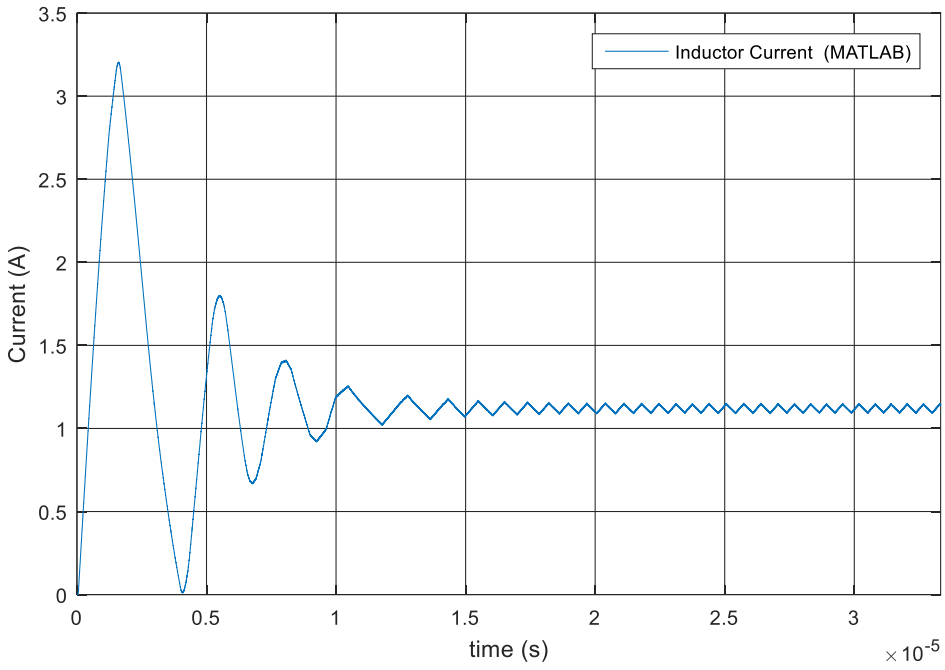


Figure 4.10: Simulated ANFIS-Driven-PID Hybrid (a) Output Voltage (b) Output voltage ripple

(a)



(b)

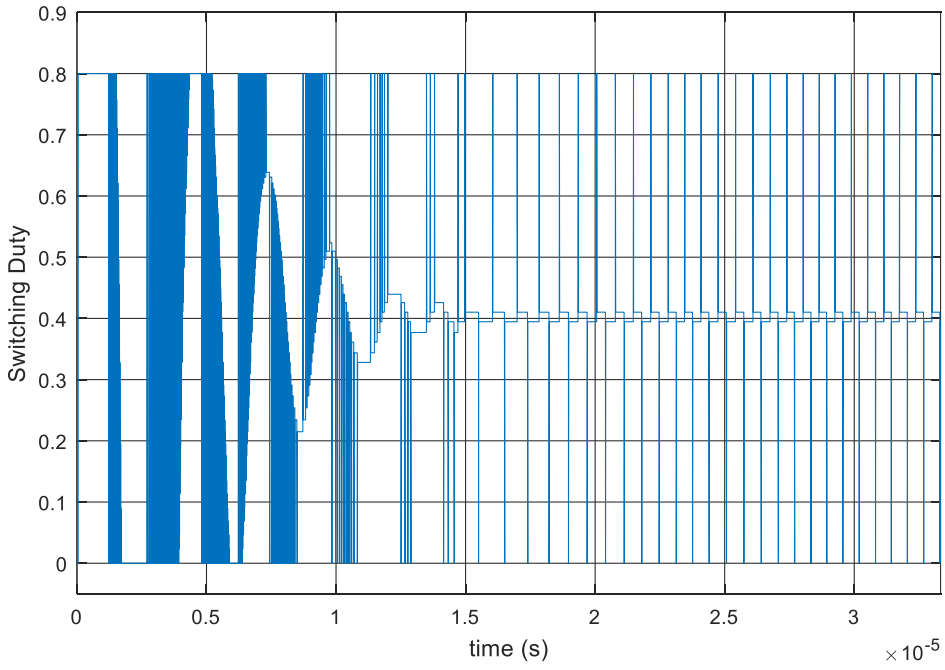


Figure 4.11: Simulated ANFIS-Driven-PID (a) Inductor Current (b) Switching Duty

4.1.6. Reference PID

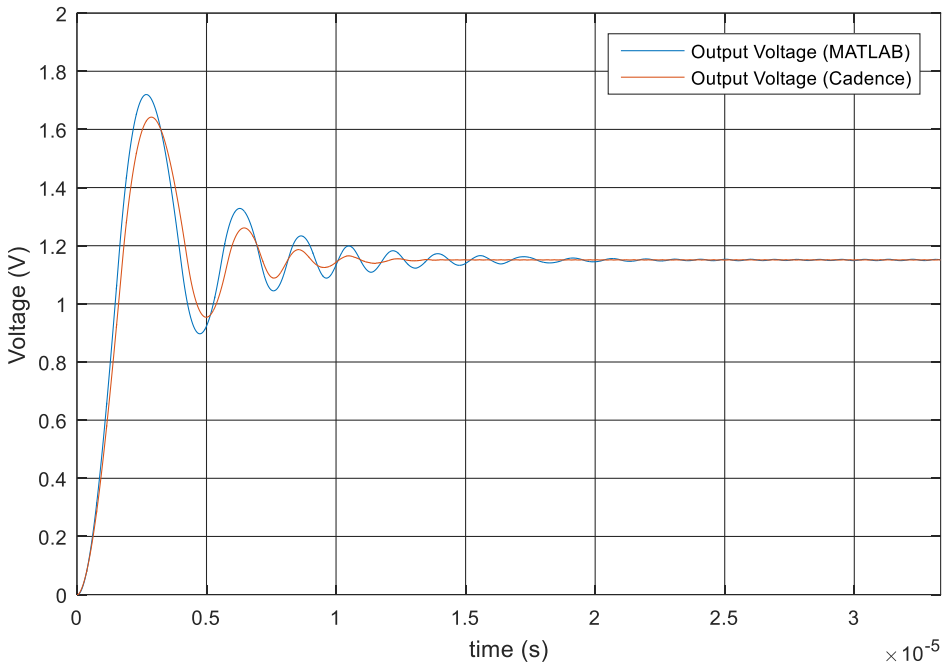
This controller with the specified DPWM was simulated in MATLAB and in Cadence for reference purposes as a benchmark. The output voltage waveform is given in Figure 4.12. The inductor current waveform and the switching duty value is given in Figure 4.13 (a) and (b) respectively.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Table 4.7.

Table 4.7: The various parameters extracted from the simulation of the PID buck converter

Parameter	MATLAB Simulation	Circuit Simulation
Steady State Error (V)	0.049	0.0488
Overshoot (%)	49.4	42.7
Rise Time (μs)	1.06	1.18
Settling Time (μs)	13.2	9.72
Output Voltage Ripple (V)	0.0043	0.0011

(a)



(b)

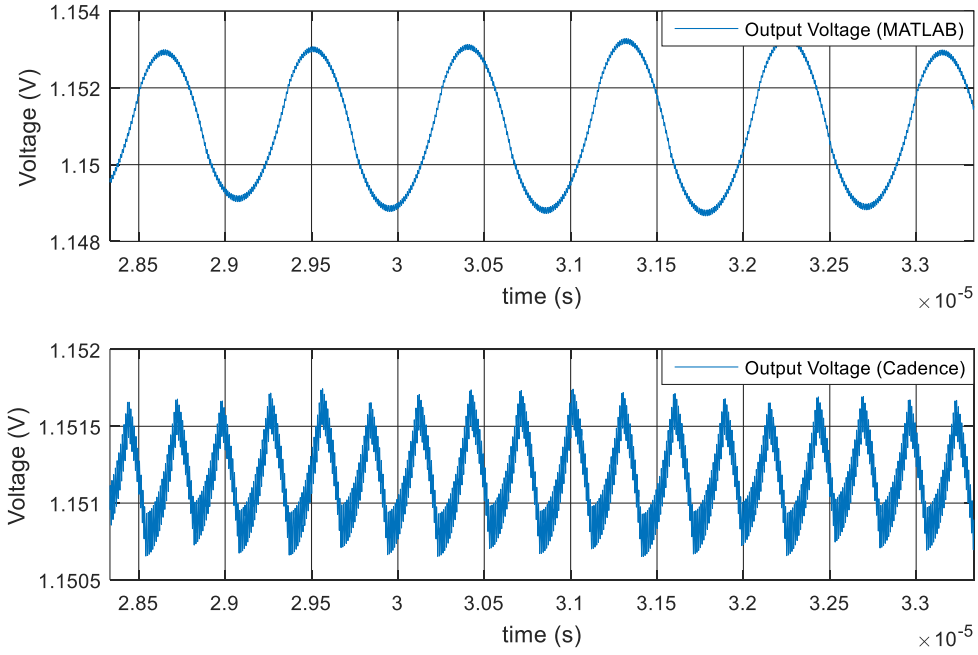
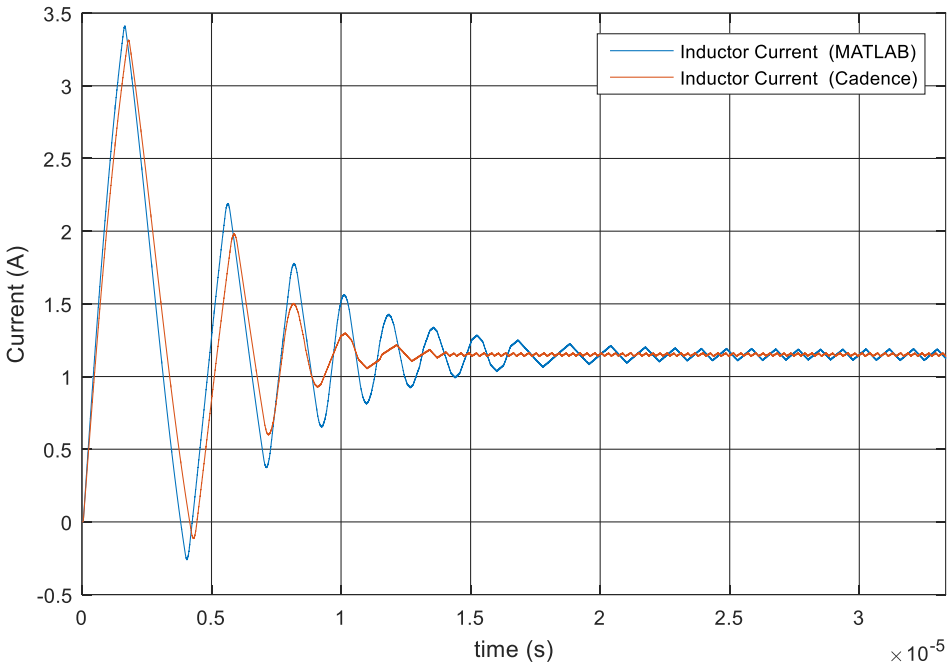


Figure 4.12: Simulated PID (a) Output Voltage (b) Output voltage ripple

(a)



(b)

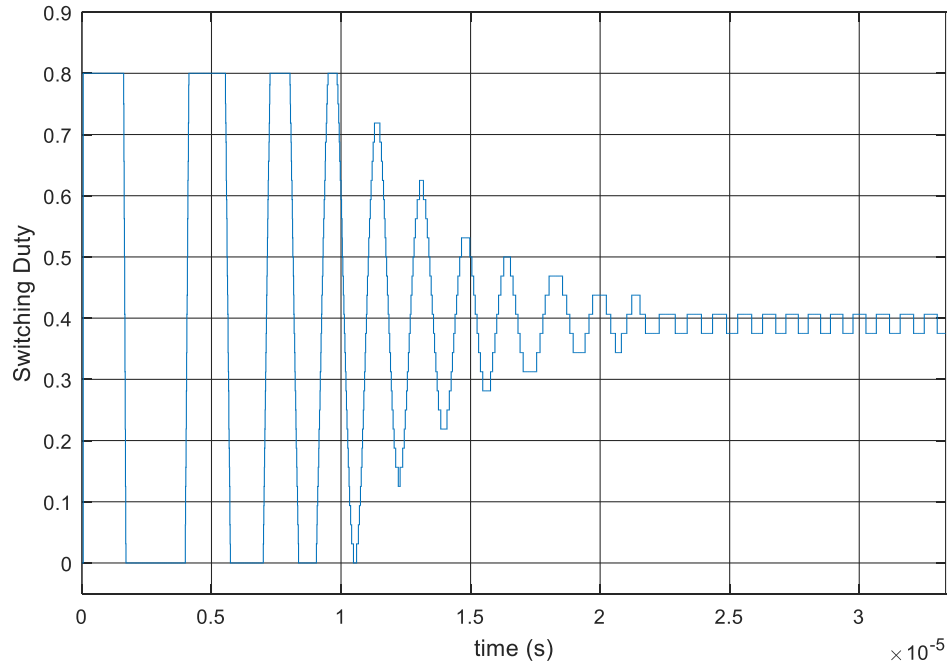


Figure 4.13: Simulated PID (a) Inductor Current (b) Switching Duty (MATLAB)

4.1.7. Comparison

Results from each type of buck controller were compared against the Reference PID simulations. Table 4.8 shows the MATLAB simulation results compared whereas Table 4.9 shows the Cadence post layout simulation results summarized for comparison.

As can be seen in the tables, the switching hybrid type I has no improvement when compared to the reference PID in either simulation environments. The switching hybrid type II controller showed improvements of 6-9 percent in terms of overshoot. The product hybrid improved the steady state error and the overshoot by 0.03 to 0.04 V and 0.1 to 1.2 percent respectively. The ANFIS Driven PID showed the most improvement among all proposed hybrid controller buck converters by showing improvements of approximately 4 percent to the overshoot, 0.02 μs to the rise time, 3.1 μs to the setting time and 2 mV to the output voltage ripple.

When compared to each other, among all the hybrids, the Product hybrid had the lowest steady-state error and a smaller settling time. The Switching Type II hybrid had the smallest overshoot. The ANFIS driven PID has the lowest settling time and smallest output voltage ripple.

Table 4.8: MATLAB Simulation results for the ANFIS-PID hybrid controllers summarized

Parameter	PID	Switching Type I	Switching Type II	Summing	Product	ANFIS Driven PID
Steady State Error (V)	0.049	0.095	0.099	0.13	0.019	0.08
Overshoot (%)	49.4	49.7	40.7	120	49.3	45.3
Rise Time (µs)	1.06	1.04	1.16	1.02	1.07	1.04
Settling Time (µs)	13.2	13.79	99.74	43.9	14.2	10.1
Output Voltage Ripple (V)	0.0043	0.0040	0.033	0.010	0.0041	0.0023

Table 4.9: Cadence Circuit Simulation results for the ANFIS-PID hybrid controllers summarized

Parameter	PID	Switching Type I	Switching Type II	Summing	Product
Steady State Error (V)	0.0488	0.095	0.099	0.044	0.0070
Overshoot (%)	42.7	43.4	36.6	88.8	41.5
Rise Time (µs)	1.18	1.16	1.29	1.24	1.21
Settling Time (µs)	9.72	11.38	8.58	87.7	8.58
Output Voltage Ripple (V)	0.0011	0.0011	0.099	0.0015	0.0012

The efficiencies of each of the ANFIS-PID hybrid controller were calculated in MATLAB and plotted with respect to the load current. This can be seen in Figure 4.14. Note that modulator power was not considered. Typically, higher overshoots and bigger output voltage ripples cause reduced efficiency.

The peak efficiencies for each of the hybrid controller are given in Table 4.10. The efficiency of a buck converter can be taken as the figure of merit since it is affected by all other performance parameters. The Product ANFIS-PID hybrid has the highest peak efficiency at 96.5 % and the largest spread allowing for it to be ideal for both light and heavy load applications. This high efficiency can be related to the product hybrid controller giving reduced overshoot and output voltage rippled compared to the other hybrids. The Switching Type II and the ANFIS Driven PID also offer efficiency improvements compared to the traditional PID.

Table 4.10: Peak efficiencies for the hybrid controllers

Hybrid Controller	Peak Efficiency
Reference PID	92.7 %
Switching Type I	88.4 %
Switching Type II	92.9 %
Summing	91.1 %
Product	96.5 %
ANFIS Driven PID	93.1 %

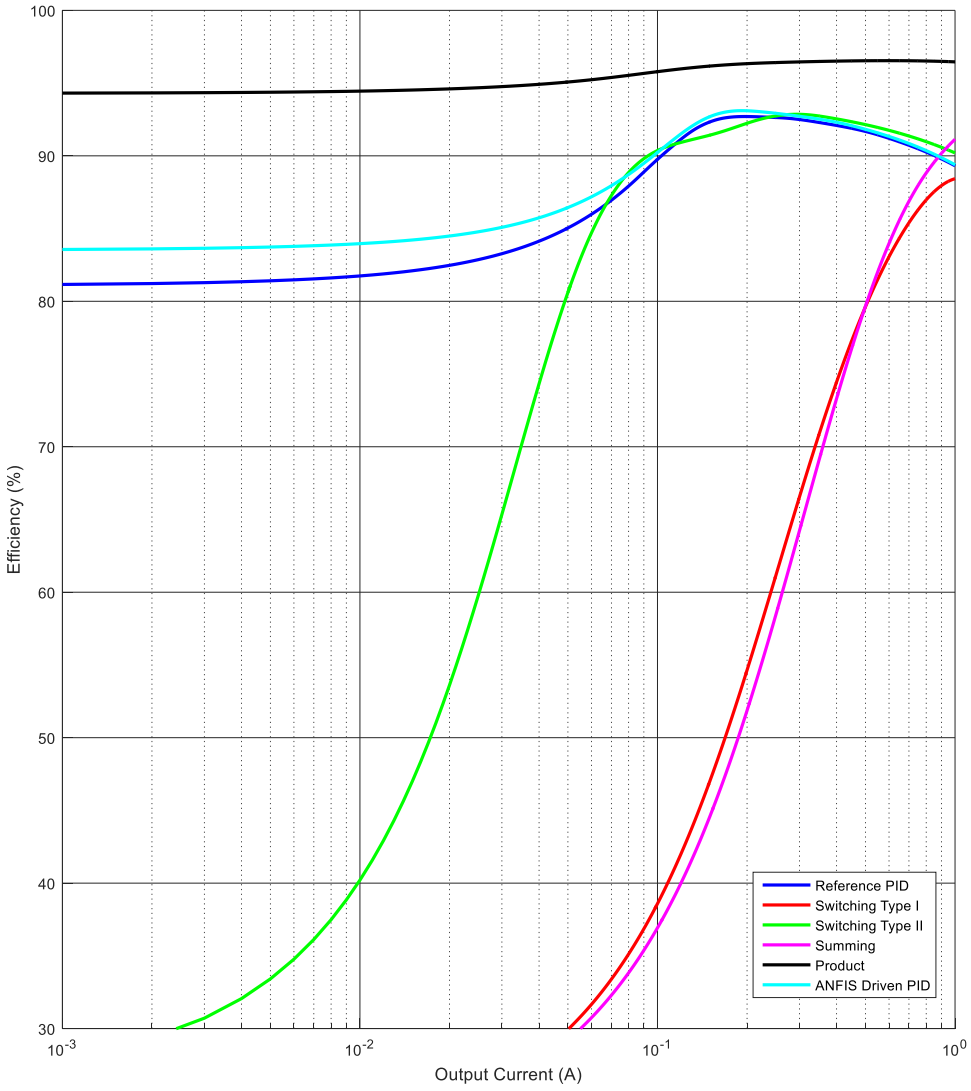


Figure 4.14: Efficiencies of each of the hybrid controller with DPWM plotted with respect to load current

4.2. Simulation with Delta-Sigma Modulators

The DPWM used with the hybrid controllers was replaced with a second order delta-sigma modulator. In this section, simulation results for each of the ANFIS-PID hybrid buck controllers covered in Chapter 3 with a Delta-Sigma (ΔΣ) will be presented and analyzed and their performance will be compared against the previous DPWM simulations.

As previously, the buck converter was designed to operate with regulated output set at 1.2 V and the input voltage of 3.3 V. The system specification used for the simulation are given in Table 4.11.

Table 4.11: System specifications used for Simulation

Parameter	Value
Input Voltage	3.3 V
Target Output Voltage	1.2 V
Inductor Value	1μH
Inductor ESR Value	20 mΩ
Capacitor Value	2 μF
Capacitor ESR Value	20 mΩ
ADC Frequency	10 MHz
ADC Resolution	8-bit
Delta-Sigma Frequency	100 MHz
Delta-Sigma Resolution	9-bit

As with the DPWM simulations, circuit simulations were done with the LFoundry's 150nm process libraries in Cadence. As before, layouts were generated for the Verilog-HDL controllers using Cadence Encounter over a silicon area of 170 by 155 micron for each.

The controller with the specified Delta-Sigma was simulated in MATLAB and in Cadence. The output voltage waveforms for MATLAB are given in Figure 4.15 and for Cadence are given in Figure 4.16.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Tables 4.12 and 4.13.

Table 4.12: MATLAB Simulation results for the ANFIS-PID hybrid controllers with Delta-Sigma Modulator

Parameter	**Switching Type I**	**Switching Type II**	**Summing**	**Product**	**ANFIS Driven PID**
Steady State Error (V)	0.0781	0.1004	0.0687	0.0004	0.054
Overshoot (%)	24.5	30.4	52.7	24.79	46.5
Rise Time (µs)	2.003	1.57	1.04	1.575	1.126
Settling Time (µs)	17.6	19.2	20.2	17.28	21.5
Output Voltage Ripple (V)	0.0054	0.0119	0.001	0.0007	0.0063

Table 4.13: Cadence Circuit Simulation results for the ANFIS-PID hybrid controllers with ΔΣ Modulator

Parameter	Switching Type I	Switching Type II	Summing	Product
Steady State Error (V)	0.0784	0.0917	0.0666	0.01
Overshoot (%)	22.1	28.9	46.3	20.18
Rise Time (μs)	2.17	1.696	1.169	1.797
Settling Time (μs)	13.504	15.14	14.4	13.42
Output Voltage Ripple (V)	0.0077	0.0061	0.0018	0.0046

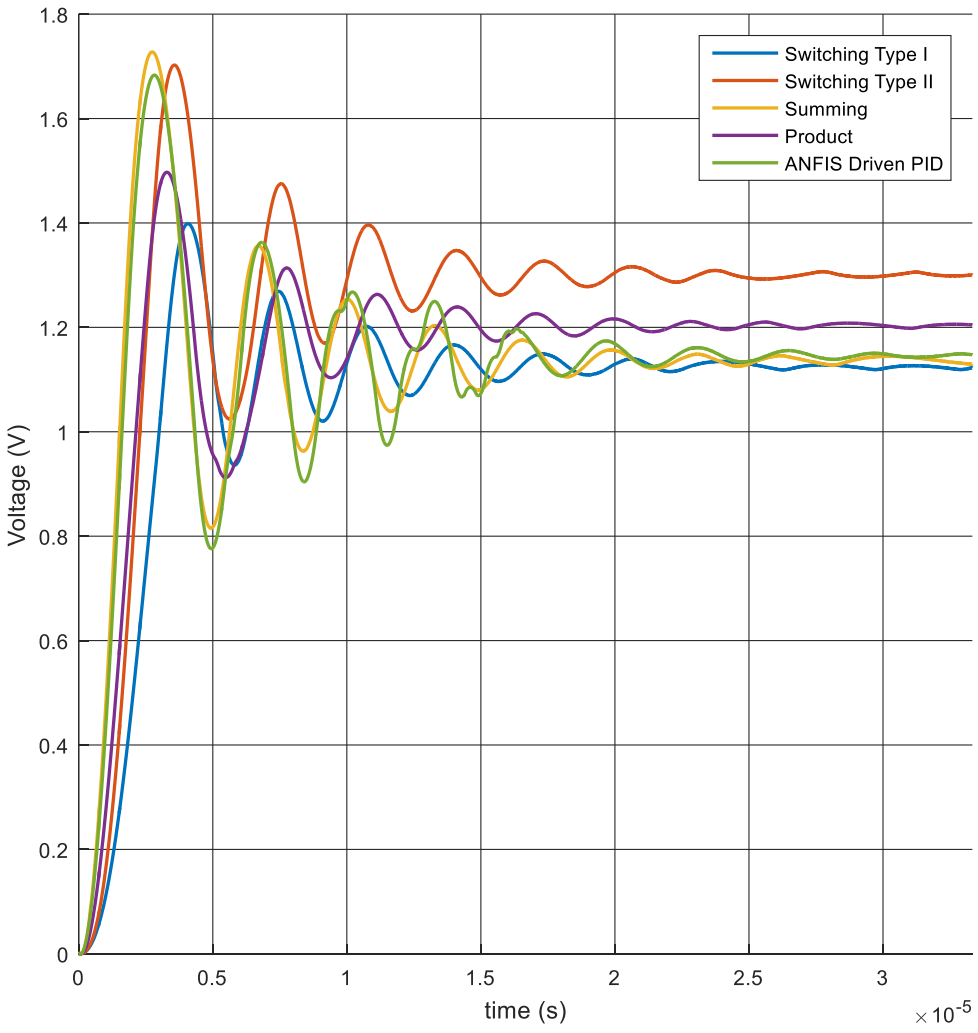


Figure 4.15: Output voltage for MATLAB simulation of the hybrid controllers with Delta-Sigma modulators

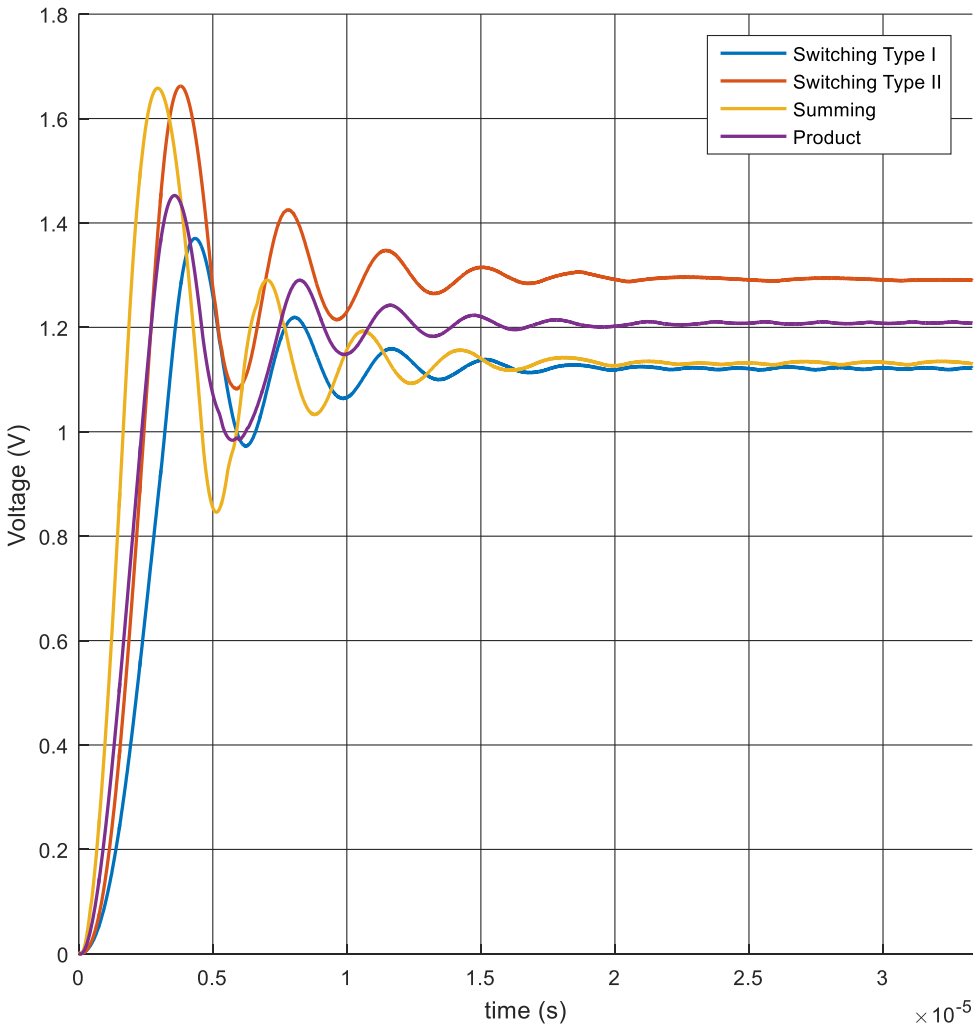


Figure 4.16: Output voltage for Cadence circuit simulation of the hybrid controllers with ΔΣ modulators

Results from each type of buck controller with the Delta-Sigma modulator were compared against the DPWM simulations. Table 4.14 shows the MATLAB simulation results compared whereas Table 4.15 shows the cirucit post layout simulation results compared. Each table list the difference between the Delta-Sigma and the DPWM. Therefore, positive values are improvements, while negative values are weaknesses.

As can be seen in the tables, in general all controllers are shown to have improved overshoot when used in conjunction with a Delta-Sigma modulator. On the other hand, the rise time is seen to increase for all hybrid controller variants. This is due to the Delta-Sigma modulators having a longer delay inherently. The switching type I hybrid also showed an improvement of approximately 0.016 V in the steady state error. The switching hybrid type II controller showed improvements of 0.02 to 0.09 V in terms of output voltage ripple. Settling time in the summing hybrid decreased by 23 to 73 us showing increased controller stability with delta-sigma modulators.

When compared against each other as presented in Tables 4.12 and 4.13, the Product hybrid controller offered the smallest steady state error, the shortest settling time, and the smallest output voltage ripple. The summing hybrid consistently showed the shortest rise times but the highest overshoots.

Table 4.14: MATLAB Simulation results for the ANFIS-PID hybrid controllers with Delta-Sigma Modulator compared against DPWM

Parameter	Switching Type I	Switching Type II	Summing	Product	ANFIS Driven PID
Steady State Error (V)	0.0169	-0.0014	0.0613	0.0186	0.026
Overshoot (%)	25.2	10.3	67.3	24.51	-1.2
Rise Time (µs)	-0.963	-0.41	-0.02	-0.505	-0.086
Settling Time (µs)	-3.81	80.54	23.7	-3.08	-11.4
Output Voltage Ripple (V)	-0.0014	0.0211	0.009	0.0034	-0.004

Table 4.15: Cadence Circuit Simulation results for the ANFIS-PID hybrid controllers with Delta-Sigma Modulator compared against DPWM

Parameter	Switching Type I	Switching Type II	Summing	Product
Steady State Error (V)	0.0166	0.0073	-0.0226	-0.003
Overshoot (%)	21.3	7.7	42.5	21.32
Rise Time (µs)	-1.01	-0.406	0.071	-0.587
Settling Time (µs)	-2.124	-6.56	73.3	-4.84
Output Voltage Ripple (V)	-0.0066	0.0929	-0.0003	-0.0034

The efficiencies of each of the ANFIS-PID hybrid controller with the delta-sigma modulators were calculated in MATLAB and plotted with respect to the load current. This can be seen in Figure 4.17. The peak efficiencies for each of the hybrid controller and their comparison with their DPWM counterparts. are given in Table 4.16.

Like with the DPWM, the arithmetic type product ANFIS-PID hybrid has the highest peak efficiency at 98.2 %. When compared with the DPWM efficiencies, utilizing a delta sigma can give us comparable, or in some cases even better, efficiency, while allowing for lower clocked and more practical ADC frequency requirements. The improved efficiency can be accounted to the reduction in output voltage ripple and overshoot. Moreover, a delta-sigma modulator clocked at the same frequency as a digital-pulse-width-modulator, consumes less power, hence making utilizing the hybrid controller with a delta-sigma modulator ideal for low power applications [21].

Table 4.16: Peak efficiencies for the hybrid controllers with Delta-Sigma Modulators and their comparison with DPWM

Hybrid Controller	Peak Efficiency	Change from DPWM
Switching Type I	88.0 %	-0.4 %
Switching Type II	96.6 %	3.7 %
Summing	89.9 %	-1.2 %
Product	98.2 %	1.7%
ANFIS Driven PID	95.5 %	2.4 %

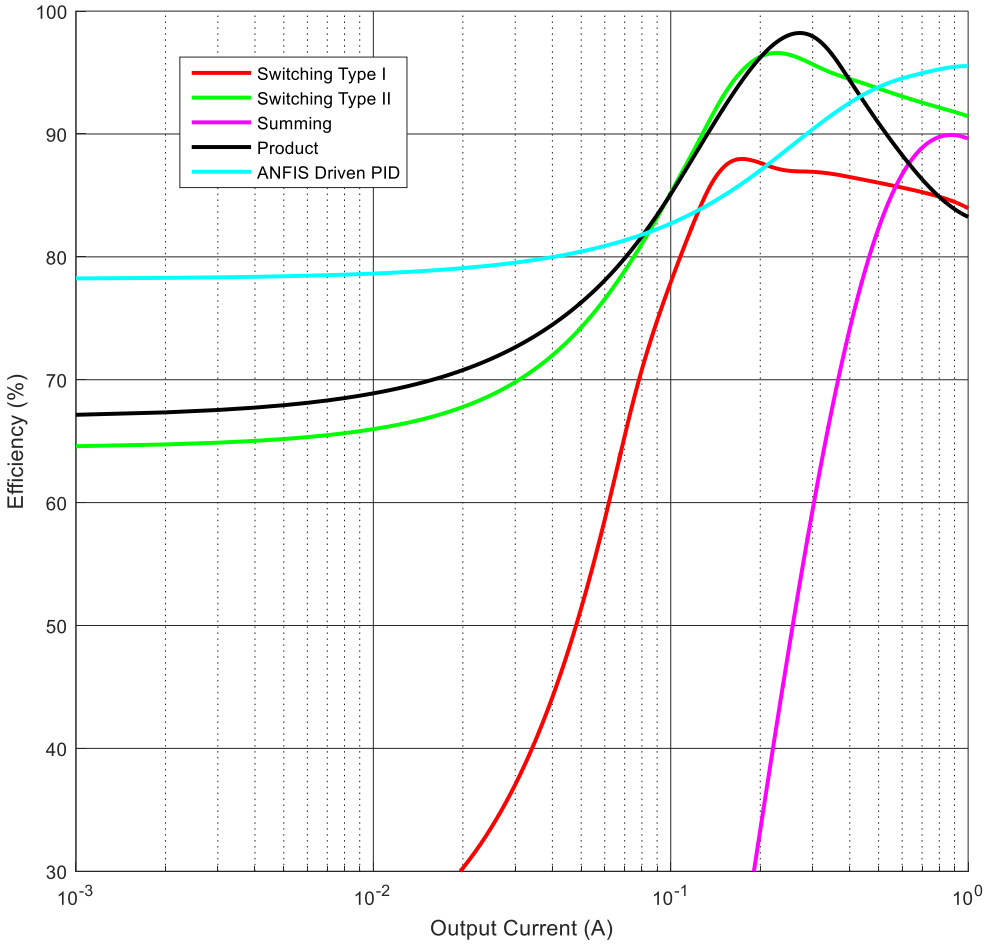


Figure 4.17: Efficiencies of each of the hybrid controller with Delta-Sigma plotted with respect to load current

4.3. Experimental Results

The proposed hybrid ANFIS-PID control techniques for buck converters were verified experimentally on an FPGA. The Intel Cyclone III LS Development Board was used for this purpose along with an external MAX1426 pipeline ADC. Results were captured using a connected oscilloscope. The full experimental setup is shown in Figure 4.18. As previously, the buck converter was set to operate with regulated output at 1.2 V and the input voltage of 3.3 V. The system specifications used for the simulation are given in Table 4.17.

Table 4.17: System specifications used for the Experimental Setup

Parameter	Value
Input Voltage	3.3 V
Target Output Voltage	1.2 V
Inductor Value	1μH
Inductor ESR Value	20 mΩ
Capacitor Value	2 μF
Capacitor ESR Value	20 mΩ
ADC Frequency	10 MHz
ADC Resolution	8-bit
Delta-Sigma Frequency	100 MHz
Delta-Sigma Resolution	9-bit

In this section, experimental results for each of the ANFIS-PID hybrid buck controllers covered in Chapter 3 with a Delta-Sigma will be presented and analyzed and their performance will be compared against the previous DPWM and Delta-Sigma simulations.

The controllers with the specified Digital Pulse-Width-Modulator and Delta-Sigma were verified experimentally. The output voltage waveforms obtained from the experimental setup via oscilloscope for the DPWM are given in Figure 4.19 and for the Delta Sigma are given in Figure 4.20.

The various transient and steady state parameters obtained from these waveforms to characterize the performance of the buck converter are given in Tables 4.18 and 4.19 for the DPWM and Delta-Sigma respectively.

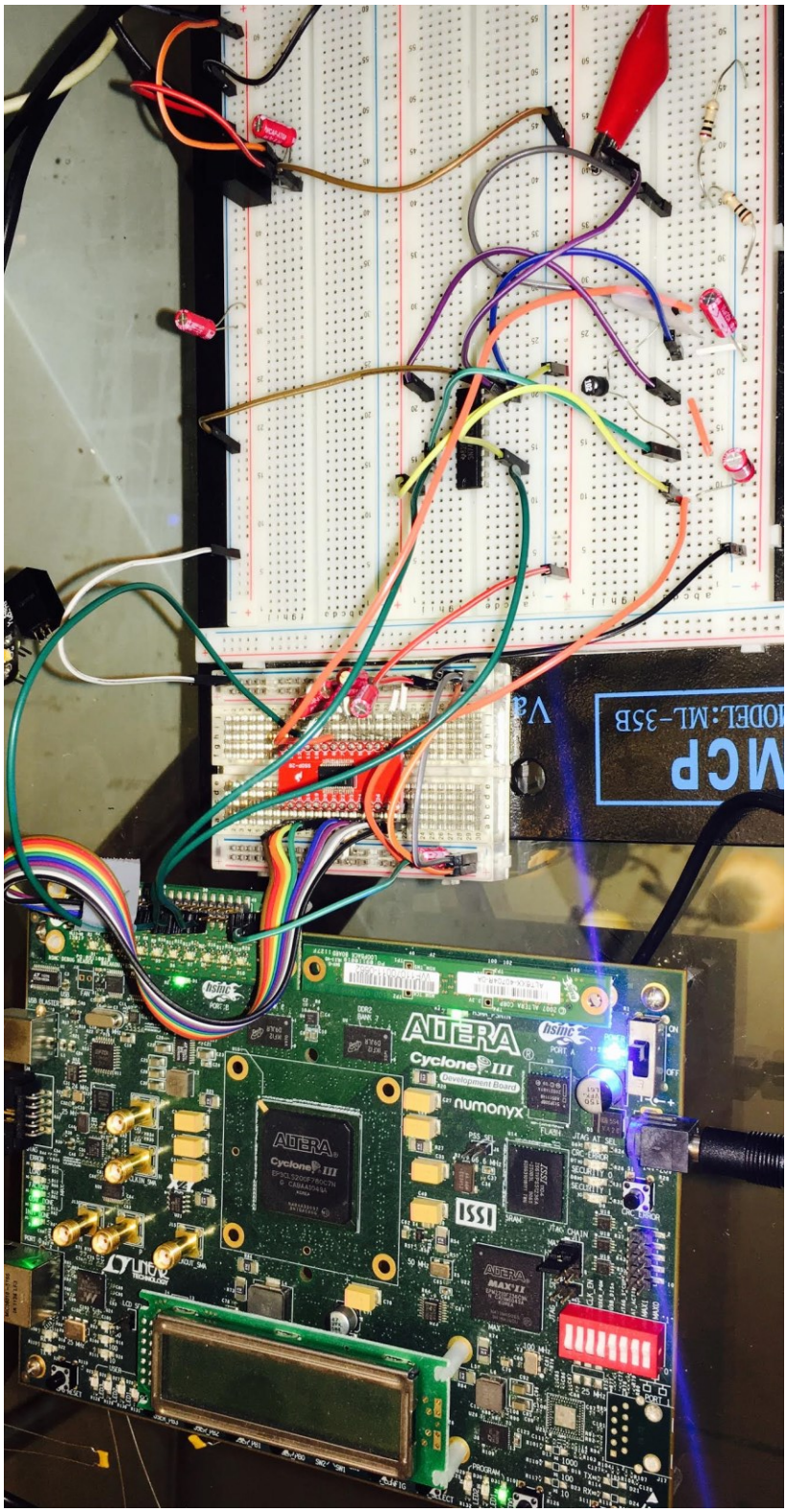


Figure 4.18: The experimental setup used for hybrid controller verification

Table 4.18: Experimental results for the ANFIS-PID hybrid controllers with Digital Pulse-Width-Modulator

Parameter	Switching Type I	Switching Type II	Summing	Product
Steady State Error (V)	0.0749	0.120	0.0093	0.011
Overshoot (%)	52.4	40.1	49.9	50.8
Rise Time (μs)	0.981	1.23	1.075	1.024
Settling Time (μs)	99.69	99.72	98.5	99.88

Table 4.19: Experimental results for the ANFIS-PID hybrid controllers with Delta-Sigma Modulator

Parameter	Switching Type I	Switching Type II	Summing	Product
Steady State Error (V)	0.0381	0.122	0.0507	0.0168
Overshoot (%)	23.7	30.1	52.9	26.0
Rise Time (μs)	2.087	1.63	1.04	1.55
Settling Time (μs)	99.75	98.63	98.48	99.88

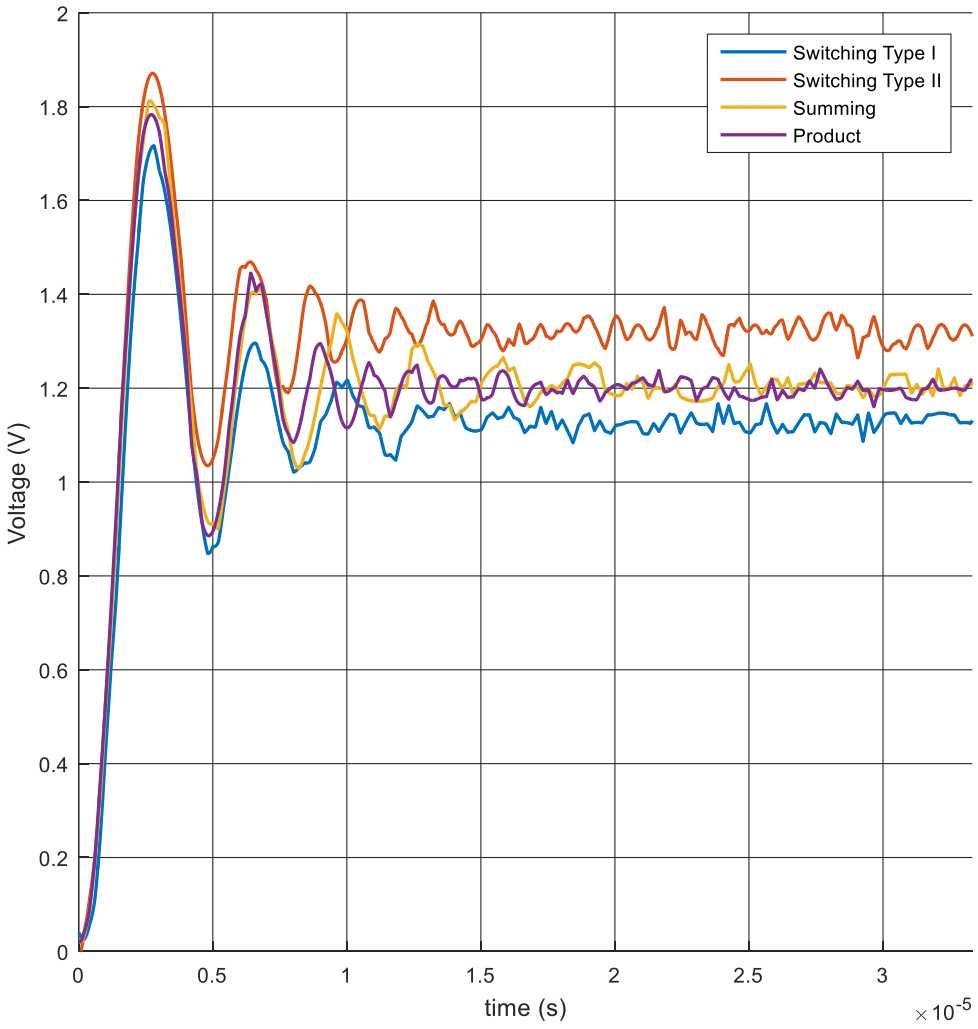


Figure 4.19: Output voltage for experimental verification of the hybrid controllers with DPWM

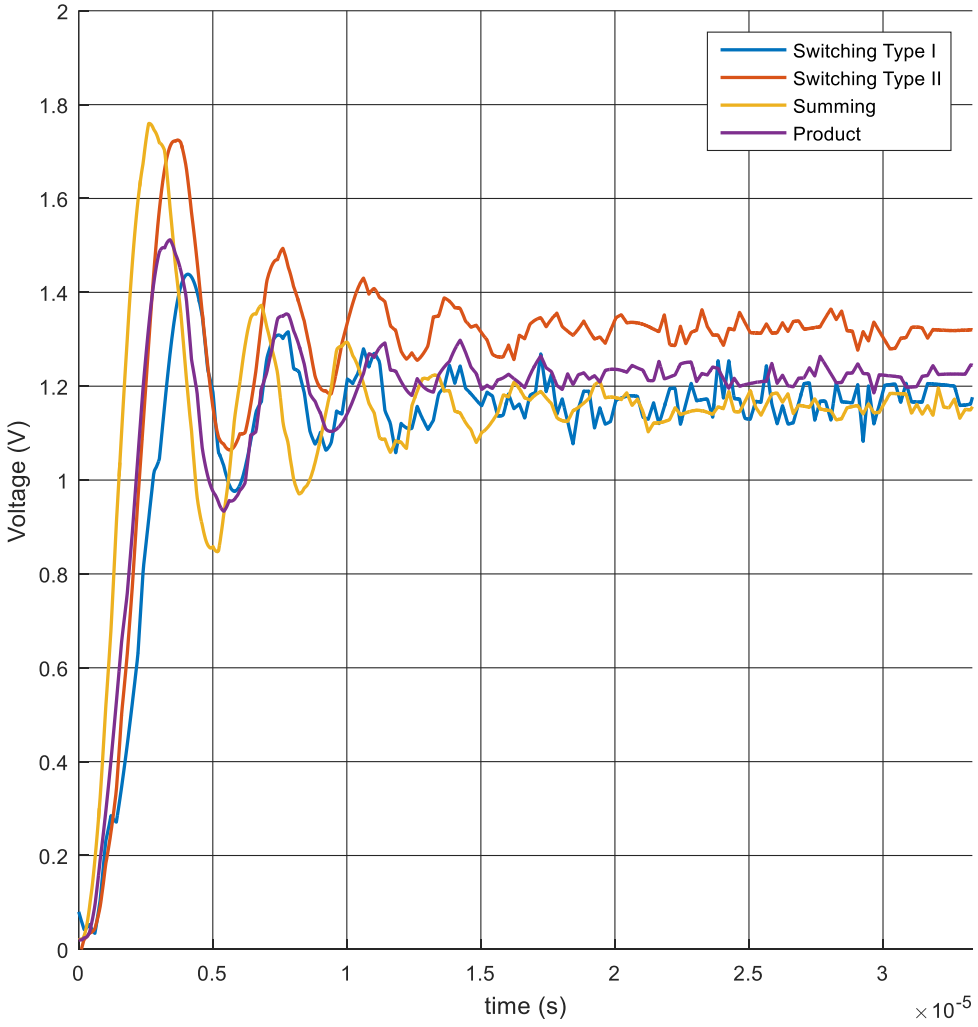


Figure 4.20: Output voltage for experimental verification of the hybrid controllers with Delta-Sigma modulator

Results from each type of buck controller were compared against the simulations. Table 4.20 shows the DPWM results compared whereas Table 4.21 shows the Delta-Sigma results compared. Each table lists both the experimental and the circuit simulation data to highlight the difference between them.

Note that due to presence of noise in the experimental results, the output voltage ripple and the settling time were not measurable and thus these results were not compared against the simulations data. On investigation, it was seen that the noise present was centered around 60 Hz, 2 MHz, and 80 MHz. This is apart from the noise attributed to the transistor switching and can be attributed to sources external from the circuit. Buck converters are highly noise sensitive, and as such the experimentally tested buck converters were seen to lose stability after approximately 0.25 seconds. This can be attributed to the breadboard implementation. To avoid this, the circuit would have to be implemented with a proper noise isolating layout on a four-layer printed circuit board.

As can be seen from Figures 4.19 and Figures 4.20, the proposed hybrid controllers were successfully implemented experimentally and tested on FPGA. The difference from the Cadence circuit simulation data is presented in Tables 4.20 and 4.21. Minimal difference within reasonable limits was seen from the simulation results which can be attributed to the stray coupling capacitances and additional resistance involved with a breadboard implementation, thus verifying the hybrid controller operation.

Table 4.20: Experimental & Simulation results for the ANFIS-PID hybrid controllers with DPWM summarized

Parameter	Simul. Switching Type I	Exper. Switching Type I	Simul. Switching Type II	Exper. Switching Type II	Simul. Summing	Exper. Summing	Simul. Product	Exper. Product
Steady State Error (V)	0.095	0.0749	0.099	0.120	0.044	0.0093	0.007	0.011
Overshoot (%)	43.4	52.4	36.6	40.1	88.8	49.9	41.5	50.8
Rise Time (μs)	1.16	0.981	1.29	1.23	1.24	1.075	1.21	1.024

Table 4.21: Experimental & Simulation results for the ANFIS-PID hybrid controllers with ΔΣ summarized

Parameter	Simul. Switching Type I	Exper. Switching Type I	Simul. Switching Type II	Exper. Switching Type II	Simul. Summing	Exper. Summing	Simul. Product	Exper. Product
Steady State Error (V)	0.0784	0.0381	0.0917	0.122	0.0666	0.0507	0.01	0.0168
Overshoot (%)	22.1	23.7	28.9	30.1	46.3	52.9	20.18	26.0
Rise Time (μs)	2.17	2.087	1.696	1.63	1.169	1.04	1.797	1.55

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1. Conclusion

In this thesis, five hybrid ANFIS-PID controllers for DC-DC buck converters were presented and analyzed targeting for SoC applications. Two hybrids, Selecting Type I and Type II, were classified to a Logical Hybrid class and another two, Summing and Product, were classified to an Arithmetic class of ANFID-PID hybrids. The last hybrid controller was the ANFIS-Driven-PID. Each of the presented controllers was implemented and simulated in MATLAB Simulink and in Cadence IC Design Suite. Also, the controllers were implemented using Verilog HDL for FPGA-based experimental verification. For both simulation, the hybrid controllers were tested with DPWMs and Delta-Sigma modulators.

It was seen in this thesis that the proposed controllers provide a variety of performance improvements when compared to traditional PID with DPWM based controllers for buck converters. The hybrids used in conjunction with DPWMs showed improvements of 6-9 % overshoot for the Switching Type II hybrid controller, steady state error and the overshoot by 0.03 to 0.04 V and 0.1 to 1.2 % respectively for the Product hybrid, and approximately 4 percent to the overshoot, 0.02 μs to the rise time, 3.1 μs to the setting time and 2 mV to the output voltage ripple for the ANFIS-Driven-PID. Efficiency compared to the reference PID controller was also seen to improve from 92.7 % to the highest efficiency of 96.5% for the product ANFIS-PID hybrid among all the presented hybrids. Commercially available buck converters with PWMs possess peak efficiency

ranging between 88 to 94%. An increase of approximately 2 % efficiency is a significant improvement.

Utilizing Delta-Sigma modulators instead of DPWMs showed improved overshoots but longer rise times for all hybrids compared to their DPWM counterparts across the board. Additionally, the Switching Type I hybrid showed an improvement of 0.016 V in the steady state error, the Switching Type II showed improvements of 0.02 to 0.09 V in terms of output voltage ripple, and the Summing hybrid improved by 23 to 73 us showing increased controller stability with delta-sigma modulators. Efficiencies with delta-sigma modulators mostly improved with the highest efficiency being 98.2 % for the Product hybrid. Thus, Delta-Sigma modulators are a better alternative to DPWMs, while allowing avoidance of the high and impractical power requirements of high clocked DPWMs and sacrificing rise time.

5.2. Future Work

The work done in this thesis can be extended proposing more complex logical or hybrid ANFIS-PID controllers. These can range from complex boolean equations to polynomials. These could allow precise tuning of the various regions of the buck converters performance. Furthermore, more than two controllers should be used, for example, two differently trained ANFIS controllers with a PID. Also, DPFMs should be tested with the buck converters to investigate any performance improvements. Finally, the proposed hybrid controllers should be extended to work with other DC-DC converter topologies, namely the boost and the buck-boost converters.

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