# DESIGN OF A PROGRAMMABLE WIDEBAND MICROWAVE FEED NETWORK 

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## DEANSHIP OF GRADUATE STUDIES

This thesis, written by SAMEIR ELSAYED DEIF under the direction of his thesis adviser and approved by his thesis committee, has been presented to and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL ENGINEERING DEPARTMENT.

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To my parents, Dawlat and Sameir,
To my beloved wife, Nesma, To my beautiful daughter, Renad.

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In the name of God and prayer and peace be upon the Messenger of Allah Muhammad, peace be upon him - and his family and companions and blessings.

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# THESIS ABSTRACT 

NAME: $\quad$ Sameir Elsayed Deif<br>TITLE OF STUDY: Design of A Programmable Wideband Microwave Feed Network<br>MAJOR FIELD: Electrical Engineering Department<br>DATE OF DEGREE: May 2013

The design and fabrication of a wide-band programmable microwave feed network is proposed. The design architecture is composed of four main stages, switching, phase shifting, amplification/attenuation and control. The proposed feed network is designed to cover a wide band from 2.5 to 6 GHz over two separate branches, one covers from 2.5 to 3 GHz and the other covers from 3 to 6 GHz. Digitally controlled phase shifters are used to control the phase. A digital control unit is used to provide the required control signals for all the feed network stages. Digitally controlled wide-band variable gain amplifiers are used to set the appropriate amplitude to the signal in both paths.

The feed network is simulated and fabricated on an FR-4 substrate with thickness of 0.8 mm . Good matching between simulation and measurement results is
achieved.The measured amplitude resolution was 0.5 dB with an error of less than $+0.22 /-0.12 \mathrm{~dB}$. The measured phase resolution was approximately $5.625^{\circ}$ with an error of less than $\pm 1^{\circ}$. This value of phase resolution can achieve a scanning beam resolution of $1.8^{\circ}$ for a linear antenna array. Also, the sidelobe levels can be controlled by amplitude tapering functionality of the proposed network. The proposed network is a generic two-path design that can be used as a standalone network to feed any kind of array system. The size of the two-path feed network was $110 \times 63 \times 0.8 \mathrm{~mm}^{3}$.

Since the feed network needs a kind of combiner circuit to combine all the outputs from the network to the input of a transceiver, a compact size 12-port microwave combiner with phase compensation is designed and fabricated. The combiner covers the band from 2.3 to 3 GHz . Its size was $78.5 \times 61 \times 0.8 \mathrm{~mm}^{3}$.

## الخناصة

الابي : سمير السيد ضيف

عنوان الدراسة: تصميم شبكة تغذية ميكروويف واسعة النطاق ومبرجة ذاتياً
القسم : الهندسة الكهربائية

في هذا العمل تم تصميم وصنع شبكة تغذية ميكروويف واسعة النطاق ومبرجة ذاتيا. تتكون بنية التصميم من أربع مراحل أساسية، التبديل، إزاحة الطور، توهين ومرحلة التحكم. صُممت هذه الشبكة لكي تغطي نطاق ترددي من ارْ با إلى 1 جيجاهيرتز. مغيري الطور يتم التحك بهم رقميا للتحك في الطور. وحدة تحكى رقية تستخدم للتحكى في جميع مراحل شبكة التغذية. لإعطاء الإتساع الطلوب يتم استخر الخدام مكبرات متغيرة التكبير رقميا.

تمت المحاكاة والتصنيع للشبكة على لوحة من مادة (FR-4) بُممك يساوي 入•• مـ توافق جيد بين نتأج المحاكاة والتتائج العملية تم تحقيقه. دقة الإتساع المقاس عمليا كانت 0.. ديسيبل . بخطأ مقدارة أقل من 0.12-0.22+ ديسيبل. كما كانت دقة الطور تقريبا حوالي
 درجة. كما يمكن التحك في مستوى الفصوص الجانبية بإستخدام خاصية الإتساع المتغير لهذه الشبكة. الشبكة المصمة هي شبكة بفرعين كما أنها متعددة الإستخدام والتي يمكن أن تستخدم لتغذية أي نظام مكون من مصفوفة. أبعاد الشبكة المصمة كان $110 \times 63$ ج

$$
0.8 \text { مع }{ }^{3}
$$

لأن الشبكة تحتاج نوع من المجمع لتجميع كل النواتج إلى مدخل جهاز الإرسال والإستقبال، تم تصميم وتصنيع جمع صغير الحجم ذو Ir آ منفذ. هذا المجمع صُم لنطاق


## CHAPTER 1

## INTRODUCTION

Programmable and tunable microwave circuits are attractive to microwave researchers because they offer flexibility and are needed in reconfigurable systems. These circuits can be digitally programmed and can be used for various functions based on specific needs. The design of dynamic reconfigurable microwave circuits operating at high frequencies seems to be a challenging task. However, these kind of circuits can be realized due to the advancement in Digital Signal Processing (DSP), microcontrollers and Field-Programmable Gate Array (FPGA) technology [1].

Radio Frequency (RF)/microwave feed networks can be constructed from a number of different high frequency circuit technologies for precise control of antenna patterns over a wide bandwidth. These networks can be used in military electronic systems, typically to control the signal amplitude and phase of multiple antennas or radiating elements in applications such as jammers, phased-array radar systems, and Unmanned Aerial Vehicles (UAV). They can be quite simple
or complex, depending on the number of processing signal beams, and can be used for both transmission and reception.

Early designs were typically fixed-beam architectures. Recent configurations include complex adaptive beam forming networks. These networks can be formed with either active or passive configurations, printed circuit board or fabricated with Microwave Monolithic Integrated Circuits (MMIC) technology. Phased array antennas are complex systems with a combination of multidisciplinary designs encompassing array synthesis and analysis, design of RF feed networks, design of phase shifters biasing network, electronic switching control and programming the control algorithm with either a microcontroller or a Field Programmable Gate Array (FPGA).

For lower power consumption, short set-up time, easy to program and easy to change the design functionality, lower cost, and small size, we propose a design of a programmable RF feed network controlled by a microcontroller unit. The feed network will be a wideband one that covers wireless communications standards that lie between 2.5-6.0 GHz.

### 1.1 Thesis Objectives

The thesis objectives are as follows:

1. To come up with a wideband microwave feed network architecture that is digitally programmable in both phase and amplitude. Two-path (simulation
and fabrication) and four-path versions (simulation) will be investigated.
2. To model and analyze the performance of the programmable wideband feed network and optimize its on-board performance.
3. To fabricate and test the performance of a 2-path programmable wideband feed network in the laboratory environment.
4. To come up with a complete program for controlling the phases and amplitudes of the feed network on a microcontroller board/chip.

### 1.2 Thesis Organization

The organization of this work is as follows, RF circuits fundamentals and design parameters are discussed in Chapter 2. Chapter 3 includes a detailed literature review in the area of feed networks and beamformers. The architecture and the design of the proposed feed network, PCB design, the fabricated model and the microcontroller unit are described in Chapter 4. Chapter 5 discusses the measured results for the proposed model. The 12-port combiner/splitter and its design process are discussed in Chapter 6 and finally Chapter 7 states the conclusions and future work.

## CHAPTER 2

## BACKGROUND

### 2.1 RF Circuits: Design and Parameters

In this section we will describe some basic RF design concepts and parameters that are used to characterize passive and active RF circuits. Then, the basic ideas of multi-beam networks and beamformers will be discussed in details.

### 2.1.1 Microstrip Transmission Lines

The planar transmission lines has the advantages of ease of fabrication and ease of integration with other microwave circuit devices. The stripline, microstrip line and slotline are examples of planar transmission lines. The most popular type of these lines is the microstrip line [2]. The structure of the microstrip line is a flat strip conductor of with $(W)$ suspended above a ground plane by a thin dielectric material substrate of thickness $(h)$ and relative permeability $\left(\varepsilon_{r}\right)$.


Figure 2.1: Structure and dimension of microstrip transmission line.

As shown in Figure 2.1 [2], microstrip has some (usually most) of its field lines in the dielectric region, concentrated between the strip conductor and the ground plane, and some fraction in the air region above the substrate. So, the microstrip line cannot support a pure TEM wave. The exact field of the microstrip line is very complex and constitute of a hybrid TM-TE waves. When the longitudinal components of the field for the dominant mode of a microstrip line is much smaller than the transverse components $(h \ll \lambda)$, the quasi-TEM approximation is applicable to facilitate design. So, by using this assumption, the phase velocity, propagation constant, and characteristic impedance can be obtained from static or quasi-static solutions. The guided wavelength of a microstrip line is given by:

$$
\begin{equation*}
\lambda_{g}=\frac{\lambda_{o}}{\sqrt{\varepsilon_{r e}}} \text { or } \lambda_{g}=\frac{300}{f(G H z) \sqrt{\varepsilon_{r e}}} m m \tag{2.1}
\end{equation*}
$$

where $\varepsilon_{r e}$ is the effective dielectric constant or the microstrip line (the equivalent dielectric constant to the air and the substrate together). Thus this value should
satisfy the following relation in (2.2) and can be calculated from (2.3).

$$
\begin{gather*}
1<\varepsilon_{r e}<\varepsilon_{r}  \tag{2.2}\\
\varepsilon_{r e}=\left\{\begin{array}{l}
\frac{\varepsilon_{r}+1}{2}+\frac{\varepsilon_{r}-1}{2}\left(1+\frac{12 h}{W}\right)^{-0.5}+0.04\left(1-\frac{W}{h}\right)^{2} ; \text { for } \frac{W}{h} \leq 1 \\
\frac{\varepsilon_{r}+1}{2}+\frac{\varepsilon_{r}-1}{2}\left(1+\frac{12 h}{W}\right)^{-0.5} ; \text { for } \frac{W}{h}>1
\end{array}\right. \tag{2.3}
\end{gather*}
$$

where, $W$ and $h$ represent the width and height of the transmission line, respectively. The characteristic impedance $\left(Z_{O}\right)$, given these line dimensions, can be calculated in (2.4).

$$
Z_{o}=\left\{\begin{array}{l}
\frac{\eta}{2 \pi \sqrt{\varepsilon r e}} \ln \left(\frac{8 h}{W}+\frac{0.25 W}{h}\right) ; \text { for } \frac{W}{h} \leq 1  \tag{2.4}\\
\frac{\eta}{\sqrt{\varepsilon r e}} \frac{W}{h}+1.393+0.677 \ln \left(\frac{W}{h}+1.4444\right)^{-1} ; \text { for } \frac{W}{h}>1
\end{array}\right.
$$

The propagation constant $(\beta)$ of such a line is given by,

$$
\begin{equation*}
\beta=\frac{2 \pi}{\lambda_{g}} \tag{2.5}
\end{equation*}
$$

while it's phase velocity $\left(\nu_{p}\right)$ is found from,

$$
\begin{equation*}
\nu_{p}=\frac{\omega}{\beta}=\frac{c}{\sqrt{\varepsilon_{r e}}} \tag{2.6}
\end{equation*}
$$

A microstrip electric length is $(\theta)$ and it is defined as,

$$
\begin{equation*}
\theta=\beta l \tag{2.7}
\end{equation*}
$$

There are many calculators available on the internet like AppCAD form Agilent, emtalk [3], and TXLINE [4] which is embedded in the Microwave Office (MWO) software that can be used to get the proper microstrip patameters based on its geometry and substrate type. Figure 2.2 shows an example for the synthesis of a microstrip line using the TXLINE software. A $50 \Omega$ microstrip on an RT/Duroid 5880 substrate of $\epsilon_{r}=4$ and loss tangent $\tan (\delta)$ of 0.03 should be 0.5 mm wide on a substrate thickness of 10 mils $(0.254 \mathrm{~mm})$.


Figure 2.2: Microstrip design example by TXLINE software.

There are several RF design concepts that should be taken into consideration during the design process. For a two-layer board (our design), the power stage, RF signal lines and RF components should be all on one layer (Top Layer) and the other layer (Bottom Layer) must be the ground (GND) plane. In the coming few sections, more details will be given on these concepts and parameters.

### 2.1.2 Layout Design Fundamentals

RF layout is usually based on microstrip lines as the wave moves faster compared to a stripline structure. In addition, the traces and connections need to be done in a way to avoid impedance discontinuities such as $90^{\circ}$ bends and vias. The separation between adjacent lines is also important to avoid crosstalk. Each of these issues will be discussed with some details in the points and definitions to come.

Crosstalk The crosstalk is defined as the mutual influence of two nearby routed parallel traces or lines such as telephone lines, data lines, or system components. One of these two traces that carry the signal is called the aggressor and the other one is called the victim that is influenced by the aggressor. This occurs because of the inductive and capacitive coupling between these two traces. This effect can only appear in microstrip lines and can be canceled completely in stripline structures. So, we must keep the traces apart from each other at least 2 times the trace width to avoid or at least minimize crosstalk. Also crosstalk can occur between layers and to minimize this effect we need to route the line $90^{\circ}$ to each other on different layers.

Vias The use of vias is important in any RF design. They are used to provide stability and trace connections on various layers. Vias increase the trace length, generate additional inductance and capacitance, and reflections can occur due to impedance change.

Also when connecting the ground pins of RF Integrated Circuits (ICs), using Vias, it should be connected to the ground plane by the shortest way. In a stripline board, a sufficient number of via holes should be used to reduce the unwanted effects of the ground.

RF T-Line bends The design of the RF bend is very important and effective. The worst way for designing a bend is to use the right angle one because it has a huge amount of radiation. This is because right angle bend change the impedance at the corner due to the capacitance generated. It is not recommended to use the right-angle bends since it is the most lossy configuration for the RF bends. This is shown in Figure 2.3.


Figure 2.3: Different design of right angle bends, worst to best from left to right.

In our design, we used Optimally Mitered bends (MBEND3 in MWO). The Mitered bend geometry as designed in MWO is shown in Figure 2.4 [5].


Figure 2.4: The structures and the design parameters of the mitered BEND.

An optimum miter based on the dimensions shown in Figure 2.4 can be found from [5]:

$$
\begin{equation*}
\frac{X}{D}=0.52+.65 \times e^{-1.35 \times(W / H)} \tag{2.8}
\end{equation*}
$$

where, H is the substrate thickness. Mitered bend has the range of use according to (2.9).

$$
\begin{equation*}
0.5 \leq \frac{W}{H} \leq 2.75,2.5 \leq \varepsilon_{r} \leq 25 \text { and } f \leq \frac{15}{H(m m)}(G H z) \tag{2.9}
\end{equation*}
$$

here $f$ is the simulation frequency. Finally, the printed mitered bend that is used in our design is shown in Figure 2.5.


Figure 2.5: Printed mitered bend.

### 2.1.3 S-Parameters

A two-port network can be represented by different parameters such as an impedance matrix $(\mathrm{Z})$, admittance matrix $(\mathrm{Y})$, hybrid matrix $(\mathrm{H})$, ABCD matrix, and S-parameters (S). At microwave frequencies $\mathrm{Z}, \mathrm{Y}, \mathrm{H}$, and ABCD parameters are very difficult if not impossible to measure. The reason is that short and open circuit conditions to AC signals are difficult to implement over a broadband at microwave frequencies. Also, an active two-port might oscillate under short or open-circuit conditions. Therefore, a more appropriate representation of the two-port network at microwave frequencies is needed.

The S-parameters are seen to represent reflection or transmission coefficients. The S-parameters are measured at the specific locations shown as Port 1 and Port 2 in Figure 2.6 and are defined as follows [6];

$$
\begin{equation*}
S_{11}=\left(\frac{b_{1}}{a_{1}}\right)_{a_{2}=0} \tag{2.10}
\end{equation*}
$$

$S_{11}$ : Input reflection coefficient with output properly terminated.

$$
\begin{equation*}
S_{21}=\left(\frac{b_{2}}{a_{1}}\right)_{a_{2}=0} \tag{2.11}
\end{equation*}
$$

$S_{21}$ : Forward transmission coefficient with output properly terminated.

$$
\begin{equation*}
S_{22}=\left(\frac{b_{2}}{a_{2}}\right)_{a_{1}=0} \tag{2.12}
\end{equation*}
$$

$S_{22}$ : Output reflection coefficient with input properly terminated.

$$
\begin{equation*}
S_{12}=\left(\frac{b_{1}}{a_{2}}\right)_{a_{1}=0} \tag{2.13}
\end{equation*}
$$

$S_{12}$ : Reverse transmission coefficient with input properly terminated.


Figure 2.6: S-parameters for two-port network.

The advantage of using the S-parameters is that they are measured using matched conditions. Using matched resistive terminations to measure the S-parameters of an amplifier has the advantage that the amplifier does not oscillate. Also, the S-parameters can be cascaded easily to predict the system performance. Most of the simulation tools also can generate the S-parameters easily in different format. Finally, all the other parameters such as Y, Z, etc can be computed by knowing the S-parameters.

### 2.1.4 Noise

Noise is usually generated by the random motions of charges or charge carriers in devices and materials. Several mechanisms that generate noise in active circuits are thermal noise, shot noise, flicker noise, plasma noise, and quantum noise. Because of the fact that, the thermal noise is the most important type of noise and it is the dominant one, we are going to discuss it in details in the next section.

Thermal Noise [7]: Any matter above 0K contains thermal energy that moves atoms and electrons around in a random way, leading to random currents,
which are considered noise or thermal noise. The thermal noise spectral density in a resistor is given by

$$
\begin{equation*}
N_{\text {resistor }}=4 k T R \tag{2.14}
\end{equation*}
$$

where $T$ is the Kelvin temperature of the resistor, $k$ is Boltzman constant $\left(1.38 \times 10^{-23} J / K\right)$, and $R$ is the value of the resistor. Thermal noise is white noise, meaning it has a constant power spectral density with respect to frequency (i.e. wideband).

The output power spectral density when maximum power transfer occurs $\left(P_{o}\right)$ is given by

$$
\begin{equation*}
P_{o}=\frac{v_{n}^{2}}{4 R}=k T \tag{2.15}
\end{equation*}
$$

where $v_{n}$ is the rms value of the noise voltage and is given as a function of the bandwidth $\Delta \mathrm{f}$ by

$$
\begin{equation*}
v_{n}=4 k T F \Delta f \tag{2.16}
\end{equation*}
$$

It is clear from (2.15) that the available power is independent of the resistor. The total output power is given as a function of the bandwidth $B(H z)$ by

$$
\begin{equation*}
P_{o u t}=k T B \tag{2.17}
\end{equation*}
$$

For any receiver required to receive a given signal bandwidth, the minimum detectable signal can now be determined. As was seen in (2.17), the noise
floor depends on the bandwidth $B$. The signal-to-noise ratio (SNR) can be determined by

$$
\begin{equation*}
S N R=\frac{S}{\text { NoiseFloor }} \tag{2.18}
\end{equation*}
$$

where $S$ is the signal power. By considering there is no noise added to the circuit from other electronics, the Noise floor is given from (2.17) by

$$
\begin{equation*}
\text { NoiseFloor }=k T B=-174 d B m / H z+10 \log _{10} B(d B m) \tag{2.19}
\end{equation*}
$$

The noise floor of a receiver determines its sensitivity to low-level signals and its capability of detecting and demodulating those signals.

Noise added by the electronics will be directly added to the noise from the input [8]. Noise from electronics is described by the NoiseFactor (F), which is a measure of how much the signal-to-noise ratio is degraded through the system and is given by [9]

$$
\begin{equation*}
F=\frac{S_{i} / N_{i(\text { Source })}}{S_{o} / N_{o(\text { Total })}} \tag{2.20}
\end{equation*}
$$

where $N_{o(t o t a l)}$ is the total noise at the output which is given by

$$
\begin{equation*}
N_{o_{(\text {total })}}=N_{o_{(\text {source })}}+N_{o_{(\text {added })}} \tag{2.21}
\end{equation*}
$$

and $N_{o(\text { source })}$ is the noise at the output originating from the source, and $N_{o_{(\text {added })}}$ is the noise at the output added by the electronic circuitry. The

Noise Figure (NF) is related to Noise Factor $(F)$ by

$$
\begin{equation*}
N F=10 \log _{10} F \tag{2.22}
\end{equation*}
$$

The NF is a measure of the degradation in the Signal-to-Noise ratio between the input and the output of the component, and thus,

$$
\begin{equation*}
F=\frac{S_{i} / N_{i}}{S_{o} / N_{o}} \geq 1 \tag{2.23}
\end{equation*}
$$

For the cascaded system shown in Figure 2.7, the cascaded NF can be calculated by the relation:

$$
\begin{equation*}
F_{c a s}=F_{1}+\frac{1}{G_{1}}\left(F_{2}-1\right) \tag{2.24}
\end{equation*}
$$



Figure 2.7: Noise figure for a cascaded system.
where $F_{1}$ and $F_{2}$ are the noise figures of the first and second stages, respectively. $G_{1}$ and $G_{2}$ are the gains of the first and second stages, respectively.

### 2.1.5 Linearity Metrics of RF Circuits

In real devices, and unlike ideal systems, the transfer function or the relationship between the input and output is not linear. The most common source of the non-linearity in RF circuits is the amplifier.

In this section, we will show the definitions of some amplifier metrics such as the $1-\mathrm{dB}$ compression point and the third-order intercept point. Also, stability and sensitivity definitions will be discussed.

Third Order Intercept Point [10] The most common way to test the linearity of a circuit is to apply two signals at the input (two-tone test), having equal amplitude and offset by some frequency. Figure 2.8 shows the third-order intercept point of a real amplifier as a function of the input power. The output of the non-linear system can be written as a power series of the form

$$
\begin{equation*}
v_{\text {out }}=k_{0}+k_{1} v_{i n}+k_{2} v^{2}{ }_{i n}+k_{3} v_{i n}^{3}+\ldots \tag{2.25}
\end{equation*}
$$

, where $v_{\text {in }}$ and $v_{\text {out }}$ are the input and output waves of the system, and $k^{\prime} s$ are the series coefficients. For the tone-tone test, the input $v_{i n}$ will be in the form

$$
\begin{equation*}
v_{i n}=v_{1} \cos \omega_{1} t+v_{2} \cos \omega_{2} t \tag{2.26}
\end{equation*}
$$

From the plot, the third-order intercept point(IP3) is determined. The thirdorder intercept point is a theoretical point where the amplitudes of the intermodulation tones at $2 \omega_{1}-\omega_{2}$ and $2 \omega_{2}-\omega_{1}$ are equal to the amplitudes of the fundamental tones at $\omega_{1}$ and $\omega_{2}$. The output voltage at the third-order intercept point $\left(v_{I P 3}\right)$ can be calculated by

$$
\begin{equation*}
v_{I P 3}=2 \sqrt{\frac{k_{1}}{3 k 3}} \tag{2.27}
\end{equation*}
$$



Figure 2.8: Third-order intercept point.

The third-order intercept point (IP3 ) can be defined either with respect to the input (IIP3) or the output (OIP3 ) power of the circuit as shown in Figure 2.8 [11].

1-dB Compression Point [10]: The $1-\mathrm{dB}$ compression point is simply the power level, specified at either the input or the output, where the output power is $1-\mathrm{dB}$ less than it would have been in an ideally linear device. The

1 - dB compression point is shown in Figure 2.9. Figure (2.9a) shows the input power versus output power. From this figure, we can get the $1-\mathrm{dB}$ point with respect of the input or the output. Figure (2.9b) shows the gain versus input power [9].

(a) Input power vs. output power

Figure 2.9: 1 dB Compression Point.

The $1-\mathrm{dB}$ compression voltage is given by

$$
\begin{equation*}
v_{1 d B}=0.22 \sqrt{\frac{k_{1}}{|k 3|}} \tag{2.28}
\end{equation*}
$$

where $k_{1}$ and $k_{3}$ are found from (2.25).

Typically, for solid state power amplifier, the third-order output intercept point is 10 dB higher than the output power at the $1-\mathrm{dB}$ compression point.

Error Vector Magnitude Error Vector Magnitude (EVM) is a very important
parameter to measure how accurately a transmitter has reproduced the vectors that correspond to the data being transmitted. EVM is the magnitude of the error vector, and is different from the magnitude error between the actual and reference constellation points. Figure 2.10 shows the error vector magnitude .

The instantaneous value of the EVM is defined as the ratio of the magnitude of the reference vector to the magnitude of the error vector

$$
\begin{equation*}
E V M_{i}=\frac{\left|e_{i}\right|}{\left|a_{i}\right|} \tag{2.29}
\end{equation*}
$$

where $e_{i}$ is the $i^{t h}$ error vector and $a_{i}$ is the $i^{t h}$ reference vector.


Figure 2.10: Error vector magnitude.

### 2.1.6 Stability of Active Circuits

The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design and can be determined from the $S$ Parameters, the matching networks, and the terminations. In an amplifier, the oscillation is possible if either the input or output port impedances have a negative real part, or in other words, when $\left|\Gamma_{\text {in }}\right|>1$ or $\left|\Gamma_{\text {out }}\right|>1$, where $\left|\Gamma_{\text {in }}\right|$ and $\left|\Gamma_{\text {out }}\right|$ are the input and output reflection coefficients, respectively. We have two types of stability:

1. Unconditional stability: The network is unconditionally stable if $\left|\Gamma_{i n}\right|<1$ and $\left|\Gamma_{\text {out }}\right|<1$ for all passive source and load impedances.
2. Potentially unstable: This happen if $\left|\Gamma_{i n}\right|<1$ and $\left|\Gamma_{\text {out }}\right|<1$ for a certain range of passive source and load impedances and not all ranges/values.

A convenient way of expressing the necessary and sufficient conditions for unconditional stability is

$$
\begin{equation*}
K>1 \text { and }|\Delta|<1, \tag{2.30}
\end{equation*}
$$

where

$$
\begin{gather*}
K=\frac{1-\left|S_{11}\right|^{2}-\left|S_{22}\right|^{2}+|\Delta|^{2}}{2\left|S_{12} S_{21}\right|}  \tag{2.31}\\
\Delta=S_{11} S_{22}-S_{12} S_{21}, \tag{2.32}
\end{gather*}
$$

where $K$ is called the stability factor.

Another form for the stability condition is:

$$
\begin{equation*}
K>1 \text { and }|B|>0, \tag{2.33}
\end{equation*}
$$

where $B$ is the stability measure and can calculated using:

$$
\begin{equation*}
B=1+\left|S_{11}\right|^{2}-\left|S_{22}\right|^{2}-|\Delta|^{2} \tag{2.34}
\end{equation*}
$$

These factors and their variants can be used to predict amplifier stability from S-parameter measurements.

### 2.2 Beamformers

Beamformers are complex networks used to precisely control the phase and amplitude of RF energy passing through them. When an array of N elements is connected to a beamformer with M beam ports, multiple simultaneous beams will be produced. Beamformers are typically used in RF transmitting and receiving systems. Beamforming can also be used to control a single beam out of an array and change its radiation maximum by changing the relative amplitude and phases of the excitations.

Beamformers are employed between the antenna arrays and the receiver, in a receiving mode, to effectively focus the radiation beam of the receiving system to a certain direction (the target). On the other hand, in the transmitting mode, radar systems for example, the beamformers are connected between the RF signal
source and the antenna array system to shape the antenna beam towards a certain target or direction.

In general, beamformers are either networks or quasioptical lenses. Networks or lenses can be called beamforming networks (BFN). Power dividers, the Butler matrix, the Blass matrix, and the Nolen matrix are an examples of BFN networks.While, the Rotman lens, the Bootlace lens, and the Dome lens are an examples of BFN lenses [12]. In a lens BFN, the beamwidths and crossover levels are dependent on frequency, while beam angles are fixed. This is because the lenses are true-time delay devices. Hence, they produce the same beam angles independent of frequency. In a network BFN, changing the frequency will change the beamwidths and beam angles, while beam crossover levels are independent of frequency.

In this section, we are going to describe in details the theory behind these different types of BFN. For the network BFN, the Butle matrix is the most popular one, while for lenses, the Rotman lenses had many practical applications.

### 2.2.1 Power Divider BFN

The simplest BFN uses power dividers to split the transmitted power between N input elements of antenna array. A constant phase shifter is employed in each division to achieve the progressive phase shift. Power dividers and directional couplers are passive microwave circuits used for splitting or combining power. Dividers and couplers are used in feed networks for antenna arrays, balanced
mixers, power transmitters and test instruments.

Figure 2.11 shows the working concept of the combiners/splitters, where $0<\alpha<$ 1. A coupler may be a three or four port component. T-junction and other power dividers are three-port networks, while directional couplers and hybrids are four-port networks.

Equal power division (3-dB type) and unequal power division ratios are also possible with power dividers. Directional couplers are used to get arbitrary power division, while hybrids $\left\{90^{\circ}\right.$ hybrid (Quadrature) or $180^{\circ}$ hybrid (magic-T) $\}$ usually have equal power division [2].

(a) Configuration A

(b) Configuration B

Figure 2.11: Power splitting/combining in dividers/splitters.

Before going into the details of the power divider beamformers, we are going to describe the functionality of the basic elements of the power dividers.

### 2.2.1.1 T-junction Power Divider

The simplest three-port power divider is the T-junction which can be used as a divider or combiner. The microstrip T-junction design and its transmission line model are shown in Figure 2.12. This type of divider is considered lossless, but it cannot be matched simultaneously at all ports. The T-junction can be modeled by a transmission line model as shown in Figure 2.12(b). By assuming a lossless
junction, we must have the condition in equation (2.35) to match the input line with the two output lines [2].

$$
\begin{equation*}
\frac{1}{Z_{1}}+\frac{1}{Z_{2}}=\frac{1}{Z_{o}} \tag{2.35}
\end{equation*}
$$

where $Z_{o}$ is the characteristic impedance of the input line, and $Z_{1}, Z_{2}$ are the characteristic impedances of the output ports. So, we can choose $Z_{1}$ and $Z_{2}$ to provide ratios of power division. For a $3-\mathrm{dB}$ (equal division) power divider, if the input line characteristic impedance $Z_{o}$ is $50 \Omega$, a $100 \Omega$ output line will be chosen.


Figure 2.12: T-junction power divider.

If we need all ports to be matched, lossy components such as lumped resistors are used. In such case, the output ports are not isolated anymore. This divider is called the resistive divider which uses lumped resistors. Equal and unequal splitting are possible with resistive dividers. Equal-split three-port resistive power divider is shown in Figure 2.13. All ports have the same characteristic impedance $Z_{o}$, accordingly all ports are matched together and matched with the load lines.


Figure 2.13: An equal-split three-port resistive power divider.

The S-parameters of the input-output ports, $S_{21}, S_{31}$ and $S_{23}$ are equal 0.5 and hence the network is reciprocal and the scattering matrix is symmetric, and can be written as

$$
[s]=\frac{1}{2}\left[\begin{array}{lll}
0 & 1 & 1  \tag{2.36}\\
1 & 0 & 1 \\
1 & 1 & 0
\end{array}\right]
$$

Low isolation between the output ports, and the resistive losses are the major two disadvantages of the resistive power divider. As a result, the Wilkinson [13] power divider is considered to overcome these two problems.

### 2.2.1.2 Wilkinson Power Divider

The Wilkinson power divider (WPD) is generally an N-way hybrid splitter with arbitrary power division. Since the isolation between the output ports in a T-
junction and the resistive divider is still not achieved, the Wilkinson power divider has the property that the reflected power is dissipated, hence good isolation between output ports is achieved. In the ideal case, the scattering matrix of a Wilkinson divider given by [14],

$$
[s]=\frac{-j}{\sqrt{2}}\left[\begin{array}{ccc}
0 & 1 & 1  \tag{2.37}\\
1 & 0 & 0 \\
1 & 0 & 0
\end{array}\right]
$$

A two-way microstrip Wilkinson power divider is shown in Figure 2.14. In this design, the input at port (1) is evenly divided in amplitude and phase at output ports (2) and (3). A high isolation between output ports can obtained by using $\lambda / 4$ impedance transformers having a charcterstics impedance of $\sqrt{2} Z_{o}$ and a lumped isolation resistor of $2 Z_{o}$ with all three ports matched. The equivelent transmission line circuit is shown in Figure 2.14(b).

(a) Microstrip equal-split WPD.

(b) Transmission line circuit.

Figure 2.14: The Wilkinson power divider.

### 2.2.1.3 Switched-Line Phase Shifters

A simple phase shifter can be implemented by switching between a two different transmission line lengths. This type of phase shifter called switched-line phase shifter. Figure 2.15 shows the fundamental unit (1 bit) of the switched-line phase shifter. It has two arms, a reference arm and a delay one. Switched-line phase shifter has the advantages of wideband, low loss, simple structure, and high performance in phase accuracy and isolation.


Figure 2.15: Switched-line phase shifter.

The switched-line phase shifter os dependent on the lengths of microstrip line used.
In N-bit phase shifter, the incoming input signal is routed/switched through one of N-way alternate paths to the output, so as to introduce specific phase shifts with minimum loss [15].

The switching elements in the switched-line phase shifter can be relays (or mechanical switch), Field Effect Transistors (FET), PIN diodes, or microelectromechanical switches (MEMS) [16]. Depending on the frequency band of interest, the switching technology can be chosen. The PIN diodes can be used up to 18 GHz
and it is preferred compared to FET technology but it is difficult for integration and fabrication.

### 2.2.1.4 The $90^{\circ}$ Hyprid Coupler

The conventional $90^{\circ}$ hyprid coupler is essentially a four-port device comprising four arms. Each of its arms has a length of one quarter-wavelength at the operating desired design frequency [17]. Schematic diagrams are shown in Figure 2.16 for two configurations of the hybrid coupler. The effect of the two configurations is the same, but Figure 2.16(b) is more suitable since it has two continuous $Z_{o} \Omega$ tracks joined by two parallel arms of impedances $Z_{o} / \sqrt{2}$.


Figure 2.16: $90^{\circ}$ Hybrid Coupler

If the signal is fed at port (1) (in this case, port (4) is loaded with $Z_{o}$ ), the output ports (2) and (3) will be have two equal output signals, but with a $90^{\circ}$ difference in phase. The same process will happen if the feed was from port (3) \{ and port (1) is loaded by $\left.Z_{o}\right\}$. No power is coupled to port (4) (the isolated port). Thus, the $[\mathrm{S}]$ matrix will have the following form [2]

$$
[s]=\frac{-1}{\sqrt{2}}\left[\begin{array}{cccc}
0 & j & 1 & 0  \tag{2.38}\\
j & 0 & 0 & 1 \\
1 & 0 & 0 & j \\
0 & 1 & j & 0
\end{array}\right]
$$

### 2.2.2 Power Dividers BFN examples

The design of a beamforming network using power dividers, hybrids, and directional couplers were done in [18-21]. A simple beamformer comprising a simple antenna array connected to a quadrature coupler is shown in Figure 2.17. As mentioned in section 2.2.1.4, the quadrature coupler in a receiver system will combine the signals separated by $90^{\circ}$ in one output and cancel it in the other output. If the wavefront is arriving form the left, it will arrive at the left antenna prior to the right one. Hence, the signal will route to the left arm of the coupler. On the other hand, a reversed situation will happen when the wavefront will arrive from the right.


Figure 2.17: Simple beamformer using quadrature coupler.

In [19], a Wilkinson-type and coupled-line power dividers were used to feed a planar antenna array system. These networks allow parallel or series feed. The outputs of the feed networks were all in-phase with non-uniform power distribution. This will control the sidelobe suppression level. In order to equalize the phase shift at the output ports, a wilkinson-type in-phase power divider is presented in 2.18. In Figure 2.18(a), a parallel feed network is shown, in which signal power is divided at each level of the pyramid structure of the network at every port, while in Figure 2.18(b), a series feed network is shown, in which the signal power is divided only at the left hand side ports of the individual dividers.


Figure 2.18: Wilkinson-type in-phase power divider.

Another work that used the hybrid power dividers as a feed network was [18]. In this work, a design of two different feed networks for phased array applications were presented. The directional couplers were applied in a series feed network while the Wilkinson dividers were applied in a parallel feed.

A novel beamforming network using a seven-way power divider/combiner was used in [20]. New two configurations of a seven power divider/combiner were presented as the key of the proposed feed networks. The schematic and electrical configuration of the first divider is shown in Figure 2.19.


Figure 2.19: Seven-way divider/combiner.

In this design, half of the input power must be delivered to the center output, while the remaining power is divided equally among the six radial ports. The second configuration of the divider depends on a two-way Wilkinson power divider as shown in Figure 2.20. The first design has the advantages of physical simplicity, circular symmetry, and low loss, while the second design has high isolation (Wilkinson) and easier construction.


Figure 2.20: Electrical configuration of the second seven-way divider/combiner.

A new way of controlling the beam shape by altering the number of array elements was presented in [21]. As shown in Figure 2.21(a), a modified Wilkinson power
divider was used to construct the reconfigurable antenna array in Figure 2.21(b). S1 and S2 are PIN (Intrinsic PN) diode RF switches that are used to alter between 4 -elements and 8-elements antenna array structure. For an 8 -element, the radiation pattern has a concave patten, while for the 4-element antenna mode, a convex pattern will be generated.


Figure 2.21: The structure of the corporate fed reconfigurable antenna array.

### 2.2.3 Network BFN

### 2.2.3.1 Maxon-Blass matrix

The Maxon-Blass matrix uses a set of array element transmission lines which intersect a set of beam ports lines, with a directional coupler at each intersection [22]. It is particularly useful when a small number of $M$ narrow beams is required from a ralatively large number of array ports $N$. The line lenghts between the couplers in the series feeds to the array ports must achieve spatial orthogonality of the beams at the design frequency. Out of frequency range, the beam directions will change. A schematic of a Blass matrix BFN for six beams with eight antenna elements is shown in Figure 2.22 [17].


Figure 2.22: Schematic of a Blass matrix BFN for 6 beams with eight antenna ports.

Along the radial directions, the transmission line section have equal length, while along the circumferential directions, the line sections have different lengths. This difference in length will generate a constant progressive phase at each array port, generating a scanned beam. If the Blass matrix is used with TEM transmission lines (ex. coaxial cables), the beam location will not change with frequency and the Blass matrix will be a true time-delay beamformer in this case. While, for non-TEM transmission lines (ex. waveguide), the beam location will change with frequency. Also, amplitude tapering can be achieved by suitably selecting coupling factors of the directional couplers [23].

### 2.2.3.2 Butler matrix

The Butler matrix is a typical example of an analog beamformer. It consist of a network of couplers, fixed phase shifter (added line length), and crossovers with N input ports, connected to the antenna elements, and an equal number of beam outputs. A schematic design for a four-port Butler matrix is shown in Figure 2.23. Because of the fact that the Butler matrix is the microwave realization of the fast Fourier transform (FFT), it has the minimum number of couplers. Since the Butler matrix has crossovers, it uses a multi-layer structure. Modern Butler matrices can be implemented on printed circuit boards. Some limitations of the Butler matrix are:

1. Narrow band.
2. Very complicated design for a large number of beam ports [17].
3. The sidelobes are realtively high (No amplitude tapering).
4. There is a loss of the order $3-5 \mathrm{~dB}$.
5. Designed for $2^{n}$ array elements.


Figure 2.23: Schematic for four-port Butler matrix.

### 2.2.3.3 Nolen Matrix

A generalization of Blass and Butler matrices yields a Nolen matrix [24]. It consists mainly of hybrid couplers and phase shifters as shown in Figure 2.24.


Figure 2.24: Schematic for Nolen matrix BFN.

In Nolen matrix, the number of beam ports can differ from the number of antenna elements as in Blass matrix. Nolen matrix is an implementation of the general discrete Fourier transform (DFT) algorithm, which can be applied to any number of elements. Therefore, it can be reduced to simpler forms, as the FFT algorithm and its application of the Butler matrix [25]. Due to the difficulties of the Nolen BFN and its network adjustments, it is seldom used [12].

### 2.2.4 Lens BFN

### 2.2.4.1 Rotman Lens

Figure 2.25 shows the schematic of a two-dimensional Rotman lens. The original lens uses parallel plate waveguide for the feed portion (beam ports), and coaxial cables for the transmission lines connecting the element ports to the radiating
array elements. The beam ports are situated along a beam port surface and the array ports are located on an array port surface. The two surfaces are circular arcs. The beam port surfaces usually have a large curvature than the array port surface [12].


Figure 2.25: Rotman lens beamformer.

The Rotman lens are, in principle, wideband systems since their design is based upon geometrical optics and corresponds to a time-delay beamformer. Assuming the transmit mode operation of the lens, the beam ports are considered radiators and the array ports as receiving elements that are connected to the array elements though transmission lines. The lengths of these transmission lines are equal. Because of this, and to keep the antenna array on a line, some of the lines are more squeezed than others.

To explain the principle of operation of the lens, assume the lens is working in
the transmit mode. If one of the beam ports (radiator) is exited, the signal will arrive at each receiving element with a phase difference proportional to the patch length between the radiator and the receiving element [23]. Now, if the array port surface is designed such that the path length varies linearly with the locations of the receiving elements on the array port surface, then the array elements will have a linear phase distribution resulting in a scanned beam. Thus each beam port has a beam with a unique scan angle. Unfortunately, it is impossible theoretically to obtain a linear phase for all beams. Also, the amplitude asymmetry for the beams raises the sidelobe levels [12]. Another disadvantage is the relatively low number of achievable beams and difficulty of achieving low sidelobes and low losses [26].

## CHAPTER 3

## LITERATURE REVIEW AND

## RESEARCH METHODOLOGY

### 3.1 Literature Review

In this section, we will go over the related work of standalone feed networks and their performance as they appeared in the literature. Many types of feed networks such as fixed beam, multi-beam (most of them done by Butler matrix feed network) and switchable feed networks were proposed. The main goal of the research in this area is to improve the resolution of the scanning beam as well as cover a wide frequency range. Most of the designs covered narrow-band frequency range and were under 3 GHz . Thus, there is a need to widen the frequency ranges as well as make the beam scanning process programmable for better flexibility.

As discussed in chapter 2, the feed network or beamformer can be done with networks such as power dividers/combiners and Butler matrix [27-31], or lenses
such as the Rotman lens [32-35]. In this literature review, we are going to focus on the most two popular BFNs which are the Butler matrix and the Rotman lens. In [27], a multi-beam matrix network created by four $90^{\circ}$ hybrid couplers which realizes the required excitation for four beams spaced by $90^{\circ}$ in the azimuth plane for antenna arrays is presented. The concept of the matrix developed for this application is much simpler than conventional methods and uses only four directional couplers feeding the four antenna elements, without additional fixed phase shifters and without line crossings as known from the Butler Matrix. The matrix covers the band from 2.4 to $3.4 G H z$ with isolation better than $25 d B$ and the reflection coefficient better than $-15 d B$. For a four-square array of monopoles, the desired four beams are at $\pm 45^{\circ}$ and $\pm 135^{\circ}$ in the azimuth plane and the $3 d B$ beam widths were about $80^{\circ}$. The cross-over levels of neighboring beams are about $3 d B$ below the main beam peak and deep nulls appear under $\pm 90^{\circ}$ form the direction of the main beam.

The design of a 2.5 GHz monolithic $4 \times 4$ Butler matrix was introduced in [28]. This was the first complementary metal oxide semiconductor (CMOS) Butler matrix MMIC. Unlike the conventional Butler matrix, the $3 d B$ quadrature coupler is replaced by a CMOS coupler that is called phased compensated transformer. The CMOS quadrature coupler is realized with the bifilar broadside-coupled transformer. Comparing this CMOS quadrature coupler (insertion loss is $4.21 d B$ at $2.5 G H z$ ) with and ideal $3 d B$ quadrature coupler, the additional $1.2 d B$ loss is caused by the parasitic resistance of metal lines and the substrate. The isola-
tion and return loss of the coupler are better than $20 d B$. The transformer-based quadrature coupler is terminated at port 2 and port 3 by purely reactive (lossless) loads to build the reflection-type phase shifter. The multilayer crossover achieves isolation better than $50 d B$. The area of the designed CMOS Butler matrix is $1.36 \times 1.47 \mathrm{~mm}^{2}$ and was fabricated using $0.18 \mu \mathrm{~m}$ CMOS process. Beam directions at $-45^{\circ},-15^{\circ}, 15^{\circ}$, and $45^{\circ}$ are generated when connecting the matrix to a $1 \times 4$ linear antenna array. The measured amplitude imbalanced is less than $1.5 d B$ and the phase imbalance is less than $4^{\circ}$ from 2.4 to 2.6 GHz .

A feed network for a $2 \times 2$ antenna array to construct a sectoral conical beam was presented in [29]. The feed network was constructed using four $90^{\circ}$ hybrids, one crossover, and four $90^{\circ}$ delay lines which are connected to the one coupled port of one of the $90^{\circ}$ hybrids. Depending on the input port used, the radiation patterns are created at $45^{\circ}, 135^{\circ}, 225^{\circ}$, and $315^{\circ}$ azimuth angles. This design can be used to communicate with satellites in geostationary orbits for Satellite Digital Multimedia Broadcasting (S-DMB). The design was fabricated on a Microstrip substrate with dielectric constant of 6.5 and thickness of 0.635 mm . The design operated at 2.6 GHz and the distance between the antenna elements was 60 mm along the x and y directions.

In [36], a single-feed switchable feed network that combines two ports of a microstrip antenna with a quarter-wavelength feed lines was presented. This network assumes that the operating frequency ratio to be less than $1.4: 1$ for the two microstrips patch antennas. The network consists basically of two quarter-wavelength
branch lines with different characteristic impedance ( $l_{1}$ and $l_{2}$ ) and two microstrip patch antennas. Since the resonance frequency of the two antennas are very close $\left(\frac{f_{1}}{f_{2}} \leq 1.4\right)$, then the two branch lines are almost equal in length. Thus if it is applied $f=f_{1}$ to the input port, one patch would be at resonance and the other one would be at off-resonant, and vice versa. So, by applying $f_{1}$ or $f_{2}$, this network will act as a switch. Such that the feed network can be applied to a radiation pattern or polarization reconfigurable antenna system where diversity is needed. The overall dimension of the network (including the two patch antennas) was $200 \mathrm{~mm} \times 100 \mathrm{~mm}$ that was designed on a Teflon substrate $\left(\varepsilon_{r}=3.48, t=1.5 \mathrm{~mm}\right)$ and fed by a $50 \Omega$ coaxial connector. This network is working at two resonant frequencies, $1.94 G H z$ and $2.13 G H z$.

Enhanced switching/steering Butler matrix combining two techniques, tunable phase shifters and conventional N-way Butler matrix was proposed in [30]. Initially the radiation beam is switched to a certain direction through the conventional Butler matrix (one direction out of the 8 directions), and then slightly adjusted by the tunable phase shifters. So, the phase shifters are responsible only for steering the beam in the range between two adjacent beams. This approach improves the beam resolution. Also, it achieves wideband performance and ultra-compact circuit size compared to the traditional Butler matrix. The design was created using a stripline configuration $\left(\varepsilon_{r}=3.38, \tan \delta=0.0025\right)$ on a four-layer board. Because of the narrowband nature of the design and of using the length difference to generate the phase shift, the Shiffman phase shifter was used. The tunable
phase shifter is integrated based on a stripline asymmetric reflection-type phase shifter. The measured return loss was better than $10 d B$ over the range of 1.6 to $2.8 G H z$. The maximum tunable phase shift was greater than $120^{\circ}$, and the average insertion loss was $2 d B$ to $3 d B$ with a loss variation of $\pm 1 d B$. The overall circuit size was $175 \times 135 \mathrm{~mm}^{2}$. A full scanning range of $108^{\circ}$ with beam resolution better than $2^{\circ}$ was achieved.

Butler-matrix based and lens-based beamformers were introduced in [32] to develop steerable antennas suitable for a use in vehicle-to-vehicle and vehicle-toroadside communications systems. A $4 \times 4$ Butler matrix beamformer was designed at a center frequency of 3.15 GHz . The Butler matrix occupied a size of $11.6 \times 9.1 \mathrm{~cm}^{2}$. For the Rotman lens beamformer, it was designed an $8 \times 8$ feed network for the 6.3 GHz band. The lens achieved a scan angle of $\pm 50^{\circ}$. In this design, instead of using the dummy ports as RF absorbers, it was used sidewalls instead. The $8 \times 8$ Rotman lens BFN occupied a size of $35.91 \times 25.80 \mathrm{~cm}^{2}$.

A Rotman lens was used to construct a beam switching antenna to provide scanning beams in [33]. The lens was designed for 2.4 GHz band and is applicable to MIMO technology in that band. In this work, it was showed that the Rotman lens, compared to the Butler matrix switching mode, has a larger fractional bandwidth and can serve more than one transceiver. The substrate used was a 1.6 mm thick RF4 board and the size was $193.2 \times 222.8 \mathrm{~mm}^{2}$. When the lens was connected to a patch antenna array, it generated 4 -beams pointing toward $-28,-12,5$, and $22^{\circ}$. Most of the previous works either passive feed networks, or they used a pack-
aged active tunable phase shifters and amplifiers. The passive networks are of huge size and can't be integrated, especially those working in low frequency ( $<6$ $\mathrm{GHz})$. There are many works that integrated active tunable phase shifters and amplifiers in a small packages with CMOS technology and used microelectromechanical (MEMS) technology. Most of these works were for high frequency (> 6 GHz ) [37-41]. However, if the active tunable phase shifters were used in low frequency such as 2.4 GHz , it was designed for a specific frequency not a range of frequencies [42].

As noticed in the literature review, network BFNs have an easy structure for small number of beams. But for a large number of beams, the design will be very complicated, especially for crossovers and directional couplers that needs multilayer structures. Also, most of the network-based BFNs are applicable only for narrow band applications such as the Butler matrix. The network BFNs can only provide a certain number of beams that are fixed and cannot be changed. So, it is difficult to reprogram. The side-lobes obtained when using network BFN were relatively high because it does not have an amplitude tapering functionality.

The lenses provide a wideband frequency coverage, but with large dimensions. They have an isolation between ports that is considered to be good for many applications. Also, it is theoretically difficult to achieve linear progressive phase with lenses due to the complicated curvature structure.

To come up with a wideband feed network that is, digitally programmable, in phase and amplitude, with high resolution in both, and compact size is a relatively
challenging goal. In this work, we propose a digitally controlled wideband RF feed network that covers the frequency band from $2.5-6 \mathrm{GHz}$. The features of the proposed feed network compared to other designs that appeared in literature are presented in Table 3.1.

Table 3.1: Comparison of proposed RF feed network.

|  | [27] | [28] | [29] | [30] | [32] | [33] | Proposed |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency | 2.4-3.4 | 2.4-2.6 | @2.6 | 1.6-2.8 | 2.5-3.5 | @2.4 | 2.5-6 |
| Range | GHz | GHz | GHz | GHz | GHz | GHz | GHz |
| Amp. Resolution | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | 0.5 dB |
| Phase Resolution | $90^{\circ}$ | $30^{\circ}$ | $90^{\circ}$ | $\ldots$ | $\ldots$ | $17^{\circ}$ | $5.625^{\circ}$ |
| Beam Resolution | $\begin{aligned} & \pm 45, \\ & \pm 135 \end{aligned}$ | $\begin{gathered} -45,-15 \\ 15,45^{\circ} \end{gathered}$ | $\begin{gathered} 45,135 \\ 225,315^{\circ} \end{gathered}$ | $2^{\circ}$ | $\ldots$ | $\begin{gathered} -28,-12 \\ 5,22^{\circ} \end{gathered}$ | $1.8^{\circ}$ |
| Programmable? | No | No | No | Yes (Phase) | No | No | Yes (Amp, Phase) |
| Main component | Butler matrix | Butler matrix (CMOS MMIC) | Buterl matrix | Butler matrix $+$ <br> Tunable phase shifters | Butler matrix | Rotman lens | Tunable <br> phase <br> shifters, amplifiers |
| Size | $\ldots$ | $\begin{gathered} 1.36 \times \\ 1.47 \\ m m^{2} \end{gathered}$ | $\ldots$ | $\begin{gathered} 175 \times 135 \\ m^{2} \end{gathered}$ | $\begin{gathered} 116 \times 91 \\ {m m^{2}}^{2} \end{gathered}$ | $\begin{gathered} 193 \times 223 \\ {m m^{2}}^{2} \end{gathered}$ | $\begin{gathered} 111 \times 63 \\ \mathrm{~mm}^{2} \end{gathered}$ |
| $\begin{gathered} \text { No. of } \\ \text { input ports } \end{gathered}$ | 4 | 4 | 2 | 8 | 4 | 4 | 2 |

### 3.2 Research Methodology

As a part of a big target project, this work covers one stage of a complete system as shown in Figure 3.1. Other stages were done by our group within the Antennas and Microwave Structure Design Laboratory (AMSDL) at the Electrical Engineering Department at KFUPM. This system will be used for unmanned surveillance purposes, such as Unmanned Aeriel Vehicles (UAV). However, our target in this work is to design a generic and standalone feed network that is able to feed an antenna array system, or any system such as a stage of amplifiers, MIMO system, and etc. In this work, the combiner/splitter and the feed network were designed, fabricated and characterized. Since we have a 12 antenna array elements in the complete system, we need a 12-port feed network.

The different project phases and the interaction between them are shown in Figure 3.2. The first step was to collect the information about the components required, part numbers from manufacturers, their functions, dimensions and footprints. Most of the RF components like RF switches, RF phase shifters, and RF amplifiers are form Hittite Microwave Corporation. Hittite also provides the Sparameters files for each component. These files are required in the simulation phase to test the model behavior. Microwave Office from Advancing the Wireless Revolution Company (AWR MWO) is used in this work for modeling and simulation. MWO RF/microwave design software is a very popular microwave design platform [43].

Using the footprints and dimensions form the components' datasheets, the fab-


Figure 3.1: Block diagram of the interaction between the various phases of the project. Shaded blocks are the contributions of this work.
ricated model of the design was done in parallel with the simulation model. Altium designer [44] was used for generating the PCB and Gerber files required for the manufacturing process. The first board was a two-path design of the programmable feed network and was given the label version V1. After the layout and fabrication phase for V1, the RF traces were imported to MWO from Altium to generate accurate simulation results and take the RF line effects into account. When the fabricated board worked, we proceeded to generate a simulation version with 4 paths and gave it the label V2. Matlab software was used to compare the simulated and measured results. the simulation model for the 4 -path board was modeled in MWO. Only the 2-path board design due to the manufacturing times
and cost was fabricated.


Figure 3.2: Block diagram of the interaction between the various phases of the project.

## CHAPTER 4

## PROGRAMMABLE FEED

## NETWORK ARCHITECTURE

## AND DESIGN

In this chapter, we will present the design and architecture of the proposed programmable wideband RF feed network and describe in detail the components used and their respective features. Then, we will go over the circuit and board designs adopted. Finally, we are going to discuss the microcontroller portion and programming.

### 4.1 Design Architecture

The design architecture of the proposed two-path feed network is shown in Figure 4.1 and is composed of four main stages, RF switching, phase shifting, am-
plification, and the digital control stage. Since, we have two phase shifters that cover the whole range from 2.5 to 6 GHz , we used a switching stage. The first phase shifter (HMC647), covers the range from 2.5 to 3 GHz and the second phase shifter (HMC649), covers the range from 3 to 6 GHz . The phase shifters are GaAs (Gallium Arsenide) MMIC 6-bit digital phase shifters that provide a 360 degrees of phase coverage with phase resolution of $5.625^{\circ}$. A broadband GaAs MMIC Single-Pole Double-Through (SPDT) non-reflective switch is used for the switching phase. The switch covers the range from DC-6 GHz and offers high isolation $(42 \mathrm{~dB}$ at 6 GHz$)$ between the two inputs and low insertion loss $(1.6 \mathrm{~dB}$ at 6 $\mathrm{GHz})$. The design architecture has two switches per path to switch to the right phase shifter and combine the signal again to the final stage of amplification. For amplitude control, a GaAs MMIC 6-bit variable gain amplifier is used (HMC625). The amplifier covers the range from DC to 6 GHz and can be programmed to provide anywhere from -13.5 dB to 18 dB gain, in 0.5 dB amplitude steps. The amplifier does not have a smooth gain versus frequency, but it has a maximum gain of 18 dB that decreases to about 5 dB at 6 GHz .


Figure 4.1: Proposed architecture of the wideband programmable Feed network.

### 4.2 Components' Specifications

The main components used to build the programmable RF feed network are:

RF Switches: We have two RF switches per path (one for each frequency range).
The RF switches are digitally controlled with two digital bits. These switches cover the range from DC-6 GHz with low insertion loss of almost 1.6 dB and offer high isolation over the given range. The truth table of the RF switch is shown in Table 4.1.

Table 4.1: Truth table for switch HMC336

| Control Input |  | Signal Path State |
| :---: | :---: | :---: |
| A | B | RFCOM to: |
| Low | High | RF1 |
| High | Low | RF2 |

Phase Shifters: The phase shifters are digitally controlled by digital control unit according to Table 4.2. The phase shifter is digitally controlled with 6 -bits. Two phase shifters for each path are used, one covers from 2.5-3.1 GHz (HMC647), and the other one covers form 3 to 6 GHz (HMC649). The two phase shifters are identical in packages, footprints, size and the function. Each one has different insertion loss. The truth table for the two phase shifters is shown in Table 4.2. This table shows only the major states. Any combinations of the above states will provide a phase shift approximately equal to the sum of the bits selected. For example, if Bit1 and Bit2 are equal to 1 , the total phase shift is equal to $16.875(5.625+11.25)$. The phase shift start at 0 phase shift with step of $5.625^{\circ}$ and cover the range from 0 to $360^{\circ}$.

Table 4.2: Truth table for phase shifters HMC647 and HMC649.

| Control Voltage Input |  |  |  |  | Phase Shift (Deg.) |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Bit1 | Bit2 | Bit3 | Bit4 | Bit5 |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 | Ref. |
| 1 | 0 | 0 | 0 | 0 | 0 | 5.625 |
| 0 | 1 | 0 | 0 | 0 | 0 | 11.25 |
| 0 | 0 | 1 | 0 | 0 | 0 | 22.5 |
| 0 | 0 | 0 | 1 | 0 | 0 | 45.0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 90.0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 180.0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 354.375 |

Variable Gain Amplifiers: At the final stage, a 6-bit digitally controlled amplifier is used for each path. The amplifier cover the range from DC-6 GHz. It has a gain that ranges from -13.5 to +18 dB with a step of 0.5 dB . The 6 -bit control truth table is shown in Table 4.3. The maximum gain $(+18$ $d B)$ is achieved when all bits are logic high and the minimum gain (-13.5 $\mathrm{dB})$ when all the bits are in logic low. Table 4.3 shows only the major states. Since the amplifier gain changes with frequency, the 0 dB is the maximum relative gain. This means that the maximum gain of the amplifier at any frequency ( DC to 6 GHz ) will considered as the 0 dB relative gain. Any
combinations of these states will provide a reduction in gain approximately equal to the sum of the bits selected relative to the maximum gain of 18 dB . To get attenuation of $1.5 \mathrm{~dB}(18-1.5=16.5 \mathrm{~dB})$, the $D_{0}$ and $D_{1}$ will be logic low. This variable gain amplifier is working on the direct parallel mode, where the attenuation state is selected using the control voltage inputs directly.

Table 4.3: Truth table for amplifier HMC625.

| Control Voltage Input |  |  |  |  | Relative Gain |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| D 5 | D 4 | D 3 | D 2 | D 1 |  |  |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 dB |
| 1 | 1 | 1 | 1 | 1 | 0 | -0.5 dB |
| 1 | 1 | 1 | 1 | 0 | 1 | -1 dB |
| 1 | 1 | 1 | 0 | 1 | 1 | -2 dB |
| 1 | 1 | 0 | 1 | 1 | 1 | -4 dB |
| 1 | 0 | 1 | 1 | 1 | 1 | -8 dB |
| 0 | 1 | 1 | 1 | 1 | 1 | -16 dB |
| 0 | 0 | 0 | 0 | 0 | 0 | -31.5 dB |

Microcontroller Board: The control unit for all these components is programmed on the Microcontroller Board (Dragon 12) chip which is called MC9S12DG256. MC9S12DG256 is a HCS12 family which was introduced by Motorola in 2002. In 2004, the semiconductor division of Motorola be-
come a separate and independent entity called Freescale Semiconductor [45].
The MC9S12DG256 consists of the following parts:

- 256 K bytes of flash EEPROM.
- 12 K bytes of RAM.
- 4 K bytes of EEPROM.
- Two 8-channel, 10-bit analog-to-digital (A/D) converter.
- Two asynchronous Serial Communication Interface (SCI).
- Three Serial Peripheral Interfaces (SPI).
- 8-channel timer module.
- 8-channel Pulse-Width Modulator (PWM).
- 29 discrete digital I/O channels.

In section 4.5, the microcontroller unit and the control program will be discussed in details.

### 4.3 Schematic Design

Figure 4.2 shows the complete schematic of the proposed network only for one path. After finishing the PCB design for this one path, we repeated it again and made the design fit within the smallest area possible. The schematic shows every component and all the details of the design. In the schematic one can assign the footprint to each component after creating its schematic. The footprints and the
schematics for all components are available in the datasheets. All the component footprints were custom layed out in the PCB design tool to make sure that the manufacturer recommendations were followed.


Figure 4.2: The complete schematic diagram of one path of the programmable RF feed network.

### 4.4 PCB Board Design

Using the software Altium designer, the PCB board was created. The PCB was designed for a 2-path network. As mentioned in section 4.3, we designed one path and then repeated it two times. Because there are two branches for each signal (two phase shifters per path), one should ensure that the two branches are identical (same length and same number of bends). Also there should be no lines under the RF ICs to avoid any distortion or coupling problems. The power lines are made wider than the digital control lines. The board dimensions were about $111 \times 63 \mathrm{~mm}^{2}$, and the substrate used was FR-4 with 0.8 mm thickness. Figure 4.3 shows the designed PCB board for the proposed network. Input1 and Output1 indicated on Figure 4.3 are path 1 RF input and output, respectively, and the same is considered for path 2.


Figure 4.3: The PCB board for 2-port model network.

To control the whole board, dip switches were used to connect the logic control to the different components on the board and check that everything is working properly before using the microcontroller. Each phase shifter has its own dip switch, and one of them shares it with the RF switches (one is 6-bits and the other is 8-bits). Each amplifier has its own switch and shares it with the output RF switch (8-bit dip-switch). The total number of dip switches used on the prototype board was 6. Dip switches numbering is shown in Figure 4.4.


Figure 4.4: The numbering of the dip switches on the board.

Table 4.4 shows the signal connections of dip switch 1 ( and $1^{\prime}$ ) shown in Figure 4.4.
This dip switch controls the first RF switch and the upper phase shifter (2.5-3 GHz ). The amplifier and the second RF switch were controlled by dip switch 2 (and $2^{\prime}$ ). The signal connections of dip switch 2 (and $2^{\prime}$ ) are shown in Table 4.5. The last switch, dip switch 3 only controls the lower phase shifter and it has only 6 positions. The signal connections of its positions are shown in Table 4.6. The control bits are not in order because of the routing constraints.

Table 4.4: Dip switch 1 (and dip switch $1^{\prime}$ ) control the phase of HMC647 (2.5 to 3.1 GHz ) and the first switch HMC336.

| Pin No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 4 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Control | CTLB | CTLA | Bit1 | Bit2 | Bit3 | Bit4 | Bit5 | Bit6 |  |

Table 4.5: Dip Switch 2 (and Dip Switch 2'): The gain of HMC625 (DC to GHz).

| Pin No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | $\Delta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Control | Do | D1 | D2 | D3 | D4 | D5 | CTLB | CTLA |  |

Table 4.6: Dip switch 3 (and dip switch $3^{\prime}$ ) control the phase of HMC649 (3 to 6 GHz ) and the second switch HMC336.

| Pin No. | 1 | 2 | 3 | 4 | 5 | 6 | $\leq 5$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Control | Bit1 | Bit2 | Bit3 | Bit6 | Bit5 | Bit4 |  |

### 4.5 Microcontroller and the Control Program

As mentioned in section 4.2, the MC9S12DG256 board will be used to test the code for the control program. This microcontroller unit can operate with speed up to 25 MHz . Figure 4.5 shown the block diagram of a typical HC 12 microcontroller.

Because of the disadvantages of the assembly language in hardware programming like importability (changing the device means changing the whole program), and longer time to write compared to high-level languages, we will use the most popular high-level language, C [46].


Figure 4.5: The block diagram of a typical HC 12 microcontroller.

Also, there are many assembly language routines that access all of the important I/O functions of the Freescale MC9S12DG256 microcontroller unit. These built-in routines are included in the file main.asm that is a part of the control program. All of these routines can simply be called by a simple C function. The Dragon-12 microcontroller board is shown in Figure 4.6.

The Freescale MC9S12DG256 microcontroller is located under the white bread board and is surrounded by four convenient female headers that bring out all of the I/O ports. These header pins will be used to get out the control bits to the proposed network. As shown in Figure 4.6, the Dragon12-plus board contains:

- Four-digit 7 -segment display.
- Four pushbutton switches.
- 8-position DIP switch.
- Eight LEDs.
- Potentiometer (0-5 V analog).
- Liquid Crystal Display (LCD).
- $4 \times 4$ keypad.


Figure 4.6: Drgon-12 Board that carry the Microcontroller Unit.

The board is connected to the PC via a serial cable to get programmed. The first stage of the design is to design the program and prompt the user to input the data manually. A sample program for a linear phased arry is developed. The data that will be entered are:

- The Frequency range.
- Number of antenna elements (M).
- The space between elements (d) as a function of wavelength $(\lambda)$.
- Choose gain or attenuation and enter the magnitude of the amplitude.
- Entering the angle theta $(\theta)$ for beam steering and phase generation.

After entering the data, the program will calculate the progressive phase ( $\beta$ ) using the following relation for a linear array,

$$
\begin{equation*}
\beta=-\frac{2 \pi}{\lambda} \cdot d \cdot \cos \theta \tag{4.1}
\end{equation*}
$$

The program will calculate the index that generate the amplitude and phase according to Table 4.3 and Table 4.2. For example, if the progressive phase $\beta$ is $45^{\circ}$, the index should be (000100) according to Table 4.2. The final stage is to send the amplitude and phase indices to the I/O ports.

Figure 4.7 shows a flow chart illustrating the various stages of the program executed on the dragon-12 board. The program was built and tested. Output screen shots are visible on the chart.


Figure 4.7: Flow chart of the Microcontroller program.

### 4.6 Conclusion

The design architecture for the proposed feed network consists of four stages; switching, phase control, amplitude control and the digital control unit. In this chapter, the features and interconnections between the various components were described. The circuit schematic along with the PCB layout were presented. The
control program was created on a microcontroller unit and its functions has been tested on a prototype board.

## CHAPTER 5

## RESULTS

### 5.1 Simulation Model

AWR Microwave Office is one of the popular microwave circuit simulators. We used MWO to model, design and simulate the feed network. Because we have two paths for the model, two circuit schematics for the model were created. Also, we are going to create two models for the network, one without RF microstrip lines (Hittite Components Only), and the other one including the RF lines. The RF microstrip lines parameters (width and length) will be imported from PCB board that was designed earlier into the design.

For the first circuit schematic (without RF lines), we only need the S-parameters of the components (switches, phase shifter, and amplifier). These S-parameters files are available on manufacturer website [47]. After obtaining these files, we import them within MWO. The S-parameters files should appear as subcircuits in the project.

The base of each package must be directly connected to the ground plane of the board. This is done by sufficient number of via holes. The RF signal lines should have 50 Ohm impedance. All of the RF pins of the components are matched to $50 \Omega$ via proper microstrip line design.

In Figure 5.1, the two circuit schematics for the first model (without RF signal lines) are shown. For branch one, the RF signal goes through the first switch from port RF1 passing through the phase shifter (3-6GHz) to port RF2 for the second switch.

The amplifier comes at the final stage. Branch two is the same as path one except that the switching directions are reversed and the range of the phase shifter is changed (2.5-3.1 GHz). Figure 5.2 shows the circuit schematic of the model (one branch) after including the RF traces that were exported from Altium designer to MWO to take its effect and get better results in the simulation model.


Figure 5.1: Two circuit schematics of the network without RF lines (a) branch one (b) branch two.


Figure 5.2: The circuit schematic included RF traces for one branch.

The S-parameters of the phase shifter are measured at certain angles. The number of digital control bits of the phase shifter are 6 . The number of states for a 6 bit control are 64 states and the phase shifter covers the whole $360^{\circ}$. So, the angle step per bit will be $5.625^{\circ}$ (360/64).

The amplifier covers the range from DC to 6 GHz , and can be programmed to provide anywhere from -13.5 dB to 18 dB of gain, in 0.5 dB step. This is achieved by a 6 bits parallel word provided by the digital control unit.

### 5.2 Plotting Script

If we are going to test the model for each angle and at different gains, we will get very large number of circuit schematics, or we should load the required Sparameter file and redraw it in the circuit schematic. This requires a massive work and is not flexible. By using the feature of MWO called Scripts, this problem can be partially solved. In scripts, one can write his own program to control every single element or graphs in the project.

The AWR design environment exposes a Component Object Model (COM) Automation Application Programming Interface (API). This API can be programmed by several programming languages such as Visual Basic, Java Script, and Visual C++. Using COM Automation client such as a Visual Basic script, the AWR MWO can be easily integrated with any other COM Automation servers. Figure 5.3 shows how a single COM Automation client is used to control a number of applications.


Figure 5.3: COM Automation client used to connect to other COM servers.

The built-in scripting engine allows us to execute scripts form within the program
environment. A full program was developed within MWO to control the number of measurements required, at which phase (or amplitude) to start, and at which certain amplitude (or phase) to be evaluated [48].

When the script is running, it asks the user for two inputs: the number of measurements he/she wants to draw, and which parameter needs to be changed (amplitude or phase) as shown in Figure 5.4. The next screen depends on the user's input from the first screen. If the user choose to change amplitude, the screen in Figure 5.5 will appear. This screen will ask about the starting amplitude and the fixed phase. The script automatically generate the measurements with 0.5 dB steps in amplitude (or $5.625^{\circ}$ in phase). A similar screen for the phase is obtained if we choose phase change in Figure 5.4.


Figure 5.4: The proposed scripting for the AWR environment.


Figure 5.5: Change Amplitude Screen.

### 5.3 Simulation Results

Figure 5.6 shows the simulated insertion loss of the proposed feed network. Figure 5.6(a) shows the insertion loss of path 1, branch 1, as shown in Figure 5.1(a), where the first phase shifter HMC647 (2.5 to 3.1 GHz ) is activated without RF signal lines and Figure 5.6(b) shows the curves for the same branch but including the RF microstrip signal lines as shown in Figure 5.2. Three curves are shown starting at the maximum absolute gain of $18 \mathrm{~dB}(0 \mathrm{~dB}$ relative gain) and 2 other curves that are 0.5 dB lower. We can notice the effect of adding the RF lines where the gain of the signal drops by 1.8 dB . Observe that the amplifier as well as the other component responses are not flat and thus, at the high frequencies, the gain drops further.


Figure 5.6: Simulated insertion loss of the first path.

Also, the amplitude resolution is almost equal to 0.5 dB . By changing the amplitude, the insertion phase is not affected as shown in Figure 5.7. By adding the RF lines to the design, the phase changed to about $26^{\circ}$ but it does not change with amplitude change showing a stable response.


Figure 5.7: Simulated phase response of first path (2.5-3 GHz).

For the second branch of the first path, the phase shifter HMC649 (3-6 GHz) is activated and the insertion loss is indicated in Figure 5.8. Same as the first branch, the amplitude resolution is almost equal $0.5 \pm 0.05 d B$. Adding the RF traces, the signal drops by approximately 1.2 dB as shown in Figure 5.8(b). The effect of adding the RF lines to the design on the insertion phase is that it is
linearly shifted by about $32^{\circ}$ as shown in Figure 5.9 for the gain steps shown in
Figure 5.8.


Figure 5.8: Simulated insertion loss of second path (3-6 GHz).


Figure 5.9: Simulated phase response of second path .

The noise figure (NF) of the feed network is shown in Figure 5.10. The RF line traces adds about 1 dB of noise figure to the design. The figure shows the NF of the two branches covering 2.5 to 6 GHz .


Figure 5.10: Noise figure of the feed network WRF and WORF.

To study the stability of the proposed feed network, the simulated stability factor K and the stability measure B are shown in Figures 5.11 and 5.12 , respectively. We can notice that the network is unconditionally stable over the whole range from 2.5 to 6 GHz . This condition is achieved before and after adding the RF trances.


Figure 5.11: Stability factor.


Figure 5.12: Stability Measure (B).

### 5.4 4-path Simulation Model

The 4-path simulation model can be build by repeating the schematic design for one path (with or without RF traces) 4 times. Because of the symmetry of the design and each path has its own components, the results will be exactly the same as discussed in Section 5.3. Figure 5.13 shows the 4 -path circuit schematic using MWO. The amplitude and phase results will be the same as in Figures 5.6 to 5.9.


Figure 5.13: Circuit schematic for the 4-path model.

### 5.5 Fabricated Board

The designed 2-layer RF feed network board was completed using Altium Designer. Figure 5.14 shows the 3D model of the top layer of the designed board
in Altium. It consists of two-identical paths to be able to feed two antennas. The first path has its RF input at $\operatorname{IN}(1)$ and output at $\operatorname{OUT}(1)$. Note the two branches for the two bands within each path. Dip switches are also visible. The gold color refers to the copper microstrip lines on the top layer. We tried to minimize the board size as much as possible. The whole dimensions of the board were $111 \times 63 \mathrm{~mm}^{2}$, and the material used was FR-4 with a thickness of 0.8 mm .


Figure 5.14: 3D view of the designed programmable wide-band feed network board in Altium.

The fabricated and assembled board is shown in Figure 5.15 after connecting the SMA connectors. The whole board was covered by solder mask except the RF lines since the mask can affect the impedance of the lines. The board was fabricated and assembled in the USA.

The board was measured in the Antennas and Microwave Structure Design Lab-
oratory (AMSDL) at KFUPM. The measurements were conducted using the N9918A(up to 26.5 GHz ) Vector Network Analyzer (VNA) from Agilent.


Figure 5.15: Fabricated (in USA) board of the proposed 2-port network.

### 5.6 Measured Results

The board was measured in AMSDL laboratory in KFUPM using the N9918A
Vector Network Analyzer from Agilent. Figure 5.16 shows the measurement setup.

Figure 5.17 show how the amplitude changes with a resolution of about 0.5 dB , with an error of $+0.22 /-0.12 \mathrm{~dB}$ within the first branch of path 1 covering 2.53 GHz . While the amplifier has a maximum gain of 18 dB to 13.5 dB attenuation, the actual gain of the whole design is about 5.5 dB and going to decrease over a 64 steps of 0.5 dB each. This drop in gain is due to the combined insertion loss
from the other components (typical losses of 11 dB without RF microstrip lines and bends). Figure 5.18 shows 7 amplitude steps measured curves from branch 2 of path 1 covering 3-6 GHz.


Figure 5.16: The measurement setup.


Figure 5.17: Measured results for amplitude change ( $2.5-3 \mathrm{GHz}$.)


Figure 5.18: Measured results for amplitude steps (3-6 GHz.)

The phase changes with a typical step of $5.6^{\circ}$ are achieved and the measured results show very good matching with simulation results. The maximum phase step measured was $6.7^{\circ}$ and the minimum one was $4.6^{\circ}$ with an error about $\pm 1^{\circ}$. The proposed network provides this phase step over the whole frequency band, from 2.5-6 GHz. Figure 5.19 shows 6 measured phase curves covering from $326.25^{\circ}$ to $354.375^{\circ}$ in branch 1 covering $2.5-3 \mathrm{GHz}$. The zoomed curves in Figure 5.19b clearly show the linear steps of approximately $5^{\circ}$ per step. Figure 5.20 shows 6 measured phase curves covering from $140.625^{\circ}$ to $168.75^{\circ}$ in branch 2 covering 3 -

6 GHz . For a linear array feed, a scanning beam of resolution $1.8^{\circ}$ can be achieved using these steps.


Figure 5.19: Measured results for phase steps (2.5-3 GHz.)


Figure 5.20: Measured results for phase steps (3-6 GHz.)

The phase response of the feed network is almost constant. So, the phase resolution from the phase shifters will not affected by the amplifier. Hence, we can change phase and amplitude simultaneously. This makes the network stable and accurate. Fig. 5.21 shows the measured phase response of the feed network for various amplitude steps. The changes in the phases due to amplitude variation is less than $\pm 1^{\circ}$.


Figure 5.21: Measured results for phase at amplitude change (2.5-3 GHz) .

In addition, amplitude stability with change in the phase should be checked meaning that the output amplitude should not change when changing the phase value for a specific branch. Figure 5.22 shows that the flat amplitude doesn't change with phase steps. The measured amplitude variations due to the phase changes is less than $\pm 0.15 \mathrm{~dB}$ for the $3-6 \mathrm{GHz}$ branch. The other branch covering $2.5-3 \mathrm{GHz}$ had a similar behavior.


Figure 5.22: Measured results for amplitude variations due to phase changes (3-6 GHz) .

### 5.7 Conclusion

In this chapter, the simulation model of the wide-band programmable RF feed network was created using MWO based on the S-parameter files for the components. We developed a script within MWO to plot all figures for amplitude and phase, each with its own step. After generating the PCB layout, the RF lines were added to the simulation model to show their effect. The simulated and measured results from a fabricated prototype had very good match for amplitude and phase changes.

The noise figure and stability factors were also studied within MWO and showed that the whole design is unconditionally stable over all the frequency range from 2.5 to 6 GHz . A 4-path simulated model was created which has the same results as the 2-port one.

## CHAPTER 6

## A COMPACT SIZE 12-PORT COMBINER/SPLITTER (C/S)

### 6.1 Introduction

The proposed microwave feed network developed in the previous sections needs a kind of combiner/splitter. This combiner/splitter circuit will be the stage between the feed network and the transceiver used to feed the whole system. In this section, a 12-port combiner/splitter will be designed, simulated, fabricated, and tested.

Power combiners/splitters (dividers) are required in many RF applications. Depending on the operating frequency, the output power, and the size, there are many configurations for the combiners/splitters to satisfy different requirements. For example, coaxial cable combiners are used in wideband applications to combine power amplifiers outputs but they suffer from large sizes.

For an ideal power combiner/splitter (C/S), it should exhibit constant, flat ampli-
tude splitting with linear phase, minimal insertion loss and high isolation. From a practical point of view, it is impossible to achieve all of these considerations in one configuration. So, depending on the end-user defined requirements, appropriate trade-offs can be made. When wide-band and high isolation are needed, big size and high insertion loss appear. Tiny packages with broad-band range can be used but at the cost of isolation and insertion loss.

The ideal power $\mathrm{C} / \mathrm{S}$ should have excellent isolation between its output ports. Above 15 dB , the isolation is accepted, and there is a trade-off between the bandwidth at high frequency and the isolation performance. For example, resistive power dividers can achieve outstanding coverage range, but with low isolation $(6 d B)$. A better performance can be achieved using the Wilkinson power C/S [49]. N-way Wilkinson combiners [13] are widely used in narrow-band applications. The Wilkinson power C/S has very practical applications. In microwave applications, the size of the devices becomes a critical issue especially when printed and compact requirements are emphasized. In general, the higher the frequency, the higher the complexity of the combiners/splitters [50].

In this chapter, a compact 12 -Way $\mathrm{C} / \mathrm{S}$ is designed, analyzed and compared to other configurations of combiners/splitters. The proposed design is based on discrete IC based combiners/splitters. The main purpose of this type of $\mathrm{C} / \mathrm{S}$ is to feed an antenna array of 12 -elements as shown in Chapter 3. Then, we are going to focus on phase and amplitude balance and isolation properties of the proposed design and try to optimize its performance.

### 6.2 Wilkinson C/S

Power combiners/splitters are used to combine the output power from multiple microwave lines (or antenna outputs) and pass them to a receiver in a single output, or split the output of a microwave device (i.e. amplifier to various branches or components (i.e. several antennas)). The traditional N-way $\mathrm{C} / \mathrm{S}$ is shown in Figure 6.1(a). In such a design, the impedances of $N$ transmission lines is equal to $Z_{o} / N$, so, we need a quarter wave $\lambda / 4$ transformer with an impedance of $Z_{o} / \sqrt{N}$, where N is the number of output ports to match them to $Z_{o}$ line impedance. The problem of such design is the isolation performance between the output ports where it is very low. One way to avoid low isolation is to include ferrite isolators in each one of the N-ports. This idea will increase the isolation at the cost of size, insertion loss and the simplicity of the design.


Figure 6.1: N-way power C/S.

The N-way Wilkinson power C/S comes to solve the isolation problem of the basic N -way $\mathrm{C} / \mathrm{S}$ design [13]. There are many configurations of the Wilkinson divider in literature [51-53]. The main idea of Wilkinson is to add a resistors $R_{o}=Z_{o}$ at the parallel terminals as shown in Figure 6.1(b). This will cause matching at all
ports, maintains low loss, and the most benefit is the high isolation between all the output ports. The disadvantage of this design is the use resistors that need to be connected over crossovers which might result in difficulty in the fabrication process. The solution of this problem is to use stepped multiple sections, but this will be at the cost of larger dimensions.

### 6.3 Proposed 12-port C/S

### 6.3.1 Schematic and Board Design

The design architcure of the proposed 12-port $\mathrm{C} / \mathrm{S}$ is shown in Figure 6.2 and Figure 6.3 shows circuit schematic of the design. 3 -way and 4 -way combiners/splitters MMICs are used to construct this structure. The 3-way C/S (SCN-3-28) [54] is ultra-small ceramic packaged IC and covers from 1.6 to 2.8 GHz . The layout and the recommended PCB are shown in Figure 6.4(a) and (b), respectively. It has high isolation between all ports of 12 dB typical and phase imbalance of $5^{\circ}$ typical ( $8^{\circ}$ maximum). The 4-way $\mathrm{C} / \mathrm{S}(\mathrm{BP} 4 \mathrm{U} 1+$ ) [55] is surface mount packaged IC that covers wideband form 1.85 to 3 GHz . Its layout and PCB are shown in Figure 6.5(a) and (b), respectively. It has a maximum phase imbalance of $28^{\circ}$ and a minimum port to port isolation of 15 dB . SMA connectors are connected to the I/O ports. All the footprints of the components were made manually in the PCB layout tool, Altium.

As shown in Figure 6.4 and Figure 6.5, the difference between the outline drawing


Figure 6.2: Design architecture for the proposed 12-port C/S.
in 6.4(a) and the recommended PCB in 6.4(b) is noticeable and this is to make sure that the grounded pads (IC bottom) are totally connected to the board's ground plane via VIA holes. Our PCB layout using Altium is shown in Figure 6.4(c). Figure 6.4 shows three external resistors that are connected to the output ports for isolation purposes and it is a part of the divider according to its datasheet in [54].


Figure 6.3: Circuit schematic for the proposed 12-port C/S.


Figure 6.4: Suggested land pattern for the 3 -way C/S.

The same procedure was done for the 4 -way $\mathrm{C} / \mathrm{S}$ in Figure 6.5. For the SMA connector, we did the footprint shown in Figure 6.6. There is no recommended
layout for this type of SMA for surface mount applications.


Figure 6.5: Suggested land pattern for the 4 -way C/S.

(a) SMA surface mount

(b) Recommended PCB

Figure 6.6: SMA Connector.

The circuit was built on an FR-4 substrate with $\epsilon_{r}=4$ at a frequency of 2.5 GHz . The RF line width for the circuit is 1.56 mm . With Altium Designer, the schematic and the printed circuit model were performed. The final PCB and the 3D layout of the proposed C/S are shown in Figure 6.7. The board occupies approximately $78.6 \times 61.3 \mathrm{~mm}^{2}$.


Figure 6.7: The PCB board of the proposed circuit and the 3D view.

### 6.3.2 V1 Model Results

The simulation model of the circuit was built in MWO. We build the simulation model for the first version (V1), as shown in Figure 6.8, using the S-parameter files given by the manufacturer. After we got the fabricated board, we add the microstrip line traces to the model, as shown in Figure 6.9 to take its effect into account.


Figure 6.8: Simulation model of the 12-port C/S without RF lines for V1.


Figure 6.9: Simulation model of the 12-port C/S included RF lines for V1.

First of all, we fabricate V1 as shown in Figure 6.10. We tried to make all paths symmetrical and identical in length and number of bends. The board consists of $4 \mathrm{C} / \mathrm{S}$ components (one is 3 -way and three are 4 -way) and three resistors. To
connect the board to coaxial cables, 13 SMA connectors are used, one per port. The board size was a approximately $7.857 \times 6.128 \mathrm{~cm}^{2}$.

The simulation and measured results for the first group (G1) of ports (from port 1 to 4) are shown in Figure 6.11. The simulated results for amplitude without and with RF lines shown in Figure 6.11(a) and Figure 6.11(b), respectively. These results shows the different amplitudes of the first four ports. The four ports has approximately the same amplitude with maximum deviation of 0.46 dB and ranges form -11.54 to -12 dB , and the maximum insertion loss of the circuit is about -12 dB.


Figure 6.10: Fabricated board for the first version V1.

To explain the insertion losses of the 12-port $\mathrm{C} / \mathrm{S}$ design, see Table 6.1. The first C/S package (SCN-3-28+) has a 5.6 dB loss and the second C/S package (BP4U+) has a typical 6.7 dB loss. Also the phase imbalance between the four ports, shown in Figure $6.12(\mathrm{a})$, is about $14.03^{\circ}$. As shown in Table 6.1, the components have about $20^{\circ}$ phase imbalance. So, even if we tried to compensate the phase deviation, we cannot guarantee the components response. It changes for every board design. We are going to explain in the design of V2 how to compensate for this phase error.

Table 6.1: Typical performance data of $\mathrm{C} / \mathrm{S}$ components.

| Component | Insertion Loss (dB) | Amplitude imbal- <br> ance (dB) | Phase imbalance <br> (Deg.) |
| :---: | :--- | :--- | :--- |
| SCN-3-28 + | 5.6 (Typ.) | 0.2 (Typ.) | 5 (Typ.) |
| BP4U1 + | 6.7 (Typ.) | 0.47 | 15.39 |

After adding the RF lines to the simulation model, the relative amplitude between the ports had no change, Figure 6.11(b), but the phase in Figure 6.12(b) was changed to $20.3^{\circ}$ due to the small difference in paths' lengths. Also, the total insertion loss of the design was increased by amount of 0.72 dB for the RF lines effect. The measured results are shown in Figure 6.11(c), 6.12(c). Figure 6.11(c) shows the measured amplitude of the first group, G1. The maximum insertion loss was 14.86 dB with a deviation of approximately 0.3 to 2 dB from the simulation results. Since we use the S-parameter representations for the components, the other groups (G2 and G3) for simulation results will be exactly the same as G1, as shown in Figures 6.14 and 6.16. But this is not the case for the measured
results because of the components practically are not identical.

The measured phase for G1, Figure 6.12 (c), has a maximum deviation between the four ports of $28.35^{\circ}$. Also, the maximum deviation for G2 and G3 are 25.71 and $28.08^{\circ}$, respectively. The three groups are around these values of deviations, but they are far for the actual values, i.e., the maximum phase is $52.48^{\circ}, 70.99^{\circ}$, and $56.26^{\circ}$ for G1, G2 and G3, respectively. So, G1 and G3 match each other due to the symmetry of the design, but the second group has a big deviation due to the difference of the main paths (from the output of the 3 -way combiner to the input of the middle 4 -way combiner). This happens because we can control the side groups and guarantee that they are almost symmetrical and this is difficult to achieve for the second group and maintain the compact size in the same time. Also, the second path does not contain any bends, while the other two paths have 4 bends in each one of them.

This was clear in MWO when we tried to compensate the phase difference between all paths by adjusting RF lines lengths. With this process, we compensate the error between the main paths. In the circuit model for the $\mathrm{C} / \mathrm{S} \mathrm{V} 2$, we are going to compensate these phase differences to reduce the phase imbalance for all ports based on the results obtained from the measurements of V1 board. Again, this is not guaranteed to work perfectly because of the fact that the imbalance is not a fixed value for different designs due to fabrication process variations of the ICs.



Figure 6.11: Simulated and measured amplitude results for the first four ports (G1).










Figure 6.15: Simulated and measured amplitude results for the third four ports (G3).
Figure 6.16: Simulated and measured phase results for the third four ports (G3).

### 6.3.3 V2 Model Results

In V2, phase compensation is taken into account. This is based on the results coming from the first design shown in Figure 6.10. The compensated schematic using MWO is shown in Figure 6.17. The rectangular shapes shows the RF lines whose lengths were changed. Measured phases for V1 and V2 for all groups are shown in Figures 6.18 and 6.19 , respectively. As shown in these figures, the maximum deviation in phase is about 19 degrees between all the 12 ports (V2). The phase error ranges are $11.34,8.25$, and 14.49 for G1, G2 and G3, respectively. Using MWO, we tried to compensate the error of the ports phase and it was shown exactly the same for all ports. However, the 4 -way C/S component at the second stage has no guaranteed phase imbalance values. It has typical values of $15^{\circ}$ between its output ports. So, this deviation is expected to happen even if we tried to compensated for it.


Figure 6.17: Compensated model of the 12-port C/S, V2.



The Table in Figure 6.20 shows numerical values for measured phase results for the V1 and V2 for all groups and indicates the maximum values for deviation for phase and amplitude.

|  | Ports | Measured Results V1 |  | Simulation (Compensated) |  | Measured Results V2 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Ports | Amplitude <br> (dB) | Phase (Degree) | Amplitude <br> (dB) | Phase (Degree) | Amplitude <br> (dB) | Phase (Degree) |
| G1 | Port 01 | -14.86 | 52.48 | -12.21 | 112 | -11.53 | 59.93 |
|  | Port 02 | -14.25 | 24.13 | -12.51 | 112 | -11.02 | 70.81 |
|  | Port 03 | -13.96 | 25.58 | -12.63 | 112 | -10.96 | 71.27 |
|  | Port 04 | -14.71 | 34.24 | -12.63 | 112 | -11.15 | 66.94 |
| G2 | Port 05 | -13.29 | 70.99 | -12.4 | 113 | -11.89 | 70.74 |
|  | Port 06 | -12.55 | 45.84 | -12.83 | 113 | -11.03 | 77.92 |
|  | Port 07 | -12.9 | 45.28 | -12.7 | 113 | -10.94 | 78.99 |
|  | Port 08 | -12.96 | 53.05 | -12.7 | 113 | -11.08 | 74.97 |
| G3 | Port 09 | -14.61 | 56.26 | -12.16 | 112 | -11.19 | 63.45 |
|  | Port 10 | -13.84 | 30.68 | -12.47 | 112 | -11.14 | 77.94 |
|  | Port 11 | -13.54 | 28.18 | -12.59 | 112 | -11 | 68.21 |
|  | Port 12 | -14.05 | 36.12 | -12.59 | 112 | -10.86 | 69.06 |
|  | Max | -12.55 | 70.99 | -12.16 | 113 | -10.86 | 78.99 |
|  | Min | -14.86 | 24.13 | -12.83 | 112 | -11.89 | 59.93 |
|  | Max_Dev | 2.31 | 46.86 | 0.67 | 1 | 1.03 | 19.06 |
|  | G1_Dev | 0.9 | 28.35 | 0.42 | 0 | 0.57 | 11.34 |
|  | G2_Dev | 0.74 | 25.71 | 0.43 | 0 | 0.95 | 8.25 |
|  | G3_Dev | 1.07 | 28.08 | 0.43 | 0 | 0.33 | 14.49 |

Figure 6.20: Measured results for V1 and V2.

A simulated 12-port WPD was built to compare its features and performance with our design. The model is designed such that it is comparable with the proposed model. So, we used one 3-Way and three 4-Way WPD. As shown in Figure 6.21, a 12-Way WPD circuit schematic was done using microstrip lines within MWO. We can say roughly that this circuit can occupy a size of $10.3 \times 12.3 \mathrm{~cm}^{2}$. A comparison between the isolation of our model and the WPD is shown in Figure 6.22. WPD shows good isolation but with the cost of large size and crossovers resistors that are difficult to implement.

The isolation of the proposed 12 -port $\mathrm{C} / \mathrm{S}$ was measured between all ports and it provides an isolation better than 22 dB at 2.5 GHz as shown in Figure 6.22(b). The curves shown are for three ports, one from each group (G1, G2, G3). The other ports are similar due to the design symmetry.


Figure 6.21: Circuit schematic of the 12-way WPD.


Figure 6.22: Isolation comparison for the WPD vs the proposed model.

### 6.4 Conclusion

A compact size 12-way power $\mathrm{C} / \mathrm{S}$ is proposed. Two versions of the design were designed and fabricated. In V1, the internal phase imbalance of the ICs make a large imbalance between the ports given that the length of all paths are the same. A compensation process made by adjusting the path lengths and a perfect phase balance was done in simulations and, V2 was created. However, when we fabricate the model, the phase imbalance still exist but with a $60 \%$ reduction compared to V1. The fabricated model occupied $7.8 \times 6 \mathrm{~cm}^{2}$ on a commercial FR-4 board material with thickness of 0.8 mm

## CHAPTER 7

## CONCLUSION AND FUTURE

## WORK

The growing complexity of communication systems and surveillance services means that there is a great demand for antenna systems with high resolution scanning capability. Multiple beams exist when an array of N elements are connected to a beamformer with M beam ports. The beamformer (or antenna feed network) controls the proportion of radiated power at a given location in space. The beamformer, the antenna array, and a real-time feedback about the surrounding environment will lead to what is called "Smart Antenna". So, the beamformer or the antenna feed netowrk is the intelligent part of the smart antenna systems. The ability to control the amplitude and phase feeding the antenna array is highly desirable for phased and multi-beam arrays. In this work a wideband digitally programmable microwave feed network operating in the range form 2.5 6 GHz was designed and fabricated. The fabricated board had a total size of $111 \times 63 \times$
$0.8 \mathrm{~mm}^{3}$. The board was fabricated on a commercial FR-4 substrate. Simulation and measured results agreed well. The feed network is a standalone network that can be applied to any type of antenna array or multi-path RF system. The results showed that the measured amplitude and phase resolutions are 0.5 dB and $5.625^{\circ}$, respectively. The digital control was performed by programming a microcontroller unit with a phased array algorithm.

To use the feed network with an antenna array, a compact size 12-port power combiner/splitter (C/S) was designed and fabricated on an FR-4 material with 0.8 mm substrate thickness. The total size of the board was $78.5 \times 61 \times 0.8 \mathrm{~mm}^{3}$. The phase imbalance due to the internal ICs phase imbalance was minimized by careful PCB design and phase compensation.

### 7.1 Future Work

Some future work that can extend the results obtained in this:

1. Integrate the microcontroller unit with the feed network to have a complete system.
2. Include the combiner/splitter with the feed network on one board a long with the antenna array.
3. Test the feed network on linear and planar array systems to check the beam resolution practically.

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