

**DESIGN AND SIMULATION OF A CURRENT-MODE
FOLDING AMPLIFIER AND ITS APPLICATION IN
ANALOG-TO-DIGITAL CONVERTER**

BY

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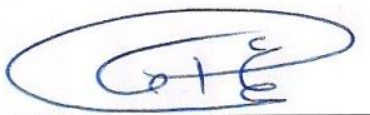
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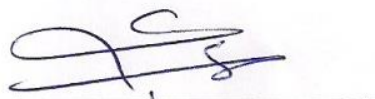
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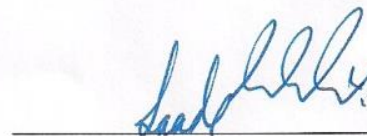
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2013

I would like to dedicate my thesis to

My parents,

My wife

and

My son Muhammad,,

your love and support are always the source of my strength

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First and foremost, I thank ALLAH for all the blessings and wonderful opportunities He has bestowed upon me in my journey through life. It is only by his grace that I have had the ability and strength to overcome life's challenges. May peace and blessing be upon his prophet Mohammed (PBUH), his family and his companions.

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ABSTRACT

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The applications of CMOS current-mode circuits have increased dramatically. Current-mode signal processing has some recognized advantages over voltage-mode signal processing in low voltage and low power application.

Folding is a technique to reduce the complexity of the flash A/D converter by reducing the number of comparators while maintaining a relatively good conversion speed. In other words, in folding A/D converters the number of comparators can be reduced significantly via an analog preprocessing circuit.

This thesis deals with design and simulation of a 5 bit new CMOS current-mode folding flash analog-to-digital converter (ADC). A new current-mode folding amplifier is designed to be used as the core block in the folding ADC, which produces a nearly ideal saw-tooth input-output characteristic. The proposed design reduces the complexity of the ADC by reducing the number of comparators, silicon area and power consumption. The functionality of the different building blocks and ADC is simulated using Tanner simulation tools in 0.35 μ m CMOS technology. The power dissipation of the proposed folding ADC is 1.26mW using a $\pm 1V$ power supply. Simulation results are in excellent agreement with the theory.

ملخص الرسالة

الاسم الكامل : شاكر أحمد محيود

عنوان الرسالة : تصميم ومحاكاة نموذج التيار لمكبرات الطي وتطبيقاته في التحولات من تماثلي الى رقمي

التخصص : هندسة كهربائية

تاريخ الدرجة العلمية : مايو 2013

التطبيقات لدوائر التيار من نوع CMOS زادت بشكل كبير. فمعالجة إشارات التيار لديها بعض المزايا على معالجة إشارات الجهد في دوائر الجهد المنخفض والتطبيقات ذات الطاقة المنخفضة.

الطي هو تقنية لتقليل عدد المقارنات المستخدمة في محول تماثلي- رقمي من نوع ومبضي مع الحفاظ على سرعة تحويل جيدة نسبياً. وبعبارة أخرى، باستخدام مكبر طي يمكن تقليل عدد المقارنات في دائرة محول تماثلي- رقمي من نوع الطي.

هذا البحث يهدف الى تصميم ومحاكاة محول تماثلي- رقمي من نوع ومبضي يعمل في نطاق التيار باستخدام ترانزستور من نوع CMOS. مضخم التيار من نوع الطي الجديد صمم لكي يتم استخدامه في المحول، والذي ينتج إشارة سن المنشار. وهذا التصميم يؤدي الى تقليل عدد المقارنات المستخدمة ومن ثم المساحة المطلوبة من السليكون والطاقة المستهلكة. تم محاكاة عمل المحول باستخدام احد البرامج المعتمدة من الصناعة وتقنية $0.35\mu\text{m}$. الطاقة المستهلكة لهذا المحول التماثلي-الرقمي المقترح 1.26mW عند استخدام مزود الجهد 2 فولت. كما تبين ان نتائج المحاكاة متطابقة تماما مع النظرية.

CHAPTER 1

INTRODUCTION

The world around us is analog. The analog to digital converter (ADC) is one of the most important building blocks to interface analog world to the digital world. An ADC is an electronic circuit that converts continuous signals to discrete digital signals. The reverse operation is executed by a digital-to-analog converter (DAC). Lately, the applications for ADCs have extended widely in numerous applications. For example: digital telephone transmission, cell phones, and medical imaging. Generally, ADC design requires more power and the circuit is more complicated than DAC to achieve a certain speed and resolution [1]. The idea of the ADC process is shown in Figure 1-1. The analog input signal is applied to the ADC and after a certain amount of time the conversion will be established, and the convertor provides a digital code at its output.

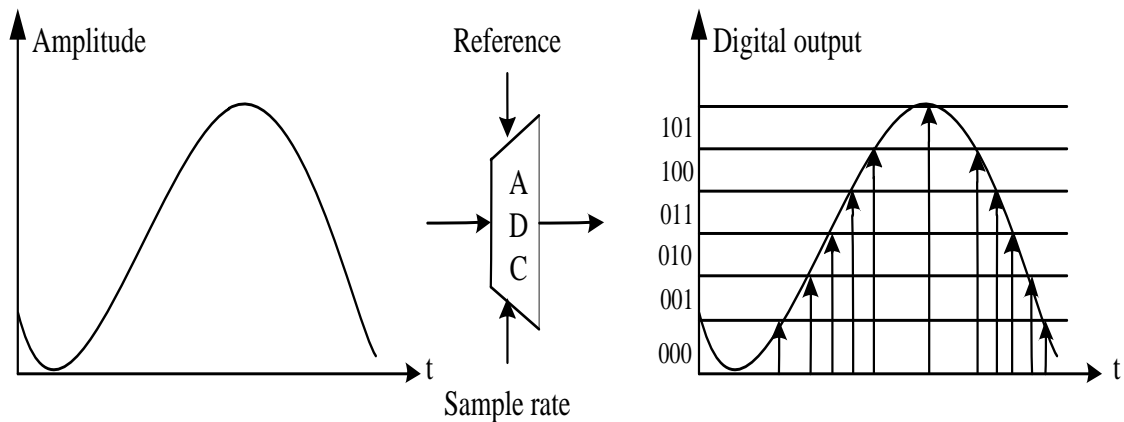


Figure 1-1: Analog-to-digital converter (ADC)

Digital systems have significant advantages over analog systems. Digital systems allow flexibility in reconfiguring the digital systems operation simply by changing the program. Digital systems offer much better control of accuracy requirements than analog systems. Digital signals are easily stored and digital implementation is cheaper than analog counterpart. Based on the advantages of digital systems, many practical systems have used digital signal processing. For example, image processing; telephone transmission, medical imaging, and detection of nuclear explosions and in vast variety of other applications. Figure 1-2 shows the block diagram of a complete signal processing system: it is clear that ADC is the core block in such system and the efficiency of the system will depend much on the ADC.



Figure 1-2: Block diagram of a complete system

ADCs are found in different architectures and each one has unique characteristics and different limitations, so the most convenient conversion technique should be chosen based on the application. The most common types of ADCs are flash, successive approximation and sigma-delta.

This thesis describes the design and simulation of a 5-bit current-mode folding ADC realized by using 0.35 μ m CMOS technology. The ADC is designed to meet certain

design specification. The design techniques and issues of folding and interpolating ADC will be further explained in the next sections.

1.1 A/D Converter Characteristics

The definitions and descriptions of important parameters and characteristics for A/D converters are as follows:

1.1.1 Resolution

Resolution is defined as the smallest amplitude change in the input signal that can be determined by ADC. It is typically represented by the number of bits in the ADC and the full-scale range of the device to represent the output digital signal. The size of each step which is equal to the LSB bit voltage or current is given by

$$\text{LSB} = \frac{FS}{2^N - 1} \quad (1-1)$$

Where FS is the full scale range or the amplitude of the input signal and N is the number of bits. Higher resolution implies a better accuracy of the digital representation. As an example, the LSB is $0.533\mu\text{A}$ for the case of 4-bit resolution and $8\mu\text{A}$ amplitude of the input analog signal.

1.1.2 Sampling rate

Sampling rate or sampling frequency is defined as the number of samples of the input signal taken per second. The sampling rate is the speed at which analog input samples can be continuously converted into a digital word.

1.1.3 Power dissipation

Power dissipation in electronic devices is defined as the conversion of electrical energy of power supply to heat. In general, complex circuits with high-resolution tend to consume more power than simpler lower resolution circuits.

1.1.4 Chip area

CMOS ICs are fabricated on thin circular slices of silicon called wafers. Each wafer may contain as few as 20 or 30 ICs or as many as several hundred or even several thousand of individual chips or die. Typically, should be minimum.

1.1.5 Signal to noise ratio (SNR)

Signal to noise ratio is a very important dynamic specification of an A/D converter in digital signal processing systems. SNR is defined as the ratio of the output signal power to the output noise power. For an N-bit ideal A/D converter with a sinusoidal input, the SNR can be expressed as [2] :

$$\text{SNR} = 6.02 * N + 1.76 \text{ (dB)} \quad (1-2)$$

Equation (1-2) can be used to evaluate the performance of any quantizer relative to the ideal.

1.1.6 Signal-to-noise and distortion ratio (SINAD)

The ratio of the signal to the noise and distortion is defined as SINAD, S/N+D, or SNDR which is the ratio of the *rms* value of the output signal to *rms* sum of all other spectral components [3].

One of the most important parameters for an A/D converter is SINAD because it represents the most significant noise and nonlinearity of an A/D converter.

1.1.7 Effective number of bits (ENOB)

ENOB represents the dynamic performance of an ADC, which gives the conversion bit of an ADC at a specific input frequency. ENOB is computed as shown below [3]:

$$\text{ENOB} = \frac{\text{SNDR} - 1.67}{6.02} \quad (1 - 3)$$

1.1.8 Spurious-free dynamic range (SFDR)

SFDR is the ratio of the strength of the fundamental frequency to the strongest spurious signal in the output, representing a usable dynamic range of an A/D converter [3].

1.1.9 Differential Non-Linearity (DNL)

DNL is defined as the difference between two adjacent codes at each vertical step in percent or LSBs, as shown in Figure 1-3 [3].

Other possible definitions DNL of ADCs is the difference between an actual step width and the ideal value of 1LSB, as shown in Figure 1-4 [4].

$DNL = \text{Actual step (code) width} - \text{Ideal step (code) width}$

1.1.10 Integral Non-Linearity (INL)

INL is defined as the difference between of the output signal or output code of an A/D and ideal finite resolution characteristic measured vertically in percent or LSBs, as shown in Figure 1-3 [3].

Other possible definitions INL of ADCs is INL error is described as the difference between the actual data converter code transition points and a straight line. A straight line is drawn between the end points of the first and last code transitions as shown in Figure 1-4. When INL is smaller than or equal to ± 0.5 LSB, this converter is monotonic [4].

The monotonicity of the converter means that the output of, for example, ADC never decreases with an increasing analog input signal.

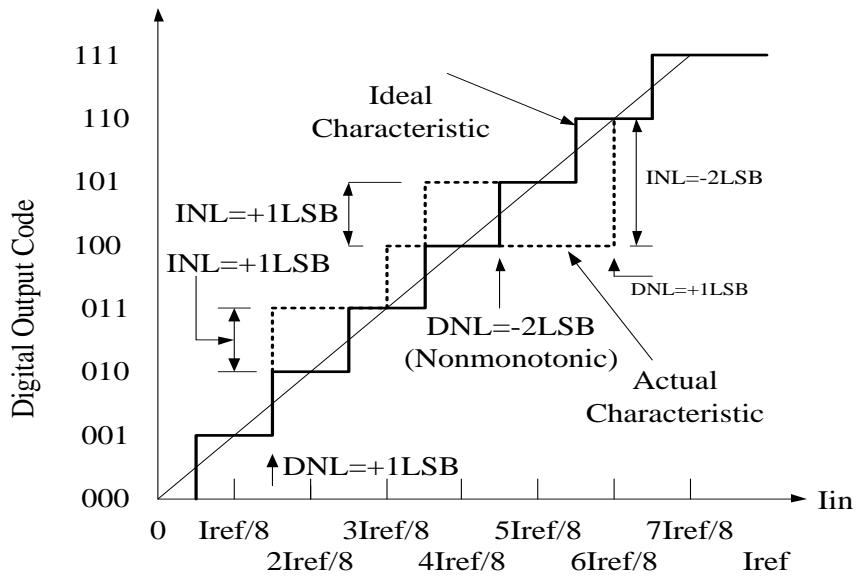


Figure 1-3: INL and DNL in A/D Converter first definition

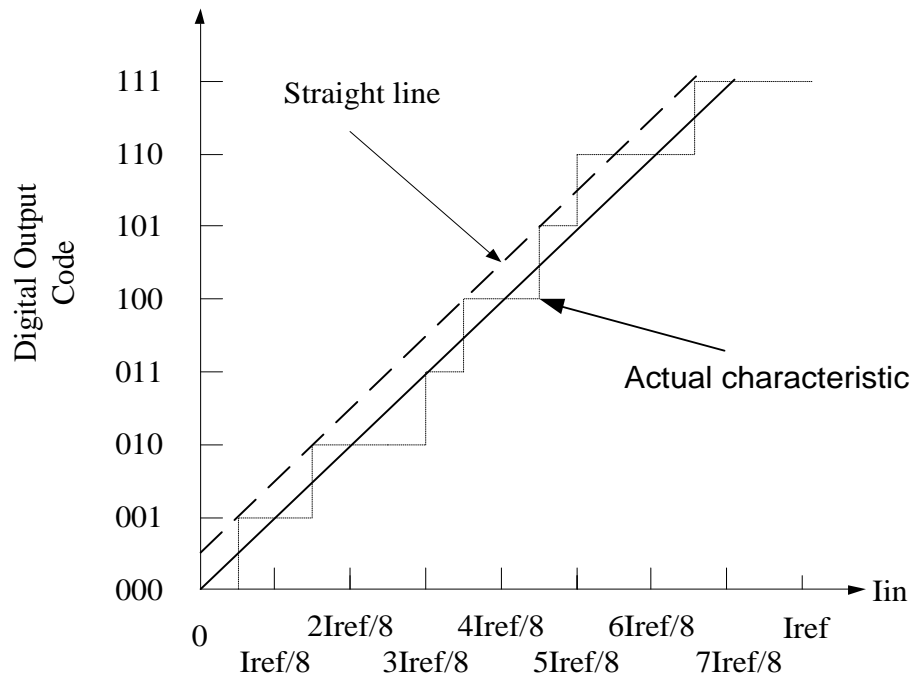


Figure 1-4: INL and DNL in A/D Converter second definition

1.2 High Speed A/D Converter Architectures

There are many different types of architectures for implementing ADCs, depending on the type of application. There are three categories to classify those types of ADCs depending on their speed of operation which are low speed ADC, medium speed ADC and high speed ADC.

In the following section flash and folding of the high speed ADC architecture is described.

1.2.1 Flash (Fully parallel) ADC

High speed ADCs are required in many applications. Flash ADC (also known as a direct conversion ADC) is the fastest ADC architecture, because the conversion speed in flash ADC is only one clock cycle per conversion. Several architectures of flash ADC are implemented in both voltage-mode and current-mode. A simple way to build a high-speed ADC is to use a flash (fully parallel) structure [5]-[14]. The concept of voltage-mode flash A/D converter is straight forward. The function of flash ADC is to compare the analog input to a set of reference voltages and feed these outputs to encoder to produce digital output. Figure 1-5 shows a typical voltage-mode flash A/D converter block diagram.

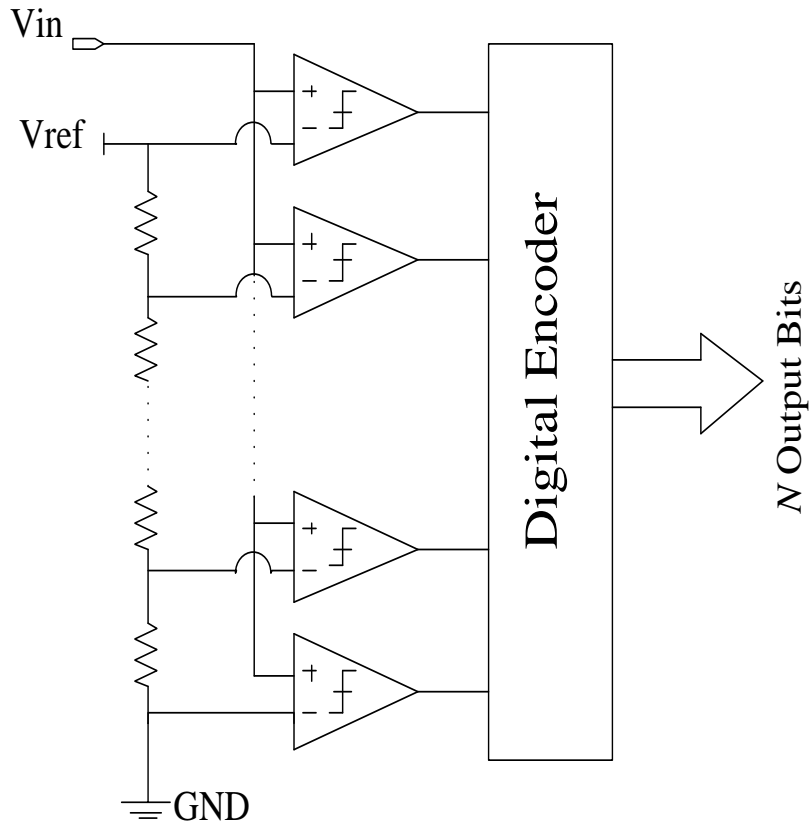


Figure 1-5: Voltage-Mode Flash A/D converter Architecture

Generally, an N bit voltage-mode flash ADC consists of 2^N resistors, $2^N - 1$ comparators. Each comparator has two inputs; one is connected to the analog input and a second input to a reference voltage. The reference voltage is generally generated by a resistor string and the difference between these reference voltages is equal to the least significant bit (LSB) voltage. The output of the comparators is called thermometer code (TC). This thermometer code is fed into digital encoding logic that converts $2^N - 1$ inputs to N bits binary code (BC).

For example, a four bit voltage-mode flash ADC consisting of 16 resistors and 15 comparators generates 15 bit thermometer code, which is encoded to four bits digital output using a digital encoder.

In this thesis, a 5 bit current-mode folding ADC is considered. Current-mode flash A/D converter architecture is shown in Figure 1-6 [6]. Fully-flash ADC is composed $2^N - 1$ comparators with N-bits of digital output resolution. Each comparator has two inputs; one is connected to the analog input and the second is connected to a reference current. These current references are generally realized using PMOS current mirrors for positive reference currents and NMOS current mirrors for negative reference currents. The output of the folding amplifier is the input signal of the current-mode flash. This signal is copied and distributed to all comparators using identical current mirrors. The Digital output is generated by using digital encoder.

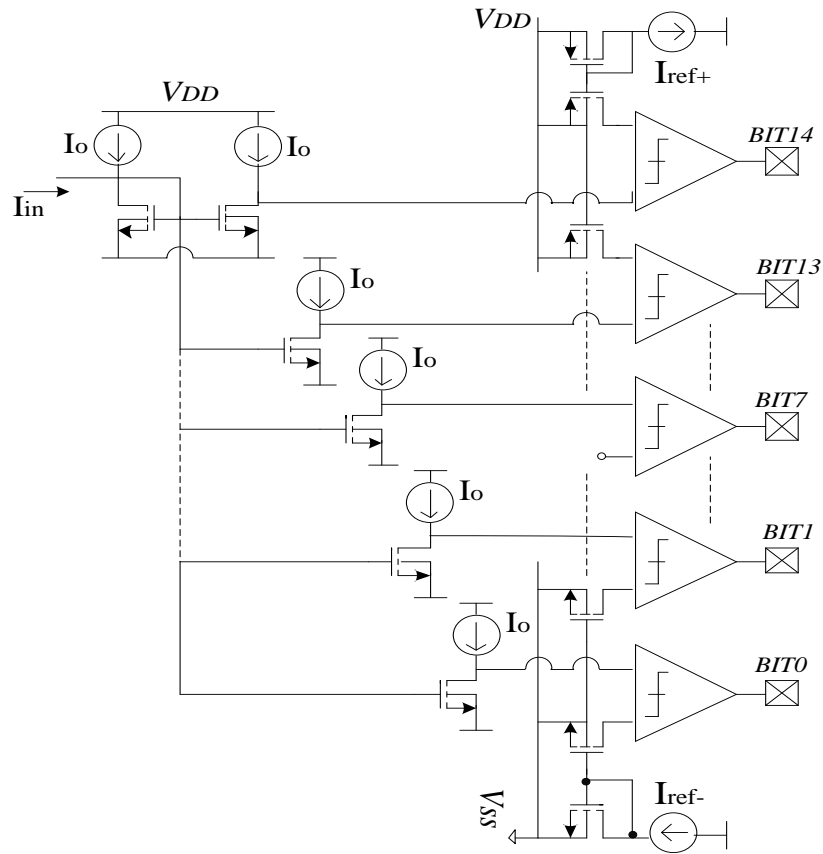


Figure 1-6: Current-Mode Flash A/D converter Architecture.

The fastest and conceptually simplest conversion process is full flash or parallel flash ADC, because the whole ADC processes finishes in one step. On the other hand, the full flash ADC suffers from several drawbacks:

- The hardware complexity increases exponentially when the number of bits increases. For N-bit resolution, it needs $2^N - 1$ comparators. This limits flash converter to 8-bits resolution.

- Large power consumption.
- Large chip area.

1.2.2 Interpolating Flash ADC

Interpolating A/D converters are used to reduce the input capacitance and the number of preamplifiers in flash architectures. Figure 1-7 shows the 4-bit interpolating ADC using an interpolation factor of four [2].

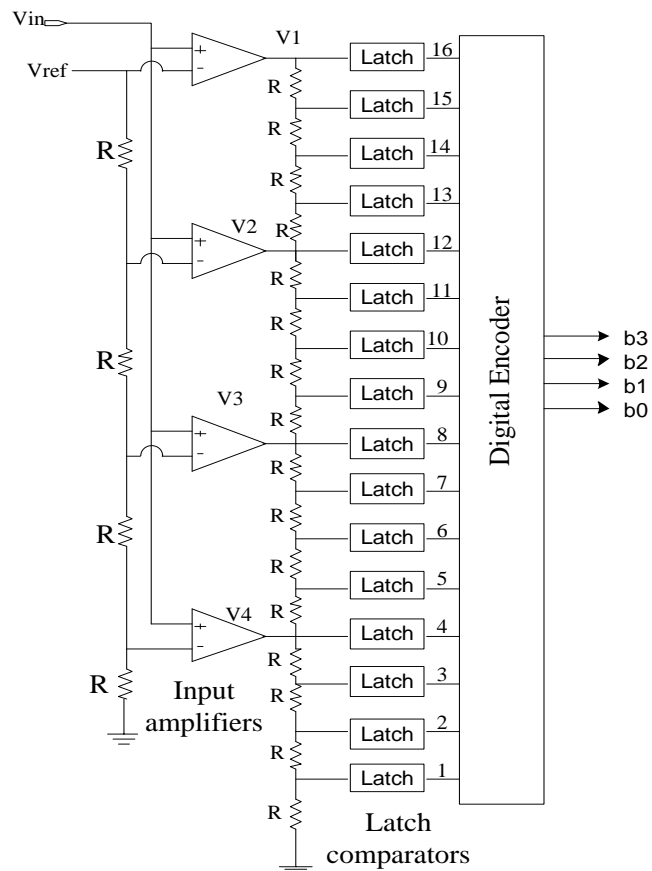


Figure 1-7: 4-bit Interpolating ADC (interpolating factor of 4)

There are two types of interpolation; current-mode and voltage-mode interpolation [15]. In voltage-mode interpolation resistors are used in most conventional flash and folding ADCs [16], whereas current-mode interpolation uses current mirrors [17].

The main benefit of an interpolating technique is to reduce the number of differential pairs attached to the input signal. This will provide less input capacitance, which is quite high for a flash converter, and reduce the power consumption. In addition, interpolation technique is used in folding ADCs to reduce the number of folding amplifier by generating extra folding waveforms. Generally speaking, the folding and interpolation achieve high speed, medium resolution, and low power consumption which is required in many applications.

There are many techniques used to reduce the number of comparators. The first technique is called subranging. The ADC subranging is slower than the flash ADC, because it needs two or more steps to complete the conversion. The second technique is called folding. This technique reduces the complexity of flash ADC while keeping high conversion rate. The third technique is called pipeline, in which the speed is much slower. In this thesis, we will focus on folding ADC. The number of comparators can be reduced significantly, by using the folding technique that produces more zero-crossing points than flash ones. Folding architectures can run at high sampling rate and low power consumption.

1.2.3 Folding ADC

Interpolating architecture can be used to reduce the number of input amplifiers (preamplifiers). Interpolation ADC has the same number of comparators as flash ADC which is almost equal to 2^N for an N-bit converter. This large number of comparators can be significantly reduced by using a folding architecture. The architecture of the folding ADC is as shown in Figure 1-8. In folding A/D converter the MSB and LSB bits are generated separately using coarse and fine quantizers respectively.

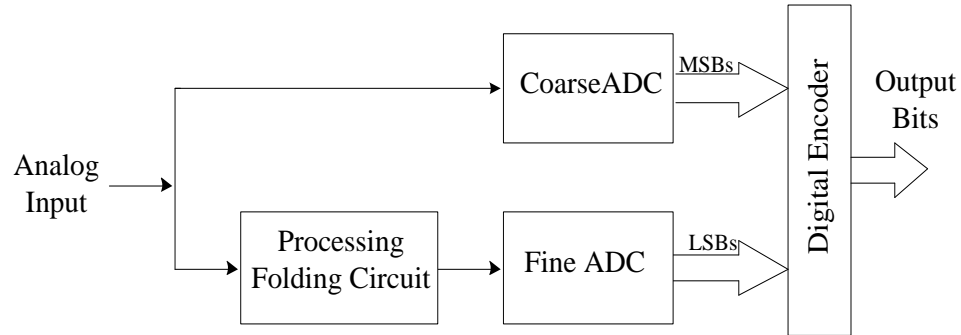


Figure 1-8: Folding ADC topology

The total resolution of folding ADC is $N = N_{MSB} + N_{LSB}$, where N_{MSB} and N_{LSB} are bits determined by coarse and fine converter respectively. The analog preprocessing consists of the folding circuits; this folding circuit could be current-mode or voltage-mode depending on the application requirements.

More information about folding ADC has presented in chapters 2 and 3.

1.3 Motivation

In the last few decades, ADC applications have grown dramatically leading to the development of many low cost integrated circuits. The demand for a low cost, low power and high speed ADC is ever increasing. In this thesis, two different ADC architectures are studied; one is a low resolution ADC and the other is a moderate resolution ADC.

Folding A/D converters are one of the fastest ADC. Current-mode folding amplifier is the core block in folding ADC. The accuracy of ADC depends heavily on the accuracy of the folding amplifier. The motivation of this thesis is to design and improve the performance of folding ADC using current-mode folding amplifier. The proposed current-mode folding amplifier should generate saw-tooth waveform instead of triangular waveform. Thus, the complete current-mode folding ADC should have good features like high accuracy, low voltage, low power consumption, occupying small chip area and operating at high speed.

To achieve the above requirements, the following tasks will be carried out:

- I. Develop a new current-mode folding amplifier to generate saw-tooth waveform.
- II. Investigate and evaluate a good current-mode comparator to be used in the design of folding ADC.
- III. Design and simulate a 5 bit current-mode folding ADC.

1.4 Problem Statement

A key element in the design of the folding ADC is the folding amplifier, and due to the wide application of ADCs, the area is open for more development especially in the current-mode approach.

The current-mode folding amplifier is available in the open literature; produce a triangular waveform, which will reduce the accuracy of ADC and leads to error, more details are given in chapter 3. This thesis will focus on designing a CMOS current-mode saw-tooth folding amplifier that is used in a current mode analog-to-digital converter (ADC). Folding the input signal to saw-tooth shape will enhance the accuracy of the conversion. Such amplifier is not available in the open literature and patent resources.

1.5 Thesis Organization

Chapter 1, INTRODUCTION, presents the ADC characteristics, high speed ADC architectures, motivation and the organization of thesis.

Chapter 2, LITERATURE REVIEW, summarizes previous work of folding ADC and current comparator and discusses the research goals.

Chapter 3, FOLDING A/D CONVERTER, presents the proposed techniques to overcome the problems of the triangular waveform of folding ADC. Also, a comparison is made between different current comparators to select the best and suitable one for our proposed design. Digital encoder is designed.

Chapter 4, DESIGN AND SIMULATION RESULTS, presents the design of a 5 bit current-mode folding ADC.

Chapter 5, CONCLUSION AND FUTURE WORK, a summary of the thesis is provided along with recommended future studies and extensions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The literature review is intended to give information about what has been done so far in ADC design. An extensive review was conducted to survey the methods of designing ADC based on both voltage and current mode folding amplifier.

As stated before, using the folding technique in ADC design, the number of comparators required in the quantization process, decreases as the order of folding increases. The concept of folding was introduced by Arbel and Kruz in 1975 and is confirmed to be efficient for moderate resolution and high speed ADC applications [18]. Initially folding ADCs have been successfully implemented in bipolar technologies [19] -[22], but now it is implemented in both CMOS and BiCMOS technologies [23] - [29].

2.2 Voltage-Mode Folding ADC

The core building block in voltage-mode ADC is the folding amplifier. A CMOS implementation of the voltage-mode folding amplifier based on differential pair is presented in [30]. The folding amplifier circuit consists of eight differential pairs with

the outputs of the odd and even numbered differential pairs cross coupled. One of the inputs is connected to the converter input voltage and the other one is connected to the reference voltages generated by a resistive ladder. The proposed 8-bit conventional folding amplifier is designed using differential pairs with small tail currents (40 μ A). The proposed circuit operates from 5V supply and consumes 110mW at 70Ms/s using. This type of folding amplifier suffers from several drawbacks, like non-linearity differential pairs, high power supply voltage requirement, and the zero crossing offset error due to the mismatch between current sources. In reference [31] a good solution to obtain larger bandwidth by using common-gate amplifiers as a load to the differential pair. The input signal is voltage, but the output of the proposed folding amplifier is current. Using current-mode signal processing in the fine quantizer path to reduce voltage swings and achieve high speed, this folding amplifier is suitable for low voltage high speed applications. A 7-bit 300MSamples/s folding and interpolating ADC has been designed to produce a bandwidth up to 60 MHz and consumes 200mW from 3.3V power supply. The chip area is 1.2mm^2 using $0.35\mu\text{m}$ CMOS technology. The reference voltages of this circuit are generated using a resistive ladder; this dissipates more power and needs large area. Also, transistor sizes of the folding amplifier must be large enough to ensure that the offset voltage is much smaller than one LSB. In [16] a CMOS folding and interpolating ADC was proposed. MOS-transistors-only folder block is introduced which contributes to a small chip area. An INL/DNL of 0.77 LSB/0.6 LSB was measured. The circuit can operate from a 3.3 V supply and was implemented in a $0.18\mu\text{m}$ CMOS process. The active area is 0.25mm^2 and consumes a total power of 181mW. Guo et. al [32] developed a current-steering voltage-mode folding amplifier. The amplifier has

several advantages over conventional voltage-mode folding amplifier. It requires a single current source, so the matching is not needed whereas the power consumption is reduced. The circuit was simulated at both 5V and 3.3V using 0.6 μ m and 0.25 μ m CMOS processes technology. It was concluded that this current steering amplifier runs much faster than the conventional folding amplifier at the same power consumption. Oza and Devashrayee in [33] and [34] presented two voltage-mode differential amplifier based folding amplifier with a folding factor=4 operating from 1.5V supply voltage [34] and a folding factor =8 operating from 1.7V supply voltage [34]. The proposed structures in [33] and [34] were simulated and implemented using 0.18 μ m and 0.13 μ m CMOS processes technology respectively. In reference [35] a threshold inverter quantization (TIQ) technique has been proposed for reduction of power and area in folding block of folding and interpolating ADC. Reference ladder inverters are used instead of resistors and as a result the area and static power consumption are expected to be lower and improves the frequency response. The disadvantage of this circuit is the threshold of inverter is a function of temperature. If there is a variation in surrounding temperature the threshold voltage of inverter will change. Lee et. al [36] have implemented a 6-bit 1GSPS folding ADC operating from a 1.8v supply voltage. The proposed architecture was based on a fully folded ADC using the resistive interpolation technique for Ultra Wide Band (UWB) applications. ADC achieves an effective resolution bandwidth (ERBW) of 200MHz, when the clock speed is 1GHz and the power consumption is 60mW. The measured results for INL and DNL are ± 0.7 LSB, ± 0.5 LSB, respectively. For an input signal of 100MHz frequency and clock frequency $F_s=1$ GHz, the measured SNDR is

33.64dB. The chip is realized using 0.18 μm CMOS technology and the active chip area is 0.27 mm^2 .

2.3 Current-Mode Folding ADC

It will be mentioned in this chapter section 5 why the current-mode circuits have more advantages over its voltage-mode counterpart. An 8-bit CMOS current-mode folding ADC with three-level folding amplifier has been presented in [37]. The proposed circuit not only reduces the number of reference current sources, but also enhances the performance of the folding block. The proposed circuit was implemented using 1.5 μm n-well CMOS technology and operated from a 5V power supply. In reference [38] current-mode folding amplifier based on the current mirror with folding factor = 5 was presented. Using this folding amplifier it is much easier to achieve an excellent piecewise linear transfer characteristic of the folding amplifier; usually a triangular-shape. The proposed circuit was implemented using 0.35 μm CMOS process and can operate from a 3V supply voltage. The proposed circuit is suitable for lower voltage design. However, the channel length of the transistor should be large to get sufficient accuracy, and this will lead to lower speed and large area. In reference [39] the authors presented a current-mode folding amplifier with a folding factor = 16 operating from 1.5V supply voltage and implemented in 0.18 μm CMOS process. This amplifier is constructed based on current mirrors, so higher linearity and lower distortion for ideal triangular transfer characteristic

curve is much easier to achieve compared with the voltage-mode based on conventional differential pair. Folding amplifier with high folding rate, high linearity and low distortion is verified to be more suitable for low supply voltage.

A key element in the design of the folding ADC is the folding amplifier, and due to the wide application of ADCs, the area is open for more development especially in the current -mode approach.

A summary of various ADCs performances is presented in Table I.

Table I: Summary of various CMOS folding ADCs.

Reference	[30]	[26]	[23]	[39]	[16]	[36]
Publication	1995	1996	2003	2006	2006	2008
Technology	0.8 μ m CMOS	1 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Bits	8	8	7	8	8	6
Type	VM	VM	VM	CM	VM	VM
Sample and Hold	No	Yes	Yes	No	Yes	Yes
Input BW (MHz)	6	5	60	1	4	200
Speed Ms/s	70	125	300	NA	200	1000
Supply Voltage	3.3V	5V	3.3V	1.5V	3.3V	1.8V
Power consumption	110mW	255mW	200mW	NA	181mW	60mW

NA: Not available

2.4 Current Comparator

In general, the current comparator is used to compare signals between two terminals with varied current and produces a digital output. Comparators are widely used in many applications such as data converters, oscillators, and sensor circuit as well. Current comparators are essential in most of the data converters designed in current mode. In reference [40] one of the most famous designs of current comparators is proposed by Traff in 1992 as shown in Figure 2-1.

The proposed circuit is designed based on a combination of two inverters with positive feedback. In most of the published works, Traff results are set to be a reference although it was simulated using the $2\mu\text{m}$ CMOS technology.

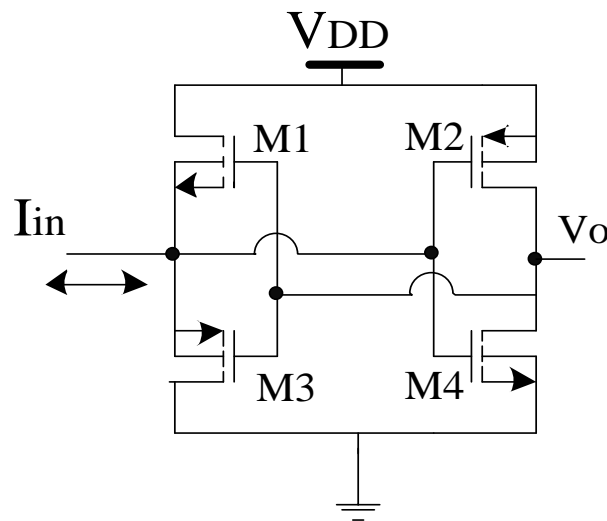


Figure 2-1: Schematic diagram of Traff's circuit

In reference [41] the authors presented a new high-speed current comparator. The proposed circuit was implemented in 1.6 μm CMOS technology and can operate from a 5V power supply. The disadvantages of this proposed circuit are the increased complexity and power consumption. On the other hand, the speed/power ratio is increased at low input current. The authors in reference [42] reported the design of a current comparator and its implementation in 0.35 μm CMOS process. The proposed circuit can operate from 3V supply voltage. The simulation results reported in this work shows the improvement in the response time as well as power consumption.

Comparators are key building blocks in ADCs. The performance of ADCs is directly related to the accuracy of the folding amplifier and comparator used.

A summary of performance comparisons used for current comparators is presented in Table II

Table II: Summary of various CMOS current comparator

Reference	Traff [40]	Tang [41]	Lin et al. [42]	Banks and Toumazou [43]	Tang [44]
Publication	1992	1994	2000	2008	2009
Technology(μm)	2	1.6	0.35	0.35	0.18
Power supply(V)	5	5	3	3	1.8
Propagation delay(ns)	10	11	2.8	14	0.6
Power consumption(μW)	390 (at 10nA)	1400 (at 100nA)	580 (at 100nA)	300 (at 10nA)	NA
Minimum Input Current amplitude (nA)	500	10	50	10	100

2.5 Why Current-Mode?

A conventional voltage-mode folding amplifier is built based on differential pair. It is well known that the differential pair is not suitable for low voltage design because of nonlinearity problem. Recently, the applications of CMOS current-mode circuits have increased dramatically. Current-mode circuits have some recognised advantages over voltage-mode. They show high speed, large dynamic range, large bandwidth, low supply voltage, high accuracy and less sensitivity to power and ground noise [45][46].

The reason for choosing current-mode signal processing is that a lot of signal sources are a current type like photo sensors, temperature sensors and several biomedical circuits. This current-mode approach is also practically useful in the analog integrated circuit (IC) environment.

2.6 Research Goals

The objective of this thesis is to design and simulate a 5-bit folding ADC using Tanner Tools. From the literature review it is obvious, that the folding amplifier circuit is a core circuit in the design of folding ADCs. The proposed current-mode folding amplifier is used to fold or map the input signal to saw-tooth like waveform using current-mode folding amplifier, which will provide a good performance of folding ADC to be compatible for many applications. This current-mode folding amplifier will be used in the design of

folding flash ADC. The proposed block diagram of current-mode folding amplifier is shown in Figure 2-2.

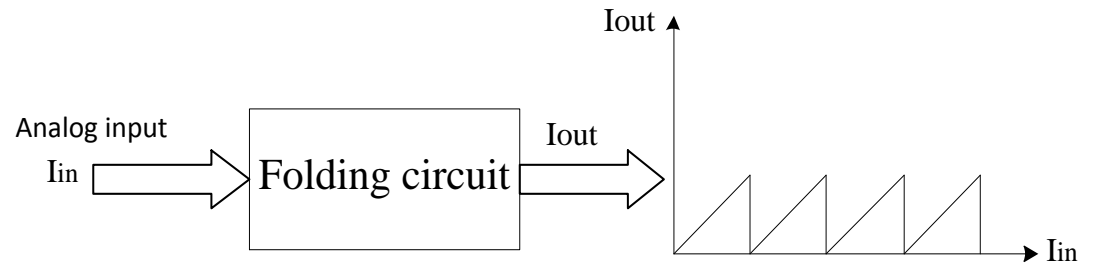


Figure 2-2: Block Diagram of Current-Mode Folding Amplifier

CHAPTER 3

FOLDING A/D CONVERTER

3.1 Introduction

Folding ADC is a combination of two ADC architectures, the flash and the folding architecture. Flash architecture is used in the coarse quantizer and folding architecture with flash architecture is used in fine quantizer. However, flash is built based on current-mode comparator and digital encoder.

Folding ADC is one of the best solutions for flash ADC to digitize the analog signals. Folding architecture reduces the number of comparators required for fully parallel (flash) architectures, while retaining the advantage of high speed. Folding is good candidate for low-power implementations of medium resolution (6 to 10b). This chapter will focus on folding ADC architectures; current comparator and digital encoder to implement a suitable folding ADC.

3.2 Concept of Folding

Earlier the folding technique was used to generate sine wave [47]. Later on, the folding circuit was used in the design of ADCs. The purpose of folding ADC converter is to form

the residue signal with simple analog circuits. Fundamentally, the circuit folds the input signal by a factor called folding factor (FF). This folding factor determines the number of signals to be combined and reduces the number of comparators. In flash ADC, $2^N - 1$ comparators are required for an N-bit resolution. In folding ADC, the number of comparators is decreased dramatically. For $(N = m + l)$ bits resolution with m most significant bits and l least significant bits, the number of comparators required for folding ADC is $(2^m - 1)$ MSB comparators and $(2^l - 1)$ LSB comparators. The total number of comparators used is $(2^m - 1) + (2^l - 1)$ instead of $2^{m+l} - 1$ for an equivalent resolution full flash ADC.

Folding is a type of analog preprocessing that is used to produce more than one zero-crossing point which reduces the number of comparators, and thus, the power consumption and silicon area of a flash ADC. The block diagram of the basic folding ADC and its characteristics are shown in the Figure 3-1 and Figure 3-2 respectively. The input signal is applied to an analog preprocessing circuit called folding amplifier, and the output of this folding circuit is connected to a fine quantizer. Also, the input signal is directly connected to a coarse quantizer. The coarse digital output represents the most significant bits (MSB) and the fine digital output will produce the least significant bits (LSB). The total bit resolution (N_B) of the folding ADC is $N_B = b_{MSB} + b_{LSB}$. Note that, both coarse and fine quantizers are full flash.

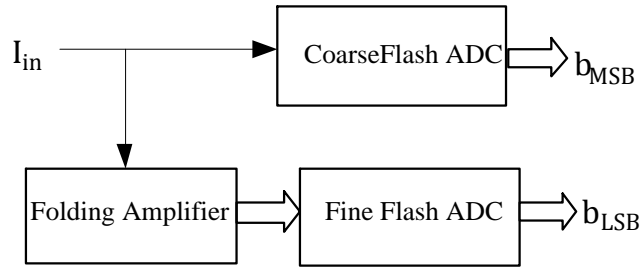


Figure 3-1: Block diagram of current-mode folding flash ADC

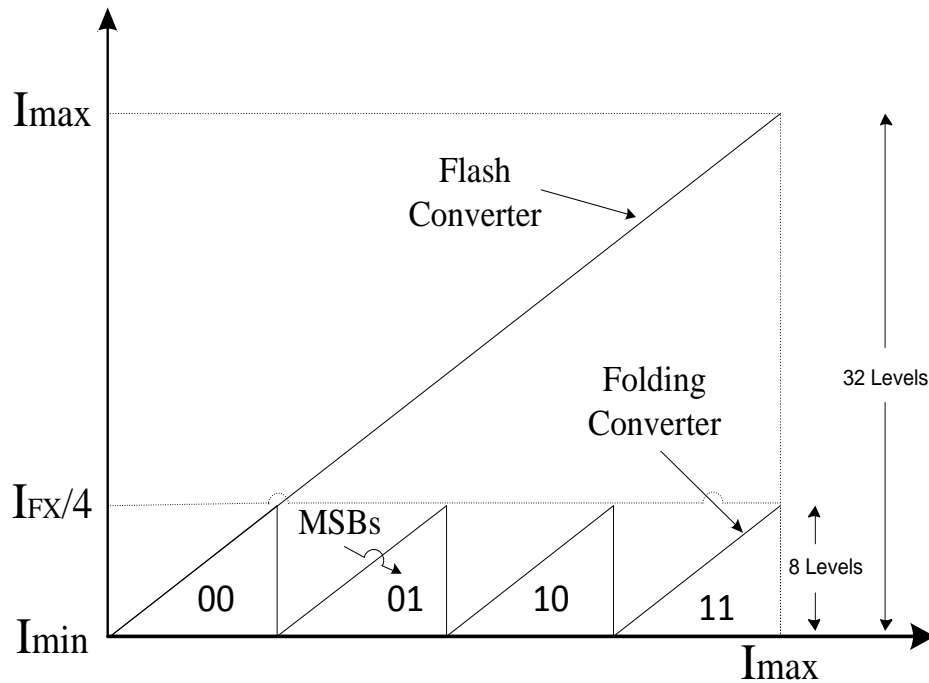


Figure 3-2: Folding characteristics for $b_{MSB}=2$ and $b_{LSB}=3$

As explained before folding reduces the number of comparators required. This will reduce the power consumption and area. For example, a 5 bit flash ADC utilizes 31 comparators and by employing folding circuit with 4 folding factor saw-tooth output, the number of comparators of 3 bit fine ADC and 2 bit coarse ADC can be reduced from 31 to 10.

There are three different approaches in folding. The transfer characteristics of the three different types of folding circuit are shown in Figure 3-3. The output of folding amplifier could be saw-tooth, triangular or sinusoidal based on the architecture. Several implementations have been reported. Some approaches are based on the differential pair which produce approximately a sinusoidal wave [28], [29], and some others are based on current mirrors which produce approximately a triangular wave [38]. Both sinusoidal and triangular waves will lead to errors in conversion and hence degrade the accuracy of A/D converter.

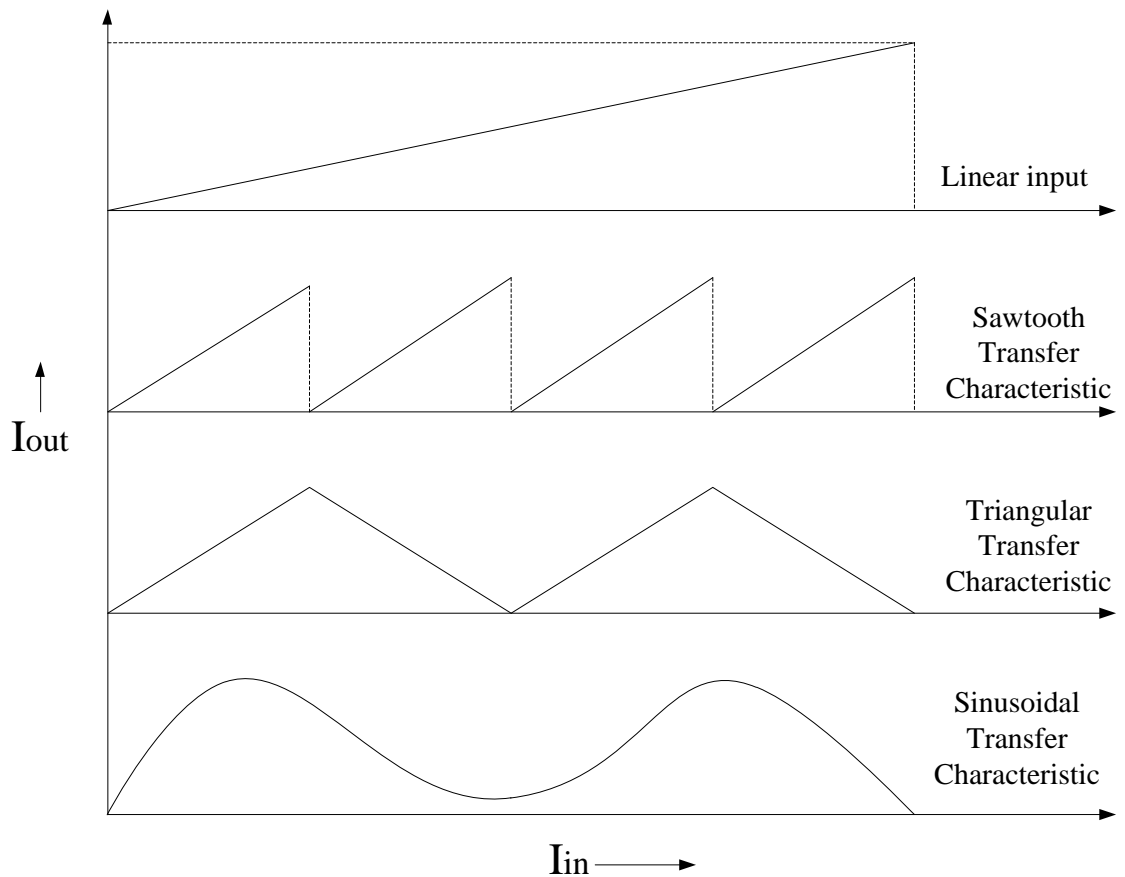


Figure 3-3: Transfer characteristics of the folding circuit.

The folding amplifier concept can be understood by referring to Figure 3-4 and Figure 3-5 in which a triangular and saw-tooth shaped transfer characteristic of folding factor 4 are shown. As an example, for 5-bit ADC, when the input current sweeps through the full scale of ADC, the output is repeated four times. Hence the comparators of folding ADC detect four zero crossings while in flash ADC a comparator detects only one zero crossing. The number of comparators needed for 5-bit folding ADC is 10 (3 for coarse quantizer and 7 for fine quantizer) whereas 31 comparators are needed for 5-bit full-flash ADC.

Folding the input to a triangular wave will lead to errors in the digitized output and compensation is needed. As an example a 5-bit folding ADC and errors produced from the triangular wave folding amplifier is shown in Figure 3-4. It is clear from Figure 3-4 that the digital output, 01010, is the same for the two different analog inputs, 0.36IFS and 0.46IFS. Thus, one digital output represents two analog inputs.

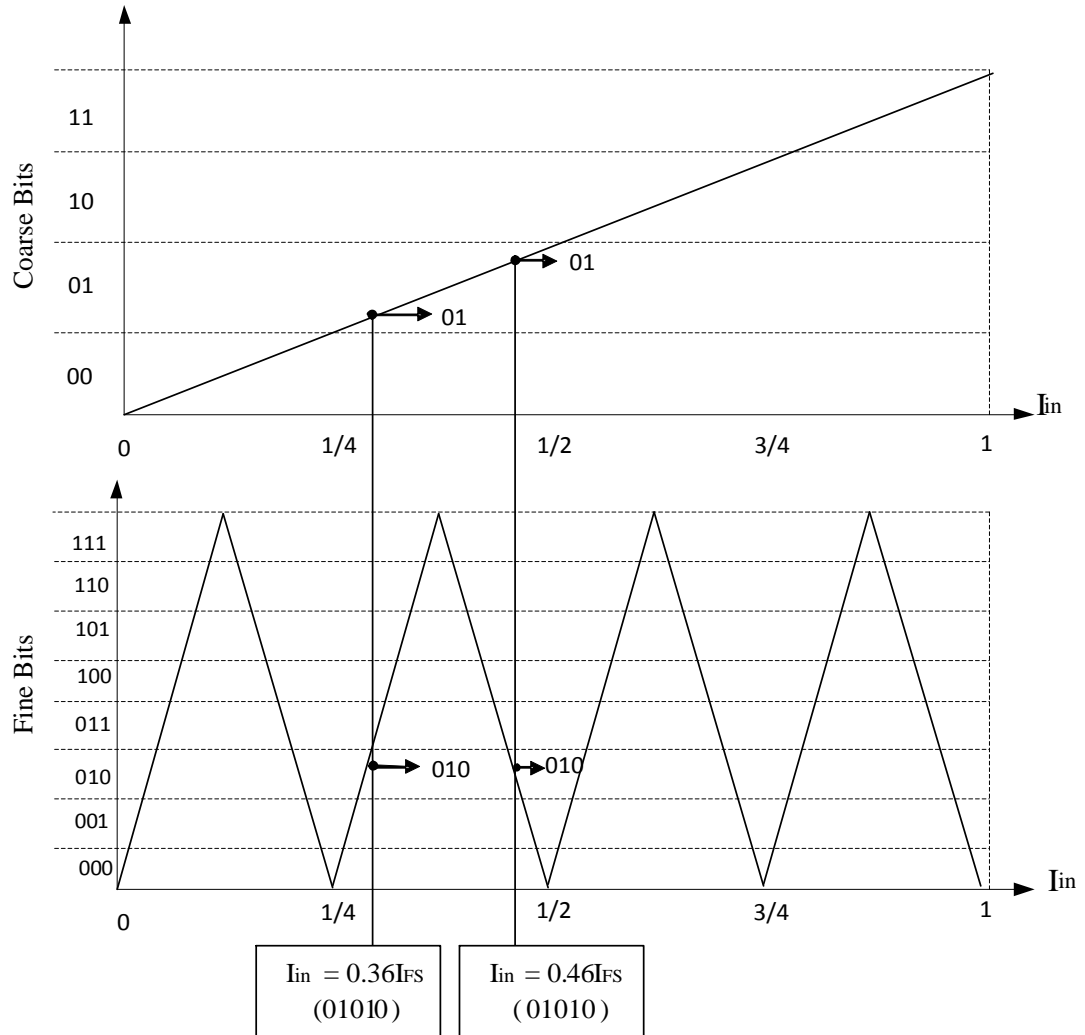


Figure 3-4: A 5-bit folding ADC using triangular wave folding amplifier

It is well known that saw-tooth transfer characteristic is the best in folding because it will eliminate or minimize the digitization error. This is clear from Figure 3-5 where two digital outputs represent two analog inputs.

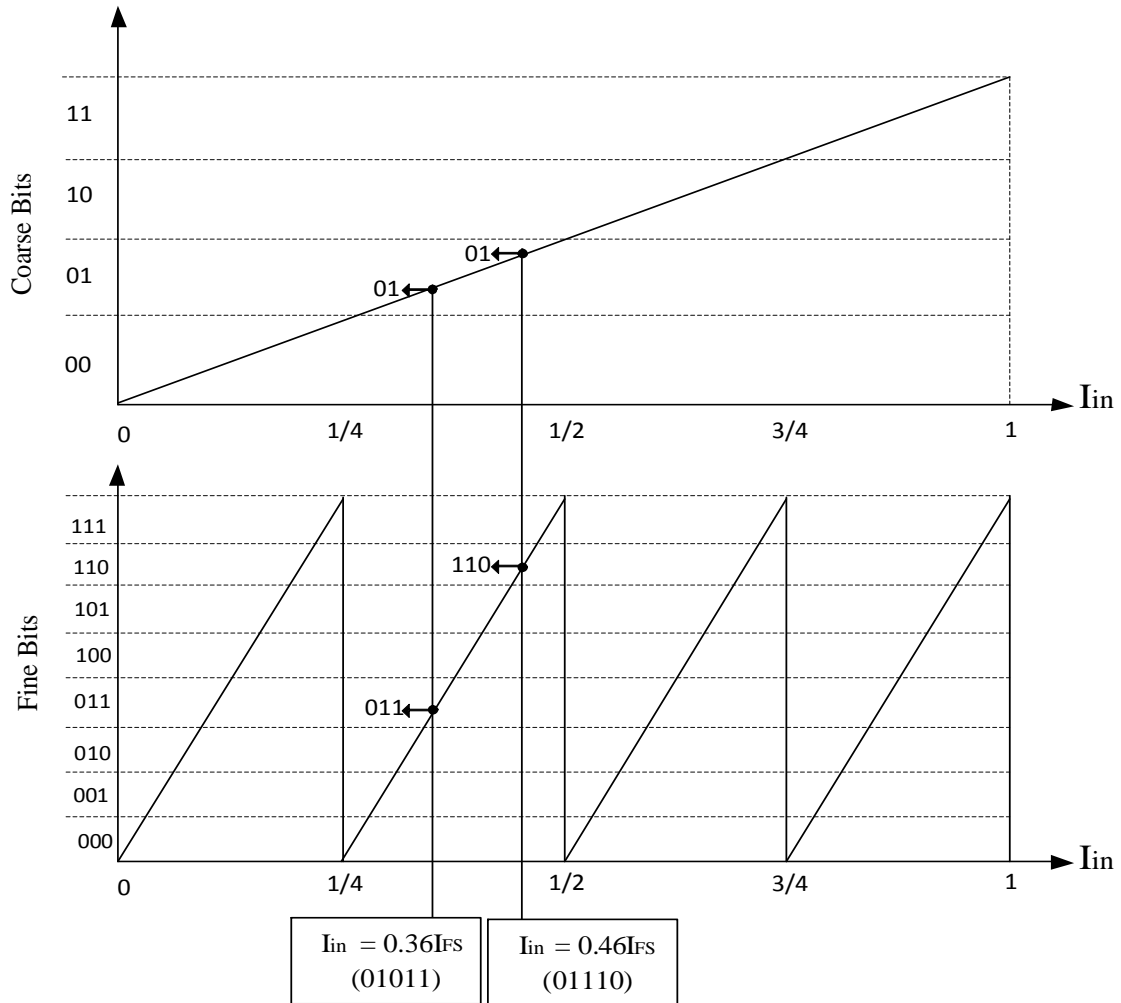


Figure 3-5: A 5-bit folding ADC (saw-tooth wave of folding amplifier)

Recently, some pure linear analog preprocessing voltage-mode folding circuits have been presented to generate saw-tooth signal [48][49]. However, there are no current-mode folding circuits that generate saw-tooth signal in the open literature.

As mentioned before, some implementation of folding amplifier have been developed which approximate the triangle wave in both voltage and current-mode. A few of them

are based on rectifier characteristic of diodes [50], [51] and some others are based on current mirrors [38].

3.2.1 Triangular Folding

Current mirror based folding amplifier is used to generate triangular wave-form as shown in Figure 3-6 by connecting basic folding blocks in cascade and each block is a simple current mirror. The current copier can be implemented using PMOS current mirror, which has one input and multiple outputs [38].

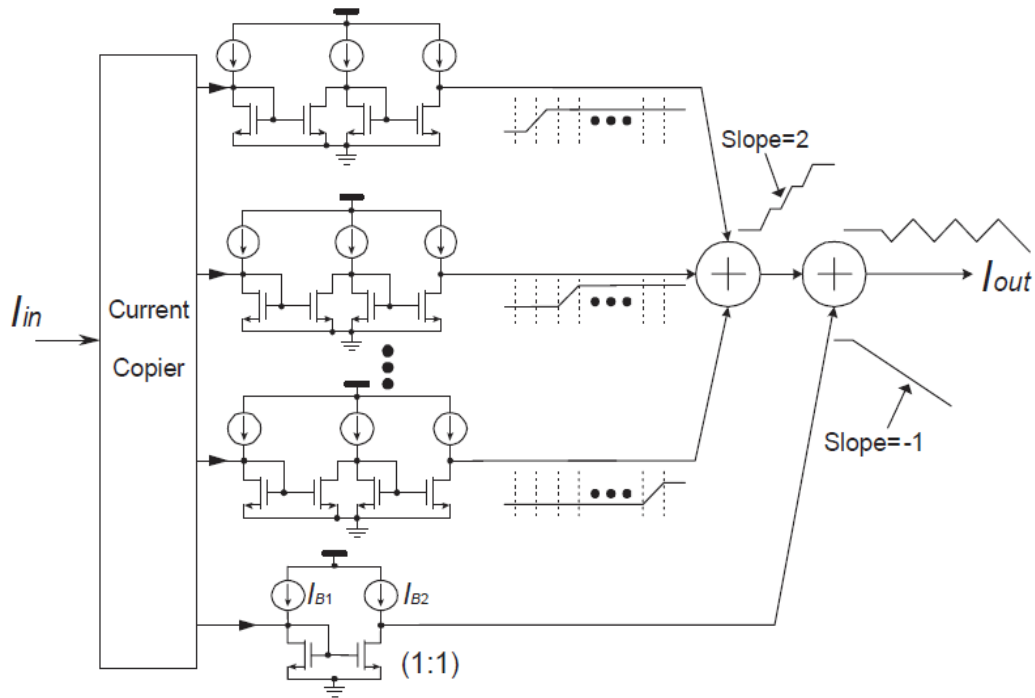


Figure 3-6: Current mirror based current mode folding amplifier [38].

3.3 Sample and Hold (S/H)

Analog switches are a common building block in analog-to digital A/D converters. The function of the S/H circuit is to sample the analog input signal and hold it for a certain amount of time while subsequent circuitry digitizes it. Traditionally, S/H circuits are designed in voltage-mode because most of the physical quantities measured are available in the form of voltage. In S/H circuits, the error in the sample voltage is caused by two charge transport mechanisms. These are called charge injection and clock feed through [52]. In this thesis, the input current is sampled instead of input voltage. S/H circuits are designed in current-mode because the input of the proposed folding ADC is in the form of current. In current-mode, the input current is sampled at discrete times and held constant until the next sampling instant.

The CMOS transmission gate (TG) S/H circuit for the proposed folding A/D converter is shown in Figure 3-2. The benefits of using CMOS TG are that it can pass logic high or logic low without a threshold voltage drop and lower overall conductance [53].

If $\mu_n \left(\frac{W}{L}\right)_n = \mu_p \left(\frac{W}{L}\right)_p$ the conductance is given as:

$$g_{ds,on} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{DD} - V_{th,n} - |V_{th,p}|) \quad (3 - 1)$$

The maximum frequency that the circuit can sample is limited. The 3dB frequency of the circuit is given as:

$$f_{3dB} = \frac{1}{2\pi} \frac{g_{ds,on}}{C_H + C_P} \quad (3 - 2)$$

Where C_H is the sampling output capacitance and C_P the parasitic capacitances associated with the output node.

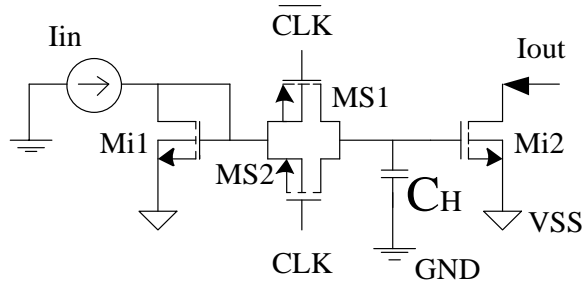


Figure 3-7: CMOS TG S/H circuit

The sampling CLK is given to the control of the TG. When the CLK is high the analog input signal is sampled and the holding capacitor is charged to the input level. When once the CLK goes to low, then the path from the input is open circuited and the sampled current is maintained constant and given to the preceding block for conversion until the CLK goes to high. For a better sampling the sampling rate should be at least 2 times to that of the input signal frequency.

3.4 Current Comparator

Comparator is the heart of A/D converters. In particular, the performance of the flash and folding A/D converters strongly depend on the performance of the comparator used. Figure 3-8 shows the symbol of the comparator. Generally speaking, comparator is the basic building block of folding flash ADC as it determines the speed and accuracy of ADC. From the previous research of current comparator summarized in table II, there are many designs and most of them are modified version of Traff's current-comparator.

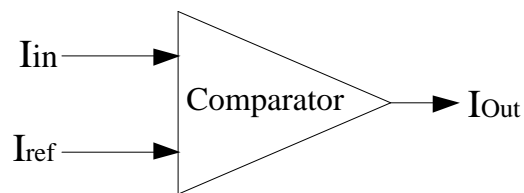


Figure 3-8: Symbol a current comparator

Some of the references reported a comparison table like [54] and [55]. One of the interesting things in those tables is that, Traff design has higher power consumption than most of the other designs although it has less number of components than the other designs. Also it is mentioned that Traff's design can respond to a minimum input current of 500nA with a propagation delay of 10ns whereas other designs respond to smaller input current with lower propagation delay [54],[55]. In this work, a Traff current comparator and the design proposed in [44] are simulated using TANNER with the 0.35 μ m CMOS technology for μ A current input to compare their performance.

The exact circuit of Traff that was simulated is shown in Figure 3-9. Traff current comparator was simulated with a square-wave input current of 10uA amplitude and 1V power supply. The aspect ratio of the transistors was chosen to get the minimum CMOS gate capacitance.

$$\left(\frac{W}{L}\right)_{NMOS} = \left(\frac{W}{L}\right)_{PMOS} = \frac{0.4\mu m}{0.35\mu m}$$

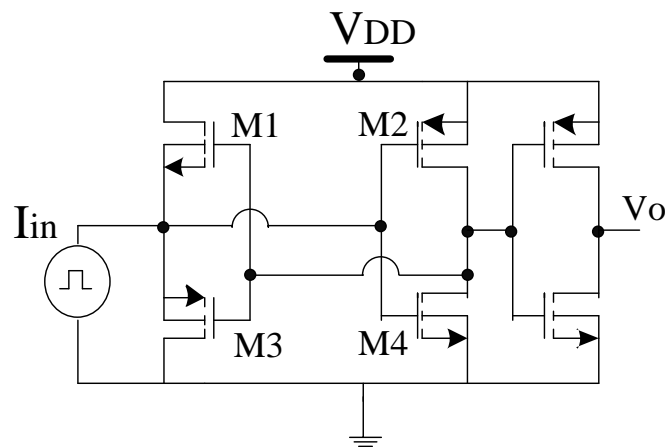
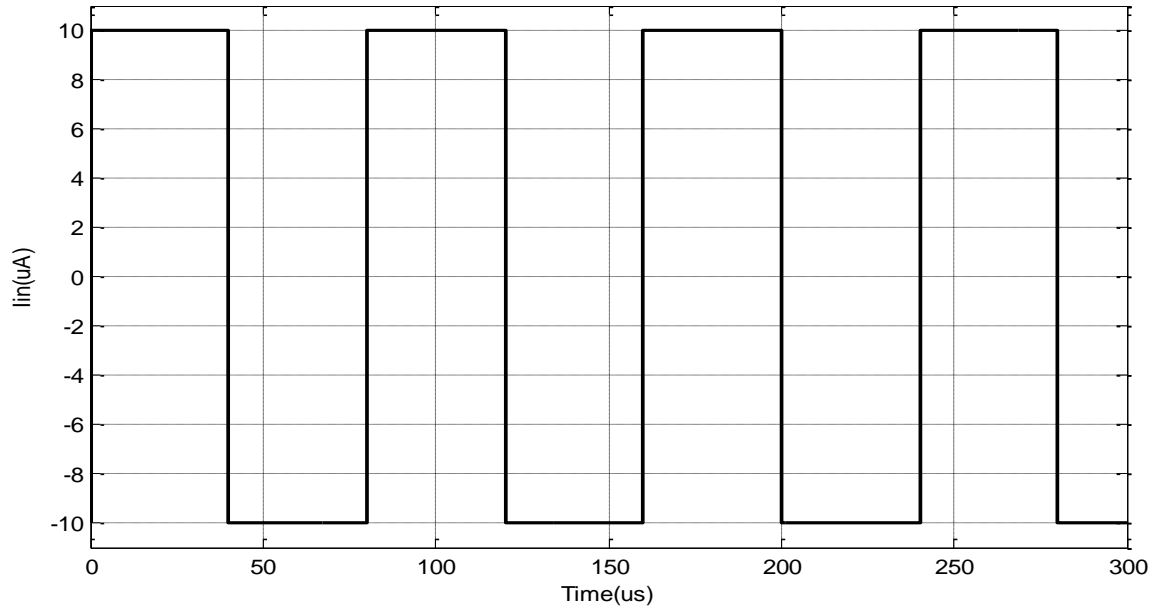
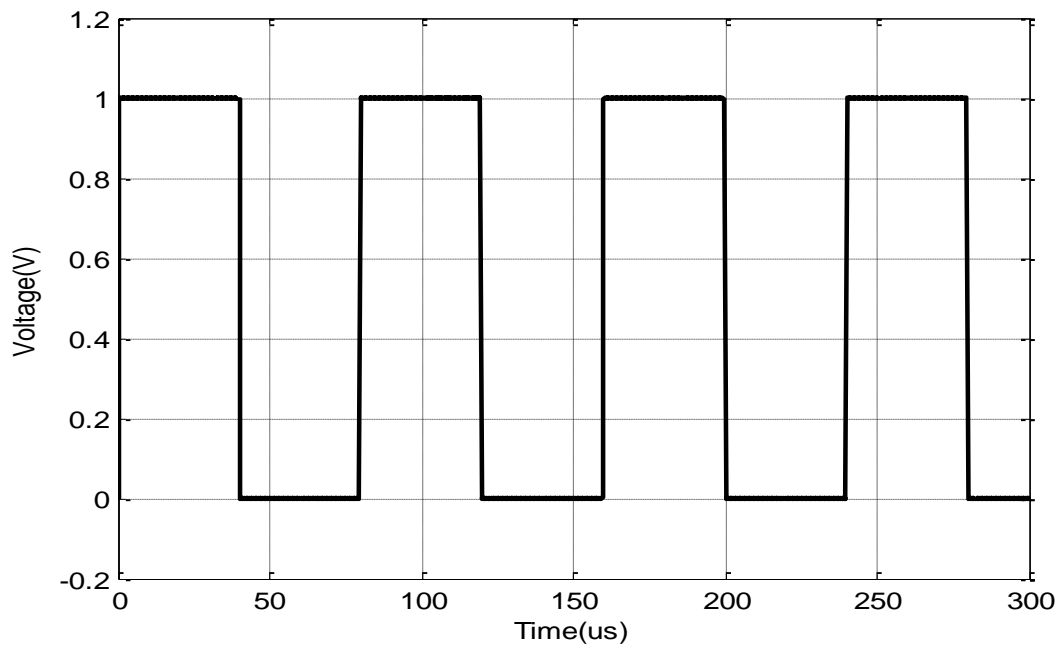


Figure 3-9: Traff current comparator circuit.

The simulation result is shown in Figure 3-10. In other words, no external capacitance in the input stage is added, but the load of the circuit is connected to capacitor of 0.5pf. Simulation results show that there is a very small propagation delay and the power consumption is calculated by summing the power supplied by the DC voltage source and the AC current source and found to be 1.6μW.



(a) Input current



(b) Output voltage

Figure 3-10: Simulation results of traff's circuit

To be fair, the current comparator circuit proposed by Tang [44] as shown in Figure 3-11 was simulated using the same simulation tools, conditions, CMOS models, and the same dimensions as the ones used in Traff. Traff approach was modified by adding two CMOS inverters (A2 and A3) to the feedback with a shunt loop of a resistor and capacitor which compensates frequency response and adding two inverters to the output stage to achieve rail-to-rail output voltage. Figure 3-12 shows the results.

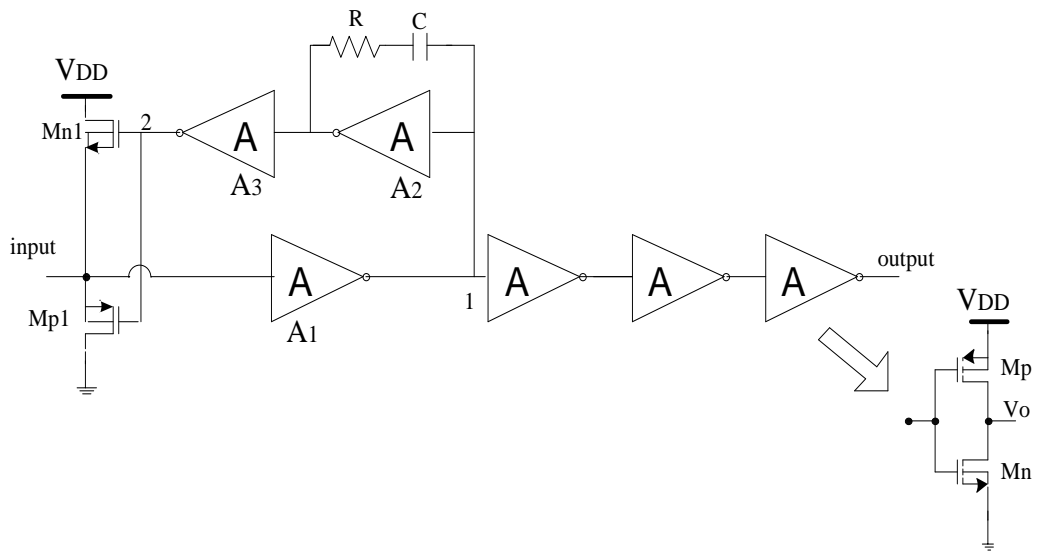
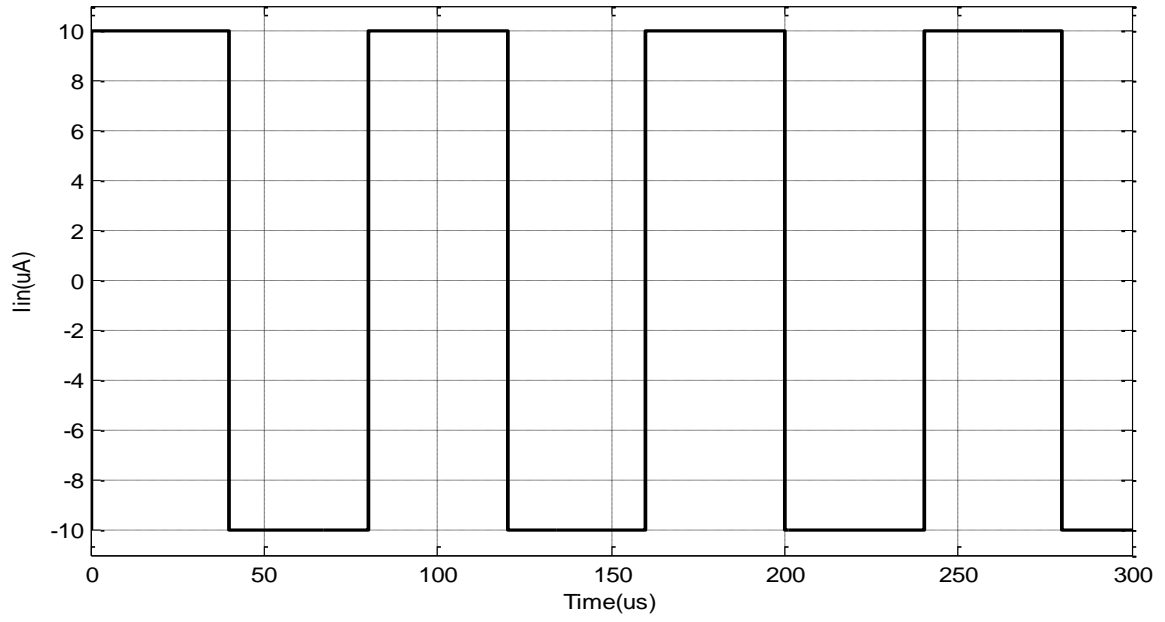
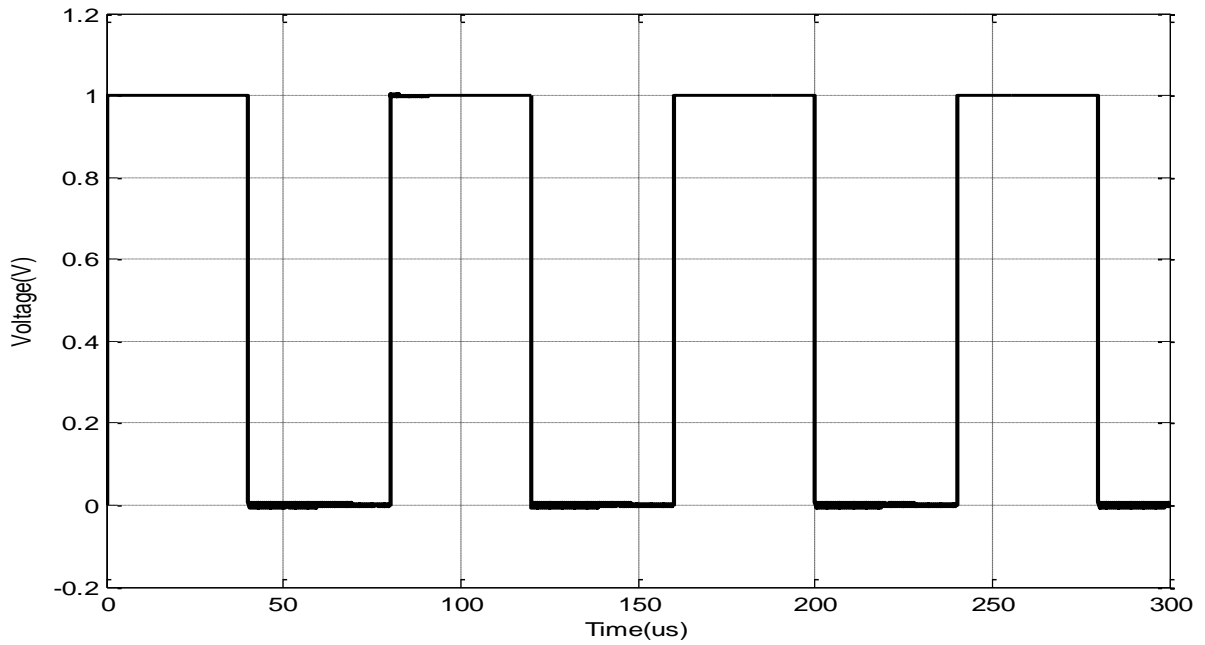


Figure 3-11: Schematic diagram of current comparator proposed by [44].



(a) Input current



(a) Output voltage

Figure 3-12: Simulation results of proposed circuit by [44]

Table III summarizes the comparison between the current comparator designed by Traff and the one reported in [44] using the same power supply and the same aspect ratio.

Table III: Comparison between Traff and tang [44] under the same simulation conditions

Reference	Traff [40]	Tang [44]
Transistors aspect ratio	$\left(\frac{W}{L}\right)_{NMOS} = \left(\frac{W}{L}\right)_{PMOS} = \frac{0.4\mu m}{0.35\mu m}$	
Technology (μm)	0.35	0.35
Power supply (V)	1	1
Input current amplitude(μA)	10	10
Propagation delay (μs)	0.0365	0.0375
Power consumption (μW)	11.6	158.3

In brief, the current comparator proposed in [44] consumes higher power and a little higher propagation delay compared to the Traff, because of its complexity. Thus, the current comparator designed by Traff will be suitable for our design and it will increase the accuracy of the folding ADC with low power dissipation.

3.5 Digital Encoder

Encoder is an important digital circuit in high-speed ADC. As it is well known, thermometer code (TC) is generated by analog comparator array outputs, and then converted to binary code (BC) in flash A/D converter designs as shown in the Figure 3-13. Due to the current-mode folding flash ADC, the output code comparator is thermometer code which is a combination of a series of zeros and a series of ones, example: 000,001,011,111. Because binary code is usually needed in digital signal processing, $(2^N - 1)$ -to-(N) encoder is used to generate a binary code from thermometer code (TC), where N is the number of bits of ADCs. Digital encoder can be designed using common logic gate, ROM or PLA. The complexity of the encoder increases as the number of bits increases, which results in high power dissipation and large chip area.

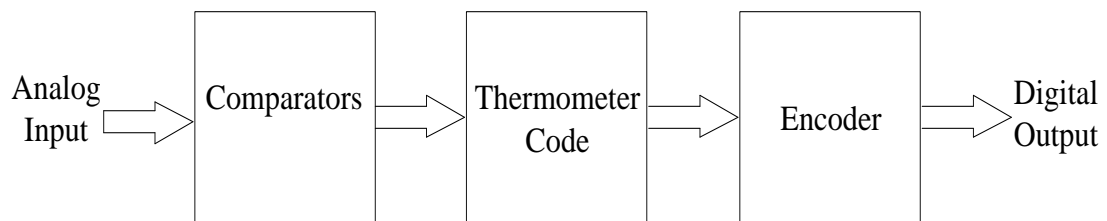


Figure 3-13: Block diagram of Flash ADC

NAND, NOT logic gates will be used to design encoder which are similar to PLA design. In this design only selected input combinations are used to derive an output bit, whereas

in PLA design all the inputs are combined to generate an output bit. Thermometer code is converted to binary code without any intermediate conversion which is the main feature of this encoder.

In this thesis it is required to design 5-bits current-mode folding ADC. The two MSB are produced from the coarse flash ADC and three LSB from the fine flash ADC. This implies two encoders are required one is 3-to-2 encoder and the second one is 7-to-3 encoder.

3.5.1 3-to-2 encoder

The main block for our encoder in the coarse flash ADC to generate 2-bit MSB is shown in Figure 3-14.

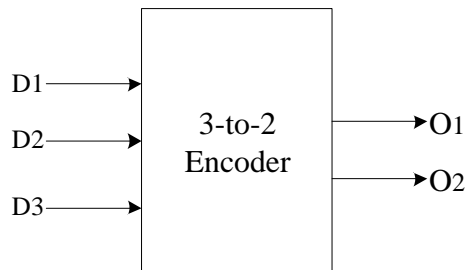


Figure 3-14: Block diagram of 3-to-2 encoder

Table IV shows the thermometer code and binary code. This table can be used to design a suitable combinational circuit to derive the logical binary expressions for a 3-to-2 bit encoder to get the component equations in equation (3-3).

Table IV: Thermometer to Binary (3x2) encoder truth table

Thermometer code			Binary Code
D3	D2	D1	O1O2
0	0	0	00
0	0	1	01
0	1	1	10
1	1	1	11

$$\left. \begin{aligned} O_1 &= D_2 \\ O_2 &= D_3 + D_1 D_2' \end{aligned} \right\} \quad (3-3)$$

Using equations (3-3), the design of 3x2 encoder converts 3-bit thermometer code to 2-bit binary code is shown in Figure 3-15.

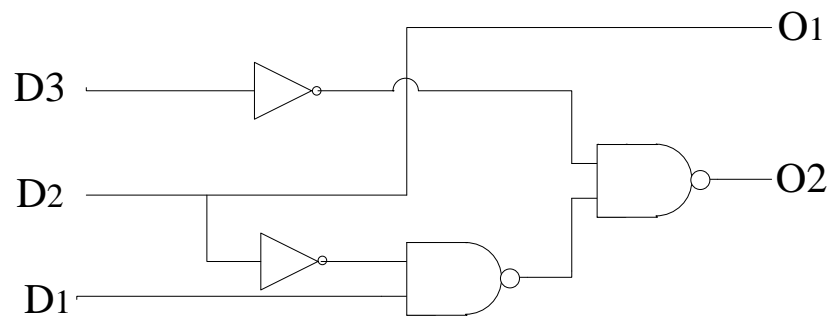


Figure 3-15: Logic circuit of 3x2 encoder

3.5.2 7-to-3 encoder

The block diagram for our encoder in fine flash ADC to generate 3-bit LSB is shown in Figure 3-16. The function of this encoder is to convert the output of the comparators which are 7 thermometer codes to 3 binary codes.

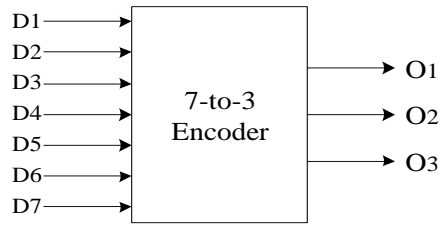


Figure 3-16: Block diagram of 7-to-3 encoder

Table V: Thermometer to Binary (7x3) encoder truth table

Thermometer code							Binary Code
D7	D6	D5	D4	D3	D2	D1	O1 O2 O3
0	0	0	0	0	0	0	0 0 0
0	0	0	0	0	0	1	0 0 1
0	0	0	0	0	1	1	0 1 0
0	0	0	0	1	1	1	0 1 1
0	0	0	1	1	1	1	1 0 0
0	0	1	1	1	1	1	1 0 1
0	1	1	1	1	1	1	1 1 0
1	1	1	1	1	1	1	1 1 1

From the truth Table V, The functions O_3 , O_2 and O_1 are given in equation (3-4) are used to design 7-to-3 bit encoder.

$$O_1 = D_4$$

$$O_2 = D_6 + D_4'D_3 + D_3'D_2 \quad (3-4)$$

$$O_3 = D_7 D_6 + D_6'D_5 + D_4'D_3 + D_2'D_1$$

The complete circuit diagram for the 7-3 encoder is shown in Figure 3-17.

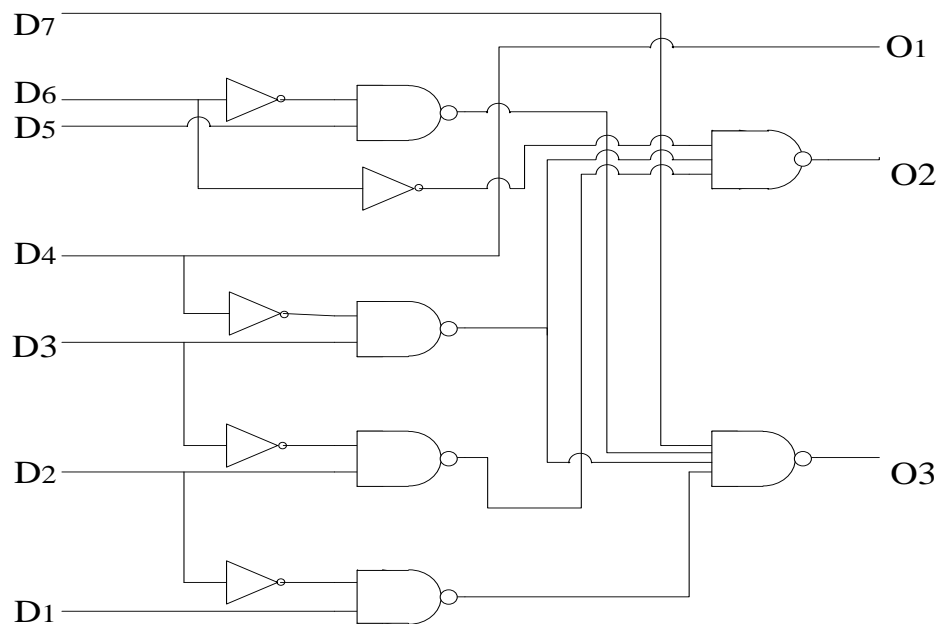


Figure 3-17: Logic circuit of 7x3 encoder

In brief, this type of digital encoder is called a priority encoder. The function of the priority encoder is such that if multiple inputs are active at the same time, the input

having the highest priority will take precedence. The digital encoder using CMOS logic is described in [56]. The design will optimize both silicon area and power consumption.

CHAPTER 4

DESIGN AND SIMULATION RESULTS

4.1 Introduction

In this chapter, a 5 bit folding ADC is designed and simulated using Tanner simulation tools in 0.35 μ m CMOS technology. It consists two of independent modules, namely fine flash ADC and coarse flash ADC to produce three bits and two bits respectively. The fine flash ADC contains a current-mode folding amplifier and current comparator, whereas the coarse ADC is flash ADC.

It must be mentioned that the techniques that would be adopted to achieve high accuracy must preserve the linearity of the folding ADC approach and maintaining low power. A design criteria to be satisfied by each building block to achieve high performance.

A detailed description of individual modules along with the simulation results are provided in the following section.

4.2 Proposed Current-Mode Folding ADC

The block diagram of the designed 5 bit current-mode folding ADC is shown in Figure 4-1. It consists of fine flash ADC and coarse flash ADC. A folding flash ADC consists of analog

preprocessing circuit in the form of folding amplifier, comparators and digital encoder. A folding circuit with folding factor of four is used as the building block of the fine ADC. Coarse flash ADC is typical flash ADC.

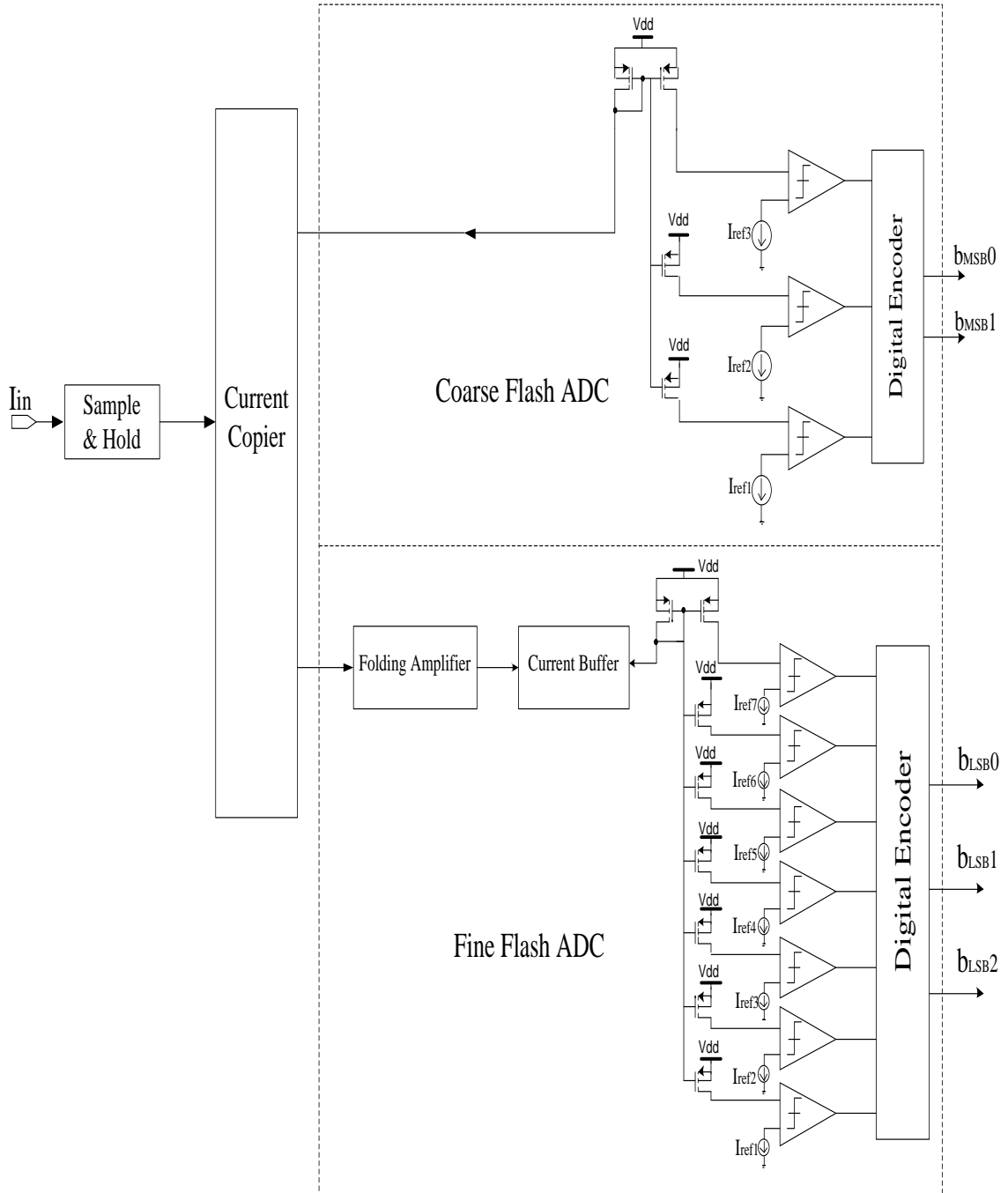


Figure 4-1: Circuit diagram of 5-bit folding ADC

4.2.1 Proposed Current-Mode Folding ADC

Current-mode folding amplifier has been developed to generate saw-tooth-shaped input-output characteristic. Figure 4-2 shows the concept used to develop the proposed folding amplifier. It consists of two blocks each block produces the shape of the signal and the two signals are summed together to produce the required saw-tooth signal.

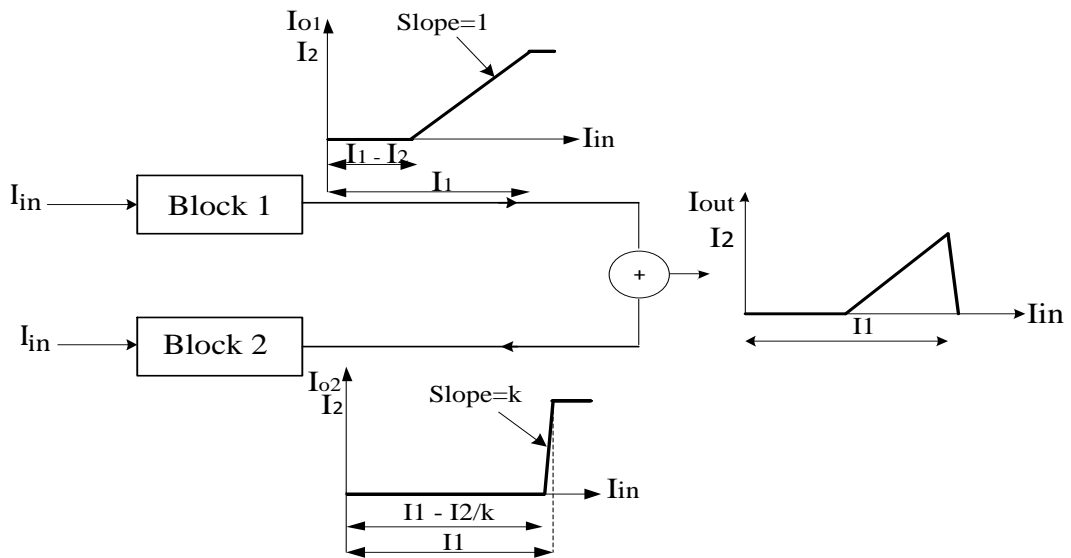
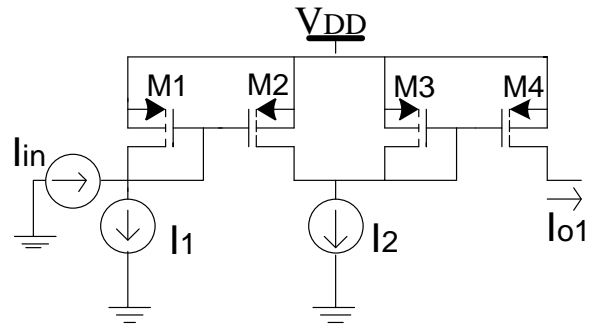
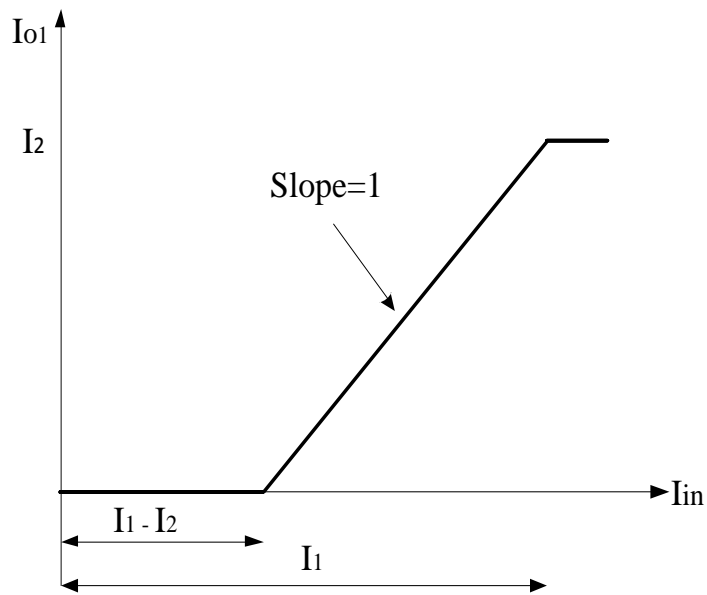


Figure 4-2: The concept used in developing the proposed folding amplifier

A possible realization for block 1 of Figure 4-2 is shown in Figure 4-3a. It consists of two current mirrors connected in cascade. The circuit is designed so that for small input current, the output is zero, while for large currents the output current is constant and equal to the bias current $\propto I_2$ where I_2 is the bias current and \propto is the aspect ratio of transistors M1 and M2. The output current is a function of the input current for the block1 as shown in Figure 4-3b.



(a) Circuit diagram



(b) Transfer curve

Figure 4-3: Circuit diagram of block 1 and its transfer curve

With reference to Figure 4-3a,

$$I_{D1} + I_{in} = I_1 \text{ or } I_{D1} = I_1 - I_{in} \quad (4-1)$$

$$I_{D2} + I_{D3} = I_2 \text{ or } I_{D3} = I_2 - I_{D2} \quad (4-2)$$

And

$$I_{D2} = I_{D1} \frac{\alpha_2}{\alpha_1} \quad (4-3)$$

Substitute equation (4-1) in equation (4-3) to get:

$$I_{D2} = (I_1 - I_{in}) \frac{\alpha_2}{\alpha_1} \quad (4-4)$$

Substitute equation (4-4) in equation (4-2) to get:

$$I_{D3} = I_2 - I_1 \frac{\alpha_2}{\alpha_1} + I_{in} \frac{\alpha_2}{\alpha_1} \quad (4-5)$$

$$I_{O1} = I_{D4} = I_{D3} \frac{\alpha_4}{\alpha_3} \quad (4-6)$$

Combining equations (4-5) and (4-6), the output current is given by:

$$I_{O1} = I_2 \frac{\alpha_4}{\alpha_3} - I_1 \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3} + I_{in} \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3} \quad (4-7)$$

Where, $\alpha_i = \frac{W_i}{L_i}$ is the aspect ratio of transistor M_i .

If $\alpha_1 = \alpha_2$, and $\alpha_3 = \alpha_4$ then:

$$I_{O1} = I_2 - I_1 + I_{in} \quad (4-8)$$

If $I_{in} \geq I_1$, then M1 and M2 will be OFF as indicated in equation (4-1), and hence:

$$I_{O1} = I_2$$

If $I_{in} \leq I_1 - I_2$:

case 1. $I_{in} = I_1 - I_2$, then equation (4-8) can be written as:

$$I_{o1} = I_2 - I_1 + I_1 - I_2$$

$$I_{o1} = 0$$

case 2. $I_{in} < I_1 - I_2$, with $I_1 > I_2$,

If $I_1 = I_2$, then $I_{in} = 0$, and

$$I_{o1} = 0$$

If $I_1 > I_2$, then:

$I_{in} < I_1 - I_2 = \beta(I_1 - I_2)$, with $\beta < 1$, *then*

$$I_{o1} = I_2 - I_1 + \beta(I_1 - I_2)$$

$$I_{o1} = I_2(1 - \beta) + I_1(\beta - 1)$$

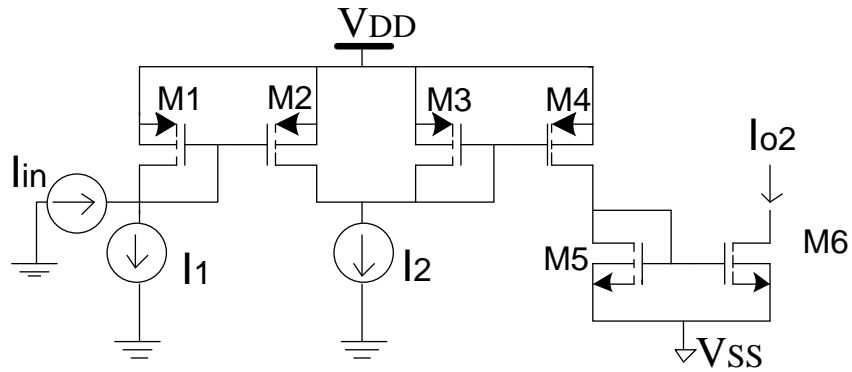
With with $I_2 < I_1$, then I_{o1} will be negative and this is impossible. Thus I_{o1} is forced to be equal to 0.

$$I_{o1} = 0$$

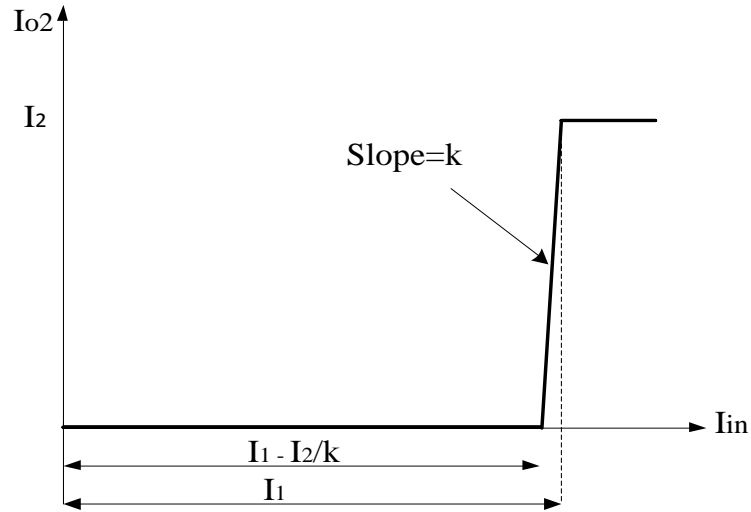
In summary:

$$I_{o1} = \begin{cases} I_2 & \text{if } I_{in} \geq I_1 \\ 0 & \text{if } I_{in} \leq I_1 - I_2 \end{cases} \quad (4-9)$$

A possible realization for block 2 of Figure 4-2, with an inverted output, is shown in Figure 4-4a. The input-output characteristic of the circuit in Figure 4-4a is shown in Figure 4-4b.



(a) Circuit diagram



(a) Transfer curve

Figure 4-4: Circuit diagram of block 2 and its transfer curve

$$I_{o2} = I_2 \frac{\alpha_4}{\alpha_3} - I_1 \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3} + I_{in} \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3} \quad (4-10)$$

If $\alpha_3 = \alpha_4$ then:

$$I_{o2} = I_2 - I_1 \frac{\alpha_2}{\alpha_1} + I_{in} \frac{\alpha_2}{\alpha_1} \quad (4-11)$$

$$I_{o2} = I_2 - k(I_1 - I_{in}) \quad (4-12)$$

Where $k = \alpha_2 / \alpha_1$

With reference to Figure 4-4a If $I_{in} \geq I_1$, then M1 and M2 will be OFF and the current I_2 will be forced through M3 giving:

$$I_{o2} = I_2$$

Now, if $I_{in} = I_1 - \frac{I_2}{k}$ equation (4-12) can be written as:

$$I_{o2} = I_2 - I_1k + k\left(I_1 - \frac{I_2}{k}\right) = 0 \quad (4-13)$$

If $I_{in} < I_1 - \frac{I_2}{k} = \beta\left(I_1 - \frac{I_2}{k}\right)$, with $\beta < 1$, then

$$I_{o2} = I_2 - k\left(I_1 - \beta\left(I_1 - \frac{I_2}{k}\right)\right) \quad (4-14)$$

$$I_{o2} = (1 - \beta)(I_2 - kI_1) \quad (4-15)$$

With $I_2 < I_1$ and $k > 1$, then I_{o2} will be negative and this is impossible. Thus I_{o2} is forced to be equal to 0.

This can be summarized as follows:

$$I_{o2} = \begin{cases} I_2 & \text{if } I_{in} \geq I_1 \\ 0 & \text{if } I_{in} \leq I_1 - \frac{I_2}{k} \end{cases} \quad (4-16)$$

The output current of Figure 4-2 will be the sum of the two currents, that is

$$I_{out} = I_{o1} - I_{o2} \quad (4-17)$$

Inspection of equations (4-9), (4-16) and (4-17) shows that the input-output characteristic of Figure 4-2 can be obtained by proper selection of the biasing currents I_1 and I_2 .

In the previous analysis it was assumed that $\alpha_1=\alpha_2$, and $\alpha_3=\alpha_4$. This resulted in a slope =1 for the characteristic of Figure 4-2. However, in general, using equations (4-7) and (4-10), the slope of the transfer characteristic for blocks 1 and 2 of Figure 4-2 is given by:

$$S = \frac{\alpha_2 \alpha_4}{\alpha_1 \alpha_3}$$

It is worth mentioning here that the slope S can be controlled by the aspect ratios of transistors M1-M4.

The complete circuit diagram of the proposed current mode folding amplifier with a folding factor of 4 is shown in Figure 4-5 with all MOSFETS substrates connected to the respected sources.

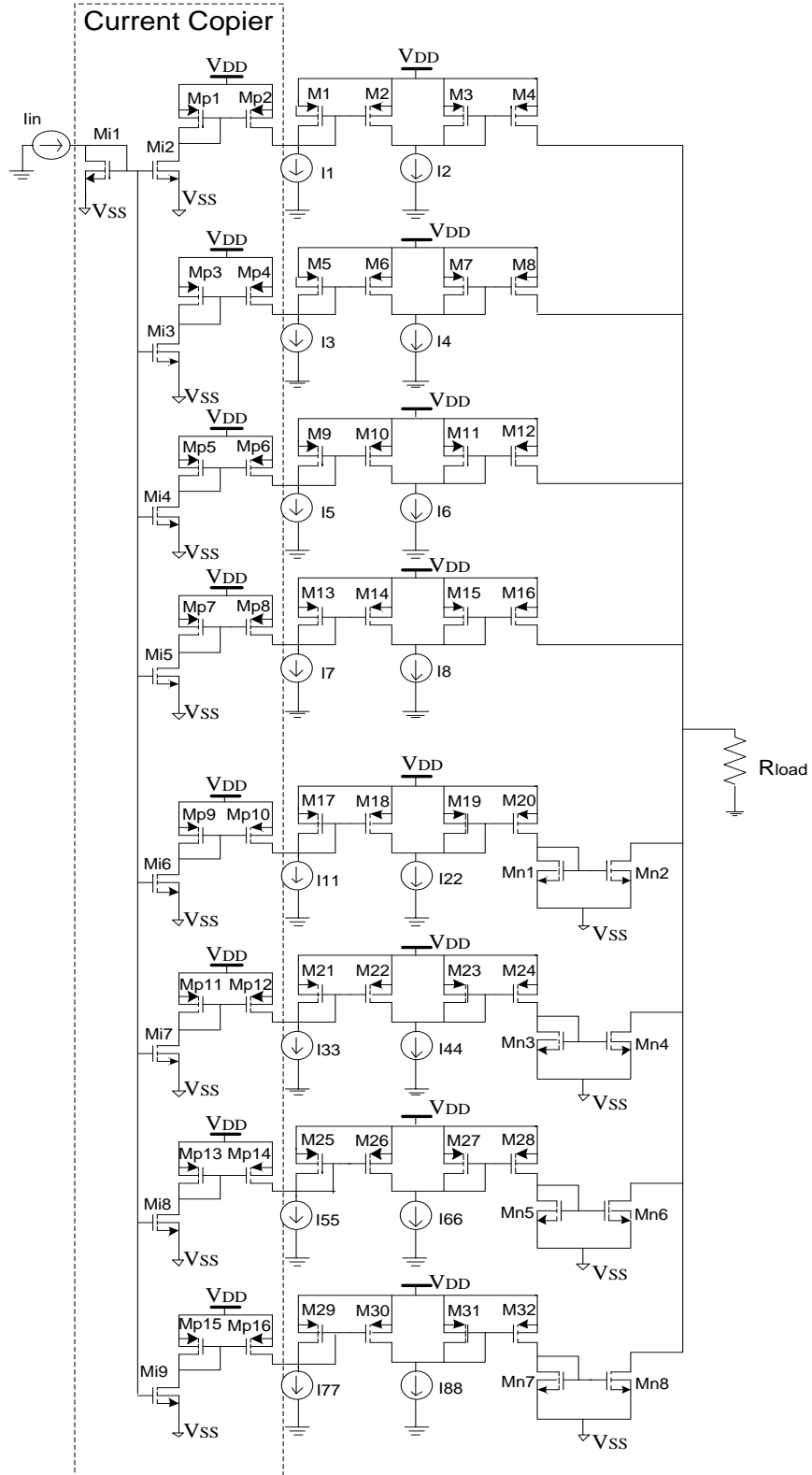


Figure 4-5: Current-mode folding amplifier with a folding factor of 4

The proposed circuit of Figure 4-5 was simulated using Tanner simulation tools in 0.35 μm CMOS process technology with DC supply voltage $V_{DD}=-V_{SS}=1\text{V}$ and bias currents as follows $I_1 = I_{11} = I_2 = I_{22} = I_4 = I_{44} = I_6 = I_{66} = I_8 = I_{88} = 8\mu\text{A}$, $I_7 = I_{77} = 4I_1$, $I_5 = I_{55} = 3I_1$, and $I_3 = I_{33} = 2I_1$.

The output current was measured by forcing it through a grounded resistive load of 1k Ω .

All transistors aspect ratios are given in Table VI.

Table VI: Transistor aspect ratios of the proposed current-mode folding amplifier

Transistor	W/L (μm)	Transistor	W/L (μm)
M1,M2,M3,M4	10 / 2	M17,M21,M25,M29	0.5 / 2
M5,M6,M7,M8		M18,M22,M26,M30	50 / 2
M9,M10,M11,M12		M19,M20,M23,M24	4/2
M13,M14,M15,M16		M27,M28,M31,M32	
Mi1-Mi9		Mn1,Mn2,Mn3,Mn4	2.4 / 2
Mp1-Mp16	20/4	Mn5,Mn6,Mn7,Mn8	

DC simulation results

The DC simulation result of the proposed current-mode folding amplifier is shown in Figure 4-6. The input current was varied from 0 to 32 μA . The input analog signal is "folded" into 4 folds (4- times folding) as shown in Figure 4-6.

It is evident from Figure 4-6 that the simulated result is close to the ideal saw-tooth shape which confirms the functionality of the developed design. The output of the folding circuit (folding signal) is folded 4 times for 8 levels corresponding to full scale current/4. In this thesis the three least significant bits (LSB's) generated from fine ADC and the two most significant bits (MSB's) generated from coarse ADC.

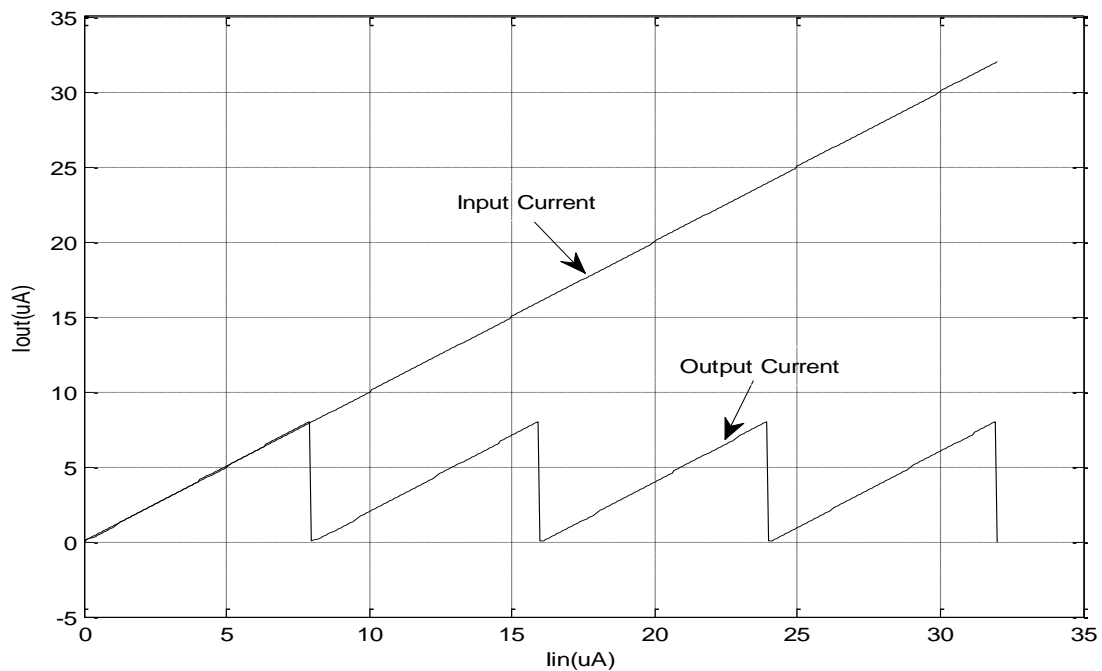
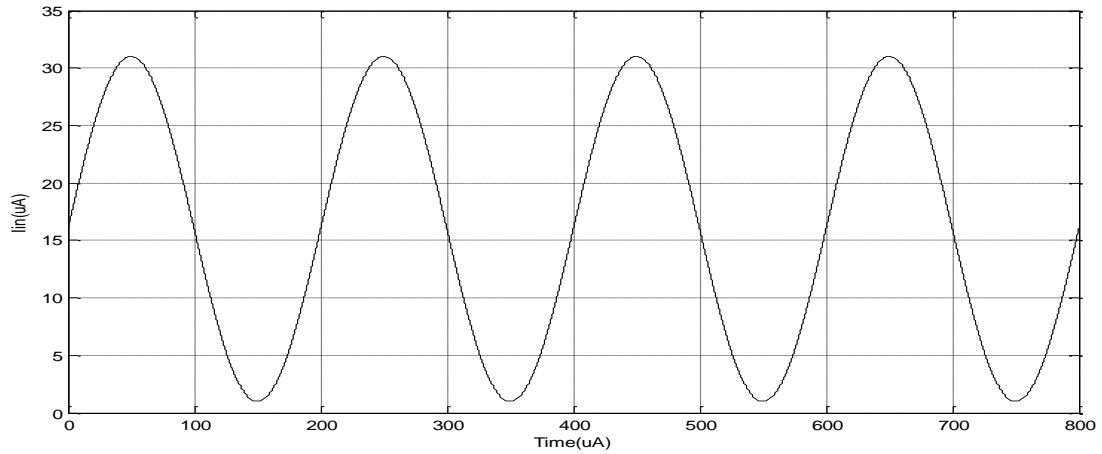


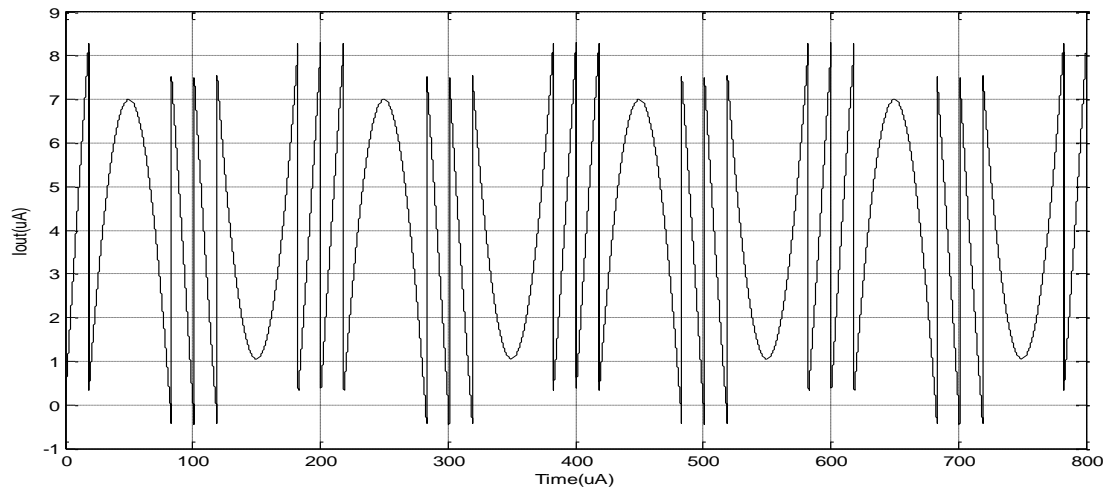
Figure 4-6 : Input and output characteristics of current-mode amplifier

Transient simulation results

The circuit was simulated for transient analysis. The input is a sine wave signal as shown in Figure 4-7a. It is evident from Figure 4-7b that simulation result confirms the functionality of the circuit.



(a) Input signal



(b) Folded output signal

Figure 4-7: Transient response of current-mode folding amplifier

Mismatch Analysis

Since the design is based on current mirrors, the accuracy of the folding amplifier will be affected by the mirror performance. Consequently, it is important to study the effect of mismatch in device dimension that may result during fabrication process [4]. With

reference to the core circuits in Figure 4-3a and Figure 4-4a assuming a mismatch in the threshold voltages between M1 and M2 such that:

If α_p is the average of α_{p1} and α_{p2} , and $\Delta\alpha_p$ is the mismatch.

Where, α_{p1} and α_{p2} are the aspect ratio of transistors M1 and M2 forming the mirror respectively and assuming all other parameters are matched, the mirrored current in M2 is given by:

$$I_{M2} = I_{M1} \left(1 + \frac{\Delta\alpha_p}{\alpha_p} \right) \quad (4-18)$$

Similarly, If α_n is the average of α_{p3} and α_{p4} , and $\Delta\alpha_n$ is the mismatch.

Where α_{p3} and α_{p4} are the aspect ratio of transistors M3 and M4, the mirrored current in M4 is given by:

$$I_{M4} = I_{M3} \left(1 + \frac{\Delta\alpha_n}{\alpha_n} \right) \quad (4-19)$$

It is obvious from equation (4-18) that reducing the effect of mismatch can be achieved by increasing the transistor aspect ratio α_p . Using equations (4-18) and (4-19), equation (4-7) can be written as:

$$I_{o1} = I_2 \left(1 + \frac{\Delta\alpha_n}{\alpha_n} \right) - I_1 \left(1 + \frac{\Delta\alpha_p}{\alpha_p} \right) \left(1 + \frac{\Delta\alpha_n}{\alpha_n} \right) + I_{in} \left(1 + \frac{\Delta\alpha_p}{\alpha_p} \right) \left(1 + \frac{\Delta\alpha_n}{\alpha_n} \right) \quad (4-20)$$

Similarly the current I_{o2} can be written as

$$I_{o2} = I_2 \left(1 + \frac{\Delta\alpha_n}{\alpha_n}\right) - I_1 \left(1 + \frac{\Delta\alpha_p}{\alpha_p}\right) \left(1 + \frac{\Delta\alpha_n}{\alpha_n}\right) + I_{in} \left(1 + \frac{\Delta\alpha_p}{\alpha_p}\right) \left(1 + \frac{\Delta\alpha_n}{\alpha_n}\right) \quad (4-21)$$

Equations (4-20) and (4-21) can be written as:

$$I_{o1} = I_2 K_1 - I_1 K_1 * K_2 + I_{in} K_1 * K_2 \quad (4-22)$$

$$I_{o2} = I_2 K_1 - I_1 K_1 * K_2 + I_{in} K_1 * K_2 \quad (4-23)$$

It is clear from equations (4-22) and (4-23) the currents I_1 and I_{in} will have the same coefficient and these mean equations (4-9) and (4-16) are valid even if there is a mismatch in aspects ratio.

Mont Carlo analysis was carried out with the variance was set to 0.03. Simulation result is shown in Figure 4-8 for 30 times iterations. It is clearly shown that the maximum variation is $0.7\mu\text{A}$ which is acceptable in terms of a 5-bit ADC where the LSB is around $1\mu\text{A}$.

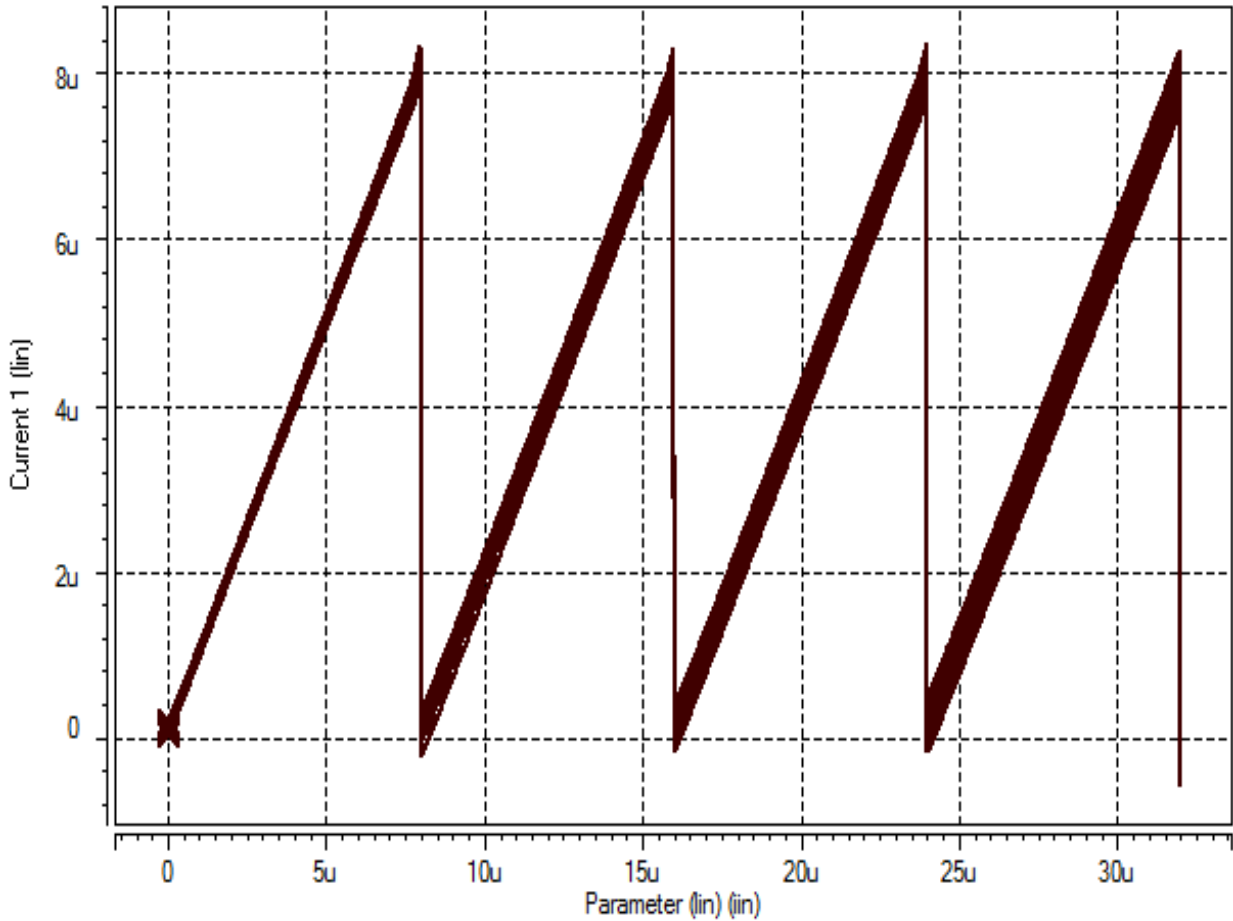


Figure 4-8: Effect of process variations (W/L) on the DC characteristic

Also Mont Carlo analysis was carried out to test the mismatch in the practical biasing current sources with the variance was set to 0.02. Simulation result is shown in Figure 4-9 for 30 times iterations. It is clearly shown that the maximum variation is $0.9\mu\text{A}$ which is acceptable in terms of a 5-bit ADC where the LSB is around $1\mu\text{A}$.

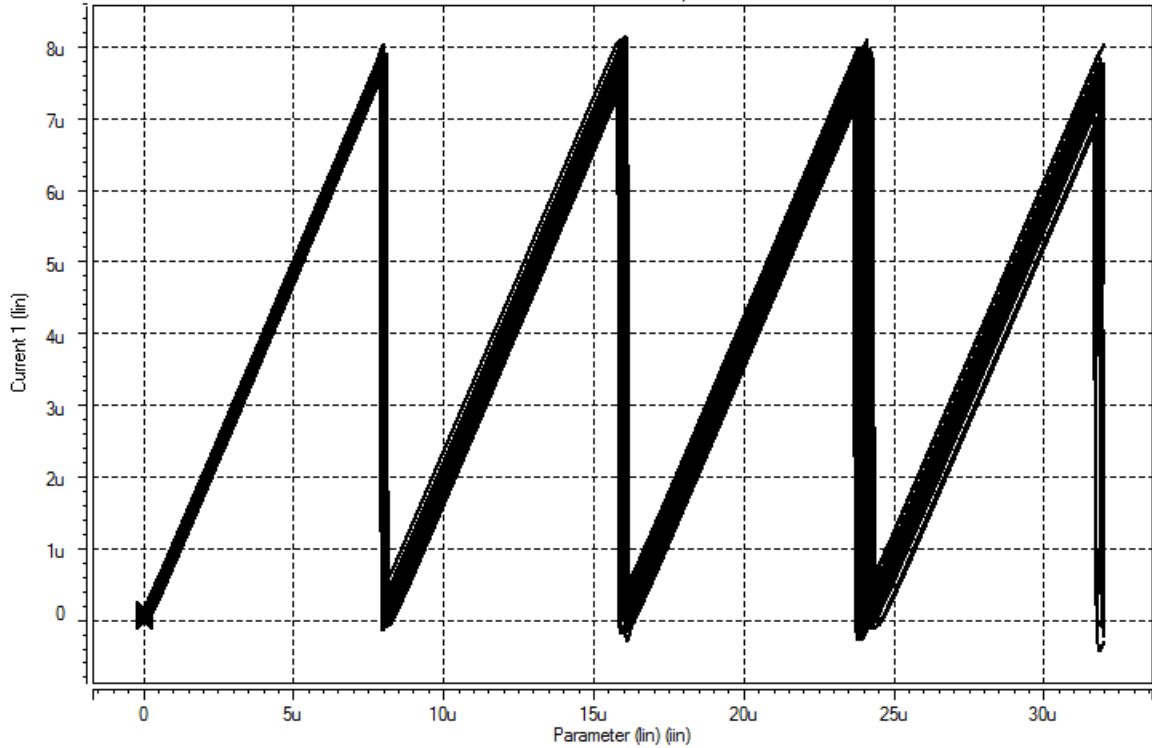


Figure 4-9: Effect of process variations of biasing currents on the DC characteristic

Simulation for temperature analysis was carried out. The temperature was swept from -25C° to 75C° in steps of 50C°. The simulation result shown in Figure 4-10 confirms that the circuit is insensitive to temperature variation.

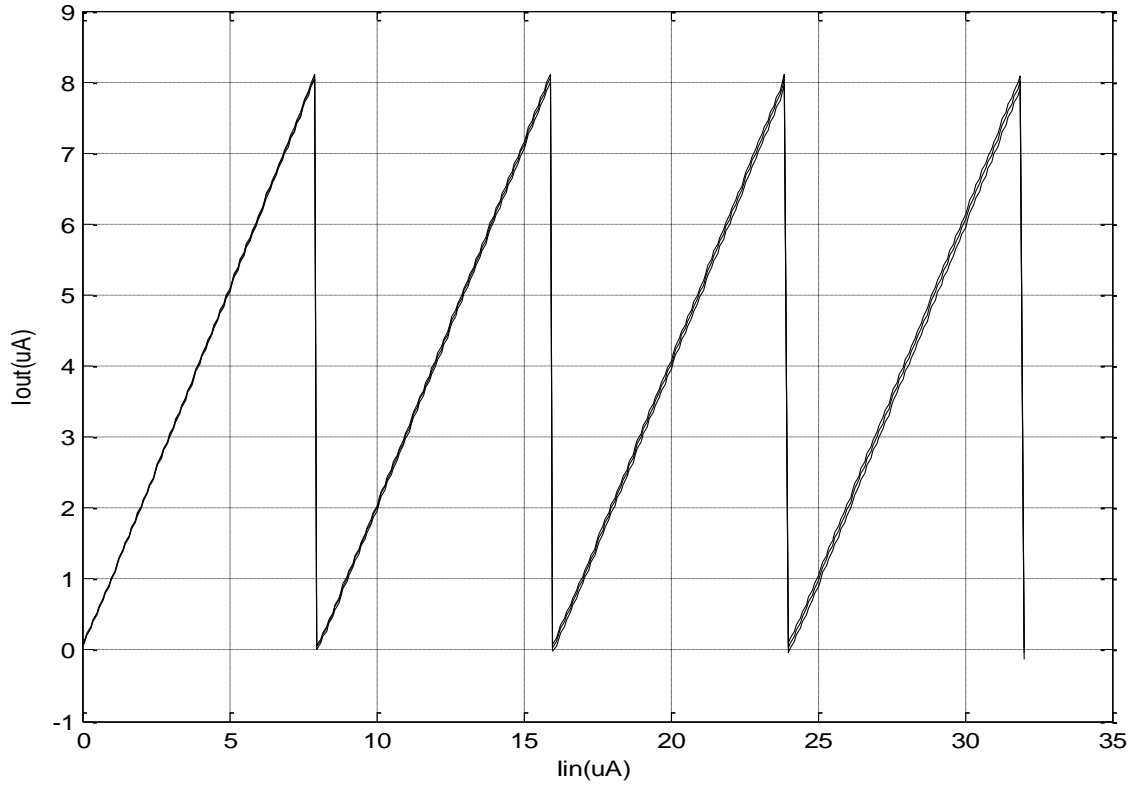


Figure 4-10: Effect of temperature variations on DC characteristic

Simulation for power supply variation was also carried out. The supply voltage was varied between 0.9V and 1.1V in steps of 0.1V. Simulation result shown in

Figure 4-11 indicates that the folded signal shape is still saw-tooth type.

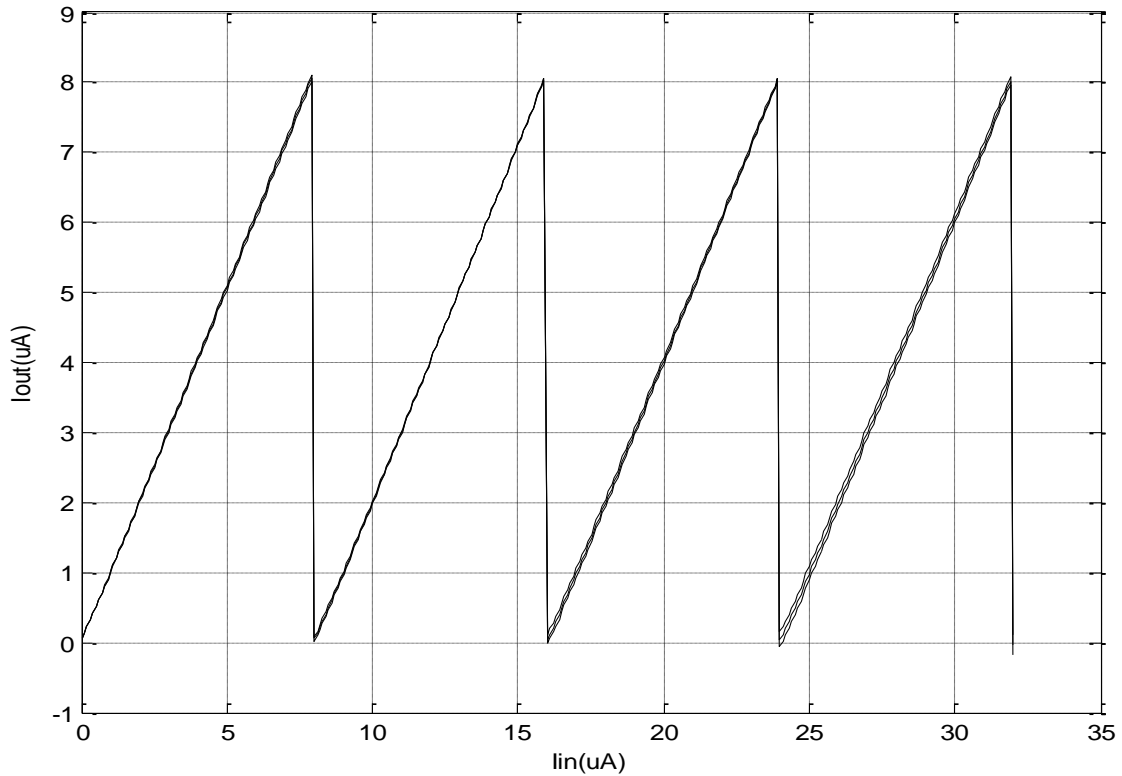


Figure 4-11: Effect of power supply variations on DC characteristic

Findings and Recommendation:

The folding amplifier works fine and produce a close to saw tooth output but the following was observed:

- 1- The proposed folding amplifier designed based on simple current mirrors using $0.35\mu\text{m}$ CMOS technology. The problem here is that transient response shows that the maximum input signal is 10 KHz. I believe that switching the mirror transistors between ON and OFF is the cause for this low frequency.

- 2- If cascode current mirrors are used, the folding amplifier can approximate saw tooth shaped folding transfer characteristics very well. But it doesn't improve the speed.
- 3- Using 0.18 μ m CMOS technology in simple and cascade current mirror folding amplifier also didn't solve the problem.

Recommendation:

The idea of folding sounds good but need to look at a way to overcome the signal frequency limitation.

4.2.2 Noise Analysis

It is well known that noise is an important factor to be considered when designing any electronic circuit or system.

There are different types of noise:

- 1- Thermal noise.
- 2- Flicker noise.
- 3- Shot noise.

In this work we focus on internal noise. Noise analysis was carried out by simulation. The frequency is swept to 10GHz. Simulation result shown in Figure 4-12 indicates that the noise level is acceptable for a frequency up to 0.5GHz in which the noise is 1nA since the circuit current range is few μ A.

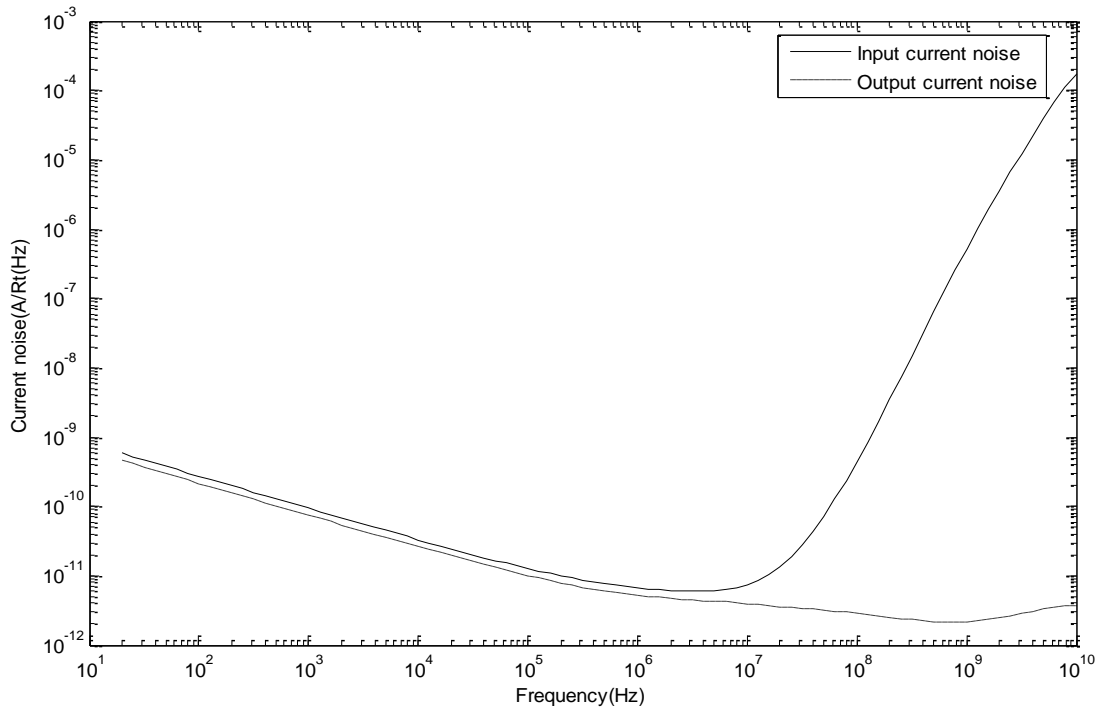


Figure 4-12: Noise current for proposed folding amplifier

4.2.3 Current Buffer

Typically a current buffer is used to transfer a current from a first stage, having a low input impedance level, to a second stage with a high output impedance level to overcome loading effect. Second generation current conveyer (CCII) is used as a current buffer by connecting Y to the ground, X to the input and take the output from Z as shown in Figure 4-13.

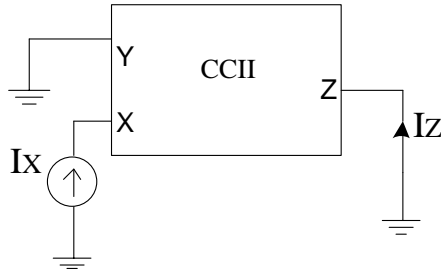


Figure 4-13: The CCII+ used as a current buffer

The circuit diagram for current conveyer presented in [57] is shown in Figure 4-14. This CCII+ simulated using 0.35 μ m technology with 1V power supply and transistor dimensions shown in Table VII to meet input-output characteristics of the current buffer in Figure 4-14. Simulation results are shown in Figure 4-15

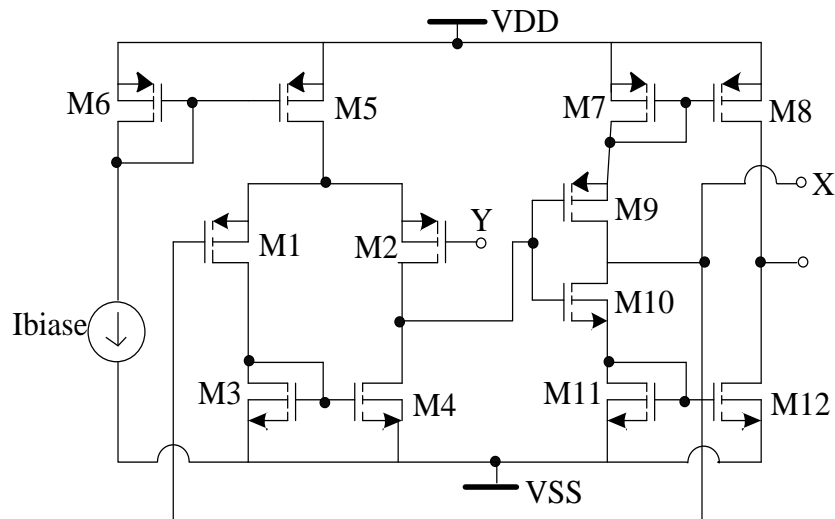


Figure 4-14: Architecture of the CCII+

Table VII: Transistors dimensions for CCII+

Transistor	W(μm)	L(μm)
M1,M2	0.7	0.35
M3, M4		
M5, M6		
M7 ,M8	4	2
M9, M10		
M11, M12		

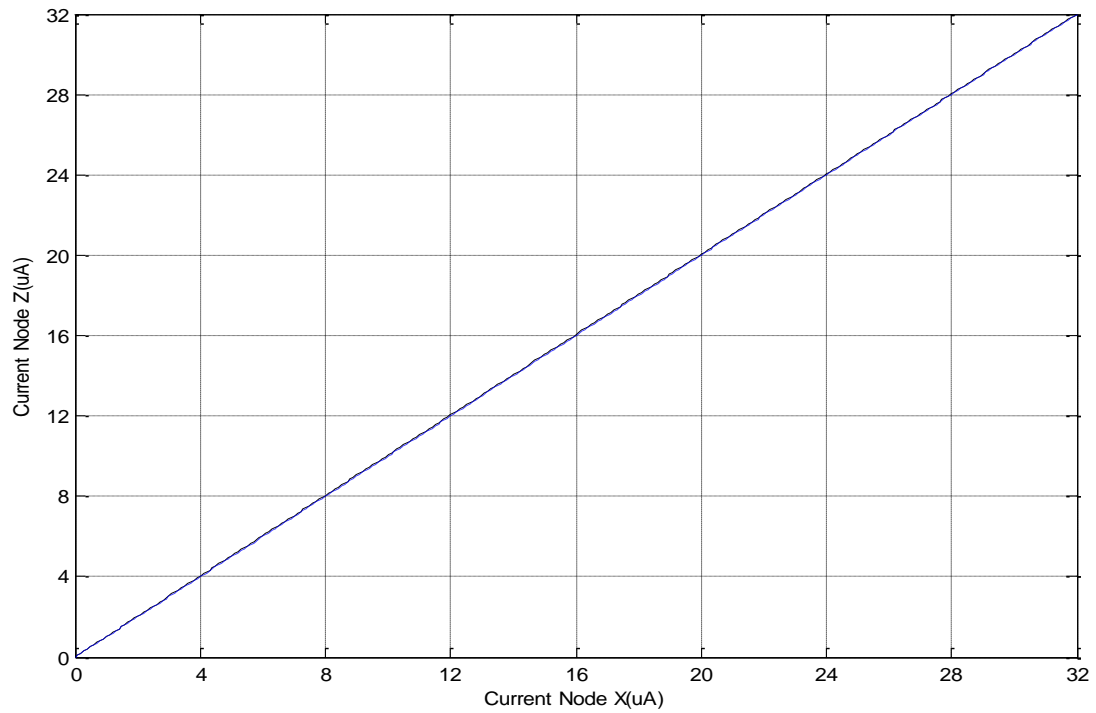


Figure 4-15: DC analysis of CCII+ used as current buffer

Figure 4-15 indicates that the CCII+ is working as a current buffer with small mismatch, which will not affect the saw-tooth shape output.

4.3 DC analysis of 5 bit proposed current-mode folding ADC

The complete circuit of the 0.35 μm CMOS current-mode folding ADC is designed and simulated using Tanner tools. Figure 4-16 shows the simulation results of 5 bit current-mode folding ADC for a ramp signal of 0 to 32 μA . As seen from the simulation result, the LSB bits are well synchronized with MSB bits.

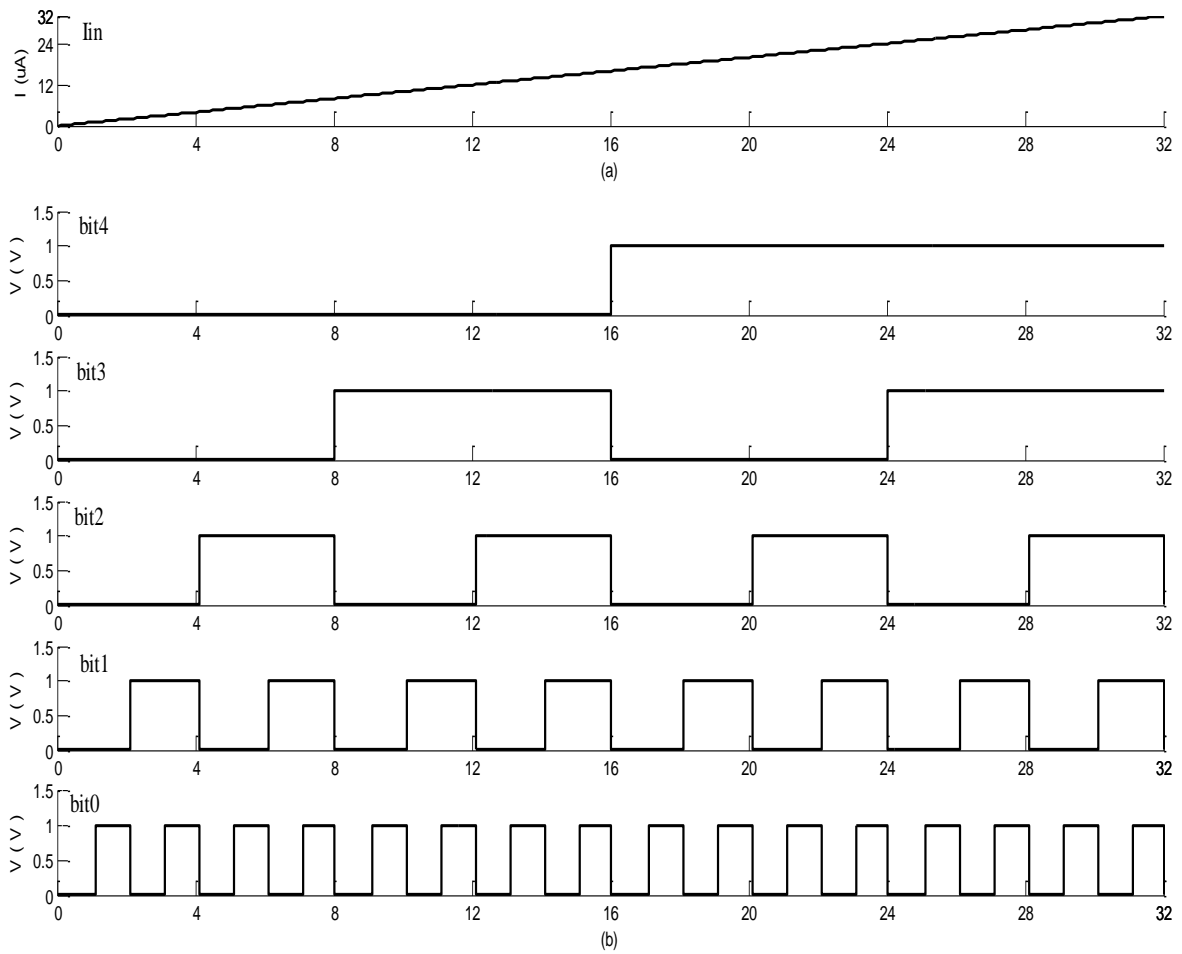


Figure 4-16: The proposed current-mode folding ADC's output to the ramp input: (a) Analog input, (b) Digital output

For better performance measurement of ADC, simulation results of output signal for an analog ramp input signal using W-edit waveform viewer of Tanner tools are exported to matlab to indicate the transfer characteristic of the folding ADC. As shown in Figure 4-17 by combining the weighted sums of the digital output as shown in the equation (4-24)

$$Y = \text{bit}_0 + 2 * \text{bit}_1 + 4 * \text{bit}_2 + 8 * \text{bit}_3 + 16 * \text{bit}_4 \quad (4 - 24)$$

For 5 bits provide a total of $2^5 = 32$ possible codes and each transition occurs at intervals of $I_{\text{ref}}/2^5 = 32\mu/32 = 1\mu = 1\text{LSB}$ as an ideal step size.

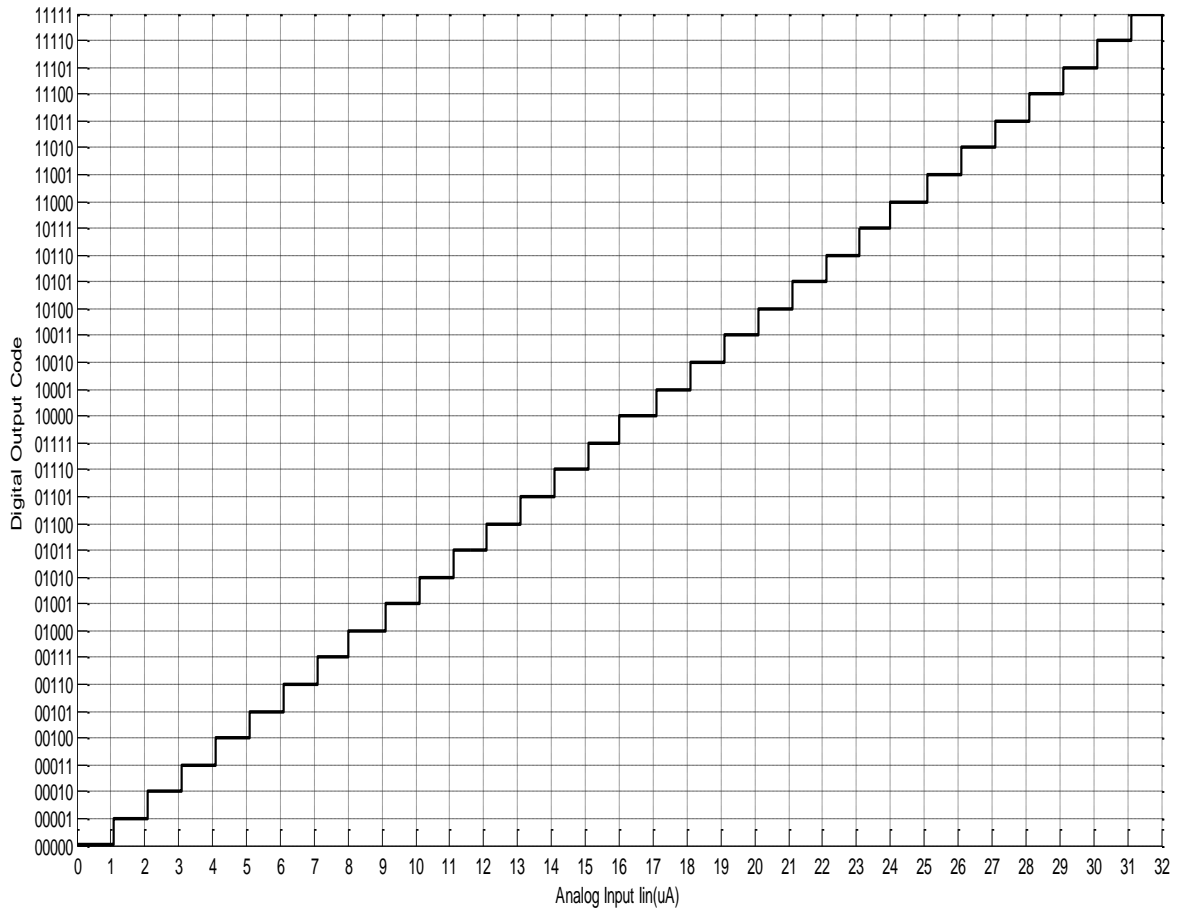


Figure 4-17: Output signal for an analog ramp input signal of the proposed folding ADC.

4.4 Characterization of ADC

The performance of ADC can be measured into two ways, namely static and dynamic characteristics.

4.4.1 Static characteristics – INL/DNL measurement

Differential nonlinearity (DNL) and integral nonlinearity (INL) are defined the static performance of an ADC. These are measured in terms of percent or LSBs of full-scale range. DNL error is the difference between an actual step width and the ideal value of 1LSB.

$$\text{DNL} = \text{Actual step (code) width} - \text{Ideal step (code) width}$$

For an ideal ADC, $\text{DNL} = 0\text{LSB}$, each step equals 1LSB, which $I_{FS}/2^5 = 32\mu/32 = 1\text{LSB} = 1\mu$, where I_{FS} is the full scale range and N is the number of bits of the ADC. INL error is described as the difference between the actual data converter code transition points and a straight line. A straight line is drawn between the end points of first and last code transitions.

DNL and INL can be calculated by comparing the actual data converter code output that shown in Figure 4-17 to the ideal code output. DNL and INL measurement results are preformed using matlab. The set of output current levels are exported from W-edit wave reviewer as .txt file subsequently read into matlab as a matrix and compared with another

matrix with the ideal current values for a 5 bit folding ADC. Figure 4-18 presents DNL and INL measurement result for ramp input signal.

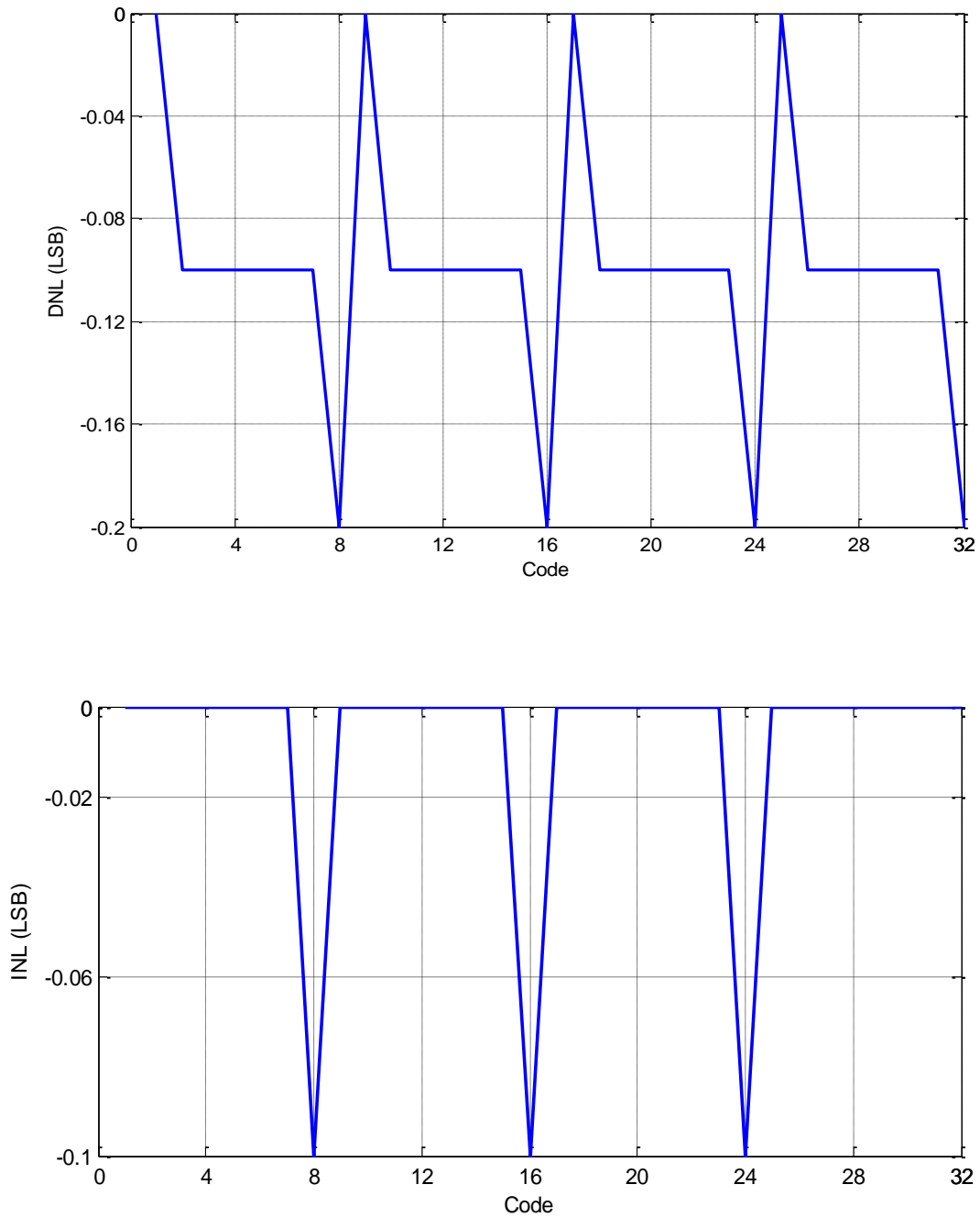


Figure 4-18: Measured DNL and INL

As observed from Figure 4-18 of DNL and INL plots for the proposed folding ADC, the DNL varies from 0 LSB to -0.2 LSB and INL is from 0 LSB to -0.1 LSB. This result guarantees the DNL and INL values are reasonable, there is no missing code and this current-mode folding ADC is monotonic.

4.4.2 Dynamic characteristics

Dynamic performance of the ADC is very important in many applications. To test the dynamic performance of the proposed ADC, sinusoidal input signals are used, which are quantized by the ADC and the digital signal codes are analyzed using transient analysis. Fast Fourier transform (FFT) analysis provides information on dynamic characteristics of the proposed folding ADC. Then SNR, SNDR, SFDR and ENOB are provided from spectrum analysis of FFT spectrum.

Figure 4-19 shows the power spectrum of a 10 kHz input sinusoid, which is a very small input frequency, sampled with 190 KHz clock rate. The FFT length is 512. Mathematically the values of SNDR and ENOB are 31.86dB and 5 bits respectively are given by equations (1-2) and (1-3). From simulation results there are strange peaks at 26, 36 and 38 KHz, degrading the SNDR from the ideal case to a 29.5dB, given 4.6 ENOB.

The strange peaks can be due to one of the following:

- 1- Circuit hardware due to MOS switching between ON and OFF state.
- 2- Though the mirroring error in single current mirror is small but the error accumulates when it propagates from the first block to the last block.
- 3- FFT sweeping steps are not properly selected.

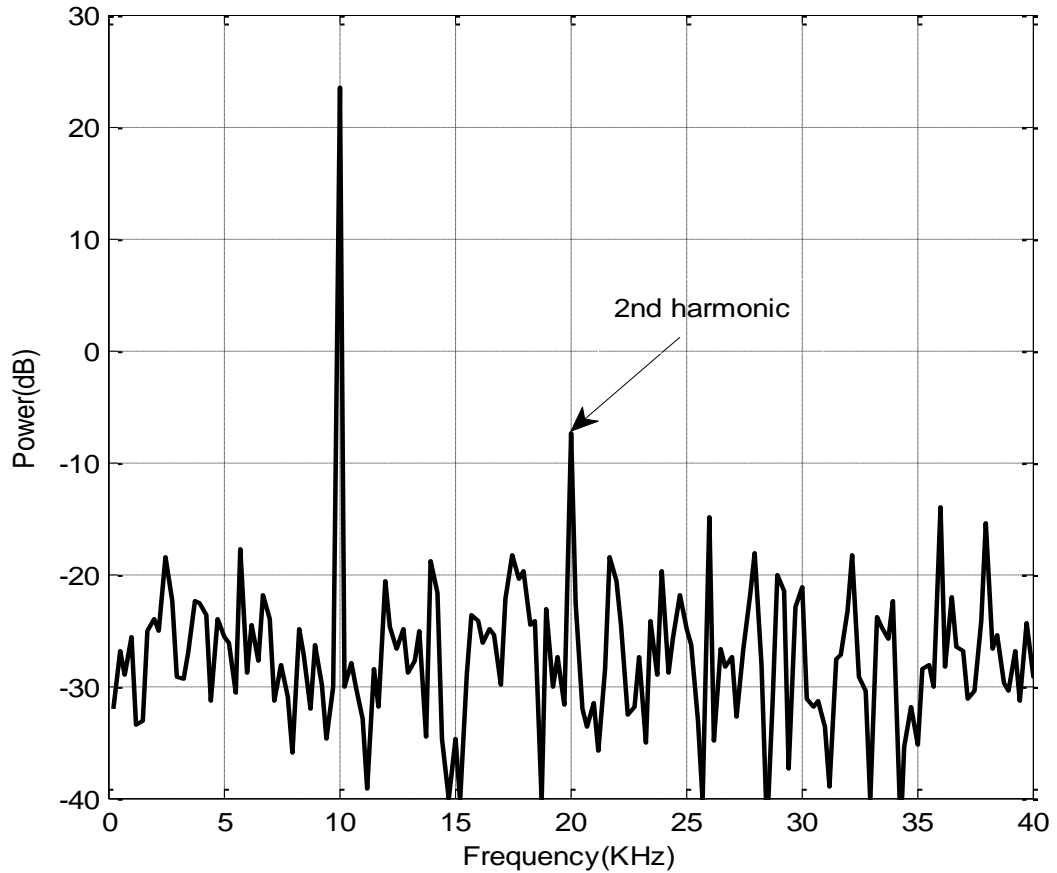


Figure 4-19: FFT calculated power spectrum from the sampled ADC output data $f_{in}=10$ kHz and $f_s=190$ KSPS.

The output spectrum of two-tone input which are 7 KHz and 9 KHz, which is very small frequencies, is shown in Figure 4-20, the zoomed in plot at the bottom shows $IMD3=15$ dB which is not good. It shows that some strange peaks at different frequencies are present in the output, degrading the $IMD3$. Again, the reason for this could be switching ON and OFF of MOS transistors in folding amplifier or is possibly due to the improper selection of the FFT sweeping steps.

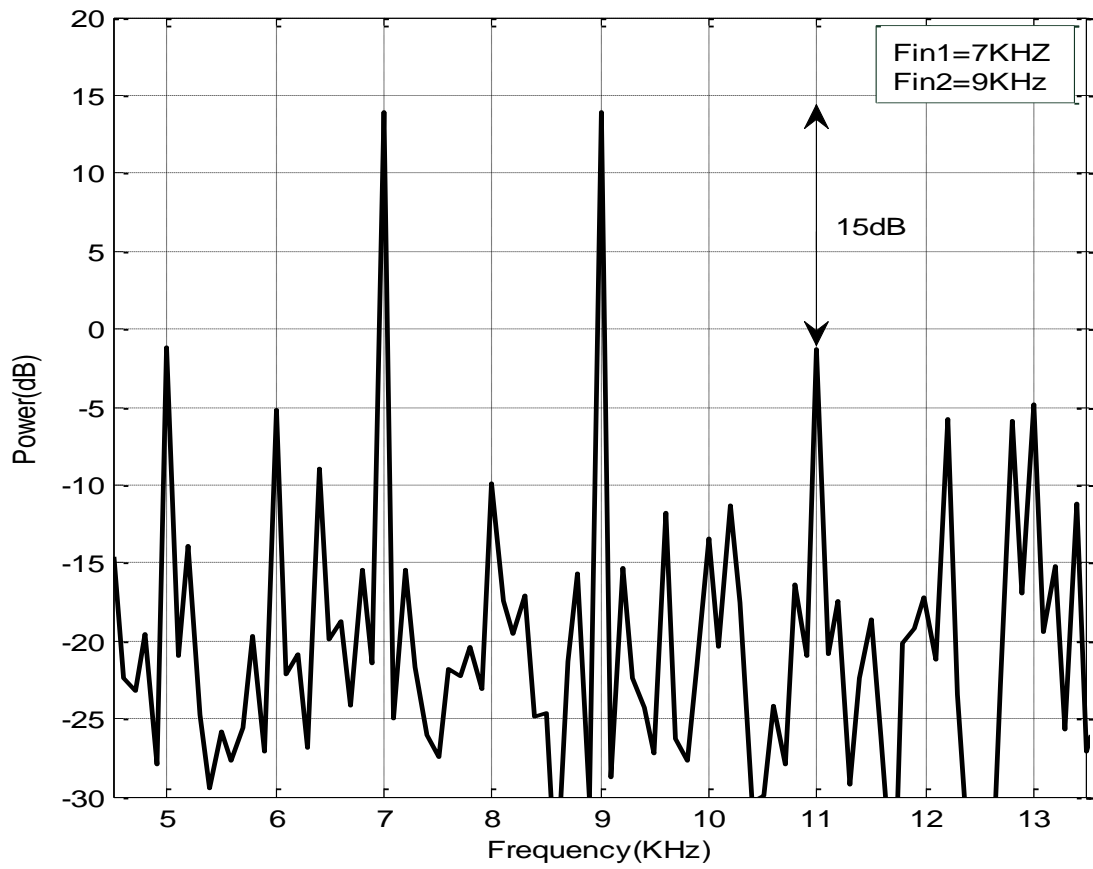


Figure 4-20: The output spectrum of two input-tone input which are 7KHz and 9KHz at 190KS/s sampling speed

4.5 Summary of Current-Mode Folding ADC

A 5 bit current-mode folding ADC requires 10 comparators to generate thermometer code. While for flash ADC 31 comparators is needed. This obviously implies that the number of components can be reduced using current-mode folding ADC and hence consume less power and can be built on small die area. The accuracy of this proposed folding ADC based on results simulation of INL and DNL is very good. Table VIII summarizes the performance of this folding ADC.

More to the point the reduction in the die area and power consumption, there are many important benefits of using the proposed current-mode folding ADC:

- I. One step operation guarantees high speed conversion.

Two-step or multi-step ADC is undesirable due to several clock cycles is required to convert the data, whereas one clock is required for folding ADC like full-flash ADC.

- II. No interpolation needed

Using the proposed current-mode folding amplifier that generates saw-tooth wave form will make the interpolation not needed.

Area estimation is done based on the design rules of the 0.35 μ m technology in S-Edit tanner tool.

The estimated area of the proposed folding ADC is 0.04 mm^2

Table VIII summarizes the ADC performance, it is clear that the Proposed ADC has relatively good DNL and INL results which are less than ± 0.5 LSB so this converter is monotonic, low power consumption and quite small chip area. SFDR, SNDR and ENOB result is slightly reasonable. The major disadvantage of the proposed ADC is the very low frequency of operation which is limited to 10 KHz. So it is suitable for low frequency signal application, for example sensor networks.

Table VIII Performance summary of Folding and Interpolating ADC

Architecture	Current-Mode Folding ADC
Technology	CMOS 0.35 μ m
Supply voltage	± 1 V
Number of bits	5
Sampling frequency	190KS/s
Input dynamic range	$0 \leq I_{in} \leq 32\mu$ A
Step size	1 μ A
Input signal frequency	10KHz
SFDR	31dB
SNDR	29.5dB
ENOB	4.6 bit
DNL	0 LSB to -0.2 LSB
INL	0 LSB to -0.1 LSB
Power dissipation	1.26mW

Table IX summarizes the comparison between the proposed ADC and previously published work. The proposed work has significantly low power consumption and better INL and DNL than previously published work. However, it must be mentioned here the INL and DNL were calculated manually. The chip area can be much smaller if 90nm technology is used. However the proposed design suffers from low speed because of very low frequency of operation which is the main disadvantage of this ADC. It is clear that using the proposed folding amplifier is not suitable for high speed ADC applications.

Table IX: State of the art medium resolution CMOS folding ADCs

Reference	[23]	[16]	[36]	[58]	This work
Publication	2003	2006	2008	2009	2013
Technology	0.35 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	90 nm CMOS	0.35 μ m CMOS
Supply Voltage	3.3V	3.3V	1.8V	1V	\pm 1V
Bits	7	8	6	5	5
Type	VM	VM	VM	VM	CM
Sample and Hold	Yes	Yes	Yes	Yes	Yes
Speed	300 Msps	200 Msps	1000Msps	1.75Gsps	190 Ksps
INL	<1LSB	0.77LSB	\pm 0.7LSB	0.3 LSB	-0.1LSB
DNL	<0.6LSB	0.6LSB	\pm 0.5LSB	0.3 LSB	-0.2LSB
Power consumption	200mW	181mW	60mW	2.2mW	1.26mW
Area (mm^2)	1.2	0.25	0.27	0.02	0.04

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In this thesis a current mode folding amplifier which produces close to ideal saw tooth signal is presented. As an application of the folding amplifier a 5 bit CMOS current-mode folding A/D converter is designed and simulated using Tanner Tools 0.35 μ m technology.

The proposed design of CMOS current-mode folding A/D converter has less complexity by reducing the number of comparators, less silicon area and less power consumption and increased the accuracy. In other words, the proposed current-mode folding A/D converter eliminates the major disadvantages of the flash and the interpolating converter structures.

However, the design suffers from low speed because the folding amplifier input signal is limited to 10 KHz which is very low and it is probably due to switching between ON and OFF of MOS transistors used, so this will limit the speed of ADC. It is clear that there is a problem in speed and more work has to be done to improve the speed of the proposed design by improving the folding amplifier.

It is worth mentioning here that FFT shows strange peaks which degrade the performance of the proposed ADC for parameters like SFDR, SNDR and ENOB. More degradation is observed in IMD3 when two input-tones are applied. This problem could

be from the core circuit due to switching between ON and OFF MOS transistors used or from FFT improper selection of sweeping steps.

5.2 FUTURE WORK

For future studies and extensions of the work presented in this thesis.

- The researcher must investigate the limitation on input signal frequency. This is essential for developing ADC that can meet the requirements of present day industry.
- The researcher can extend this architecture from medium to high resolution.

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