



**CMOS CIRCUIT TECHNIQUES FOR BIOMEDICAL  
APPLICATIONS**

BY

**YAQUB ALHUSSAIN MAHNASHI**

A Thesis Presented to the  
DEANSHIP OF GRADUATE STUDIES

**KING FAHD UNIVERSITY OF PETROLEUM & MINERALS**

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the  
Requirements for the Degree of

**MASTER OF SCIENCE**

In

**ELECTRICAL ENGINEERING**

**MAY 2012**

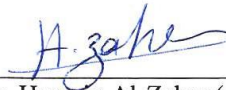
KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS

DHAHRAN 31261, SAUDI ARABIA

DEANSHIP OF GRADUATE STUDIES

This thesis, written by **Yaqub Alhussain Mahnashi** under the direction of his thesis advisor and approved by his thesis committee, has been presented to and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE IN ELECTRICAL ENGINEERING.**

Thesis Committee



Dr. Hussain Al-Zaher (Advisor)



Dr. Mohamed Mohandes (Member)



Dr. Munir Al-Absi (Member)



Dr. Ali Al-Shaikhi

Department Chairman



Dr. Salam A. Zummo  
Dean of Graduate Studies



5/6/14

Date

*I would like to dedicate my thesis to*

*My parents*

*My Brothers and Sisters*

*My wife*

*and My son Yusuf,,*

*your love and support are always the source of my strength*

## ACKNOWLEDGMENT

First and foremost, I thank ALLAH for all the blessings and wonderful opportunities he has bestowed upon me in my journey through life. It is only by his grace that I have had the ability and strength to overcome life's challenges. May peace and blessing be upon his prophet Mohammed (PBUH), his family and his companions.

My deep appreciation goes to my thesis advisor, Dr. Hussein Al-Zaher, for his continuous help, guidance and the countless hours of attention he devoted during this work. Thanks are also due to my thesis committee members (Dr. Munir Al-Absi and Dr. Mohamed Muhandes) for their useful comments on the thesis. Heartfelt thanks are also due to Mr. Numan Tasadduq, who helped me a lot during my work. Also, I would like to thank my colleagues and friends who helped me through my study.

Acknowledgment is due to King Fahd University of Petroleum and Minerals for supporting this research.

I wish to express my heartfelt gratitude to my parents for their encouragement, prayers and continuous support. Also, I would like to express my sincere appreciation to my dear wife for her great patience and motivation. I owe great thanks to my brothers and sisters for their encouragement.

# TABLE OF CONTENTS

|   |           |
|---|-----------|
| ACKNOWLEDGMENT                                | II        |
| TABLE OF CONTENTS                             | III       |
| LIST OF FIGURES                               | V         |
| LIST OF TABLES                                | VII       |
| THESIS ABSTRACT (ENGLISH)                     | VIII      |
| THESIS ABSTRACT (ARABIC)                      | IX        |
| <b>1. INTRODUCTION</b>                        | <b>1</b>  |
| 1.1    BIOELECTRONICS                         | 1         |
| 1.2    PROBLEM STATEMENT                      | 4         |
| 1.3    THESIS ORGANIZATION                    | 6         |
| <b>2. LITERATURE REVIEW</b>                   | <b>7</b>  |
| 2.1    INTRODUCTION                           | 7         |
| 2.1.1    Low Frequency Nature                 | 7         |
| 2.1.2    Weak Signals                         | 9         |
| 2.1.3    Low Power Needs                      | 10        |
| 2.2    RESEARCH GOALS                         | 11        |
| <b>3. LOW FREQUENCY FILTERS TECHNIQUES</b>    | <b>13</b> |
| 3.1    INTRODUCTION                           | 13        |
| 3.2    ANTONIO SIMULATED INDUCTANCE TECHNIQUE | 14        |

|   |           |
|---|-----------|
|   | IV        |
| 3.3 R-2R LADDER TECHNIQUE                             | 16        |
| 3.4 DIFFERENCE TERM TECHNIQUE                         | 23        |
| 3.5 CURRENT ATTENUATOR TECHNIQUE                      | 32        |
| <b>4. DESIGN AND SIMULATION RESULTS</b>               | <b>37</b> |
| 4.1 INTRODUCTION                                      | 37        |
| 4.2 OP-AMP SELECTION                                  | 38        |
| 4.3 LOW PASS FILTER DESIGN BASED ON R-2R APPROACH     | 46        |
| 4.4 LOW PASS FILTER DESIGN BASED ON COMBINED APPROACH | 55        |
| <b>5. CONCLUSION AND FUTURE WORK</b>                  | <b>61</b> |
| 5.1 CONCLUSION  | 61        |
| 5.2 FUTURE WORK                                       | 62        |
| APPENDEX A  | 63        |
| REFERENCES  | 67        |
| VITA  | 72        |

## LIST OF FIGURES

|  |    |
|--|----|
| Figure 1.1: Interactions of biomaterials and electronics elements for bioelectronics applications [2].   | 2  |
| Figure 1.2: Voltage and frequency ranges of some bio-signals [3].  | 3  |
| Figure 1.3: The generic blocks of typical biomedical system.   | 4  |
| Figure 1.4: Electrocardiogram signal.  | 5  |
| Figure 3.1: The <i>Antoniou</i> inductance simulation circuit.   | 15 |
| Figure 3.2: Digitally controlled R-2R ladder.  | 16 |
| Figure 3.3: The total and equivalent resistances for R-2R vs. number of bits.  | 17 |
| Figure 3.4: The ratio of the equivalent resistance to the actual one for $\alpha=0.5$ , $\alpha=1$ and $\alpha=2$ .  | 19 |
| Figure 3.5: Finite gain Op-Amp based amplifier with R- $\alpha$ R networks.  | 20 |
| Figure 3.6: Finite gain Op-Amp based amplifier.  | 21 |
| Figure 3.7: Simulation vs. theoretical results for the open loop gain increase.  | 22 |
| Figure 3.8: The integrator used for the difference term approach.  | 25 |
| Figure 3.9: 2 <sup>nd</sup> order LPF applying difference approach.  | 25 |
| Figure 3.10: The sensitivity vs. $R_2$ ( $R_1$ is kept constant equals to 10k $\Omega$ ).  | 28 |
| Figure 3.11: 2 <sup>nd</sup> order LPF frequency responses based on difference term technique for two cases: $R_2=9.4\text{k}\Omega$ and $R_2=5\text{k}\Omega$ . | 29 |
| Figure 3.12: The frequency bandwidth histogram when $R_2=5\text{k}\Omega$ .  | 30 |
| Figure 3.13: The frequency bandwidth histogram when $R_2=9.4\text{k}\Omega$ .  | 30 |
| Figure 3.14: The current feedback operational amplifier block diagram.   | 33 |
| Figure 3.15: Programmable CFOA.  | 34 |

|   |    |
|---|----|
| Figure 3.16: CFOA based integrator. ....  | 35 |
| Figure 3.17: 2 <sup>nd</sup> order CFOA with voltage attenuators (VA) based LPF. ....   | 35 |
| Figure 4.1: A two stage class-AB Op-Amp[32]. ....   | 39 |
| Figure 4.2: Supply independent current refrence. ....   | 41 |
| Figure 4.3: Magnitude and phase responses of the Op-Amp. ....   | 42 |
| Figure 4.4: Op-Amp open loop gain histogram. ....   | 43 |
| Figure 4.5: Op-Amp unity gain bandwidth histogram. ....   | 44 |
| Figure 4.6: Setup to find the slew rate. ....   | 45 |
| Figure 4.7: Single ended 2 <sup>nd</sup> LPF Op-Amp realization of Tow-Thomas bi-quad with R-2R approach. ....                  | 46 |
| Figure 4.8: Differential input and output 2 <sup>nd</sup> LPF Op-Amp realization of Tow-Thomas bi-quad with R-2R approach. .... | 47 |
| Figure 4.9: Resistor layout serpentine pattern. (a) with corners. (b) without corners. ....                                     | 49 |
| Figure 4.10: Poly-Poly capacitor layout structure [35]. ....  | 50 |
| Figure 4.11: 2 <sup>nd</sup> order R-2R based LPF layout. ....  | 52 |
| Figure 4.12: Frequency responses of 2 <sup>nd</sup> order LPF based on R-2R approach. ....                                      | 53 |
| Figure 4.13: Frequency and gain tuning feature for the R-2R based filter. ....  | 53 |
| Figure 4.14: Temperature effect on the pole frequency. ....   | 54 |
| Figure 4.15: Differential realization of 2 <sup>nd</sup> order LPF based on the combined approach. ....                         | 55 |
| Figure 4.16: 2 <sup>nd</sup> order combined based LPF layout. ....  | 57 |
| Figure 4.17: 2 <sup>nd</sup> LPF frequency response based on the combined approach. ....  | 58 |
| Figure 4.18: Frequency and gain tuning feature for the combined based filter. ....  | 58 |
| Figure 4.19: Frequency response of the combined approach filter. ....   | 59 |



## LIST OF TABLES

|   |    |
|---|----|
| Table I: Electrocardiogram system requirement .....                         | 6  |
| Table II: Summary of various filters used for biomedical applications. .... | 9  |
| Table III: General performance comparison of various structures. ....       | 11 |
| Table IV : Summary of Monte Carlo simulation results. ....                  | 31 |
| Table V: Comparison between four different Op-Amps. ....                    | 38 |
| Table VI: Op-Amp transistor sizes.....                                      | 42 |
| Table VII : Area estimation for different R-2R networks. ....               | 51 |
| Table VIII : Comparison between this work and other related work.....       | 60 |

**THESIS ABSTRACT (ENGLISH)**

NAME OF STUDENT: YAQUB AI-HUSSAIN MAHNASHI

TITLE OF STUDY: CMOS CIRCUIT TECHNIQUES FOR BIOMEDICAL  
APPLICATIONS

MAJOR FIELD : ELECTRICAL ENGINEERING

DATE OF DEGREE : MAY, 2012

The exponential increase in demand of biological systems has renewed research in very low frequency circuit techniques. Developing new fully integrated solutions exhibiting improved characteristics is highly desired. Area, linearity, noise and power consumption are the main performance indicators of biomedical applications. In this thesis, various techniques to realize low power and low frequency (LPLF) operation are investigated. Consequently, new circuit design solutions are developed. The proposed designs provide advantages over the available solutions in terms of power consumption, linearity, noise and area. As an application example, Low pass filter for portable Electrocardiogram (ECG) system is designed and simulated using 0.18 $\mu$ m CMOS technology in Tanner tools. Implementation of such filters in a relatively small silicon area and with high linearity and low power promotes the utilization of very large-scale integration (VLSI) techniques in biomedical instrumentation.

**MASTER OF SCIENCE**

**KING FAHD UNIVERSITY OF PETROLUUM AND MINERALS**

**DHAHRAN-SAUDI ARABIA**

**MAY 2012**

## خلاصة الرسالة

الاسم: يعقوب الحسين يحي محنشي

العنوان: حلول عملية لتصميم الدوائر الإلكترونية المناسبة للتطبيقات الحيوية باستخدام تقنية CMOS

التخصص: هندسة كهربائية

التاريخ: مايو 2012

مع الزيادة الكبيرة والمطرقة في الطلب والحاجة إلى الأجهزة الإلكترونية المستخدمة في المجالات الطبية كجهاز مقياس نبضات القلب (Electrocardiogram)، أصبح تطوير وإستحداث طرق جديدة تساهم في رفع كفاءة هذه الأجهزة مطلباً هاماً. وتعد تقنية CMOS من أهم التقنيات المستخدمة حالياً في تصنيع الدوائر الإلكترونية والأساسية لهذه الأجهزة.

في هذه الرسالة قام الباحث بدراسة أربع طرق مختلفة باستخدام تقنية (CMOS) للوصول إلى التقنية الأمثل في تصميم المرشحات ذات النطاق المنخفض والمهمة جداً في كثير من الأجهزة الحيوية الحديثة حيث توجد صعوبة في تصميم مثل هذه المرشحات لما تتطلبه من قدرة عالية للتعامل مع الإشارات القادمة من جسم الإنسان والتي تكون بطبيعتها منخفضة النطاق والجهد وكذلك من السهل أن تتأثر بالضوضاء. وكذلك يتطلب تصميم وصنع هذه المرشحات مساحة قليلة لتساهم في إمكانية تصغير مساحة الدوائر الإلكترونية الداخلة في تصنيع الجهاز وبالتالي يسهل حمله على المريض وبذلك يتمكن الطبيب من مراقبة وظائف المريض الصحية عن بعد. وشرط آخر للتحقق من مدى جدوى هذه التقنيات وهو القدرة المستهلكة للمرشح حيث تم دراستها. وتم تصميم مرشحات ذات نطاق منخفض باستخدام تقنية R-2R ومرشح آخر عن طريق دمج تقنية R-2R مع تقنية أخرى تعمل على التحكم في نطاق المرشح لنقله من نطاق عالي إلى نطاق منخفض. وقد أستخدم برنامج TANNER وتقنية CMOS 0.18µm لمحاكاة عمل المرشحات المصممة وقد أثبتت النتائج مدى تفوق هذا التقنيات على بعض التقنيات الأخرى المستخدمة في هذا المجال. وأخيراً ختمت الرسالة بعرض سريع لأهم مميزات المرشحات المصممة وتقديم توصيات و مقترحات للبحوث المستقبلية في هذا المجال.

درجة الماجستير في العلوم

جامعة الملك فهد للبترول و المعادن

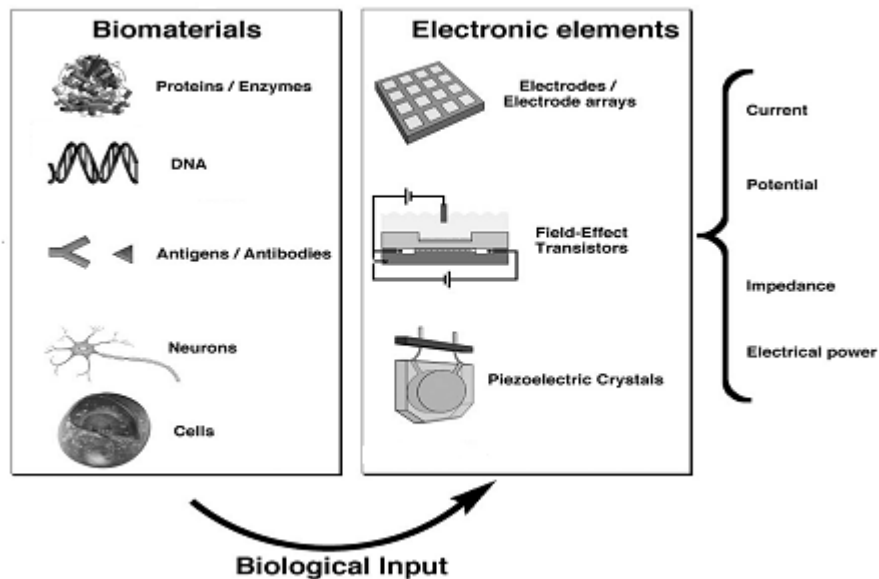
الظهران- المملكة العربية السعودية

مايو 2012

# 1. INTRODUCTION

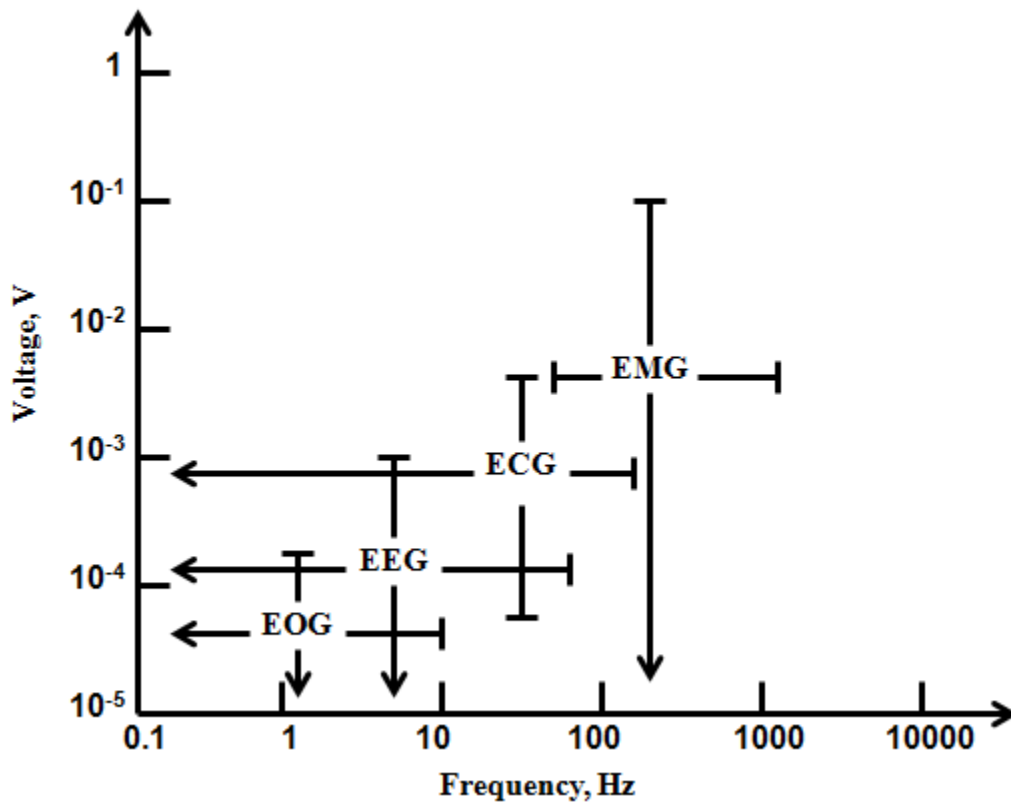
## 1.1 BIOELECTRONICS

The field of combining biology and electronics hold a great promise to enhance the quality of humanity health care [1]. Nowadays, these two fields have emerged resulting in attraction of great scientific attention and funding. Bioelectronics was firstly appeared in the science fiction books and research in this area was established in the mid-1970 [2]. Although bioelectronics has many aspects to look at, for example biosensors, animals' bimolecular systems, implanted devices etc; only the aspect of designing circuits for biomedical systems is investigated in this thesis. Figure 1.1 shows the combination of biomaterials and electronics elements forming what is called bioelectronics [2]. It shows that some biomaterials, such as DNA, neurons and protein can be sensed and translated into electrical parameters, voltage, current and/or impedance, using proper sensing elements. For example, the movement of the foot muscle for a person while walking can be sensed and converted to electrical signal using the piezoelectric crystal. Such transformation is crucial for medical doctors when they need more information about the operation of a specific organ. In addition to that, it provides a quick test for some diseases, such as adiabatic portal test devises which are widely used to monitor the level of the sugar in the human body without visiting the hospital.



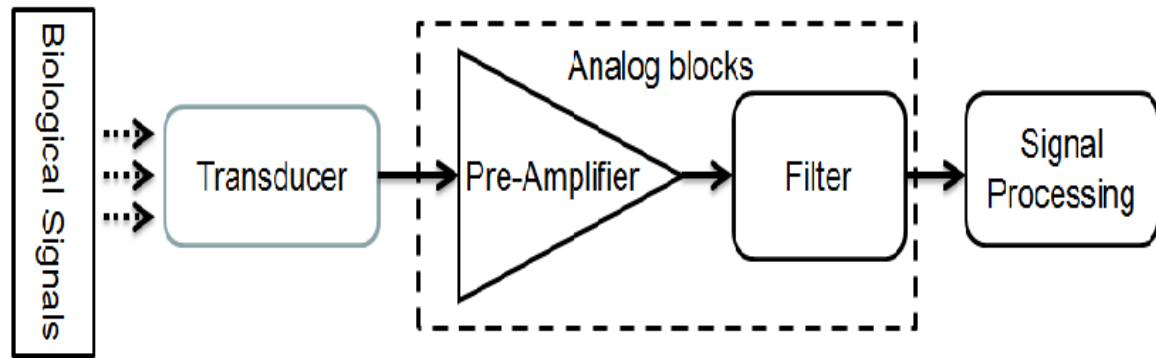
**Figure 1.1: Interactions of biomaterials and electronics elements for bioelectronics applications [2].**

Biomedical signals are the recorded signals of the biomedical actions through special devices. ECG (Electro**cardio**gram), EMG (Electro**myo**gram), EEG (Electro**encephalo**gram), EOG (Electro-**oculo**gram) etc. are some examples of these measuring devices. These signals are generated by electrochemical operation of excitable cells such as nervous, muscular and glandular tissue. Electric potentials are developed when millions of such cells are generated. Weak biomedical signals in order of  $100\mu\text{V}$  to  $10\text{mV}$  can be monitored at the body surface. The bandwidth of EEG, for example, refers to the monitored signal due to the brain activities and ECG which is the signal being recorded due to the heart beats, is  $0.1\text{-}30\text{Hz}$  and  $0.01\text{-}100\text{Hz}$ , respectively. Figure 1.2 shows the frequency ranges of some physiological signals [3].



**Figure 1.2: Voltage and frequency ranges of some bio-signals [3].**

Amplification and pre-filtering of these signals are mandatory before further digital signal processing (DSP) Figure 1.3 [3]. The main function of the low pass pre-analog filtering is to attenuate low frequency drift signals produced by bio-potential electrodes as well as to reject high frequency noise. However, such very low frequency filters need large passive component values which cannot be implemented in standard analog integrated circuit (IC) fabrication. Typical values for integrated resistors are from several ohms to 40k $\Omega$  and for capacitors are from 0.5pF to 50pF [4].



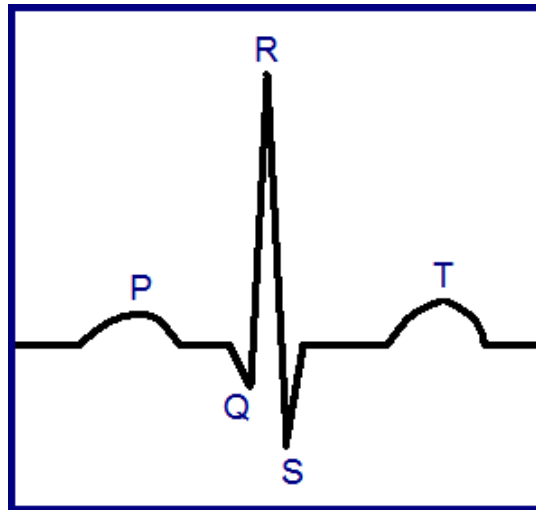
**Figure 1.3: The generic blocks of typical biomedical system.**

Low frequency continuous time filters are difficult to integrate on a chip because of the difficulty in creating large time constants which results in large component values. For example, a filter with pole frequency of 100Hz would require resistance in Mega- $\Omega$  range and capacitor in the nano-farad range, which are impractical options for integration on a chip. An application example that involves very low frequency low pass filtering is used in portable/battery powered ECG monitoring devices.

## 1.2 PROBLEM STATEMENT

Monitoring heart beats is one of the most important aspects which helps medical doctors to better diagnose the patient's disease and also crucial for preventive care. Since 1903, when the first ECG system was invented by a noble prize winner **Willem Einthoven**, many research works has been conducted to come up with an efficient and reliable ECG system.

The heart beats generate a sequence of electrical signals comprises the typical heart signal and sometimes called QRS shown in the Figure 1.4 .The ECG QRS amplitude can range from  $500\mu\text{ V}$  to  $5\text{ mV}$  peak depending on the recording site and the patient's body type.



**Figure 1.4: Electrocardiogram signal.**

The ECG system requirements are highlighted in Table I [3]. It can be clearly noticed that this system needs a  $150\text{ Hz}$  corner frequency low pass filter. However, the order of the filter and stop band attenuation are not specified. Nevertheless, a  $2^{\text{nd}}$  order LPF with maximally flat response is considered here in this work. The preamplifier block shown in Figure 1.3 can be adopted to relax the noise performance of the filter. But in this case this filter should exhibit good linearity to process larger (amplified) signals.



**Table I: Electrocardiogram system requirement**

| <b>Requirement Description</b> | <b>Value</b>      |
|--------------------------------|-------------------|
| <b>Frequency operation</b>     | 150 Hz            |
| <b>Input Dynamic Range</b>     | $\pm 5\text{mV}$  |
| <b>Input referred noise</b>    | $< 30\mu\text{V}$ |
| <b>Slew rate change</b>        | 320 mV/s          |

### **1.3 THESIS ORGANIZATION**

This chapter, INTRODUCTION, presents the motivations, low pass filtering application and the organization of thesis. Chapter 2, LITERATURE REVIEW, discusses the problems of the biomedical systems and summarizes previous work. Chapter 3, LOW FREQUENCY FILTERS TECHNIQUES, presents the proposed techniques to overcome the problems of the very low frequency continuous time filters. Also, simulation results are presented. Chapter 4, DESIGN AND SIMULATION RESULTS, presents the steps to design the low pass filter. Also, a comparison is made between different Op-Amps to select the best one to fulfill the requirements of the proposed filters. In Chapter 5, CONCLUSION AND FUTURE WORK, a summary of the thesis is provided along with recommended future studies and extensions.

## **2. LITERATURE REVIEW**

### **2.1 INTRODUCTION**

Traditionally, large off-chip capacitors were used for very long time constant. The recent trend is to design complete systems on chip (SoC) without the need of external components. This gives the advantage of increased reliability and results in less cost over large scale production. The design of these systems for biomedical needs faces three main challenges, low power needs, noise sensitivity and low frequency operation [5]. The following subsections will give an overview about these problems and some suggested solutions being proposed in the literature.

#### **2.1.1 LOW FREQUENCY NATURE**

The bioelectronics signals are naturally low frequency signals in the range of few hertz to few kilo-hertz (Figure 1.2) and hence low cutoff frequency filters are needed. Several solutions were suggested to implement very low frequency filters [6]-[18]. Low frequency switched capacitor (SC) filters are suitable for integration [6]-[8]. But they generate switching noise hindering their use in most applications. The use of high-frequency switches makes SC filter unattractive for delicate analog environment. Also, a continuous-time anti aliasing filter is usually required before the SC filter to eliminate any undesired (out-of-band) energy that could alias into the baseband as a result of sampling. Operational trans-conductance amplifier (OTA) based filters [9]-[13] have

been designed using current mirrors, current cancellation technique or triode biased transistors. Also, all of these filters suffer from low dynamic range limited by the linearity of the trans-conductors particularly for low supply voltages [15]. These problems are overcome by the operational amplifier (Op-Amp) based filter presented in [14]. But the solution of [14] has several disadvantages. First, the circuit uses 10 Op-Amps and more than 25 resistors to realize a second order section. Thus the power consumption is expected to be large and the circuit will take large chip area. Second, the filter does not exhibit programmable feature and therefore it is not suitable for IC implementation since RC time constants can vary as high as 50% [15]. The filter in [16] uses a novel approach of chopper stabilization (CHS) for low frequency filtering, which has been the technique of flicker-noise reduction, to reject the power line interference. In this approach the power line interference is filtered at a much higher frequency band. The output chopper demodulates them back to the baseband after filtering. This approach reduces the capacitor values by a huge amount. But it suffers from the common problem of spikes, generated due to the chopping technique [17].

Another novel technique used for low frequency applications is current steering technique [18]. This technique can achieve very low cutoff frequencies, and results in very simple design. Although, it is effective in capacitance reduction, the current steering transistors exhibit a nonlinear effect, as it suffers from the linearity problem with the decrease in frequency. A summary of various filters performance is presented in Table II

**Table II: Summary of various filters used for biomedical applications.**

| Reference      | [6]                     | [11]        | [12]            | [13]            | [16]                    | [18]                      |
|----------------|-------------------------|-------------|-----------------|-----------------|-------------------------|---------------------------|
| Technology     | 2 $\mu$ m BiCMOS        | NA          | 0.35 $\mu$ CMOS | 0.35 $\mu$ CMOS | 90nm CMOS               | 0.35 $\mu$ CMOS           |
| Structure      | SC                      | Gm-C        | Gm-C            | Gm-C            | Chopper                 | Op-Amp (Current Steering) |
| Type           | LPN                     | LP          | LPN             | LP              | Notch                   | LP                        |
| Order          | 2                       | 3           | 5               | 2               | NA                      | 2                         |
| Application    | Power Line Interference | General     | EEG             | General         | Power Line Interference | Heart Rate                |
| Pole frequency | 31.4Hz/<br>50.2Hz       | 10 Hz       | 30-67Hz         | 3.8 Hz          | 50/60 Hz                | 18Hz                      |
| Power          | 58 $\mu$ W              | 15 $\mu$ W  | 11 $\mu$ W      | 96.5nW          | 75 $\mu$ W              | N/A                       |
| Supply Voltage | NA                      | $\pm$ 1.5 V | $\pm$ 1.5 V     | 1.5 V           | 3 V                     | 3 V                       |
| Dynamic Range  | NA                      | 62 dB       | -50dB (THD)     | NA              | NA                      | 40dB                      |

### 2.1.2 WEAK SIGNALS

The amplitude of these signals, physiological signals, is relatively small that spans from a few micro-volts to milli-volts and hence a good noise performance is needed. There are many techniques have been used to tackle this problem. Examples include Chopper stabilization technique (CHS), input device optimization technique and auto zeroing technique (AZ) [19]. In CHS, the signal is modulated to a higher frequency where no  $1/f$  noise before the amplification then demodulated back to the baseband. This

approach suffers from the charge injection which causes dc offset in the output and spikes caused by the clock. The AZ technique was introduced to give a better performance than CHS technique. The basic principle of AZ technique is subtracting the sampled noise and offset during the sampling phase from the instantaneous value of the input. So, the noise and offset is removed and only the amplified signal is present for further processing. This technique, however, increases the presence of white noise component in the output. In general, analog IC designers tend to avoid using clocks as they have two main problems; the charge injection mentioned earlier and the clock feed through [20].

### **2.1.3 LOW POWER NEEDS**

The system should exhibit low power consumption, especially the implanted systems because it is hard to repower the implanted chips. Not only that, but also to reduce the amount of dissipated heat which may cause problems to the surrounding tissues. Many approaches have been proposed to overcome this problem. One approach is to bias the transistors in sub-threshold region where  $V_{GS}$  less than  $V_{th}$  is needed and hence low power design can be achieved. Sub-threshold region also called weak inversion operation circuit was firstly proposed in 1970s [21]. In this technique when  $V_{GS}$  of the transistor drops below the threshold voltage  $V_{th}$  a small current is measured, however this current should be ideally zero. Interestingly, it was found that this drift current and the gate to source voltage are characterized by an exponential relation and as a result MOSFET working in sub-threshold acts like bipolar junction transistor (BJT) with low power consumption. More details about this methodology are present in section 4.2.

Another approach is to lower the supply voltage by lowering the threshold voltage which is a process dependent, through some techniques, like the bulk-driven MOSFET [22] and the floating gate MOSFET [23]. In both techniques, special design considerations different than normal MOS transistor should be taken in account.

## 2.2 RESEARCH GOALS

Developments of programmable very low frequency continuous time filters for biomedical applications are investigated. The dynamic range of the filter must be as high as possible so that the performance of the application using this filter is not degraded. Table III provides a comparison between the widely used different circuit design techniques. The purpose of this work is to investigate new circuit technique to achieve the implementation of power efficient, high dynamic range (DR), and small area continuous time filters.

**Table III: General performance comparison of various structures.**

|                   | SC       | $G_m$ -C | Active-RC                       |
|-------------------|----------|----------|---------------------------------|
| IC Implementation | Possible | Possible | Impossible for conventional one |
| Power             | Low      | Low      | Low                             |
| Linearity         | Good     | Poor     | Good                            |
| Switching-Noise   | Yes      | No       | No                              |
| Programmability   | Yes      | Yes      | No                              |

Based on Table III, switched-capacitor (SC) technique is very attractive. But it suffers from unavoidable switching noise coming from the clocks and usually unsuitable

for delicate biomedical applications. On the other hand, the main problem with Gm-C filters is their limited linearity. This makes the active-RC filters based on Op-Amp the most attractive candidate. Active-RC filters can achieve high dynamic ranges. In fact, active-RC filters are designed based on the larger open-loop gain of Op-Amps and closed-loop configurations. The larger the open-loop gain of Op-Amps, the better is the filter linearity. Since the frequency of operation is low therefore the Op-Amp will not suffer from the gain bandwidth product problem and hence can provide high gain for optimum linearity.

This thesis investigates and proposes some techniques to implement such very low frequency biomedical filters in analog CMOS integrated circuits (ICs). Implementation of such filters in a relatively small silicon area while exhibiting high linearity and low power consumption will promote the utilization of very large-scale integration (VLSI) techniques in biomedical instrumentations.

Four different CMOS active-RC circuit techniques for implementing these filters such as low pass filters for ECG are studied and can be categorized as two groups. The first group is resistor replacing in which two techniques are proposed to realize the high resistance on chip, namely Antonio simulated inductance technique and R-2R ladder technique. The other two techniques can be grouped under the frequency scaling approach. One of them proposes applying the difference term technique which has been used to realize very low frequency oscillators to scale down the frequency through introducing a difference term in the pole frequency. The other technique proposes a CFOA based filter with current and voltage attenuators to scale down the frequency.

## 3. LOW FREQUENCY FILTERS TECHNIQUES

### 3.1 INTRODUCTION

Filters can be realized using different techniques. One of the most used techniques is active RC which simply uses resistors and capacitors with an active element(s), commonly operational amplifier, to realize filters following different topologies, for instance Sallen Key, Tow Thomas and Kerwin-Huelsman-Newcomb filters.

Conventionally, huge external resistors are used to realize low frequency filters. Nowadays, people think of integrating all the components of such filters in one single chip and hence the presence of these huge resistances should be resolved to permit integration. Two circuit elements are considered to provide possible solutions to the integration problem of active-RC filters namely R-2R ladders and the *Antoniou* inductance simulating circuit. In the following subsections 3.2 and 3.3, a deep discussion over these solutions is presented. Another technique applying the difference term approach to the filters is presented in section 3.4. Final possible solution using CFOA is studied in section 3.5.



### 3.2 ANTONIO SIMULATED INDUCTANCE TECHNIQUE

The first proposed solution is to use inductor simulation circuits. These circuits are traditionally used for simulating an inductor to permit inductor integration, but this work investigates their utilizations as capacitance or resistance scaling. Impedance scaling circuits can provide large time constants and therefore can be a suitable candidate for low frequency filters. For example, the Antoniou inductance-simulation circuit [24] shown in Figure 3.1 has an input impedance of:

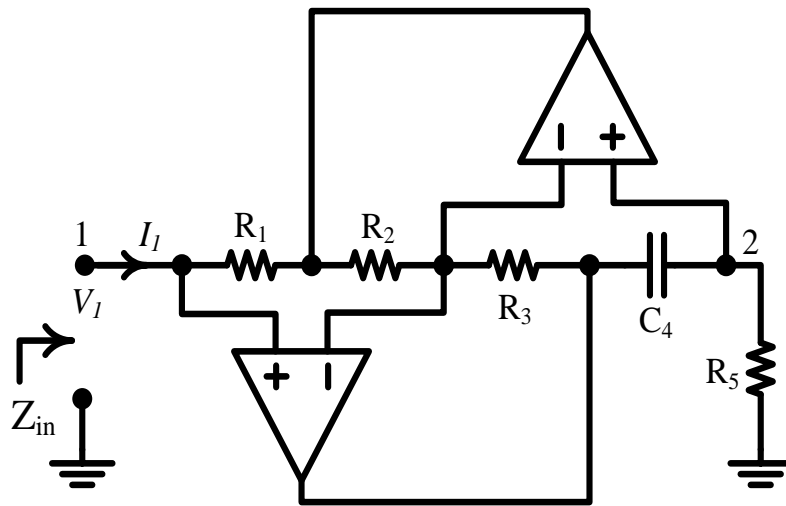
$$Z_{in} = \frac{V_1}{I_1} = \frac{sC_4R_1R_3R_5}{R_2} \quad (1)$$

which is that of an inductance  $L$  given by:

$$L = \frac{C_4R_1R_3R_5}{R_2} \quad (2)$$

Replacing  $C_4$  by another resistor  $R_4$ ,  $Z_{in}$  becomes:

$$Z_{in} = \frac{R_1R_3R_5}{R_2R_4} \quad (3)$$



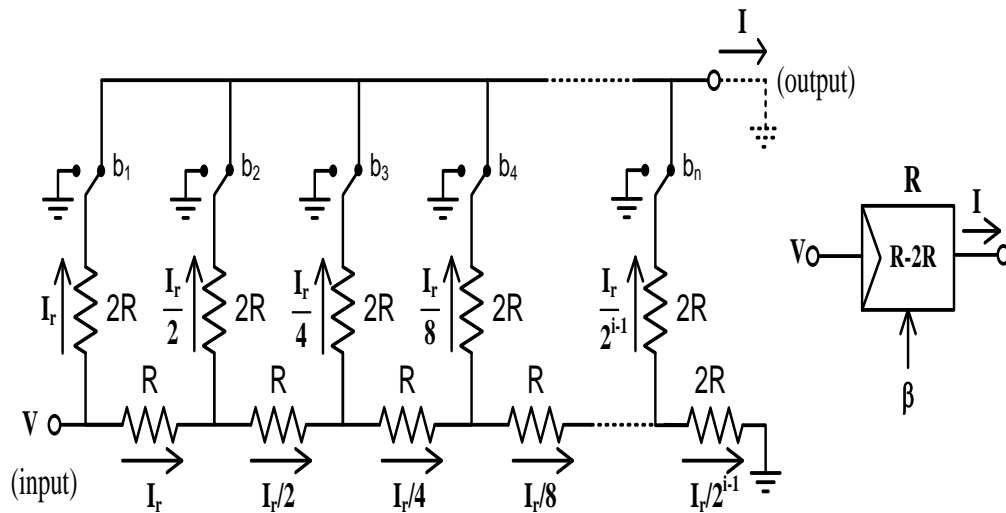
**Figure 3.1: The Antoniou inductance simulation circuit.**

Therefore, it can be seen that a very large equivalent resistance can be obtained by proper selection of the five resistor values. For instance, selecting  $R_1=R_3=R_5=10\text{k}\Omega$  and  $R_2=R_4=0.1\text{k}\Omega$ , then this circuit simulates a  $100\text{M}\Omega$  resistor, while actually using total actual resistance of approximately  $30\text{k}\Omega$ .

This is indeed a good solution from area optimization point of view. But unfortunately, this technique suffers from high power consumption where two operation amplifiers are needed for each single resistor. In other words, to realize a 2<sup>nd</sup> Tow Thomas low pass filter 10 Op-Amps are needed.

### 3.3 R-2R LADDER TECHNIQUE

R-2R ladder is widely used in realizing analog to digital converters (ADC). In this study, R-2R ladder will be used as a digitally programmable resistor and it will be incorporated to provide huge resistance as the number of bits increased. The non-ideal effects of this approach are studied with deep discussion about choosing the right index (1, 2 or 0.5) for our circuit. The R-2R ladder shown in Figure 3.2 can be considered as a digitally programmable resistor [25].



**Figure 3.2: Digitally controlled R-2R ladder.**

It can be seen from Figure 3.2 that the output current ( $I$ ) is given by:

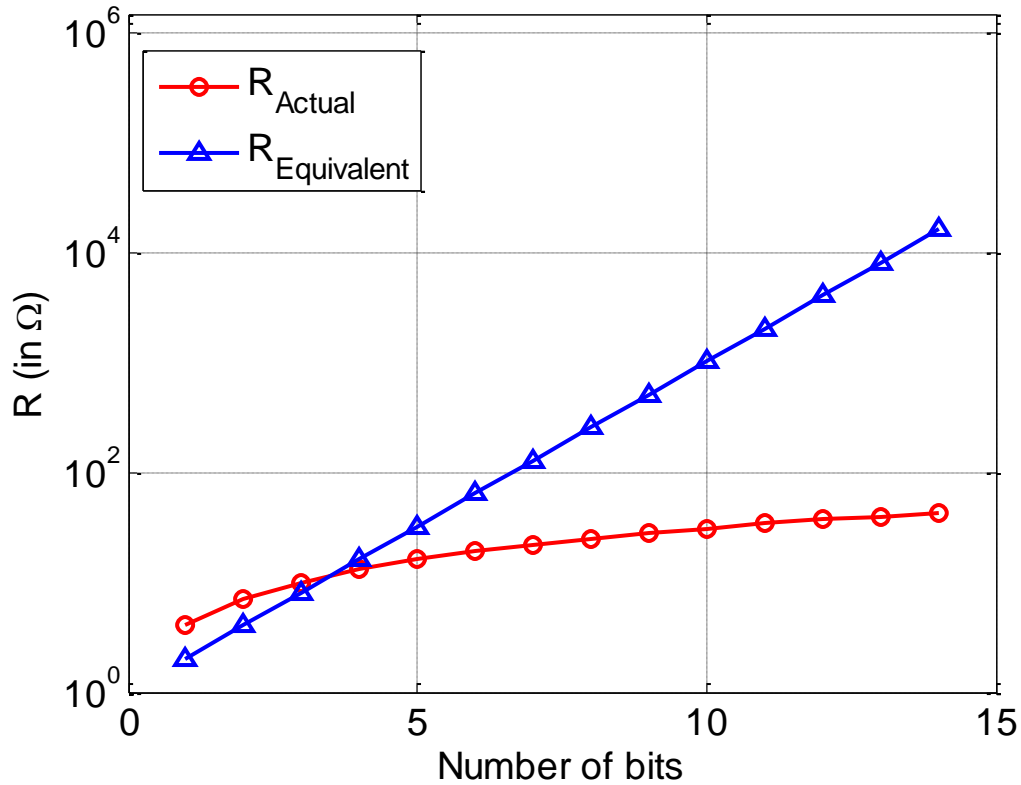
$$I = \sum_{i=1}^n \frac{b_i I_r}{2^{i-1}} \quad \text{where } I = \frac{V}{2R} \quad (4)$$

Therefore, the equivalent resistance, seen between the input and output nodes, is given by:

$$R_{eq} = \frac{V}{I} = \beta R \quad \text{where} \quad \beta = \frac{1}{\sum_{i=1}^n b_i 2^{-i}} \quad (5)$$

where  $b_i$ , equaling 0 or 1, is the  $i^{th}$  bit in an  $n$  bit digital control word.

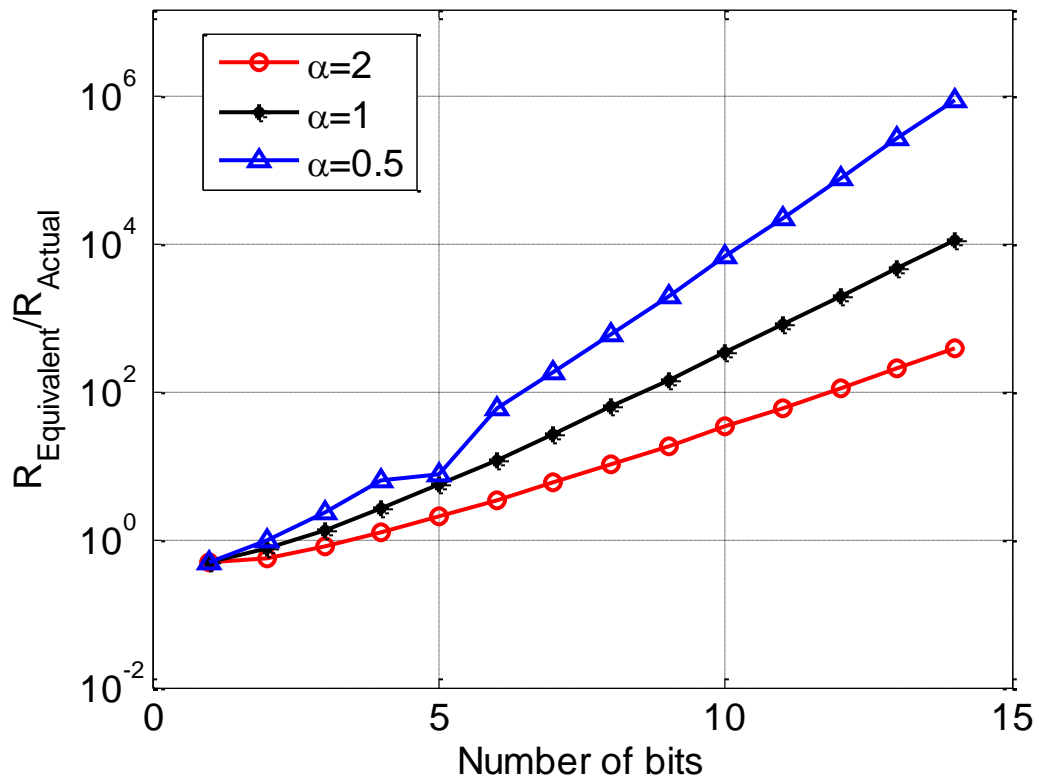
It can be observed that a large R-2R ladder equivalent resistance can be achieved using a relatively small passive resistance. For example, for a 10 bit R-2R ladder with  $R=10\text{k}\Omega$ , equivalent resistance as high as  $10\text{M}\Omega$  can be achieved while requiring an actual resistance of only  $300\text{k}\Omega$ . Figure 3.3 compares the value of the equivalent resistance and the actual value on the chip for different number of bits. It can be concluded that using R-2R ladder to emulate high resistance value will save the area on the chip, save more power and introduce less noisy design.



**Figure 3.3: The total and equivalent resistances for R-2R vs. number of bits.**

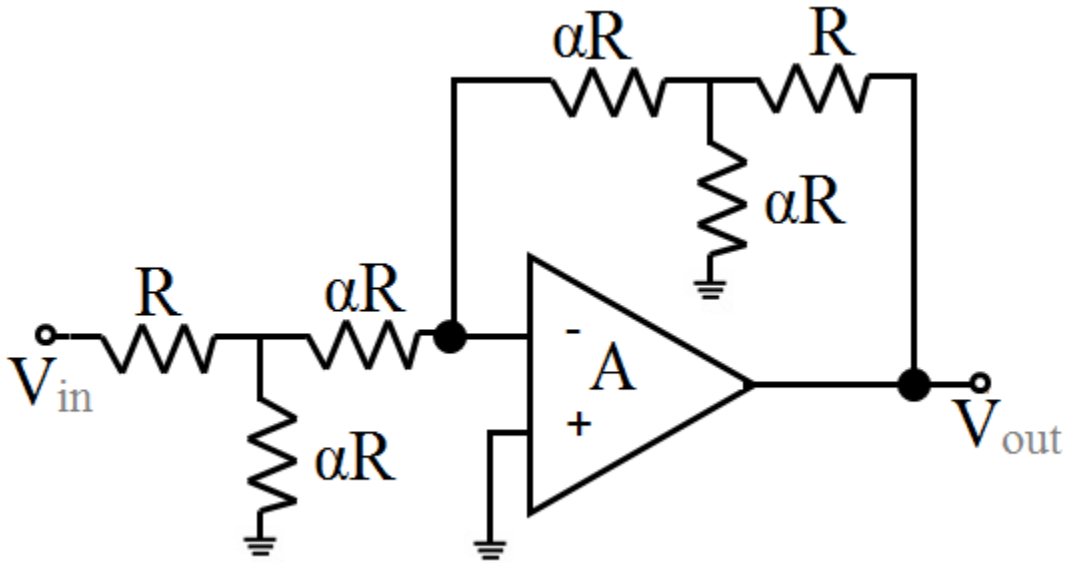
R-2R ladders will replace the passive resistors determining the pole frequency of the filters to achieve very low frequency characteristic using relatively small silicon resistors. This can be applied as long as these resistors are connected to virtual ground, which simulates the proper operating condition of the R-2R ladder.

R-2R is chosen in ADC because it provides weighted values of resistance ( $R, 4R, 8R \dots 2^n R$ ) which is essential to fulfill the requirements of ADC algorithms. In the other hand, such algorithm is not important when this approach is implemented to simulate high resistance. It can be seen clearly from Figure 3.4 that as the index decreased the actual resistance on the chip decreased and the equivalent resistance increased for the same number of bits and hence less area consumption is achieved. This was the starting point to think differently and raise a question why not to try to play with the index,  $\alpha$ , i.e make it 1 or  $\frac{1}{2}$  instead of 2, to get the optimum solution for achieving less area consumption. From Area consumption perspective, we can claim that  $R - (\frac{1}{2})R$  is the best solution because as number of bits increases, it provides a huge resistance with less resistance on chip.



**Figure 3.4: The ratio of the equivalent resistance to the actual one for  $\alpha=0.5$ ,  $\alpha=1$  and  $\alpha=2$ .**

Theoretical analysis is very important to track the effect of increasing/decreasing the index and number of bits of  $R-\alpha R$  ladder on the circuit performance. Non-ideal analysis is done using the circuit in Figure 3.5, with 2-bits  $R-\alpha R$  networks acting as normal resistances.

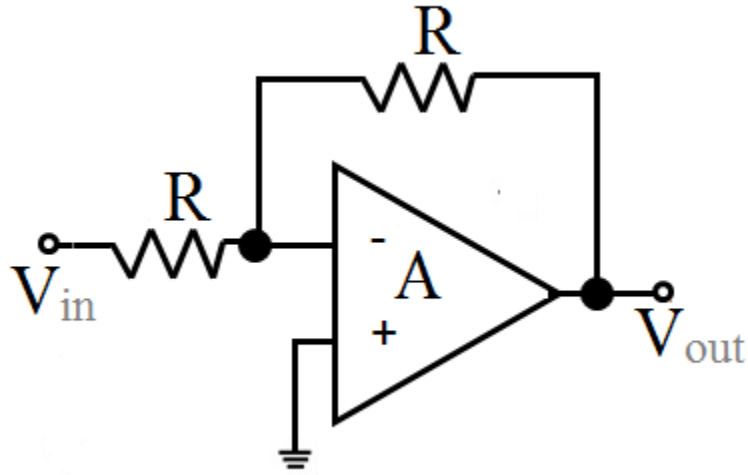


**Figure 3.5: Finite gain Op-Amp based amplifier with R- $\alpha$ R networks.**

Applying Kirchhoff Current Law (KCL) at the inverting node of the Op-Amp and other nodes leads to the following transfer function:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = - \left( \frac{1}{1 + \frac{2(\alpha+1)}{\alpha A}} \right) \quad (6)$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \begin{cases} - \left( \frac{1}{1 + \frac{3}{A}} \right) ; \text{ for } \alpha = 2 \\ - \left( \frac{1}{1 + \frac{4}{A}} \right) ; \text{ for } \alpha = 1 \\ - \left( \frac{1}{1 + \frac{6}{A}} \right) ; \text{ for } \alpha = \frac{1}{2} \end{cases} \quad (7)$$



**Figure 3.6: Finite gain Op-Amp based amplifier.**

For normal Op-Amp based amplifier shown in Figure 3.6, the given is given by:

$$\frac{v_{out}}{v_{in}} = - \left( \frac{1}{1 + \frac{2}{A}} \right) \quad (8)$$

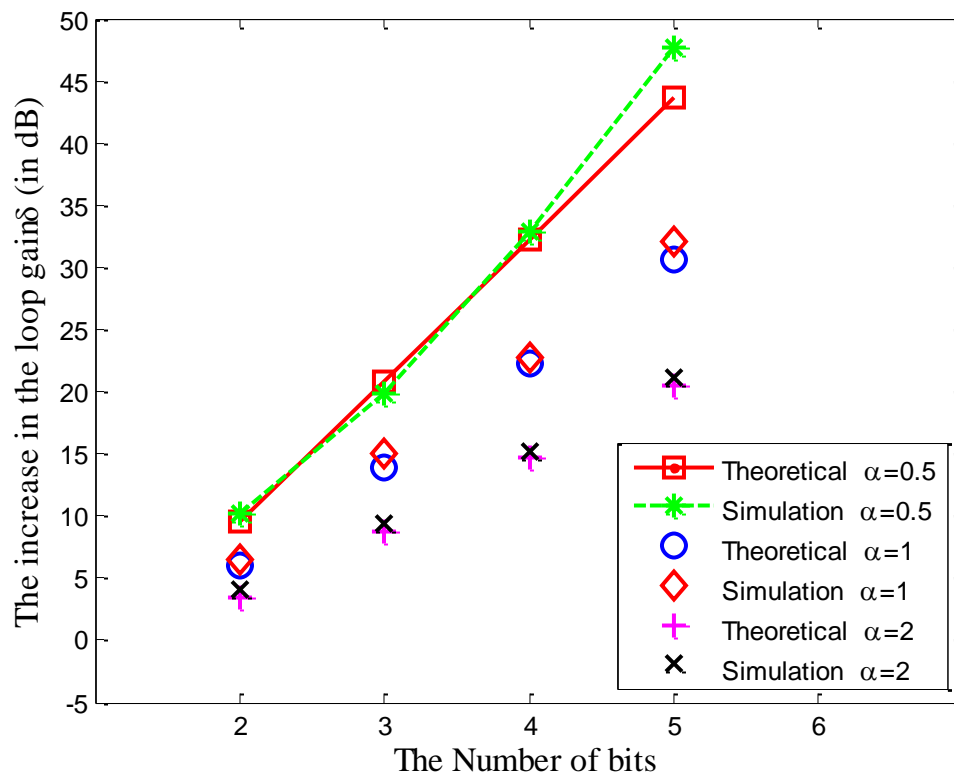
It can be seen clearly that the index of R- $\alpha$ R ladder affects the performance of the circuit. An increase in the open loop gain of the Op-Amp should be ensured to have the same gain performance as the normal resistance in equation (8). Hence the circuit consumes more power. It was also found that as the number of bits of R- $\alpha$ R network increases more open loop gain is needed.

$$A = \begin{cases} A_o + 5 & \text{dB; for } \alpha = 2 \\ A_o + 7.5 & \text{dB; for } \alpha = 1 \\ A_o + 10 & \text{dB; for } \alpha = \frac{1}{2} \end{cases} \quad (9)$$

where A is the new open loop gain and  $A_o$  is the initial open loop gain of the Op-Amp.



SPICE simulation for different number of R- $\alpha$ R networks using ideal Op-Amp was conducted. It was found that as the index  $\alpha$  decreases and the number of bits increases, more open loop gain value of the Op-Amp is needed to have the same performance matching our analysis and expectation, Figure 3.7.



**Figure 3.7: Simulation vs. theoretical results for the open loop gain increase.**

Figure 3.7 illustrates also that for a specific index value,  $\alpha=2$  for example, the increase in the loop gain ( $\delta$ ) is almost (+5 dB) for each increase in the number of bits with some error. Following the same pattern, a general relation between the increase in the open loop gain ( $\delta$ ), index ( $\alpha$ ) and number of bits ( $n$ ) can be obtained as follows:

$$\delta(\text{dB}) = \begin{cases} 5(n - 1) \pm \varepsilon ; \text{ for } \alpha = 2 \\ 7.5(n - 1) \pm \varepsilon ; \text{ for } \alpha = 1 \\ 11(n - 1) \pm \varepsilon ; \text{ for } \alpha = \frac{1}{2} \end{cases} \quad (10)$$

The increase in the open loop gain requires more voltage supply. Equation (10) emphasizes the fact that as  $\alpha$  increases, more open loop gain level is needed and as a result this may requires more power. So it can be stated that  $\alpha$  is proportional to the actual resistance on the chip, *the area*, and inversely proportional to the increase in the open loop gain  $\delta$ , *power consumption*. Consequently and compared to other indices, R-2R is the best candidate from power consumption point of view as it is often more important than the area.

### 3.4 DIFFERENCE TERM TECHNIQUE

In the previous sections, two techniques to replace the huge resistors on chip were discussed. Besides that, frequency scaling techniques are investigated in this section and the following one. In this section, the difference term approach is applied to the filter to scale down the frequency and the limitation of the filter is discussed.

The typical transfer function that describes the low pass filter is given in the following equation:

$$\frac{V_o}{V_{in}} = \frac{H}{s^2 + s\left(\frac{Q}{BW}\right) + \omega^2} \quad (11)$$

where  $H$  is the gain of the filter,  $Q$  is the quality factor,  $BW$  represents the bandwidth and  $\omega$  is the corner frequency (3-dB frequency). Traditionally, the corner frequency of the low pass is given by:

$$f = \left( \frac{1}{2\pi CR} \right) \quad (12)$$

Obviously to get low frequencies in the range of few hertz to few kilo-hertz, large capacitors and resistors are needed.

One novel approach to scale down the frequency is to introduce a difference term of  $R_1$  and  $R_2$ ,  $m=R_1-R_2$ , in  $\omega$  term. So, as  $m$  decreases the frequency scaled down and very low corner frequency can be obtained. This approach has been used for realizing very low frequency oscillators 'VLFO' [26]-[28]. The challenge in this approach when applied to filters is the need to introduce difference term,  $m$ , not only in the pole frequency,  $\omega$ , but also in the *s-coefficient* term,  $\left( \frac{Q}{BW} \right)$ , to cancel the effect of  $m$  in  $Q$  and hence the quality factor can be controlled via ratio of resistors  $\frac{R_x}{R_y}$  independent of  $R_1-R_2$ . So the filter topology is modified to tackle this problem by introducing a square of the difference term,  $m^2$ , in the pole frequency and  $m$  in the *s-coefficient* term and hence the effect of  $m$  on the  $Q$  is cancelled. Also,  $m^2$  is introduced in the numerator coefficient such that the gain is not disturbed.

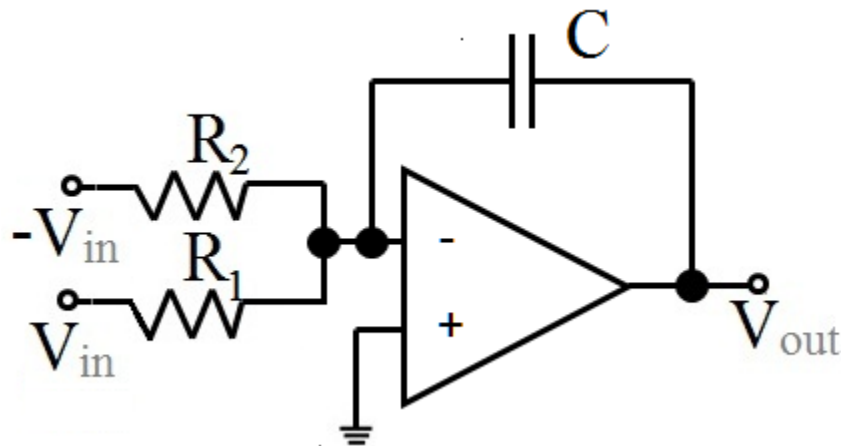


Figure 3.8: The integrator used for the difference term approach.

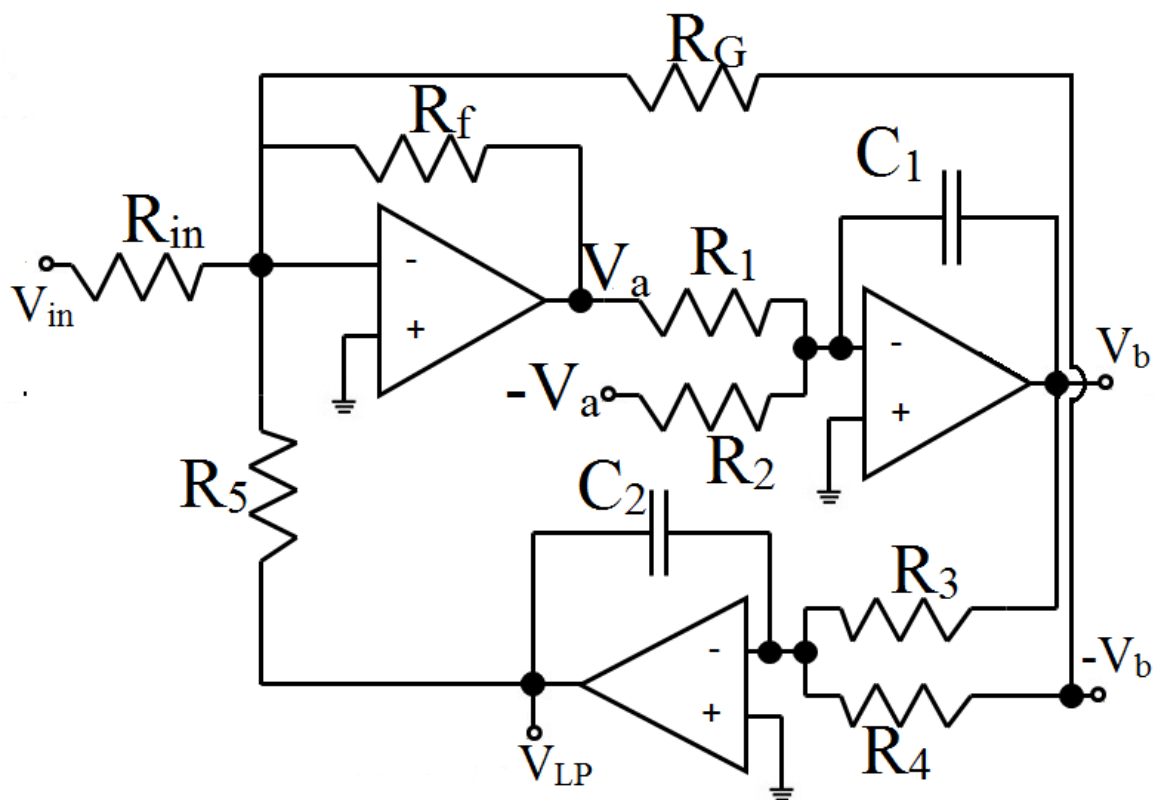


Figure 3.9: 2<sup>nd</sup> order LPF applying difference approach.

A low pass filter can be obtained using the integrator shown in Figure 3.8 in two integrator loop topology. The transfer function of the proposed filter shown in Figure 3.9 is obtained as follows:

$$\frac{V_o}{V_{in}} = \frac{\frac{R_f(R_1-R_2)(R_3-R_4)}{C_1 C_2 R_1 R_2 R_3 R_4 R_{in}}}{S^2 + S \left( \frac{R_f(R_1-R_2)}{C_2 R_1 R_2 R_G} \right) + \frac{R_f(R_1-R_2)(R_3-R_4)}{C_1 C_2 R_1 R_2 R_3 R_4 R_5}} \quad (13)$$

From the above transfer function and assuming  $R_f=R_5=R$ ,  $R_1=R_3$ ,  $R_2=R_4$  and  $C_1=C_2=C$ , we can obtain the DC gain, the corner frequency and the quality factor as follows:

$$\text{DC Gain} = \frac{R}{R_{in}} \quad (14)$$

$$Q = \frac{R_G}{R} \quad (15)$$

$$2\pi f = \frac{(R_1-R_2)}{CR_1 R_2} \quad (16)$$

In this approach, it can be seen clearly that the DC gain, the quality factor and the corner frequency can be all controlled independently, equations (14)-(16). Moreover, the corner frequency can be scaled down exploiting the presence of the difference term of resistors in the numerator. However, this technique suffers from the high sensitivity.

Sensitivity, which was introduced by Bode in 1940s, is an important issue in filter design [7]. Once a filter is designed, the sensitivity of DC gain, quality factor and the corner frequency to all the parameters should be studied and tested to verify the sustainability of the operation of this filter. The sensitivity should be as small as possible

reaching a desired value of zero which means the two elements are independent of each other. The sensitivity of a function  $\mathbf{Y}$  to the function/element  $\mathbf{x}$  is defined as follows:

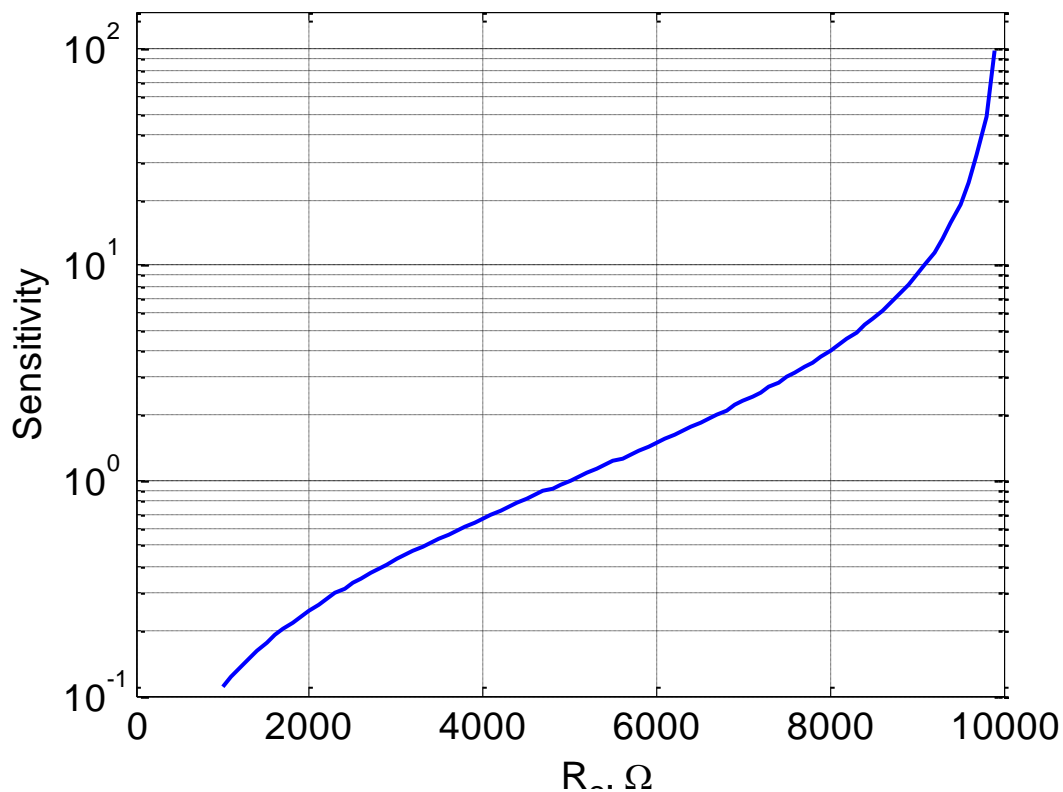
$$S_{\mathbf{x}}^{\mathbf{Y}} = \frac{\partial y}{\partial x} \left( \frac{x}{y} \right) \quad (17)$$

For the difference term approach based filter, the sensitivity for all the parameters is given below:

$$S_{R1}^Q = S_{R2}^Q = S_w^Q = 0, \quad S_{Rg}^Q = -S_R^Q = -S_{DC \text{ Gain}}^Q = 1 \quad (18)$$

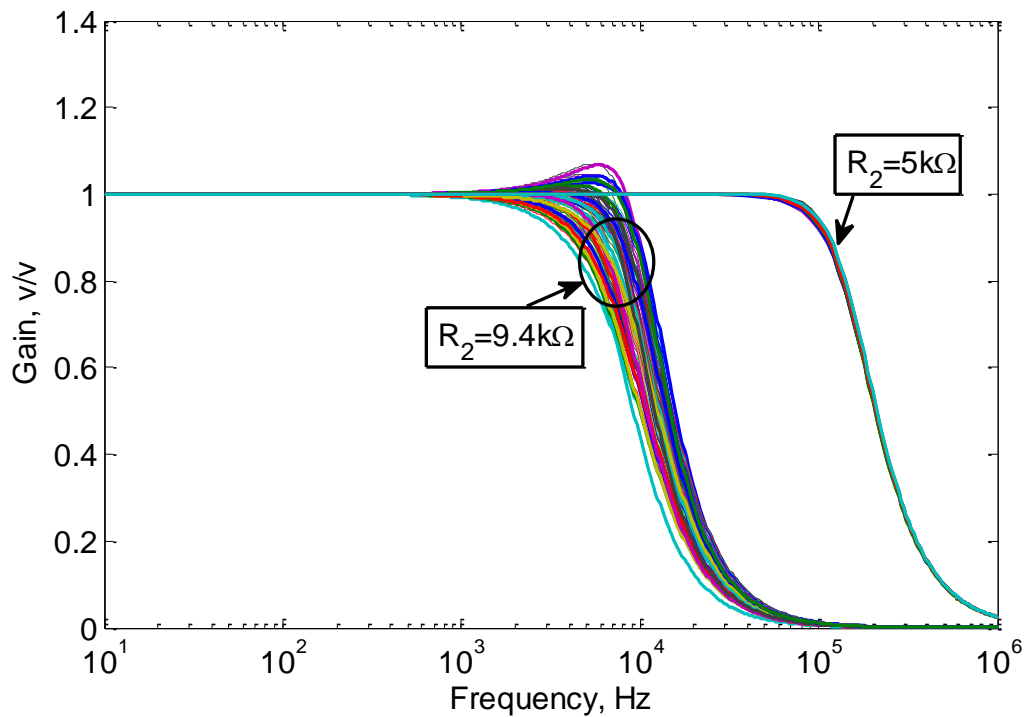
$$S_{R1}^w = \frac{R_2}{R_1 - R_2} \quad (19)$$

Unfortunately, this approach suffers from high sensitivity hitting infinity for equal resistors, equation (19). So, as the value of  $R_2$  is changed closer to the value of  $R_1$ , a bad filter performance is obtained. Figure 3.10 demonstrates that the sensitivity of the filter has reasonable values of **(0-1)** when  $R_2$  is changed from  $1k\Omega$  to  $5k\Omega$ . Otherwise, the sensitivity starts to increase dramatically heading infinity for  $R_1=R_2$ .



**Figure 3.10: The sensitivity vs.  $R_2$  ( $R_1$  is kept constant equals to  $10k\Omega$ ).**

SPICE Simulation was carried out for 2<sup>nd</sup> order low pass filter with frequency scaling technique and values of  $C=100pF$ ,  $R_1= 10k\Omega$  for different cases of  $R_2$ . Using Mont Carlo analysis, the filter has been extensively simulated for 100 runs with an applied resistance tolerance of 1% to  $R_1$  and  $R_2$  which is a practical value to check the reliability of the proposed filter.

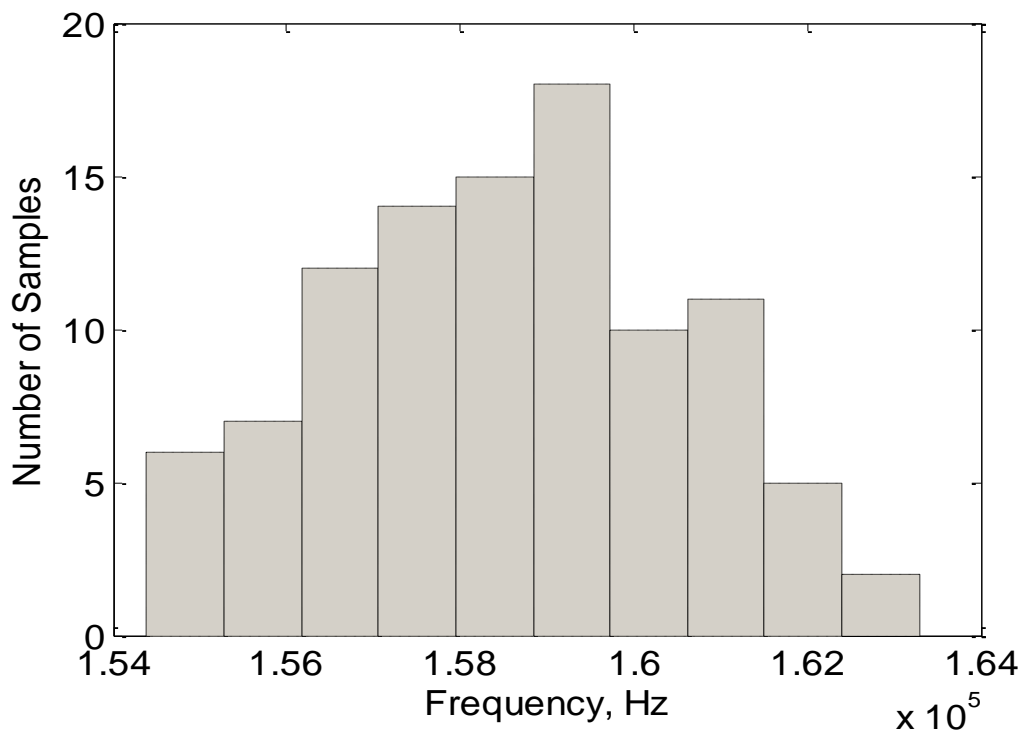


**Figure 3.11: 2<sup>nd</sup> order LPF frequency responses based on difference term technique for two cases:  $R_2=9.4\text{k}\Omega$  and  $R_2=5\text{k}\Omega$ .**

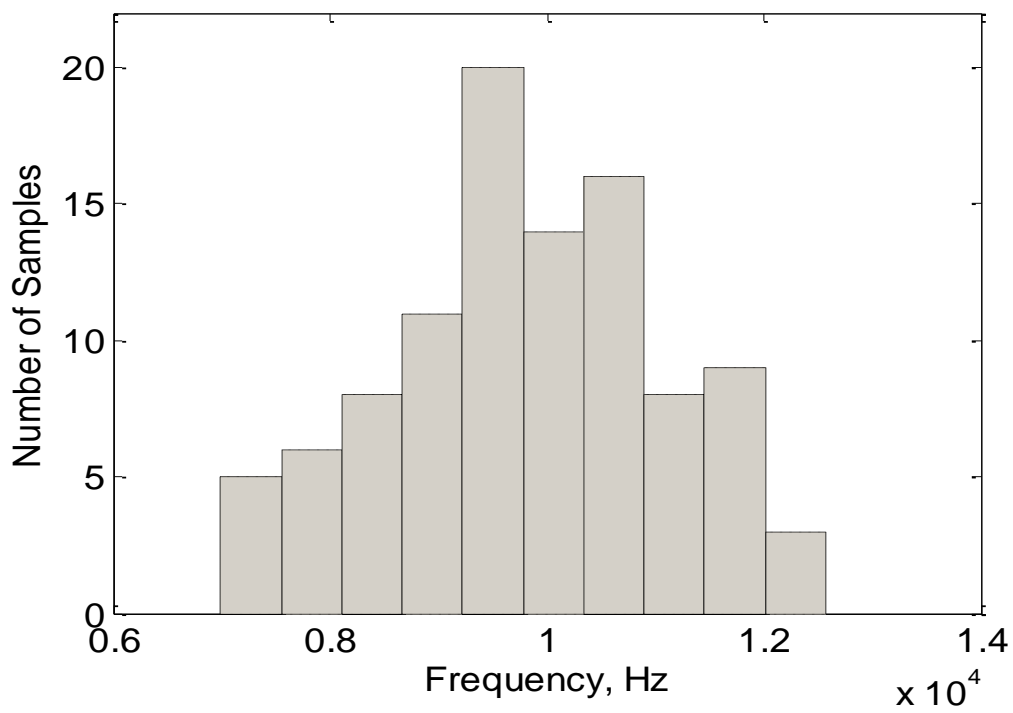
The frequency responses of two different cases, namely  $R_2=9.4\text{k}\Omega$  and  $R_2=5\text{k}\Omega$  are provided in Figure 3.11. It can be noticed that the pole frequency is scaled down from 159 kHz to approximately 9.9 kHz for  $R_2=9.4\text{k}\Omega$  by controlling only  $R_2$ .

Figure 3.12 and Figure 3.13 show the histogram of the two different cases,  $R_2=5\text{ k}\Omega$  and  $R_2=9.4\text{k}\Omega$ , which represents the distribution of the samples over a range of frequency. In other words, this figure presents the probability of the design to meet the required corner frequency. Table IV summaries the results obtained from the conducted simulation and percentage of error.





**Figure 3.12:** The frequency bandwidth histogram when  $R_2=5\text{k}\Omega$ .



**Figure 3.13:** The frequency bandwidth histogram when  $R_2=9.4\text{k}\Omega$ .

**Table IV : Summary of Monte Carlo simulation results.**

| R <sub>2</sub> (kΩ) | Number of Bit Reduction, n | Pole Frequency (Theoretical, kHz) | Pole Frequency (MC simulation, kHz) |        |        | Deviation from Nominal value (Tuning) |
|---------------------|----------------------------|-----------------------------------|-------------------------------------|--------|--------|---------------------------------------|
|                     |                            |                                   | Range                               |        | Mean   |                                       |
|                     |                            |                                   | Min.                                | Max.   |        |                                       |
| 1                   | NA                         | 1432.4                            | 1413.5                              | 1446.3 | 1428.1 | 1.33%                                 |
| 5                   | NA                         | 159.2                             | 154.4                               | 163.6  | 159    | 3%                                    |
| 8.9                 | 3 bits                     | 19.9                              | 16.6                                | 22.8   | 19.6   | 16%                                   |
| 9.4                 | 4 bits                     | 9.9                               | 6.7                                 | 12.7   | 9.6    | 33%                                   |
| 9.7                 | 5 bits                     | 4.97                              | 1.7                                 | 7.5    | 4.6    | 65%                                   |
| 9.85                | 6 bits                     | 2.5                               | 0.2                                 | 4.8    | 2      | 92%                                   |

It can be interfered from Table IV that this technique can be used to scale down the pole frequency. Table IV demonstrates also the range and the mean values of the pole frequency of the simulated filter. It can be seen that the mean values are close to the theoretical ones in most of the cases. The tuning values indicate the percentage of tuning needed to maintain a yield of 1, i.e all samples are working in range.

Capacitor arrays can be incorporated to introduce a tuning in the pole frequency. A 5-bit pole frequency reduction can be realized as indicated in Table IV by maintaining a 65% pole tuning and a 6-bit reduction if a 92% tuning is allowed. This is indeed a huge range of tuning, however, if the yield is relaxed, low range of scaling can be obtained. For example, 5-bit reduction can be used with 30% of tuning but the yield decreased to

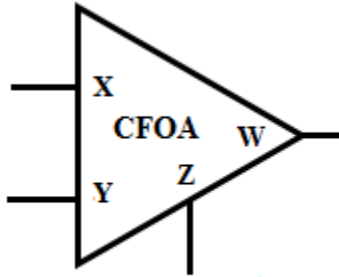
0.76 instead of 1. Practically, 33% tuning is achievable through capacitor arrays and thus 4-bit case is the best choice to keep the yield as maximum as one.

To conclude, the above analysis shows that the difference term approach can be used to introduce a 4-bit reduction in the pole frequency given that 33% tuning is maintained, but this is alone not suitable for biomedical filters. In the integrated biomedical filters and in some application, a reduction in the frequency of more than 10 bits is needed to realize very low frequency operation to avoid using huge values of resistors and capacitors. Nevertheless, this technique can be integrated with other techniques, R-2R ladder for example, to relax the number of bits and hence power consumption is reduced and the area can be optimized.

### 3.5 CURRENT ATTENUATOR TECHNIQUE

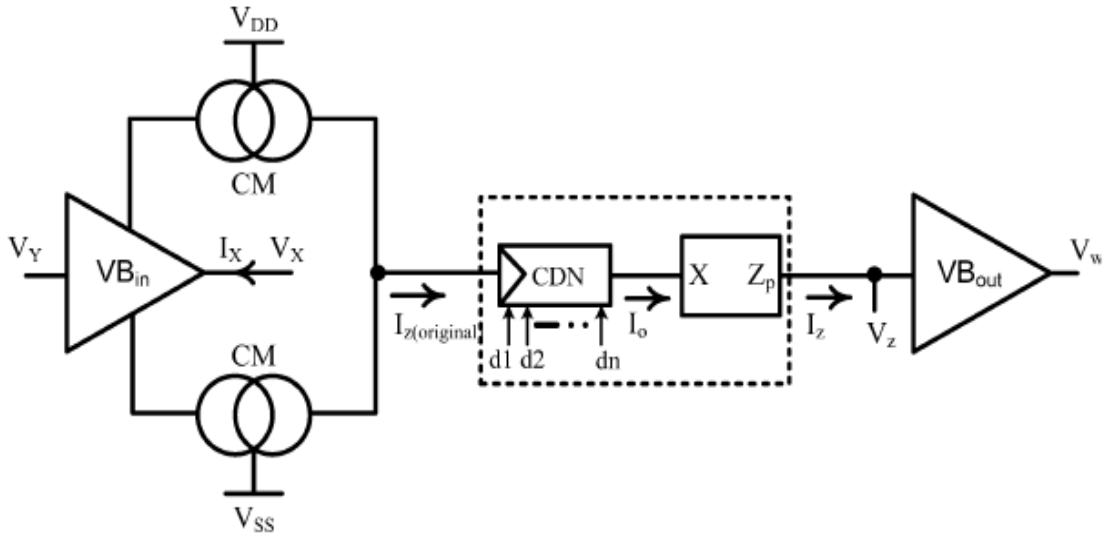
The forth proposed technique can achieve very low frequency through using current and voltage attenuators employed inherently in the current feedback operational amplifier. The Current feedback operational amplifier (CFOA) is one of the most widely used devices in analog current mode circuits which is attracting researcher due to the simplicity it provides to realize some circuit operations such as addition. CFOA shown in Figure 3.14 is a four terminal device characterized by the following matrix:

$$\begin{bmatrix} I_Y \\ I_Z \\ V_X \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (20)$$



**Figure 3.14: The current feedback operational amplifier block diagram.**

Unlike the operational amplifier (Op-Amp), CFOA does not suffer from the gain bandwidth product and as such has a high bandwidth compared to the Op-Amp and also has high slew rate. On the other hand, this device, CFOA, is not programmable and hence it is not good for IC design where tuning feature is crucial. A programmable CFOA is proposed in [29] which is achieved by inserting a current division network (CDN) between the **Z** and **W** terminals to allow a digital control over the current gain,  $I_z = \alpha I_x$ , of the CFOA shown Figure 3.15 and by which a current attenuation can be achieved making  $\alpha < 1$ . Also another current follower (CF) is added to maintain the proper operation of CDN which requires one of its terminals to be virtually grounded. In addition to that, the current follower is needed to provide high output impedance.



**Figure 3.15: Programmable CFOA.**

The proposed filter in [29] achieves high tuning range 200kHz to 8MHz by controlling  $\alpha$  which is given as follows:

$$\alpha = \left( \sum_{i=1}^n d_i 2^{-i} \right) \quad (21)$$

where  $n$  is the size of the control word and  $d_i$  is the  $i$ th digital bit.

To realize very low frequency operation, very low  $\alpha$  value should be used which results in increasing the number of current division network bits. Another way of doing it is to employ two voltage attenuators inside the CFOA instead of the normal buffers providing the following characteristics:

$$\begin{bmatrix} I_Y \\ I_Z \\ V_X \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \alpha & 0 & 0 \\ \beta & 0 & 0 & 0 \\ 0 & 0 & \gamma & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (22)$$

where  $\alpha$ ,  $\beta$  and  $\gamma$  are the attenuation factors,  $I_X/I_Z$ ,  $V_X/V_Y$  and  $V_W/V_Z$  respectively.

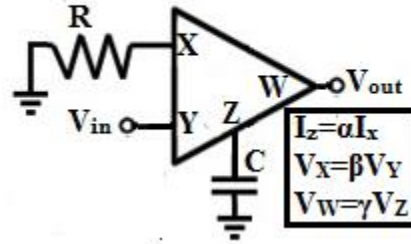


Figure 3.16: CFOA based integrator.

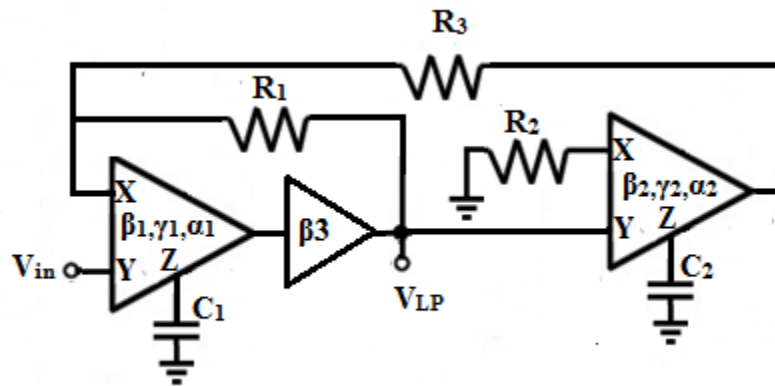


Figure 3.17: 2<sup>nd</sup> order CFOA with voltage attenuators (VA) based LPF.

Using the modified version of CFOA, a simple integrator can be realized using the circuit in Figure 3.16. The proposed low pass filter shown in Figure 3.17 is implemented using two integrator loop topology. A third voltage attenuator is placed between the **W** terminal of the first CFOA before the local feedback and the **Y** terminal of the second CFOA to provide more control over the quality factor and the corner frequency as illustrated in equations (24)-(26). The transfer function of this filter is given as follows:

$$\frac{V_o}{V_{in}} = \frac{\alpha_1 \alpha_2 \gamma_1 \gamma_2 \beta_1 \beta_2 \beta_3 (R_1 + R_3)}{C_1 C_2 R_1 R_2 R_3} \frac{1}{s^2 + \left[ \frac{\alpha_1 \gamma_1 \beta_3}{C_1 R_1} \right] s + \frac{\alpha_1 \alpha_2 \gamma_1 \gamma_2 \beta_2 \beta_3}{C_1 C_2 R_2 R_3}} \quad (23)$$

By routine analysis the dc gain, corner frequency and the quality factor of the proposed filter can be described in the following equations:

$$\text{DC Gain} = \frac{\beta_1(R_1+R_3)}{R_1} \quad (24)$$

$$Q = R_1 \sqrt{\frac{(\alpha_2 \gamma_2 \beta_2) C_1}{(\alpha_1 \gamma_1 \beta_3) C_2 R_2 R_3}} \quad (25)$$

$$\omega_0 = \sqrt{\frac{\alpha_1 \alpha_2 \gamma_1 \gamma_2 \beta_2 \beta_3}{C_1 C_2 R_2 R_3}} \quad (26)$$

So these components can be carefully selected as follows:  $R_1=R_2=R_3=R$  and  $C_1=C_2=C$  to allow digital tuning for all the parameters and it can be also noticed that the quality factor and the pole frequency can be all controlled independently by adjusting the  $\alpha_1, \alpha_2, \gamma_1, \gamma_2$  and/or  $\beta_2, \beta_3$  simultaneously.

The main disadvantage of this technique is the high power consumption because to realize second order low pass filter, five voltage attenuators and two current attenuators are needed compared to only two Op-Amps in the R-2R ladder approach. To conclude this is indeed a good technique to provide a huge range frequency tuning but it is power hungry.

## 4. DESIGN AND SIMULATION RESULTS

### 4.1 INTRODUCTION

The design of an integrated time continuous very low frequency filter is not straightforward. That is because three crucial design methods must simultaneously be adopted during the design phase. First, the design must adopt low frequency design technique to realize the extra-large time constants of the filter. Second, low power design methods must be incorporated to reduce amount of heat, decrease battery size and increase batteries life. Third, the filter must exhibit better linearity. As previously mentioned, active-RC approach inherently has superior linearity and hence we are left with the first two requirements which are finding methods to implement extra-large time constant and fulfilling the low power specifications.

It must be observed that the techniques that would be adopted to achieve large time constants must preserve the high linearity of the active-RC approach while maintaining low power and occupying small chip area. In this work, one solution that satisfies these features is proposed which is the R-2R ladder. This network consumes no standby power. Therefore, the overall power consumption of the filter will be decided by the number of active elements and their individual power consumption.



## 4.2 OP-AMP SELECTION

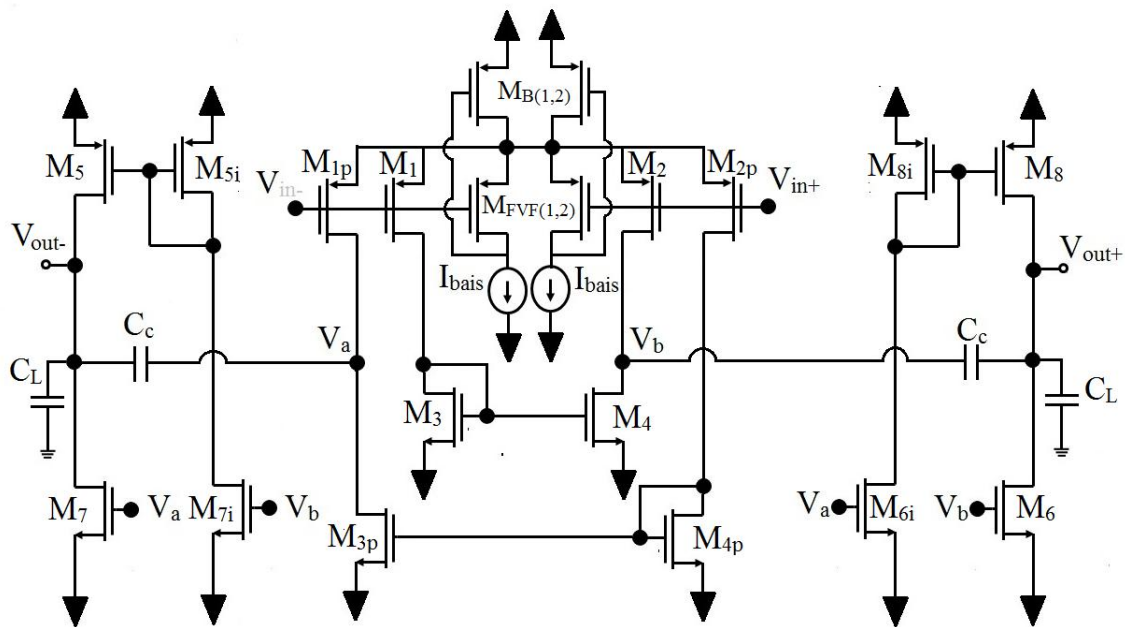
Op-Amp serves as the basic building block for most of the analog circuits such as filters. Low power and high gain performance are considered the two key factors to select the suitable Op-Amp for the proposed filter. Various Op-Amps performance is presented in Table V [6],[30]-[32] and they are selected upon the mentioned two criteria.

**Table V: Comparison between four different Op-Amps.**

| Reference            | [6]                | [30]                 | [31]                 | [32]                 |
|----------------------|--------------------|----------------------|----------------------|----------------------|
| Technology           | 2 $\mu$ m<br>BiMOS | 0.18 $\mu$ m<br>CMOS | 0.35 $\mu$ m<br>CMOS | 0.35 $\mu$ m<br>CMOS |
| Power consumption    | 29 $\mu$ W         | 20.1 $\mu$ W         | 200nW                | 33nW                 |
| Gain                 | 80 dB              | 85 dB                | 80 dB                | 90 dB                |
| Unity Gain Bandwidth | 30 kHz             | 5.5 MHz              | 42 kHz               | 30 kHz               |
| Supply voltage       | NA                 | $\pm$ 0.6 v          | 0.9 V                | 1.2v                 |
| Phase Margin         | 86 $^{\circ}$      | 89.39 $^{\circ}$     | 50 $^{\circ}$        | NA                   |

Op-Amps proposed in [6] and [30] consume high power compared to the others, i.e 29 $\mu$ W and 20 $\mu$ W compared to 200nW and 33nW. Moreover, the Op-Amp presented in [6] is implemented using BiCMOS which is a costly process and also suffers from switching noise as it employs the switching capacitor technique. On the other hand, Op-Amp presented in [30] provides a high unity gain bandwidth, 5.5MHz, and as a biomedical environment use, no need for this high bandwidth. As a result this Op-Amp can be optimized to achieve lower gain bandwidth product providing higher gain. By routine calculation and assuming a bandwidth of 200Hz is needed which is the bandwidth

where ECG signals are confined, the gain of this Op-Amp can hit 95dB instead of 85dB while consuming the same power,  $20\mu\text{W}$ , which makes it uncompetitive to other two Op-Amps and as such it is excluded. The Op-Amp proposed in [31] is relatively attractive as it consumes low power and provides relatively good DC gain level. But unfortunately the common mode feedback circuit (CMFB) of this Op-Amp is realized using switch capacitor technique which raises the same disadvantage of the one presented in [6]. The Op-Amp proposed in [32] is very attractive as it exhibits low power performance exploiting the advantage of being class AB in the input and output stage. This Op-Amp depicted in Figure 4.1 is fully differential structured to enhance the performance in terms of noise rejection, signal swing and harmonic distortion. This Op-Amp is considered for optimization to achieve high gain with low power consumption profile.



**Figure 4.1: A two stage class-AB Op-Amp[32].**

This Op-Amp was redesigned in 0.18 $\mu\text{m}$  CMOS technology and simulated using supply voltages of  $\pm 0.75\text{V}$ . All transistors should be working in the sub-threshold region (weak inversion) to achieve low power consumption. Consequently, three conditions should be satisfied to ensure that the transistor is working in the weak inversion region, Eq(28)-(30).

The drain current of MOSFET transistor working in weak inversion is given by the following equation:

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS} - V_{th}}{nV_T}} \left( 1 - e^{\frac{-V_{DS}}{V_T}} \right) \quad (27)$$

where  $V_T = \frac{kT}{q} \approx 26\text{mV}$  and it is called the thermal voltage,  $n$  is the inversion slope coefficient and  $V_{th}$  is the threshold voltage and it is process dependent.

$$V_{GS} < V_{th} \quad (28)$$

$$I_D < I_{D0} \quad (29)$$

$$V_{DS} \geq 4V_T \quad (30)$$

First condition, the gate-source voltage should be kept less than the threshold voltage. Second, the drain current should be less than the specific current,  $I_{D0}$  as illustrated in equation (29). The last one is to ensure that the drain-gate voltage is more than or at least equals four times the thermal voltage which allows vanishing  $e^{\frac{-V_{DS}}{V_T}}$  term, see equation (27). Then, the Op-Amp is optimized to achieve an open loop gain of about 100dB. This is achieved when  $I_{bais}$  is set to 1nA leading to a total current of 3.6 $\mu\text{A}$ . Such low basing currents can be realized using inversion level techniques and as an example a

very low power 0.4nA current source is proposed in [33]. Also, another supply independent current source is proposed in [34] where a very low current of 27nA is reported. The proposed current reference circuit of [34] is depicted in Figure 4.2. The current reference  $I_r$  can be designed and found using the following equations:

$$I_r = \mu_n C_{ox} \frac{2d}{(d+1)^2} \frac{(w/l)_5^2}{(w/l)_5 + (w/l)_6} V_d^2 \quad (31)$$

$$d = \frac{(w/l)_7}{(w/l)_4} \quad (32)$$

$$V_d = \frac{nKT}{q} \ln \frac{(w/l)_1}{(w/l)_2} \quad (33)$$

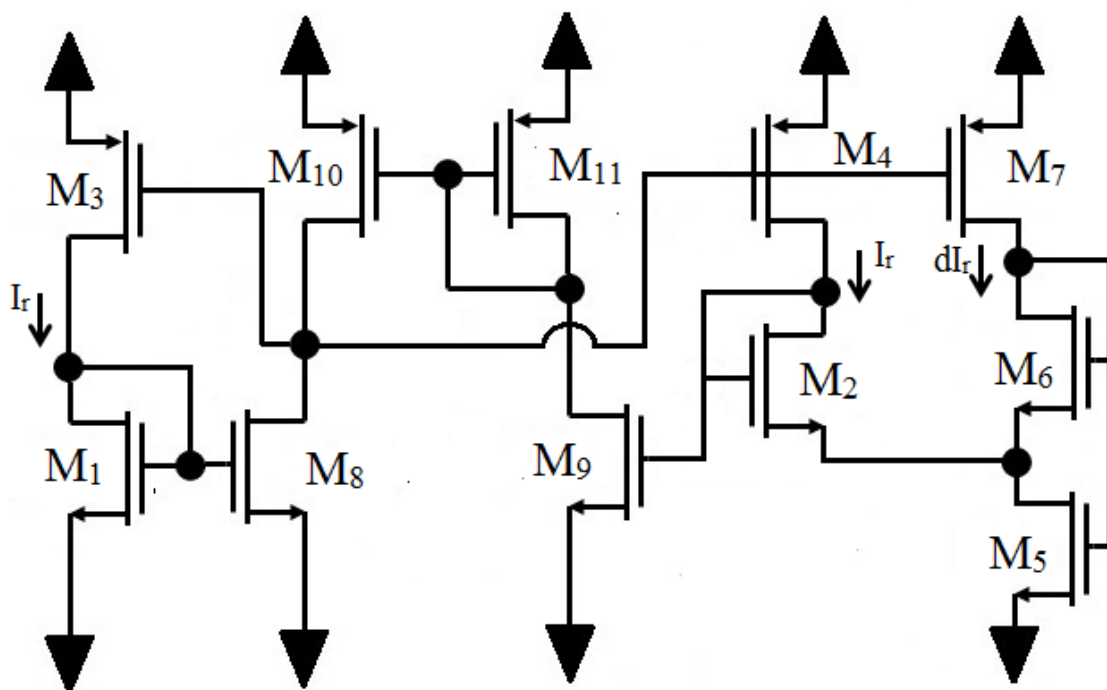
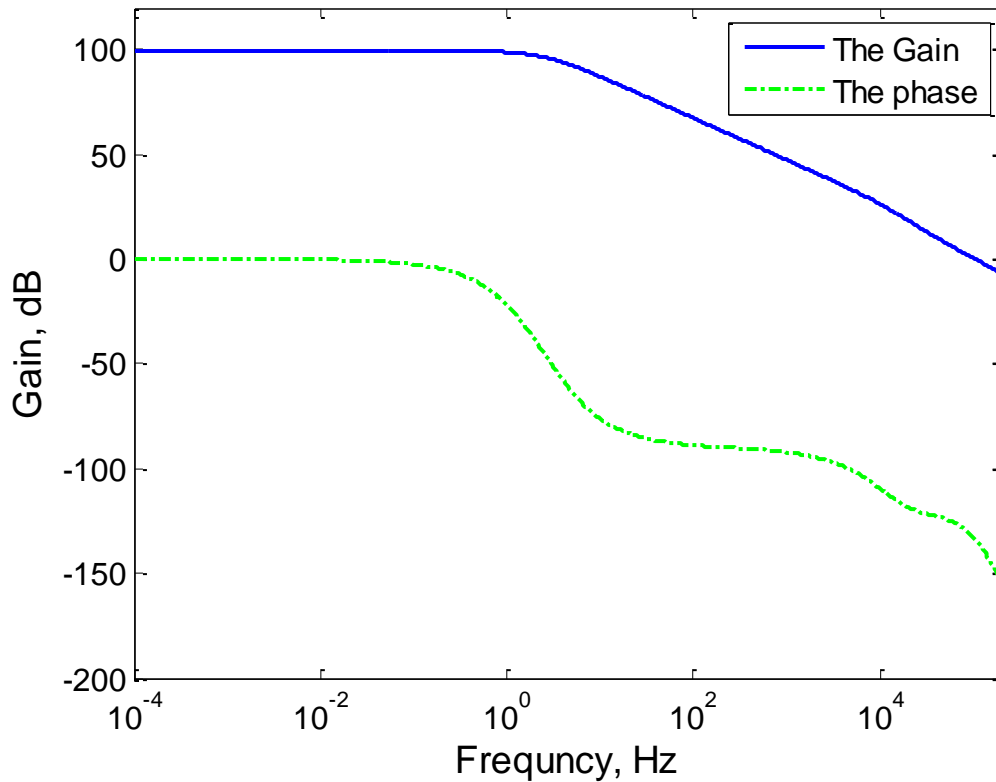


Figure 4.2: Supply independent current reference.

The Op-Amp is compensated to have a phase margin of better than  $46^\circ$  resulting in a unity gain frequency ( $f_t$ ) of 105 kHz as shown in Figure 4.3. The transistor sizes of the optimized Op-Amp are described in Table VI. Frequency

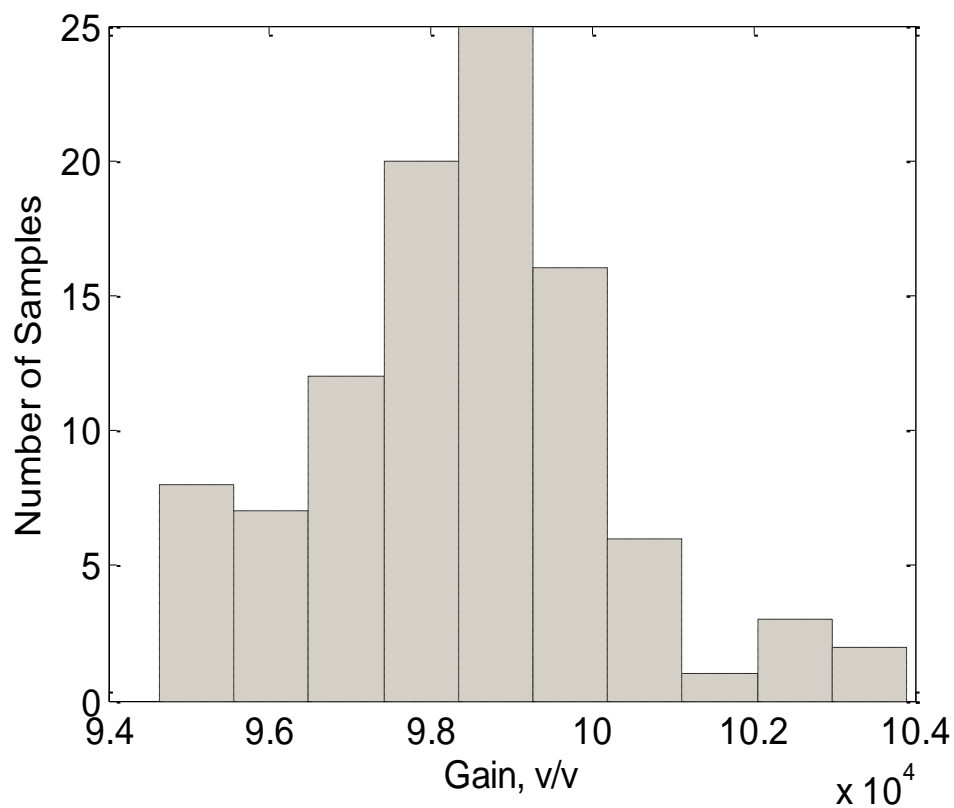


**Figure 4.3: Magnitude and phase responses of the Op-Amp.**

**Table VI: Op-Amp transistor sizes.**

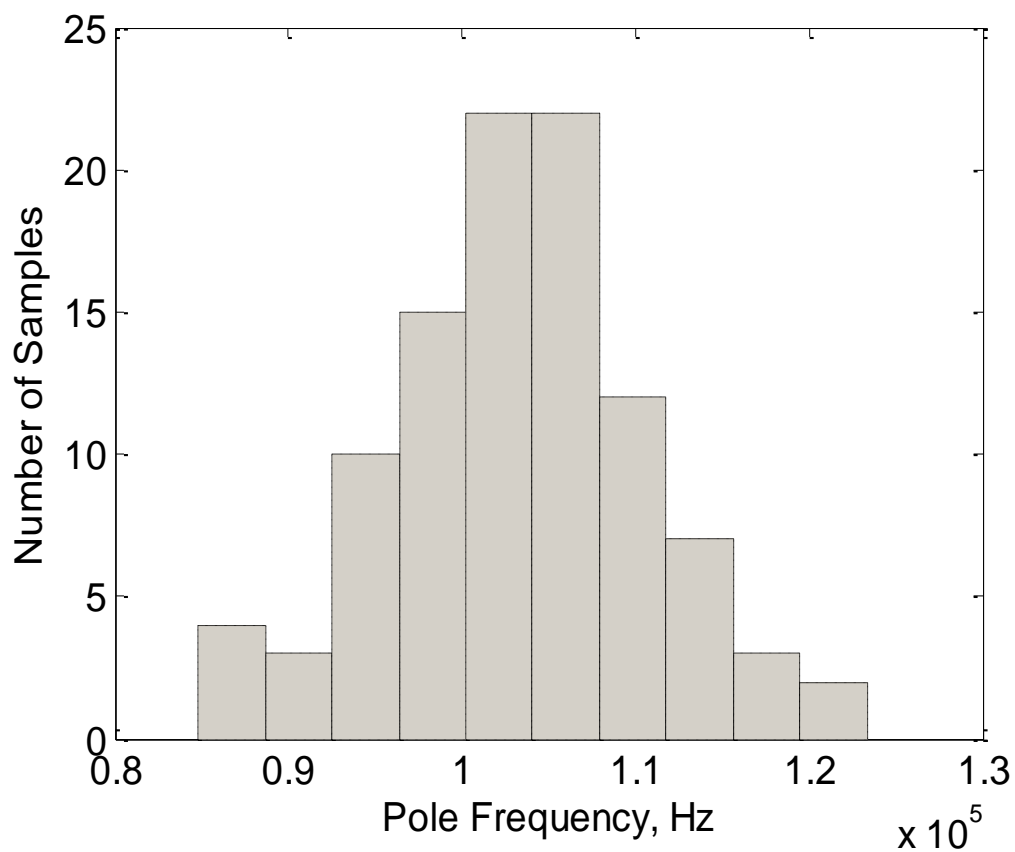
| Transistor                   | W                  | L                  |
|------------------------------|--------------------|--------------------|
| $M_1, M_{1P}, M_2, M_{2P}$ , | 13.5 $\mu\text{m}$ | 13.5 $\mu\text{m}$ |
| $M_3, M_{3P}, M_4, M_{4P}$   | 40.5 $\mu\text{m}$ | 40.5 $\mu\text{m}$ |
| $M_{FVF1}, M_{FVF2}$         | 13.5 $\mu\text{m}$ | 3 $\mu\text{m}$    |
| $M_{B1}, M_{B2}$             | 40.5 $\mu\text{m}$ | 3 $\mu\text{m}$    |
| $M_6, M_{6i}, M_7, M_{7i}$   | 72 $\mu\text{m}$   | 0.6 $\mu\text{m}$  |
| $M_8, M_5, M_{8i}, M_{5i}$   | 24 $\mu\text{m}$   | 0.6 $\mu\text{m}$  |

In addition, Monte Carlo analysis is used to investigate the transistor mismatch. Monte Carlo analysis was performed with  $\pm 10\%$  transistor mismatches in  $M_1$ ,  $M_{1P}$ ,  $M_2$ ,  $M_{2P}$ ,  $M_3$ ,  $M_{3P}$ ,  $M_4$ ,  $M_{4P}$ ,  $M_6$ ,  $M_{6i}$ ,  $M_7$ ,  $M_{7i}$ ,  $M_8$ ,  $M_5$ ,  $M_{8i}$  and  $M_{5i}$  transistors in 100 trials. The results showed a maximum of 5% change in the open loop gain from the nominal value, 100dB, as shown in Figure 4.4. Also, for the same parameter Monte Carlo simulation showed a mean value of almost 99dB which is close to the designed value with a 1% error.



**Figure 4.4: Op-Amp open loop gain histogram.**

It was also found that the unity gain bandwidth changed from 85 kHz to 122 kHz resulting in a maximum change of 19.1% from the designed value, 105 kHz, and a mean value of 103 kHz. The histogram of the pole frequency is shown in Figure 4.5. This seems to be a huge amount of error, however, in biomedical applications, the wide bandwidth Op-Amps are not needed due to the low frequency bandwidth of the bio-signals. Hence, this change in the unity gain bandwidth will not affect the filter performance.

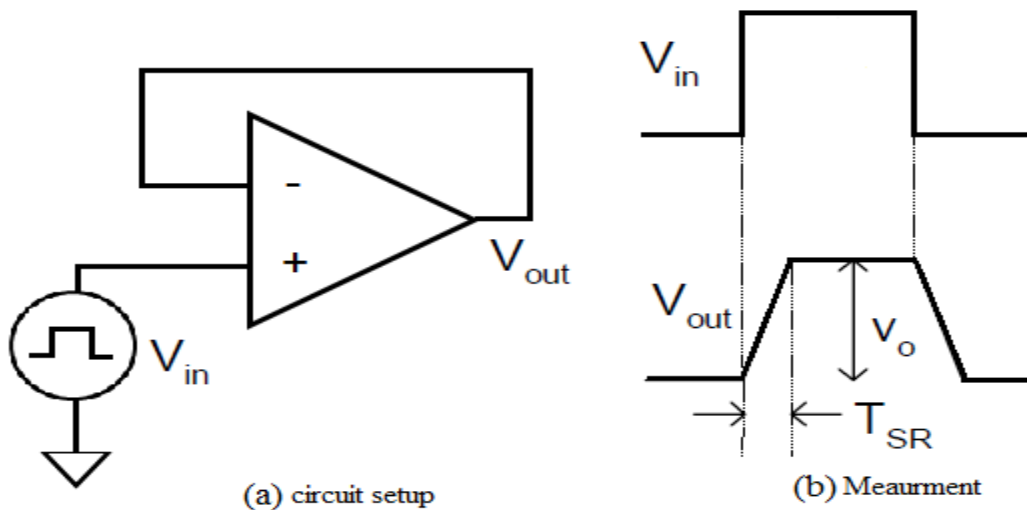


**Figure 4.5: Op-Amp unity gain bandwidth histogram.**

The slew rate is an important issue when designing Op-Amp. The slew rate is defined as the maximum change of the output to the input and it is problematic in high voltage and high frequency operation. The slew rate can be found as follows:

$$SR = \max\left(\frac{dV_{out}}{dt}\right) = \frac{V_{out}}{T_{SR}} \quad (34)$$

The circuit setup and the measurement to find the slew rate of the Op-Amp are shown in Figure 4.6. The Op-Amp is connected as a voltage buffer with pulse input to easily find the time difference between the output and input voltages,  $T_{SR}$  shown in Figure 4.6(b).



**Figure 4.6: Setup to find the slew rate.**

For this Op-Amp, it was found that  $SR=0.544 \text{ mV}/\mu\text{s}$  which is much greater than the required rate shown in Table I.



### 4.3 LOW PASS FILTER DESIGN BASED ON R-2R APPROACH

The first proposed filter is based on the active-RC filter where passive resistors are replaced with R-2R ladders to achieve low frequency response. The proposed filter circuit using Tow-Thomas bi-quad is shown in Figure 4.7 and Figure 4.8, both single ended and differential realization. For simplicity, in Figure 4.8 the arrows that indicate the digital tuning are removed.

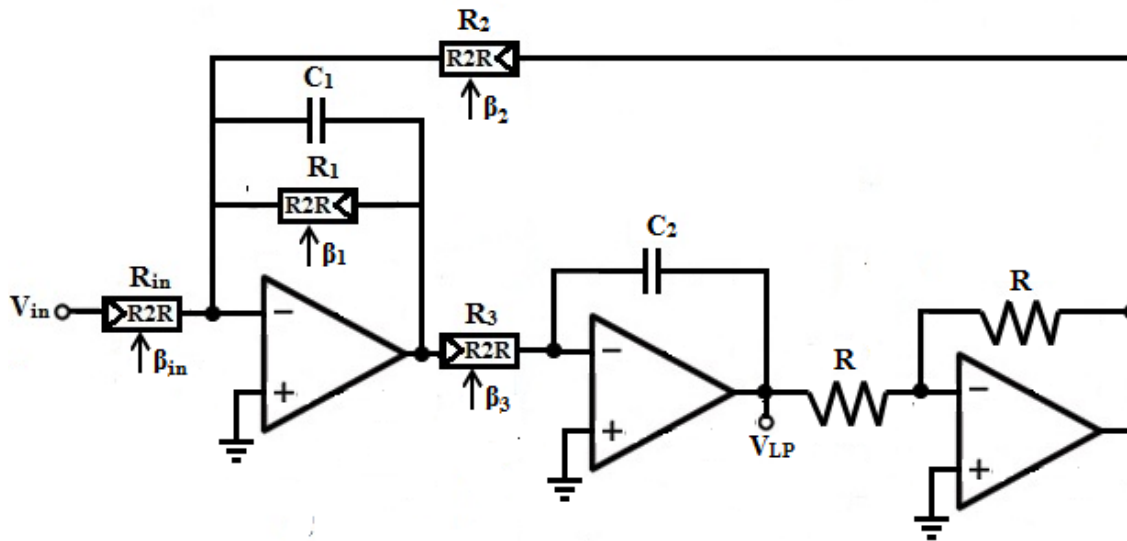
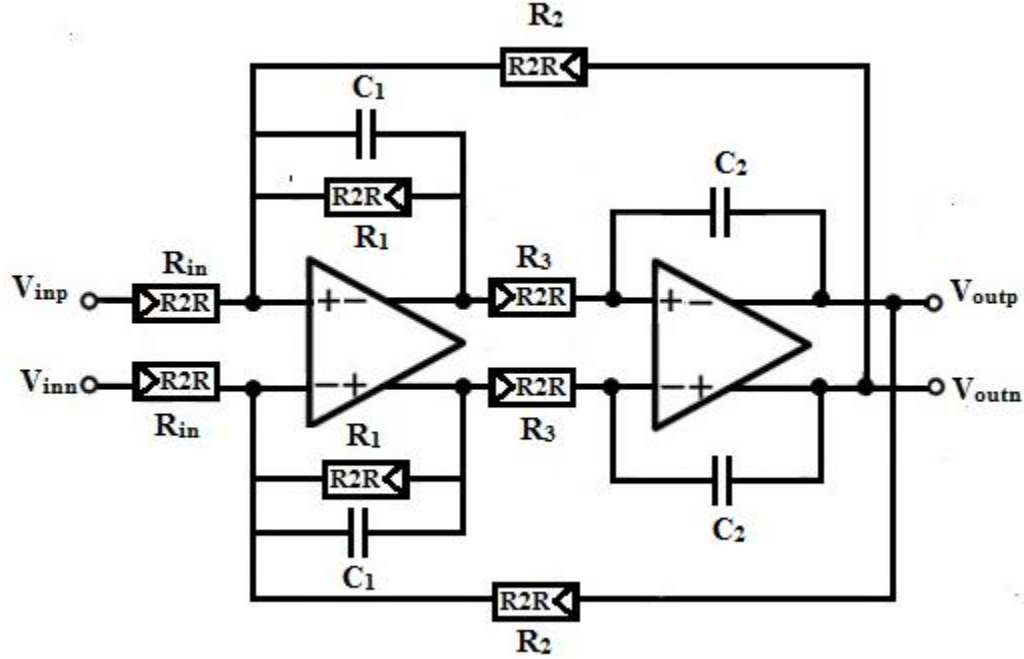


Figure 4.7: Single ended 2<sup>nd</sup> LPF Op-Amp realization of Tow-Thomas bi-quad with R-2R approach.



**Figure 4.8: Differential input and output 2<sup>nd</sup> LPF Op-Amp realization of Tow-Thomas bi-quad with R-2R approach.**

The active-R-2R approach based filter incorporates three Op-Amps which are reduced to two for differential realization and four R-2R ladders increased to eight ladders for differential per bi-quad. It can be shown that the low pass response is given by:

$$\frac{V_{LP}}{V_{in}} = - \frac{1/(\beta_{in}\beta_3R_{in}R_3C_1C_2)}{s^2 + s/(\beta_1R_1C_1) + 1/(\beta_2\beta_3R_2R_3C_1C_2)} \quad (35)$$

It can be shown that the pole frequency ( $\omega_o$ ), the quality factor ( $Q$ ) and the DC gain are given as follows:

$$\omega_o = \frac{1}{\sqrt{\beta_2\beta_3R_2R_3C_1C_2}} \quad (36)$$

$$Q = \sqrt{\frac{\beta_1 \beta_1 R_1 R_1 C_1}{\beta_2 \beta_3 R_2 R_3 C_2}} \quad (37)$$

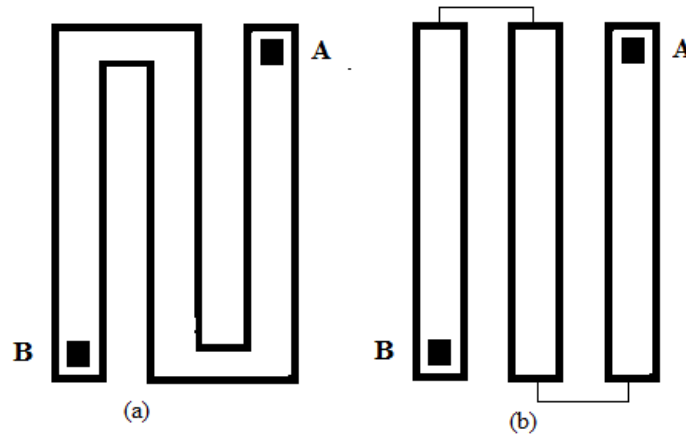
$$DC \text{ Gain} = \frac{\beta_2 R_2}{\beta_{in} R_{in}} \quad (38)$$

From these equations, it can be seen that the pole frequency can be tuned independently without changing the gain and quality factor through simultaneously adjusting all ladders and/or through changing the value of the two capacitors simultaneously. Also, it can be noticed that the pole frequency can be made ultra low with R-2R ladders. For example, pole frequency of 150Hz can be obtained using C of 50pF and R of 40k $\Omega$  with ladder size of 9bits.

Optimizing the area is also an important issue at this stage. Area estimation is done based on the design rules of the TSMC 0.18 $\mu$ m CMOS technology in L-Edit tanner tool. The resistance value can be calculated using the following equations:

$$R = R_{\text{square}} \frac{L}{W} \quad (39)$$

where  $R_{\text{square}}$  is the sheet resistance, W and L are the width and the length of the resistor. Different patterns and ways can be used to layout the resistor, however, to minimize the space and hence optimize the area, the serpentine pattern shown in Figure 4.9 is used and also it is preferred to avoid the corners by connecting separate sections through normal connectors as shown in Figure 4.9(b)[35].



**Figure 4.9: Resistor layout serpentine pattern. (a) with corners. (b) without corners.**

The area of the resistor following the serpentine pattern can be estimated using the following equation:

$$\text{Area} = L(W + \Delta) \quad (40)$$

where  $\Delta$  is the minimum distance between two consecutive resistors.

The highest resistivity can be obtained using n-well resistor where  $R_{\text{square}}=927\Omega/\text{square}$ , the minimum width is  $0.86\mu\text{m}$  ( $W=0.86\mu\text{m}$ ) and a minimum distance of  $0.6\mu\text{m}$  should be maintained between two consecutive n-well sections ( $\Delta= 0.6\mu\text{m}$ ).

On the other hand, a poly-poly capacitor structure shown in Figure 4.10 is used to layout the capacitor [35]. The capacitance value and area can be found following these equations:

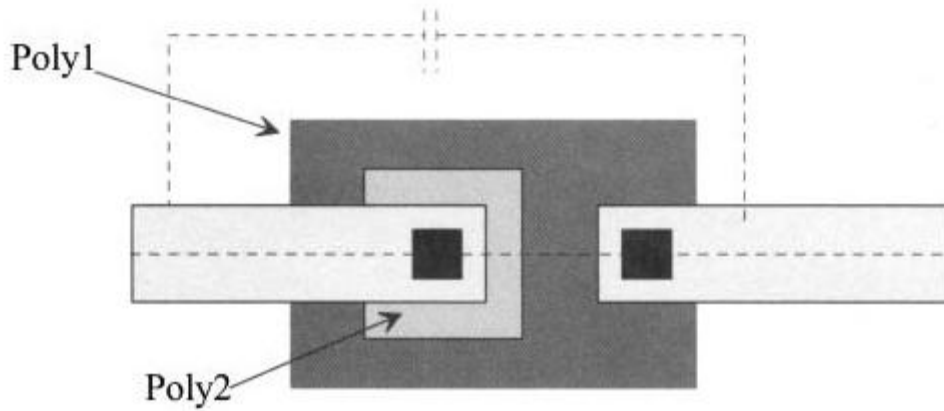
$$C = C_{\text{ox}}(WL) \quad (41)$$

where  $C_{\text{ox}}$  is the oxide capacitance per area and can be calculated as follows:

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \quad (42)$$

where  $\varepsilon_{ox} = \varepsilon_r \varepsilon_0 = (3.97)(8.85 \times 10^{-18}) = 35.136 \times \frac{10^{-18}F}{\mu m} = 35.136 \frac{aF}{\mu m}$  which is a  $SiO_2$  dielectric constant, and  $tox$  is a process parameter and equals  $41\text{\AA}$  for the technology used in this work.

$$\text{capacitor area}|_{\text{best case}} = W \times L \quad (43)$$



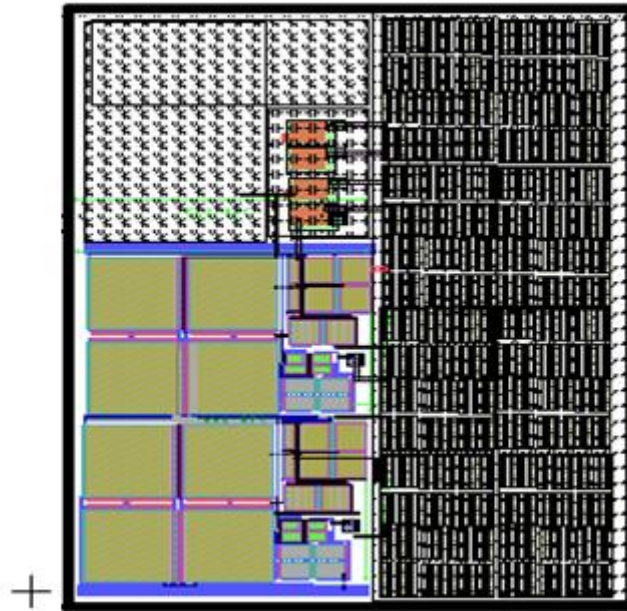
**Figure 4.10: Poly-Poly capacitor layout structure [35].**

Using these equations (39)-(43) and assuming the best case of having no unused spaces in the layout, the total area which is the sum of eight R-2R ladders and four capacitors without the Op-Amp area can be estimated. Table VII summaries the capacitance values and the estimated area of a 150Hz pole frequency 2<sup>nd</sup> order low pass filter for different networks to better select the value of the capacitance in order to optimized the area on the chip.

**Table VII : Area estimation for different R-2R networks.**

| R-2R Ladder<br>(Number of bits) | C (pF)<br>(simulation) | Area (mm <sup>2</sup> )<br>(without Op-Amp) | Gain (dB) |
|---------------------------------|------------------------|---|-----------|
| 9 bits                          | 50                     | 0.0355                                      | 0         |
| 10 bits                         | 19                     | 0.0223                                      | -2        |
| 11 bits                         | 6.3                    | 0.0177                                      | -5        |
| 12 bits                         | 1.8                    | 0.0169                                      | -11       |

It can be seen from Table VII that the optimum area can be achieved using 12 bits R-2R ladder. Also, it can be figured out that the gain of the filter reduces as the number of R-2R network increases which also supports the previously mentioned claim that the gain and the number of R-2R networks are two contradicting parameters. The gain of the filter can be increased by reducing the value of  $R_{in}$ . Simulations were carried out using 0.18 $\mu$  CMOS technology for the proposed filter. The filter operates from a supply voltage of  $\pm 0.75V$  while consuming total power of 10.38 $\mu W$  while occupying an area of 0.102mm<sup>2</sup> the layout photo of the filter is depicted in Figure 4.11. The R-2R ladders were made up of 12-bit.



**Figure 4.11: 2<sup>nd</sup> order R-2R based LPF layout.**

The simulation results showed that the filter achieved a corner frequency of 150Hz, Q of approximately 0.707 with a total harmonic distortion (THD) of better than -77.8dB with an input signal of 1mV and 15Hz and the input noise is better than -79.4dB resulting in an input referred noise of less than 106.7 $\mu$ V. The noise can be further decreased by increasing the gain of the filter and it can reach a noise floor of 1.25 $\mu$ V if the gain is pushed to the maximum limit, 50dB. The theoretical and simulation frequency responses of the filter before and after tuning are depicted in Figure 4.12. The proposed filter response is close to the ideal case. Figure 4.13 shows the gain and frequency tunability feature of the filter.

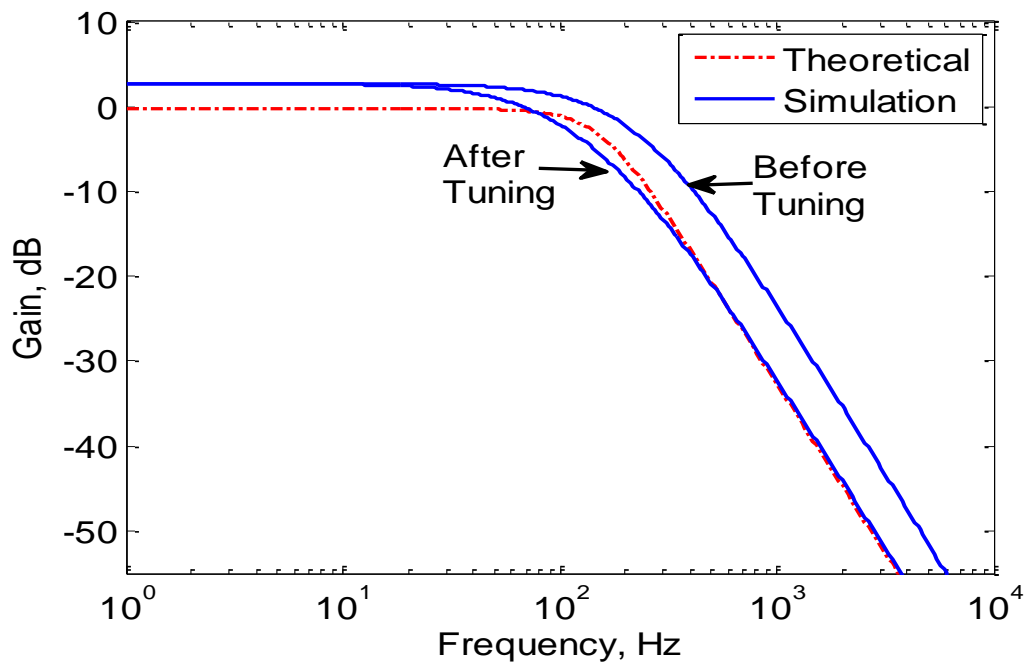


Figure 4.12: Frequency responses of 2<sup>nd</sup> order LPF based on R-2R approach.

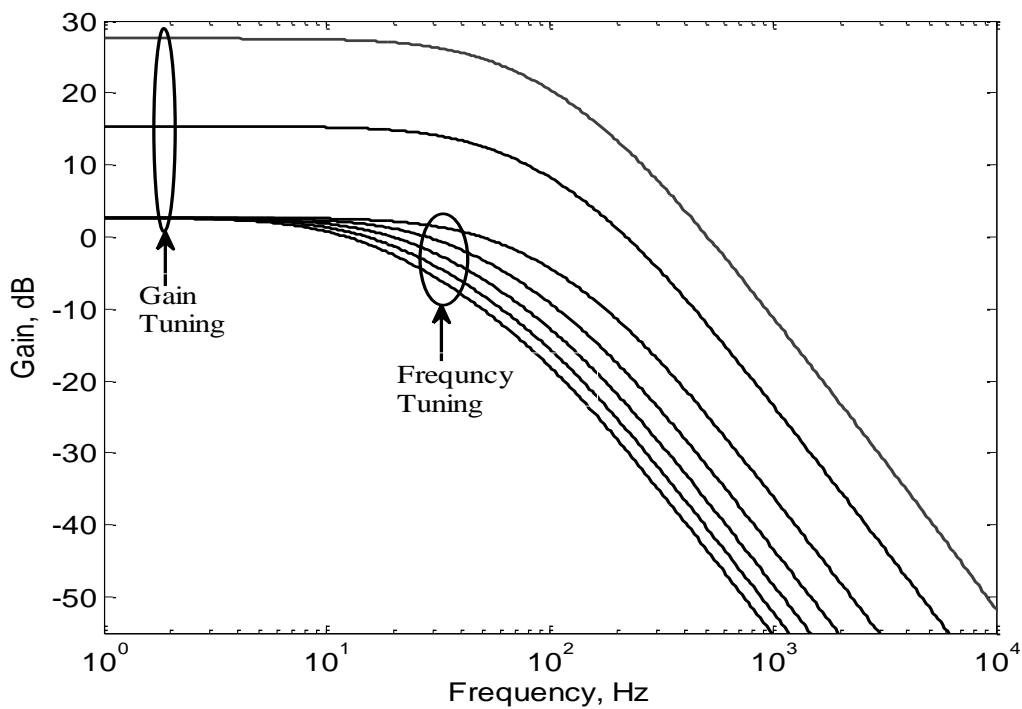
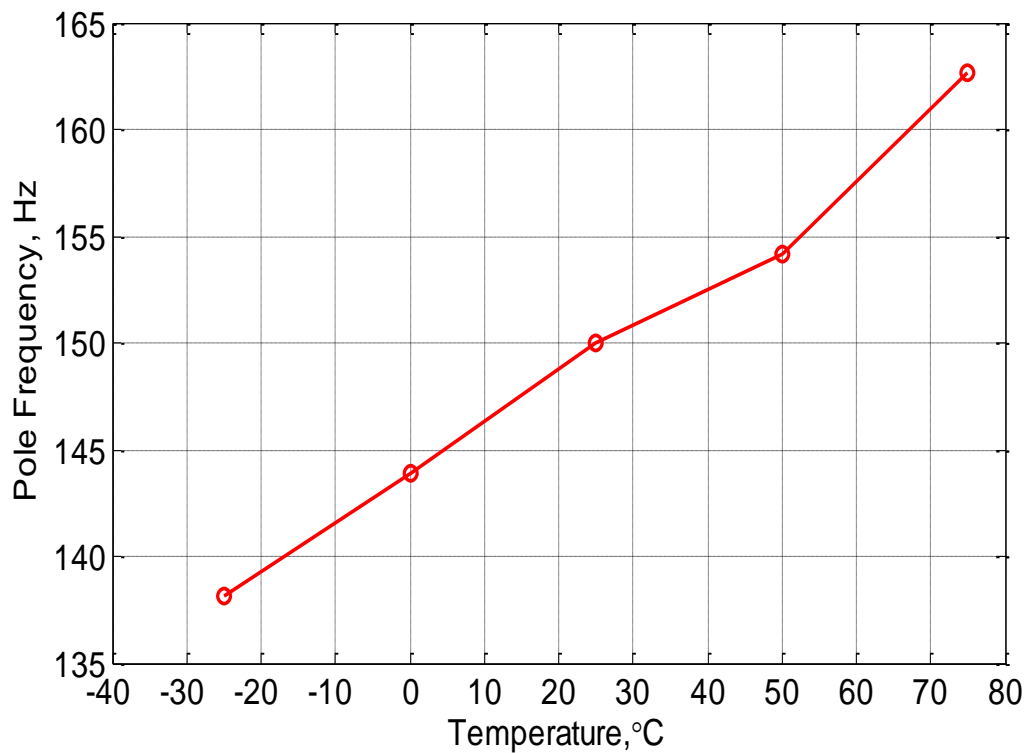


Figure 4.13: Frequency and gain tuning feature for the R-2R based filter.





**Figure 4.14: Temperature effect on the pole frequency.**

Figure 4.14 shows the effect of the temperature variation on the pole frequency of the proposed filter. The temperature was swept from  $-25^{\circ}$  to  $75^{\circ}$  covering possible range of low and high temperature levels. It was found that the pole frequency was shifted by a maximum of 12.5 Hz from 150 Hz resulting in an 8.3% error due to the change in the temperature.

#### 4.4 LOW PASS FILTER DESIGN BASED ON COMBINED APPROACH

The second proposed filter is based on the combination approach between the R-2R ladder technique and the difference term technique to relax the number of R-2R networks and hence less power can be achieved. As discussed earlier the difference term approach cannot be directly realized using the Two-Thomas bi-quad and hence an additional Op-Amp should be used in the differential realization, see Figure 4.15.

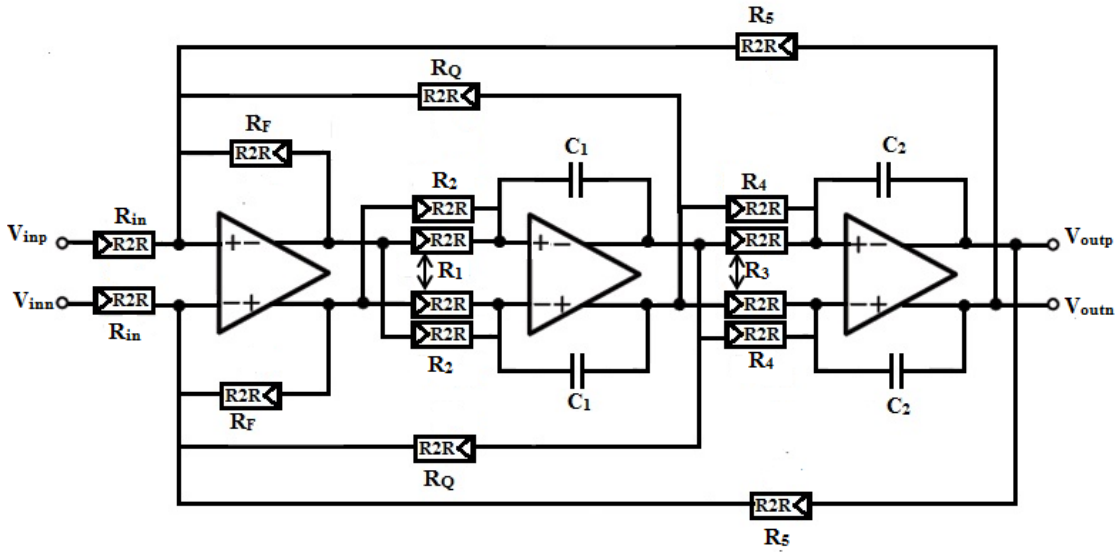


Figure 4.15: Differential realization of 2<sup>nd</sup> order LPF based on the combined approach.

By routine analysis, the low pass transfer function of this filter can be obtained as following:

$$\frac{V_{LP}}{V_{in}} = \frac{\frac{\beta_F R_F (\beta_1 R_1 - \beta_2 R_2) (\beta_3 R_3 - \beta_4 R_4)}{C_1 C_2 \beta_1 R_1 \beta_2 R_2 \beta_3 R_3 \beta_4 R_4 \beta_{in} R_{in}}}{s^2 + s \left( \frac{\beta_F R_F (\beta_1 R_1 - \beta_2 R_2)}{C_2 \beta_1 R_1 \beta_2 R_2 \beta_Q R_Q} \right) + \frac{\beta_F R_F (\beta_1 R_1 - \beta_2 R_2) (\beta_3 R_3 - \beta_4 R_4)}{C_1 C_2 \beta_1 R_1 \beta_2 R_2 \beta_3 R_3 \beta_4 R_4 \beta_5 R_5}} \quad (42)$$

By proper values selection making  $\beta_1 R_1 = \beta_3 R_3$ ,  $\beta_2 R_2 = \beta_4 R_4$ ,  $\beta_5 R_5 = \beta_F R_F = \beta R$  and  $C_1 = C_2 = C$ , the DC gain, the pole frequency, the quality factor and the scaling constant are given as follows:

$$\text{DC Gain} = \frac{\beta R}{\beta_{in} R_{in}} \quad (43)$$

$$Q = \frac{\beta_Q R_Q}{\beta R} \quad (44)$$

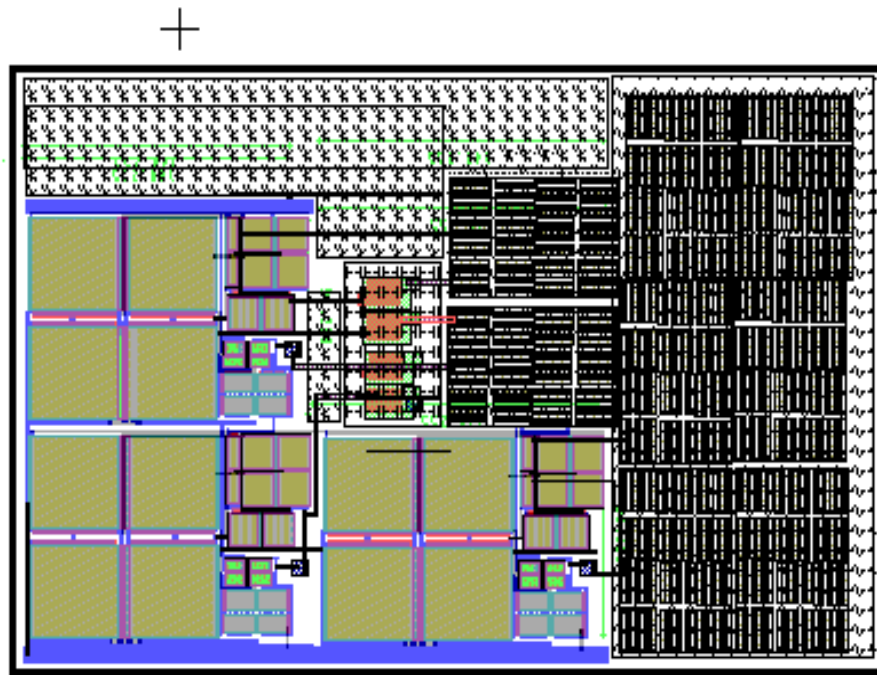
$$2\pi f = \frac{(\beta_1 R_1 - \beta_2 R_2)}{C \beta_1 R_1 \beta_2 R_2} \quad (45)$$

$$k = \left( \frac{\beta_1 R_1}{\beta_2 R_2} - 1 \right) \quad (46)$$

It can be figured out from the above equations that the DC gain, the pole frequency and the quality factor of the proposed filter can be controlled independently. The poles can achieve low pole frequency exploiting the presence of the difference term and  $\beta_1$ . Note that from equation (41),  $\beta_1$  and  $\beta_2$  should be changed simultaneously to maintain the same reduction constant. The gain can be controlled via  $\beta_{in}$  to compensate the decrease in the gain due to the effect of using R-2R ladder. For example, a 6-bit R-2R ladder with 40k $\Omega$  and a capacitor of 25pF can realize 150Hz by maintaining a 4-bit reduction.

A second order low pass filter based on the combined approach was designed and simulated using 0.18 $\mu$  CMOS technology. After optimization process, the filter consumes 4.52 $\mu$ W from  $\pm 0.65$ V voltage supply and occupying an area of 0.125 mm<sup>2</sup> the layout view is shown in Figure 4.16. A 6-bit R-2R ladder was used with different values of R.

The simulation results showed that the filter achieves a corner frequency of 150Hz, Q of approximately 0.707 and with a total harmonic distortion (THD) of better than -73dB and can be increased to almost -78.8dB for a voltage supply of  $\pm 0.67\text{v}$ . Hence the power is increased a little bit to almost  $5.87\mu\text{W}$  using a test input signal with an amplitude of 1mV and frequency of 15Hz.



**Figure 4.16: 2<sup>nd</sup> order combined based LPF layout.**

Theoretical and simulated frequency responses of the proposed filter are shown in Figure 4.17. The filter showed an input referred noise of  $147.85\mu\text{V}$  and it can be improved to  $24.3\mu\text{V}$  by increasing the gain of the filter. Also, this filter allows gain and frequency tuning through the capacitors and/or R-2R ladders, see Figure 4.18. The temperature effect was also studied. The pole frequency changed from 133.8 Hz to 164.9 Hz showing a maximum change of 10.8% due to the temperature variation from  $-25^\circ$  to  $75^\circ$ .

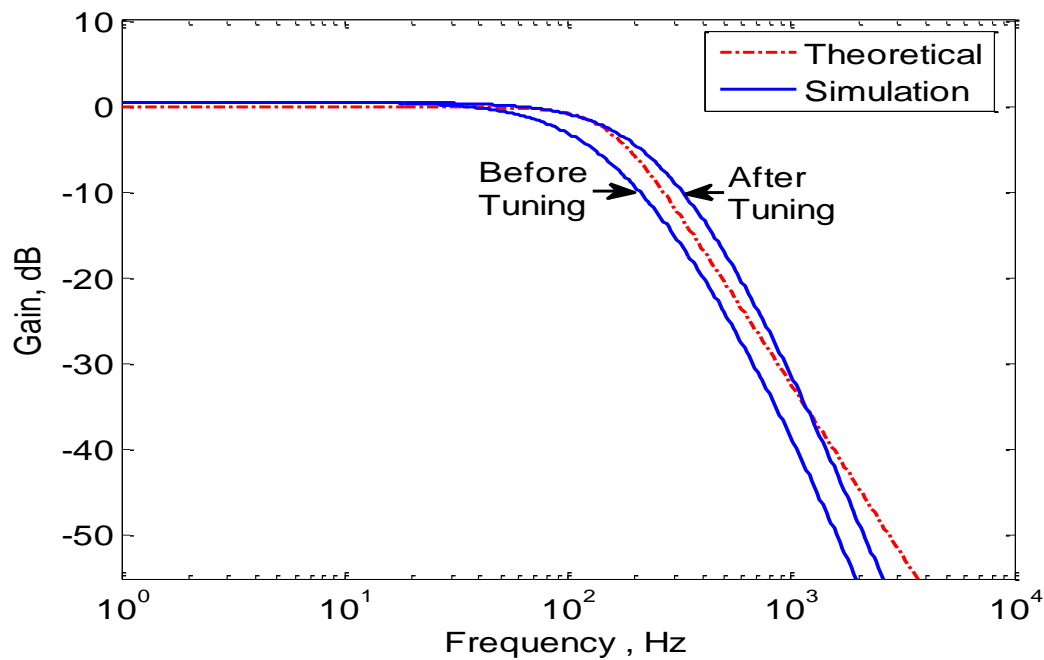


Figure 4.17: 2<sup>nd</sup> LPF frequency response based on the combined approach.

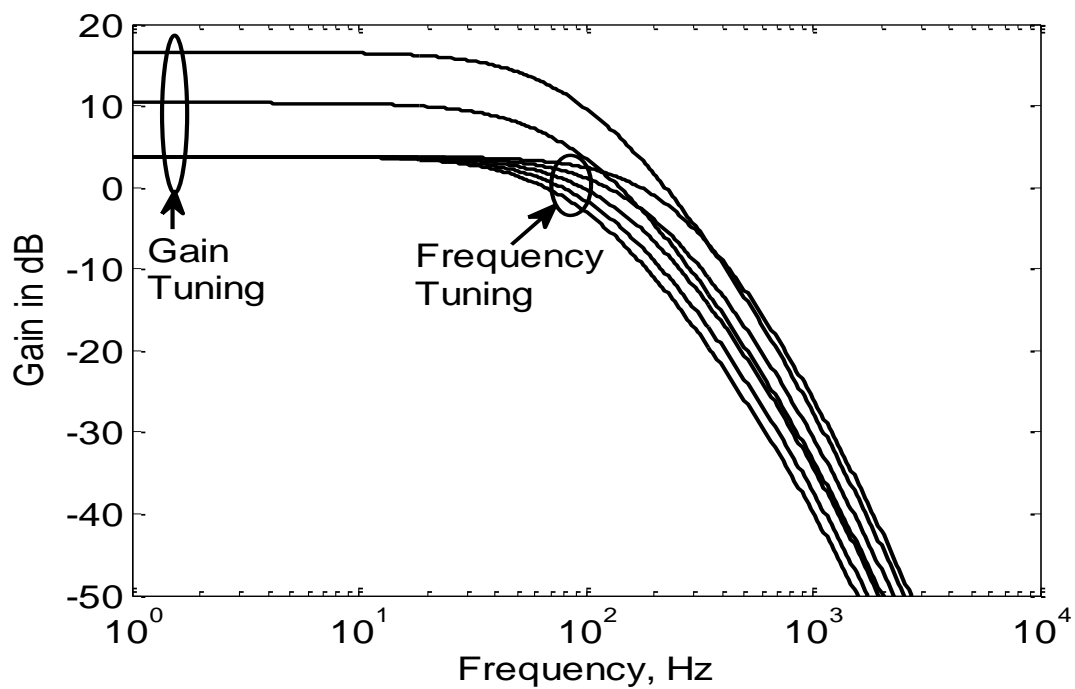
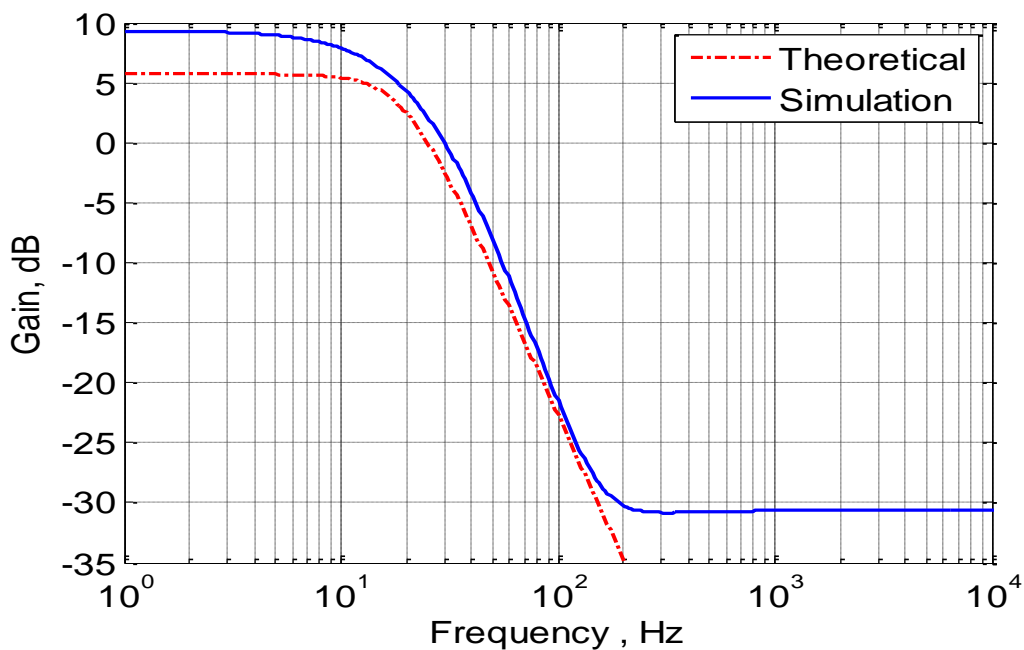


Figure 4.18: Frequency and gain tuning feature for the combined based filter.

A comparison between the proposed filters and others in the literature is made and presented in Table VIII. It can be noticed that the proposed filters exhibit low power performance and it provides a digital and independent programmability over the gain, the quality factor and the corner frequency. In addition to that, a better linearity and noise performance is achieved. It can be noticed from Table VIII that the filter proposed in [13] has a superior power performance over the proposed ones; however, the combined approach based filter can be further optimized based on the fact that the combined based filter requires lower open loop gain and hence lower power than the R-2R only based one. This filter was successfully optimized and a very low power of 108nW was achieved. This is in price of increasing noise floor and less linearity as shown in Table VIII. The frequency response of this filter compared to the theoretical response is shown in Figure 4.19.



**Figure 4.19: Frequency response of the combined approach filter.**

**Table VIII : Comparison between this work and other related work.**

| Reference                | [6]                     | [11]         | [12]            | [13]            | [18]            | This Work         |                            |              |
|--------------------------|-------------------------|--------------|-----------------|-----------------|-----------------|-------------------|----------------------------|--------------|
| Tech.                    | 2 $\mu$ m BiCMOS        | NA           | 0.35 $\mu$ CMOS | 0.35 $\mu$ CMOS | 0.35 $\mu$ CMOS | 0.18 $\mu$ CMOS   | 0.18 $\mu$ CMOS            |              |
| Structure                | SC                      | Gm-C         | Gm-C            | Gm-C            | Op-Amp          | Op-Amp (R2R only) | Op-Amp (Combined approach) |              |
| Type                     | LPN                     | LP           | LPN             | LP              | LP              | LP                | LP                         |              |
| Order                    | 2                       | 3            | 5               | 2               | 2               | 2                 | 2                          |              |
| App.                     | Power Line Interference | General      | EEG             | General         | Heart Rate      | ECG               | ECG                        |              |
| Pole Frequency           | 31.4-50Hz               | 10 Hz        | 37-67Hz         | 3.8 Hz          | 18Hz            | 150 Hz            | 150 Hz                     | 2.5-20Hz     |
| Power(W)                 | 58 $\mu$                | 15 $\mu$     | 11 $\mu$        | 96.5n           | N/A             | 10.38 $\mu$       | 4.52 $\mu$                 | 108n         |
| Supply Voltage(V)        | NA                      | $\pm 1.5$ V  | $\pm 1.5$ V     | 1.5 V           | 3 V             | $\pm 0.75$ V      | $\pm 0.65$ V               | $\pm 0.25$ V |
| Linearity                | NA                      | 62 dB        | -50dB (THD)     | NA              | 40 dB           | -77.8dB (THD)     | -73dB (THD)                | -46dB (THD)  |
| Input referred noise (V) | NA                      | NA           | 243 $\mu$       | NA              | NA              | 1.25 $\mu$        | 24.3 $\mu$                 | 34.1 $\mu$   |
| Area(mm <sup>2</sup> )   | NA                      | NA           | 0.25            | 0.607           | NA              | 0.102             | 0.125                      | 0.125        |
| Gain (dB)                | -0.1                    | $\approx -6$ | 0               | 0               | 11.5-44.6       | 0-50              | 3.9-16                     | $\approx 10$ |

## 5. CONCLUSION AND FUTURE WORK

### 5.1 CONCLUSION

In this thesis, four different techniques to design a very low frequency filters were investigated. These solutions permit IC integration. However, two of them suffer from high power consumption while the other two show promising simulation results. Non-ideal analysis of these techniques was studied. Different low pass filters were designed and realized using 0.18 $\mu\text{m}$  TSMC CMOS technology, the first one based on the R-2R technique and the other one is based on the combination approach between R-2R and the difference term technique. Comparison between the proposed filters and other related work were made and well presented. The combined approach based filters have a disadvantage of using three active elements instead of two in the R-2R only based filter. Also, duplicating the number of R-2R ladders is another issue to be considered in the combined based filter. In general, the proposed filters show good performance and results to some other related work in terms of area, linearity, noise performance and power.



## 5.2 FUTURE WORK

Since there is nothing perfect, there must be a room for improvement and this work can be extended to the following directions:

- Fabricating the proposed design and testing it to match the analysis and simulation results with experimental proof.
- Considering the current mode circuits and designing a voltage and current attenuators with low power and good linearity performance.
- Designing filters based on these techniques for other biomedical applications such as cochlear implant, oximeter, EEG...etc.
- Developing new techniques to further improve the power, noise and linearity.
- Designing and fabricating a complete portable ECG system and applying some of these techniques to all the filters incorporated in the system.

## APPENDIX A

The process parameters used for this work, TSMC 0.18 $\mu$ m Technology:

.MODEL nenh NMOS (LEVEL = 49

|                     |                    |                     |
|---------------------|--------------------|---------------------|
| +VERSION = 3.1      | TNOM = 27          | TOX = 4.1E-9        |
| +XJ = 1E-7          | NCH = 2.3549E17    | VTH0 = 0.3694303    |
| +K1 = 0.5789116     | K2 = 1.110723E-3   | K3 = 1E-3           |
| +K3B = 0.0297124    | W0 = 1E-7          | NLX = 2.037748E-7   |
| +DVT0W = 0          | DVT1W = 0          | DVT2W = 0           |
| +DVT0 = 1.2953626   | DVT1 = 0.3421545   | DVT2 = 0.0395588    |
| +U0 = 293.1687573   | UA = -1.21942E-9   | UB = 2.325738E-18   |
| +UC = 7.061289E-11  | VSAT = 1.676164E5  | A0 = 2              |
| +AGS = 0.4764546    | B0 = 1.617101E-7   | B1 = 5E-6           |
| +KETA = -0.0138552  | A1 = 1.09168E-3    | A2 = 0.3303025      |
| +RDSW = 105.6133217 | PRWG = 0.5         | PRWB = -0.2         |
| +WR = 1             | WINT = 2.885735E-9 | LINT = 1.715622E-8  |
| +XL = 0             | XW = -1E-8         | DWG = 2.754317E-9   |
| +DWB = -3.690793E-9 | VOFF = -0.0948017  | NFACTOR = 2.1860065 |
| +CIT = 0            | CDSC = 2.4E-4      | CDSCD = 0           |
| +CDSCB = 0          | ETA0 = 2.665034E-3 | ETAB = 6.028975E-5  |
| +DSUB = 0.0442223   | PCLM = 1.746064    | PDIBLC1 = 0.3258185 |

```

+PDIBLC2 = 2.701992E-3  PDIBLCB = -0.1          DROUT  = 0.9787232
+PSCBE1  = 4.494778E10  PSCBE2  = 3.672074E-8  PVAG    = 0.0122755
+DELTA   = 0.01         RSH      = 7           MOBMOD  = 1
+PRT     = 0           UTE     = -1.5        KT1     = -0.11
+KT1L   = 0           KT2     = 0.022       UA1     = 4.31E-9
+UB1    = -7.61E-18   UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0           WLN     = 1           WW      = 0
+WWN    = 1           WWL     = 0           LL      = 0
+LLN    = 1           LW      = 0           LWN     = 1
+LWL    = 0           CAPMOD  = 2           XPART   = 0.5
+CGDO   = 8.58E-10   CGSO    = 8.58E-10   CGBO    = 1E-12
+CJ      = 9.471097E-4  PB       = 0.8        MJ       = 0.3726161
+CJSW   = 1.905901E-10  PBSW    = 0.8        MJSW    = 0.1369758
+CJSWG  = 3.3E-10     PBSWG   = 0.8        MJSWG   = 0.1369758
+CF      = 0           PVTH0   = -5.105777E-3  PRDSW   = -1.1011726
+PK2    = 2.247806E-3  WKETA   = -5.071892E-3  LKETA   = 5.324922E-4
+PU0    = -4.0206081  PUA     = -4.48232E-11  PUB     = 5.018589E-24
+PVSAT  = 2E3         PETA0   = 1E-4         PKETA   = -2.090695E-3 )
.MODEL penh PMOS (          LEVEL = 49
+VERSION = 3.1             TNOM    = 27           TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 4.1589E17    VTH0    = -0.3823437

```

|                       |                       |                       |
|-----------------------|-----------------------|-----------------------|
| +K1 = 0.5722049       | K2 = 0.0219717        | K3 = 0.1576753        |
| +K3B = 4.2763642      | W0 = 1E-6             | NLX = 1.104212E-7     |
| +DVT0W = 0            | DVT1W = 0             | DVT2W = 0             |
| +DVT0 = 0.6234839     | DVT1 = 0.2479255      | DVT2 = 0.1            |
| +U0 = 109.4682454     | UA = 1.31646E-9       | UB = 1E-21            |
| +UC = -1E-10          | VSAT = 1.054892E5     | A0 = 1.5796859        |
| +AGS = 0.3115024      | B0 = 4.729297E-7      | B1 = 1.446715E-6      |
| +KETA = 0.0298609     | A1 = 0.3886886        | A2 = 0.4010376        |
| +RDSW = 199.1594405   | PRWG = 0.5            | PRWB = -0.4947034     |
| +WR = 1               | WINT = 0              | LINT = 2.93948E-8     |
| +XL = 0               | XW = -1E-8            | DWG = -1.998034E-8    |
| +DWB = -2.481453E-9   | VOFF = -0.0935653     | NFACTOR = 2           |
| +CIT = 0              | CDSC = 2.4E-4         | CDSCD = 0             |
| +CDSCB = 0            | ETA0 = 3.515392E-4    | ETAB = -4.804338E-4   |
| +DSUB = 1.215087E-5   | PCLM = 0.96422        | PDIBLC1 = 3.026627E-3 |
| +PDIBLC2 = -1E-5      | PDIBLCB = -1E-3       | DROUT = 1.117016E-4   |
| +PSCBE1 = 7.999986E10 | PSCBE2 = 8.271897E-10 | PVAG = 0.0190118      |
| +DELTA = 0.01         | RSH = 8.1             | MOBMOD = 1            |
| +PRT = 0              | UTE = -1.5            | KT1 = -0.11           |
| +KT1L = 0             | KT2 = 0.022           | UA1 = 4.31E-9         |
| +UB1 = -7.61E-18      | UC1 = -5.6E-11        | AT = 3.3E4            |

|                      |                     |                        |
|----------------------|---------------------|------------------------|
| +WL = 0              | WLN = 1             | WW = 0                 |
| +WWN = 1             | WWL = 0             | LL = 0                 |
| +LLN = 1             | LW = 0              | LWN = 1                |
| +LWL = 0             | CAPMOD = 2          | XPART = 0.5            |
| +CGDO = 7.82E-10     | CGSO = 7.82E-10     | CGBO = 1E-12           |
| +CJ = 1.214428E-3    | PB = 0.8461606      | MJ = 0.4192076         |
| +CJSW = 2.165642E-10 | PBSW = 0.8          | MJSW = 0.3202874       |
| +CJSWG = 4.22E-10    | PBSWG = 0.8         | MJSWG = 0.3202874      |
| +CF = 0              | PVTH0 = 5.167913E-4 | PRDSW = 9.5068821      |
| +PK2 = 1.095907E-3   | WKETA = 0.0133232   | LKETA = -3.648003E-3   |
| +PU0 = -1.0674346    | PUA = -4.30826E-11  | PUB = 1E-21            |
| +PVSAT = 50          | PETA0 = 1E-4        | PKETA = -1.822724E-3 ) |

## REFERENCES

- [1]. W. Eberle, A.S. Mecheri, T.K. Nguyen, G. Gielen, R. Campagnolo, A. Burdett, C. Toumazou and B. Volckaerts, "Health-care electronics, the market, the challenges, the progress " , *DATE '09*, pages 1030-1034.
- [2]. E. Katz, "Bioelectronics," *Electroanalysis* 18, No. 19-20 1855-1857, 2006.
- [3]. J. Webster, "Medical Instrumentation: Application and Design", John Wiley, 3<sup>rd</sup> Edition, 1998
- [4]. R. Schaumann, M. S. Ghausi, and K. R. Laker, 'Design of Analog Filters: Passive, Active RC, and Switched Capacitor'. Englewood Cliffs, NJ: Prentice-Hall, 1990, chs. 5/7.
- [5]. Yan Li, Carmen C. Y. Poon and Yuan-Ting Zhang, "Analog Integrated Circuit Design for Processing Physiological Signals", *IEEE Reviews in Biomedical Engineering*, vol.3, 2010
- [6]. Q. Huang and M. Oberle 'A 0.5-mW Passive Telemetry IC for Biomedical Applications' *IEEE J. of Solid-State Circuits*, vol. 33 no. 7, July 1998.
- [7]. K. Nagaraj, "A parasitic-insensitive area-efficient approach to realizing very large constants in switched-capacitor circuits," *IEEE Trans. Circuits Syst.*, vol. 36, no. 9, pp. 1210-1216, Sep. 1989.
- [8]. N. A. Radev and K. P. Ivanov, "Comparative analysis of two gain- and offset-compensated very large time constant switched-capacitor integrators," *Proc. Int. Conf. Microelectronics (ICM 2000)*, pp. 51-54, Oct. 2000.

- [9]. E. Sanchez-Sinencio, "Continuous-time filters from 0.1Hz to 2.0GHz," Tutorial: ISCAS 2004.
- [10]. R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," IEEE Circuits and Devices Magazine, Vol. 1, pp. 20-32, March 1985.
- [11]. J. Silva-Martinez and J. S. Suner, "Very low frequency IC filters," Proceedings of the 38<sup>th</sup> Midwest Symposium on Circuits and Systems, Vol. 2, pp. 1325-1328, Aug. 1995.
- [12]. X. Qian, Y. P. Xu, and X. Li, "A CMOS continuous-time low-pass notch filter for EEG systems," Analog Integr. Circuits Signal Process., vol. 44, no. 3, pp. 231-238, 2005.
- [13]. C. Hsu, M. Ho, Y. Wu, and T. Chen, "Design of low-frequency low-pass filters for biomedical applications," IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS), pp. 690-695, 2006.
- ‘for Active-RC ’
- [14]. B. K. Casper, D. J. Comer, and D. T. Comer, "An Integrable 60-Hz Notch Filter," IEEE Trans. on circuits and systems-II, Vol. 46, No. 1, pp. 74-77, Jan. 1999.
- [15]. A. Durham, W. Redman-White, and J. Hughes, "High-linearity continuous time filter in 5-V VLSI CMOS," IEEE J. Solid-State Circuits, vol. 27, pp. 1270-1276, Sep. 1992.
- [16]. C. Ma, P. Mak, M. Vai, P. Mak, S. Pun, W. Feng, and R. P. Martins, "Frequency-bandwidth-tunable powerline notch filter for biopotential acquisition systems," Electron. Lett. vol. 45, no. 4, Feb. 2009.

- [17]. C. Ma, P. Mak, M. Vai, P. Mak, S. Pun, W. Feng, and R. P. Martins, "A 90nm CMOS bio-potential signal readout front-end with improved powerline interference rejection," *IEEE Int. Symp. Circuits Syst. (ISCAS 2009)*, pp. 665-668, May 2009.
- [18]. A. Wong, K. Pun, Y. Zhang, and K. Hung, "A near-infrared heart rate measurement IC with very low cutoff frequency using current steering technique," *IEEE Trans. on circuits and systems-I*, Vol. 52, No. 12, pp. 2642-2647, Dec. 2005.
- [19]. C. Enz, E. Vittoz and F. Krummenacher "A CMOS Chopper Amplifier", *IEEE J. Solid-State Circuits*, vol. sc-22, no.4, pp.335-342, June 1987.
- [20]. Yu, Jonathan, "Charge Injection and Clock Feedthrough" MS Theses. San Jose State University, 2010.
- [21]. E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation", *IEEE J. Solid-State Circuits*, vol.12, no.3, pp.224-231, June 1977.
- [22]. Y. Haga, H. Zare-Hoseini, L. Berkovi and I. Kale, "Design of a 0.8 volt fully differential CMOS OTA using the bulk-driven technique", *IEEE International Symposium in Circuits and Systems*, pp. 220-223, May 2005.
- [23]. E. Rodriguez- Villegas, A. Yufera and A. Rueda, "A 1.25 v micro power Gm-C filter based on FGMOS transistors operating in weak inversion", *IEEE J. Solid-State Circuits*, vol.39, no.1, pp.100-111, Jan 2004
- [24]. A. Antoniou, "Realization of gyrators using operational amplifiers, and their use in RC-active-network synthesis," *IEE Proc.*, vol. 116, no. 11, pp. 1838-1850, Nov. 1969.



- [25]. H. alzaher and M. Ismail, 'Digitally tuned analogue integrated filters using R-2R ladder', *Electronics Letters* 2000.
- [26]. R. Senani and D. Bhasjar, 'Single Op-Amp Sinusoidal Oscillators Suitable for Generation of Very Low Frequencies', *IEEE trans. on instrumentation and measurement*, vol.47 no.2, pp. 777-779, August 1991.
- [27]. A. Elwakil, 'Systematic Realization Low-Frequency Oscillators Using Composite Passive-Active Resistors', *IEEE trans. On instrumentation and measurement*, vol.47 no.2, pp. 584-586, April 1998.
- [28]. D. Bhashar and R. Senani, 'New CFOA-Based Single-Element-Controlled Sinusoidal Oscillators', *IEEE tran. on instrumentation and measurement*, vol. 55 no.6, pp. 2015-2021, December 2006.
- [29]. H. Alzaher, 'A new CMOS Channel Select Filter for Dual Mode Bluetooth/WLAN Direct-Conversion Receiver', *Analog Integrated Circuit Signal Processing*, vol 63 no 1, pp. 53-58, 2010.
- [30]. Y. Lin, 'a new architecture of constant- $g_m$  rail-to-rail input stage for low voltage low power cmos op amp' *MS thesis*, The Ohio State University, March 2010.
- [31]. V. Cheung, H. Luong, M. Chan 'A 0.9-V 0.2- $\mu$ W CMOS single-Op-Amp-based switched-Op-Amp  $\Sigma\Delta$  modulator for pacemaker applications' *IEEE International Symposium on Circuits and Systems*, ISCAS vol.5 2002.
- [32]. E. Lopez-Morillo, R. Carvajal, F. Munoz, H. Gmili, A. Lopez- Martin, J. Ramirez-Angulo, E. Rodriguez-Villegas, 'A 1.2 V 140 nW 10 bit sigma-delta modulator for electroencephalogram applications'. *IEEE Trans. Biomed. Circuits Syst.* Vol. 2 no. 3 223–230, Sep 2008.

- [33]. E. Camacho-Galeano, C. Galup-Montoro, and M. Schneider, 'A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology'. *IEEE Trans.of Circuit and Systems*, vol. 52 no. 2 pp 61-65, February 200.
- [34]. A. Plaza, 'Nano-ampere Supply Independent Low-Voltage Current Reference'. *Faible Tension Faible Consumption (FTFC) Conference*, pp 9-11, June 2011.
- [35]. R. Jacob Baker, 'CMOS circuit Design, Layout and Simulation'. *Wiley-Interscience, IEEE Press*, 2<sup>nd</sup> Edition 2008.

## VITA

Yaqub Alhussain Yahya Mahnashi was born in Alquful in Jazan Province and he is a Saudi nationality. He is a graduate student in Electrical Engineering Department at King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, Saudi Arabia. He received his bachelor's degree in Electrical Engineering from the same university in June 2008. He joined Electrical Engineering Department, KFUPM, as a graduate assistant in March 2009.

**Current Address:**

King Fahd University of Petroleum & Minerals  
Dhahran 3126, Saudi Arabia.

**Permanent Address:**

AlQuful Village, Jazan , Saudi Arabia

**Telephone:**

+966 3 860 1376  
+966 7 332 0930

**Email:**

ymahnashi@gmail.com