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Scheduling and allocation in high-level synthesis using stochastic techniques
MICROELECTRONICS JOURNAL 27 (8): 693-712 NOV 1996

Abstract

High-level synthesis is the process of automatically translating abstract behavioral models of digital systems to implementable hardware. Operation scheduling and hardware allocation are the two most important phases in the synthesis of circuits from behavioral specification. Scheduling and allocation can be formulated as an optimization problem. In this work, a unique approach to scheduling and allocation problem using the genetic algorithm (GA) is described. This approach is different from a previous attempt using GA (Wehn *et al., IFIP Working Conference on Logic and Architecture Synthesis*, Paris, 1990, pp. 47–56) in many respects. The main contributions include: (1) a new chromosomal representation for scheduling and for two subproblems of allocation; and (2) two novel crossover operators to generate legal schedules. In addition the application of tabu search (TS) to scheduling and allocation is also implemented and studied. Two implementations of TS are reported and compared. Both genetic scheduling and allocation (GSA) and tabu scheduling and allocation (TSA) have been tested on various benchmarks and results obtained for data-oriented control-data flow graphs are compared with other implementations in the literature. (A discussion on GSA was presented at the European Design Automation Conference Euro-DAC'94 in Grenoble, France, and TSA at the International Conference on Electronics, Circuits and Systems — ICECS'94 in Cairo, Egypt.) A novel interconnect optimization technique using the GA is also realized.