Computer Engineering Department Research Profile

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Computer Engineering Department

King Fahd University of Petroleum & Minerals

Engineering Faculty

- **20 Professorial Rank faculty members**
  - 2 Full Professor
  - 2 Associate Professor
  - 16 Assistant Professor
- **6 lecturers**

rch Areas

- Data Communications & Computer Networks.
- Computer Applications: Robotics, Interfacing, Data acquisition, Machine learning, Data Mining.
- Digital Design Automation & VLSI System Design & Test.
- Computer Architecture & Parallel Processing.
- Computer Arithmetic & Cryptography.

Research Projects: Data ions & Computer Networks

- Wireless Multi-hop Voice over IP over Wi-Fi using Client-Server UDP (user datagram protocol).
- Mobile Patient using sensor network.
- Wireless Local Area Networks Integration for Mobile Networks Operators.
- eTourism Promoter – An Internet Assisted Location Tracker and Map Reader for Tourists.
- A Framework for Integration of Web-based Network Management and Management by Delegation.
- Radio Resource Management and QoS Control for Wireless Integrated Services Networks.
- Adaptive TCP Mechanisms for Wireless Networks.
- Engineering Modern Iterative Heuristics to Solve Hard Computer Network Design Problems.

Research Projects: Computer

- Design of a wireless safety system for smart kitchen.
- Predicting log properties from seismic data using abductive networks.
- Design of an Intelligent Tele-robotic System.
- Designing and building a mobile emergency warning system for patients under health care.
- Context aware energy management system.

Research Projects: Design & VLSI System Design & Test.

- Iterative Heuristics for Timing & Low Power VLSI Standard Cell Placement.
- Parallelization of Iterative Heuristics for Low Power VLSI Standard Cell Placement.
- Efficient Test Relaxation Based Static Test Compaction Techniques for Combinational and Sequential Circuits.
- Efficient Test Data Compression Techniques for Testing Systems-on-Chip.
- Segmented Addressable Scan Architecture for Effective Test Data Compression.

Research Projects: Design & VLSI System Design & Test.

- Development of Digital Circuit Techniques for Clock Recovery and Data Re-Timing for High Speed NRZ Source-Synchronous Serial Data Communications.
- Fast context switching configurable architectures supporting dynamic reconfiguration for computation intensive applications.
- Development of Integrated Micro-electronic Heavy Metal Sensors for Environmental Applications.
- Multi-objective Finite State Machine Encoding using Non-Deterministic Evolutionary Algorithms targeting area, low power and testability.
- Design and Implementation of Scalable Interconnect Efficient LDPC Error Correcting Codes.

Non-Deterministic Iterative Solve VLSI CAD Problems

- CAD Problems such as Floorplanning, Placement, Routing, Scheduling, etc., require an enormous amount of computation time.
- Iterative Heuristics such as Genetic Algorithms, Tabu Search, Simulated Evolution, and others have been found effective in solving several NP-hard optimization problems.
- **Objective**: To use a cluster of PCs to solve multi-objective VLSI CAD problems in order to improve quality and reduce run-time.

o employ a Cluster of PCs to mputationally Intensive Tasks

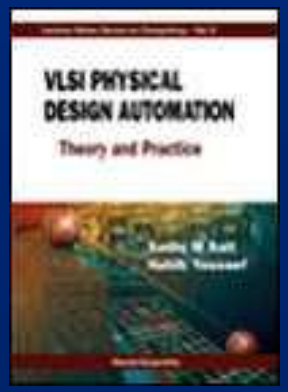
- Clusters of low end PCs are easy to build.
- Tools such as MPI and PVM are available for message passing.
- Tools such as gprof, Intel's VTUNE Performance Analyzer, etc., are used for generating profiles for serial codes and determining the part of the code that has the bottlenecks.
- Iterative algorithms are non-deterministic, and dividing work load, i.e. partitioning the search space, is a challenge.
- The parallelizing model (i.e., Partitioning, Communication, Agglomeration and Mapping) is very well-defined for numerical problems, which are mostly deterministic. This is not the case for Iterative heuristics, which are non-deterministic.

in our Current Cluster

- **MPICH Library** provides a flexible implementation of MPI for easier message-passing interface development on multiple network architectures.
- **Intel® Trace Collector 5.0** applies event-based tracing in cluster applications with a low-overhead library. Offers performance data, recording of statistics, multi-threaded traces, and automatic instrumentation of binaries on IA-32.
- **Intel® Trace Analyzer 4.0** provides visual analysis of application activities gathered by the Intel Trace Collector.
- TotalView (MPICH) is also used for observing communication between processors.
- Also used in Condor (for scheduling jobs on the cluster).

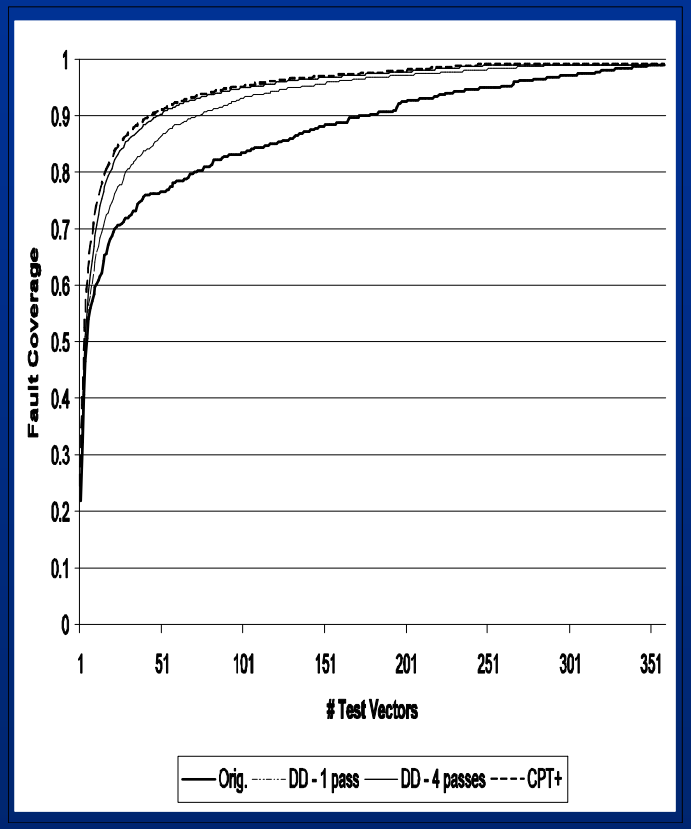
p to Intel's R&D

- COE Department has faculty experienced in VLSI Design.
- Two books in the area of iterative algorithms and VLSI Design have been authored by the department faculty.
- The Technology Center being proposed in RI will have the state-of-art tools and equipment.
- Faculty and students currently interested in HPC and parallelization of heuristics can work together to address industrial and real-world problems.



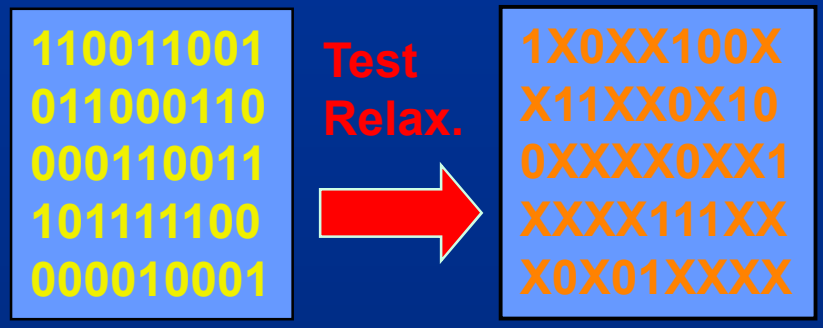
Test Compaction & Compression for Comb. & Seq. Circuits

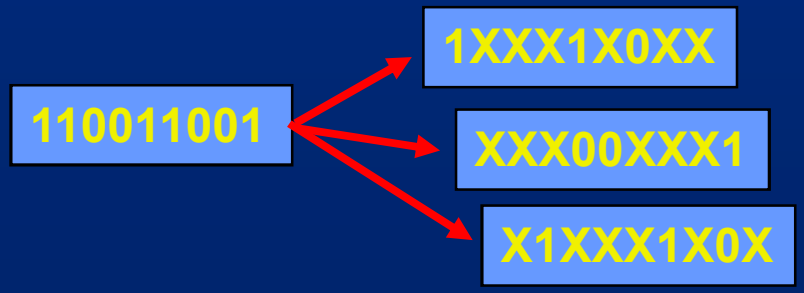
- **SOC Testing Challenges**
  - Reduce amount of test data.
  - Reduce time a defective chip spends on a tester.
- **Test Compaction & Compression**
  - Reduce the size of a test set as much as possible.
- **Test vector reordering for combinational circuits.**
  - Steepen the curve of fault coverage vs. number of test vectors.



Compaction & Compression for Comb. & Seq. Circuits

- **Efficient Test Relaxation for Combinational & Sequential circuits**
  - Enabling technology for test Compaction & Compression
  - Test power reduction
- **Developed efficient test compaction techniques based on test relaxation.**
- **Test Vector Decomposition**
  - Maximizes test compaction by vector clustering techniques
  - Maximizes test width-based compression techniques.





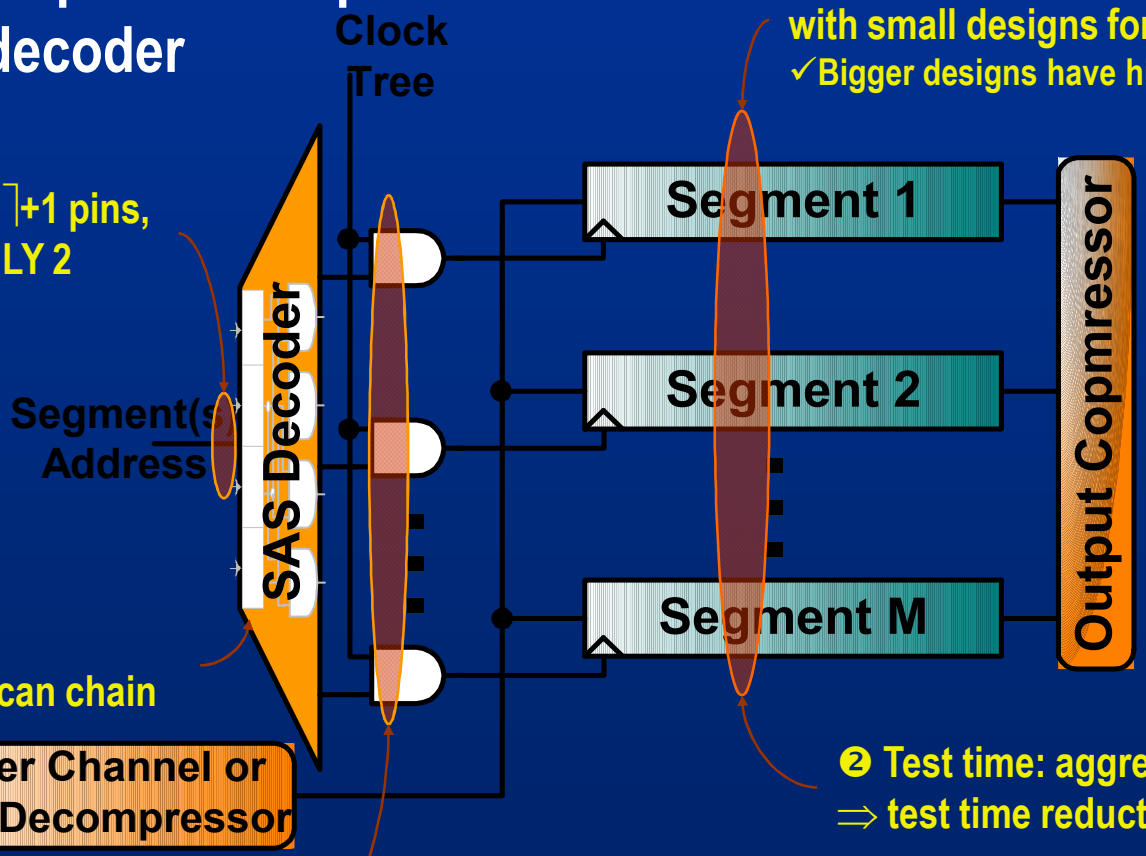
ddressable Scan: Scan Test

- **Test data volume challenge**
  - Limited IOs & unlimited increase in transistors
  - Exponential increase in test data volume
- **Tester pin count challenge**
  - Tester cost is almost linear in number of pins
- **Test time challenge**
  - Critical path
  - Hard to parallelize test loading massively
- **Test power challenge**
  - High activity leading to high power consumption.

Addressable Scan

- Aggressive parallelization of scan chains
- Reconfigurable partial compatibilities
- Special SAS decoder

❶ Data volume: 10x ~ 20x compression with small designs for both SAF and TDF
✓Bigger designs have higher compression



❸ Pin count: $2\times\lceil \log_2 S \rceil+1$ pins,
✓can be reduced to ONLY 2

❹ Overhead:
✓few gates per scan chain

❷ Test time: aggressive parallelization
⇒ test time reduction

❺ Power consumption
✓selective clocking

lume & Test Time (Delay test)

Total Data Volume		98 Mb	Compression Ratio
SAS Data Volume	32 Segments	7.7 Mb	12x
	64 Segments	5.3 Mb	17x
	128 Segments	4.5 Mb	22x
	256 Segments	3.6 Mb	27x

$Ms of annual test cost savings

Research Projects: Computer & Parallel Processing

- Load Balancing for Parallel Visualization of Blood Head Vessel Angiography on Cluster of PCs.
- Shared Channels in Interconnection Networks.
- Study of modified Multistage Interconnection Networks for Networks-on-Chips.
- Design of a Simulator for a Class of Dynamic Execution Processors.
- Beyond Instruction-Level Parallelism in Processor Architecture.
- Design and Performance Evaluation of a Distributed Crossbar Scheduler.
- Software Pipelining for Reconfigurable Instruction Set Processors.

Research Projects: Computer Cryptography

- High-Performance Arithmetic for Cryptographic Applications.
- Design of efficient integrated circuits for the inverse computation in different finite fields.
- Design of Elliptic Curve Cryptography Architectures using parallel multipliers.
- Secure reliable storage system.
- Design, Analysis, and FPGA prototyping of High-Performance Arithmetic for Cryptographic Applications.

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