An Iterative Heuristic for State Justification in Sequential Automatic Test Pattern Generation

Aiman H. El-Maleh   Sadiq M. Sait   Syed Z. Shazli
Department of Computer Engineering
King Fahd University of Petroleum and Minerals
Dhahran, Saudi Arabia

Outline

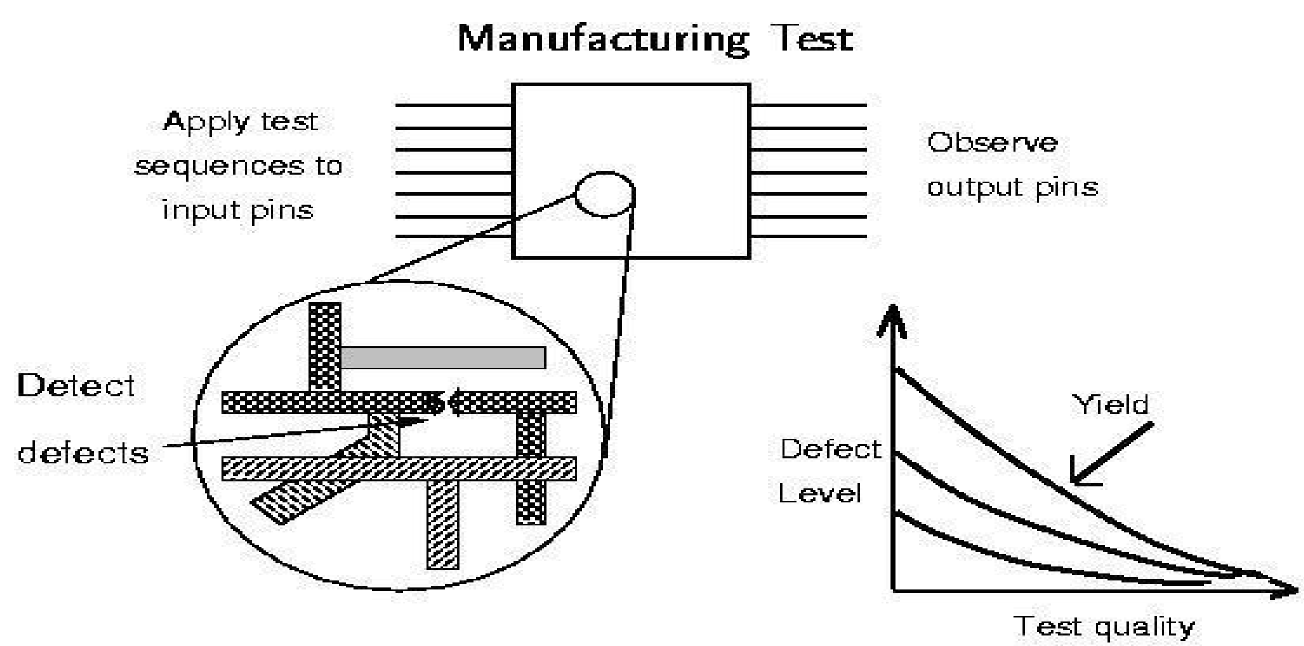
- Motivation
- Test Pattern Generation for Sequential Circuits
- Genetic Algorithms (GA)
- Problem Definition
- The Proposed Approach
- Experiments and Results
- Contributions
- Future Directions

Present and Future*

	1997 -2001	2003 - 2006
Feature size (micron)	0.25 - 0.15	0.13 - 0.10
Transistors/sq. cm	4 - 10M	18 - 39M
Pin count	100 - 900	160 - 1475
Clock rate (MHz)	200 - 730	530 - 1100
Power (Watts)	1.2 - 61	2 - 96

* SIA Roadmap, IEEE Spectrum, July 1999

Testing Principle



Complexity of Sequential Circuits

- A sequential circuit has memory in addition to combinational logic.
- Test for a fault in a sequential circuit is a sequence of vectors, which
    - Initializes the circuit to a known state
    - Activates the fault, and
    - Propagates the fault effect to a primary output

Genetic Algorithms (GAs)

- Basic Idea: Population improves with each generation.
  - Construction of initial population
  - Fitness criteria
  - Parent selection
  - Crossover and mutation
  - Replacement policy

GAs for Test Generation

- Population: A set of input vectors or vector sequences.
- Fitness function: Based on Fault or Logic simulation of candidate vectors or sequences
- Regeneration rules (heuristics): Members with higher fitness function values are selected to produce new members via transformations like mutation and crossover.

Problem Definition

- State Justification: Process of finding a sequence of inputs that will drive the state machine from the reset (or unknown) state to the present state required by the test.
- The most time consuming step in sequential ATPG

Existing Solutions

- Deterministic Algorithms:
  - State justification involves backtracking
  - More effective for control-dominant circuits
  - Able to identify redundant faults
- Simulation-based Approaches:
  - Processing occurs in forward direction only
  - More effective for data-dominant circuits
  - Unable to identify redundant faults

Existing Solutions

- A Hybrid Approach is needed
  - Deterministic algorithms for fault activation and propagation
  - State justification using Simulation-based approaches

The Approach used in [Hsiao 98]

- Test sequences are generated randomly and each chromosome in the GA corresponds to a sequence of TVs
- Each vector in a sequence is logic simulated to get the state reached. This is compared with all the desired flip-flop assignments

The Approach used in [Hsiao 98]

Å Objective:

  ï To engineer a state justification sequence by ógeneticallyô combining candidate sequences

Å If a sequence was found, it was appended to the test set

Å Else, search was aborted and the next target state was picked

pproach used in [Hsiao 98]

Desired state 10x10x

V_4	V_3	V_2	V_1		
0101	1011	1100	0110	001100	Fit (P_1) = 3 / 4
1101	0011	0100	1110	101001	Fit (P_2) = 3 / 4
0101	0011	0100	0110	101101	Fit (Child) = 1

The Approach used in [Hsiao 98]

- Length of the sequence is a multiple of the sequential depth of the circuit
- The fitness function matches only the last state reached, with the desired state.

Drawbacks of the approach

Å Fixed length sequences

Å Length of the sequence depends on structural sequential depth of the circuit

Å Quality of intermediate states reached is not considered while justifying a target state

The Proposed Approach

Å We apply GA while moving from a state to a state

Å Hence, the chromosome consists of a single vector instead of a sequence of vectors

Å State justification sequences are genetically engineered vector-by-vector

The Proposed Approach

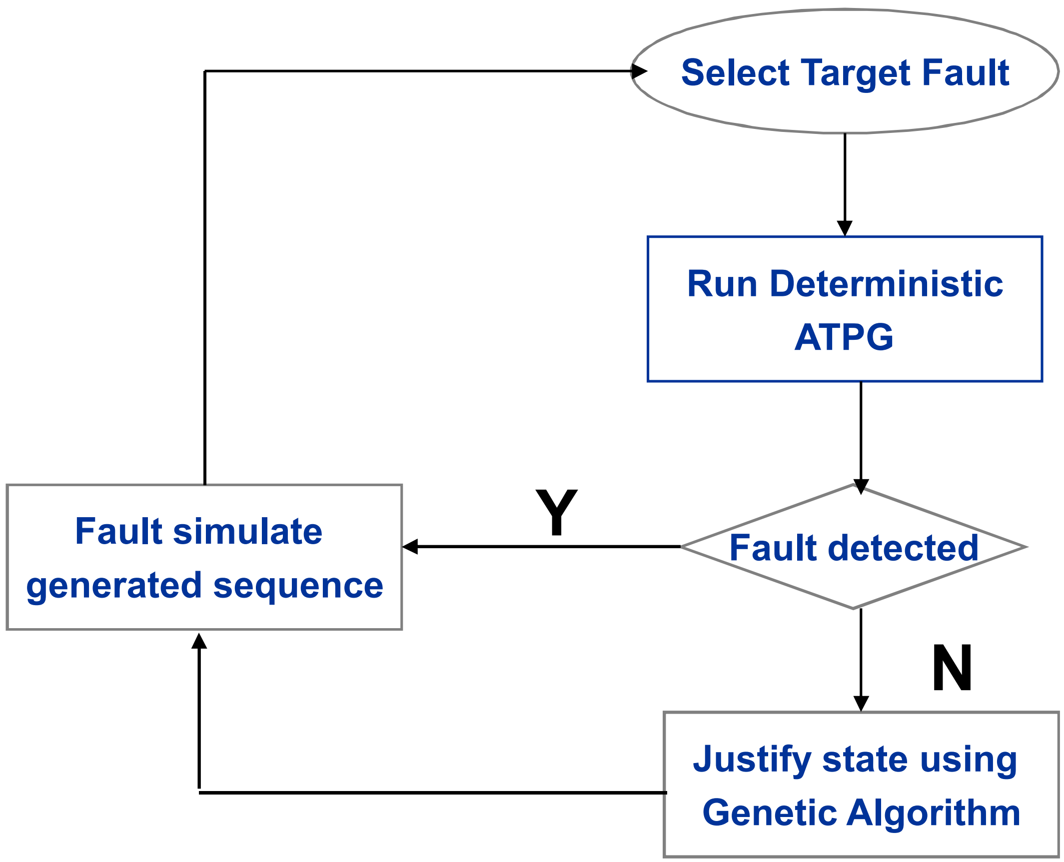
Reset state 0000 **Target state 11x0**

C1: 010011	**0001**	**Fit(P1) = 0 / 3**
C2: 110101	**0010**	**Fit(P2) = 1 / 3**
C3: 010101	**0110**	**Fit(C) = 2 / 3**

010101 is added to the state justification sequence

0110 becomes the new reset state

Proposed Hybrid Framework



The Proposed Approach

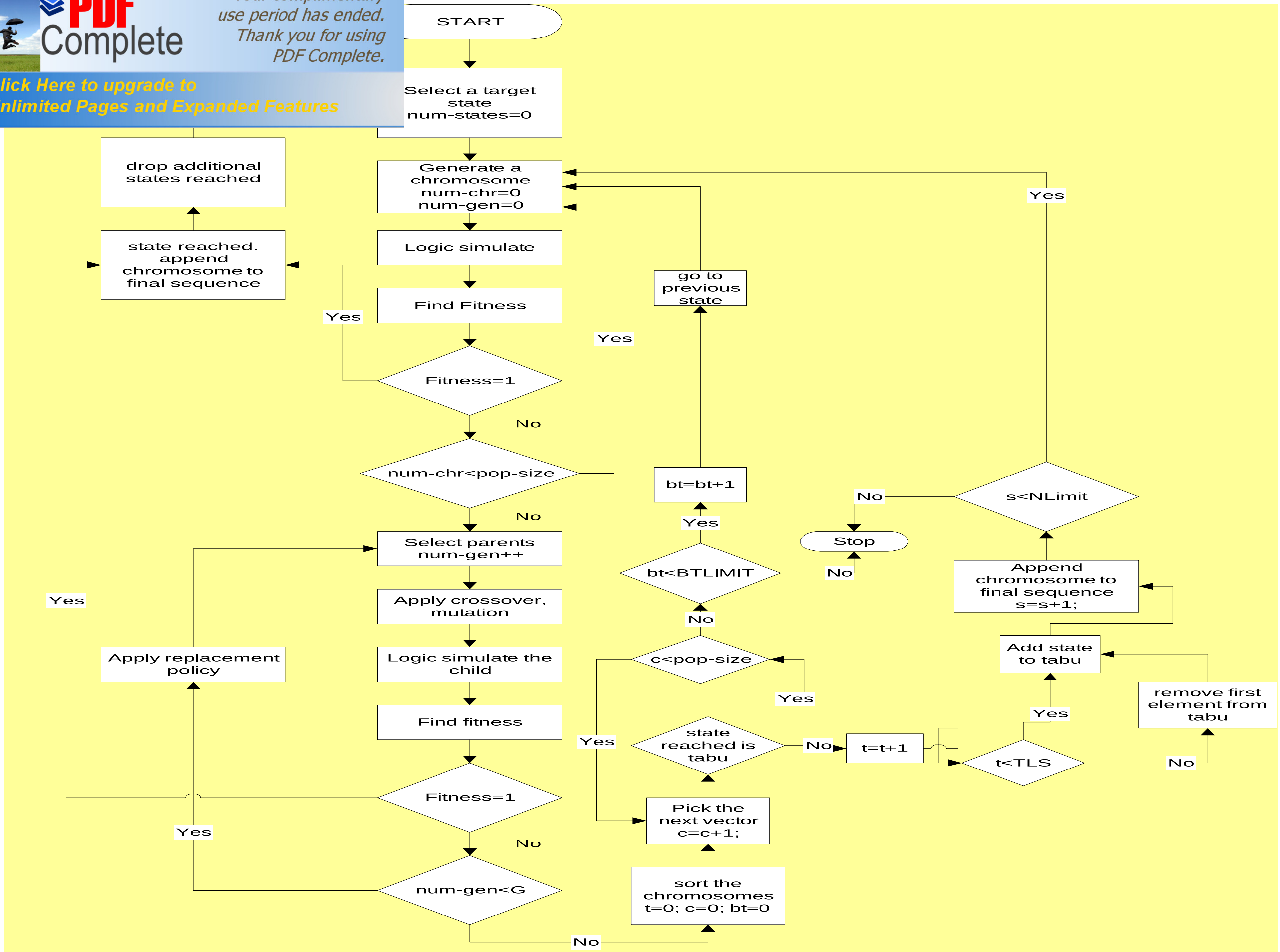
Å A minimum limit (Nlimit) on the number of states to be traversed for reaching an objective state is fixed

Å A backtrack limit is also fixed

Å Search continues for a state if either the state is found or one of the above limits exceeds

The Proposed Approach

- A Tabu List containing the last visited states is maintained.
- This is done to disallow moves which can result in a recycle
- Fault simulator HOPE was used and simulations were run on SUN ULTRA 10 stations


START
Select a target state num-states=0
Generate a chromosome num-chr=0 num-gen=0
Logic simulate
Find Fitness
Fitness=1
num-chr<pop-size
Select parents num-gen++
Apply crossover, mutation
Logic simulate the child
Find fitness
Fitness=1
num-gen<G
Apply replacement policy
state reached. append chromosome to final sequence
drop additional states reached
sort the chromosomes t=0; c=0; bt=0
Pick the next vector c=c+1;
state reached is tabu
c<pop-size
bt<BTLIMIT
bt=bt+1
go to previous state
Stop
t=t+1
t<TLS
Add state to tabu
remove first element from tabu
Append chromosome to final sequence s=s+1;
s<NLimit
Yes
No

Benchmarks used

circuit	# of PI	# of PO	# of DFF
s1423	17	5	74
s3271	26	14	116
s3384	43	26	183
s5378	35	49	179
s6669	83	55	239
scfRjisdre	27	54	20
s832jcsrre	18	19	31
s510Rjcsrre	20	7	30
s510Rjosrre	20	7	32

Obtaining the list of desired states

- To obtain the list of required states, we ran HITEC for 10^9 backtracks for all the circuits to remove redundant faults.
- Aborted faults are converted to full-scan equivalents
- TV is obtained which detects the fault
- State relaxation

The Parameters used

Å The initial population is randomly generated

Å Rate of crossover is 1

Å Mutation rate is 0.01

Å Single point crossover

Å Roulette-wheel used for selecting parents

Å Three replacement strategies were explored

(n+1) replacement strategy

- In the first strategy, the worst member of the previous generation was replaced by the new chromosome if the new chromosome was fitter.
- Average fitness monotonically increased in every generation

Random-Elitist strategy

- N/2 crossovers in every generation
  where N is the pop. size
- Half of the chromosomes were transferred directly to the next generation
- The other half was selected randomly
- Time taken was more than the first strategy

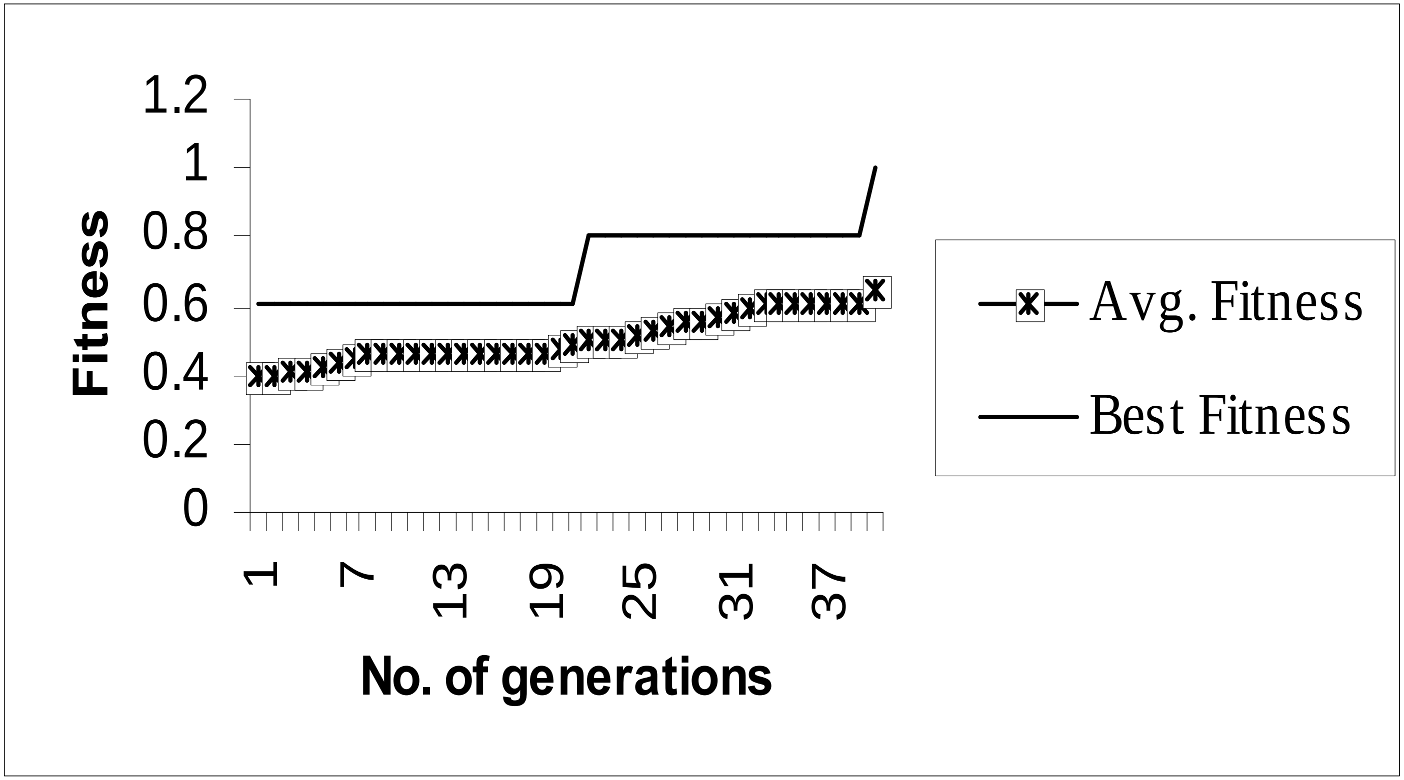
Roulette Elitist strategy

- N/2 crossovers in every generation
- Half of the chromosomes were transferred directly to the next generation
- The other half was selected by roulette wheel
- Time taken was more than the second strategy

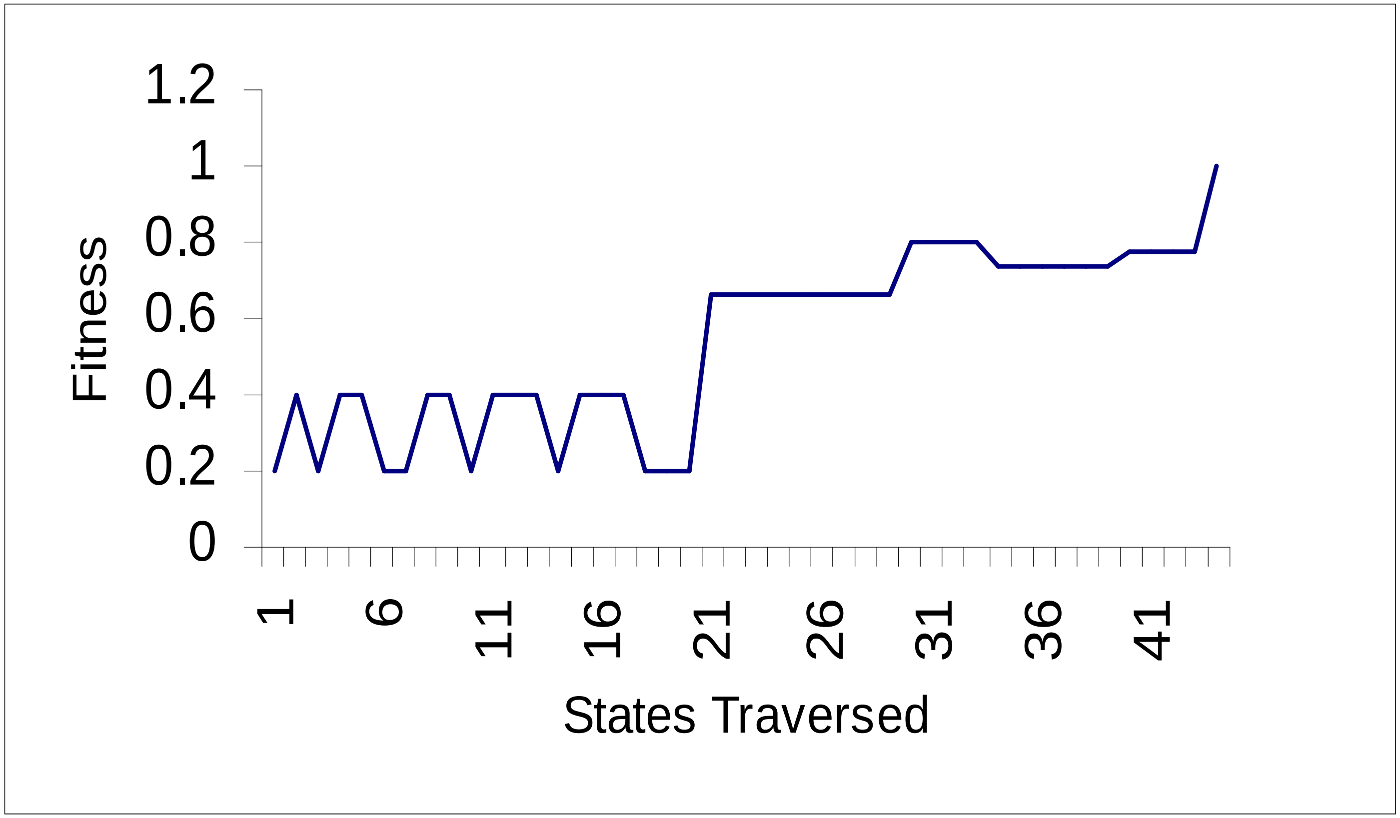
Replacement Policies

circuit	CHR	GEN	BT	NLimit	TLS	(n+1)		Random Elitist		Roulette Elitist	
						SR	Time	SR	Time	SR	Time
s1423	16	100	10	120	150	58	126	19	508	32	748
	32	100	10	120	150	64	365	31	778	49	3586
	64	100	10	120	150	64	572	49	11300	68	13704
s3271	16	800	20	225	150	20	4592	11	5023	15	11214
	32	100	20	225	150	21	6244	18	11805	20	18113
	256	100	20	225	150	21	10625	19	12976	21	109612
s3384	16	800	10	375	150	65	11849	23	14912	34	17445
	64	800	10	375	150	66	23115	51	24905	41	30023
	256	800	10	375	150	66	41225	65	68428	50	100615
s5378	16	400	10	275	150	64	25294	22	84225	45	112610
	32	400	10	275	150	113	29274	53	100324	61	141251
	64	400	10	275	150	115	34893	55	117520	61	161225
s6669	16	10	10	375	150	19	130	19	871	22	914
	16	100	10	375	150	27	503	19	5151	22	8681
	16	400	10	375	150	30	1664	22	17905	22	24668
scfRjisdre	16	100	10	40	150	18	25	17	285	26	836
	64	100	10	40	150	19	42	34	832	43	6700
	256	100	10	40	150	20	114	46	5055	50	48820
s832jcsrre	16	400	100	100	150	7	79	6	77	6	82
	256	400	100	100	150	7	190	7	1946	7	2126
	1024	400	100	100	150	9	360	8	3441	9	4956
s510Rjcsrre	16	400	10	45	150	12	14	8	120	6	140
	256	400	10	45	150	16	132	23	523	23	1208
	512	400	10	45	150	23	260	31	2340	31	5038
s510Rjosrre	16	800	10	45	150	12	92	5	233	4	305
	64	800	10	45	150	19	661	13	1171	11	2841
	256	800	10	45	150	19	2740	17	9870	19	19342

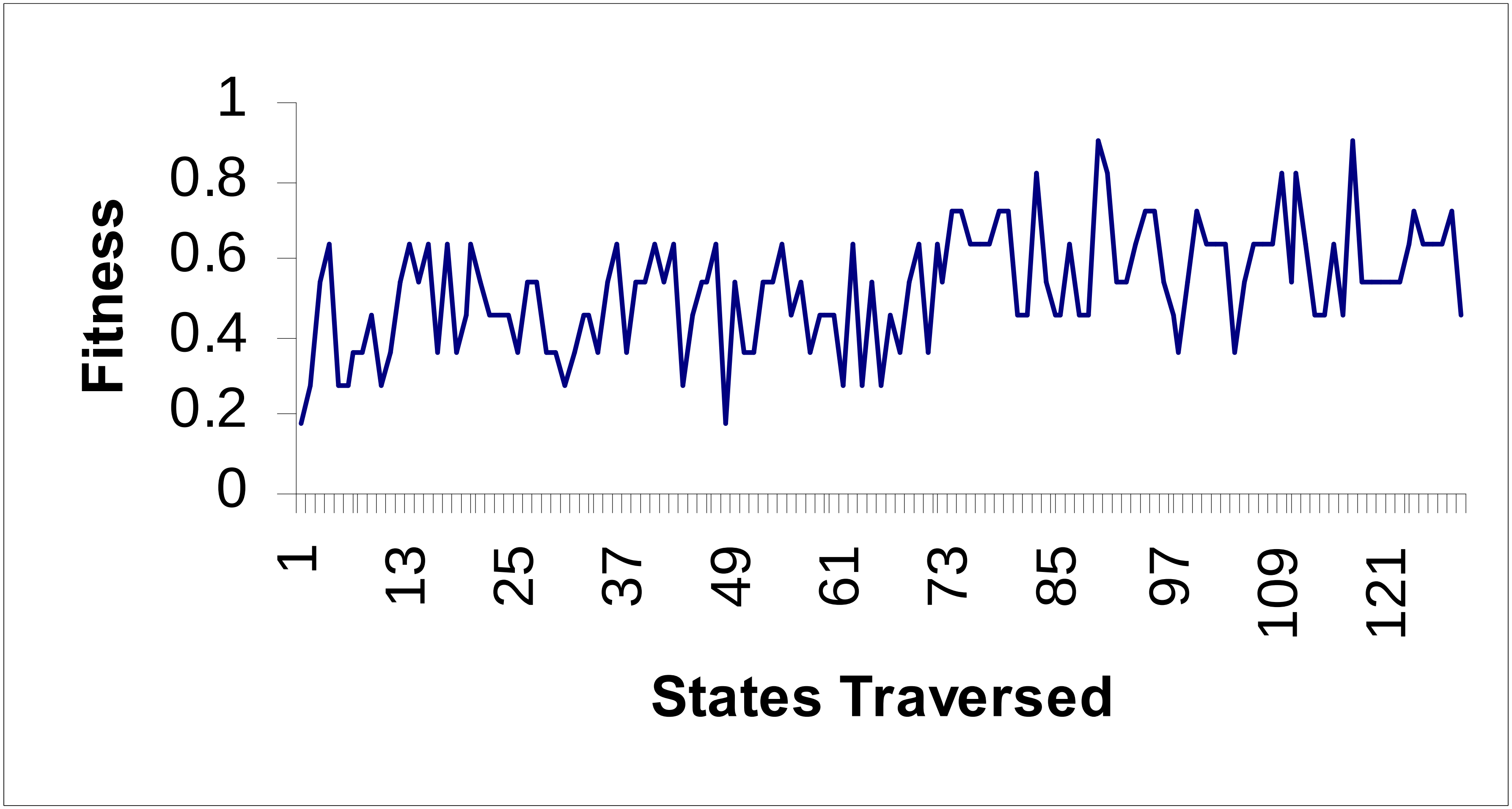
Average and Best Fitness



Quality of the states reached



Quality of the states reached



Effect of population size

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s1423	16	100	10	120	150	58	126
	32	100	10	120	150	64	365
	64	100	10	120	150	64	572
s3271	16	100	10	225	150	19	831
	32	100	10	225	150	21	1244
	256	100	10	225	150	21	2625
s3384	16	800	10	375	150	65	11849
	32	800	10	375	150	66	18122
	64	800	10	375	150	66	23115
	256	800	10	375	150	66	41225
s5378	16	400	10	275	150	64	25294
	32	400	10	275	150	113	29274
	64	400	10	275	150	115	34893
s6669	16	100	10	375	150	22	503
	32	100	10	375	150	23	788
	64	100	10	375	150	23	1349

Effect of population size

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
scfRjisdre	16	100	10	40	150	18	25
	32	100	10	40	150	19	33
	64	100	10	40	150	19	42
	256	100	10	40	150	20	114
s832jcsrre	16	400	100	100	150	7	79
	32	400	100	100	150	7	118
	256	400	100	100	150	7	190
	1024	400	100	100	150	9	360
s510Rjcsrre	16	400	10	45	150	12	14
	32	400	10	45	150	12	77
	256	400	10	45	150	16	132
	512	400	10	45	150	23	260
s510Rjosrre	16	800	10	45	150	12	92
	32	800	10	45	150	16	334
	64	800	10	45	150	19	661
	256	800	10	45	150	19	2740

Effect of no. of generations

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s1423	32	10	10	120	150	46	91
	32	100	10	120	150	64	365
	32	200	10	120	150	68	1457
	32	400	10	120	150	71	2912
	32	800	10	120	150	71	6303
s3271	16	10	10	225	150	12	105
	16	100	10	225	150	19	831
	16	400	10	225	150	21	2455
	16	800	10	225	150	21	4592
s3384	16	10	10	375	150	29	1104
	16	100	10	375	150	45	2687
	16	200	10	375	150	45	4744
	16	400	10	375	150	49	7794
	16	800	10	375	150	65	11849
	16	1200	10	375	150	69	15887
s5378	32	10	10	275	150	51	3125
	32	400	10	275	150	113	29274
	32	800	10	275	150	115	49257

Effect of no. of generations

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s6669	16	10	10	375	150	19	130
	16	100	10	375	150	22	503
	16	400	10	375	150	30	1664
scfRjisdre	16	100	10	40	150	18	25
	16	400	10	40	150	28	108
	16	800	10	40	150	42	183
	16	1400	10	40	150	45	233
s832jcsrre	16	10	10	45	150	5	3
	16	100	10	45	150	6	11
	16	400	10	45	150	6	49
	16	800	10	45	150	7	73
s510Rjcsrre	256	100	10	45	150	14	30
	256	400	10	45	150	16	132
	256	800	10	45	150	20	210
	256	1400	10	45	150	20	1063
s510Rjosrre	32	10	10	45	150	3	5
	32	100	10	45	150	7	81
	32	400	10	45	150	12	167
	32	800	10	45	150	16	334

Effect of no. of generations

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s6669	16	10	10	375	150	19	130
	16	100	10	375	150	22	503
	16	400	10	375	150	30	1664
scfRjisdre	16	100	10	40	150	18	25
	16	400	10	40	150	28	108
	16	800	10	40	150	42	183
	16	1400	10	40	150	45	233
s832jcsrre	16	10	10	45	150	5	3
	16	100	10	45	150	6	11
	16	400	10	45	150	6	49
	16	800	10	45	150	7	73
s510Rjcsrre	256	100	10	45	150	14	30
	256	400	10	45	150	16	132
	256	800	10	45	150	20	210
	256	1400	10	45	150	20	1063
s510Rjosrre	32	10	10	45	150	3	5
	32	100	10	45	150	7	81
	32	400	10	45	150	12	167
	32	800	10	45	150	16	334

Effect of TLS

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s1423	32	400	10	120	150	71	2912
	32	400	10	120	50	71	2966
	32	400	10	120	15	74	3119
s3271	16	800	10	225	150	21	4592
	16	800	10	225	50	21	4627
	16	800	10	225	15	21	4894
s3384	16	800	10	375	150	65	11849
	16	800	10	375	50	65	11703
	16	800	10	375	15	67	16121
s5378	32	400	10	275	150	113	29274
	32	400	10	275	50	113	31127
	32	400	10	275	15	115	31281
s6669	16	400	10	375	150	27	503
	16	400	10	375	50	27	715
	16	400	10	375	15	30	1466
scfRjisdre	16	800	10	40	150	42	183
	16	800	10	40	50	42	355
	16	800	10	40	15	46	533
s832jcsrre	16	400	10	45	150	6	49
	16	400	10	45	50	6	77
	16	400	10	45	15	7	106
s510Rjcsrre	256	400	10	100	150	16	410
	256	400	10	100	50	16	492
	256	400	10	100	15	19	663
s510Rjosrre	32	800	10	45	150	16	334
	32	800	10	45	50	16	416
	32	800	10	45	15	18	441

Effect of Nlimit

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s1423	32	400	10	120	150	71	2912
	32	400	10	500	150	74	9447
s3271	16	800	10	225	150	21	4592
	16	800	10	500	150	21	10654
	16	800	10	800	150	23	22096
s3384	16	800	10	50	150	53	2289
	16	800	10	375	150	65	11849
	16	800	10	500	150	67	16219
s5378	32	400	10	275	150	113	29274
	32	400	10	600	150	115	57135
s6669	16	400	10	50	150	19	130
	16	400	10	375	150	30	1664
	16	400	10	500	150	30	3716
scfRjisdre	16	800	10	40	150	42	183
	16	800	10	100	150	43	533
s832jcsrre	16	400	10	45	150	6	49
	16	400	10	100	150	6	73
	16	400	10	500	150	7	664
s510Rjcsrre	256	400	10	45	150	16	132
	256	400	10	100	150	16	410
	256	400	10	200	150	20	1063
s510Rjosrre	32	800	10	45	150	16	334
	32	800	10	100	150	16	1243
	32	800	10	500	150	19	3717

Effect of BT Limit

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s1423	32	400	200	120	15	75	4217
	32	400	100	120	15	75	4212
	32	400	10	120	15	74	3119
s3271	16	800	200	225	15	21	5042
	16	800	100	225	15	21	4992
	16	800	10	225	15	21	4894
s3384	16	800	200	375	15	68	17714
	16	800	100	375	15	68	17703
	16	800	10	375	15	67	16121
s5378	32	400	200	275	15	115	31311
	32	400	100	275	15	115	31302
	32	400	10	275	15	115	31281
s6669	16	400	200	375	15	30	1723
	16	400	100	375	15	30	1715
	16	400	10	375	15	30	1466
scfRjisdre	16	800	200	40	15	48	735
	16	800	100	40	15	48	735
	16	800	10	40	15	46	533
s832jcsrre	16	400	200	45	15	7	189
	16	400	100	45	15	7	187
	16	400	10	45	15	7	106
s510Rjcsrre	256	400	200	100	15	21	951
	256	400	100	100	15	21	949
	256	400	10	100	15	19	663
s510Rjosrre	32	800	200	45	15	18	460
	32	800	100	45	15	18	462
	32	800	10	45	15	18	441

Best results obtained

circuit	Chromes	Gen	BT	NLimit	TLS	Reached	Time(sec)
s1423	32	400	100	120	15	75	4212
s3271	16	400	10	225	150	21	2455
s3384	16	800	100	375	15	68	17703
s5378	32	400	10	275	15	115	31281
s6669	16	400	10	375	15	30	1466
scfRjisdre	16	800	100	40	15	48	735
s832jcsrre	1024	400	100	100	150	9	360
s510Rjcsrre	512	400	10	45	150	23	260
s510Rjosrre	64	800	10	45	150	19	661

Recommended Parameters

Population size	32
Generations	400
Nlimit	1.5 * (#DFF)
TLS	15
BT Limit	10

Recommended vs. Best

			best results obtained	
c rcuit	# of FF	Target States	states reached	time(sec)
s1423	74	135	75	4212
s3271	116	45	21	2455
s3384	183	102	68	17703
s5378	179	524	115	31281
s6669	239	32	30	1466
s:fRjisdre	20	267	48	735
s832jcsrre	31	57	9	360
s510Rjcsrre	30	114	23	260
s510Rjcsrro	32	114	19	661

Genetic Parameters used in [Hsiao 98]

Å Two-point uniform crossover has been used.

Å The probability of crossover is 1.

Å Any vector in the chrome is replaced with another random vector in mutation

Å The probability of mutation is 0.01

Å Tournament selection mechanism is applied

Å A population size of 32 gave the best results

Å Length of sequence = 4*seq.depth

Comparison with [Hsiao 98]

			approach	in Hsiao 98
circuit	# of	Target	states	time(sec)
	FF	States	reached	
s1423	74	135	50	2743
s3271	116	45	15	1664
s3384	183	102	31	3794
s5378	179	524	45	3133
s6669	239	32	23	1701
scfRj sdre	20	267	25	501
s832jcsrre	31	57	7	120
s510Rjcsrre	30	114	12	61
s510Rjcsrro	32	114	9	62

Comparison with [Hsiao 98]

circuit	TS	gen	approach states reached	in Hsiao 98 time(sec)
s1423	135	50	61	3953
s3271	45	200	18	6319
s3384	102	250	45	21161
s5378	524	100	48	225160
s6669	32	50	24	2209
scfRjisdre	267	100	31	5196
s832jcsrre	57	100	7	2170
s510Rjcsrre	114	100	13	504
s510Rjcsrro	114	100	13	503

Comparison with [Hsiao 98]

Contributions

Å A hybrid ATPG approach for sequential circuits, where both deterministic and GA-based state justification are involved

Å A novel state justification procedure based on GA

Å Genetic engineering of a sequence óvector by vectorô

- ï Advantage of dynamically determining the length of justification sequence
- ï Benefit of taking quality of intermediate states into account

Contributions

Å Comparison of three replacement strategies
  ï (n+1) replacement strategy gave better results
Å Use of Tabu List to prevent the algorithm from visiting previously visited state
Å Sensitivity analysis of the parameters used

Future Directions

Å Experimenting with other heuristics (like Tabu Search)

Å Parallelization of the algorithm (for eg. Fitness evaluation)