DEPOSITION AND CHARACTERIZATION OF POLYFLUORENE / CERIUM OXIDE ORGANIC-INORGANIC THIN FILMS

FARAH HAYATI BINTI HAJI AHMAD

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DEPOSITION AND CHARACTERIZATION OF POLYFLUORENE / CERIUM OXIDE ORGANIC-INORGANIC THIN FILMS

by

FARAH HAYATI BINTI HAJI AHMAD

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TABLE OF CONTENTS

ACKNOWLEDGEMENT ii

TABLE OF CONTENTS iii

LIST OF TABLES vi

LIST OF FIGURES vii

LIST OF SYMBOLS xii

LIST OF ABBREVIATIONS xiv

ABSTRAK xvi

ABSTRACT xvii

CHAPTER 1 INTRODUCTION 1

1.1 Overview 1

1.2 Problem Statement 4

1.3 Objectives of the Study 6

1.4 Scope of the Study 6

1.5 Outline of the Thesis 7

CHAPTER 2 LITERATURE REVIEW 8

2.1 Development of Metal-Oxide-Semiconductor (MOS) Based Device 8

2.1.1 Gate Oxide as Passivation Layer in MOS Devices 8

2.1.2 Influence of Bias on MOS Capacitor 10

2.1.2(a) Flatband 10

2.1.2(b) Accumulation 11

2.1.2(c) Depletion 12

2.1.2(d) Inversion 12

2.1.3 Capacitance Voltage (C-V) Characteristics of MOS Device 13

2.1.4 Scaling and Breakdown of Gate Oxide in MOS Device 15

2.2 Challenges and Current Issues Faced by Gate Oxide 15

2.2.1 Selection of High Dielectric Constant (*k*) Oxide 16

2.3 Cerium Oxide (CeO_2) – General Properties... 18

2.3.1 Cerium Oxide (CeO_2) for Device Application................................. 21

2.4 Polyfluorenes (PFs) – General Properties 28

2.4.1 Polyfluorenes (PFs) for Device Application..................................... 29

2.5 Metal Organic Decomposed (MOD) Method 32

2.5.1 Advantages and Limitations of MOD Method 33

2.6 Thin Film Deposition Method 33

CHAPTER 3 METHODOLOGY 36

3.1 Methodological Approach 36

3.2 Materials, Chemicals and Apparatus 40

3.2.1 Substrate Materials.. 41

3.2.2 Material, Chemical and Apparatus for Substrate Cleaning Process 41

3.2.3 Material, Chemical and Apparatus for Metal Contact Deposition Process.. 43

3.3 Experimental Procedures 44

3.3.1 Substrate Cleaning Process 44

3.3.2 Film Deposition Process 46

3.3.3 Post Deposition Annealing Process 48

3.3.4 Metal Contact Deposition Process 49

3.4 Characterization Method.. 50

3.4.1 X-ray Diffraction (XRD) 52

3.4.2 Field Emission Scanning Electron Microscopy (FESEM) 54

3.4.3 Energy-Dispersive X-ray (EDX) Spectroscopy 56

3.4.4 Atomic Force Microscopy (AFM) 57

3.4.5 Fourier Transform Infrared (FTIR).. 58

3.4.6 UV-visible (UV-VIS) Spectrophotometer 59

3.4.7 Photoluminescence (PL) Spectroscopy 59

3.4.8 Raman Spectroscopy 61

3.4.9 Filmetric (Optical Reflectometer) 62

3.4.10 Capacitance-Voltage (C-V) & Current-Voltage (I-V) Measurement 63

CHAPTER 4 RESULTS AND DISCUSSION 65

4.1 Introduction 65

4.2 Effects of post-deposition annealing temperature (400, 600, 800 and 1000 °C) on CeO_2 Films Deposited on Si Substrate 65

4.3 Investigation on Characteristics of PFs with Different Composition (0.625 mg, 1.25 mg and 2.5 mg) Spin-Coated on Indium Tin Oxide Glass Substrate 92

4.4 Study of Characteristics for Stacking PFs Deposited on CeO_2 Films 101

CHAPTER 5 CONCLUSION AND FUTURE RECOMMENDATIONS 124

5.1 Conclusion 124

5.2 Recommendations for Future Research 127

REFERENCES 129

LIST OF PUBLICATIONS

LIST OF TABLES

Page

Table 2.1 Chemical and physical properties of CeO_2 (Chiu & Chang, 2014; Chiu & Lai 2010; Masalov et al., 2014; Quah et al., 2010; Vangelista, 2017)........ 25

Table 3.1 Specification of Si substrates used for the deposition of CeO_2 and PFs/CeO_2 samples........ 41

Table 3.2 Specification of ITO glass substrates used for deposition of PFs........ 41

Table 3.3 Type of chemical, chemical formula, chemical grade and supplier for substrate cleaning process........ 42

Table 3.4 Type of chemical, chemical formula, chemical grade and supplier for preparation of CeO_2 precursors and PFs solution........ 43

Table 3.5 Type of analysis, machine and model........ 51

Table 4.1 Elemental composition of CeO_2 thin films annealed at different temperatures (400, 600, 800, and 1000 °C)........ 71

Table 4.2 The diffraction angle with respect to the temperature of CeO_2 films that had undergone post-deposition annealing temperatures at 400, 600, 800, and 1000 °C........ 102

LIST OF FIGURES

Page

Figure 2.1 Typical MOS structure possessing metal electrode, oxide layer, and semiconductor substrate. 9

Figure 2.2 Energy band diagram for an ideal n-type MOS capacitor at $V_g = 0$ V (Sze et al., 2007). 10

Figure 2.3 Energy band diagram for an ideal n-type MOS capacitor under accumulation condition (Sze et al., 2007). 11

Figure 2.4 Energy band diagram for an ideal n-type MOS capacitor under depletion condition (Sze et al., 2007). 12

Figure 2.5 Energy band diagram for an ideal n-type MOS capacitor under inversion condition (Sze et al., 2007). 13

Figure 2.6 Schematic illustration of C-V measurement of n-type MOS device. The arrows on the curve are showing the direction of voltage ramp. The regions showing stretch-out and hysteresis are established (Tsirimpis, 2018). 14

Figure 2.7 Lanthanide series (https://courses.lumenlearning.com/ cheminter/chapter/lanthanides-and-actinides/). 18

Figure 2.8 Schematic cubic fluorite crystal structure of CeO_2 (Karl et al., 2018). 19

Figure 2.9 Photocatalytic water splitting in semiconductor photocatalysts (Kong et al., 2018). 22

Figure 2.10 Structures of OLEDs (Kamalasanan et al., 2010). 30

Figure 2.11 Schematic illustration of spin coating (Ricciardulli & Blom, 2020). 34

Figure 2.12 Schematic illustration of dip coating (Ricciardulli & Blom, 2020). 34

Figure 2.13 Schematic illustration of spray coating (Ricciardulli & Blom, 2020). 35

Figure 3.1 Summary of research methodology in this research work. 37

Figure 3.2 Summary of research methodology for phase 1 (CeO_2 on Si). 37

Figure 3.3 Summary of research methodology for phase 2 (PFs on ITO glass). 38

Figure 3.4 Summary of research methodology for phase 1, phase 2, and phase 3 (stacking of PFs on CeO_2). 39

Figure 3.5 Summary of characterization techniques used in this research work. 40

Figure 3.6 Pattern mask measuring 0.08 cm circular shape in diameter. 43

Figure 3.7 Steps of Si substrate cleaning process. 45

Figure 3.8 Spin-coater to deposit the precursor. 47

Figure 3.9 Ceramic boat to put the samples. 48

Figure 3.10 Horizontal tube furnace 21100 for post-deposition annealing. 49

Figure 3.11 Flowmeter for gas flow rate measurement. 49

Figure 3.12 AUTO 306 thermal evaporator for Al metal contact deposition. 50

Figure 3.13 Stages of the thermal evaporator process for metal gate electrode and backside metal contact using Al sources. 50

Figure 3.14 Schematic of X-ray diffraction pattern (Sivia, 2011). 53

Figure 3.15 BRUKER D8 Discover X-ray diffraction machine. 54

Figure 3.16 FEI Nova NanoSEM 450 equipped with Energy-Dispersive X-ray (EDX) spectrometer. 55

Figure 3.17 Atomic Force Microscopy with model of Dimension EDGE, BRUKER. 57

Figure 3.18 Fourier Transform Infrared Spectroscopy system with He-Ne laser. 58

Figure 3.19 UV-Visible-NIR Spectrophotometer (Cary 5000). 59

Figure 3.20 Room temperature Mini PL spectra images with PC connection. 60

Figure 3.21 Raman spectroscopy system. 61

Figure 3.22 Optical Reflectometer system with model of Filmetric F20. 62

Figure 3.23 Keithley 4200A-SCS Semiconductor Parameter Analyser (SPA). 63

Figure 3.24 Probe station with microscope to measure the samples. 64

Figure 4.1 XRD patterns of metal-organic decomposed on CeO_2 thin films subjected to post-deposition annealing at 400, 600, 800 and 1000 °C. 66

Figure 4.2 Coefficient of texture, T_{hkl} for CeO_2 thin films with respect to annealing temperature. 67

Figure 4.3 Crystallite size (D) and microstrain (ε) on CeO_2 thin films. 69

Figure 4.4 A relationship of lattice parameter of CeO_2 thin films as a function of annealing temperature. 70

Figure 4.5 Surface morphology of CeO_2 thin films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 73

Figure 4.6 Cross-sectional images of CeO_2 thin films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 74

Figure 4.7 Total oxide thickness and dielectric constant (inset) obtained for CeO_2 thin films annealed at different temperatures. 74

Figure 4.8 Fourier Transformed Infrared absorbance spectra of CeO_2 thin films in the range of (a) 400-1400 cm^{-1} and (b) 1500-4000 cm^{-1}. 76

Figure 4.9 Surface topography of CeO_2 thin films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 77

Figure 4.10 RMS roughness of CeO_2 thin films annealed at different temperatures. 78

Figure 4.11 Raman spectra of CeO_2 thin films in the range of (a) 200-500 cm^{-1} and (b) 580-900 cm^{-1}. 80

Figure 4.12 Room temperature photoluminescence (PL) spectra of CeO_2 thin films annealed at different temperatures. 82

Figure 4.13 Direct and indirect bandgap (E_g) for CeO_2 thin films calculated using Kulbelka-Munk theory 84

Figure 4.14 1 MHz capacitance-voltage characteristics of MOS capacitor based on CeO_2 thin films. Inset shows the presence of dual switching behaviour for the thin film annealed at 1000 °C. 85

Figure 4.15 Changes in effective oxide charge and slow trap density in the CeO2 thin films with respect to annealing temperature. 88

Figure 4.16 A relationship between interface trap density and energy level of the CeO_2 thin films. 89

Figure 4.17 Current-voltage characteristics of CeO_2 thin films annealed at different temperatures. 91

Figure 4.18 Field emission scanning electron microscopy (FESEM) images of (a) 0.625 mg, (b) 1.250 mg, and (c) 2.500 mg polyfluorene (PFs) coated ITO samples. 92

Figure 4.19 Three-dimensional atomic force microscopy (AFM) images of (a) 0.625 mg, (b) 1.250 mg, and (c) 2.500 mg PFs coated ITO samples. Figure 4.19(d) presents root-mean-square (RMS) roughness of the samples. 94

Figure 4.20 X-ray diffraction (XRD) peaks of PFs coated samples. 95

Figure 4.21 Photoluminescence emission spectra detected for (a) 0.625 mg, (b) 1.250 mg, and (c) 2.500 mg PFs coated samples. 97

Figure 4.22 Current-voltage (I-V) characteristics of 0.625 mg, 1.250 mg, and 2.500 mg PFs coated Al/PFs/ITO structures. 99

Figure 4.23 Energy band gap values calculated for different PFs coated samples. 100

Figure 4.24 Energy band diagram in (ai)-(ci) flatband and (aii)-(cii) forward bias condition for 0.625 mg, 1.250 mg, and 2.500 mg PFs coated Al/PFs/ITO structures. 101

Figure 4.25 XRD patterns of stacking of PFs on CeO_2 films annealed at 400, 600, 800, and 1000 °C. 103

Figure 4.26 A relationship of lattice parameter of PFs/CeO2 thin films as a function of annealing temperature 105

Figure 4.27 Crystallite size (*D*) and microstrain (ε) of stacking PFs on CeO_2 films. 106

Figure 4.28 Surface morphology of stacking PFs on CeO_2 films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 107

Figure 4.29 Surface morphology of CeO_2 thin films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 107

Figure 4.30 Cross-sectional images of stacking PFs on CeO_2 thin films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 108

Figure 4.31 Cross-sectional images of CeO_2 thin films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 108

Figure 4.32 Total oxide thickness obtained for stacking PFs on CeO_2 films annealed at different temperatures. 108

Figure 4.33 Fourier Transform Infrared absorbance spectra of stacking PFs on CeO_2 films in the range of (a) 400- 1400 cm^{-1} and (b) 1500-4000 cm^{-1}. 110

Figure 4.34 Surface topography of stacking PFs on CeO_2 films annealed at (a) 400 °C, (b) 600 °C, (c) 800 °C, and (d) 1000 °C. 112

Figure 4.35 RMS roughness of stacking PFs on CeO_2 films annealed at different temperatures. 113

Figure 4.36 Raman spectra of stacking PFs on CeO_2 films in the range of (a) 200-500 cm^{-1} and (b) 1000-1800 cm^{-1}. 115

Figure 4.37 Breathing motion of the pentagon within the monomer (Lim et al., 2016). 116

Figure 4.38 Room temperature photoluminescence (PL) spectra of stacking PFs on CeO_2 films annealed at different temperatures. 118

Figure 4.39 Direct and indirect bandgap (E_g) for stacking PFs on CeO_2 films calculated using Kulbelka-Munk theory. 120

Figure 4.40 1 MHz capacitance-voltage characteristics of MOS capacitor based on (a) CeO_2 films and (b) stacking PFs on CeO_2 films. 121

Figure 4.41 Dielectric constant value of (a) CeO_2 films and (b) stacking PFs on CeO_2 films. 122

Figure 4.42 Current-voltage characteristics of (a) CeO_2 films and (b) stacking PFs on CeO_2 films annealed at different temperatures. 123

LIST OF SYMBOLS

Å	Angstrom
A_G	Capacitor area (cm^2)
C_{ox}	Oxide capacitance (pF)
c	Speed of light
d_{hkl}	Inter-plane distance between the two neighboring lattice planes
D	Crystallite size (nm)
D_{it}	Interface trap density (eV^{-1} cm^{-2})
E_g	Energy gap
I	Current (A)
J	Current density (A cm^{-2})
k	Dielectric constant
ρ	Film density
hkl	Miller indices
$h\nu$	Energy of photon
T_{hkl}	Coefficient of texture
V_g	Gate voltage
ε	Microstrain
θ	Bragg's angle
λ	Wavelength
E_C	Conduction band (eV)
E_F	Fermi energy (eV)
E_V	Valence band (eV)
nm	Nanometer
µm	Micrometer
cm	Centi meter

q	Charge (C)
ρ	Oxide density (g cm^{-2})
Q_{eff}	Effective oxide charge
V	Voltage (V)
V_B	Breakdown voltage (V)
V_{os}	Oxygen vacancy
STD	Slow trap density (cm^{-2})
T	Temperature

LIST OF ABBREVIATIONS

AFM	Atomic force microscope
Al	Aluminium
a.u.	Arbitrary unit
C-V	Capacitance-Voltage
CH_3COOH	Acetic acid
CH_3OH	Methanol
DC	Direct current
EDX	Energy dispersive X-ray electron microscopy
eV	Electron volt
FESEM	Field emission scanning electron microscopy
FTIR	Fourier Transform Infrared Spectrometer
FTO	Fluorine doped tin oxide
ICCD	International conference for diffraction data
ITO	Indium tin oxide
I-V	Current-Voltage
LED	Light-emitting diode
MOD	Metal organic decomposition
MOS	Metal-oxide-semiconductor
N_2	Nitrogen
O_2	Oxygen
PF	Polyfluorene
PL	Photoluminescence
RCA	Radio Corporation America
RMS	Root mean square
RT	Room temperature

Si	Silicon
SiO_2	Silicon oxide
UV-VIS	UV-visible Spectrophotometer
XRD	X-ray diffraction

PEMENDAPAN DAN PENCIRIAN FILEM NIPIS ORGANIK INORGANIK POLIFLUORENA / SERIUM OKSIDA

ABSTRAK

Penyiasatan tentang pendekatan novel dengan menggunakan lapisan oeganik polifluorena (PFs) pada pemalar dielektrik (*k*) tinggi bukan organik serium oksida (CeO_2) yang berpotensi digunakan sebagai lapisan kepasifan bagi peranti logam-oksida-semikonduktor (MOS) berasaskan silikon (Si) telah dijalankan. Pada mulanya, kesan suhu penyepuhlindapan (400, 600, 800 dan 1000 °C) pasca pemendapan telah dijalankan ke atas filem CeO_2 untuk menyiasat perubahan suhu terhadap ciri-ciri struktur, morfologi, optik dan elektrik filem CeO_2. Seterusnya, komposisi PFs yang berbeza telah dilarutkan ke dalam toluena dan dimendapkan atas substrat kaca indium timah oksida untuk melihat kesan komposisi PFs yang berbeza ke atas ciri-ciri optik, struktur, morfologi dan elektrik PFs. Komposisi PFs yang dioptimumkan kemudiannya digunakan sebagai lapisan bertindan atas filem CeO_2 yang disepuhlindap pada suhu berbeza untuk menghasilkan peranti fungsian MOS hibrida organik-bukan organic Al/PFs/CeO_2/Si/Al dimana secara relatifnya agak baharu. Ciri-ciri struktur, morfologi, optik dan elektrik yang ditunjukkan oleh lapisan bertindan PFs pada filem CeO_2 telah dibandingkan dengan sampel yang terdiri daripada filem tunggal CeO_2. Hasil kajian telah mendedahkan bahawa sampel yang mempunyai lapisan bertindan PFs pada filem CeO_2 tidak dapat mengatasi prestasi oleh filem tunggal CeO_2. Namun begitu, lapisan bertindan PFs pada filem CeO_2 yang disediakan memberikan satu kejayaan dalam konteks sebagai lapisan kepasifan *k* tinggi yang berpotensi menggantikan silikon oksida (SiO_2) konvensional *k* rendah disebabkan nilai *k* tinggi yang secukupnya dan ciri-ciri arus-voltan yang setanding dengan CeO_2. Penyiasatan dan penjelasan yang terperinci telah dijalankan, dibentangkan dan dibincangkan dalam tesis ini.

DEPOSITION AND CHARACTERIZATION OF POLYFLUORENE / CERIUM OXIDE ORGANIC-INORGANIC THIN FILMS

ABSTRACT

The investigation of a novel approach by applying an organic polyfluorenes (PFs) layer on inorganic high dielectric constant (*k*) cerium oxide (CeO_2) film for potential use as passivation of silicon (Si)-based metal-oxide-semiconductor (MOS) devices was carried out. Initially, the effects of post-deposition annealing temperatures (400, 600, 800, and 1000 °C) was carried out onto the CeO_2 films in order to investigate the changes of temperatures onto structural, morphological, optical and electrical characteristics of the CeO_2 films. Subsequently, different composition of PFs was dissolved in toluene and deposited onto indium tin oxide glass substrate to examine the effects of varying PFs composition onto the optical, structural, morphological and electrical properties of the PFs. The optimised PFs composition was then applied as an overlayer stacked on CeO_2 films post-deposition annealed at different temperatures to fabricate functional Al/PFs/CeO_2/Si/Al hybrid organic-inorganic Si-based MOS device, which was relatively new. Structural, morphological, optical, and electrical properties demonstrated by the stacking PFs on CeO_2 films were compared with the samples consisting of single CeO_2 films. Outcome of the study revealed that the samples having stacking of PFs on CeO_2 films could not surpass the performance provided by single CeO_2 films. Nonetheless, the stacking of PFs on CeO_2 films provided a breakthrough in the context as a potential high *k* passivation layer to replace the conventional low *k* silicon oxide (SiO_2) due to the adequately higher *k* value and comparable current-voltage characteristics with CeO_2. Detailed investigation and explanation were carried out, presented, and discussed in this thesis.

CHAPTER 1

INTRODUCTION

1.1 Overview

Nowadays, an increasing energy demand in the Electrical and Electronics (E&E) industry, which has been a main driver of industrial development to accelerate economy growth of a nation has become a motivation for investigation of energy efficient semiconductor components and/or electronic devices (Nagy et al., 2018). Proliferate growth of semiconductor industry throughout the decades has enabled the development of electronics devices with enhanced performance at reasonable cost due to continous miniaturization of device form factor. Otherwise, electronic devices were developed rapidly in semiconductor industry by producing a lot of applications such as laptop, mobile phones, tablet computer, digital camera, storage devices, input and output devices as well as e-readers. The improvement of electronic devices could be thus seen by the emergence of these various applications. Researchers have thereafter tried to investigate a better performance of the electronics devices in accordance to the Gordon Moore's law (Bhanu & Thangadurai, 2020). Nonetheless, cost of the devices must be also reasonable due to the emerging miniaturization and the reduction in size of the electronic devices (Charles Jr, 2005).

Silicon (Si) is the main substrate material widely used in the semiconductor industry, especially in the fabrication of electronic devices. For example, Si-based metal-oxide-semiconductor (MOS) devices have emerged and transformed the advancement of semiconductor industry through the discovery of thermally grown silicon dioxide (SiO_2) with an exceptionally good passivating properties to minimize leakage current of the devices (Robertson & Wallace, 2015). However, the

employment of thermally grown SiO_2 has encountered with stumbling block in recent times due to the shrinkage of SiO_2 thickness (El Amrani et al., 2019; Quah & Chong, 2012; Robert & Wallace, 2015), wherein an excessively high leakage current has ensued due to direct tunneling mechanism (Quah et al., 2010; Robert & Wallace, 2015). This can be circumvented as so to enhance the reliability of Si-based MOS devices by using high dielectric constant (*k*) materials that would provide the beneficial outcome of attaining larger capacitance at a similar physical thickness with SiO_2 passivation layer (Chiu & Chang, 2014; Chiu & Lai, 2010; El Amrani et al., 2019; Robertson & Wallace, 2015).

Throughout the decades, the research studies have diverted towards the employment of high-*k* materials, such as HfO_2 (Fu et al., 2011) , ZrO_2 (Kumar et al., 2016), Al_2O_3 (Huang et al., 2009), Y_2O_3-ZrO_2 (Xiao et al., 2008 ; Lim et al., 2015), $LaAlO_3$ (Suzuki, 2012), $HfSiO_4$ (Lok et al., 2017), $ZrSiO_4$ (Lok et al., 2018) and $SrTiO_3$ (Lue et al., 2002) as the alternatives to SiO_2 for Si-based MOS devices. Cerium oxide (CeO_2) known as rare-earth oxide has received substantial attention for different applications, such as photocatalysis, fuel cells (Chen et al., 2013), corrosion inhibitors (Carvalho et al., 2014), gas sensors (Michel et al., 2014) and high-temperature superconductors (Sato et al., 1997). In addition to MOS which could be allied with its fascinating properties of high *k* values (~23-26), large bandgap (~3.0-3.6 eV) (Agrawal et al., 2017; Chiu & Chang, 2014 ; Chiu & Lai, 2010 ; Masalov et al., 2014 ; Quah et al., 2010; Vangelista, 2017), high dielectric breakdown strength (~2.6 MV cm^{-1}), high refractive index (~2.2-2.8), large conduction band offset with respect to Si (~ 1.48 eV), high thermal and chemical stability on Si substrate. Other than that, CeO_2 consists of small mismatch (-0.35%) with respect to Si and has demonstrated low interface-state density (~10^{11} cm^{-2} eV^{-1}) (Chiu & Lai, 2010).

CeO_2 is unique as it possesses two types of charge states (Ce^{3+} and Ce^{4+}), which are the key contributor to the above-mentioned applications because of the release and acceptance of oxygen (Zhou et al., 2019) based on valence change between the Ce^{3+} and Ce^{4+} charge states. The release of oxygen from CeO_2 would form oxygen vacancies, of which the generation and control of the oxygen vacancies would contribute to the enhancement of CeO_2 properties, and this has thus improving oxygen storage capacity of CeO_2 (Campbell et al., 2005). The higher storage oxygen efficiency, the larger amount of oxygen vacancies would be occupied (Wu et al., 2010). In addition, oxygen vacancies are essential in stabilizing grain boundaries in the oxide (Hojo et al., 2010), of which the amount of grain boundaries must be large to develop the diffusion of oxygen. The oxygen vacancies of CeO_2 could be increased by either reducing the pure CeO_2 or by incorporating suitable dopant element (Babu et al., 2009; Frayret et al., 2010) into the CeO_2.

Polyfluorenes (PFs) were the first conjugated polymers demonstrating good solubility and effective emission in the blue spectral region (Fukada et al., 1993 ; Pei & Yang, 1996). The emission could be modified through the insertion of chromophores (phenylene, pyridine, anthracene and thiophene) or by producing copolymers in the backbone of the main chain (Yu et al., 2008 ; Evan et al., 2010 ; PéreS et al., 2017 ; Liu et al., 2000 ; Wang et al., 2009 ; Chen et al., 2009 ; Wang et al., 2002). PFs were widely used in organic light-emitting diodes (OLEDs) (Grice et al., 1998 ; Morteani et al., 2003 ; Voigt et al., 2005 ; Bolink et al., 2007) and transistors (Chua et al., 2005 ; Zaumseil et al., 2006 ; Kajii et al., 2010), surpassing other conjugated polymers, owing to the high luminescence efficiency and greater charge carrier mobility possessed by PFs (Xie et al., 2012 ; Alehdaghi et al., 2015 ; Jokinen et al., 2015 ; Gioto et al., 2016; Cao et al., 2018). In recent times, the use of PFs in

combination with high *k* Al_2O_3 to produce a hybrid organic-inorganic MOS device structure operated at a low voltage with low power dissipation was reported (Hussain et al., 2017). The presence of high *k* oxide would assist in compensating limitation in charge carriers of the polymer and further improving switching speed of the devices. The high *k* CeO_2 could be a promising candidate similarly to Al_2O_3 to serve the purpose yet the exploration of applying a layer of the PFs on the CeO_2 for the development of MOS devices has not been attempted.

1.2 Problem Statement

Thermally grown SiO_2 has been found use as a good passivation layer for Si-based MOS devices, owing to the relatively low lattice mismatch with the Si substrate (Quah et al., 2015 ; Quah et al., 2014 ; Lim et al., 2013 ; Lim et al., 2011). However, the development of MOS devices using SiO_2 as the passivation layer was challenged by shrinkage issue of the SiO_2 thickness when the thickness was decreasing to below 2 nm thick, and thus triggering high leakage current off the devices (Robertson, 2004). Alternatively, the deployment of CeO_2 to replace the SiO_2 has been a choice of material as passivation layer as CeO_2 would provide the positive effect of achieving a larger capacitance at a similar physical thickness with respect to the SiO_2. This would assist in controlling the leakage current issue. According to the previous work reporting about CeO_2 passivation layer, Ce^{4+} oxidation state in CeO_2 would tend to be reduced to Ce^{3+} along with the formation of oxygen vacancies (Kumar et al., 2015 ; Lim et al., 2012) would take place regardless of the type of deposition ambient and temperature. Furthermore, interfacial layer growth could also happen at the CeO_2/Si interface, influencing performance of the MOS devices. The existence of adequately thick SiO_2 or silicate interfacial layer at the interface would decrease dielectric

polarization effect at the CeO_2/Si interface, and thereby minimizing the distortion of molecular bond. With these, phonon scattering was reduced and device breakdown voltage was improved (Wang et al., 2018). Nevertheless, the increase of interfacial layer thickness would pose a greater polarization effect that resulted in current instabilities of the device (Subbarao et al., 2015). In this work, a mixed ambient consisting of nitrogen and oxygen was employed during post-deposition annealing of the CeO_2, which was different from previous work that employed argon, oxygen, and ammonia gas ambient. Rationale of introducing nitrogen was associated with the role of nitrogen as a nitridation agent that could prevent excessive growth of interfacial layer at the interface (Quah et al., 2020).

In addition, the emergence of organic electronic devices using organic polymers, such as poly[(9,9-dioctylfluorenyl-2,7-diyl)-co-(1,4-phenylene)] end capped with dimethylphenyl group (Yang et al., 2005 ; de Azevedo et al., 2017 ; Azadinia et al., 2020) and poly[(9,9-di-n-octylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4,8-diyl)] (Hassan et al., 2019 ; Choi et al., 2017 ; Shih et al., 2019) and poly(9,9-bis(2-ethylhexyl)fluorene) derivatives with different fractions of crosslinkable acrylate groups (Kahle et al., 2017) as well as the reported hybrid organic-inorganic MOS devices have attracted considerable interest in the related field to explore the feasibility of depositing PFs as an organic semiconducting layer on the inorganic CeO_2 passivation layer in order to determine the potential of employing the stacking of PFs on CeO_2 passivation layer as a high *k* passivation layer to replace SiO_2 for MOS devices. The aspects of structural, morphological, optical, and electrical characteristics of the functional Al/PF/CeO_2/Al/Si and Al/CeO_2/Al/Si devices were systematically studied.

1.3 Objectives of the Study

The main purpose of this study is to investigate the feasibility of stacking PFs on metal-organic decomposition (MOD) derived CeO_2 as a new passivation layer for Si-based MOS devices. In order to achieve this purpose, the following objectives are identified:

1. To investigate the effects of post-deposition annealing temperatures (400, 600, 800, and 1000 °C) on MOD derived CeO_2 films deposited on Si substrate.
2. To explore optical, structural, morphological, and electrical properties of PFs spin coated on ITO glass substrate.
3. To study optical, structural, morphological, and electrical properties of stacking PFs on post-deposition annealed CeO_2 films.

1.4 Scope of the Study

In this project, at an initial phase, metal-organic decomposition derived CeO_2 films were spin-coated on n-type Si (111) substrates and the resulting CeO_2/Si samples were subjected to post-deposition annealing before characterization was performed. In this phase, effects of post-deposition annealing temperature on CeO_2 films deposited on Si substrates were studied. In phase 2 of the research, different composition of PFs was prepared and deposited on indium tin oxide (ITO) substrates to determine properties of the PFs before moving to the next phase, which was to deposit the optimised composition of PFs onto CeO_2 film to explore the feasibility of the stacking PFs on CeO_2 to serve as high k passivation layer for Si-based MOS devices. X-Ray Diffraction (XRD), Field-Emission Scanning Electron Microscopy (FESEM), Energy-Dispersive X-ray (EDX) spectroscopy, Atomic Force Microscopy (AFM), Fourier

Transform Infrared (FTIR), UV-Visible (UV-VIS) spectrophotometer, Photoluminescence (PL) spectroscopy, Raman spectroscopy and Filmetric (Optical Reflectometer) to investigate structural, morphological, and optical properties of CeO_2 and PFs/CeO_2 films deposited on Si substrates. Besides, functional MOS devices were fabricated using CeO_2 and PFs/CeO_2 films as the passivation layer while Al electrodes were deposited as the top and bottom contacts to measure capacitance-voltage (C-V) and current-voltage (I-V) characteristics of the MOS devices using semiconductor parameter analyzer (SPA).

1.5 Outline of the Thesis

This thesis is arranged into five chapters. Chapter 1 develops a brief background and problems associated with MOS-based devices, research objectives, as well as the scope of present study. Chapter 2 presents a review about the background studies and theories related to this study in more details. Chapter 3 describes systematic research methodology, raw materials, design of experiments, and characterization techniques used in this work. Chapter 4 discusses findings and results acquired from different characterization techniques of this research. Chapter 5 summarizes main outcomes of this research with some future recommendations.

CHAPTER 2

LITERATURE REVIEW

2.1 Development of Metal-Oxide-Semiconductor (MOS) Based Device

In growth of semiconductor industry, the development of electronics devices is an important thing and has contributed to science and technology. The fabrication of metal-oxide-semiconductor (MOS) based devices by inserting a passivation layer is to protect the semiconductor substrate (Abdullah et al., 2005). The passivation layer acts as an insulating layer to provide passivation, electrical insulation, isolation to other devices (Irokawa et al., 2004), and to prevent the device from environmental hazards (Kikuta et al., 2006). Thus far, MOS based devices have been used to create a wide variety of application devices, such as memory device, sensors, satellites, mobile phone, laptop and fridge. Amongst the electronic devices, MOS based devices emerge as one of the important devices to be used (Schroder, 2006 ; Donald, 2006) as well as investigated for the electrical and physical properties (Sze et al., 2007). According to Gordon Moore, there is an increase in the number of transistors per chip every year (Moore, 1998). To enhance the performance of electronics devices, the cost of the devices must be also reasonable due to emerging miniaturization and the size of electronic devices has been reduced (Charles Jr, 2005).

2.1.1 Gate Oxide as Passivation Layer in MOS Devices

Semiconductor substrate, oxide layer and metal electrode are important components of a MOS structure commonly used in electronic devices, illustrated in Figure 2.1. The characteristics of a MOS device could be accessed by fabricating a MOS capacitor possessing the basic MOS structure. The gate oxide is a thin oxide

layer embedded between the metal electrode and underlying semiconductor substrate in a MOS capacitor. An ideal MOS structure consists of good quality of oxide as a passivation layer with no current flow across it under all static bias conditions (Schroder, 1998).

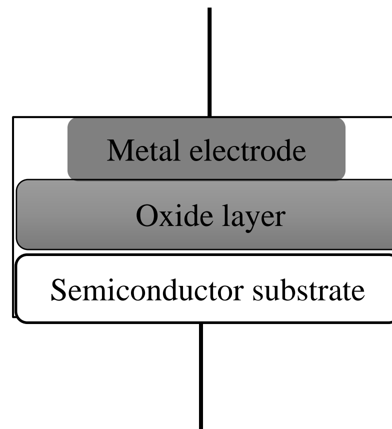

Figure 2.1 Typical MOS structure possessing metal electrode, oxide layer, and semiconductor substrate.

Silicon dioxide (SiO_2) has been used in silicon (Si) based MOS devices. The advantages of SiO_2 include the high quality interface between the Si and SiO_2, thermodynamic and electrical stability of SiO_2 on Si substrate, as well as superior electrical insulation properties. Thermally grown native SiO_2 has been considered as a good passivation layer to reduce leakage current of the MOS devices but the researchers still realized a problem with regards to continuous employment of SiO_2 as the gate oxide for MOS based devices. This could be owing to the further reduction of SiO_2 thickness to the range of 1.0 to 1.5 nm, in which an extremely high leakage current would happen via a direct tunnelling mechanism. This phenomenon if uncontrolled would lead to severe degradation of the MOS device performance.

2.1.2 Influence of Bias on MOS Capacitor

2.1.2(a) Flatband

Zero bias condition in a MOS capacitor occurs when charges are absent in the oxide and/or at the oxide-semiconductor interface. A typical band diagram showing the flat-band condition was shown in Figure 2.2. The application of bias will result in accumulation of charges at the oxide-semiconductor and metal-oxide interfaces. The charges exaggerate performance and stability of the MOS devices (Pierret, 1990 ; Schroder, 1998). There are a number of properties that must be given attention. For instances, the oxide layer must play as a passivation layer that does not allow current flow via the oxide layer under bias conditions (Sze et al., 2007); no accumulation of charges in the oxide layer, at the interface between the oxide and the semiconductor and between the metal gate and the oxide (Sze et al., 2007; Schroder, 2006). The application of a bias to a MOS capacitor ideally consists of three different process conditions or modes, such as accumulation, depletion, and inversion.

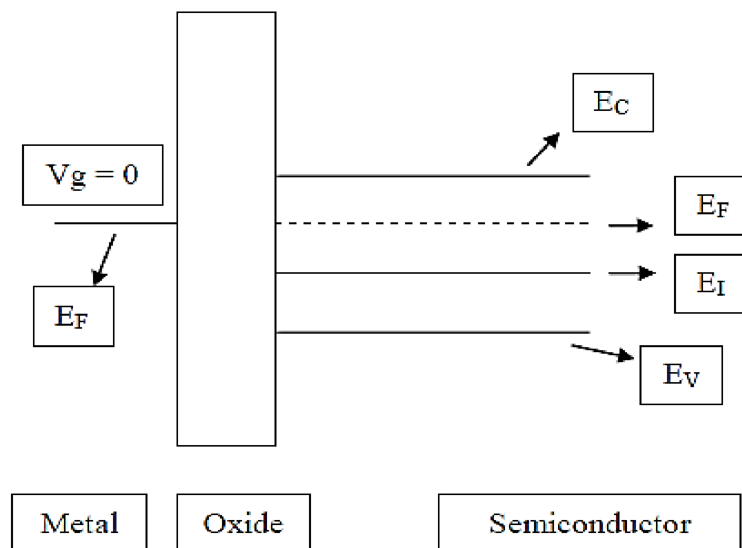

Figure 2.2 Energy band diagram for an ideal n-type MOS capacitor at $V_g = 0$ V (Sze et al., 2007).

2.1.2(b) Accumulation

Accumulation condition takes place when positive bias ($V_G > 0$) is applied. The fermi energy (E_F) in the metal is less than E_F in the semiconductor (Figure 2.3). The oxide and semiconductor consist of positive slope in the energy band. A greater amount of electrons is generated for n-type semiconductor during the positive slope of energy band condition because of the occurrence of majority carrier concentration at the oxide-semiconductor interface as compared to that in the semiconductor. The electrons at the semiconductor-oxide interface must be concerned to ensure balance of charges (Pierret, 1990 ; Schroder, 1998). When a large positive bias is applied to the gate electrode, electrons are accumulated at the semiconductor surface to compensate the excess positive charges accumulated at the gate as a result of application of positive bias ($V_G > 0$). A downward band bending is obtained and accumulation of a thin layer of high electron concentration at the semiconductor or oxide-semiconductor interface happens, which is referred to as the accumulation capacitance of a MOS device, dominated by capacitance of the oxide, C_{Ox}.

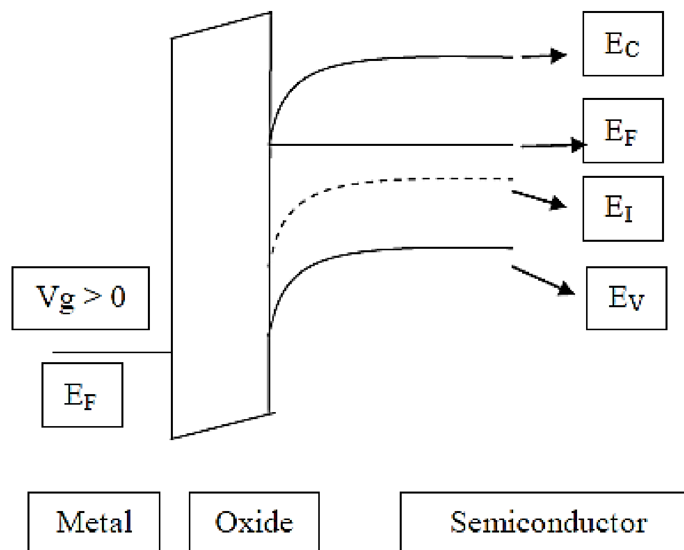

Figure 2.3 Energy band diagram for an ideal n-type MOS capacitor under accumulation condition (Sze et al., 2007).

2.1.2(c) Depletion

Negative slope of the energy band between oxide and semiconductor occurs when small negative bias ($V_G < 0$) is applied. The E_F in the metal is higher than the E_F in the semiconductor (Figure 2.4). Depletion happens when the electrons concentration at the oxide-semiconductor interface are lesser than doping concentration (N_A or N_D) of the semiconductor (Pierret, 1990 ; Schroder, 1998). When the negative bias ($V_G < 0$) is applied to the gate electrode, a depletion zone is formed and the band will bend to upward. The depletion zone is depleted from free carrier concentration.

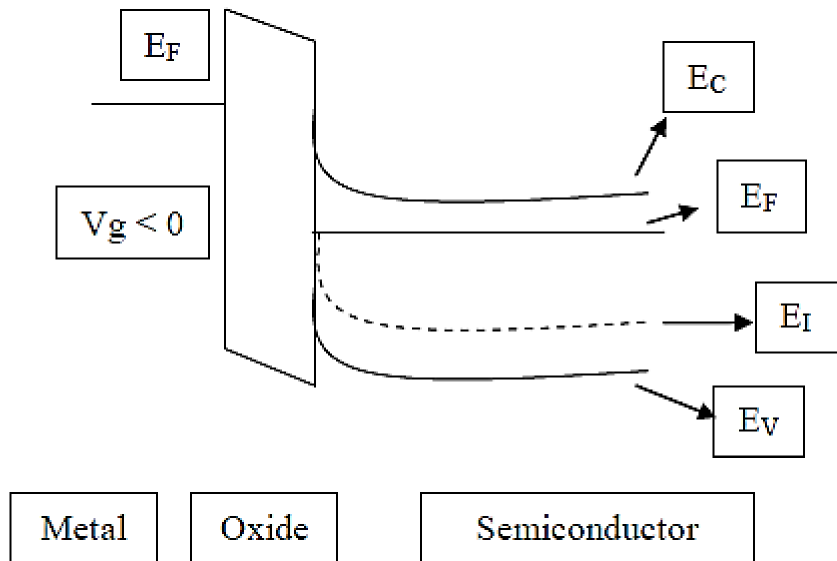

Figure 2.4 Energy band diagram for an ideal n-type MOS capacitor under depletion condition (Sze et al., 2007).

2.1.2(d) Inversion

Negative bias ($V_G < V_T$) happens when the band is further bend up at the semiconductor surface while the concentration of minority carriers (holes) at the surface becomes more than that of the majority carriers (electrons). The switching from n-type to p-type will occur in the surface area and this phenomenon is called

inversion effect (Pierret, 1990 ; Schroder, 1998) (Figure 2.5). When a larger negative bias is applied, E_V (valence band edge) will approach E_F at the semiconductor surface. This would increase the possibility of finding the minority carriers (holes) at the semiconductor surface. The application of even larger negative bias would increase the minority carrier concentration at the surface. The area possessing high concentration of the minority carriers is called inversion layer.

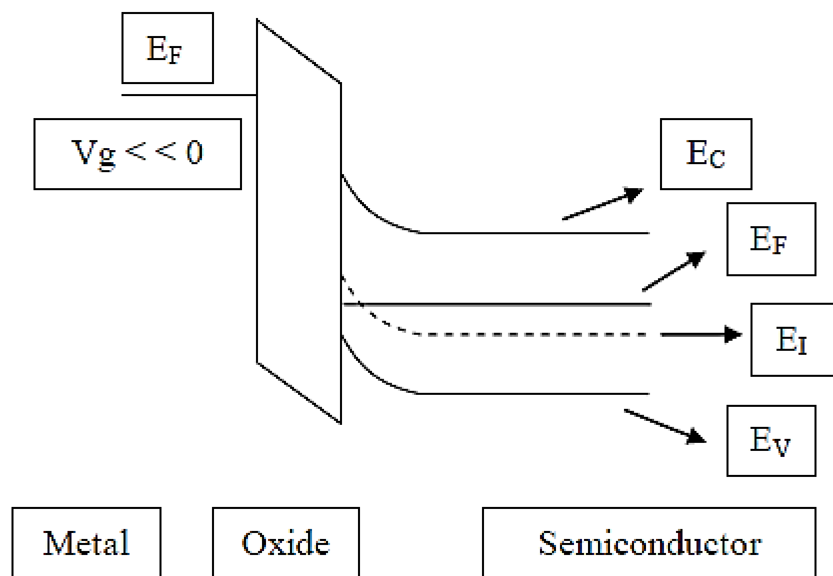

Figure 2.5 Energy band diagram for an ideal n-type MOS capacitor under inversion condition (Sze et al., 2007).

2.1.3 Capacitance Voltage (C-V) Characteristics of MOS Device

C-V characteristics of MOS devices are important to extract information, such as bulk and interface charges, oxide thickness, flatband voltage, and threshold voltage of the MOS devices. Electric charges at the interface would cause the changes in C-V characteristics of MOS devices with respect to E_F. The presence of new interface states close to E_F will be charged and add into the total charges of the MOS device at each point of the voltage ramp. Stretch-out effect will happen whereby the stored electric

charges at the interface broaden the C-V curve. It is independent of the voltage ramp direction (Figure 2.6). During C-V measurement, mobile electric charges in the oxide and deep interface states possessing low emission times and thus may not be able to follow the switching frequency. Hence, hysteresis behaviour is demonstrated by the device (Figure 2.6). The hysteresis will be less intense if a longer period of time is required for emission of the charge carriers (Tsirimpis, 2018).

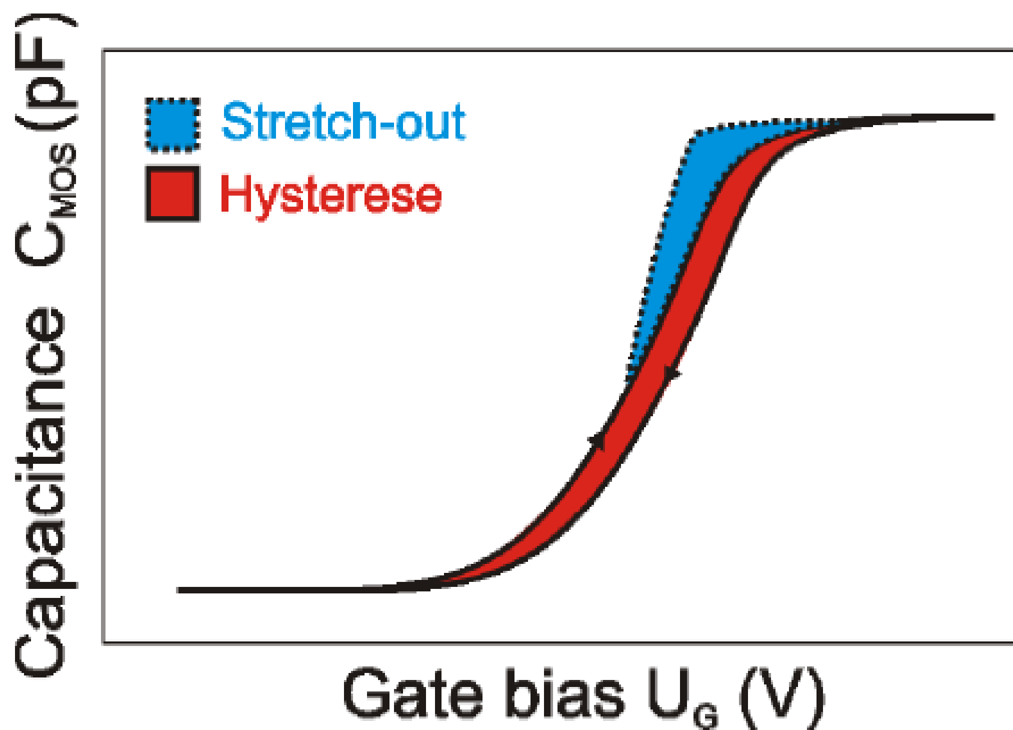

Figure 2.6 Schematic illustration of C-V measurement of n-type MOS device. The arrows on the curve are showing the direction of voltage ramp. The regions showing stretch-out and hysteresis are established (Tsirimpis, 2018).

The conventional method of scaling the gate oxide in MOS devices is attributed to reducing the SiO_2 thickness (d) to rise the oxide capacitance (C_{Ox}), which is defined as in Equation 2.1 (Robertson, 2004):

$$C_{Ox} = k \, \varepsilon_o \, A / d \quad (2.1)$$

where k is the dielectric constant of the oxide and ε_o is the permittivity of free space (8.85×10^{-3} F/m). Investigation has been conducted to down scale the MOS devices, yet the limitation of SiO_2 thickness could not be decreased further from five atoms thick (Bohr et al., 2007) because of relatively high leakage current over the SiO_2 layer that would take place related to quantum mechanical tunneling of electrons when the thickness was at five atoms thick.

2.1.4 Scaling and Breakdown of Gate Oxide in MOS Device

Gate oxide will undergo degradation mechanism during electric field application. Multi incidents occur when the degradation involves gate oxide through the breakdown process. This phenomenon happens if the stored energy inside the MOS-capacitor is incompletely cleared via the breakdown area. Soft breakdown happens for thinner gate oxide while hard breakdown happens commonly for thicker gate oxide. The occurrence of soft breakdown was because of the release of stored energy in the MOS device while hard breakdown occurs when a destructive degradation and breakdown due to the larger damaged area by the thicker gate oxide happens (Durnin, 2002). The presence of trap density in the oxide layer will create a conducting path for soft breakdown to take place. The area will become open source for subsequent electrons to be trapped, leading to device degradation (Quah et al., 2010).

2.2 Challenges and Current Issues Faced by Gate Oxide

According to the Moore's law, the development of MOS-based devices can be studied by scaling down from 100 nm to 1.2 nm of the thickness for SiO_2 on the devices (Bohr et al., 2007). The less gain performance of MOS-based device as the scaling

down from sub-100 nm has also been shown (Frank et al., 2001). The gate oxide leakage is a main issue for degradation of the device performance (Wong et al., 2006). Currently, the researchers have demonstrated that MOS devices consisting of gate length lower than 30 nm should not be a limit (Taur et al., 1998; Wong et al., 1998). This is because of the acceptable device performance and a better concern towards the device feature match with the wafer. The most important feature would be allied with a good gate oxide to serve as the passivation layer and the oxide must be in sufficiently thicker because the electrons during forward bias must be suppressed from tunneling via the gate oxide. In conclusion, the gate oxide material must be physically thick but electrically thin (Bohr et al., 2007; Robertson, 2004).

2.2.1 Selection of High Dielectric Constant (*k*) Oxide

High leakage current is one of main problems accompanying the further down scaling of MOS devices. The restriction can be mitigated by replacing the low *k* SiO_2 with thicker high *k* oxide materials. The employment of high *k* oxide materials as the alternative passivation layers to SiO_2 would provide a larger capacitance at the same physical thickness with respect to the SiO_2 passivation layer. There are instances of ideas to classify potential high *k* oxides. Gate structure, dielectric material properties, and dielectric material fabrication are the few significance features that are considered to enhance the passivation layer (Robertson, 2004; Wilk et al., 2001). According to Robertson, several conditions for new oxide candidates serve as the selection criteria (Robertson, 2004). The high *k* oxide must possess *k* value higher than SiO_2 (k= 3.9). The high *k* candidate was selected based on thermally stability at high processing temperature up to 1000 °C. This situation has been considered and acts as a main issue to control the electrical properties (Wilk et al., 2001). According to Schlom (2008),

the oxide must be also thermodynamically stable with the underlying substrate material to prevent the formation of thick SiO_2 interfacial layer that will form electrical interface with Si. Besides, the oxide must be equipped with good insulator properties to reduce carrier injection and probability of current direct tunneling into its layer.

There have been widely research and investigation towards using high *k* oxide materials to substitute SiO_2 for MOS based devices. Thus far, different high *k* oxides, such as HfO_2 (Xu et al., 2017 ; Jung et al., 2018 ; Guan et al., 2018 ; Seo et al., 2020 ; Kahraman et al., 2020) , ZrO_2 (Singh et al., 2021 ; Gupta et al., 2017 ; Kondaiah et al., 2020 ; Zhu et al., 2017), Al_2O_3 (Uenuma et al., 2018 ; Tan et al., 2022 ; Guan et al., 2018 ; Lee et al., 2018 ; Lee et al., 2019 ; Taoka et al., 2017 ; Kikuta et al., 2017 ; Ren et al., 2018) , Y_2O_3 (Liu et al., 2017 ; Kang et al., 2017 ; Kim et al., 2021 ; Lee et al., 2019), CeO_2 (Park et al., 2019 ; Agrawal et al., 2017 ; Wang et al., 2022 ; Nsar et al., 2022 ; Zhang et al., 2017), Ta_2O_5 (Thapliyal et al., 2021 ; Choi et al., 2019 ; Novkoyski et al., 2017), $LaAlO_3$ (Liu et al., 2020 ; Huang et al., 2022) and $HfSiO_4$ (Lok et al., 2017 ; Kahraman et al., 2020 ; Kahraman et al., 2021 ; Bhanu et al., 2021 ; Carey et al., 2017) have been investigated. Rare earth oxides are emerging candidates for gate oxides based upon the thermodynamic data and stability on Si (Hubbard & Schlom, 1996). Besides, they possess good thermal stability, high *k* (20 to 30), and high conduction band offset with Si. Other than that, rare earth oxide with close lattice match with Si as compared to ZrO_2 and HfO_2 demonstrates thermodynamically stable phases (Leskela et al., 2006). Amongst the investigated rare earth oxides, CeO_2 has received considerable attention for MOS-based devices as well as other appropriate applications, which include photocatalysis, fuel cells (Chen et al., 2013), corrosion inhibitors (Carvalho et al., 2014), gas sensors (Michel et al., 2014), and high-temperature superconductors (Sato et al., 1997) due to its fascinating properties of high

k values (~23-52), large band gap (3.4-3.8 eV), high refractive index (~2.2-2.8), large conduction band offset with respect to Si (~ 1.48 eV), as well as high thermal and chemical stability when in contact with Si substrate.

2.3 Cerium Oxide (CeO_2) – General Properties

Cerium dioxide (CeO_2) is the most stable oxide of cerium, which consists of. Ce^{3+} and Ce^{4+} oxidation states. According to the lanthanide series of Periodic table (Barry, 1992) (Figure 2.7), cerium is a second member and one of the reactive elements. CeO_2 is well known for its oxygen vacancies (V_o) and change of valence states from Ce^{4+} to Ce^{3+} (Pokha et al., 2020) and vice versa, forming CeO_2 and cerium sesquioxide (Ce_2O_3), of which CeO_2 has a higher stability over Ce_2O_3 (Younis et al., 2016).

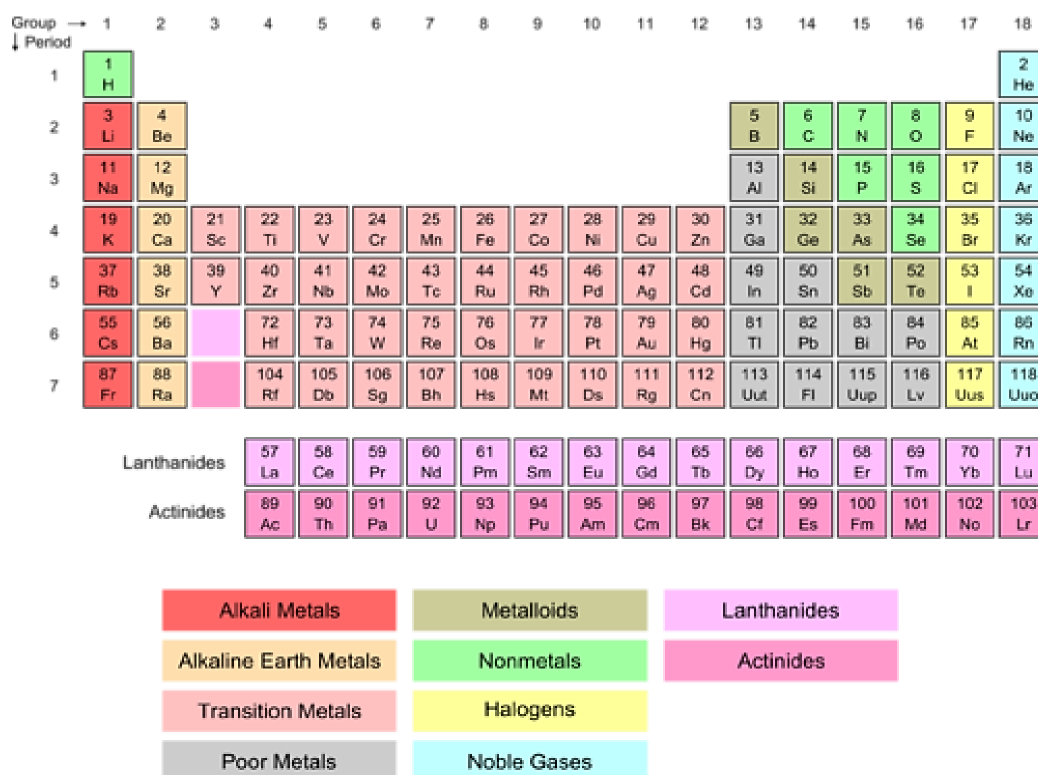

Figure 2.7 Lanthanide series(https://courses.lumenlearning.com/cheminter/chapter/lanthanides-and-actinides/).

Based on the crystal structure, CeO_2 is made up from cubic fluorite structure and is considered as the most important rare-earth oxide (Bumajdad et al., 2009). In the cubic fluorite structure, CeO_2 contains a cubic oxygen sub-lattice with the cerium ions positioned in another cube center. Each Ce cation (purple) is located at the corners and face centers of a cube, and O anions (red) are located at the center of tetrahedral cerium cages, as illustrated in Figure 2.8 (Karl et al., 2018). Basically, some Ce^{3+} ions are existing in the structure of CeO_2 and the number of these ions is related to the number of oxygen vacancies (Campbell et al., 2005).

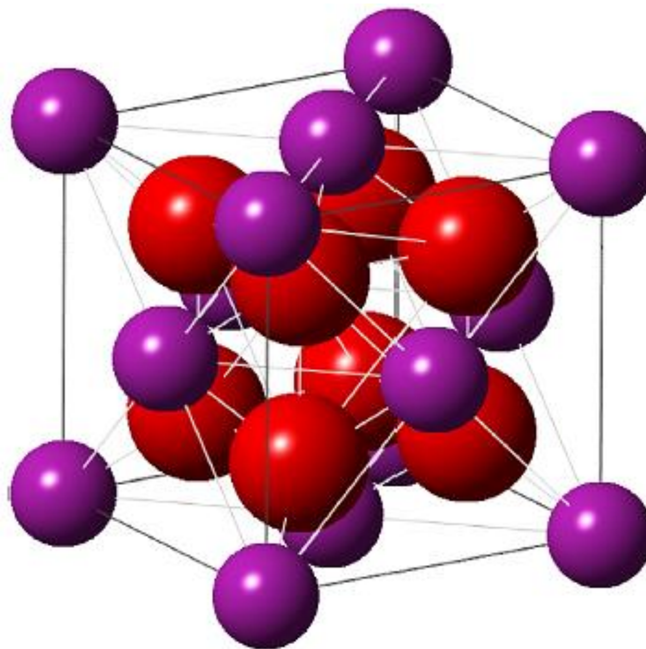

Figure 2.8 Schematic cubic fluorite crystal structure of CeO_2 (Karl et al., 2018).

The aspects, such as substrate material, deposition technique, preparation parameter and chemical composition are important factors to ensure the shape of microstructure and morphological surface of CeO_2 thin film to be observed (Younis, 2016). The reports on CeO_2 have been investigated on different types of substrate materials, such as bare glass (Kumar et al., 2019 ; Kurtaran et al., 2021 ; Yu et al.,

2017 ; Yang et al., 2018 ; Murugan et al., 2017) , indium tin oxide (ITO) glass (Ismail et al., 2019 ; Li et al., 2018 ; Park et al., 2019 ; Yang et al., 2018 ; Sharma et al., 2018 ; Khan et al., 2017), fluorine doped tin oxide (FTO) glass (Ehsan et al., 2018 ; Dey & Roy., 2021 ; Manibalan et al., 2019 ; Mohanty et al., 2021) , and Si (100, 110 or 111 oriented) (Quah et al., 2017 ; Toloshniak et al., 2019 ; Vangelista et al., 2018 ; Tan et al., 2020 ; Popkov et al., 2019 ; Devi et al., 2020). Until now, many deposition techniques have been carried out to investigate CeO_2 films on Si, such as spin coating (Kumar et al., 2019 ; Li et al., 2018 ; Ali et al., 2020 ; Agrawal et al., 2017), thermal evaporation (Li et al., 2017 ; Manibalan et al., 2019 ; Cop et al., 2020 ; Lan et al., 2022), electron beam evaporation (Quah et al., 2017 ; Devi et al., 2020 ; Agrawal et al., 2017 ; Ginting et al., 2020), RF magnetron sputtering (Ismail et al., 2019 ; Stadnichenko et al., 2019 ; Park et al., 2019 ; Yüzüak et al., 2017), and pulsed laser deposition techniques (Wang et al., 2019 ; Liu et al., 2020 ; Zinzuvadiya et al., 2019 ; Kumar et al., 2021).

The properties of CeO_2 is reliant on whether it is a cluster, bulk, nano rods, nano cubes, nano tubes, nano wires (Huang et al., 2014 ; Zhang et al., 2015) or on a soft, dense or amorphous thin film surface (Sun et al., 2013). During characterization, the results can be seen either as amorphous films or polycrystalline films grown with different crystallite sizes from nanometer to micrometer (Younis et al., 2016). The combination between one or more active thin films can make a thin film device, such as thin film solar cells (SCs), transistors, thermoelectric devices, sensors, and actuators. Many types of thin film devices can share same principles of operation or fabrication processes, and thus advances in one device may provide new opportunity for the development of other devices (Eslamian, 2016).

2.3.1 Cerium Oxide (CeO_2) for Device Application

In the advance technology nowadays, CeO_2 has received considerable attention as functional material due to its applications in many diverse fields. CeO_2 is well known for applications, such as catalytic, photocatalysis (Channei et al., 2014), solid oxide fuel cells (Chen et al., 2013), corrosion inhibitors (Carvalho et al., 2014), gas sensors (Michel et al., 2014), and high-temperature superconductors (Sato et al., 1997). In recent times, CeO_2 film has been explored for its capability to function as a high *k* passivation layer for MOS based devices by using Si (Park et al., 2019 ; Quah et al., 2017 ; Shi et al., 2017 ; Tan et al., 2020 ; An et al., 2018 ; Chuah et al., 2011), 4H-SiC (Gao et al., 2021 ; Quah et al., 2017 ; Lim et al., 2012, Lim et al., 2010 ; Lim et al., 2011 ; [c]Quah et al., 2011) and GaN substrate ([a]Quah et al., 2011 ; [b]Quah et al., 2011 ; [c]Quah et al., 2011 ; Quah et al., 2010 ; Nigro et al., 2015).

Catalytic application is one of the signature applications of CeO_2 for oxygen uptake and release (Younis et al., 2016). Carbon monoxide (CO) oxidation has been used in this application whereas CeO_2 can raise oxygen storage capability of the catalysts at low temperature during the process. High surface occupied CeO_2 is ideal because high surface area provides good tendency for the active species to contact the reactants, the catalytic performance will develop. For example, a greater active site was provided by nanotubes for the adsorption of reactants, improving catalytic performance in the CO oxidation process (Pan et al., 2008).

Visible light photocatalytic water splitting is an active research area for renewable energy as well as water and air purification (Younis et al., 2016). Au-supported CeO_2 nanoparticle-based photocatalysts were fabricated (Primo et al., 2011) and it was reported that the photocatalytic of CeO_2 nanoparticles was investigated for

oxygen generation from water. Figure 2.9 illustrates the process and principle of photocatalytic water splitting in semiconductor photocatalysis. The first step is about photon adsorption to generate electron-hole pairs (I). Afterwards, charge separation takes place and migrate to the reaction sites or recombine (II). Finally, reaction between electrons or holes with water molecules happens with the evolution of H_2 or O_2 (III) (Kong et al., 2018).

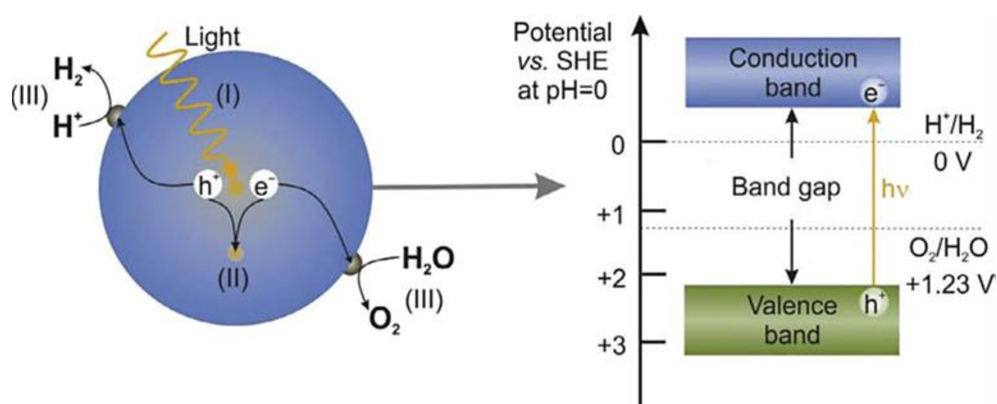

Figure 2.9 Photocatalytic water splitting in semiconductor photocatalysts (Kong et al., 2018).

Solid oxide fuel cells (SOFCs) is an application that has good attention in providing clean and consistent electric power. CeO_2-based ion conductors were used for its resistance to carbon deposition and allowed overpowering supply of dry hydrocarbon fuels to the anode (Gorte et al., 2009). Gorte and Vohs performed a direct electrochemical oxidation of hydrocarbons, such as methane and toluene using SOFCs application with copper and CeO_2 composites. CeO_2-based ceramics showed mixed ionic and electronic conductivity by reducing atmosphere based on reversible redox transition between Ce^{3+} and Ce^{4+}. Furthermore, the catalytic activities also matched to ease in an oxygen-vacancy formation mechanism (Younis et al., 2016).

Corrosion inhibitors is an application for corrosion protection of coatings, cathodic, anodic and selection of materials (Bregman, 1963 ; Eldredge & Warner, 1948 ; Putilova et al., 1966 ; Ranney, 1976). Corrosion inhibition happened when any delaying process occurred, which might be achieved by adding chemical compounds. Corrosion inhibitors involved two phases, which were the transfer of inhibitor molecules over the metal's surface and the interaction of inhibitor's functional groups with the metallic surface. Solubility of inhibitor in corrosive medium, compatibility of inhibitor in corroding system, stability of inhibitor by varying pH and temperature, inhibitor cost, environmental friendliness and corrosion inhibition efficiency are the parameters taken into consideration (Pandian et al., 2016). The electronic structure of CeO_2 was associated with the unique redox property, where cerium established two oxidation states. The transformation of Ce^{4+} into Ce^{3+} caused an oxygen vacancy formation for charge neutrality in CeO_2 lattice, which contributed to better corrosion resistance property (Kumar et al., 2019).

Izu et al. (2002) started to use the mist pyrolysis method to prepare CeO_2 at 700 °C. The work resulted in CeO_2 powder with an average particle size of 200 nm and a random network structure for gas sensor application. After a few years, CeO_2 with larger average particle sizes (200 and 2000 nm) formed at 712 °C was investigated to fabricate a resistive oxygen gas sensor (López-Mena et al., 2017). It was reported that the sensor kinetics were controlled by the diffusion of oxygen vacancies and the particle size affected sensor response time. Xie et al. (2015) reported about the acquisition of CeO_2 nanoparticles (10 - 15 nm) at 500 °C using a solvothermal method and the nanoparticles were used to prepare for humidity sensor device.

In addition, CeO_2 has been used as the buffer materials in high temperature superconductors (HSTC) which could be related with its passivation properties, chemical stability and small lattice mismatch (Thuy et al., 2010). The HSTC requires homogeneous and high-purity metal oxide species for both superconductors and buffer layers prepared using sol–gel chemistry. The second generation HTSC was promising in applications and the deposition of HTSC films on small, single crystal substrates was successful (Falter et al., 2002 ; Dekkers et al., 2003 ; Ye et al., 2005). Sathyamurthy et al. (2004) discovered the use of sol–gel processed epitaxial lanthanum zirconate films as seed and barrier layers to simplify the coated conductor from YBCO/CeO_2/YSZ/Y_2O_3/Ni–W to YBCO/LZO/Ni–W or YBCO/CeO_2/LZO/Ni–W. As the years go by, researchers are focusing on the enhancement of buffer layers and $Y_1Ba_2Cu_3O_x$ (YBCO) super conducting properties (Cloet et al., 2006). Materials, such as CeO_2 (Kim et al., 2009 ; Wesolowski et al., 2006 ; Bhuiyan et al., 2003 ; Coll et al., 2009 ; Solovyov et al., 2009), YSZ (Amezaga et al., 2008), MgO (Izumi et al., 2001), $La_2Zr_2O_7$ (Engel et al., 2008) and $SrTiO_3$ (Chen et al., 2004) are chemically and structurally well-matched with the high temperature superconducting YBCO. In recent studies, CeO_2 films fabricated from cerium acetate precursors and inorganic solvents showed a high texture quality (Bhuiyan et al., 2006).

Apart from the above-mentioned applications, CeO_2 films have been gaining much attraction in the field of MOS applications as a potential high *k* oxide to substitute SiO_2. The chemical and physical properties of CeO_2 as a promising material of gate oxide in MOS devices are listed in Table 2.1.