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A Pragmatic Model to Predict Future Device Aging

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ABSTRACT To predict long term device aging under use bias, models extracted from voltage accelerated tests must be extrapolated into the future. The traditional model uses a power law, to linearly fit the test data on a log-log plot, and then extrapolates aging kinetics. The challenge is that the measured data do not always follow a straight line on the log-log plot, calling the accuracy of such prediction into question. Although there are models that can fit test data well in this case, their prediction capability for future aging is typically not verified. The key advance of this work is the development of a methodology for extracting models that can verifiably predict future aging over a wide (Vg, Vd) bias space, when aging kinetics do not follow a simple power law. This is achieved by experimentally separating aging into four types of traps and modelling each of them by a straight line individually. The applicability of this methodology is verified on 3 different CMOS processes where it can predict aging at least 3 orders of magnitude into the future. The contributions of each type of traps across the (Vg, Vd) space are mapped. It is also shown that good fitting with test data does not warrant good prediction, so that good fitting should not be used as the only criterion for validating a model.

INDEX TERMS —Hot carriers, BTI, Aging, Degradation, Lifetime, Instability, Device-to-device variations, Time dependent variations.

I. INTRODUCTION

Predicting long term device aging under use bias has been a key challenge for CMOS technologies since their earliest usage. Despite early efforts [1]–[29] accurately modelling and predicting future device aging remains an area of significant developmental effort for modern CMOS technologies. Hot Carrier aging (HCA), in particular, still offers many challenges and a reliable model for future aging prediction has yet to be verified across the (Vg, Vd) bias space. A major issue for predicting future degradation is that the kinetics of HCA do not always follow an ideal power law. Fig. 1(a) shows one example of this case reported by early work [21] and Fig. 1(b) gives one example recorded in this work. Some recently proposed models can fit this non-power law behavior well. However, their ability to predict future aging has not been verified [3], [6], [10], [12], [14], [16],[26]–[28]. It will be shown that good fitting with test data does not warrant good prediction. Fig. 1 shows how the deviation from an ideal power law causes uncertainty in the predicted future device aging through extrapolation. There is a clear need for the development of an aging model that can not only fit test data, but also predict future aging across the (Vg, Vd) space.

The key advance of this work are: (i) Develop a measurement technique that separates the aging into four components; (ii) Develop a methodology for modelling aging by fitting the four components separately, rather than fitting the measured data directly; (iii) Experimentally verify the capability of the model extracted by our methodology to predict future aging.

The four separated components are as grown and generated electron and hole traps. It is shown that each type of trap can be modelled by a straight line, enabling reliable extrapolation. The model extracted by this method can predict device aging at least 3 orders of magnitude ahead, thus bridging the gap between a feasible test duration of a few days and the 10-year operating lifetime required.

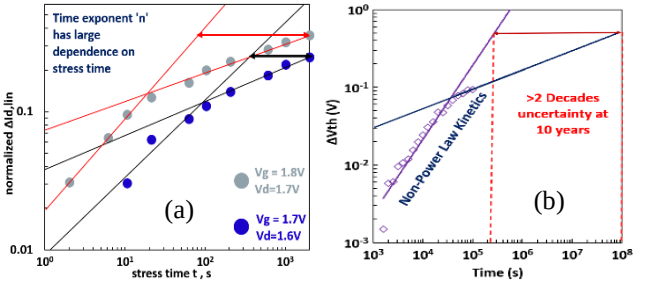

Fig. 1. Examples from early work [21] (a) and this work (b), showing how aging kinetics deviate from power law, making future aging prediction challenging.

II. DEVICES AND EXPERIMENTAL SETUP

The methodology is first used to model aging for FinFETs comparable to a 22 nm node technology with channel width/length of 1/0.028 µm. The applicability of the methodology is also verified on devices fabricated by a commercial 28 nm HKMG (Hi-k Metal Gate) process of 180/27 nm, and a 45 nm Gate-First HKMG process of 1/0.07 µm, to show that it is generally applicable to different types of CMOS technologies.

If not otherwise specified, FinFETs were used and measurements were taken at 125 °C using fast pulse (10µs) Id ~ Vg (IV) supplied by WGFMU units, connected to a Keysight B1500A Semiconductor Analyzer. The threshold voltage, Vth, was extracted from each measured IV by using the maximum transconductance technique [20]. Idlin was extracted at Vg = 0.9 V, Vd = 0.1 V, and Idsat was extracted at Vg = Vd = 0.9 V.

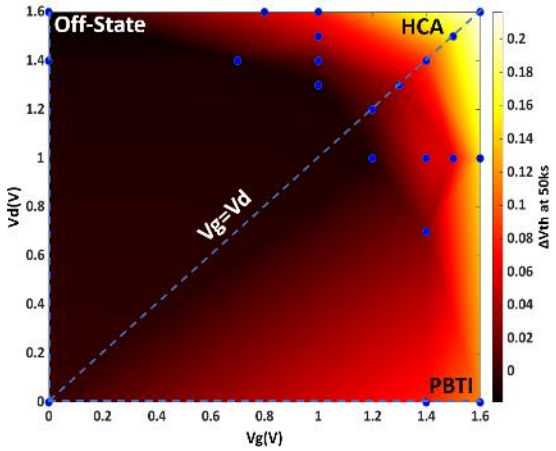

Fig. 2. ΔVth over (Vg, Vd) space after 50 ks stresses. Circles indicate sampled stress voltages.

III. A FRAMEWORK OF DEFECTS AND THE MODEL

A. THE FRAMEWORK

It is well known that both electron and hole traps exist in the gate dielectric of MOSFETs [30]-[34]. In the gate dielectric, electron traps capture electrons and cause an increase in Vth, i.e. the shift ΔVth>0. On the other hand, hole traps capture holes, causing a decrease in Vth, i.e. ΔVth<0. For bias temperature instability (BTI), only one of them is commonly considered: electron traps for PBTI [35] and hole traps for NBTI [36]. For the full (Vg, Vd) space (Fig. 2), however, the gate can be either positive or negative relative to different regions of the substrate. For instance, under 0<Vg<Vd, the relative gate voltage is positive near source, but negative near drain, resulting in different types of traps being active in different regions of the device.

For a model to be applicable to a wide range of (Vg, Vd) bias conditions, the defect framework should include both electron and hole traps in principle as both can contribute to aging under different conditions. Moreover, it has been reported that new electron and hole traps can be generated [30],[31],[35],[36]. This leads to four types of defects: As-grown electron trap (AE), Generated electron traps (GE), As-grown hole traps (AH), and Generated hole (GH). The challenge is how to separate them experimentally, model them individually, and then combine their impacts to give an accurate model of aging kinetics.

The left side of Fig. 3 shows the presence of AH in a fresh device, which can be charged and discharged repeatedly through alternating hole charging and discharging voltage conditions. When the hole charging voltages (Vg=-0.7 V, Vd=+0.7 V) have been applied, the ΔVth is negative relative to the reference level of fresh device (see the symbol 'o'), indicating the presence of trapped holes. When the discharge voltages (Vg=0, Vd=-0.7 V) is applied, the symbol '◊' shows that ΔVth returns to zero, i.e. the fresh device level, indicating that the trapped holes have been discharged back to neutral level. Repeating the hole charging leads to reach the same level of trapped holes, as shown by the second set of symbol 'o' in the left side of Fig. 3. As the trapping level has not increased, it supports that new hole traps are not generated during the hole charging and discharging processes. In another word, the hole trapping observed in the left side of Fig. 3 comes from as-grown hole traps.

After stress (the stress step is not shown in Fig. 3), the same hole charging/discharging conditions were applied. The right side of Fig. 3 shows that the cyclable hole traps have clearly increased, when compared with that on the left side. This increase supports that new hole traps must be generated by the stress.

As will be described in Section III.B, to separate electron traps from hole traps, we need to find a bias condition for efficiently discharging hole traps. After scoping tests designed to find a condition that will fully discharge hole traps, without causing further aging, Vg=0 and Vd=-0.7 V is chosen, where discharging completes in 10 sec, i.e. the symbol '◊' returns to zero as shown in Fig. 3. To test whether drain or gate bias is more effective, discharging was also tested under Vg=+0.7 V, Vd=0 and Fig. 4 shows that discharging does not complete back to the fresh level in 10 sec under this condition, indicating that negative bias applied to the drain is more effective at discharging the AH defects.

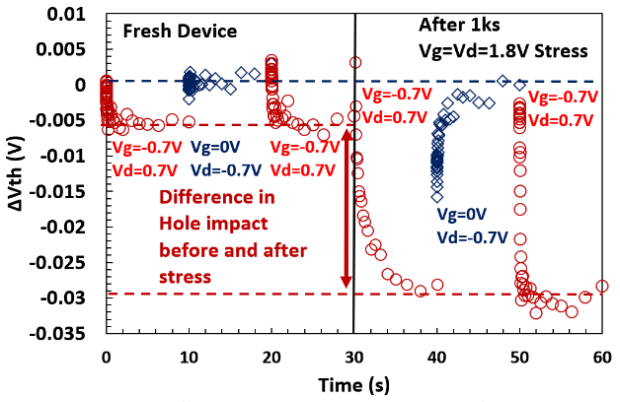

Fig. 3. Demonstration of how the as-grown hole traps in a fresh device can be charged-discharged repeatedly (left) and the increase of hole traps after stressing (right).

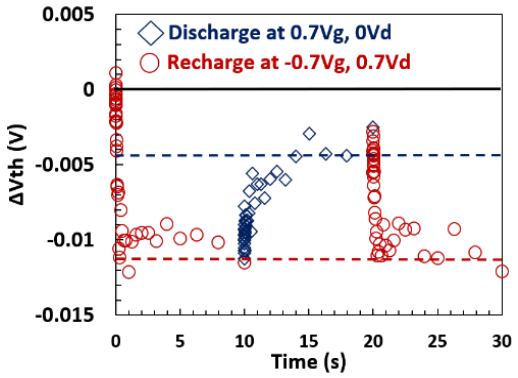

Fig. 4. Charging and discharging of as grown hole traps under Vg=+0.7 V and Vd=0 V.

B. DEFECT SEPARATION AND JUSTIFICATION FOR THE FRAMEWORK

Test starts by measuring Id versus Vg (IV) on a fresh device, which is used to extract the reference Vth for evaluating aging induced shift. Fig. 5 shows a typical result obtained by following the proposed test pattern in Fig. 6. After stress reaches a preset time, it is interrupted and the first 'IV' marked in Fig. 6 is taken. The threshold voltage shift, ΔVth, extracted is given as the symbol '×' in Fig. 5(a). The ΔVth is negative at short time due to hole trapping, before electron trapping eventually turns it to positive during hot carrier aging (HCA). The negative ΔVth at short time cannot be plotted on a logarithmic scale. One can plot only the positive ΔVth at later time on the log-scale, but the symbol '×' in Fig. 5(b) shows that it does not follow a straight line, making extrapolation difficult. This motivates us to develop a technique to separate electron traps from hole traps.

Fig. 6 shows the new proposed methodology where a hole discharging step is inserted after measuring the first IV at each measurement point of the traditional measure-stress-measure procedure. Based on the results in Figs. 3 and 4, hole discharging was carried out under Vgdis=0 V, Vddis=-0.7 V for tdis=10 s. After this hole discharging step, the second IV in Fig. 6 is taken and the ΔVth evaluated from it is shown as the symbol 'o' in Figs. 5(a) and (b). As the trapped holes were neutralized, the symbol 'o' represents the ΔVth caused by electron trapping only.

In many cases (typically stress conditions with Vg > Vd) after discharging trapped holes, the aging kinetics can have a flat region over several orders of magnitude in time before rising and an example is shown in Fig. 7(a). This flat region supports the presence of charged as-grown electron traps (AE). As filling as-grown traps reaches saturation quickly, their contribution to long term aging is taken from their saturation level, S_{AE}, in this work. By subtracting S_{AE} from the total electron trapping, the generated electron traps (GE) can be obtained, as shown in Fig. 7(b). The GE includes both electron traps in the gate dielectric and the generated acceptor-like interface traps. These two are not separated because the model with them combined can predict future aging well, as shown in section IV. As a pragmatic model, we would like to make it as simple as possible.

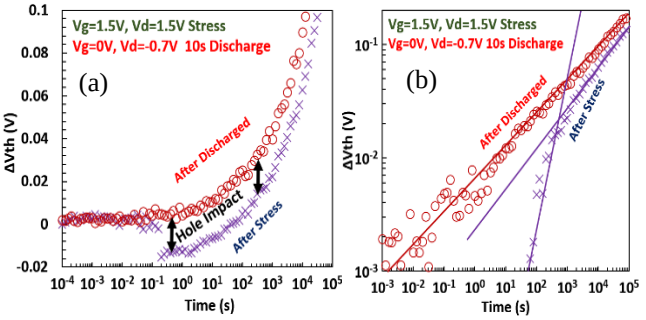

Fig. 5. Measured ΔVth immediately after-stress ('×') and after discharging trapped holes ('○') on a semi-log scale (a) and on a log-log scale (b).

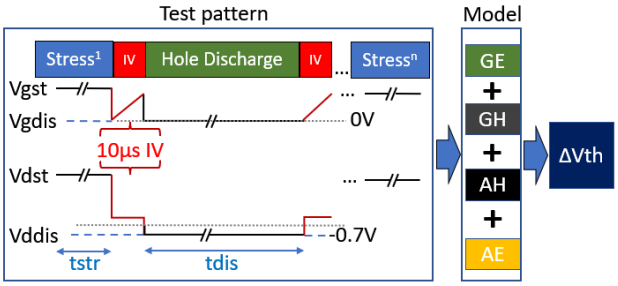

Fig. 6. Test pattern for separating trapped holes from trapped electrons. A hole-discharge step is inserted, and Id-Vg is recorded before and after this step.

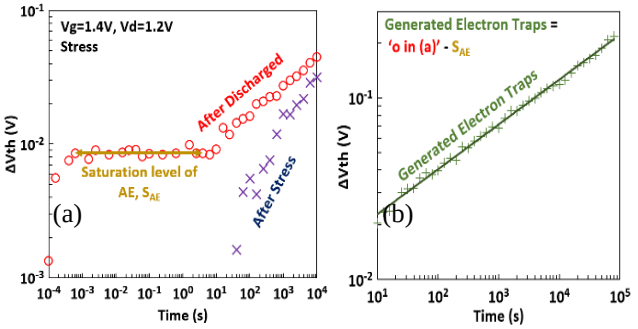

Fig. 7. (a) As grown electron traps are taken from the flat region of the data measured after discharging trapped holes. (b) Kinetics of the generated electron traps after subtracting the flat line in (a).

To accurately model the measured ΔVth, i.e., the symbol '×' in Fig. 5(a), the contribution of hole traps to ΔVth must also be included. The hole trap contribution can be extracted from the difference between '×' and '○' of Fig. 5(a). The hole trap contribution is plotted in Fig. 8(a). Fig. 8(a) shows that AH charging reaches a saturation level, S_{AH}, rapidly, giving a flat region over two orders of magnitude in time. S_{AH} can be used as the AH contribution for predicting future aging. Fig. 8(a) shows that, as stress time increases, |ΔVth(Hole trap)| starts increasing without saturation, which is a signature of generating new hole traps (GH). To extract the kinetics of the GH, S_{AH} is subtracted and Fig. 8(b) shows that GH can be fitted by a power law.

To show the impact of GH on the aging kinetics, Fig. 9 compares ΔVth before and after compensating GH by adding |ΔVth (GH)| to ΔVth (After Stress), as GH causes negative ΔVth. The results show that GH can make a substantial contribution to the reduction of aging slope.

Following this methodology, the aging model is given in the equation (1), which combines the four components: Generated electron traps (GE), Generated hole traps (GH), As-grown electron traps (AE), and As-grown hole traps (AH):

$$\Delta Vth = C_{GE}t^{n_{GE}} + C_{GH}t^{n_{GH}} + S_{AE} + S_{AH} \quad (1)$$

where C_{GE} and C_{GH} are voltage dependent constants.

IV. PREDICTIVE MODELLING

A. FUTURE AGING PREDICTION

This section demonstrates that the extracted models can predict future aging. The data from short stress (≤100 sec) is used to extract the parameters in equation (1). The model is then used to predict at least 3 orders of magnitude into the future. The accuracy of the prediction is verified by comparing the prediction with the measured data between ~100 sec and ~100 ksec. 100ks is used as the maximum value here because of the practical limitation for continuous use of shared test facilities in the laboratory.

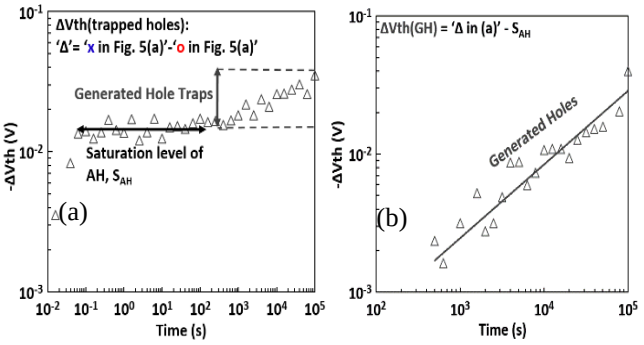

Fig. 8. Contribution of trapped holes evaluated from the differences in ΔVth measured pre- and post-discharging trapped holes (difference between '×' and '○' of Fig. 5(a)). (b) The contribution of generated hole traps obtained by subtracting the flat line (AH) in (a).

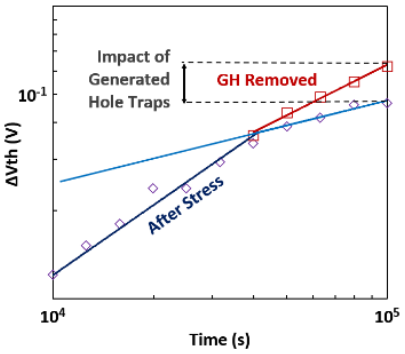

Fig. 9 When GH is compensated by '□'='◊'+|ΔVth(GH)|, the 'soft saturation' is reduced.

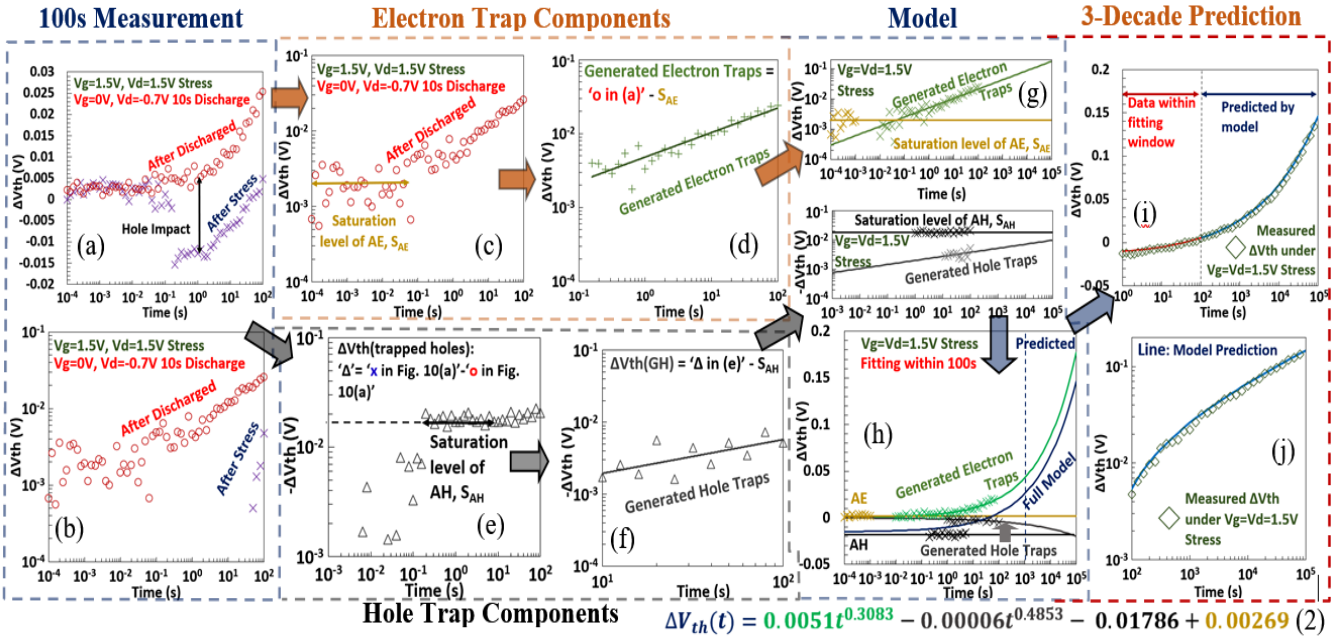

Fig. 10. Procedure for trap separation, model extraction, and prediction. The ΔVth measured pre- (×) and post-hole discharge (○) in the initial 100 s of stress under Vd=Vg=1.5 V is used to create the model. (a) semi-log scale and (b) Log-Log scale. (c) The saturation level of as-grown electron trap is evaluated from the flat region (The line). (d) Generated electron traps are obtained by subtracting the flat line in (c). The line in (d) is fitted with power law. (e) Total contribution of trapped holes created by '×'-'○' in (a). The flat line is the saturation level of as-grown hole traps. (f) Generated hole traps are obtained by subtracting the flat line in (e). The line in (f) is fitted with power law. (g) Extrapolating the four 4 straight lines obtained from (c)-(f). (h) The 'Full model' is evaluated from equation (1) by combining the four lines in (g). (i) A comparison of the prediction by the 'Full model' (line) with test data (symbols) between 10^2 and 10^5 sec. The red line before 10^2 s is the fitted model. (j) A replot of the prediction region in Log-Log scale. RMSE of prediction = 3.05mV

For stresses under different Vg/Vd ratios, the time exponents are different. It is important to verify the applicability of the methodology to predict future aging across the (Vg, Vd) space. This is carried out by showing the predictions for the three corners of Fig. 2: HCA (Vg=Vd), PBTI (Vg>0V, Vd=0V), and off-state stress (OSS, Vg=0V, Vd>0V).

HCA under Vg=Vd: This is the most severe aging condition in the (Vg, Vd) stress space (Fig. 2). Fig. 10 shows the full process of extracting the model from 100s of measured data. Fig. 10(a)&(b) show the measured data in 100s pre- (symbol '×') and post-hole discharging (symbol '○') in linear and logarithmic scale, respectively. The saturation level of as-grown electron traps, S_{AE}, is extracted from the flat region of ΔVth after hole-discharging, as shown by the line in Fig. 10(c). After subtracting S_{AE}, the contribution of generated electron traps (GE) is given in Fig. 10(d), which is fitted with a power law to extract C_{GE} and n_{GE} in equation (1).

Fig. 10(e) shows the contribution of hole traps, which was obtained from the difference between the pre- and post-hole discharge data in Fig. 10(a). Similar to AE, the flat region in Fig. 10(e) gives the saturation level of as-grown hole traps, S_{AH}. After subtracting S_{AH}, Fig. 10(f) gives the contribution of generated hole traps, which is then fitted with a power law to extract C_{GH} and n_{GH} in equation (1). The time range for extracting exponent is one decade or longer in this work. The ΔVth (GH) here is relatively small and a start time of 10 sec was chosen in Fig. 10(f) when ΔVth(GH) is ~ 2 mV.

Fig. 10(g) shows the extracted four straight lines and they were extrapolated ahead by 3 orders of magnitude to 10^5 sec. Fig. 10(h) shows how the 4 lines in linear scale are combined through equation (1) to give the full ΔVth. The predicted full ΔVth between 100 and 10^5 sec is then compared with the measured data (symbols) in linear (Fig. 10(i)) and log-scale (Fig. 10(j)), respectively. Good agreement has been achieved, even when the measured ΔVth in Fig. 10(j) does not follow a simple power law. We believe that the success of this prediction originates from the transformation of the non-linear measured ΔVth into four straight lines by our methodology and extrapolating straight lines is more reliable than extrapolating non-linear curve.

We do not have test data to verify that our model can predict aging beyond 10^5 sec. If we use all measured data up to 10^5 sec to extract the model, the GE in Fig. 10(d) and GH in Fig. 10(f) can be fitted over a larger time range, so that the two power laws in equation (1) can be fitted at least equally accurately. This leads to the expectation that the model extracted from data within 10^5 sec should also be able to predict at least 3 decades ahead, reaching ~10 years, if the aging is within the designed level for device lifetime definition, i.e. ΔVth ≤0.1V where aging saturation effects are insignificant.

To demonstrate that separating into four components is essential for achieving the good prediction, we also fitted equation (1) directly with the test data in the fitting window of Fig. 10(i). Based on the least squared error, the parameters in equation (1) were simultaneously extracted. Fig. 11 shows that good agreement was again obtained with the test data in the fitting window. When the fitted model was used to predict future aging, however, the agreement was poor.

To measure the agreement quantitatively, we use the Root-Mean-Square-Error (RMSE) between test data and the computed results by the model. Table 1 shows that, in the fitting region, direct simultaneous fitting can in fact give a slightly smaller RMSE than the separated fitting. In the prediction region, however, the simultaneously fitted parameters clearly cannot be used to make prediction. These results demonstrate that good fitting does not warrant good prediction and should not be used as the criterion for validating a model. Instead, good prediction of future aging should be used to validate a model.

In sharp contrast with the poor prediction by the model when parameters were extracted through direct simultaneous fitting, Table 1 shows that the RMSE of the prediction three orders of magnitude ahead is only a few milli-volts, when the model parameters were extracted separately from the four components. This endorses our methodology for extracting the aging model.

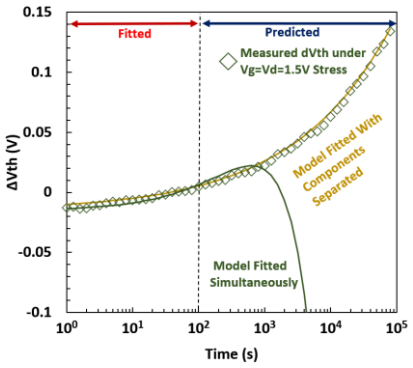

Fig. 11. A comparison between accuracy of model in fitting and prediction regions when fitting was carried out by (1) separating into four components (as outlined in Fig.10) and (2) fitting all model parameters in equation (1) simultaneously with measured data based on least squares errors.

Table 1. A comparison in RMSE between model when fitted by (1) separating into four components and (2) fitting all model parameters in equation (1) simultaneously with measured data based on least squares errors. The RMSE is in unit of Volt.

Fitting Type	RMSE (ΔVth)	
	Fitting Region (<100s)	Prediction region (100s-100ks)
Separated Model	0.00196	0.00305
Simultaneous Fit	0.00177	1.75719

PBTI (Vg>0V, Vd=0V): is another key condition of device aging. Fig. 12(a) shows how the initial 63 s of data are used to create the model. Under a PBTI stress the gate is positive over the whole channel as there is no drain voltage. This makes the hole trap contribution below the measurable level, so that AH and GH are set at 0 in the aging model. Figs. 12(b), 12(c) and 12(d) show the proposed methodology can be used to give good predictions, even when some components are insignificant.

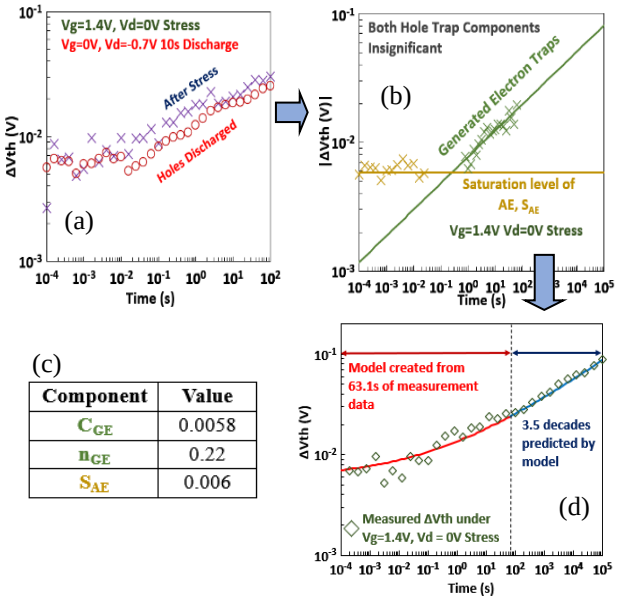

Fig. 12. (a) Initial 63.1s of PBTI test data were used to create aging model. (b) Extraction and extrapolation of AE and GE components from initial data. Both AH and GH are insignificant under PBTI conditions. (c) Values for significant model parameters. (d) Comparison between the model prediction and test data. RMSE of prediction = 4.81 mV.

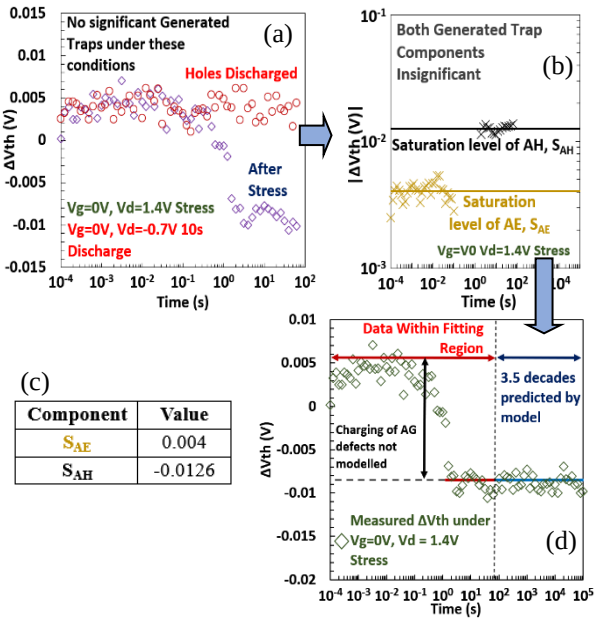

Fig. 13. (a) Initial 63.1s of OSS test data were used to create the model. (b) The extraction and extrapolation of traps under OSS. (c) Values for significant model parameters. (d) Comparison between the model prediction and test data. RMSE of prediction = 0.87 mV.

Off-state stress (OSS): Vg=0V, Vd>0V is the third corner of (Vg, Vd) stress space in Fig. 2. Under OSS, the electrical field within the device is strongly in favor of charging hole traps. Fig. 13 shows an example of modelling under an OSS condition. Fig. 13(a) shows the initial 63s of data used to extract the S_{AE} and S_{AH} shown Fig. 13(b). Their values are given in Fig. 13(c). In this case, ΔVth is dominated by AH, which saturates well within 10 seconds and changes little during the following 100 ksec, as shown in Fig. 13(d). Good prediction is verified in Fig. 13(d). At very high stress Vd, beyond the typical range of relevance for logic applications, OSS can generate hole traps. It is not shown here as it is outside the scope of this work.

B. PREDICTION OF AGING AT LOWER STRESS VOLTAGES

As device aging under use bias is typically too small to establish aging kinetics in a practical time, voltage-accelerated tests have been commonly used. To predict aging under use bias, it is essential to extrapolate the model extracted from stress voltage to the real use level, such as 0.9 V. Although the main thrust of this work is to propose a method for extracting the aging model that can predict future aging, we assess the accuracy of the voltage extrapolation under HCA with Vg=Vd here, since this is the most severe aging conditions in the (Vg, Vd) space of Fig. 2.

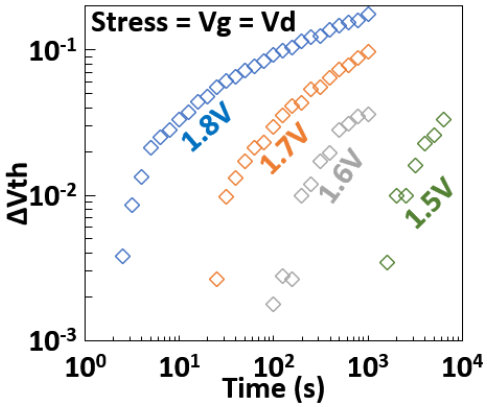

Fig. 14. The measured ΔVth pre-hole discharge under different stress biases on a commercial grade 28nm process.

The stress voltages were varied between 1.5 V and 1.8 V and the extracted model will be used to predict the aging under 1.2 V. 1.2 V is selected because it is the lowest stress condition where aging kinetics can be reliably established within a reasonable time window (100 ksec).

When the measured ΔVth is plotted on the log-log scale, Fig. 14 shows that the aging kinetics under different stress voltages are not in parallel, making voltage prediction highly challenging. By following the methodology outlined in Section III, Fig. 15(a) shows that the separated GE under different voltages can be modelled well with a common time exponent of n_{GE} =0.33. The voltage dependent parameter, C_{GE}, in equation (1) can be modelled by the formula given in Fig. 15(b).

With n_{GE} =0.33 and C_{GE} at 1.2 V extrapolated using the formula in Fig. 15(b), the GE at 1.2 V can be predicted. Fig. 16(a) shows that the prediction (the line) agrees well with the test data with an RMSE of 1.46 mV.

The devices used here were made by a 28 nm commercial process as they have the smallest device-to-device variation. Under Vg=Vd, the measured GH is insignificant and was set to zero. The S_{AE} and S_{AH} in equation (1) under 1.2 V were measured. After combining the contributions from GE, S_{AE}

and S_{AH}, Fig. 16(b) shows that the predicted ΔVth by equation (1) (the line) agrees well with the measured data. The model extracted from 1.5-1.8 V can be used to predict aging at 0.3 V below the lowest stress voltage used to create the model, therefore.

If we extract the model from the data obtained under 1.2-1.8 V, there will be more data points over a wide voltage range in Fig. 15(b) for extracting the parameters of C_{GE}. It is reasonable to assume that extracted model parameters will not be less accurate and can be used again to predict 0.3 V below the lowest stress voltage used to create the model, i.e. 1.2 V. This will reach the use bias of 0.9 V. Although we do not have the aging data at 0.9 V to verify it, we expect that the model has the potential to predict aging under use bias.

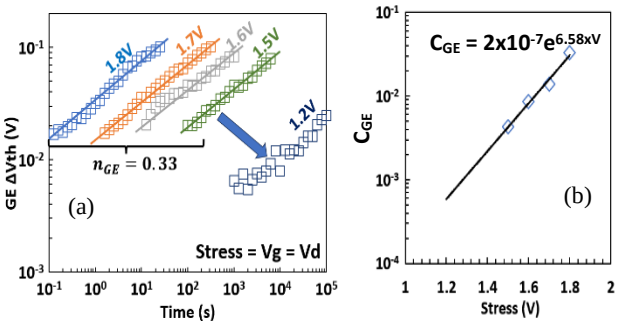

Fig. 15. (a) The generated electron traps. The data from 1.5 - 1.8 V are fitted with power law to extract the n_{GE} and C_{GE} in equation (1). (b) The C_{GE} extracted under different voltages can be fitted by the given equation.

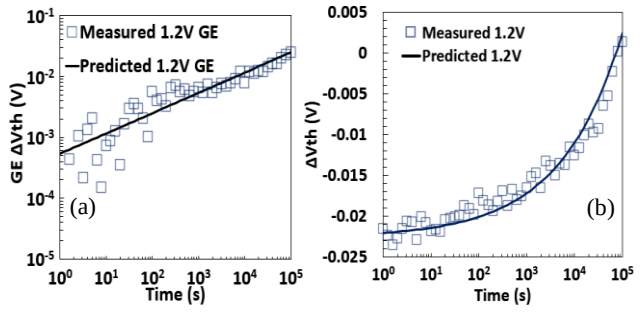

Fig. 16. (a) A comparison of the GE predicted by the model extracted from the data between 1.5 and 1.8 V in Fig. 16 with the measured one at 1.2 V. (b) The predicted ΔVth after-stress is compared to the measured value at 1.2 V after including the AE and AH. RMSE of predicted GE = 1.46 mV

C. STRESS MAP OF THE FOUR TYPES OF DEFECTS

To develop a richer picture of how each type of defect responds to different stress conditions, 20 different conditions were applied to the FINFETs and the impact of each type of defect after 50 ksec was used to create the stress maps in Fig. 17. Blue lines on the stress maps are a rough guide to distinguish weak from strong impact regions.

Fig. 17(a) shows that as-grown hole traps (AH) have a heavy dependence on Vd. For a given high Vd, AH increases with Vg. As a result, the polarity of oxide field is not the only factor controlling AH and HC also plays a role in the charging of holes.

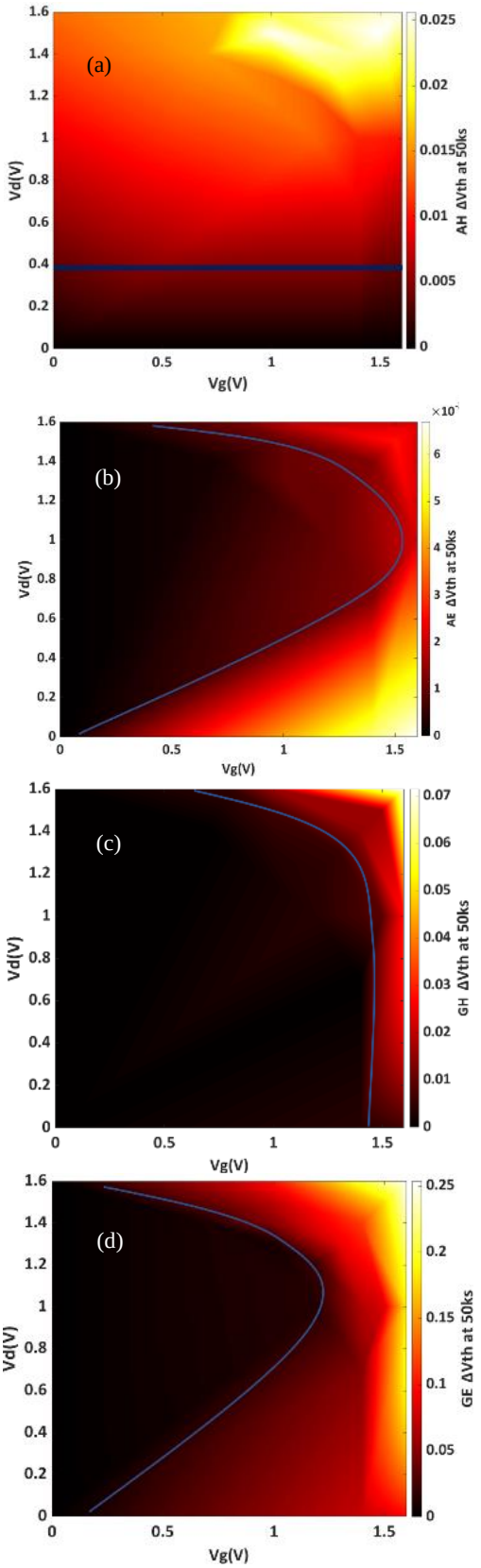

Fig. 17. 2D stress map of the ΔVth contribution from (a) the as-grown hole traps, (b) the as grown electron traps, (c) the generated hole traps, (d) the generated electron traps at 50ks of stress.

Fig. 17(b) shows that as-grown electron traps (AE) depend strongly on Vg and reach its maximum under PBTI. For a given high Vg, AE reduces initially with increasing Vd and then increases. The initial reduction is caused by lowering oxide field near drain, while the later rise can be caused by enhanced HC generation under high Vd.

Fig. 17(c) shows that the generated hole traps (GH) are strongest when both Vg and Vd are high and expand furthest into low Vg under Vg<Vd. Both HC and oxide field polarity play a role here. Finally, Fig. 17(d) shows the generated electron traps (GE) is strongest under Vg=Vd. GE reduces rapidly with lowering Vg, but the reduction is slower with lowering Vd. Both HC and oxide field contribute strongly to GE.

D. SATURATION OF GENERATED INTERFACE STATES

Under heavy stress conditions, Fig. 18(a) shows that there is soft saturation in aging kinetics, even after the hole traps were neutralized. This soft saturation cannot be explained by the generated hole traps, therefore. Early works [9], [14], [26], [27], [37], [38] have also reported soft saturation under such heavy stresses. One explanation for this behaviour is a saturation of generated interface states. As there is a limited number of interface state precursors [39], [40], the generated interface states will saturate when their precursors run out, leading to the saturation in Fig. 18(a). The change in the subthreshold swing (ΔSS) was extracted, as generated interface states always increase ΔSS. Fig. 18(b) shows how the ΔSS also saturates, supporting the limitation in the generated interface states at high stress level.

As the saturation of generated interface states has not been considered in the proposed model, the model will not be able to predict this saturation. However, Fig. 18(a) shows that this saturation only occurs under heavy stress conditions and when the ΔVth is well beyond the level typically used to define lifetime of CMOS devices (<0.1 V). As the goal of the proposed model is to accurately model HCA within device lifetime, it is only important that ΔVth<0.1 V can still be predicted under such heavy stress conditions. Fig. 19 shows that this is the case.

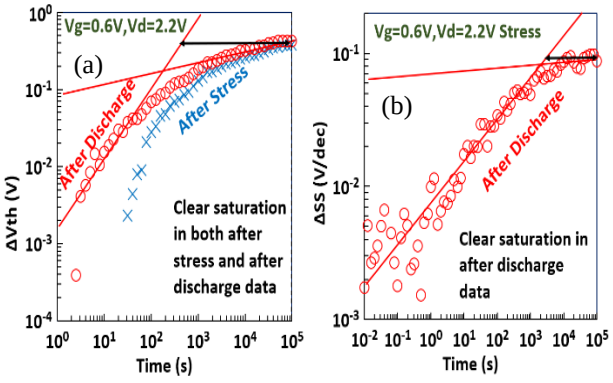

Fig. 18. (a) Example of aging kinetics where there is soft saturation in both the before and after hole discharge data. (b) Corresponding ΔSS for ΔVth data shown in (a) also shows soft saturation.

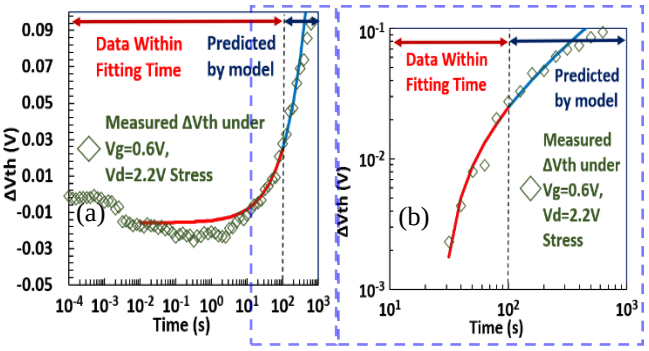

Fig. 19. Aging prediction within ΔVth<0.1 V for a device with clear interface state induced saturation. (a) Semi-log scale (b) log-log scale. RMSE of prediction = 16.2 mV.

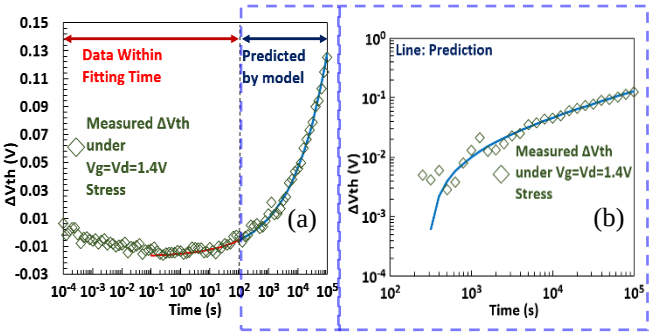

Fig. 20. Example of aging prediction in terms of ΔVth on a commercial grade 28nm HKMG process in (a) semi-log scale (b) log-log scale. Test data are symbols and prediction is the line after 100 s. RMSE of prediction = 3.11 mV.

V. ALTERNATE PROCESSES, PROBES, AND TEMPERATURES

To fully demonstrate the applicability of the proposed methodology, this section gives examples of how the same technique can be used to make accurate aging predictions on different processes and probes. Firstly, examples of the predictive capability are shown on a commercial 28 nm HKMG process in Fig. 20. Secondly, Fig. 21 shows that the methodology is also applicable to the 45 nm process. The predictive capability of the methodology is generic, even though the extracted model parameters are process-specific.

In addition to ΔVth, the methodology is also applicable to other aging probes, i.e. ΔIdlin/Idlin and ΔIdsat/Idsat. Fig. 22(a) and 22(b) show the good predictive capability of the model in terms of ΔIdlin/Idlin and ΔIdsat/Idsat, respectively where the RMSE is within 1%.

The tests up to here were carried out at 125 °C, but devices can operate at other temperatures. To demonstrate that the methodology is equally applicable at other temperatures, an example is given in Fig. 23, showing that prediction is also good at room temperature.

Finally, aging not only shifts threshold voltage and driving current, but also causes the stress induced leakage current (SILC) through the gate dielectric. It has been reported that the defects responsible for SILC act as 'step-stones' for electrons passing through the dielectric and will not result in steady trapping [41]. Further work is needed to

find if the methodology proposed here can be adapted to model the SILC.

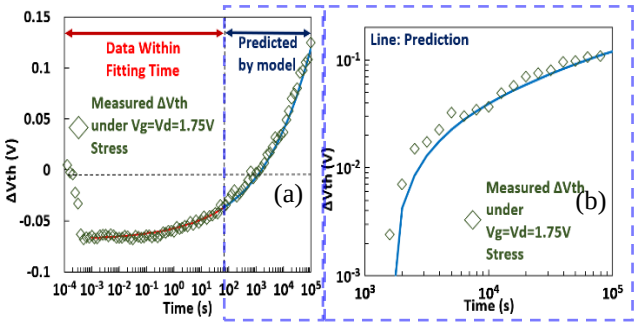

Fig. 21. Example of aging prediction in terms of ΔVth on samples fabricated by a 45nm process in (a) semi-log scale (b) log-log scale. Test data are symbols and prediction is the line after 100 s. RMSE of prediction = 5.97mV

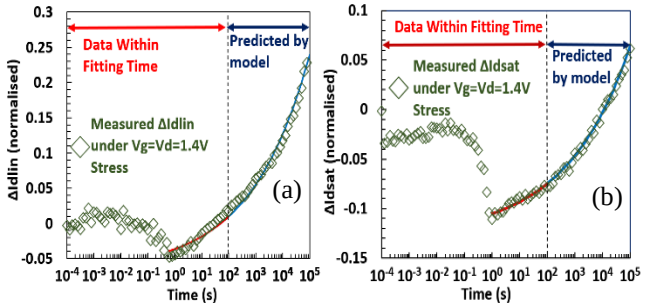

Fig. 22. Example of aging prediction on the 22nm FinFET process in terms of ΔIdlin/Idlin (a) and ΔIdsat/Idsat (b). RMSE of prediction is (a) 0.7% (b) 0.4%.

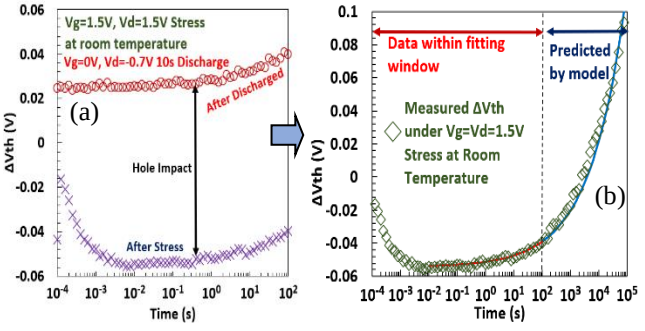

Fig. 23. Applicability of the proposed methodology for predicting future ageing at room temperature. (a) The data within 100 sec were used to extract the model parameter. (b) The extracted model (red line before 100 s) predicts ageing 3 orders of magnitude ahead well. RMSE of prediction = 9.89mV

VI. CONCLUSIONS

A framework has been proposed for defects induced by aging over the (Vg,Vd) bias space. The four types of traps are as-grown electron traps, as-grown hole traps, generated electron traps, and generated hole traps. A measurement methodology has been developed to experimentally separate them. This methodology enables transforming the non-linear aging kinetics for the measured ΔVth into linear ones for the four types of traps. As extrapolating straight lines is more reliable than extrapolating non-linear curves, we demonstrate that the straight lines extracted from short time (<100 sec) tests can be combined to predict future aging at least three decades ahead. The methodology is applicable to different combinations of stress Vg and Vd, different aging probes, temperatures, and different CMOS technologies.

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