A 54.8-nW, 256-bit Codeword Temperature-Robust Wake-Up Receiver minimizing False Wake-Ups for Ultra-Low-Power IoT Systems

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***Abstract*—This paper presents a Wake-Up Receiver for ultra-low-power IoT systems requiring robustness against temperature variations and false wake-ups. The former is accomplished by implementing a dedicated biasing block to ensure a roughly constant Analog Front-End input impedance and matching network gain over temperature. The latter is achieved thanks to a data-startable baseband logic featuring a Gated Oscillator Clock and Data Recovery circuit, which allows the reception of 256-bit codewords. A prototype was fabricated in an STMicroelectronics 90-nm CMOS technology; it receives 1-kbps OOK-modulated packets with a 433-MHz carrier frequency and consumes 54.8 nW with a 0.6-V supply voltage. The measured sensitivity at room temperature is -49.5 dBm with a 10^{-3} Missed Detection Ratio and its variation is 6 dB over a -40 °C to + 95 °C temperature range. Zero false wake-ups were detected transmitting random packets for 60 hours, resulting in an overall reduction in the IoT node energy consumption.**

Keywords— Clock and Data Recovery, IoT, Temperature Compensation, Ultra-Low-Power, Wake-Up Receiver

I. Introduction

Internet of Things (IoT) systems empower the synergy between environment, smart devices, and end users. They typically operate via wireless links and require ultra-low-power consumption to maximize battery lifetime [1] and operation in harsh environments (e.g. industrial applications) in which temperature may significantly fluctuate. The integration in the IoT node of a Wake-Up Receiver (WuRX) is beneficial as it allows the synchronization between the gateway and the end node with both minimum latency and energy by waking-up the power-hungry main transceiver of the node only when a communication request is detected. The energy consumption per day E_n of an IoT node with WuRX is:

$$E_n = E_{WU} + I_n^{OFF} V_{dd}^n \left(86400 - T_n^{ON}(N_{WU}^T + N_{WU}^F)\right) + I_n^{ON} V_{dd}^n \left(T_n^{ON}(N_{WU}^T + N_{WU}^F)\right), \quad (1)$$

E_{WU} is the energy due to the WuRX, V_{dd}^n is the node supply voltage, I_n^{OFF} is the node current in sleep state and I_n^{ON} is the average current in T_n^{ON} which is the time interval, in seconds, after the wake-up, wherein the node operates in the active state. N_{WU}^T and N_{WU}^F are the number of true and false wake-ups. False wake-ups must therefore be minimized to extend the node lifetime.

A WuRX is generally composed of an Analog Front-End (AFE) and a BaseBand Logic (BBL). Unlike conventional radios utilizing power hungry mixer-based architectures, the AFE of a nanowatt WuRX employs an Envelope Detector (ED), either active or passive, to down-convert to baseband the OOK-modulated RF signal coming from the antenna. The ED is generally preceded by an external Matching Network (MN) and is followed by a baseband amplifier and a comparator to output a digital stream, which is then sampled and processed by the BBL. To wake-up the IoT node, the BBL compares the received packet with the codeword, i.e. the node address, stored in the WuRX itself and produces the Wake-Up (WU) interrupt in case the correlation has a positive outcome. Passive EDs are typically composed of a Dickson Charge Pump and due to their zero-current biasing, which ensures no flicker noise, allow better sensitivity performances than active solutions [2][3][4][5]. Reference [3] propose a single-ended passive ED operating at 434 MHz wherein receiver sensitivity is optimized by appropriately setting the channel resistance of the MOSFET-based diodes. It requires an external source to bias the diode gates, which, however, needs to be calibrated if the operating temperature changes. In addition, since the ED input resistance is determined by that of the diodes, the MN gain will also vary with temperature. References [4][5] propose temperature-robust passive EDs operating at 9 GHz and 4.9 GHz, respectively. Unlike [3], [4][5] implement differential passive EDs to improve conversion gain compared to single-ended passive architectures and do not require any MN adjustments for different operating temperatures thanks to the high input resistance of the EDs. State-of-the-art WuRXs use BBLs featuring oversampling techniques to overcome the phase misalignment between received data and clock [3][4][5]. However, these architectures are not suitable for receiving hundred-bit codewords (up to 63 bits in [5]), which is a key feature to reduce the occurrence of false wake-ups. Furthermore, increasing the codeword length allows the neutralization of brute-force cryptographic attacks [6] and the reception of encrypted packets (e.g. One-Time Pad, AES) through the WuRX itself, which is a fundamental specification in IoT applications requiring the processing of sensitive data.

This paper presents a nanowatt WuRX for medium range applications (up to 100 m). It features a variation of the ED in [3] to ensure temperature robustness of sensitivity by implementing a biasing block for the ED diodes which guarantees a constant input resistance and thus no need for any MN adjustments over temperature. An additional key feature is the BBL, which implements a Gated Oscillator Clock and Data Recovery (GO-CDR) circuit to correctly receive up to 256-bit codewords. Section II presents the system architecture and the circuit implementation, Section III describes the measurement results of the fabricated prototype and finally, Section IV concludes the paper.

II. WuRX Architecture and Circuit Implementation

The WuRX architecture is shown in Fig. 1; the always-on AFE is clockless, while the BBL requires a clock to sample the incoming data. This allows the WuRX to operate in two phases [7][8]: during phase 1, both the GO-CDR and the Biasing Circuit (BC) in the BBL are off, whereas the AFE is

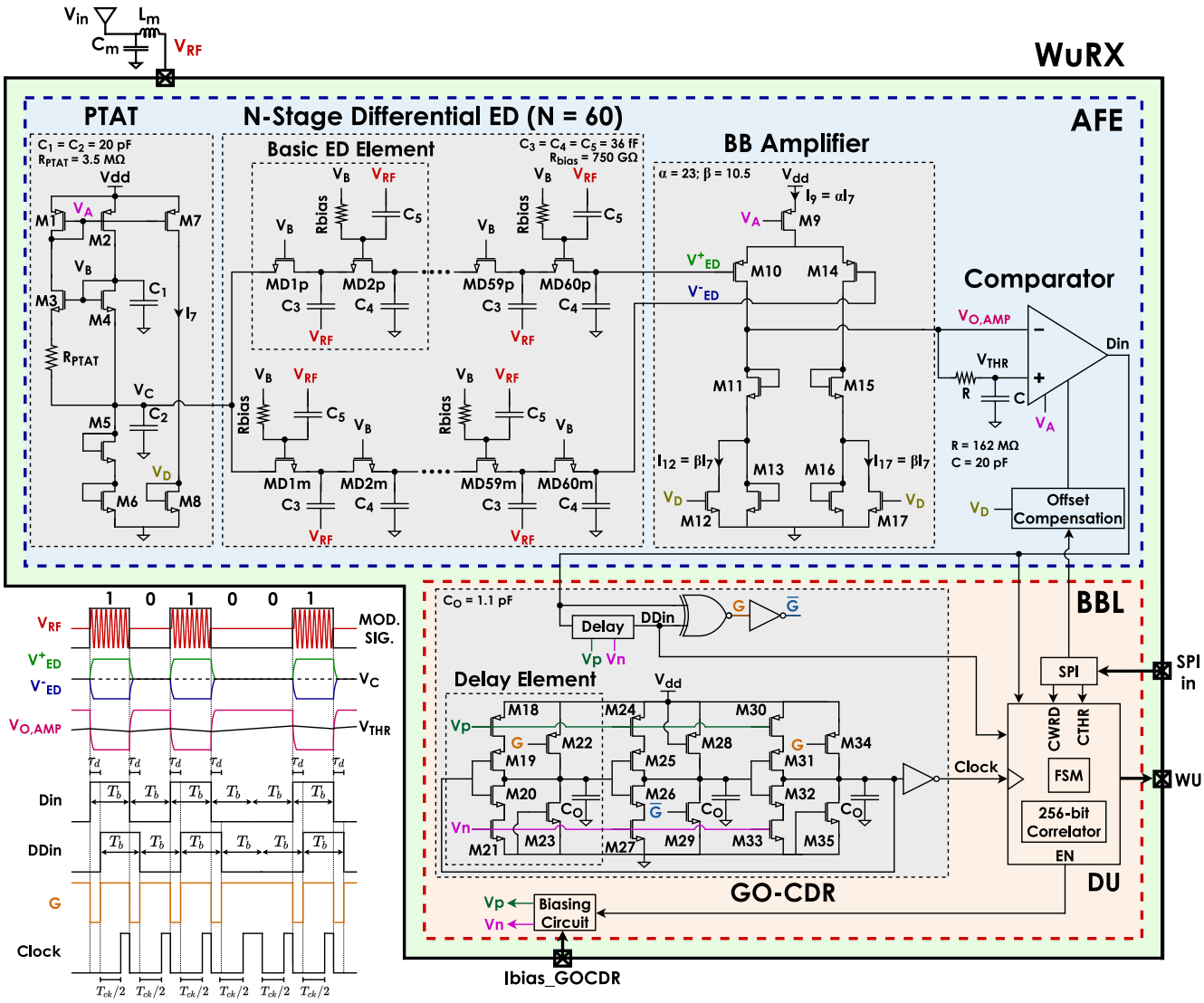


Fig. 1. Block diagram of the proposed WuRX. Inset: time-domain response to an OOK-modulated input signal. Clock drawn in the ideal case, i.e. $T_{ck} = T_b$.

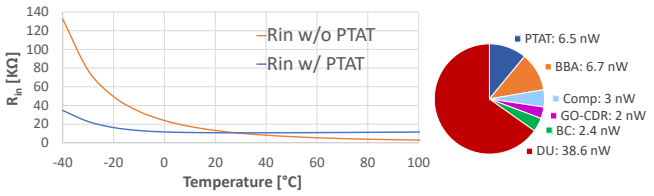
active; phase 2 starts upon recognition of the first 0-to-1 transition of the AFE output signal (*Din*). After that, the BC and the GO-CDR are triggered on and the incoming bitstream is sampled and compared with the stored codeword.

A. Analog Front-End

The AFE is composed of an external L-shaped LC MN (L_m, C_m) providing both impedance transformation and passive gain to the RF signal coming from the antenna (V_{in}). It is followed by a differential ED, which demodulates the OOK-modulated RF input, $V_{RF} = v_m \cos(\omega t)$, to baseband and generates a differential signal (V^+_{ED} - V^-_{ED}) for the BaseBand Amplifier (BBA). The input signal for the BBL (D_{in}) is generated by a standard two-stage clockless comparator that compares the BBA output ($V_{O,AMP}$) with its RC-filtered version (V_{THR}). The Offset Compensation (OC) block generates binary weighted currents to compensate for the overall offset at the comparator input and is programmed at system start-up through the Serial Peripheral Interface (SPI) in the BBL. Bias voltages/currents for the ED, the BBA, the comparator and the OC block are generated by the PTAT reference shown in Fig. 1, which also includes capacitors C_1 and C_2 for filtering purposes. All MOSFETs are biased in the subthreshold region to minimize power consumption. The ED, based on the architecture presented in [3], is composed of a cascade of N MOSFET-based diode stages, as shown in Fig. 1. Its basic element, biased at zero current, features two diode stages in series in two different configurations and outputs a signal generated by the second-order non-linearities of MOSFETs in the subthreshold region. Since the diode stages appear in parallel to V_{RF} but in series to the output baseband signal, the ED output is $Nv_m^2/4nV_t$, i.e. each stage adds its contribution to the preceding ones. ED sensitivity, namely the minimum detectable input power, is [3]:

$$P_{SEN} = \sqrt{\frac{SNR_{req} \cdot NF \cdot (4nV_T)^2 \cdot k_B \cdot T \cdot R_{in} \cdot f_s}{A_v^4 \cdot R_S^2}}, \qquad (2)$$

where SNR_{req} and NF are the minimum required Signal-to-Noise Ratio (SNR) and the noise factor of the BBA, respectively; n is the non-ideality coefficient of MOSFETs in the subthreshold region, V_T the thermal voltage, k_B Boltzmann's constant, T the absolute temperature, R_{in} the ED input resistance, f_s the bitrate, R_S the resistance of the antenna and A_v the matching network gain, which is dependent on both R_{in} and ED input capacitance (C_{in}). Ideally, assuming C_3, C_4, C_5 >> C_{GS} and these capacitances to have negligible parasitics, $C_{in} = NC_{GS} + C_{PAD}$ and $R_{in} = r_{DS}/N$, where C_{GS} is the gate-to-source capacitance of diodes, C_{PAD} is the RF input pad capacitance and r_{DS} is the channel resistance of the diodes. The number of stages N, the r_{DS} of the diodes and the values of C_3,



(a) (b)

Fig. 2. (a) Simulated R_{in} over temperature with $N = 60$. Orange: ED biased with constant V_B (w/o PTAT); blue: ED biased with V_B supplied by the proposed PTAT block (w/ PTAT). (b) WuRX simulated power consumption.

C_4 and C_5 are design parameters. N determines the ED propagation delay and should thus be designed according to the maximum bitrate; furthermore, maximizing N allows to minimize NF. Once N has been designed, to optimize P_{SEN} an optimum R_{in}, thus an optimum r_{DS}, must be properly set by adjusting the gate-to-source voltage (V_{GS}) of the diodes [3]. According to (2), ED sensitivity is heavily dependent on temperature: $P_{SEN} \propto \sqrt{T^3 R_{in}/A_v^4}$, where R_{in} is an exponential function of T through the r_{DS} of the diodes in the subthreshold region; furthermore, also A_v depends on T through R_{in}. Since R_{in} is determined by r_{DS}, we designed the PTAT reference to make R_{in} roughly temperature independent by providing the V_{GS} of the diodes in an appropriate way. This yields both a reduced sensitivity dependence on T and an A_v roughly temperature independent, thus requiring no MN adjustments in case of temperature changes. Assuming the standard subthreshold current model for the diodes:

$$I = I_S \frac{W}{L} e^{\frac{V_{GS}}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}}\right), \tag{3}$$

with $I_S = I_{S0} \exp(-V_{TH}/nV_T)$ and considering that PTAT provides the ED diodes with the same voltage V_{GS} as M4, i.e. $V_{GS} = V_{GS,M4} = V_B - V_C$, the r_{DS} of the diodes is:

$$r_{DS} = \frac{V_T}{I_S \frac{W}{L}} e^{\frac{-V_{GS}}{nV_T}} = \frac{V_T}{I_S \frac{W}{L}} e^{\frac{-V_{GS,M4}}{nV_T}} \cong \frac{V_T}{I_{M4}} \frac{\left(\frac{W}{L}\right)_{M4}}{\frac{W}{L}}, \tag{4}$$

where I_{M4} is the DC current of M4.

The current through M_3 and M_4 is:

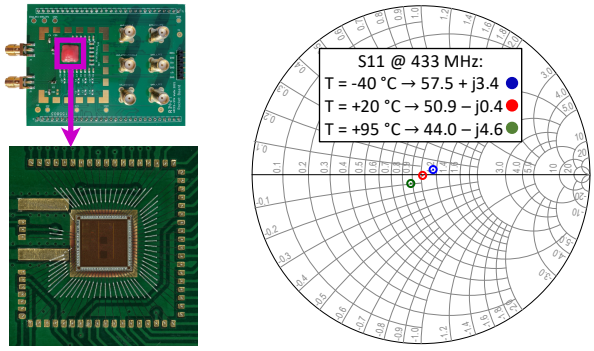
$$I_{M3} = I_{M4} = \frac{nV_T}{R_{PTAT}} ln \frac{(W/L)_{M3}}{(W/L)_{M4}}, \tag{5}$$

therefore, by combining (4) and (5), it is possible to prove that:

$$R_{in} = \frac{r_{DS}}{N} \cong \frac{1}{N} \frac{(W/L)_{M4}}{(W/L)} \frac{R_{PTAT}}{n \cdot ln \frac{(W/L)_{M3}}{(W/L)_{M4}}}. \tag{6}$$

Therefore, PTAT makes R_{in} roughly temperature independent, as shown in Fig. 2.a. Moreover, in order to avoid the thermal and flicker noise introduced by the PTAT, a differential approach was chosen, using two diode ladders as shown in Fig. 1. PTAT noise is seen as common mode at the input of the BBA and thus gets cancelled out.

The BBA is a differential temperature robust inverting amplifier with single ended output ($V_{O,AMP}$), which amplifies the ED output signal (V^+_{ED} - V^-_{ED}) to make $V_{O,AMP}$ detectable by the comparator. As shown in Fig. 1, the BBA is biased with $I_9 = \alpha I_7$ where I_7 (the current of PTAT MOSFET M7) is also mirrored through M12 and M17, i.e. $I_{12} = I_{17} = \beta I_7$, to steer some current from load MOSFETs M13 and M16. The ratio α/β optimizes the BBA gain-linearity trade-off. Diode-connected MOSFETs M11 and M15 are implemented to improve $V_{O,AMP}$ linearity, thus making the BBA suitable even for input signal amplitudes well above system sensitivity.



(a) (b)

Fig. 3. (a) Board and Chip-on-Board photograph, (b) Matching Network S11 measurements at 433 MHz with T = -40 °C, +20 °C and +95 °C.

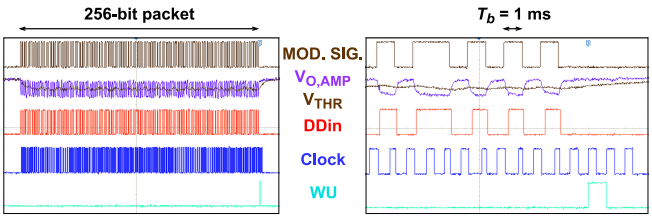
B. BaseBand Logic

As shown in Fig. 1, the BBL is composed of a GO-CDR circuit [7] to generate the clock signal, *Clock*, phase and frequency aligned with the delayed replica, *DDin*, of the AFE output data (*Din*). It is composed of a three-stage current-starved ring oscillator and a delay circuit to generate *DDin*, which is implemented using the same Delay Element as the oscillator and provides a delay equal to τ_d. It also includes an EXNOR-based edge detector, which compares *Din* with *DDin*, thus resulting in a pulse of the gate signal (G) at each *Din* transition. The Biasing Circuit supplies voltages V_p and V_n to GO-CDR when $EN = 1$. All MOSFETs in the BBL but those in the Digital Unit (DU) and the logic gates in the GO-CDR are biased in the subthreshold region.

With reference to Fig. 1, when $G = 1$, the GO is in free-running mode with frequency $f_{CK} = 1/T_{CK}$, while with $G = 0$, it is blocked to *Clock* = 0. When G switches from 0 to 1, the GO generates the positive edge of *Clock* after $T_{CK}/2$, thus allowing it to clear any phase errors accumulated up to that time and thus implying no limit in the maximum codeword length. The Correlator in the DU compares *DDin* with the node address (*CWRD*) and generates the WU interrupt when the result of the comparison between the received packet and *CWRD* is higher than the correlator threshold (*CTHR*); both *CWRD* and *CTHR* are programmed through the SPI. The FSM in the DU pushes the WuRX into Phase 2, by setting *EN* from 0 to 1, when the first 0-to-1 transition in the comparator output (*Din*) has been detected.

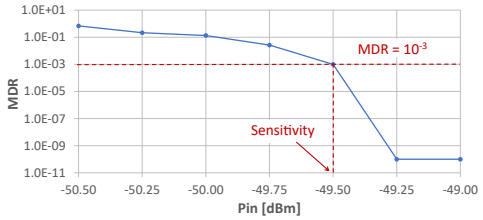
C. Circuit Implementation

The proposed WuRX was designed using an STMicroelectronics 90-nm CMOS technology with $V_{dd} = 0.6$ V. It receives 1-kbps OOK-modulated and Manchester encoded 256-bit packets at 433-MHz carrier frequency. The values of the passive components in the AFE and the BBL are indicated in Fig. 1 as well as the current ratios of the BBA (α, β); R_{bias} was implemented through a diode-connected MOSFET with zero V_{GS}. The ED is composed of $N = 60$ diode stages targeting $SNR_{req} = 4.1$ and $NF = 3$ dB; the BBA gain is 16 dB. *Ibias_GOCDR* was set to 2 nA to generate a 1-kHz free-running clock and $\tau_d = 70\ \mu s$. The simulated WuRX power consumption is reported in Fig. 2.b. During Phase 1 and Phase 2, the WuRX consumes 54.8 nW and 59.2 nW, respectively, in which the contribution of the DU is 70.5% and 65%. Assuming 1% activity of reception (Phase 1 + 1% Phase 2), the WuRX average power consumption is 54.84 nW. Fig. 3.a shows the chip-on-board photograph.

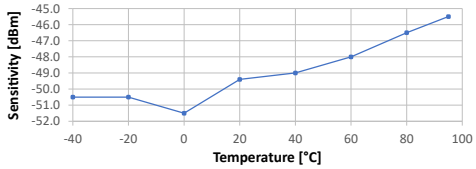


(a) (b)

Fig. 4. WuRX measured transient waveforms. (a) 256-bit packet, (b) zoom at the end of the 256-bit packet.



(a)



(b)

Fig. 5. (a) MDR vs. input signal power at room temperature, (b) WuRX measured sensitivity through MDR = 10^{-3} over temperature.

III. Measurement Results

Figure 3.b shows the results of Matching Network S11 measurements performed over temperature. As predicted by simulations in Fig. 2.a, the slight variation confirms that there is no significant change in the ED input resistance from -40 °C to +95 °C. Figure 4 shows the measured transient waveforms in response to a 256-bit packet matching the codeword with -49.5-dBm input power. WuRX performances were characterized through Missed Detection Rate (MDR) measurements by transmitting packets matching the codeword and counting the number of missed WU pulses. The WuRX sensitivity corresponds to the minimum input power which guarantees MDR = 10^{-3} [2][3][4][5][7]. MDR measurements were performed with 256-bit packets with the correlator threshold set to 248/256, i.e. 3% error tolerance on the codeword. Figure 5.a shows -49.5 dBm sensitivity at room temperature. Figure 5.b shows that sensitivity variation, evaluated through MDR measurements, is 6 dB in the -40 °C to +95 °C temperature range. The WuRX False Alarm Rate (FAR), which is the number of false WUs per hour, was evaluated transmitting 256-bit random packets with a 15-ms delay. Measurements lasting 60 hours revealed zero overall false WUs. The maximum input power is -17 dBm and the Signal-to-Interferer Ratio is -11 dB for CW interferers from ±100 kHz to ±100 MHz with respect to the carrier frequency.

Table I compares performances with prior art WuRX featuring passive EDs. The main features of the proposed WuRX are the ED compensation in a wider temperature range (-40 °C to +95 °C) and the reception capability of longer codewords (256 bits). The -49.5-dBm sensitivity is due to the choice of a higher bitrate (1 kbps), lower error tolerance and longer codeword; the latter allows us to minimize the FAR and demonstrates a state-of-the-art node energy per day E_n, as in (1), of 1.32 J assuming typical values for I_n^{OFF}, I_n^{ON} and T_n^{ON} [1].

TABLE I. Comparison Table Including Energy Consumption of an IoT Node with WuRX

	This work	[3]	[4]	[5]
	Sub-GHz & kbps	*Sub-GHz & sub-kbps*	*GHz & sub-kbps*	
Technology [nm]	90	65-LP	65/180	65
Freq. [MHz]	433	434.4	9000	4900
Supply [V]	0.6	0.4	0.4	1.2 – 1.5
Power [nW]	54.84 [a]	0.42	22.3	184
Sensitivity @ 25°C [dBm]	-49.5	-79.1	-69.5	-78.3
Bitrate [kbps]	**1**	**0.1**	**0.066**	**0.016**
Codeword length [bit]	**256**	**11**	**36**	**63**
Error tol. [b]	**3%**	**9%**	**N/A**	**N/A**
FAR [1/h]	**0**	**≤ 1**	**0.08**	**≤ 1**
T range [°C]	**-40, +95**	**N/A**	**-10, +40**	**-30, +70**
E_n [c] [J]	**1.32**	**1.87**	**1.37**	**1.89**

[a] Power in listening + 1% reception

[b] Percentage of required number of correct received bits in codeword / codeword length

[c] E_n = total energy consumption per day of a node with WuRx as in (1) assuming: I_n^{OFF} = 6 µA [1], I_n^{ON} = 60 µA [1], T_n^{ON} = 60 s [1], V_{dd}^n = 2.5 V, N_{WU}^T = 1 and N_{WU}^F = FAR · 24 h.

IV. Conclusions

A nanowatt WuRX for IoT applications has been presented. The AFE features a dedicated PTAT block for biasing the MOSFET-based diodes in the ED and guarantees a roughly constant WuRX input impedance from -40 °C to +95 °C. This feature ensures both a reduced sensitivity dependence and no Matching Network gain loss over temperature. The GO-CDR in the BBL generates in an energy efficient way a clock phase/frequency aligned with the received data. This allows the reception of 256-bit codewords and the reduction to zero of the number of false wake-ups detected in 60-hour measurements. This results in an overall consumption reduction, which guarantees an energy per day for an IoT node with WuRX lower than prior art.

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