RF Amplification and Filtering Techniques for Cellular Receivers

Amir Bozorg

RF Amplification and Filtering Techniques for Cellular Receivers

by

Amir Bozorg

Master of Science in Electrical Engineering

Tehran Polytechnic, 2012

The thesis is submitted to University College Dublin

in fulfilment of the requirements for the degree of,

Doctor of Philosophy

School of Electrical and Electronic Engineering

Head of School:

Professor Michael Peter Kennedy

Principal Supervisor:

Professor Robert Bogdan Staszewski

May 2021

To my lovely parents, Zar and Ali

To my lovely brother, Amin

"If you want to find the secrets of the universe, think in terms of energy, frequency and vibration."

Nikola Tesla, 1856–1943

Contents

Abstract

The usage of various wireless standards, such as Bluetooth, Wi-Fi, GPS, and 4G/5G cellular, has been continually increasing. In order to utilize the frequency bands efficiently and to support new communication standards with lower power consumption, lower occupied volume and at reduced costs, multimode transceivers, software defined radios (SDRs), cognitive radios, etc., have been actively investigated. Broadband behavior of a wireless receiver is typically defined by its front-end low-noise amplifier (LNA), whose design must consider trade-offs between input matching, noise figure (NF), gain, bandwidth, linearity, and voltage headroom in a given process technology.

Moreover, monolithic RF wireless receivers have been trending toward high intermediate-frequency (IF) or superhetrodyne radios thanks to recent breakthroughs in silicon integration of band-pass channel-select filters. The main motivation is to avoid the common issues in the currently predominant zero/low-IF receivers, such as poor 2nd-order nonlinearity, sensitivity to $1/f$ (i.e. flicker) noise and time-variant dc offsets, especially in the fine CMOS technology. To avoid interferers and blockers at the susceptible *image* frequencies that the high-IF entails, band-pass filters (BPF) with high quality (Q) factor components for sharp transfer-function transition characteristics are now required. In addition, integrated low-pass filters (LPF) with strong rejection of out-of-band frequency components are essential building blocks in a variety of applications, such as telecommunications, video signal processing, anti-aliasing filtering, etc. Attention is drawn toward structures featuring low noise, small area, high in-/out-of-band linearity performance, and low-power consumption.

This thesis comprises three main parts. In the first part (Chapters 2 and 3), we focus on the design and implementation of several innovative wideband low-noise (transconductance)

amplifiers [LN(T)A] for wireless cellular applications. In the first design, we introduce new approaches to reduce the noise figure of the noise-cancellation LNAs without sacrificing the power consumption budget, which leads to NF of 2 dB without adding extra power consumption. The proposed LNAs also have the capability to be used in current-mode receivers, especially in discrete-time receivers, as in the form of low noise transconductance amplifier (LNTA). In the second design, two different two-fold noise cancellation approaches are proposed, which not only improve the noise performance of the design, but also achieve high linearity (IIP3=+4.25 dBm). The proposed LN(T)As are implemented in TSMC 28-nm LP CMOS technology to prove that they are suitable for applications such as sub-6 GHz 5G receivers.

The second objective of this dissertation research is to invent a novel method of band-pass filtering, which leads to achieving very sharp and selective band-pass filtering with high linearity and low input referred (IRN) noise (Chapter 4). This technique improves the noise and linearity performance without adding extra clock phases. Hence, the duty cycle of the clock phases stays constant, despite the sophisticated improvements. Moreover, due to its sharp filtering, it can filter out high blockers of near channels and can increase the receiver's blocker tolerance. With the same total capacitor size and clock duty cycle as in a 1st-order complex charge-sharing band-pass filter (CS BPF), the proposed design achieves 20 dB better out-of-band filtering compared to the prior-art 1st-order CS BPF and 10 dB better out-of-band filtering compared to the conventional 2nd-order C-CS BPF.

Finally, the stop-band rejection of the discrete-time infinite-impulse response (IIR) low-pass filter is improved by applying a novel technique to enhance the anti-aliasing filtering (Chapter 5). The aim is to introduce a 4th-order charge rotating (CR) discrete-time (DT) LPF, which achieves the record of stop-band rejection of 120 dB by using a novel pseudo-linear interpolation technique while keeping the sampling frequency and the capacitor values constant.

Chapter

1

Introduction

We live in a world of communication and the wireless communication, in particular, is a key part of our lives. Some of the commonly used wireless communication systems in our day–to–day life are: mobile phones, GPS receivers, remote controls, Bluetooth audio and Wi-Fi etc. Generally, in a communication system, information is transmitted from the transmitter to the receiver that are placed over a limited distance. With the help of Wireless Communication, the transmitter and receiver can be placed anywhere between few meters (like a T.V. Remote Control) to few thousand kilometers (Satellite Communication).

Figure 1.1 shows that the majority of cellular and wireless standard frequency bands are allocated from 400 MHz to 6 GHz, and have not significantly changed for many years. Meanwhile, the transistor cutoff frequency (f_T) has improved dramatically with scaling, as shown in Figure 1.2. For example, the period from 1999 to 2011 has seen f_T increasing from 20 GHz in 0.35 μm to more than 400 GHz in 28-nm process. This suggests that conventional CT techniques that were optimized for the older technology do not effectively use the ultra-high speed of transistors of scaled CMOS to improve the performance of RF/analog designs.

On the other hand, while the main motivations of CMOS scaling have been to reduce

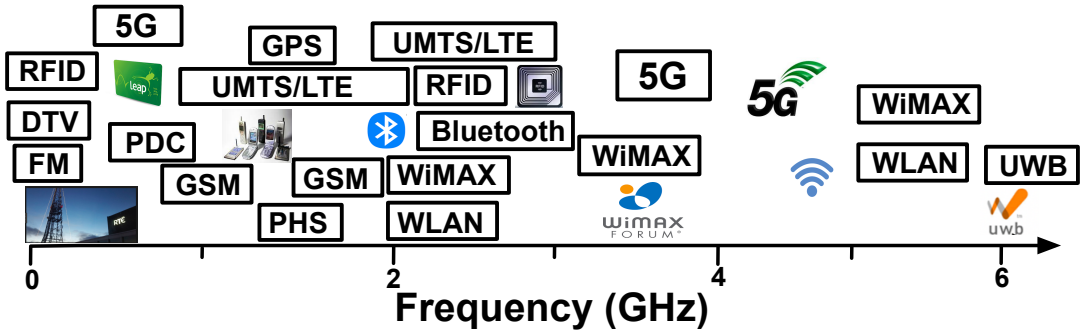


Figure 1.1: Sub- 6 GHz RF spectre.

transistor cost and to improve digital performance, conventional RF/analog designs have not benefited significantly. A finer process node produces shorter digital gate delays while a lowered supply voltage and gate capacitance reduce power consumption. As shown in Figure 1.2, going from 180-nm to 28-nm CMOS, the V_{DD} supply is reduced more than 30% while the MOS threshold voltage (V_{th}) has not changed considerably. Therefore, the precious available voltage headroom for RF/analog design is now reduced dramatically [1]. Considering also the reduced MOS intrinsic gain [1] and its saturation linearity in scaled CMOS [2], continuous-time (CT) RF/analog design is becoming generally more difficult. In this way, the power consumption and area of the traditional RF/analog designs are not directly process scalable.

In contrast, as Fig 1.3(a) shows, the digital RF transceiver (TRX) introduced in [3] mostly

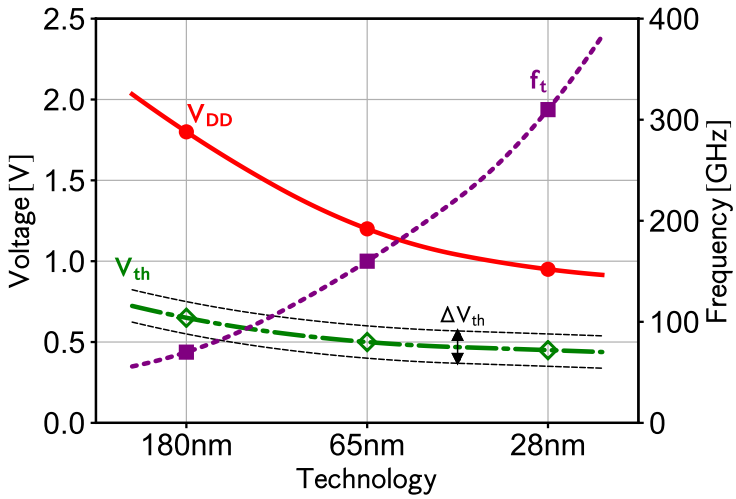
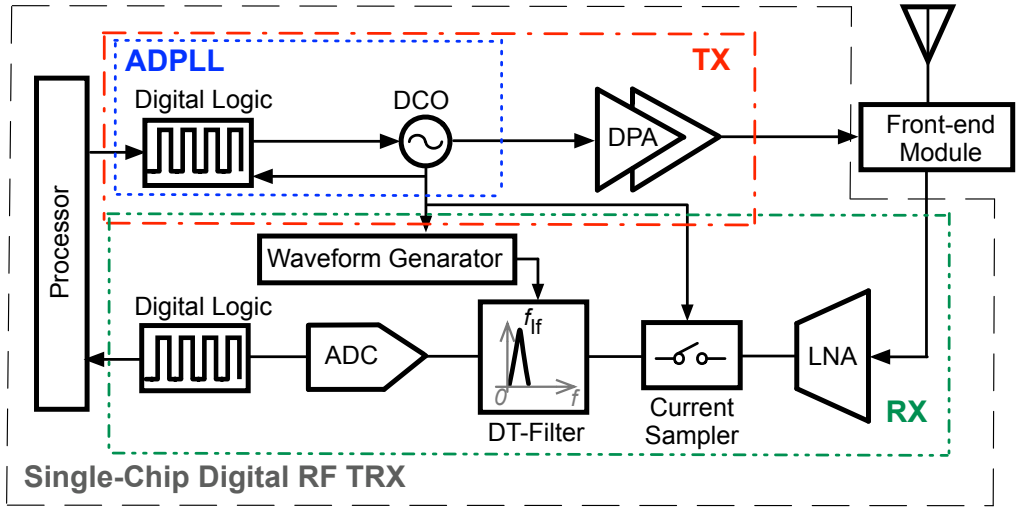
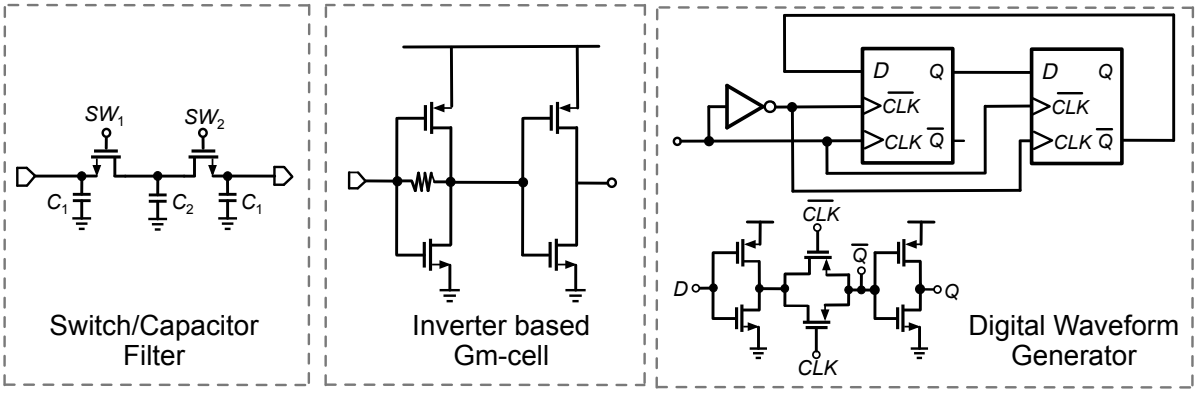


Figure 1.2: Typical CMOS scaling trends for low-power/low-leakage process technology.



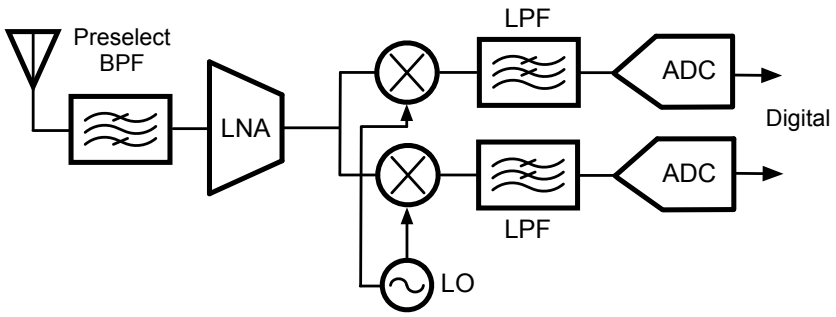
(a)



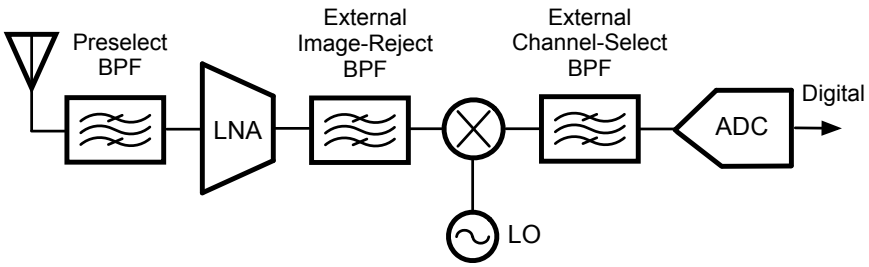
(b)

Figure 1.3: (a) Single chip digital RF transceiver, (b) components used in DT signal processing.

consists of discrete-time (DT) RF/analog blocks (Figure 1.3 (b)) and avoids using complicated traditional analog components such as opamps; most of signal processing and filtering are done using passive switched-capacitor circuits [4, 5]. Waveforms required for driving the switches are also generated using digital logic. To provide signal gain, DT techniques use inverter-based gm-cells that avoid transistor stacking and are always compatible with digital technology. As the technology scales, MOS switches become faster and tinier with lower parasitic capacitances. Digital waveform generator becomes also faster and more power efficient. Moreover, the metal capacitor density improves from one process node to the next, resulting in a reduced area. In addition, the inverter-based gm-cell structure is fully scalable



(a)



(b)

Figure 1.4: Comparison of conventional receiver architectures: (a) zero-IF/low-IF; and (b) superheterodyne.

with improved g_m over its bias current. In this way, DT receivers directly benefit from scaling similar to that in digital circuits. Refs. [6–15] are examples of DT process-scalable receivers.

1.1 Overview of Wireless Receiver Architectures

The pioneers of RFIC integration [16] have quickly realized the superiority of operating receivers at zero-IF (ZIF) and low-IF (LIF) rather than at high-IF (HIF): simpler architecture, and a much higher level of monolithic integration as a result of using low-frequency low-pass filters (LPF) for channel selection [see Figure 1.4(a)]. This was despite the many issues associated with ZIF/LIF receivers: time-variant DC offsets, sensitivity to $1/f$ (flicker) noise, large in-band local oscillator (LO) leakage and the second-order nonlinearity [17–22]. The LO leakage to the low-noise amplifier (LNA) input is amplified and then mixed with the LO again, creating a DC offset. This offset could be up to 2 to 3 orders of magnitude larger than the wanted signal at the mixer output [23]. Considering the LO leakage to antenna, it could be radiated out and subsequently reflected from a moving object back to the antenna. In this case, the DC offset is time-varying and thus much harder to be canceled. In general,

all ZIF/LIF issues were viewed rather as an inconvenience and handled through various calibrations. However, high-performance cellular ZIF/LIF receivers now require extensive calibration efforts. For example: an intensive IIP2 calibration needs to be concurrently run in the background with DC offset and harmonic rejection (HR) calibration [24, 25].

A superheterodyne architecture, shown in Figure 1.4(b), pushes the IF frequency much higher such that the aforementioned problems are not a major concern anymore. Despite the obvious advantages, the superheterodyne radios were abandoned decades ago because it was extremely difficult to integrate a high quality (Q)-factor BPF for image rejection and channel selection in CMOS using continuous-time (CT) circuitry [16].

Furthermore, conventional multi-band, multi-standard cellular receivers (RXs) require many external duplexers, surface acoustic wave (SAW) filters and switches, typically one per band, to attenuate out-of-band (OB) blockers before they reach the sensitive LNA's input. In time-division duplexing (TDD) systems, external SAW filters can be eliminated if the RX chain could handle large interferers (e.g., 0 dBm at 20 MHz away from a GSM channel of interest [26]). On the other hand, for frequency-division duplexing (FDD) systems, the external SAW filters are responsible for not only the filtering of out-of-band blockers but also for duplexing, i.e., separation of concurrent transmit (TX) and RX operations. To reduce the cost and size of the total system solution, in which the external antenna interface network is nowadays the largest contributor, the recent trend is to eliminate SAW filters and switches by using a highly linear wideband RX [18–22, 27]. As a consequence, the isolation of TX-to-RX, and the suppression of TX interferers are worsening, which all further increase the RX linearity requirements in FDD systems.

The resulting reduction in out-of-band filtering implies tough IIP2 requirements (e.g., 90 dBm [22, 25]) for ZIF and LIF receivers. The IIP2 performance of such receivers depends mainly on the second-order nonlinearity of LNA and RF mixer in the receiver chain. Since the typical IIP2 of an RF mixer is between 50–70 dB [28], ZIF/LIF receivers require highly sophisticated calibration algorithms [22, 29–34] to be frequently executed to account for variations in power supply, V_{DD}, [19, 24, 35–38], process corner [38], temperature [39], mixer transistor's gate bias [35], RF blocker frequency [33, 36–38], LO frequency [36–38], LO power [38] and channel frequency [39]. Also, the IIP2 calibration time is rather very slow to find optimum setting for the mixer and it needs to be run repeatedly due to environmental and operational changes [35].

Most of the filtering and amplification in a zero-IF receiver are done after the mixer, at low frequency. In CMOS implementations, the flicker noise of devices at low frequencies corrupts the wanted signal, leading to a higher noise figure (NF) of the receiver. In contrast, filtering and amplification in a superheterodyne are done normally at higher frequencies than the device's flicker corner.

Superheterodyne or HIF architectures, on the other hand, can have a theoretically infinite IIP2. The desired signal and modulated blocker at the RF input will be down-converted to a higher IF and DC, respectively; thus the modulated blocker can be completely filtered out by a band-pass filter (BPF) [40, 41]. For this reason, there is an increasing interest in uncalibrated high-IIP2 SAW-less superheterodyne RXs with integrated blocker-tolerant BPFs that are amenable to CMOS scaling. However, the main challenges towards fully integrated superheterodyne receivers were the non-linearity of LNTA, especially in the FDD mode and the integration of IF bandpass filters. Both of which have been addressed in this work.

1.2 Thesis Objective

Based on the previous discussion, the underlying objective of this thesis is to implement an innovative RF low noise amplifier and band/low pass filter to improve the noise, linearity, blocker tolerance and selectivity of the entire wireless receiver and to take advantage of the future CMOS technology scaling. This will offer better cost than in the traditional techniques.

The first objective of this thesis is to introduce new approaches to reduce the noise figure of the noise cancellation LNAs without sacrificing the power consumption budget. The proposed LNAs also have the capability to be used in the current mode receiver, especially in the discrete-time receiver as a low noise transconductance amplifier (LNTA). The proposed LN(T)As are implemented in TSMC 28-nm LP CMOS technology to prove that it is effective to be applied in 4G/sub-6 GHz 5G receivers.

The second objective of this dissertation research is to invent a novel method which leads to achieving a very sharp and selective band-pass filter with high linearity and low input referred (IRN) noise, which improves the noise and linearity performance without changing the duty cycle of the required clock phases. Moreover, due to its sharp filtering, it can filter out high blocker in from adjacent channels and it increases the receiver blocker tolerance. This technique should be approved and tested in TSMC 28-nm LP CMOS.

The final objective is to improve the stop band rejection of the discrete-time low-pass filter by applying a novel technique. The aim is to introduce a charge-rotating discrete time LPF which achieves the stop-band rejection of the order of 120 dB without increasing the sampling period and the capacitor values. Moreover, this design should be implemented and verified in TSMC 28-nm LP CMOS.

In conclusion, the goal of this work is to invent circuit techniques to improve overall performance of the *overall* receiver path to achieve:

- NF$\sim$2 dB
- IIP3>-5 dBm
- improved filter selectivity
- improved filter stop band rejection $\sim$120
- Flexibility/tunability
- Increased filter order without expense of decreasing the clock sampling period
- minimal power consumption
- minimal active area

1.3 Thesis Outline

The thesis is organized as follows: In Chapter 2, a new noise reduction/cancellation technique is proposed to improve the noise figure (NF) of a broadband low-noise transconductance amplifier (LNTA) for 5G (sub-6 GHz) receivers. The LNTA combines a common-gate (CG) stage for wideband input matching and a common-source (CS) stage for canceling the noise and distortion of the CG stage. Yet another noise reduction is applied to reduce the channel thermal noise of the noise cancellation stage itself. The technique further exploits current reuse and increases transconductance of the CS transistor while keeping its power consumption low. Fabricated in 28-nm CMOS, the proposed LNTA is capable of driving an external 50 Ω load and achieves the noise figure of 2.09 dB to 3.2 dB and input return loss (S_{11}) better than -10 dB over the 3-dB bandwidth of 20 MHz to 4.5 GHz while consuming

4.5 mW from a single 1 V power supply. The achieved gain (S_{21}) and IIP3 are 15.2 dB and -4.6 dBm, respectively.

Chapter 3 discusses two wideband low-noise (transconductance) amplifiers (LN(T)A), in which two novel two-fold noise-cancellation schemes are proposed. Fine tuned for advanced CMOS, the first proposed LNA architecture uses a common-gate input branch to provide wideband input matching. It is followed by two stages of the common-source structure which cancel the noise and distortion of the first and second stages and relax the design restriction on the first noise-cancellation stage. The provided circuit-level analysis is verified by simulations. The proposed LNA is fabricated in 28-nm CMOS. It achieves a minimum noise figure (NF) of 2.5 dB and input return loss (S_{11}) < -15 dB over 0.02–2 GHz bandwidth while consuming only 4.1 mW from a 1 V supply and driving an external 50-Ω load. The -3 dB power gain (S_{21}) is 18.5 dB and IIP3 is +4.15 dBm.

In another design, the proposed LNTA employs a cross-coupled common-gate stage for wideband input matching. By applying a two-fold noise cancellation technique, the channel thermal noise of the first stage is removed, which improves its noise performance and linearity. We perform a detailed analysis of the transfer function, noise and linearity, which are then verified in simulations in TSMC 28-nm LP CMOS technology. The presented LNA achieves a power gain of 18.9–16 dB within 100 MHz $\sim$ 3.7 GHz and the input and output return loss of better than 10 dB. The IIP3 is +2.8 dBm and the noise figure (NF) ranges 1.58–2.4 dB over the band of interest with 24 mW DC power consumption.

In Chapter 4, we propose a novel clock-phase reuse technique for a discrete-time IIR complex-signaling band-pass filter (BPF). This leads to a deep improvement in filtering, especially the stop-band rejection, while maintaining the area, sampling frequency, number of clock phases and their pulse widths. Fabricated in 28-nm CMOS, the proposed BPF is highly tuneable and is capable of achieving a 70 dB stop-band rejection at 50 MHz offset with 25%-duty-cycle clock, while consuming 1.65 mW. The achieved in/out-of-band IIP3 is +2.5 dB and +17.3 dBm, respectively, and the input referred noise (IRN) is 1 nV/$\sqrt{\text{Hz}}$.

Chapter 5 introduces a new architecture of a discrete-time charge-rotating low-pass filter (LPF) which achieves a high-order of filtering and improves its stop-band rejection while maintaining a reasonable duty cycle of the main clock at 20%. Its key innovation is a linear interpolation within the charge-accumulation operation. Fabricated in 28-nm CMOS, the proposed IIR LPF demonstrates a 1–9.9 MHz bandwidth programmability and achieves a

record-high 120 dB stop-band rejection at 100 MHz while consuming merely 0.92 mW. The in/out-of-band IIP3 is +18.6/+26.6 dBm.

Finally, Chapter 6 concludes this dissertation and presents suggestions for future developments.

1.4 Original Contribution

The original contributions of this dissertation are as follows:

- Introducing several new wideband LN(T)As with improved noise and linearity performance (Chapter 2 and 3);
- Comprehensive analysis of gain, noise and linearity of LN(T)As structures (Chapter 2 and 3);
- Implementing and verifying the proposed wideband two-fold noise cancellation and noise reduction LN(T)As in 28-nm CMOS technology (Chapter 2 and 3);
- Proposing a novel complex charge sharing band pass filter (Chapter 4);
- Comprehensive analysis of transfer function and noise of BPF structures (Chapter 4);
- Implementing and verifying the proposed complex charge-sharing BPF in 28-nm CMOS technology (Chapter 4);
- Proposing a new charge-rotating infinite impulse-response low-pass filter (Chapter 5)
- Implementing and testing the proposed charge-rotating IIR LPF with linear interpolation in 28-nm CMOS technology (Chapter 5);

The list of IC chips and publications resulting from this work is at the end of this dissertation document.

Chapter

2

Wideband Noise-Cancelling LNTA

To be able to amplify an RF signal located at any of the supported frequency bands in a receiver, wideband noise cancelling LNA [42] appears to be a good choice. As the introduced receiver in Chapter 4 is based on sampling the input charge, the RF amplifier needs to provide current rather than voltage, thus acting as a transconductance amplifier (TA) exhibiting a high output impedance, as compared to the input load of its subsequent stage. An LNTA (i.e., LNA+TA) could trivially be constructed by cascading the LNA and TA (g_m) stages [43–46]. However, to improve noise and linearity, both of these circuits should be co-designed and tightly coupled [13], [47].

2.1 Introduction

The usage of various wireless standards, such as Bluetooth, Wi-Fi, GPS, and 2G/3G/4G/5G cellular, has been continually increasing. In order to utilize the frequency bands efficiently and to support more communication standards with lower power consumption, lower occupied volume and at reduced costs, multimode transceivers, software defined radios (SDRs),

cognitive radios, etc. have been actively investigated [48].

Broadband behavior of a wireless receiver is typically defined by its front-end low-noise amplifier (LNA), whose design must consider trade-offs between input matching, noise figure (NF), gain, bandwidth, linearity, and voltage headroom in a given process technology. There are several wideband LNA design topologies and techniques, including filter type amplifiers [49], g_m-enhancement technique [50], common-gate (CG) amplifiers [51], resistive shunt feedback amplifiers [52–54], and distributed amplifiers [55].

A very wide bandwidth LNA can be constructed using a common-source (CS) amplifier topology with several bandpass filters for providing wideband input matching. In [49], a three-section bandpass Chebyshev filter is used to resonate the reactive part of the input impedance to provide wideband input matching over the whole band from 3.1 to 10.6 GHz. However, several of associated bulky inductors there occupy a large chip area, which makes this technique not suitable for wideband applications below 3 GHz [55]. Moreover, although the CS configuration typically ensures better noise performance than in a CG structure, a low quality factor (Q) of on-chip inductors, especially those at the gate of input stage, deteriorate the noise performance where the minimum achieved NF is limited to 4.2 dB. Distributed amplifiers satisfy the required bandwidth for SDRs and optical communications, but they need several parallel stages to simultaneously provide a sufficiently high bandwidth and gain, thus resulting in high power consumption and large chip area. Moreover, they suffer from high NF due to noise from the gate's line-termination resistors and losses in the inductors [55].

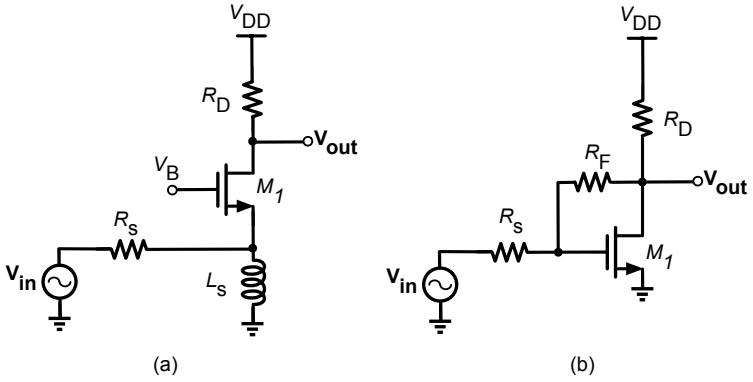


Figure 2.1: Common wideband input-matching techniques: (a) common-gate, and (b) shunt-feedback CS amplifiers.

Among popular techniques for designing wideband LNAs, CG and shunt-feedback CS structures, shown in Fig. 2.1, are of particular interest. The CG stage in Fig. 2.1(a) can

realize a broadband input impedance matching without extra components. Since the parasitic gate-drain capacitor there is AC grounded, the CG amplifier has a better input-output isolation than in a shunt-feedback CS amplifier [51]. The linearity of the CG structure is better than that of the CS amplifier, because in the former the input source resistance further provides the source degeneration. The input impedance of the CG structure is roughly $1/(g_{mb1} + g_{m1})$ and the noise factor is $F = 1 + (\gamma/\alpha g_{m1} R_S) + (4/g_{m1} R_D)$ [51], where γ is the excess noise factor in short-channel devices and α is the ratio $\alpha = g_m/g_{ds0}$ of the small-signal transistor transconductance g_m to the zero-bias drain conductance g_{ds0}. g_{mb} models the transistor's body effect. This structure suffers from poor noise performance since its total g_m should be 20 mA/V so as to satisfy the input matching condition. A popular method to enhance its noise performance is a noise-cancellation technique provided by a successive stage, which removes the channel thermal noise of the main CG transistor [42]. However, the aggregate noise performance is now limited by the channel thermal noise of the cancellation stage. Finally, another architecture in [56] uses current combining as a means to provide noise cancellation in a receiver which not only cancels the noise due to the antenna input resistance, but the base-band noise of a transimpedance amplifier (TIA) is also up-converted to RF and canceled out there.

In the following, two noise cancellation schemes will be introduced where in the first structure we further improve upon the aggregate noise performance of the CG architecture with the successive noise-canceling stage by reducing the channel thermal noise of the cancellation stage itself. The key aim is to lower the NF without increasing the consumed power, which is mainly achieved by employing a current-reuse technique. Then, in the second architecture, a two-fold noise cancellation is introduced, which shows how the noise performance of the CG architecture can be improved while simultaneously providing high gain.

2.2 Overview of Noise-Cancellation and -Reduction Techniques

In this section, we first describe the basic idea of noise-cancellation scheme. Then, based on that, we propose a new noise-reduction technique. Finally, the two techniques are combined in a manner that saves power.

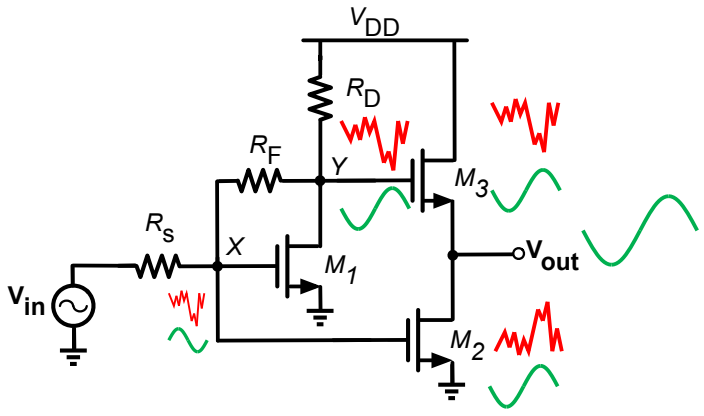


Figure 2.2: Conventional noise cancellation of M_1 configured as a CS shunt-feedback amplifier (biasing not shown).

2.2.1 Conventional Noise-Cancellation Technique

The most important noise source in CMOS LNAs is the channel thermal noise of MOS transistors. This noise is modeled as a shunt current source across the transistor's drain and source terminals. The designer's goal is to minimize the generation and propagation of this noise. Among various publications introducing noise-cancellation techniques in LNAs, [42, 57–59] are noteworthy.

The conventional noise-cancellation scheme in the CS shunt-feedback topology is shown in Fig. 2.2. The noise current of the main, i.e. input-matching, transistor, M_1, flows through the feedback resistor, R_F, towards the M_1 gate and creates two noise voltages at nodes X and Y with the same phase but different amplitudes. On the other hand, the *signal* voltage at these nodes has opposite polarities and different amplitudes due to the inverting operation of the M_1 amplifier. The signal and noise polarities being opposite at nodes X and Y make it possible to cancel the noise originating from the input-matching transistor while adding the signal contributions constructively. The noise voltage at node X, V_{nX}, is amplified and inverted by M_2, while the noise voltage at node Y, V_{nY}, is passed across M_3 barely changed. At the output node, the two voltages with opposite phases are canceled. Ultimately, the channel thermal noise of M_1 will be greatly attenuated or altogether canceled provided that

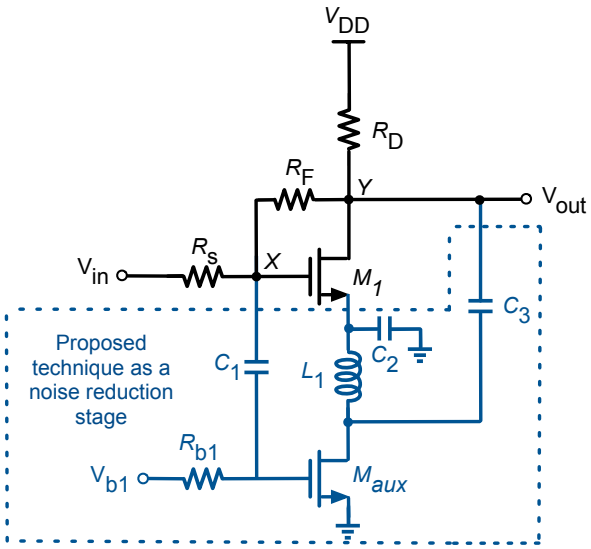


Figure 2.3: Proposed noise-reduction technique of M_1's channel noise.

the following condition is satisfied:

$$\begin{aligned} V_{n,out} =& V_{nY}\frac{r_{ds2}}{r_{ds2}+1/g_{m3}} - v_{nX}\frac{g_{m2}}{g_{m3}} = 0 \\ & \frac{R_F+R_s}{R_s} = \frac{g_{m2}}{g_{m3}} \end{aligned} \tag{2.1}$$

where $g_m r_{ds} \gg 1$ was assumed.

As mentioned, this kind of noise cancellation is commonly used in LNA structures with the CS input stage. The main drawback here is the need for the extra following stage in order to amplify and invert the voltage noise at node X and add it with the voltage noise at the output. According to (2.1), since the feedback resistor is much larger than the input source resistor, $R_F \gg R_s$, the transconductance of M_2, g_{m2}, must be large enough to satisfy the noise-cancellation condition, but at a cost of higher power consumption. In the following, we offer a new technique which can be used either as a noise cancellation or as a noise-reduction technique *without* substantially increasing the power consumption.

2.2.2 Noise-Reduction Technique

2.2.2.1 Technique to Cancel the Noise of Main Transistor

The aforementioned goal of improved noise performance at no extra consumed power can be achieved by means of a current-reuse technique that was inspired by [60, 61]. Figure 2.3 shows the proposed method. Just as in Fig. 2.2, channel noise of the main transistor M_1 develops a noise voltage at node Y, V_{nY}, which appears on its gate at node X as V_{nX} via the resistive divider attenuation $R_S/(R_S + R_F)$. Likewise, it is then amplified and inverted via M_{aux}. Here, however, the M_{aux}'s current is injected right back into node Y via C_3 to subtract the original noise perturbation in the M_1's channel. This way, there is no need for an extra branch M_3 used in the conventional noise cancellation of Fig. 2.2. Further, the source of M_1 is connected to the ground via C_2. Inductor L_1 provides some AC isolation between the source of M_1 and drain of M_{aux}. By stacking M_1 on top of M_{aux} dc-wise, the dc current is reused, and M_{aux} is biased by the main transistor current. However, AC-wise, M_{aux} is paralleled with the main transistor M_1 by means of C_1 and C_3, but completes the negative feedback around M_1 for its noise. For the proposed technique to cancel the noise of M_1, the following condition should be met:

$$\begin{aligned} V_{n,out} =& V_{nY} - v_{nX} g_{m_{\text{aux}}} R_D = 0 \\ & \frac{R_F + R_s}{R_s} = g_{m_{\text{aux}}} R_D \end{aligned} \tag{2.2}$$

Equation (2.2) suggests that the full noise cancellation of M_1 is rather expensive in terms of consumed power since the ratio of R_F/R_D and $g_{m_{\text{aux}}}$ need to be very high. However, this technique could be beneficially used at low expended power for a *partial* noise cancellation, i.e. noise *reduction*, of M_1.

2.2.2.2 Current Reuse Technique as Noise Reduction

Noise factor excess, F_{M1}, contributed by the M_1 transistor of the shunt-feedback CS amplifier shown in Fig. 2.1(b) is calculated as:

$$\begin{aligned} F_{M1} &= \left| \frac{\overline{V}^2_{n,M1}/A_v^2}{\overline{V}^2_{n,Rs}} \right| = \left| \frac{\overline{I}^2_{n,M1} Z^2_{out}}{\overline{V}^2_{n,Rs} A_v^2} \right| \\ &= \frac{4kTg_{m1}|Z_{out}|^2}{kTR_s g_{m1}^2 |Z_{out}|^2} \frac{\gamma}{\alpha} = \frac{4}{R_s g_{m1}} \frac{\gamma}{\alpha}. \end{aligned} \tag{2.3}$$

where, Z_{out} is the output impedance of the amplifier as seen by the unloaded output node. In addition, $\overline{I}^2_{n,M_1} = 4kTg_{m1}\gamma$ is the channel thermal noise of M_1 and $|A_v| \simeq g_{m1} Z_{out} \cdot Z_{in}/(Z_{in} + R_S)$ is the voltage gain of M_1, where $Z_{in} = R_F/(1 + g_{m1}R_D)||1/sC_{in}$, and C_{in} is due to parasitics at the gate of M_1, for the sake of simplicity Z_{in} is considered equal to R_s. Hence, the noise factor of the shunt-feedback amplifier shown in Fig. 2.1(b) is approximately equal to [53]:

$$F_{(\text{fig1b})} \geqslant 1 + \frac{4}{R_s g_{m1}} \frac{\gamma}{\alpha} \tag{2.4}$$

According to (2.4), the noise factor has a reverse relationship with the transconductance. It means that by increasing the transconductance of the main transistor, the circuit's relative noise contribution is decreased. However, this results in a higher power dissipation.

By using the proposed current-reuse technique of Fig. 2.3, the noise factor is roughly equal to: $F_{(\text{fig3})} = 1 + F_{M1} + F_{M_{\text{aux}}}$ where F_{M1} and $F_{M_{\text{aux}}}$ are expressed by:

$$\begin{aligned} F_{M1} &= \frac{4kTg_{m1}|Z_{out}|^2}{kTR_s(g_{m1} + g_{m_{\text{aux}}})^2 |Z_{out}|^2} \frac{\gamma}{\alpha} \\ &= \frac{4g_{m1}}{R_s(g_{m1} + g_{m_{\text{aux}}})^2} \frac{\gamma}{\alpha}. \end{aligned} \tag{2.5}$$

$$\begin{aligned} F_{M_{\text{aux}}} &= \frac{4kTg_{m_{\text{aux}}}|Z_{out}|^2}{kTR_s(g_{m1} + g_{m_{\text{aux}}})^2 |Z_{out}|^2} \frac{\gamma}{\alpha} \\ &= \frac{4g_{m_{\text{aux}}}}{R_s(g_{m1} + g_{m_{\text{aux}}})^2} \frac{\gamma}{\alpha}. \end{aligned} \tag{2.6}$$

Finally, the total noise factor of the presented structure, without considering the thermal

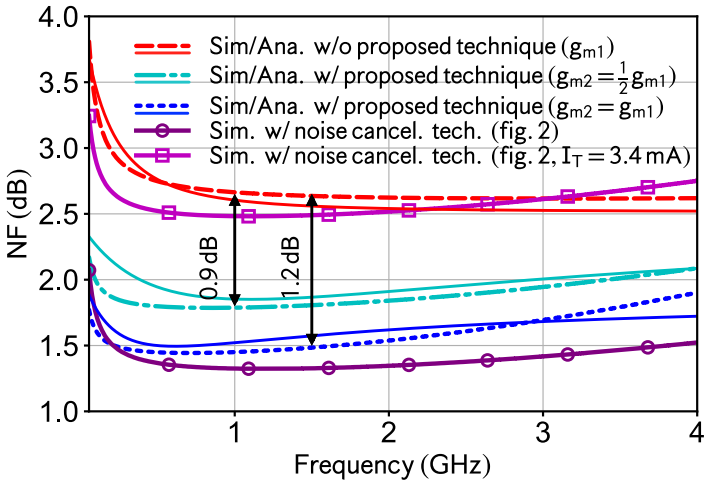


Figure 2.4: Comparison of simulated/derived NF of the shunt feedback CS amplifier of Fig. 2.1(b), with the same structure but with the noise-reduction technique of Fig. 2.3, while both structures sink the same current, 1.7 mA, from 1 V supply. NF of the conventional noise-cancellation configuration (Fig. 2.2) is included for reference.

noise of R_D, is approximately given by:

$$F_{(\text{fig3})} \geq 1 + \frac{4\gamma}{\alpha(g_{m1}+g_{m_{\text{aux}}})R_s} + \frac{4}{R_s R_D (g_{m1}+g_{m_{\text{aux}}})^2} \tag{2.7}$$

From the standpoint of the received signal, M_{aux} is paralleled with the main transistor M_1, and hence, according to (2.7), their transconductances are summed up. This boost in transconductance reduces the noise figure without increasing the bias current. Without the current-reuse technique, M_{aux} would be paralleled with M_1 in a conventional way as in Fig. 2.2, and the structure would consume twice the power in order to achieve the same NF. Nonetheless, the main drawback of the new technique is the reduced voltage headroom leading to some deterioration of linearity.

To demonstrate the benefit of the noise-reduction technique introduced in Fig. 2.3, we now apply it into the CS noise-canceling LNA of Fig.2.2 for the purpose of reducing the noise of the latter's second stage (i.e. M_2). To have a better comparison between Figs. 2.2 and 2.5, their respective simplified noise factors, $F_{(\text{fig2})}$ and $F_{(\text{fig5})}$, are calculated as:

$$F_{(\text{fig2})} \geq 1 + \frac{\gamma}{\alpha g_{m2} R_s} + \frac{\gamma g_{m3} + \alpha R_D g_{m3}^2}{\alpha R_s g_{m2}^2} \tag{2.8}$$

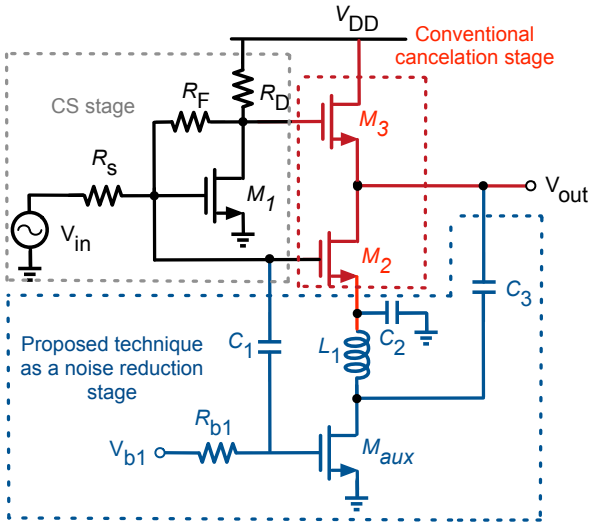


Figure 2.5: Conventional noise cancellation along with the proposed noise-reduction technique.

$$F_{(\text{fig5})} \geq 1 + \frac{\gamma}{\alpha(g_{m2} + g_{m_{\text{aux}}})R_s} + \frac{\gamma g_{m3} + \alpha R_D g_{m3}^2}{\alpha R_s (g_{m2} + g_{m_{\text{aux}}})^2} \tag{2.9}$$

By comparing (2.8) and (2.9), it can be seen that for the same value of g_{m2} and g_{m3} in both structures (Figs. 2.2 and 2.5), the noise performance in Fig. 2.5 has improved.

The efficacy of the proposed noise-reduction technique of Fig. 2.3 is illustrated by the NF circuit simulation plots in Fig. 2.4 with superimposed analytical plots to verify the derived noise equations[1]. It is compared with the basic shunt feedback amplifier of Fig. 2.1(b) consuming the same power of 1.7 mW. The minimum NF of the basic amplifier is 2.65 dB, while the new technique improves it to 1.45 dB. The obtained NF is now within a small fraction of a dB to the straightforward manner of noise cancellation shown in Fig. 2.2, but which consumes as much as 10 mW. However, when the current is insufficiently high, not only the noise of the first stage cannot be canceled entirely, but it ends up actually adding more noise sources to the circuit, which results in increasing the NF. While we maintain the current of the second stage at 1.7, mA, at the same level as the current of the first stage (the total current of Fig. 2.2 in this case is 3.4 mA), the current of Fig. 2.3 can be just

[1]We extend (2.4) and (2.7) by further considering the thermal noise of R_{D1}, i.e. $F \simeq 1 + [(R_D(R_F(1 + (g_{m1} + kg_{m1})R_D))^2/R_s(Z_D + R_F(1 + (g_{m1} + kg_{m1})R_D))^2 Z_D^2(g_{m1} + kg_{m1})^2(R_F + R_F Z_{in} C_{in} s + g_{m1} R_D Z_{in} + Z_{in})^2] + [\gamma/4(R_s(g_{m1} + kg_{m1})(R_s/(R_s(1 + R_s C_{in} s) + R_s)^2)] + (4R_s/R_F)$, where $k = 0$ gives the result for basic circuit and also, since R_F is high, its noise effect, $4R_s/R_F$, in the total noise factor is negligible.

1.7 mA. As shown in Fig. 2.4, the noise-cancellation technique of this case improves the noise performance slightly (i.e. 0.2 dB). The power efficiency advantages could be summarized as follows: According to (2.1), which describes the conventional noise-cancellation technique, the current of the second stage should be increased in order to satisfy the noise-cancellation condition, resulting in more power drain. Moreover, there are at least two branches in the conventional noise-cancellation technique, which means an extra power consumption because, in addition to the main branch, M_1, the cancellation branch, $M_{2,3}$ drains an extra dc current, while in the proposed technique there is only one branch, which reuses the DC current for M_1 and M_2.

The salient feature of the proposed noise *reduction* technique of Fig. 2.3 is that it consists of a single stage and it saves power by means of the current reuse. This feature allows the structure to be incorporated into the (second) noise *cancellation* stage of the two-stage amplifier of Fig. 2.2, as illustrated in Fig. 2.5 (another example will be shown Section 2.3). This way, the channel thermal noise of the noise-canceling device itself (M_2) will be reduced at no extra power. As a net result, the noise-cancellation condition is satisfied more effectively. This is given by:

$$\begin{aligned} \overline{V}^2_{n,out} &= \overline{V}^2_{nY}\left(\frac{r_{ds2}||r_{ds_{\text{aux}}}}{r_{ds2}||r_{ds_{\text{aux}}}+1/g_{m3}}\right)^2 \\ &\quad -\overline{V_{nX}}^2\left(\frac{g_{m2}+g_{m_{\text{aux}}}}{g_{m3}}\right)^2 \\ V_{n,out}=0 \Rightarrow \frac{R_F+R_s}{R_s} &= \frac{g_{m2}+g_{m_{\text{aux}}}}{g_{m3}} \end{aligned} \tag{2.10}$$

In (2.10), g_{m2} is added to g_{m4}, and hence the noise-cancellation condition can be satisfied at lower power. Therefore, applying the proposed noise-reduction approach in the noise-cancellation stage of the conventional noise-cancellation scheme reduces the power dissipation without affecting the NF. Moreover, the added new transistor, M_{aux}, also decreases the noise contribution of the cancellation stage, M_2, without any extra power.

It is worth mentioning that (2.10) is used just to show the beneficial effect of M_{aux} in the conventional noise-cancellation condition, so the parasitic capacitances are not considered. Although, in practice, the condition of (2.10) is not completely satisfied due to the parasitic capacitances and the limitation of power consumption, the noise will be reasonably attenuated

even by meeting this condition partially.

2.3 Noise Reduction Noise Cancellation LNTA

The previous section introduced the noise-cancellation and -reduction techniques. An example was given in Fig. 2.5 on how they could be beneficially combined to form a noise-canceling LNA in the CS configuration that saves significant power. The channel thermal noise of the noise-cancellation stage (M_2 in the second stage in Fig. 2.2) was reduced by applying the noise reduction by M_{aux} of Fig. 2.3.

These techniques are now combined such that the channel thermal noise of the noise-cancellation stage, which operates now on the input-matching CG stage, is reduced by applying the same noise-reduction technique. Figure 2.6 shows the proposed wideband LNTA. We take advantage of the CG input stage, M_1, to provide the wideband 50 Ω input matching. M_2 and M_3 of the CS stages are configured to cancel the channel thermal noise of M_1. To reuse the M_2 current and to improve the IIP3 linearity, M_3 is chosen now as a pMOS transistor. The external antenna-port inductor L_s is employed to provide a dc current path to ground and to damp the total parasitic capacitance at the input node. In the proposed noise-reduction technique, by exploiting the current-reuse, transistor M_4 is paralleled AC-wise with M_2, thus boosting its transconductance and hence decreasing its thermal noise effects. The pMOS-nMOS structure and "sweet spot" biasing are applied to improve the linearity. Moreover, the off-chip inductor L_s is on a PCB, hence its value can be fairly large, in the order of a few 100s of nH, which can resonate out all parasitics at the input node at 1.2–1.5 GHz.

2.3.1 Input Matching

To consider the body effect of the wideband input-matching common-gate M_1 transistor and also to simplify the relations, G_{m1} stands for $(1+R_{D0}g_{m0})(g_{m1}+g_{mb1}) \approx (1+R_{D0}g_{m0})g_{m1}$. Hence, the input impedance is given by:

$$\begin{aligned} Z_{in} &= (R_{Ls}+sL_s)\left\|\frac{1}{sC_X}\right\|\frac{1}{G_{m1}} \\ &= \frac{R_{Ls}+sL_s}{C_XL_ss^2+(R_{Ls}C_X+G_{m1}L_s)s+(G_{m1}R_{Ls}+1)} \end{aligned} \tag{2.11}$$

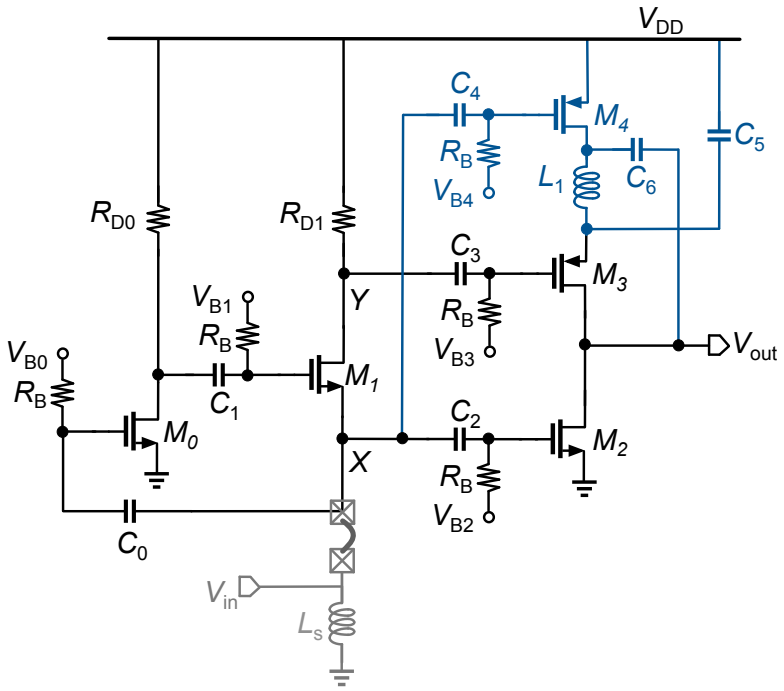


Figure 2.6: Proposed wideband LNTA with noise-cancellation and -reduction techniques (the blue part is the proposed noise-reduction technique).

where C_X lumps the total parasitic capacitance at node X which is damped by L_s. Since L_s is external and connected to the antenna pin, thus not consuming any extra pads on the chip, it can be fairly large (150 nH), therefor (2.11) can be simplified to $Z_{in} = 1/(sC_X + G_{M1})$. This shows that the input matching is mainly defined by M_0 and M_1. In this case, if the size of L_s changes, for instance, from 150 nH to 200 nH, there will be just a barely noticeable affect on S_{11}. However, the lower limit of bandwidth (f_L) will be improved. On the other hand, if the size of L_s is decreased, its series resistance, R_{Ls}, will go down (to as low as 5 Ω) for the constant Q-factor of L_s. This resistance is paralleled with $1/G_{m1}$ and so it lowers the equivalent input impedance. Although, a new technique was described in [62] to extend the bandwidth at lower frequencies without increasing the size of L_s, here an *off-chip* inductor in-parallel with the IC antenna input pin is used to realize L_s in order to save the silicon die area. Although the g_m-boost transistor, M_0, adds a bit more parasitics to the input node, it is of small size so it does not affect the bandwidth substantially. By increasing its size from W=10 μm to 20 μm, the simulated upper cutoff frequency lowers by 450 MHz, from 7.78 to 7.33 GHz.

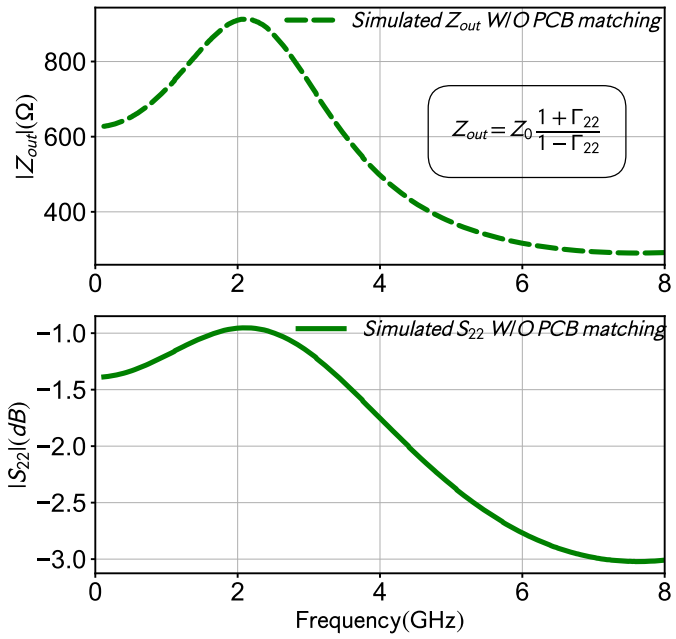


Figure 2.7: Simulated output impedance without matching network on PCB .

2.3.2 Gain Analysis

The equivalent impedance seen from the drain of M_1 towards the ground is termed Z_Y and is equal to $R_{D1}||[r_{ds1} + (1/sC_X||sL_s)(1 + G_{m1}r_{ds1})]||1/sC_Y$, where R_{D1} is the load resistance of M_1, and C_Y is the total parasitic capacitance at node Y. Z_{out} determines the output impedance which is calculated as $r_{ds2}||r_{ds3}||r_{ds4}||1/sC_{out}$, where C_{out} is the total output parasitic capacitance seen by V_{out}. Therefore, the voltage gain of the proposed LNTA is given by:

$$A_v = -\frac{1/G_{m1}}{1/G_{m1} + R_s}(G_{m1}g_{m3}|Z_Y| + g_{m2} + g_{m4})|Z_{out}| \tag{2.12}$$

As mentioned above, the proposed design can be used either as an LNTA in an integrated current-mode RX or as a standalone LNA if it is externally loaded by a 50 Ω termination. In the latter, the amplifier must properly handle the intermediate network of wire-bonding inductance, pad capacitance, package parasitics, and PCB transmission lines (TL) and components. Figure 2.7 shows the simulated output impedance of the proposed LNTA, which confirms that it is suitable for the current-mode application where its output impedance is at least eight times larger than the 50 Ω load impedance [63]. In this matching network, the

pad capacitance is in parallel with Z_{out} where the equivalent impedance is in series with the wire-bond inductance. The rest of matching network is provided on the PCB by using SMD capacitors and TLs which makes the equivalent output impedance to be compatible with 50 Ω.

To examine the effect of the 50-Ω load impedance of the external test equipment on the gain of the proposed structure, (2.12) for A_v is plotted in Fig. 2.8. As expected, when unloaded, the voltage gain is high since Z_{out} is high[1]. When the amplifier is loaded with 50 Ω, the provided gain drops by ∼20 dB.

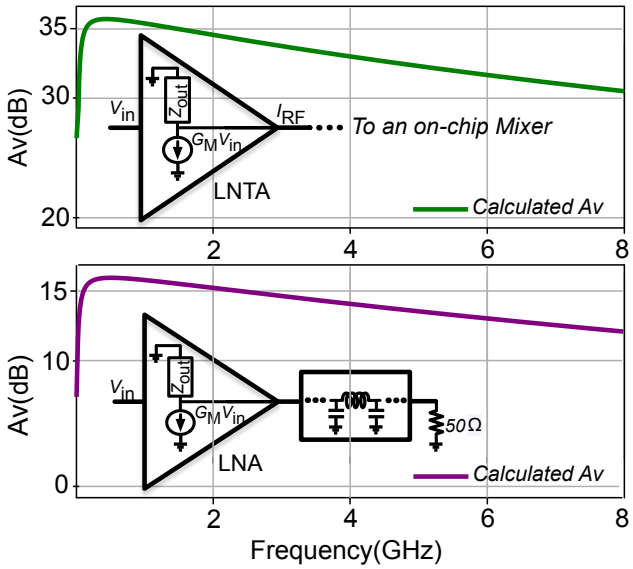


Figure 2.8: Calculated A_v from (2.12) (top) when the amplifier is self-loaded in the LNTA mode, (bottom) when the amplifier is loaded by 50 Ω through matching network in the LNA mode.

Unfortunately, the technology scaling causes r_{ds} to be reduced. Also, by employing the pMOS transistors at the output node, the parasitic capacitances go up, resulting in more variation in Z_{out} at high frequencies. These are the main reasons that limit the LNTA bandwidth at high frequencies. To solve this problem, the inductive shunt-peaking and series-peaking techniques can be used. The shunt inductive peaking causes a resonance at the output of each stage when the gain starts to roll off at higher frequencies [62]. It is worth mentioning that L_1 also helps to dampen the parasitic capacitance at the output node. By increasing L_1 from 240 pH to 1.2 nH, the 3-dB bandwidth can be extended from 7.5 to 9 GHz.

[1]When the LNTA transconductance drives an internal on-chip mixer, its *voltage* gain will actually be very low but it can be recovered in subsequent stages [64].

The quality factor of L_1 improves the gain only marginally. Increasing it from 5.5 to 10 (L_1 = 440 pH), the gain improves only by 0.1 dB.

2.3.3 Noise Analysis

As mentioned above, the purpose of noise cancellation is to disassociate the input matching from the noise considerations by virtue of canceling the noise from the matching stage at the output node [42]. In the proposed LNTA, the current noise of the input transistor flows *into* node X, but *out of* node Y, causing two voltages with opposite phases. These two voltages are converted into currents by M_2 and M_3 [65]. However, the input signal appears at these two nodes at the same phase. Thus, the input signal is constructively combined at the output. The two noise voltages are calculated as $V_{nX}{}^2 = Z_{in}^2 I_{n,M1}^2$ and $V_{nY}{}^2 = Z_Y^2\ I_{n,M1}^2$. Therefore, the output current noise due to the thermal noise of M_1 is as follows:

$$\begin{aligned} \overline{I_{n,out}}^2 &= \overline{V_{nX}}^2 (g_{m2} + g_{m4})^2 - \overline{V_{nY}}^2 g_{m3} = 0 \\ &\Rightarrow \frac{g_{m2} + g_{m4}}{g_{m3}} = \frac{Z_Y}{Z_X} \end{aligned} \tag{2.13}$$

To reuse the current of M_2, M_3 is chosen as a pMOS transistor. Also, the noise-reduction technique is applied to improve the NF without any additional power cost. In this technique, M_4 is in-parallel with M_2, and hence, the transconductance of M_4 is added to that of M_2. Moreover, M_4 is selected as a pMOS transistor in order to be able to reuse the current of M_2. The consequential increase of M_2's transconductance reduces the channel thermal noise of the cancellation stage, thus avoiding any need for extra branches. Consequently, the improvement in noise figure is achieved without burning more current, as explained in Section 2.2.

The most important noise sources in this noise-cancellation scheme are the thermal noise of R_{D1} and the channel thermal noise of transistors M_2, M_3, and M_4. The noise factor of the proposed LNA is equal to $F = 1 + F_{R_{D1}} + F_{M2} + F_{M3} + F_{M4}$, where the $F_{R_{D1}}$ term is given by the following relation:

$$\begin{aligned} F_{R_{D1}} &= \frac{4kTR_{D1}(g_{m3}|Z_{out}|)^2 (Z_{o1}/(Z_{o1} + R_{D1}))^2}{4kTR_s A_v^2} \\ &\cong \frac{R_s}{R_{D1}} \end{aligned} \tag{2.14}$$

where, according to Fig. 2.6, $Z_{o1} = [r_{ds1} + (R_s||1/sC_X||sL_s)(1 + G_{m1}r_{ds1})]$ and $Z_Y = R_{D1}||Z_{o1}$ when the parasitic capacitance at node Y is not considered for simplicity. A_v is the voltage gain of the LNTA, which is simplified by considering the noise cancellation and input matching conditions, $(g_{m2} + g_{m4})R_s = g_{m3}R_{D1}$ and $Z_{in} = R_s = 1/G_{m1}$, respectively. The other constituting terms of the noise factor F are:

$$\begin{aligned} F_{M2} &= \frac{4kTg_{m2}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{4g_{m2}}{R_s(Z_YG_{m1}g_{m3}+g_{m2}+g_{m4})^2}\frac{\gamma}{\alpha} \\ &\cong \frac{g_{m2}}{R_s(g_{m2}+g_{m4})^2}\frac{\gamma}{\alpha} \end{aligned} \tag{2.15}$$

$$\begin{aligned} F_{M3} &= \frac{4kTg_{m3}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{4g_{m3}}{R_s(Z_YG_{m1}g_{m3}+g_{m2}+g_{m4})^2}\frac{\gamma}{\alpha} \\ &\cong \frac{R_s}{|Z_Y|^2g_{m3}}\frac{\gamma}{\alpha} \end{aligned} \tag{2.16}$$

$$\begin{aligned} F_{M4} &= \frac{4kTg_{m4}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{4g_{m4}}{R_s(Z_YG_{m1}g_{m3}+g_{m2}+g_{m4})^2}\frac{\gamma}{\alpha} \\ &\cong \frac{g_{m4}}{R_s(g_{m2}+g_{m4})^2}\frac{\gamma}{\alpha}. \end{aligned} \tag{2.17}$$

By considering the noise-cancellation condition, (2.16) can be simplified as:

$$\begin{aligned} F_{M3} &= \frac{\gamma R_s}{\alpha|Z_Y|^2g_{m3}} \cong \frac{\gamma R_s}{R_{D1}(g_{m2}+g_{m4})R_s\alpha} \\ &\cong \frac{\gamma}{\alpha R_{D1}(g_{m2}+g_{m4})}. \end{aligned} \tag{2.18}$$

Finally, the total noise factor of the LNTA is approximately given by:

$$F \cong 1 + \frac{R_s}{R_{D1}} + \frac{\gamma}{\alpha R_{D1}(g_{m2}+g_{m4})} + \frac{\gamma}{\alpha R_s(g_{m2}+g_{m4})} \tag{2.19}$$

where the fourth component is the total noise factor due to M_2 and M_4 transistors. According to (2.19), to reduce the noise contribution of R_{D1}, its value should be increased, but, this is limited by the voltage drop on R_{D1}. In addition, the channel thermal noise of M_3 can be decreased by enhancing g_{m2}. As suggested by (2.19), the noise factor of M_2 is decreased since

g_{m4} is added to g_{m2} without any power penalty.

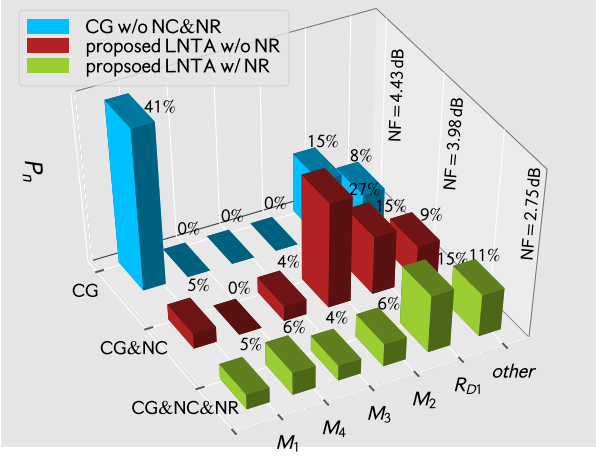


Figure 2.9: Relative contributions to the total noise factor F of various circuit components at 800 MHz for: CG structure ("CG w/o NC & NR"), proposed structure without the noise-reduction technique ("LNTA w/o NR"), and the proposed LNTA ("LNTA w/ NR"). Note: the complement to 100% is due to the 50-Ω antenna-terminal thermal source.

The simulated relative contributions of noise sources to the total noise factor, F, at 800 MHz are shown in Fig. 2.9. The proposed LNTA is compared with two other designs: 1) the CG topology shown in Fig. 3.15(a) without any noise-cancellation and -reduction techniques, and 2) the proposed structure but without M_4, i.e. without the noise-reduction technique. In this comparison, the LNTA with and without M_4 consumes 4.5 mW with the same-size transistors. The size of transistor in the CG structure is the same as the size of CG transistor in the proposed LNTA and also its power consumption is exactly like the power consumption of the first stage in the proposed structure, which is about 1.5 mW.

As revealed in Fig. 2.9, the CG structure (top row bars) suffers from high noise. The channel thermal noise of the main transistor, M_1, is 41% of the total noise factor. By canceling its noise, the next highest contributor is M_2. The second row (CG & NC) shows that the thermal noise contribution of the main transistor, M_1, is reduced to 5%, whereas the thermal noise of the cancellation transistor, M_2, is added with a contribution of almost 27%. By using both the noise-reduction (NR) and noise-cancellation (NC) techniques (bottom row bars in Fig. 2.9), the thermal noise contribution of M_2 is decreased to 6%, thus improving the system noise performance. The thermal noise of R_{D1} is now dominant. According to the second term of (2.19), to reduce the noise effect of R_{D1}, its value should be increased. However, as mentioned before, the value of R_{D1} is limited by the supply voltage of first stage

which should be at a certain level in order to provide the input matching. Therefore, to further improve the noise performance, a g_m-boosting technique by means of M_0 is introduced. This way, the amount of current of the first stage decreases as well as the voltage drop on M_1. Consequently, the value of R_{D1} can be increased, leading to the decrease of NF. The g_m-boosting stage of M_0 boosts the g_{m1} of input stage, $G_{m1} = (1 + g_{m0}R_{D0})g_{m1}$, so the input matching can be provided with less current.

2.3.4 Linearity and Stability

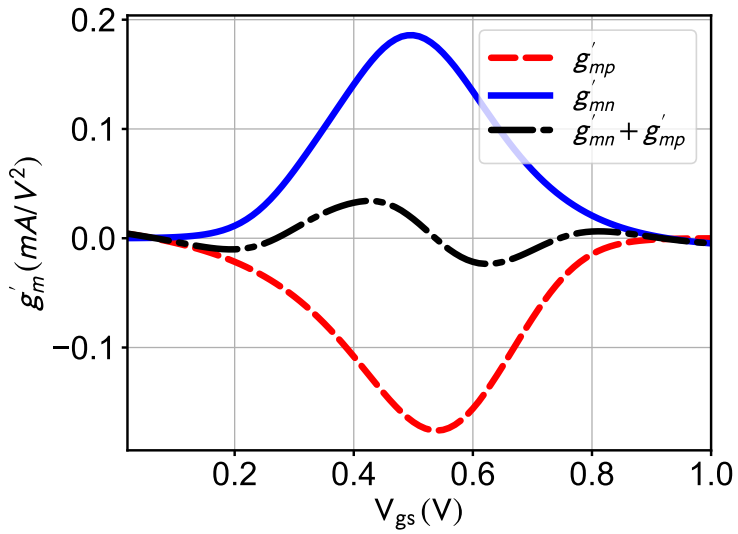


Figure 2.10: Second-order nonlinear components of g_m of pMOS and nMOS transistors.

Since the nonlinearity of a CS configured transistor is worse than that of the CG, the pMOS-nMOS structure placed at the output stage turns out to also improve the 2nd and 3rd-order nonlinearities. By using a power series, the total output current of the pMOS and nMOS transistors in the complementary connection is equal to $i_{ds_{tot}} = i_{ds_P} + i_{ds_N} = (g_{mN} + g_{mP})(v_g - v_s) + (g'_{mN} - g'_{mP})(v_g - v_s)^2 + (g''_{mN} + g''_{mP})(v_g - v_s)^3$, where g_m, g'_m, and g''_m are the first-, second- and third-order derivatives of the transistor's composite (large-signal) drain-source current, i_{ds}, with respect to its composite gate-source voltage, v_{gs}. Since the ac input signal for the pMOS and nMOS transistors is out of phase, the total transconductance increases while the total second nonlinear term, $g'_{mN} - g'_{mP}$, decreases [58]. Figure 2.10 shows that by applying the noise-reduction technique, the pMOS and nMOS transistors, M_2 and M_4, in fact are like a complementary circuit in the output stage which causes the 2nd-order

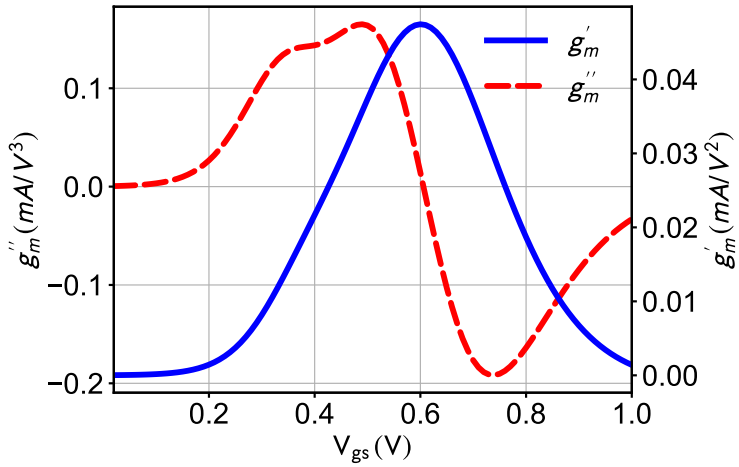


Figure 2.11: Second and third-order derivatives of the drain-source DC current, i_{ds}, with respect to V_{gs} of M_1.

nonlinear components, g'_{mP} and g'_{mN}, to neutralize each other within the range of the bias voltage. As a result, the 2nd-order nonlinear term is attenuated and since the 2nd-order nonlinear current can be mixed with the input by the feedback path through c_{gd} [58], both IIP2 and IIP3 are significantly improved. However, in this design, the PMOS-NMOS pair is not considered to be biased at the exact point where $g'_{mn} + g'_{mp} = 0$. The measured linearity variation due to different voltage biases of the PMOS-NMOS pair is less than 2 dB. It is worth mentioning that the linearity performance deteriorates a bit (<2 dB) by adding M_4 due to lowering of the available voltage swing in the output stage.

Consequently, to improve the linearity of the CG transistor, it is biased in a “sweet spot". According to Fig. 2.11, at the right bias voltage at which the 3rd-order nonlinear component of the CG transistor, g''_m, is equal to zero, the IIP3 of the CG structure can be improved. It is worth mentioning that by modeling the circuit’s non-linearity via Volterra series, it can be shown that the parasitic capacitance can also effect the second/third-order nonlinearity cancellation based on the “sweet spot". Although the sweet spot could be a bit shifted with frequency, it will be demonstrated in Section 2.4 that the variation of measured IIP3 is within 1 dB across the entire bandwidth. The most important drawback of the sweet-spot technique is its sensitivity to the process corners [66], which might require process calibration. Another option could be a constant-g_m biasing circuit. Once the sweet spot has been calibrated for the process, the LNA is quite insensitive to temperature and voltage variations. The reason is that M_1, located in the first stage, is mainly used for input matching, so its effective gain

is small, and thus its linearity contribution is not dominant and the signal provided to the second stage is still small. In other words, it is biased mainly to provide the required g_m for the input matching.

To examine the stability of the LNTA with an arbitrary source and load impedances, the Stern stability factor defined in (2.20) is often utilized [67]:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{2.20}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ and S_{11}, S_{22}, S_{21} and S_{12} are the input return loss, output return loss, forward gain and reverse gain, respectively. If $K > 1$ and $\Delta < 1$, then the circuit is unconditionally stable [67]. According to (2.20), the stability of the circuit is improved by maximizing the reverse isolation.

2.4 Measurement Results

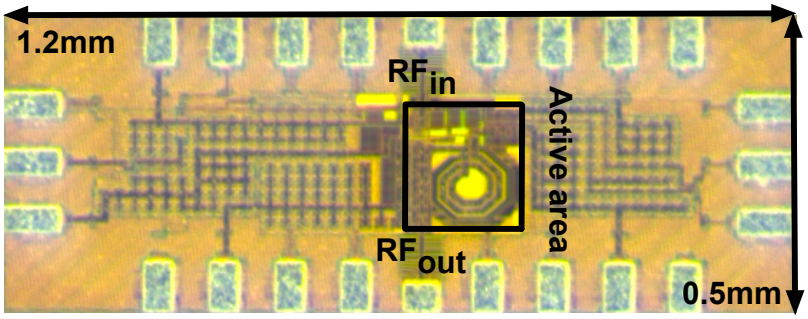


Figure 2.12: Microchip photograph.

The proposed wideband LNTA, whose chip micrograph is shown in Fig. 2.12, is fabricated in TSMC 28-nm bulk LP CMOS. Although this amplifier is specifically designed to drive a mainly capacitive load of integrated mixers as a high-impedance transconductor (thus, LNTA), it is also capable of driving heavy external resistive loads. Hence, it can also function as an LNA with 50 Ω input and output ports. To avoid adding an extra test buffer for driving the output port, which would need to be separately characterized, all the performance and power consumption measurements are with the external load of 50 Ω. By carefully sizing the transistors and using the noise-cancellation and -reduction techniques (with current

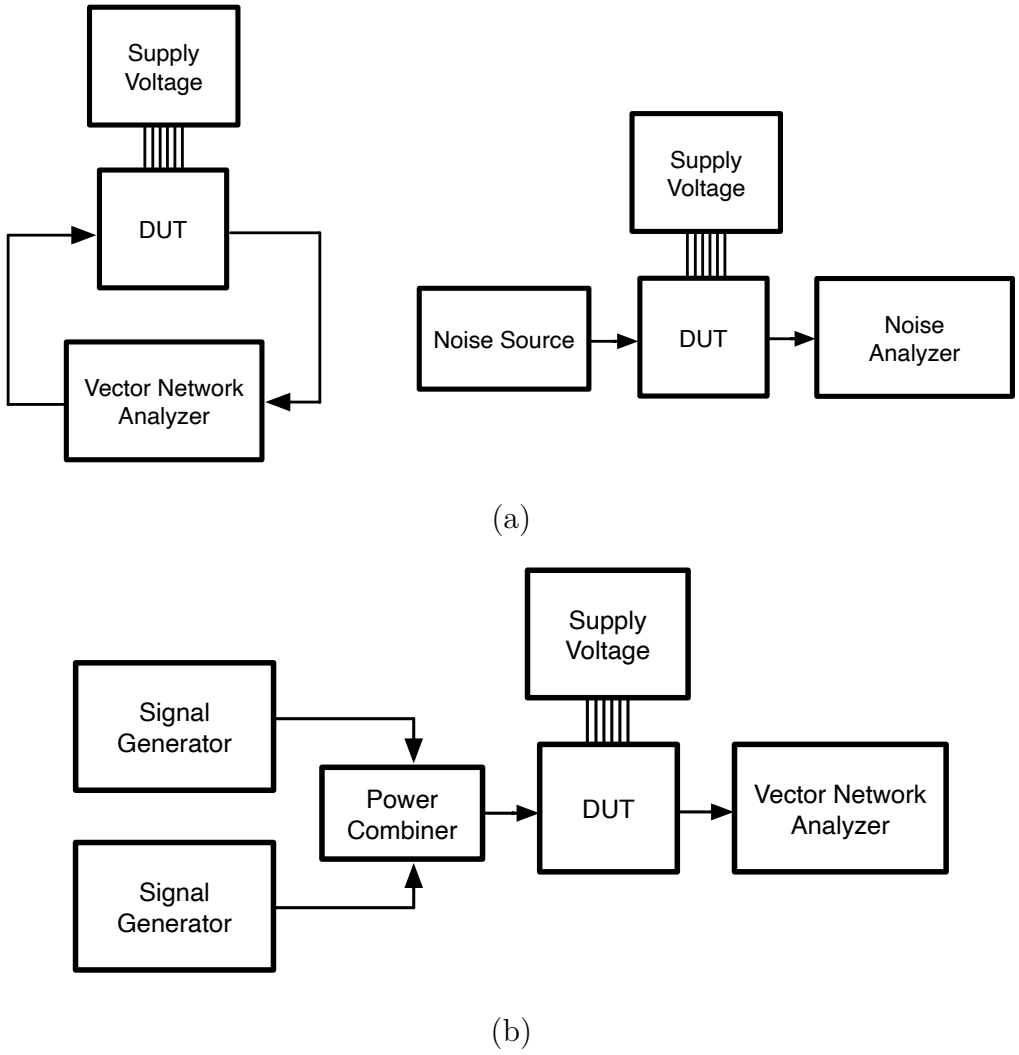


Figure 2.13: Measurement set-up: (a) S-parameter and noise; and (c) linearity.

reuse), this amplifier operates at a 1 V power supply with a power dissipation of 4.5 mW, while achieving remarkably high and flat small-signal gain and a very low noise figure in the whole wide bandwidth. The S-parameter, noise and linearity measurement set-up is shown in Fig. 2.13 and the results are discussed in the following paragraphs.

Measured S-parameters of the LNTA are shown in Fig. 2.14, which illustrates the best input return loss around 2.7 GHz (i.e. the input impedance is matched at this frequency). Although the input return loss gets worse away from this point, the wideband input matching feature is well controlled as $S_{11} < -10$ dB in the whole bandwidth. The measurement results are well matched with the simulations. Figure 2.15 shows the power gain which varies between 12–15.2 dB in the range of 20 MHz to 4.5 GHz. By adding transistor M_4, the

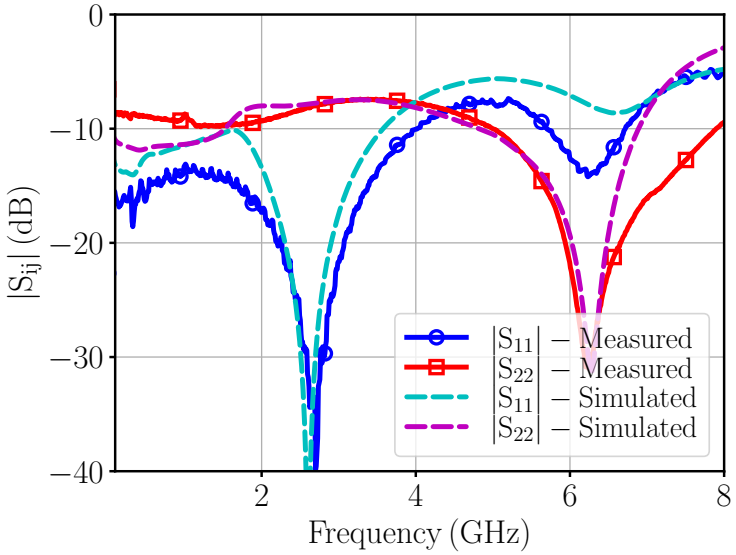


Figure 2.14: Measured and simulated input/output return loss.

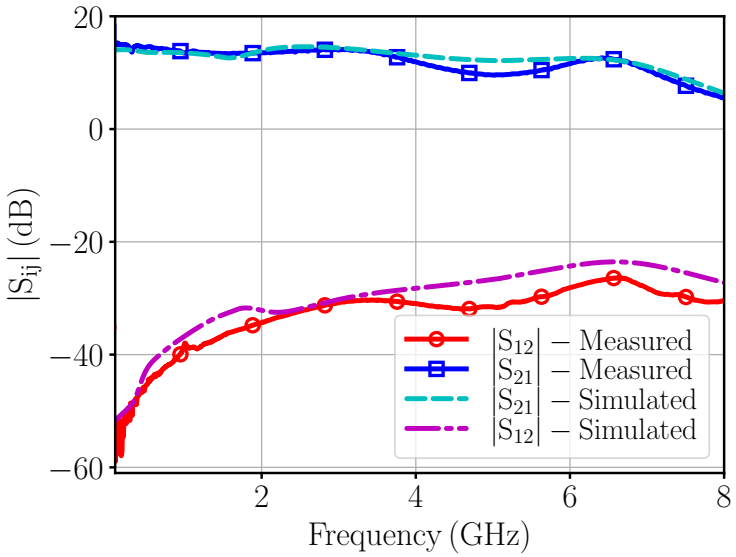


Figure 2.15: Measured and simulated gain and isolation.

second-stage transconductance in the presented LNA increases, resulting in more power gain, which is also expected from (2.12). Since the drains of three transistors, M_2, M_3, M_4, are connected to the output node, the total parasitic capacitance at this node increases. Hence, the -3-dB bandwidth of the LNTA is partially decreased. However, L_1 helps to dampen the parasitic capacitance at the output node and compensate for the reduction in bandwidth. Unfortunately, the measurement results of the bandwidth fall short mainly because of the larger wire-bonding inductance and parasitic capacitance of the pad and PCB traces affecting

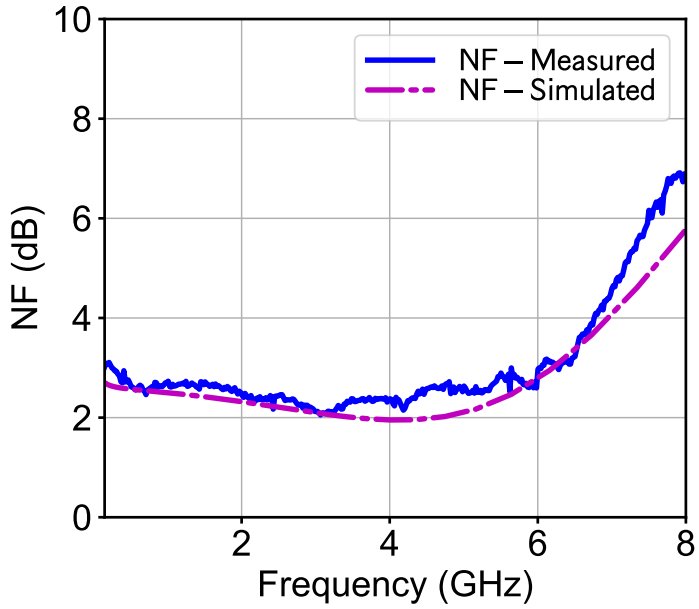


Figure 2.16: Measured and simulated NF.

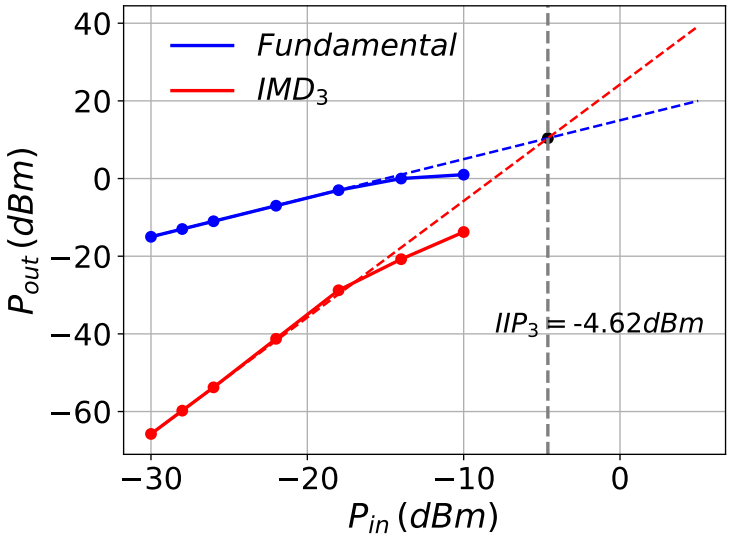


Figure 2.17: Measured IIP3 at maximum gain.

the *dominant* pole at the external output port. It is worth mentioning that this issue is irrelevant in integrated receivers or if the LNA is followed by an integrated mixer on the same die.

The measured NF of the LNTA is superimposed on the simulated NF in Fig. 2.16. It varies from 2.09 dB to 3.2 dB in the 4.4 GHz bandwidth. A two-tone RF signal at 500 MHz, 2 GHz and 4 GHz (i.e. at the beginning, middle and end of the band, respectively) is used to

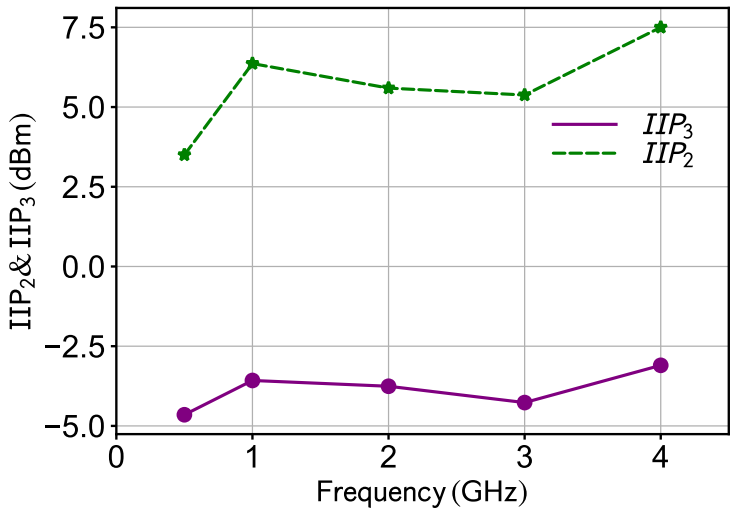


Figure 2.18: Measured IIP3 and IIP2 versus frequency.

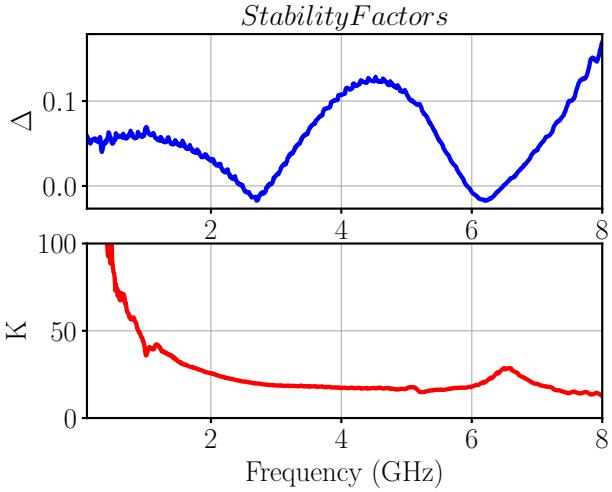


Figure 2.19: Measured stability factors K and Δ.

measure the wideband linearity performance. In order to examine the flatness of linearity, various two-tone spacings of 2.5, 10, 50, and 100 MHz are applied but, as expected, exhibit no difference in performance. As shown in Fig. 2.17, the measured IIP3 at 500 MHz with 10 MHz spacing, where maximum gain is achieved, is −4.63 dBm, which is the minimum IIP3 in the entire bandwidth. Figure 2.18 shows the measured IIP2 and IIP3 versus frequency. Note that in integrated designs there is always a dc-blocking capacitor between the LNA and a passive mixer, so the dc will be blocked and low-frequency IM2 products will be heavily attenuated (i.e. if two blocker signals are close to each other). Without the 50-Ω load, the simulations show the linearity of −8.7 dBm at the gain of 35.2 dB.

Table 2.1: Summary and comparison with state-of-the-art wideband LNAs.

	CMOS tech. [nm]	BW [GHz]	S_{11} [dB]	S_{21} [dB]	IIP3 [dBm]	NF [dB]	VDD [V]	Power [mW]	Active area [mm^2]	Noise cancel. used?	Can drive extern. 50 Ω?	FoM_1 [-]	FoM_2 [-]	FoM_3 [-]
This work	**28**	**0.02∼4.5**	**≤-10**	**15.2**	**-4.62∼-3.53**	**2.09∼3.2**[#]	**1**	**4.5**	**0.03**	**Yes**	**Yes**	**7.76**	**327**	**172.6**
[68] TCASI'20	65	0.05∼1.3	≤-10	27.5	-4∼-1	2.3∼3	1	5.7	0.046	Yes	No[**]	6.18	123.7	6.95
[69] TMTT'20	65	1∼20	≤-10	12.8	1∼5.8	3.3∼5.3	1.6	20.3	0.096	Yes	No[**]	2.4	2.4	5.28
[70] TCASI'19	65	0.05∼1	≤-10	30	-10∼-2.5	2.3∼3.3	2.2	19.8	0.0448	Yes	No[**]	1.6	33.51	26.6
[71] TCASII'19	65	0.4∼2.2	–	16.4	-5	2∼2.5	1.2	29	0.16	Yes	Yes	0.6	1.5	0.47
[72] TMTT'19	65	0.3∼4.4	–	26.7	-14.2	3∼4.4	1	13.7	0.009	No	No[**]	4.8	16	0.6
[73] TCASII'19	65	0.5∼7	–	16.8	-4.5	2.87∼3.77	1.2	11.3	0.044	Yes	No[**]	3.5	7	2.48
[74] TCASI'18	65	0.2∼2.7	<-5	21.2	-2	3∼3.5	1.2	0.96	0.05	Yes	No[**]	26.85	134.2	84.7
[75] TCASII'18	180	2∼5	–	13	-9.5	6∼8	1.8	1.8	0.72	Yes	No[**]	1.85	0.93	0.1
[76] JSSC'17	180	0.1∼2	–	17.5	10.6	2.9∼3.5	2.2	21.3	0.63	Yes	Yes[*]	0.6	6.14	70.5
[77] JSSC'2016	130	0.6∼4.2	<-10	14	-10	4∼9	0.5	0.25	0.39	No	No[**]	20.8	34.7	3.46
[78] TMTT'16	130	0.1∼2.2	–	12.3	-11.5∼-9.5	4.9∼6	1	0.4	0.0052	Yes	No[**]	8.6	86.2	9.68
[79] TCASI'2014	90	3.5∼9.25	≤-8	15	-16.3∼-12	2.4	0.8	9.6	0.56	No	–	4.5	1.3	0.0823
[80] MWL'14	180	0.02∼1.4	≤-10	16.4	-13.3∼-9	3∼4.7	1.8	12.8	0.04	No	No[***]	0.5	24.96	3.1
[81] JSSC'2013	65	0.1∼10	≤-11	24	-15∼-12	2.59∼4.92	1.2	8.64	0.012	No	–	15.29	152.9	9.65
[82] TCASI'2012	65	0.1∼5.1	–	10.7	∼6	2.9∼5.4	1	6	0.03	Yes	–	1.75	17.52	69.7
[83] JSSC'12	130	0.1∼2.7	–	20	-12	4	1.2	1.32	0.007	No	No[***]	13	130.3	8.2

[*] Differential load is 100 Ω. [**] Uses addt'l on-chip measurement buffer. [***] Needs addt'l external measurement buffer.
measured over 100 MHz–6.5 GHz

Finally, to verify the stability, the Stern stability factor (2.20), K, with Δ are plotted in Fig. 2.19 based on the measured data. As evident, the LNA is stable over the whole bandwidth, as $K > 1$ and $\Delta < 1$.

To compare this LNTA with prior-art architectures and to emphasize the capabilities of reaching lower frequencies in this wideband design, the following figures-of-merit (FoM_2 and FoM_3) are defined based on the original FoM (termed here FoM_1) introduced in [51] and the results are summarized in Table 2.1.

$$\text{FoM}_1 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}]}{(F_{\text{av}} - 1) \times P_{\text{dc}}[\text{mW}]} \tag{2.21}$$

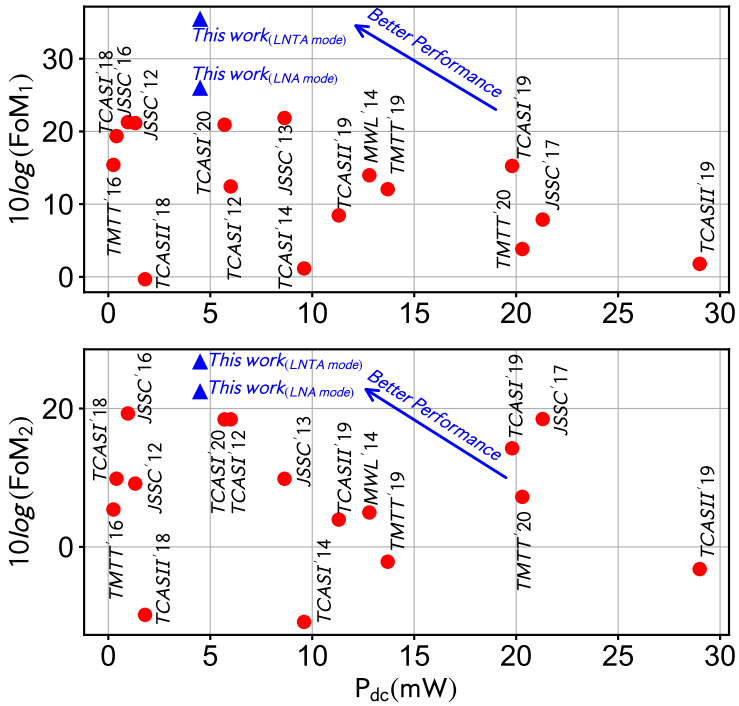


Figure 2.20: FoM landscape of high-performance LNAs. Note: $\mathrm{FoM}_{2,3}$ of our work in the LNTA mode (assuming a hypothetical test buffer) is based on a combination of measurements and simulations.

$$\mathrm{FoM}_2 = \frac{\mathrm{Gain_{av}[abs]} \times (f_H - f_L)[\mathrm{GHz}]}{(F_{\mathrm{av}} - 1) \times f_L[\mathrm{GHz}] \times P_{\mathrm{dc}}[\mathrm{mW}]} \tag{2.22}$$

$$\mathrm{FoM}_3 = \frac{\mathrm{Gain_{av}[abs]} \times (f_H - f_L)[\mathrm{GHz}] \times \mathrm{IIP3[mW]}}{(F_{\mathrm{av}} - 1) \times f_L[\mathrm{GHz}] \times P_{\mathrm{dc}}[\mathrm{mW}]} \tag{2.23}$$

where F_{av} is the average noise factor, $\mathrm{Gain_{av}}$ is the average power gain over the 3 dB frequency range f_L to f_H, and P_{dc} is the power consumption. Even without any extra output buffer to mitigate the loading effects of the external 50-Ω termination, the introduced LNTA provides a very low noise figure and has competitive power consumption for the ultra-wide bandwidth (4.48 GHz), which is achieved by virtue of using both noise-reduction and -cancellation techniques. Moreover, the circuit has a competitive linearity and quite high power gain versus the other leading designs. As shown in the comparative landscape in Fig. 2.20, this design achieves the best FoM among the recent state-of-the-art LNAs. Moreover, one of the main advantages of this architecture compared to prior reports is that it provides a high impedance at its output, which makes it suitable to drive an integrated passive mixer in a modern receiver. Despite the use of the additional on-chip (0.3 nH) inductor, the area still

remains very competitive.

2.5 Conclusion

A novel wideband noise-canceling low-noise transconductance amplifier (LNTA) is introduced in this chapter. It features two-fold noise-cancellation core transistor pairs: in addition to noise of the input matching transistor pair, noise of another transistor pair in the LNA core is also canceled. As showed through calculations, this LNTA could even achieve sub-1dB noise figure by increasing gain of LNA core and the total transconductance. This LNTA constructs the first stage of the proposed DT receiver in Chapter 4.

Chapter

3

Two-Fold Noise-Canceling LN(T)As in 28-nm CMOS

In this chapter, two wideband low-noise (transconductance) amplifier (LN(T)A) with a two-fold noise cancellation scheme are proposed. Finetuned for an advanced CMOS, the proposed LNA architecture uses a common-gate input branch to provide wideband input matching. It is followed by two stages of the common-source structure which cancel the noise and distortion of the first and second stages and relax the design restriction on the first noise-cancellation stage.

3.1 Introduction

to be able to amplify the received RF signal at any of the supported cellular frequency bands, a wideband (WB) noise-canceling (NC) low-noise amplifier (LNA) has become a subject of intensive research in both industry and academia [42,57,84,85]. Replacing multiple LNAs with a single LNA not only saves the silicon area, but also the printed circuit board (PCB) footprint of volume-constrained applications, and lowers the total bill of materials

(BOM). It further eliminates the antenna switch that would be otherwise necessary to route the received signal to the appropriate LNA, thus worsening the noise figure of the overall receiver. To provide wideband input matching, a common-gate (CG) topology of the LNA input stage is one of the appealing candidates [51]. The noise factor (NF) and input impedance of the CG structure depend inversely on its transconductance, g_m, which means that the CG structure will suffer from poor noise performance if it is designed to provide the wideband input matching. Moreover, high linearity is required for multi-mode RF front-ends to reduce cross-modulation/inter-modulation because of the increased need for co-existence of adjacent blockers or on-chip leakage from its own transmitter [86]. A popular method to enhance the noise performance of a CG amplifier is a noise cancellation (NC) technique which removes the channel thermal noise of the main antenna-interfacing transistor [42] [87] [88].

Recently, a new approach of combining noise cancellation and noise reduction techniques was introduced in [85]. The noise reduction technique there is based on a current-reuse approach, which was applied to the CG noise-cancellation stage to reduce the channel thermal noise of the following common-source (CS) cancellation stage. Moreover, it was designed as an low noise transconductance amplifier (LNTA) with an intention of providing high impedance for driving a passive mixer in an integrated receiver, while also being able to drive an external 50 Ω load. The noise reduction stage improves the noise performance of the CG noise-canceling structure. However, stacking up three transistors limits the available voltage swing in its output stage, thus leading to some degradation in the linearity performance.

Figure 3.1 shows a conventional WB-NC LNA [76, 89]. Common-gate transistor M_1 is used as an input stage so as to provide the wideband input matching to 50 Ω. The channel thermal noise of M_1 creates two out-of-phase voltage noise perturbations at nodes P and N, with the latter being smaller in amplitude. By amplifying the voltage noise N through M_2 and adding it to the voltage noise P amplified through M_3, the noise originated by the input transistor M_1 can be canceled at the output. Although this structure can effectively cancel the channel thermal noise of M_1 by means of the second stage (M_2 and M_3), the noise of the second stage is unaffected and can negatively impact the overall noise performance. This is reinforced by the fact that the input matching stage does not provide enough gain, so M_2 can now be the dominant noise source. As will be later shown in Section 3.2.3, to meet this noise-cancellation condition, the size of M_2 should be chosen large enough, but this will add more design restrictions, such as burning more power as well as increasing the amount of

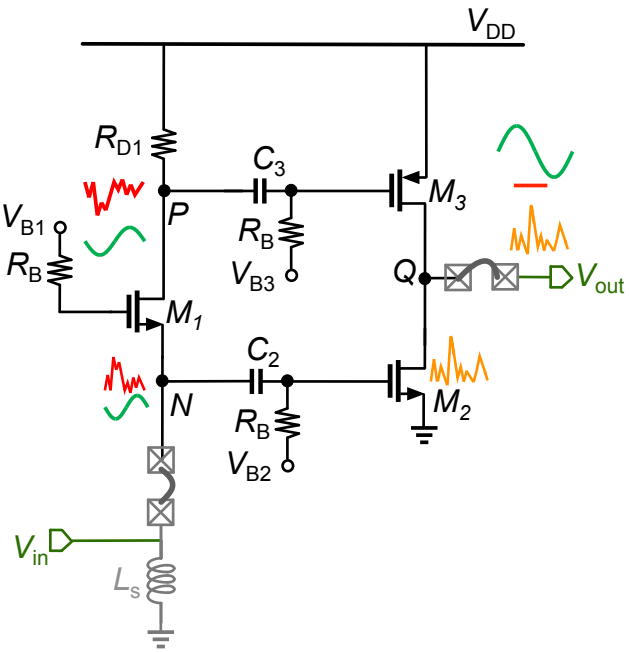


Figure 3.1: Conventional wideband noise-canceling LNA.

parasitic capacitance at the output node.

In this chapter, we propose a two-fold noise canceling LNA architecture which not only

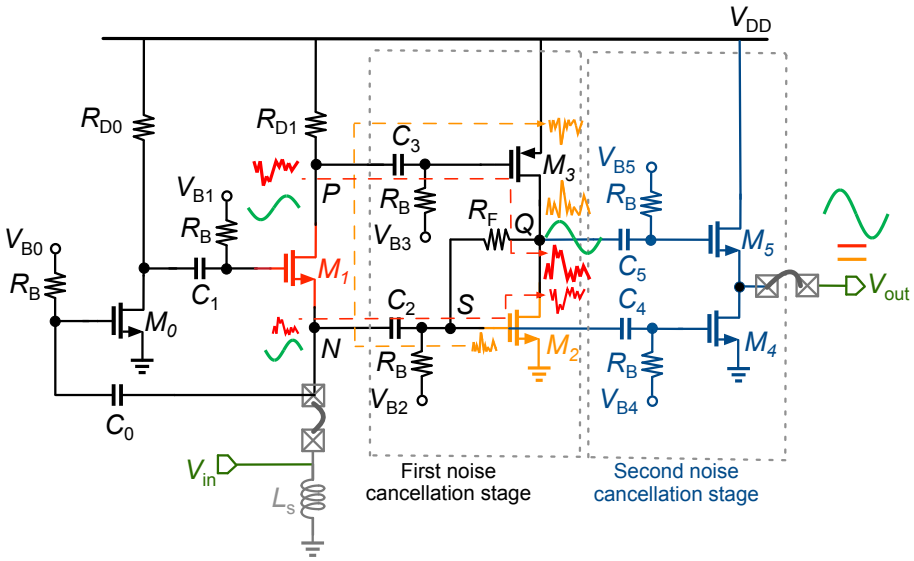


Figure 3.2: Proposed two-fold noise cancellation LNA.

cancels the noise of the input matching transistor, as done conventionally, but it also cancels

the noise of the noise-canceling transistor itself. Furthermore, the proposed complementary pMOS/nMOS structure can also cancel the transistors' distortions.

The chapter is organized as follows. The proposed wideband LNA is explained in Section 3.2, further providing an analysis of input matching, gain, noise, and linearity. In Section 3.2.5, the measurement and simulation results are presented. The conclusions are drawn in Section 3.4.

3.2 Two-Fold Noise Cancellation Wideband LNA

The proposed LNA architecture is shown in Fig. 3.2. The three stages realize the two-fold noise cancellation (NC) to further lower the noise figure (NF) while extending the bandwidth. M_1 is used as the CG structure for providing the broadband input matching. As in the prior art, the second stage is a NC complementary common-source (CS) topology consisting of M_2 and M_3, which is a pMOS/nMOS pair used to improve linearity. After applying the conventional noise-cancellation technique, the most important noise source is now due to the CS transistors in the second stage. To deal with this new challenge, the third stage, consisting of M_4 and M_5, is utilized to cancel the channel thermal noise of M_2 and M_3.

External input shunt inductor L_s (4310LC series SMD component) is used at the source of M_1 to provide a dc current path and to cancel the degrading effect of the parasitic capacitances of transistors M_0, M_1, M_2 and M_4. Since node Q is of high impedance, its voltage can vary substantially. Consequently, the negative feedback resistor, R_F, is used to prevent the variation of dc voltage at node Q. Since the Miller multiplication of R_F makes it much larger than the input and output impedances, its effect is ignored in all analysis.

3.2.1 Input Matching

As shown in Fig. 3.2, the CG transistor M_1 of the first stage realizes the wideband input matching. Its input impedance of $1/(g_{m1}+g_{mb1})$ is, to the first order, independent of frequency. To simplify the ensuing notations, we lump the body effect into the main transconductance g_m. Henceforth, G_{m1} stands for $(1+g_{m0}R_{D0})(g_{m1}+g_{mb1})$. The input impedance is calculated as:

$$Z_{in} = \frac{R_{Ls} + sL_s}{C_N L_s s^2 + (R_{Ls}C_N + G_{m1}L_s)s + G_{m1}R_{Ls} + 1} \tag{3.1}$$

where R_{Ls} is the series resistance of L_s. C_N denotes the total parasitic capacitance seen by the input node which is damped by L_s. The input matching condition, $S_{11} < -10\,\text{dB}$, will be achieved if $|Z_{in}|$ is around $50\,\Omega$. As indicated by (3.1), at mid frequencies, the input impedance is $\sim 1/G_{m1}$. At very low frequencies, the input matching can be effectively influenced by external L_s, so its value should be chosen high enough to ensure good matching there.

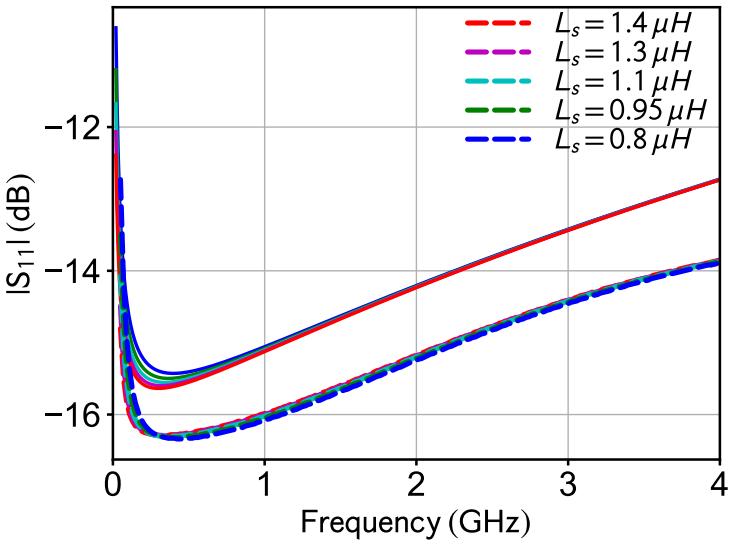


Figure 3.3: Effect of external L_s on the input matching: (dotted curves) full circuit SPICE simulations, (solid curves) plots of equation (3.1).

The off-chip inductor L_s is connected to the antenna pin, thus not consuming any extra pads on the chip. It is used for dc biasing but *not* used for matching; hence its value has to be merely high enough (e.g. $1.3\,\mu$H) as not to affect the input impedance (i.e. a lower value of the inductor could only affect the lower frequency limit of the bandwidth, f_L). In this case, equation (3.1) can be simplified to:

$$Z_{in} \approx \frac{1}{C_N s + G_{m1}} \tag{3.2}$$

According to (3.2), the input matching is mainly defined by M_0 and M_1. Therefore, if L_s changes, for instance from $0.8\,\mu$H to $1.4\,\mu$H, there will be no tangible change on S_{11}. This has been confirmed in full-circuit SPICE simulations shown in Figure 3.3, which plots the input matching characteristic S_{11} for various values of L_S. For reference, plots based on (3.1) are also included. A zoomed-in version concentrating on lower frequencies is re-plotted in

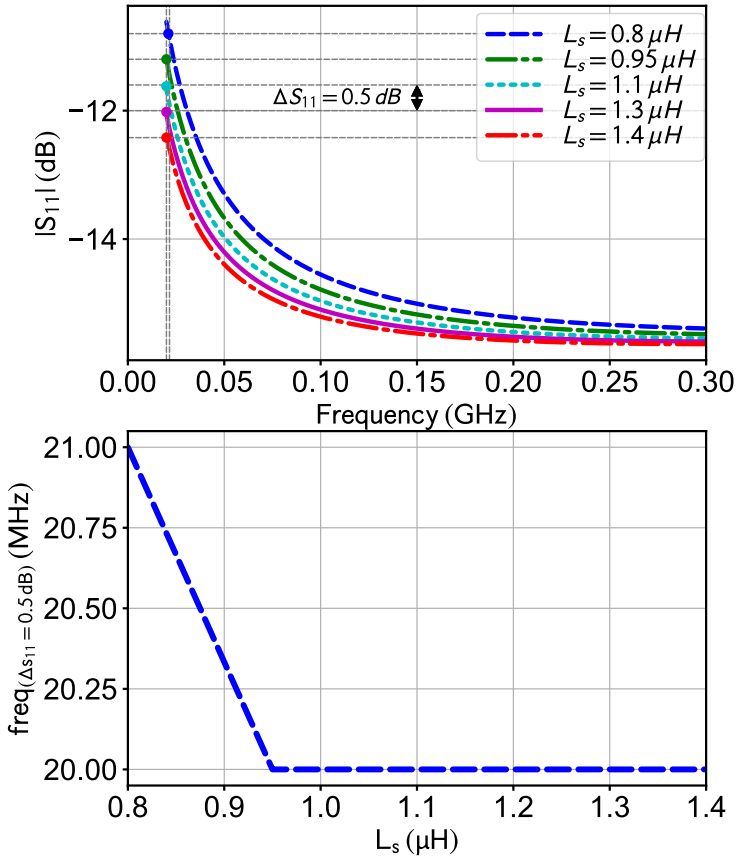


Figure 3.4: (top) Zoomed-in S_{11} of Fig. 3.3 showing the sensitivity of low-side frequency f_L at which S_{11} changes by 0.5 dB for different values of L_s with respect to $S_{11,(L_s=1.4\,^-\mathrm{H})}$=−12.45 dB at 20 MHz; (bottom) the sensitivity of the lower frequency of the input matching to L_s for $\Delta S_{11} = 0.5\,dB$.

Fig. 3.4 (top). Based on this data, Fig. 3.4 (bottom) visualizes at what frequency (y-axis) the magnitude of S_{11} worsens by 0.5 dB for a given value of L_s (x-axis).

3.2.2 Gain Analysis

Three stages are used in the proposed structure, so a significant gain is expected. The second stage is the most effective in providing the gain and so it consumes the most current. Since the first stage should ensure the input matching condition, it draws less current. Therefore, its voltage gain cannot be very high. In addition, the third stage acts as an output buffer and so its gain cannot be substantially increased.

The equivalent small-signal impedance seen from the drain of M_1 toward the ground is

termed Z_P and is equal to

$$Z_P = R_{D1}||\Big[r_{ds1} + \frac{1}{sC_N}||sL_s(1 + G_{m1}r_{ds1})\Big]\,||\frac{1}{sC_P}, \tag{3.3}$$

where C_P is the total parasitic capacitance to ground at node P. Z_Q is equal to $r_{ds2}||r_{ds3}||1/sC_Q$ where C_Q is the total parasitic capacitance at node Q. Z_{out} is defined as the output impedance, which is calculated as $r_{ds4}||r_{ds5}||1/g_{m5}||1/sC_{out}$, where C_{out} is the output parasitic capacitance. By considering the input matching condition, $1/G_{m1} = R_s$, the voltage gain of the proposed LNA is calculated as:

$$|A_v| \cong \frac{1}{2}[(G_{m1}g_{m3}|Z_P| + g_{m2})Z_Q g_{m5} + g_{m4})]|Z_{out}| \tag{3.4}$$

The voltage gain of the proposed LNA, A'_v, without considering the third stage, is equal to: $A'_v = \beta Z_Q$, in which β is equal to $(1/2)[g_{m2} + G_{m1}g_{m3}Z_P]$. As stated by the transfer function of Z_Q, the dominant pole causes Z_Q to have a large variation (Z_Q's roll-off happens at low frequencies), so its bandwidth reduces. When considering the third stage, the total voltage gain is equal to: $A_v = (g_{m5}\beta Z_Q + g_{m4}/2)|Z_{out}|$. The M_4's transconductance is added to $g_{m5}A'_v$ which creates a zero after the pole in order to neutralize its effect. Parasitic capacitance of the last stage defines the dominant pole as well as the roll-off frequency. Hence, by applying the proposed double noise-cancellation technique, although the gain of the proposed LNA increases, the bandwidth of the circuit slightly decreases due to more parasitic capacitances.

To validate the theoretical calculation derived in (3.4), it is superimposed on the full-circuit SPICE simulation in Fig. 3.5. It reveals good matching within the 3-dB bandwidth of 4 GHz. It is worth mentioning that although the g_m-boost transistor, M_0, slightly increases the parasitics at the input node, its small size does not affect the bandwidth substantially. Figure 3.6 shows the effect of M_0 size on the bandwidth: By increasing the size of M_0 from 10 to 20 μm, the upper cutoff frequency lowers by 210 MHz, from 3.9 GHz to 3.69 GHz.

3.2.3 Noise Analysis

As mentioned above, the proposed LNA exploits the two-fold noise cancellation to lower the NF. The first (conventional) technique is applied to the CG structure. The second (new) technique is used for the CS transistors in the second stage.

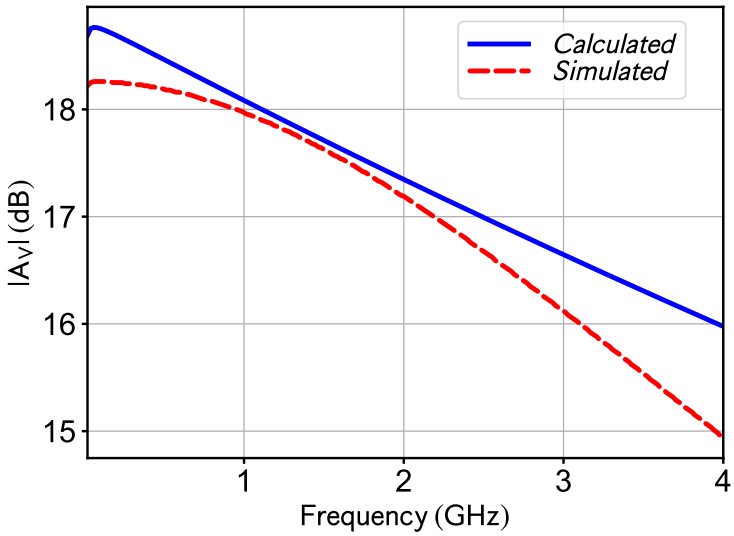


Figure 3.5: Simulated and theoretically derived gain A_v.

3.2.3.1 First noise cancellation for CG transistors

As mentioned, to compensate for the high NF of the CG structure, the noise cancellation technique is applied to cancel the thermal noise of the input transistors (see Fig. 3.1). The two noise voltages generated due to the thermal current noise of M_1 are calculated as $\overline{V}_{nN}^2 = Z_N^2 \cdot \overline{I}_{n,M1}^2$ and $\overline{V}_{nP}^2 = -Z_P^2 \cdot \overline{I}_{n,M1}^2$. Thus, the current noise (I_{n2}) generated in the second stage must be canceled:

$$\overline{I}_{n2}^2 = \overline{V}_{nN}^2 g_{m2}^2 - \overline{V}_{nP}^2 g_{m3}^2 = 0 \tag{3.5}$$

$$\rightarrow \frac{g_{m2}}{g_{m3}} = \left|\frac{Z_P}{Z_N}\right| \approx \frac{R_{D1}}{R_s} \tag{3.6}$$

To reuse the current of M_2, M_3 is selected as a pMOS transistor. By applying the noise cancellation condition, the noise factor of the structure shown in Fig. 3.1 (i.e without yet applying the proposed third stage), $F_{(\text{fig1})}$, is equal to $F_{(\text{fig1})} \cong 1 + F_{M2} + F_{M3}$ where the noise factor terms are given by:

$$F_{M2} = \frac{4kTg_{m2}|Z_Q|^2}{4kTR_s{A'_v}^2}\frac{\gamma}{\alpha} = \frac{4g_{m2}}{R_s(|Z_P|G_{m1}g_{m3} + g_{m2})^2}\frac{\gamma}{\alpha}$$
$$\cong \frac{1}{R_s(g_{m2})}\frac{\gamma}{\alpha} \tag{3.7}$$

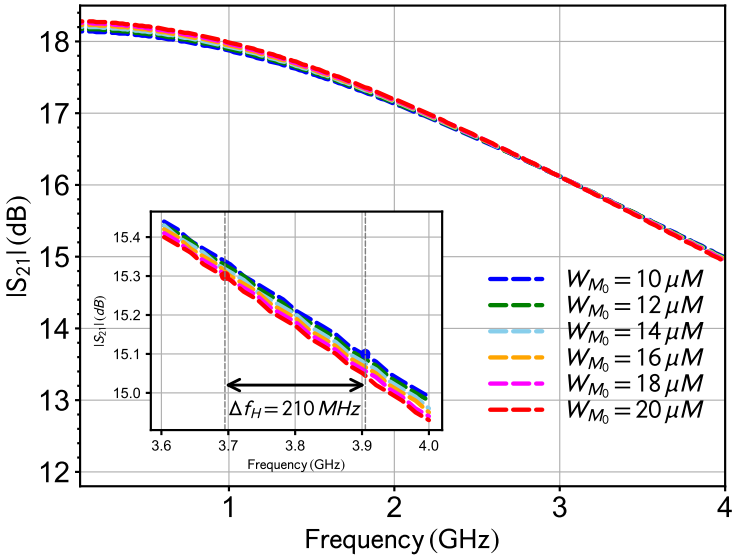


Figure 3.6: Simulated S_{21} for different values of M_0.

$$F_{M3} = \frac{4kTg_{m3}|Z_Q|^2}{4kTR_s{A'_v}^2}\frac{\gamma}{\alpha} = \frac{4g_{m3}}{R_s(|Z_P|G_{m1}g_{m3}+g_{m2})^2}\frac{\gamma}{\alpha}$$
$$\cong \frac{1}{|Z_P|^2 G_{m1}g_{m3}}\frac{\gamma}{\alpha}. \tag{3.8}$$

where A'_v is the voltage gain of the Fig. 3.1 LNA and given in Section 3.2.2, γ is the excess noise factor in short channel devices, and α is the ratio of the transconductance g_m to the zero-bias drain conductance g_{d0}. Moreover, Z_P and Z_Q were calculated in Section 3.2.2. Since the entire parasitic capacitance, C_N, at the input node is damped by L_s, the relationship $Z_{in} = Z_N = R_s = 1/G_{m1}$ is assumed. Thus, F_1 is approximately given by:

$$F_{(\text{fig1})} \cong 1 + \frac{\gamma}{\alpha R_s g_{m2}} + \frac{\gamma}{\alpha|Z_P|^2(G_{m1})g_{m3}} \tag{3.9}$$

As stated by (3.9), the noise performance gets better by canceling the noise effect of M_1, whereas the thermal noise of $M_{2,3}$—i.e. common source transistors—now substantially influences the noise factor. Moreover, according to (3.6), to fully cancel the noise of M_1, g_{m2} should be at least 8× larger than g_{m3} (i.e $R_{D1}/R_s \geq 8$), leading to a large size for transistor M_2, which increases the power and parasitic capacitance at the output node. The proposed second noise-cancellation technique is applied for both canceling out the noise of M_2 and relaxing the design constraints on the first cancellation stage (M_2).

3.2.3.2 Proposed second noise cancellation for CS transistors

By proposing the second noise-cancellation stage (i.e. M_4, M_5), the noise of both the first and second stages (i.e the input and first noise cancellation stages) are canceled twice through the proposed two-fold noise cancellation technique.

As shown in Fig. 3.2, firstly, the noise of M_1 reduces significantly at node Q through $M_{2,3}$; then it is canceled completely at the output node by passing through the second noise-cancellation stage. Hence, the noise-cancellation criterion of the input transistor is calculated as:

$$\frac{g_{m2}g_{m5}Z_Q + g_{m4}}{g_{m3}g_{m5}} = \left|\frac{Z_P}{Z_N}\right| \approx \frac{R_{D1}}{R_s} \tag{3.10}$$

The noise current of transistor M_2 flows through the feedback resistor, R_F, to node S (i.e AC-wise, it has the same voltage as at node N) and 'instantaneously' creates two noise voltages at nodes S and Q with the same phase but different amplitudes. On the other hand, the *signal* voltage at these nodes has opposite phases and different amplitudes due to the inverting amplifier. The difference between signal and noise polarities at nodes S and Q makes it possible to cancel the M_2 noise while adding the signal contributions constructively.

The thermal current noise of M_2 is canceled twice at node Q and at the output. Firstly, the noise voltage at node S, $\overline{V}_{nS}^2$, is amplified and inverted by M_1 and M_3 and added with the already generated noise voltage at node Q, $\overline{V}_{nQ}^2$. Hence, the noise of M_2 reduces significantly at node Q. Moreover, $\overline{V}_{nS}^2$ is amplified and inverted by M_4. Also, the noise voltage at node Q, $\overline{V}_{nQ}^2$, is passed across M_5 without any change in phase. Finally at the output, these two noise voltages with opposite phases are added. Therefore, the channel thermal noise of M_2 will be canceled completely at the output provided the following condition is satisfied:

$$\frac{g_{m5}g_{m3}G_{m1}Z_PZ_Q + g_{m4}}{g_{m4}} = \frac{(R_F + R_s)||Z_Q|}{R_s} \cong \frac{|Z_Q|}{R_s} \tag{3.11}$$

By canceling the thermal noise of transistors $M1$ and M_2, the most important noise sources in this two-fold noise cancellation scheme are the thermal noise of R_{D1} and the channel thermal noise of transistors M_4, and M_5. The noise factor of the proposed LNA is

equal to $F = 1 + F_{R_{D1}} + F_{M4} + F_{M5}$, where the $F_{R_{D1}}$ term is given by the following relation:

$$F_{R_{D1}} = \frac{4kTR_{D1}(g_{m3}g_{m5}|Z_Q Z_{out}|)^2(Z_{o1}/(Z_{o1}+R_{D1}))^2}{4kTR_sA_v^2} \cong \frac{4Z_Q^2}{G_{m1}R_{D1}(1+Z_Q)^2} \tag{3.12}$$

where Z_{o1} is the impedance seen from the drain of transistor M_1 and is equal to $Z_{o1} = [r_{ds1} + (R_s||1/sC_N||sL_s)(1+G_{m1}r_{ds1})]$. The F_{M4} and F_{M5} terms are derived as:

$$F_{M4} = \frac{4kTg_{m4}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{\gamma 4g_{m4}}{\alpha R_s[(|Z_P|G_{M1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} \tag{3.13}$$

$$F_{M5} = \frac{4kTg_{m5}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{\gamma 4g_{m5}}{\alpha R_s[(|Z_P|G_{m1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} \tag{3.14}$$

where $g_m r_{ds} \gg 1$ and $(R_F + R_s/2) \gg Z_Q$ is assumed.

By exploiting the two noise cancellation techniques, the noise factor is given by the following formula, in which the noise-cancellation and input-matching conditions are applied for simplification:

$$\begin{aligned} F \cong 1 &+ \frac{\gamma 4g_{m4}}{\alpha R_s[(|Z_P|G_{m1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} \\ &+ \frac{\gamma 4g_{m5}}{\alpha R_s[(|Z_P|G_{m1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} \\ &+ \frac{4Z_Q^2}{G_{m1}R_{D1}(1+Z_Q)^2} \end{aligned} \tag{3.15}$$

The channel thermal noise of the third stage is incorporated in (3.15). However, the effect of the third and fourth terms of (3.15)—i.e. the noise effect of the third stage referred to the input—is very small because it is divided by the total voltage gain of the LNA so that it has the least influence on the total noise factor. Therefore, it is expected that the presented structure achieves a very low noise figure by virtue of meeting the noise cancellation conditions. The main drawback of the proposed structure is the additional extra branch in the LNA signal path, which slightly increases the power consumption.

The efficacy of the proposed two-fold noise-cancellation technique of Fig. 3.2 is depicted by the NF circuit simulation plots in Fig. 3.7 with superimposed analytical plots to verify the derived noise equations. It is also compared with the conventional noise cancellation

presented in Fig. 3.1. By applying the proposed technique, the total NF improves by more than 1 dB compared to the conventional technique (e.g. Fig. 3.1). Moreover, this technique relaxes the design constraints on M_2, which helps to provide the noise cancellation criteria at a smaller transistor size.

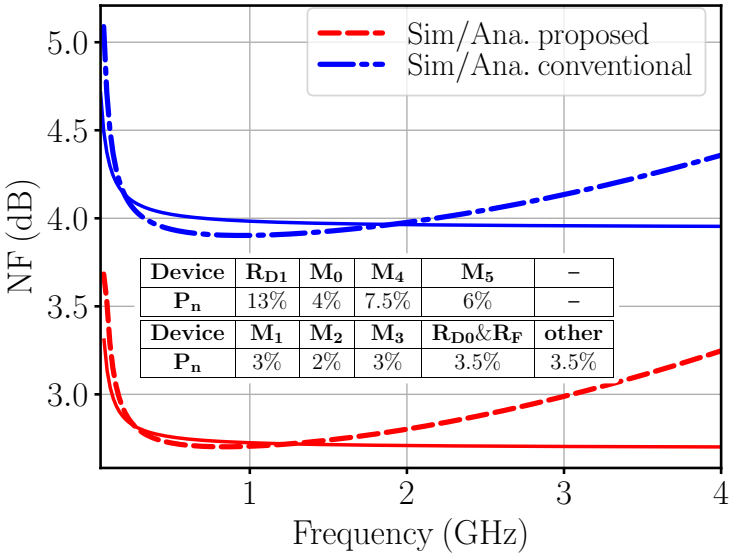


Figure 3.7: Comparison between the simulated (dotted line) and derived [solid line, formulas (3.9) and (3.15)] NF of the conventional and proposed LNA. The simulated contributions of each device of the proposed design is shown in inserted table.

3.2.4 Linearity

We have shown that by applying the two noise-cancellation techniques, the noise performance of the proposed LNA can be improved. Moreover, the nonlinearity of the CG transistor, including its second- and third-order products, can be modeled as a nonlinear current source between its drain and source, controlled by both V_{gs} and V_{ds}. This nonlinear current also produces two voltage drops at nodes N and P, which can be defined based on Volterra series and can be completely neutralized at the output if the non-linearity cancellation conditions are satisfied [88, 90]. This analysis is not provided here; however, intuitively, meeting the noise cancellation criteria helps to decrease the intrinsic distortion generated by M_1, including g_m and g_{ds} nonlinearities.

Moreover, by biasing transistor M_1 in a “sweet spot", its third nonlinearity coefficient (i.e. g_m'' which is the second derivative of g_m) will be zero, which improves the linearity

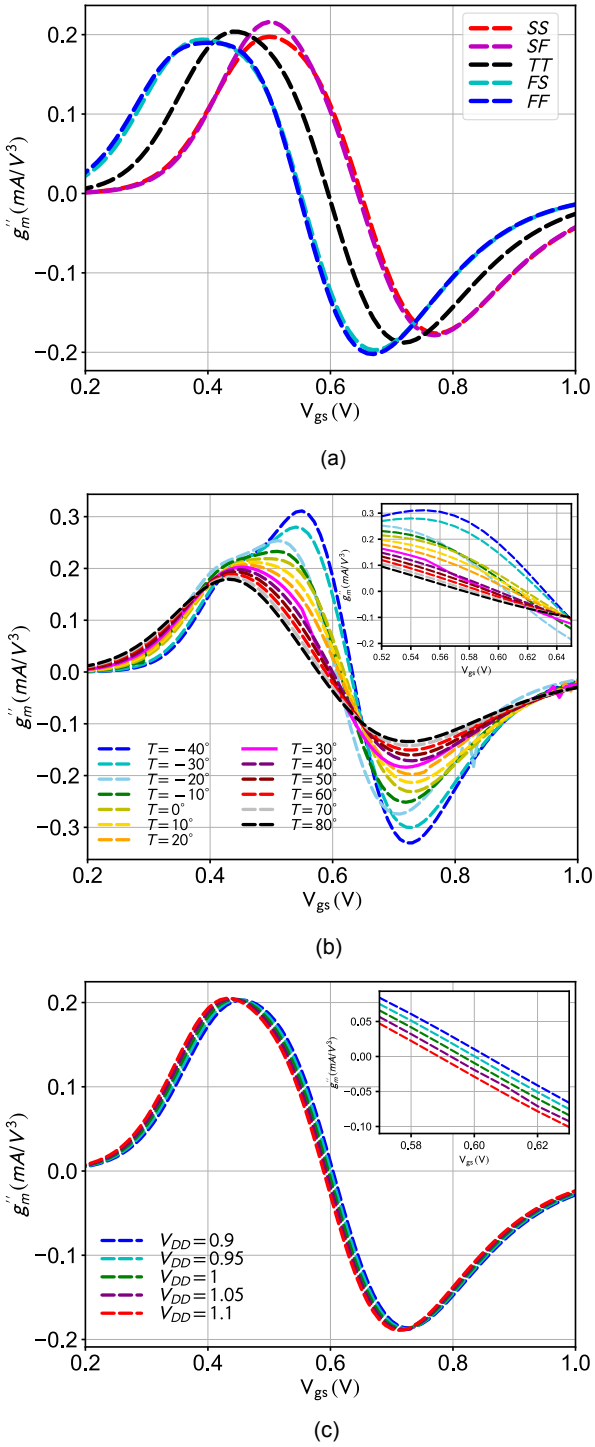


Figure 3.8: (a) Process, (b) temperature, (c) V_{DD} variations of third-order derivatives of the drain-source DC current, i_{ds}, with respect to V_{gs} of M_1.

performance of the proposed LNA. The “sweet spot" biasing means that the external supply voltage for the M_1 biasing is set to its optimal value to adjust for the process spread (see

Fig. 3.8) before the full suite of performance measurements, and is *not* adjusted afterwards. It is worth mentioning that the sweet-spot biasing only pertains to M_1 and is not relevant for the other transistors, hence its complexity is only 1-dimensional, thus manageable. More importantly, it is quite insensitive to the process and temperature variations, as verified by the simulations in Figs. 3.8(a) and (b), respectively. By changing the temperature, the second derivative of gm, g''_m, which has a direct effect on IIP3, shifts only slightly, 50 mV. Furthermore, since M_1 is mainly applied for the input matching, placed in the first stage, its effective gain is not high, so its linearity contribution is less dominant and the signal provided to the second stage is still small. In other words, it is biased mainly to provide the required g_m for the input matching. Moreover, Fig. 3.8(c) shows the variation of g''_m versus V_{B1} for different values of $V_{\rm DD}$, which also confirms the "sweet spot" of the first stage is less sensitive to the V_{DD} variations. As a result, the $V_{\rm DD}$ and temperature induced variations of g''_{m1} show that M_1 is not significantly sensitive, so there is no strong need to use the g_m-constant biasing here.

Finally, it is worth to mention that it is the $M_{2,3}$'s distortion that dominates the residual nonlinearity. It can also be modeled as a nonlinear current between their drain and source. By passing this current through R_F and R_s, two nonlinear voltages are created at nodes Q and S, which, by extending the Volterra series at these nodes, it can be shown that the second noise-cancellation technique can help to reduce the effects of nonlinearities of $M_{2,3}$ [58, 90]. Moreover, the second-order non-linearities of nMOS and pMOS transistors ($M_{2,3}$) neutralize each other's effects. As a result, the effective IM2 decreases significantly leading to a significant improvement in the IIP2

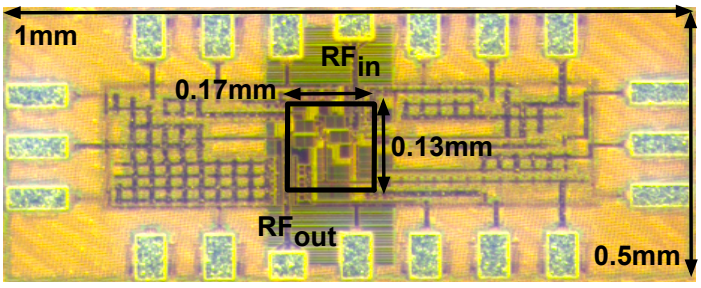


Figure 3.9: Microchip photograph.

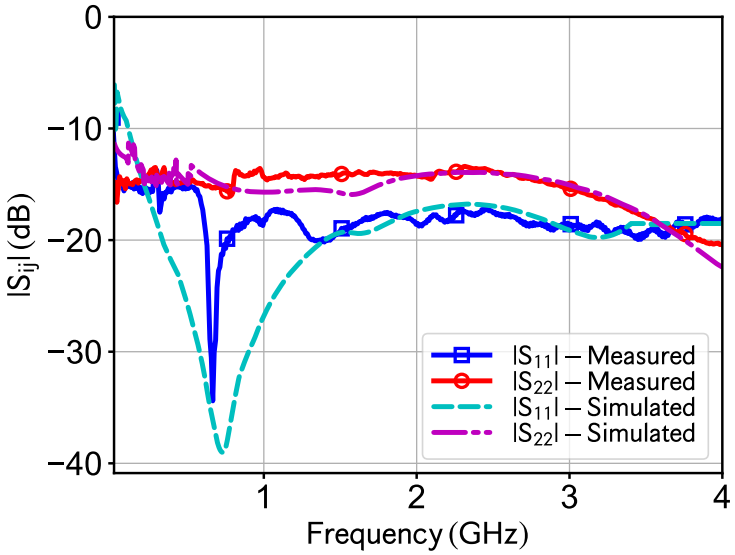


Figure 3.10: Measured and simulated input and output return loss.

3.2.5 Measurement Results

The proposed 0.02–2 GHz LNA is fabricated in TSMC 28-nm bulk LP CMOS, whose microchip photograph is shown in Fig. 3.9. Although the advanced technology node transistors provide better noise performance, their intrinsic gain, g_m/g_{ds}, reduces because the output conductance increases as a result of poorer short-channel control. Moreover, by going from older technology to an advanced one, V_{DD} is normally reduced by almost half while the MOS threshold voltage, V_{th}, does not change considerably. Hence, the available voltage headroom reduces dramatically, as does the gain. By means of the two-fold noise-cancellation technique, it is now possible to achieve a reasonably high and flat small-signal gain with a low NF performance. This LNA is able to reach 18.5 dB of maximum gain with NF of 2.5 dB, while dissipating only 4.1 mW.

Figure 3.10 shows the input and output return loss, S_{11} and S_{22}, versus frequency. The use of CG transistors in the input stage provides an acceptable S_{11}. The measured S_{11} is $\leq$-15 dB over the 0.02–4 GHz bandwidth. The simulated and measured transfer functions are plotted in Fig. 3.11. The 3 dB gain variation is between 18.5 down to 15.5 dB in the 0.02–2 GHz bandwidth. This architecture was designed to achieve the upper band at f_H = 4 GHz, as shown in Figs. 3.11 simulations. Unfortunately, the measurement result cannot explicitly show it because of the larger wire-bonding inductance and parasitic capacitance of the pad and traces on the printed circuit board (PCB). The wire-bonding inductance

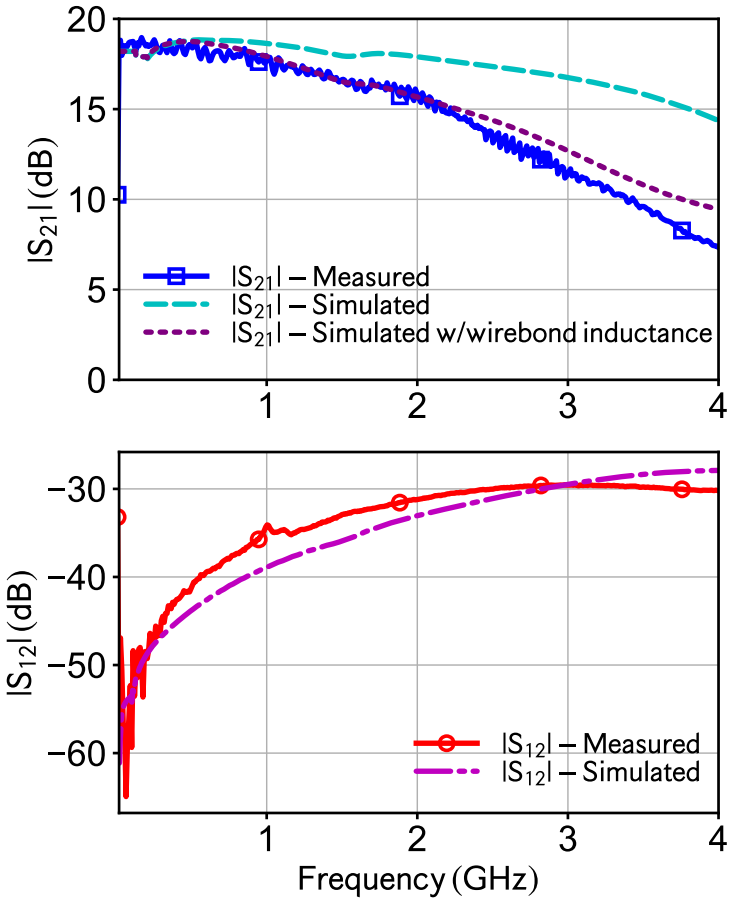


Figure 3.11: Measured and simulated: (top) gain S_{21} and (bottom) isolation S_{12}. The dotted curve is the simulated gain by considering 1 nH for the wire-bonding inductance and 700 fF for the parasitic PCB capacitances.

decreases the upper limit of the bandwidth to 2 GHz (wire-bonding is estimated between 1 nH and 1.5 nH, also confirmed by the dotted-line simulation plot with the inclusion of wirebonding inductor). Furthermore, the pad capacitance also causes the bandwidth limitation. It is worth mentioning that this issue is irrelevant in integrated receivers or if the LNA is followed by an integrated mixer on the same die.

Figure 3.12 plots the NF, which exhibits a particularly close agreement with the simulations below 2 GHz, where the gain is matched as well. The NF varies from 2.5 dB to 3.5 dB in the 2 GHz bandwidth, where it is below 3 dB (from 330 MHz to 2 GHz). As the gain drops above 2 GHz, the NF gets deteriorated. By carefully designing the PCB and choosing high Q-factor off-chip passive components, the NF could be further improved.

A two-tone RF signal at 100 MHz, 500 MHz, 1 GHz, 2 GHz, 3 GHz and 4 GHz (i.e. at the beginning, middle and end of the band) is used to measure the wideband linearity

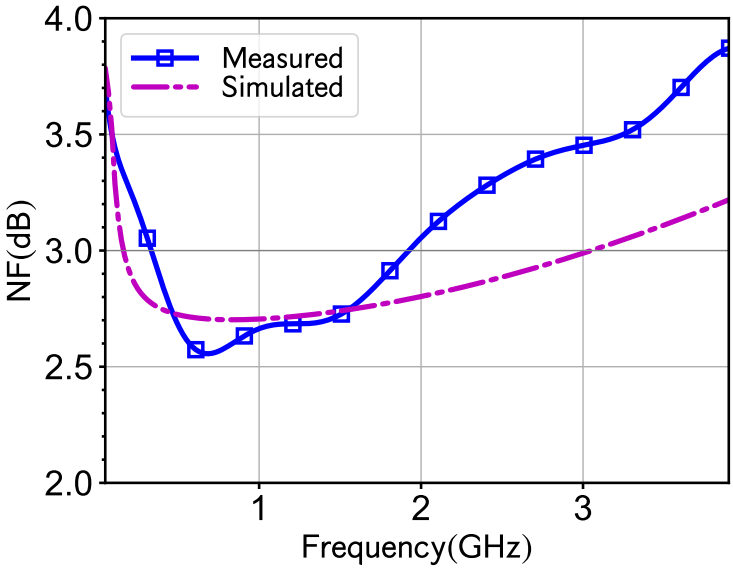


Figure 3.12: Measured and simulated NF.

performance. As shown in Fig. 3.13, the measured IIP3 at 500 MHz with 10 MHz spacing, where the maximum gain is reached, is +2.25 dBm. Figure 3.14 shows the measured IIP3 versus frequency, where +4.25 dBm is the maximum IIP3 in the entire bandwidth occurring at 1 GHz.

To compare the proposed LNA with recent state-of-the-art stand-alone wideband RF LNAs, and to emphasize the capability of reaching the lower frequencies in this wideband design, the following figures-of-merit (FoM) is introduced in [51] and [85] and the overall results are summarized in Table 2.1.

$$\mathrm{FoM}_1 = \frac{\mathrm{Gain_{av}[abs]} \times (f_H - f_L)[\mathrm{GHz}]}{(F_{\mathrm{av}} - 1) \times P_{\mathrm{dc}}[\mathrm{mW}]} \tag{3.16}$$

$$\mathrm{FoM}_2 = \frac{\mathrm{Gain_{av}[abs]} \times (f_H - f_L)[\mathrm{GHz}] \times \mathrm{IIP3[mW]}}{(F_{\mathrm{av}} - 1) \times P_{\mathrm{dc}}[\mathrm{mW}]} \tag{3.17}$$

$$\mathrm{FoM}_3 = \frac{\mathrm{Gain_{av}[abs]} \times (f_H - f_L)[\mathrm{GHz}] \times \mathrm{IIP3[mW]}}{(F_{\mathrm{av}} - 1) \times f_L[\mathrm{GHz}] \times P_{\mathrm{dc}}[\mathrm{mW}]} \tag{3.18}$$

where $\mathrm{Gain_{av}}$ is the average power gain, F_{av} is the average noise factor over the 3 dB frequency range f_L to f_H, and P_{dc} is the power consumption. This LNA achieves the best FoM (i.e FoM_3), features high power gain and high linearity and low noise figure, while drawing only 4.1 mA current from the 1 V supply. The proposed LNA reaches the record-low 3 dB

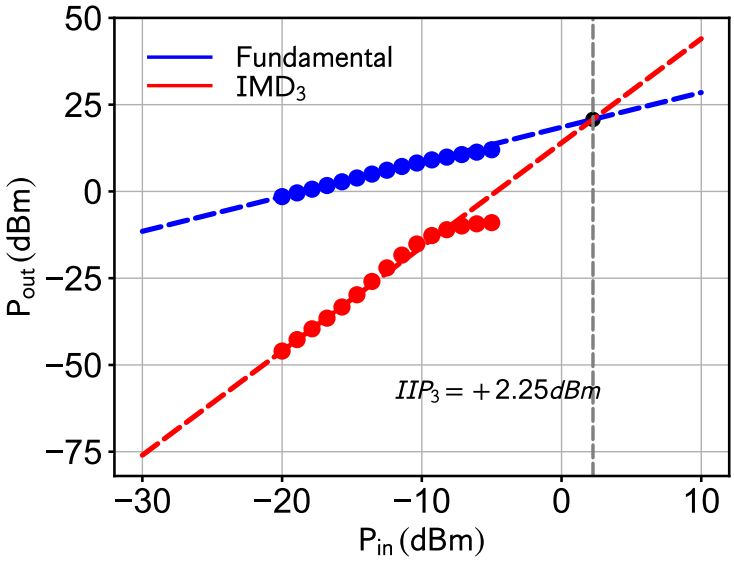


Figure 3.13: Measured IIP3 at maximum gain.

bandwidth cutoff frequency f_L of 20 MHz, which makes it suitable for certain applications, such as software defined radio (e.g. Aaronia SPECTRAN V6 or AD-FMCOMMS4-EBZ). It maintains high performance and low power consumption, especially compared with [80]. It can also directly drive the external 50 Ω load, while most other reports require additional buffers which do not count towards their final power consumption numbers. Although [74] achieves comparable gain with better power consumption, the acceptable wideband input matching cannot be provided in the whole reported bandwidth based on its S_{11} performance. Moreover, its noise and linearity performance are worse than in our structure. It also requires a higher supply of 1.2 V. Although [78] reaches quite high FoM due to its low power consumption, its gain, NF and IIP3 performance get compromised. Even though [68] provides high gain and slightly better NF, its linearity is worse, while consuming more power and occupying 2× the area. Moreover, [91] consumes lower dc power; however, its NF, gain and bandwidth performance are worse, and it needs a higher 1.2 V supply, while requiring an additional buffer to drive the external 50 Ω load. Finally, [83] consumes less dc power and provides a bit higher gain; however, its NF and linearity performance are worse even at a higher 1.2 V supply, and it requires an extra buffer to drive the external 50 Ω load. Moreover, it requires a couple of external high-quality current sources to directly bias its input stage.

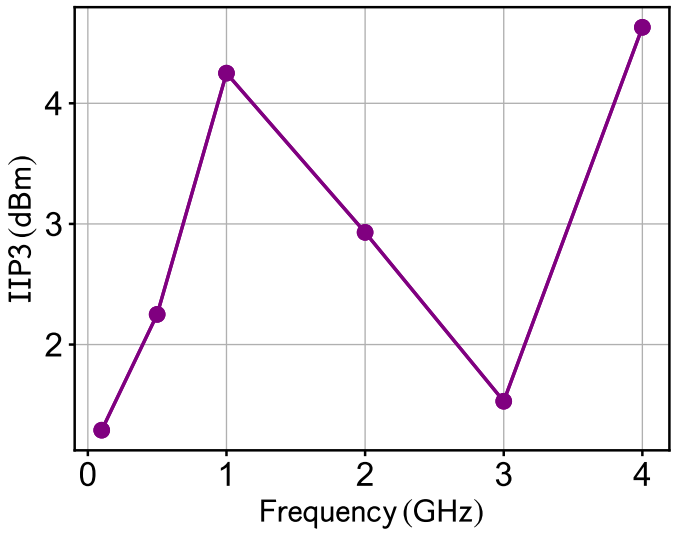


Figure 3.14: Measured IIP3 versus frequency.

3.3 Two-Fold Cross-Coupled Wideband LNTA

In this section another technique is introduced. It improves the noise performance of the CG structure while providing high gain. In the following sub-sections it will be shown in more detail how a two-fold cross-coupled LNTA can be designed.

3.3.1 Cross-Coupled Common-Gate LNA

As the first basic LNA structure, cross-coupled common-gate LNA [92] is shown in Fig. 3.15. To have input source impedance (R_S) matching in this structure, input transistors (M_1 and M_2) should have transconductance of:

$$g_{m1} = g_{m2} = \frac{1}{2R_s} \tag{3.19}$$

This is half the required gm for a common-gate LNA without the cross-coupling, which saves power consumption. To analyze noise of this structure, initially noise of M_2 (indicated in red in Fig. 3.15) is only considered in the right branch. First by writing KCL at V_1, we have:

$$\frac{V_1}{R_s} = (V_2 - V_1)g_{m1} \tag{3.20}$$

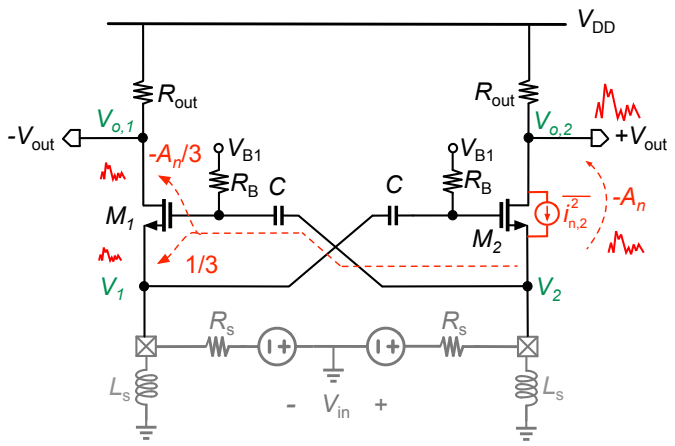


Figure 3.15: Cross-Coupled common-gate LNA [92] with reduced required input matching transconductance and partial noise input noise-cancellation at differential output.

Substituting Eq. (3.19) in Eq. (3.20) gives:

$$V_1 = \frac{1}{3}V_2 \tag{3.21}$$

Then, by writing KCL at V_2, we have:

$$\frac{V_1}{R_s} = (V_2 - V_1)g_1 + i_{n2} \tag{3.22}$$

where $\overline{i_{n2}^2}$ is a spectral density of M_2 noise current. Replacing Eq. (3.21) in Eq. (3.22) and considering the input matching condition, it is simplified to:

$$V_2 = \frac{3}{4}i_{n2}R_s \tag{3.23}$$

It could be easily shown that the M_2 noise appears the V_{o2} with A_n times V_1, where A_n is given by:

$$A_n = \frac{R_{out}}{R_s} \tag{3.24}$$

In addition to M_2 noise, R_{out} noise ($\overline{v}^2_{n,R_{out}}$) also goes to the output. Note that noise of the left branch is also the same amount. Moreover, all noise sources are uncorrelated. While

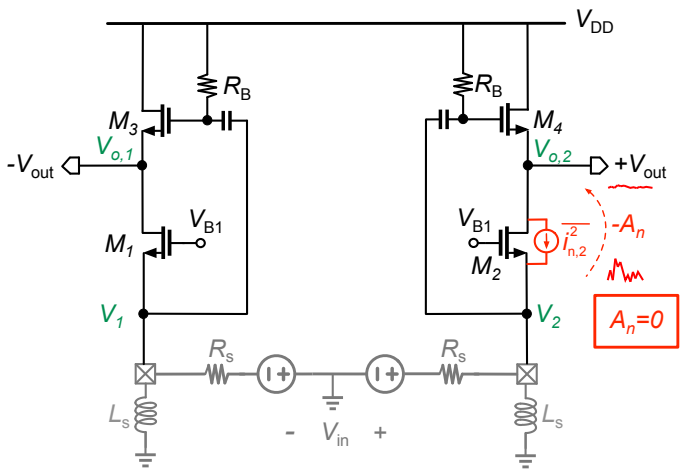


Figure 3.16: Common-gate-source-follower noise-cancelling LNA [93] with noise-cancellation of the input matching transistors.

the input is matched, signal gain from input to output is calculated:

$$A_v = \frac{V_{out,d}}{V_{in,d}} = \frac{V_{o,d}}{V_{a,d}} = g_{m1} \times 2R_s = \frac{R_{out}}{R_s} \tag{3.25}$$

Now, noise figure (NF) of the LNA can be found by referring the effect of different noise sources from the output $V_{o,diff}$ to the input $V_{a,diff}$, and normalizing to the noise of input source (R_s):

$$NF = 1 + \frac{\frac{2\times((1/2)i_{n2}R_{out})^2}{A_v^2} + \frac{2\times v_{n,R_{out}}^2}{A_v^2}}{2 \times (1/2)^2 \times v_{n,R_s}^2} = 1 + \frac{\frac{2\times(1/2)^2 4kT\gamma_a g_{m,a} \times (R_{out})^2}{(R_{out}/R_s)^2} + \frac{2\times 4kTR_{out}}{(R_{out}/R_S)^2}}{2 \times (1/2)^2 \times 4kTR_s} \tag{3.26}$$

The 2x multiply in the numerators and the denominator is to account for noise of both branches deferentially. Also, the 1/2 coefficient in the denominator is because of the gain of 1/2 from input source to LNA input made by input matching. M_2 noise, $\overline{i_{n2}^2}$, is considered $4kT\gamma g_m$, where k, T, and γ are Boltzmann constant, absolute temperature, and MOS noise excess factor, respectively. After simplification and considering input matching condition,Eq. 3.26 can be written as:

$$NF = 1 + \frac{\gamma_a}{2} + \frac{4}{R_{out}/R_s} \tag{3.27}$$

The second term is noise contribution of M_1 transistors that is reduced to half due to the cross-coupling and less required g_{m1} for input matching. Supposing $\gamma_1 \sim 1$ in nano-scale

CMOS and 20 dB voltage gain, NF of this LNA is limited to ≥ 2.8 dB.

3.3.2 Basic Common-Gate Noise-Cancelling Structure

The common-gate-source-follower noise-canceling LNA structure [93] shown in Fig. 3.16 is able to cancel noise of the input matching transistors. In this LNA, R_{out} is replaced with two transistors, M_3, that transfer signal and noise of the input nodes (V_1) to the outputs (V_3). Input signal goes to the output from two paths, through M_1 and M_3 that are added in-phase on V_3 node. However, M_1 noise reaches to the output from the two paths anti-phase, and therefore can be reduced or canceled out.
Input matching in this LNA is achieved by:

$$g_{m,a} = \frac{1}{R_s} \tag{3.28}$$

Substituting (3.27) in (3.28) gives: First, noise of M_2 is only considered in the right branch. By writing KCL at V_2, we have:

$$\frac{V_2}{R_S} = -V_2 g_{m2} + i_{n2} \tag{3.29}$$

Substituting (3.28) in (3.29) gives:

$$V_2 = -\frac{1}{2} R_s i_{n2} \tag{3.30}$$

Then, KCL at V_4 node gives:

$$i_{n2} - V_2 g_{m2} = (V_2 - V_4) g_{m4} \tag{3.31}$$

By replacing (3.28) in (3.30) gives:

$$V_2 = \frac{1}{2} i_{n2} (R_s - \frac{1}{g_{m4}}) \tag{3.32}$$

Here M_2 noise transfer ration (A_n) from V_4 to V_2 is found from (3.30) and (3.32):

$$A_n = -\frac{V_4}{V_2} = \frac{1}{g_{m4} R_s} - 1 \tag{3.33}$$

To have perfect noise cancellation of M_2, A_n should become zero. Hence we have:

$$A_n = 0 \Rightarrow g_{m4} = \frac{1}{R_s} \tag{3.34}$$

With this condition, the amount of M_2 noise current that directly goes to the output ($V_{o,2}$) is the same amount transferred from M_4, but with opposite direction. In this way, only M_4 noise is left in the right branch that it output noise voltage is trivially:

$$\overline{v_{n4}^2} = \frac{\overline{i_{n4}^2}}{g_{m4}^2} \tag{3.35}$$

Considering the input matching (3.28) condition, signal voltage gain from the two path is derived:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m,z}}{g_{m4}+1} = \frac{a}{g_{m4}R_s} + 1 \tag{3.36}$$

where, the first and second terms are through M_2 and M_4 paths, respectively. The signal gain (A_V) in (3.36) is different than M_2 noise ratio (A_n) in (3.33). Also accounting for M_2 noise-cancellation (3.34) condition, (3.26) is reduced to:

$$A_n = 0 \Rightarrow A_v = 2 \tag{3.37}$$

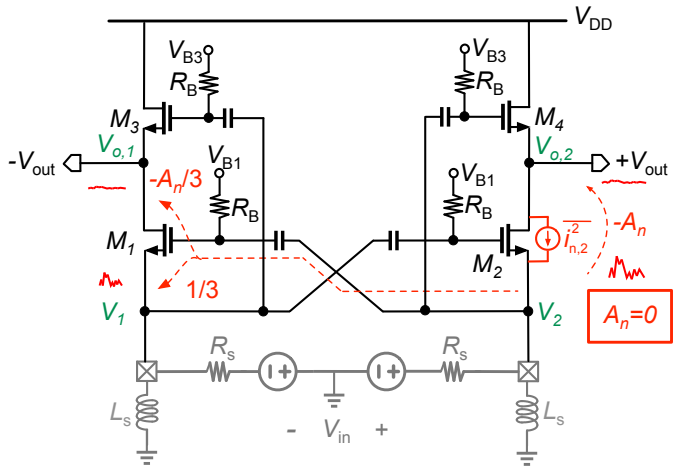


Figure 3.17: Common-gate-source-follower noise-cancelling LNA with input cross-coupling.

Therefore, the noise-cancellation condition forces a fixed voltage gain in this LNA. Noise

figure of this LNA is found by considering the only left noise source in (3.35):

$$NF = 1 + \frac{\frac{\overline{4i_{n4}^2}/g_{m4}^2}{A_v^2}}{v_{n,R_s}^2} = 1 + \frac{4kT\gamma_4}{4kTR_s g_{m4}} = 1 + \gamma_4 \tag{3.38}$$

Although noise of the input matching is eliminated compared to (3.27), M_4 noise still imposes a high NF. Supposing $\gamma_4 \approx 1$, NF of this LNA is limited to >3 dB while providing only 6 dB voltage gain.

3.3.3 Noise-Cancelling Structure with Input Cross-Coupling

The first step to reach to the proposed LNTA structure is combining the two cross-coupled common-gate LNA and the basic common-gate noise-cancelling structures (Fig. 3.17). In this structure, input matching condition is the same as (3.19), $g_{m1} = 1/(2R_s)$. Also similar to the cross-coupled common-gate LNA in Fig. 3.15, M_1 noise appears on the input nodes:

$$\begin{cases} V_2 = \frac{3}{4} i_{n2} R_s \\ V_1 = \frac{1}{3} V_2 \end{cases}$$

KCL at $V_{b,p}$ gives us:

$$i_{n2} + g_{m2}(V_1 - V_2) = (V_2 - V_{o,2}) g_{m4} \tag{3.39}$$

By substituting (3.39), M_2 noise on the output node is found:

$$V_{o,2} = \frac{3}{4} i_{n2} (R_s - \frac{1}{g_{m4}}) \tag{3.40}$$

Therefore, this structure has also the same noise ratio as in (3.33):

$$A_v = -\frac{V_{o,2}}{V_2} = \frac{1}{g_{m4} R_s} - 1 \tag{3.41}$$

Again here, $g_{m4} = 1/R_s$ leads to complete M_2 noise cancellation. Signal voltage gain is similarly derived the same as (3.36) that can be alternately written as:

$$A_v = -A_n + 2 \tag{3.42}$$

This LNA structure still has the noise figure of (3.38). However, it requires less power consumption to provide the input matching. In addition to the problem of a high NF limitation, this structure still does not have freedom to set voltage gain (A_V).

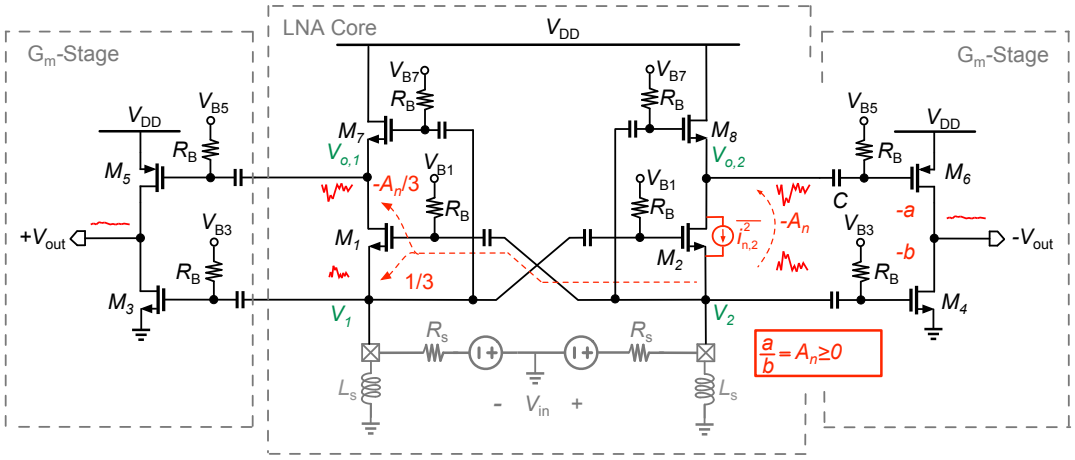


Figure 3.18: Noise-cancelling LNTA (proposed structure 1).Noise of the input matching transistors are cancelled out with an arbitrary gain of LNA core.

3.3.4 Adding Gm-Cell

As the final design goal is to have an LNTA, an inverter-based g_m-stage is added at the output of the LNA core of Fig. 3.18. However, instead of connecting both NMOS and PMOS to $V_{o,1}$ node, one is connected to $V_{o,1}$ and the other one to V_1 (see Fig. 3.18, the proposed LNTA 1). In this way, M_1 noise cancellation can be done for an arbitrary voltage gain (A_V) by exploiting an available degree-of-freedom in the g_m-stage, where signals from V_2 and $V_{o,2}$ to out- has a voltage-to-current gain of g_{m4} and g_{m6}, respectively. Then, instead of setting $g_{m8} = 1/R_s$ to cancel M_1 noise in the LNA core itself, a lower g_{m8} can be used. Consequently, A_V is increased that lowers input-referred noise of M_8 and the g_m-stage. To cancel M_2 noise at the output of g_m-stage we have:

$$g_{m4}V_2 + g_{m6}V_{o,2} = 0 \tag{3.43}$$

Substituting (3.41) into (3.43) gives:

$$g_{m4}V_2 + g_{m6}(-A_V V_2) = 0 \Rightarrow \frac{g_{m4}}{g_{m6}} \tag{3.44}$$

With this condition satisfied, noise of M_2 does not appear at output node. As calculated in (3.39), this noise appears on each corresponding node at the left side of LNA core with a gain of 1/3 Fig. 3.18. Consequently, in the same way it is also canceled at output.

Total gain of the LNTA from input to output is provided by two paths: through V_1 and V_2 nodes. Using (3.42) and (3.44), the total single-ended transconductance is derived:

$$g_{m,tot} = -(g_{m4} + A_V g_{m6}) = -2g_{m6}(1 + A_n) \tag{3.45}$$

Total noise figure of the LNTA is calculated by input-referring noise of M_8, M_6 and M_4 from the output to the input:

$$NF = 1 + \frac{\frac{(\overline{i_{n8}^2}/g_{m8}^2)\times g_{m6}^2}{g_{m,total}^2} + \frac{\overline{i_{n4}^2}+\overline{i_{n6}^2}}{g_{m,total}^2}}{(1/2)^2 4KTR_s} = 1 + \frac{\frac{(4KT\gamma_b/g_{m8}^2)\times g_{m6}^2}{g_{m,total}^2} + \frac{4KT(\gamma_\alpha g_{m4}+\gamma_\beta g_{m6})}{g_{m,total}^2}}{KTR_s} \tag{3.46}$$

After assuming $\gamma_a = \gamma_b$ and replacing (3.45), the noise figure is simplified to:

$$NF = 1 + \frac{\gamma_b}{(1 + A_n)} + \frac{2\gamma_a}{g_{m,tot}R_s} \tag{3.47}$$

The second term is due to noise of M_b that is reduced $1 + A_n$ times by signal gain from other paths. The third term is the total noise contribution of the g_m-stage that is reduced 2 times by the total multi path gain provided in the LNA core (compared with NF of a standalone g_m-stage).

3.3.5 Final Structure with a 2nd Noise-Cancellation

The fully differential LNA, shown in Fig. 3.19, realizes the two-fold noise cancellation to further improve the circuit's noise performance. The core of this structure consists of the cross-coupled common-gate (CG) topology, $M_1(M_2)$, which is used for implementing the broadband input matching. The cross-coupled structure helps to provide input matching with half of the required g_m, thus leading to a reduced power consumption. The source-follower transistors, M_7 and M_9 (M_8, M_{10}), complete the core of the two-folded noise cancellations. The common-source (CS) transistors, M_{5a} and M_3 (M_{6a}, M_4), cancel the channel thermal noise of M_1 (M_2). The second noise-cancellation stage helps to cancel the channel thermal

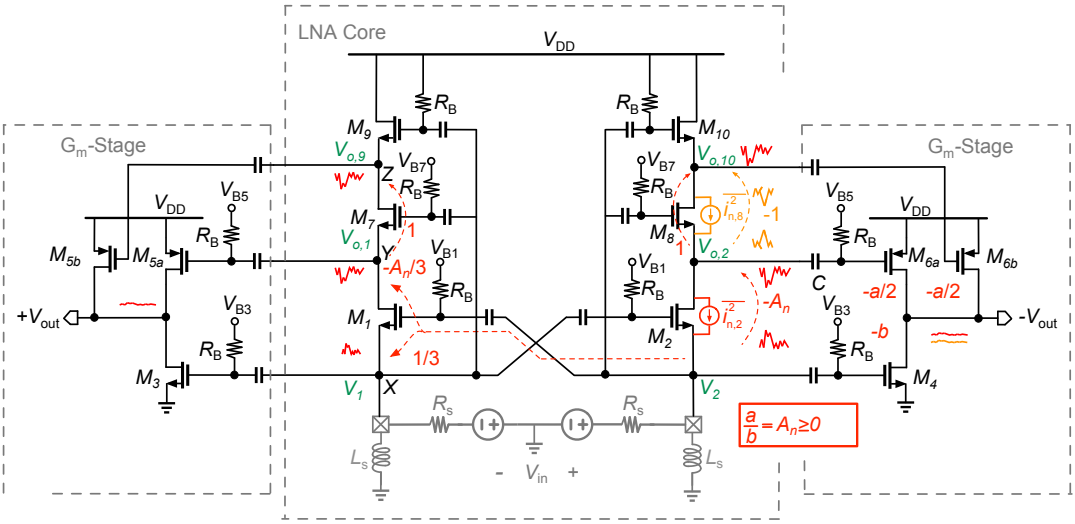


Figure 3.19: Wideband noise-cancelling LNTA (proposed structure 2). Noise-cancellation mechanisms of M_2 and M_8 is show in red and yellow, respectively, that is cancelled at the output. Noise of M_8 goes to the output with half gain, $\beta/2$.

noise of M_7 (M_8) by using M_{5a} and M_{5b} (M_{6a}, M_{6b}).

As was derived in (3.47), noise of gm-stage can be reduced by increasing the total gm. Also, M_2 noise can be lowered by increasing voltage gain of the LNA core. However, to reach a very low NF in range of $1-2\,dB$, excess increase of voltage gain degrades linearity of the g_m-stage.

To achieve this with a reasonable LNA core gain, M_4 noise in Fig. 3.18 is also reduced substantially, in addition to complete cancellation of M_2 noise. Instead of using only one M_4 on each side of the LNA core, two identical transistors M_8 and M_{10} are stacked (see Fig. 3.19, the proposed LNTA 2 [94]). Although the amplified input signal appears in-phase with the same gain, noise of M_8, (shown yellow in Fig. 3.19), appears anti-phase on $V_{o,2}$ and $V_{o,10}$. Then, splitting M_6,n into two half transistors ($M_{6,a}$ and $M_{6,b}$) cancels noise of $M_{b1,p}$ at the output via the introduced noise splitting technique. This way, only noise of M_{10}contributes to the output, but with a reduced gain of $g_{m6}/2$ instead of previously g_{m6} in (3.46). The noise splitting technique can be further utilized to cancel noise of M_{10} at the cost of a higher LNA core supply voltage.

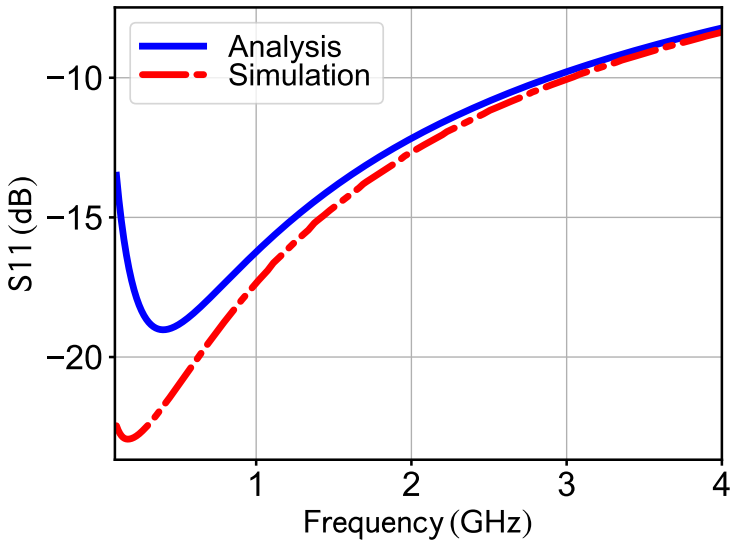


Figure 3.20: Simulated and calculated input return loss.

3.3.6 Input Matching

In the two-fold noise-cancelling architecture, the common-gate (CG) stage is used to provide wideband input matching which is roughly equal to $Z_{in} = 1/g_{m1}$ at low frequencies. Since the proposed architecture is fully differential, the gates of the input transistors, M_1 and M_2, are cross-coupled to save power consumption. In doing so, the total g_m needed to provide the 50 Ω input matching is cut in half, i.e. to 10 mS. The equivalent input impedance seen at input node, X, calculated as:

$$\begin{aligned} Z_{in} &= (R_{Ls} + sL_s) \left\| \frac{1}{sC_X} \right\| \frac{1}{2(g_{m1} + g_{mb1})} \\ &= \frac{R_{Ls} + sL_s}{C_X L_s s^2 + (R_{Ls} C_X + 2(g_{m1} + g_{mb1})L_s)s + (2(g_{m1} + g_{mb1})R_{Ls} + 1/2} \end{aligned} \tag{3.48}$$

where g_{mb1} represents the body effect of transistor M_1, R_{Ls} is a series resistance of the off-chip inductor L_s due to its finite quality factor and C_X is the lumped parasitic capacitances at the input node X.

The simulated S_{11} input return loss is shown in Fig. 3.20. The wideband input matching feature is well controlled with S_{11} < -10 dB in the whole bandwidth. The theoretical calculations show that by providing just half of the required transconductance, g_{m1}=10 mS, the 50 Ω input matching is properly provided, which is also confirmed by simulations. Both simulations and theoretical calculations prove that at higher frequencies the input matching

is getting worse, which is explained by the fact that the parasitic capacitances at input node become dominant and shape the input matching.

3.3.7 Gain Analysis

As indicated in Fig. 3.19, the input signal reaches the output node via four parallel paths. In the main path, path 1, the input signal is amplified by M_1 and M_{5a} to get to the output node. Paths 3 and 4 use M_7, M_{5a} and M_9, M_{5b}, respectively, to provide the boosted input signal at the output. Finally, the output voltage provided by path 2 is amplified by M_3. As shown in Section 3.3.6, Z_{in} is expressed by Eq. (3.48). Z_Y and Z_Z are total impedances to ground seen at nodes Y and Z, and defined as $r_{ds1} \left|\left|(sC_Y)^{-1}\right|\right| (g_{m7})^{-1}$ and $r_{ds7} \left|\left|(sC_Z)^{-1}\right|\right| (g_{m9})^{-1}$, respectively, where C_Y and C_Z are total parasitic capacitances to ground at nodes Y and Z. Finally, Z_{out} is a total impedance seen at the output node and is equal to $r_{ds3} \left|\left|(sC_{out})^{-1}\right|\right| r_{ds5}$ where C_{out} is the total parasitic capacitance at the output. Then, the LNA gain, by considering the effects of all parasitic capacitances, is equal to:

$$\begin{aligned} A_v =& \frac{Z_{in}}{Z_{in}+R_s}(2g_{m1}g_{m5}Z_Y + g_{m_{5a}} + g_{m_{5b}} \\ &+ g_{m3} + g_{m1}g_{m_{5b}}g_{m7}Z_Z Z_Y)Z_{out} \end{aligned} \tag{3.49}$$

According to Eq. (3.49), by increasing the transconductances g_{m1}, g_{m3} and g_{m5}, higher gain can be achieved but the total power consumption will be increased. Moreover, by increasing the size of M_3 and M_5 for the sake of increasing the gain, the total parasitic capacitances at output node increases thus leading to reduction in the -3–dB bandwidth of the proposed architecture.

To consider the body effect of M_1 and also to simplify the formulation, in all following equations g_{m1} stands for $g_{m1}+g_{mb1}$. In order to simplify Eq. (3.49), it is considered $Z_Y = 1/g_{m7}$, $Z_Z = 1/g_{m9}$ and $g_{m5a} = g_{m5b}$. By applying constraints from the calculated noise-cancellation equations in the next subsections, i.e. Eqs. (3.1) and (3.9), the gain of the proposed circuit can be simplified to:

$$A_v = \frac{3}{2}(g_{m5} + g_{m3})Z_{out} \tag{3.50}$$

As explained previously, the second-stage transistors, M_3 and M_5, are key contributions to

the total gain of the proposed circuit. Now, total gain of LNTA from input to output is provided by three paths: through V_a,V_{b1}, and V_{b2} nodes. However, the same equation in (3.45) is still valid here (signal voltage gain from V_{b1} to V_{b2} is 1).

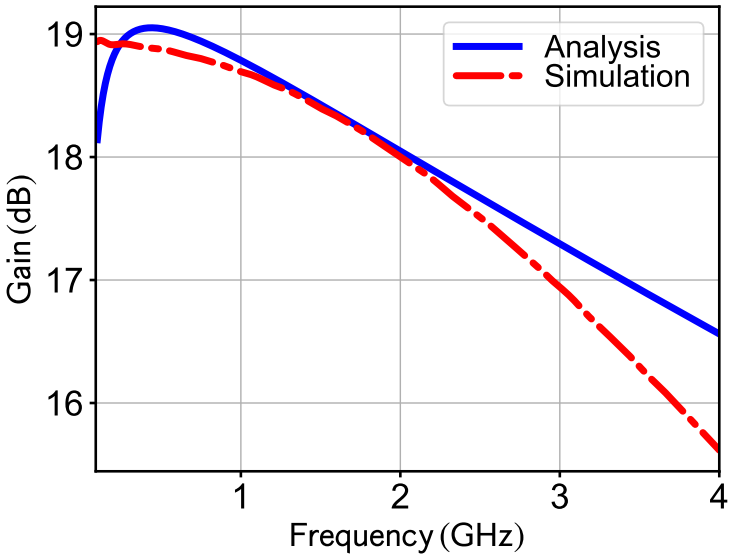


Figure 3.21: Simulated and calculated power gain S_{21}.

The S_{21} power gain is illustrated in Figs. 3.21. The S_{21} gain varies between 16–18.9 dB within 100 MHz up to 3.7 GHz where the calculated and simulated results are well-matched within the -3-dB bandwidth of 3.6 GHz. As explained in (3.50), by increasing the size of output transistors, the amount of parasitic capacitances at the output node increases. Consequently, the gain increases while the bandwidth narrows.

3.3.8 Noise Analysis

The half-circuit of the proposed LNA, shown in Fig. 3.22(a), is examined for its noise performance. All parasitic capacitances, including C_X, C_Y and C_Z associated with nodes X, Y and Z, are considered for bandwidth limitations. The channel thermal noise of M_1 and M_7 generates two anti-phase noise voltages at their respective drain and source ports. By utilizing the double noise-cancellation technique, their effects are canceled at the output node, ultimately leading to the enhancement of the LNA noise performance. Moreover, the channel thermal noise of M_9 is also partially cancelled through the noise-cancellation mechanism. This further reduces its contribution in the total output noise. As shown in Fig. 3.22(a), by cancelling the noise of $M_{1,7}$ and reducing the noise of M_9, the channel thermal noise of the

remaining transistors, M_3 and M_5, are now dominant in the total noise factor at the output node.

It is worth mentioning that M_7 can be used to intrinsically cancel the noise of M_1. However, it limits the available gain of the first stage. According to Fig 3.22(a), the two noise voltages generated by thermal noise of M_1 at nodes X and Y are amplified through path 1 and path 2 and added together at the output node. Since the amplitude voltage noise sources at nodes X and Y are not equal, paths 1 and 2 should provide different amplification factors such that their summation becomes zero at the output node, thus leading to first noise-cancellation condition expressed in the following equation:

$$\frac{g_{m3}}{g_{m5}} = \frac{g_{m1,T}}{g_{m7}} - 1 \tag{3.51}$$

The channel thermal noise of M_7 also generates two voltage sources at nodes Y and Z. By passing these voltages through paths 2 and 3 toward the output, they are amplified and added up at the output nodes. Since the equivalent impedances to ground seen at nodes Y and Z are equal, two generated voltage noises have the same amplitude at these nodes. By providing the same amplification factors through path 3 and 4, the effective contribution of the noise of M_7 becomes zero at the output node which defines the second noise criterion brought by Eq. (3.52).

$$\frac{g_{m5b}}{g_{m9}} = \frac{g_{m5a}}{g_{m7}} \tag{3.52}$$

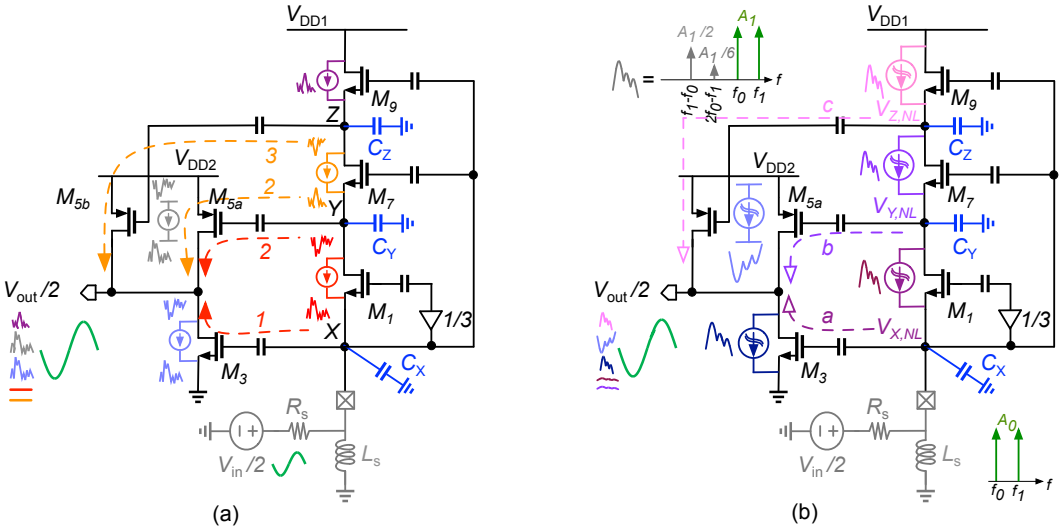


Figure 3.22: Half-circuit of two-fold noise-cancellation LNA: (a) noise contributions of each stage, (b) non-linearity contributions of each stage.

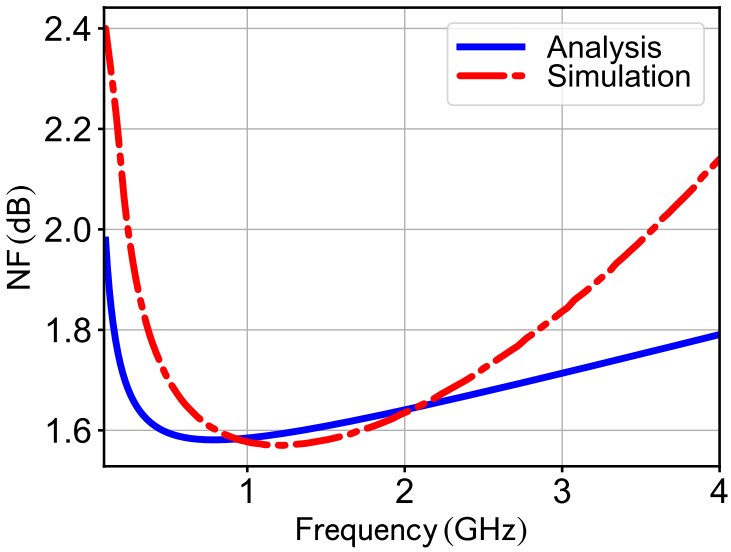


Figure 3.23: Simulated and calculated noise figure.

By canceling the channel thermal noise of M_1 and M_7, the total noise factor of the half circuit of 3.22(a) is equal to the summation of the noise factors of M_3, M_5 and M_9, which can be derived as in Eq. (3.53):

$$\begin{aligned}\frac{F_T}{2} =& 1+\frac{1}{9R_s g_{M9}(1+g_{m3}/g_{m5})^2}\frac{\gamma}{\alpha}+\frac{4}{9R_s g_{M3}(1+g_{m5}/g_{m3})^2}\frac{\gamma}{\alpha}\\ &+\frac{4}{9R_s g_{M5}(1+g_{m3}/g_{m5})^2}\frac{\gamma}{\alpha}\end{aligned} \tag{3.53}$$

Total new noise figure of the LNTA is derived by referring noise contribution of M_{b2}, M_α and M_β from the output to the input (the same way as (3.46) is derived) and is simplified to:

$$NF = 1+\frac{\gamma_b}{4(1+A_n)}+\frac{2\gamma_a}{g_{m,tot}R_S} \tag{3.54}$$

The second term is due to noise of M_{b2} that is substantially reduced 4 times by the proposed noise splitting technique, and $1+A_n$ times by signal gain from other paths.

Figure 3.23 plots the noise figure of the LNTA compared with the theoretical calculations derived previously. By canceling the thermal noise of transistors $M_{1,2}$ and $M_{7,8}$, the NF of merely 1.58 to 2.4 dB is achieved over the ultra-wide frequency range of 100 MHz to 4 GHz. The simulated NF results agree very well with the theoretical calculations using (3.53), and the maximum fitting error is only 0.4 dB.

3.3.9 Linearity

Figure 3.22(b) shows the non-linearity contributions of each transistor in this two-fold noise-cancellation structure. The non-linearity of each transistor, including its second and third-order products, is modeled with a non-linear current source. For a small-signal operation, the nonlinear transconductance of a short-channel CMOS transistor is represented by a power series:

$$i_m = g_m V_{gs} + \frac{g'_m}{2} V_{gs}^2 + \frac{g''_m}{6} V_{gs}^3 \tag{3.55}$$

where g_m is a small-signal transconductance and g'_m and g''_m are its higher-order coefficients, which define the strengths of the corresponding non-linearity. Figure 3.22(b) shows that the non-linearities of M_1, M_7 and M_9 generate voltages at nodes X, Y and Z, which are defined based on Volterra series as $V_{X,\mathrm{NL}}$, $V_{Y,\mathrm{NL}}$ and $V_{Z,\mathrm{NL}}$, respectively. These non-linear voltages will be canceled at the output node after passing through the three paths shown in Fig. 3.22(b). This happens if the nonlinear coefficients a, b and c, are properly defined with Volterra series analysis leading to gain distortion conditions related to $g'_{m_{1,7}}$ and $g''_{m_{1,7}}$.

By canceling the non-linearity of the first stage, the linearity performance of the proposed LNA is now only limited by the third-order distortion of M_3 and M_5. Through a long derivation, it can be proven that by properly setting the 3$^{\mathrm{rd}}$ order non-linearity conditions for M_3 and M_5 (e.g., via biasing), the distortion products of M_3 and M_5 will cancel each other, thus leading to to a significant improvement in the total IIP$_3$.

3.3.9.1 Non-linearity derivation based on Volterra series analysis

In this section, based on Volterra series analysis, [95] and [84], the non-linearity performance of the two-fold noise cancellation structure, the half circuit shown in Fig. 3.22 (b), has been investigated. All parasitic capacitances including C_X, C_Y and C_Z associated with nodes X, Y and Z, are considered to show bandwidth limitation.

According to (3.55), the small signal current following to M_1,M_7 and M_9 are expressed as:

$$\begin{aligned} i_{m1} &= -2g_{m1}V_X + \frac{g'_{m1}}{2}(-2V_X)^2 + \frac{g''_{m1}}{6}(-2V_X)^3 \\ i_{m7} &= g_{m7}(V_X - V_Y) + \frac{g'_{m7}}{2}(V_X - V_Y)^2 + \frac{g''_{m7}}{6}(V_X - V_Y)^3 \\ i_{m9} &= g_{m9}(V_X - V_Z) + \frac{g'_{m9}}{2}(V_X - V_Z)^2 + \frac{g''_{m9}}{6}(V_X - V_Z)^3 \end{aligned} \tag{3.56}$$

The nonlinear voltages generated by nonlinear current at nodes X, Y, and Z are defined based on Volterra series as follows.

$$\begin{aligned} V_X &= A_1(s)oV_s + A_2(s_1,s_2)oV_s{}^2 + A_3(s_1,s_2,s_3)oV_s{}^3 \\ V_Y &= B_1(s)oV_s + B_2(s_1,s_2)oV_s{}^2 + B_3(s_1,s_2,s_3)oV_s{}^3 \\ V_Z &= C_1(s)oV_s + C_2(s_1,s_2)oV_s{}^2 + C_3(s_1,s_2,s_3)oV_s{}^3 \\ V_{out} &= D_1(s)oV_s + D_2(s_1,s_2)oV_s{}^2 + D_3(s_1,s_2,s_3)oV_s{}^3 \end{aligned} \tag{3.57}$$

where $A_n(s_1,s_2,...,s_n)$, $B_n(s_1,s_2,...,s_n)$, $C_n(s_1,s_2,...,s_n)$ and $D_n(s_1,s_2,...,s_n)$ are the Laplace transforms of the n^{th}-order Volterra kernel at X, Y, Z and output nodes, also often called the n^{th}-order nonlinear transfer function. $s = j\omega$ is the Laplace variable, and the operator "o" means that the magnitude and phase of each spectral component of v_x^n is to be changed by the magnitude and phase of $A_n(s_1,s_2,...,s_n)$, where the frequency of the component is $\omega_1 + \omega_2 + \ldots + \omega_n$ [95].

By calculating the KCL equation at node X,Y and Z and applying Equations (3.56) and (3.57) and solving it, the first-order Volterra kernel is equal to:

$$\begin{aligned} g_{m9}(A_1(s) - C_1(s)) &= g_{m7}(A_1(s) - B_1(s)) + \frac{C_1(s)}{Z_Z} \\ C_1(s) &= \frac{(g_{m9} - g_{m7})A_1(s) + g_{m7}B_1(s)}{g_{m9} + \frac{1}{Z_Z}} \end{aligned} \tag{3.58}$$

Next, consider the following equations for the second-order Volterra series kernel are calculated at the following equations, where $\overline{A_1(s_1)A_2(s_2,s_3)}$ represents the second order interaction

operator.

$$A_2(s_1,s_2)=\frac{2g'_{m1}A_1(s_1)A_1(s_2)}{\frac{1}{Z_X(s_1+s_2)}-\frac{1}{Z_s(s_1+s_2)}+2g_{m1}} \tag{3.59}$$

$$-2g_{m1}A_2(s_1,s_2)oV_s^2+2g'_{m1}A_1(s_1)A_1(s_2)oV_s^2+\frac{A_2(s_1,s_2)oV_s^2}{Z_s(s_1+s_2)}=\frac{A_2(s_1,s_2)oV_s^2}{Z_X(s_1+s_2)}$$

$$A_2(s_1,s_2)=\frac{2g'_{m1}A_1(s_1)A_1(s_2)}{\frac{1}{Z_X(s_1+s_2)}-\frac{1}{Z_s(s_1+s_2)}+2g_{m1}} \tag{3.60}$$

$$\begin{aligned}B_2(s_1,s_2)=&\Big(\frac{g'_{m7}}{2}-2g'_{m1})A_1(s_1)A_1(s_2)+(2g_{m1}+g_{m7})A_2(s_1,s_2)+\frac{g'_{m7}}{2}B_1(s_1)B_1(s_2)\\&-g'_{m7}\overline{A_1(s_1)B_1(s_2)}\Big)\times\Big(g_{m7}+\frac{1}{Z_Y(s_1+s_2)}\Big)^{-1}\end{aligned} \tag{3.61}$$

$$\begin{aligned}C_2(s_1,s_2)=&\Big((\frac{g'_{m9}}{2}-2g'_{m1})A_1(s_1)A_1(s_2)+(2g_{m1}+g_{m9})A_2(s_1,s_2)+\frac{g'_{m9}}{2}C_1(s_1)C_1(s_2)\\&-g'_{m9}\overline{A_1(s_1)C_1(s_2)}-\frac{B_2(s_1,s_2)}{Z_Y(s_1+s_2)}\Big)\times\Big(g_{m9}+\frac{1}{Z_Z(s_1+s_2)}\Big)\end{aligned} \tag{3.62}$$

By considering α_0 and α_1 are defined as $A_1(s_1)A_1(s_2)A_1(s_3)$ and $3\overline{A_1(s_1)B_1(s_2)B_1(s_3)}-3\overline{A_1(s_1)B_1(s_2)B_1(s_3)}-B_1(s_1)B_1(s_2)B_1(s_3)$ respectively. Moreover $\beta_0=\overline{A_1(s_1)A_2(s_2,s_3)}$ and $\beta_1=\overline{B_1(s_1)B_2(s_2,s_3)}-\overline{A_1(s_1)B_2(s_2,s_3)}-\overline{B_1(s_1)A_2(s_2,s_3)}$. In calculation of third Volterra kernel of V_Z, it is considered $\lambda_0=\overline{C_1(s_1)C_2(s_2,s_3)}-\overline{A_1(s_1)C_2(s_2,s_3)}-\overline{C_1(s_1)A_2(s_2,s_3)}$ and $\lambda_1=3\overline{A_1(s_1)C_1(s_2)C_1(s_3)}-3\overline{A_1(s_1)C_1(s_2)C_1(s_3)}-C_1(s_1)C_1(s_2)C_1(s_3)$, the third-order

Volterra kernels are achieved in the following equations.

$$A_3(s_1,s_2,s_3)=\frac{4g'_{m1}\beta_0-\frac{4}{3}g''_{m1}\alpha_0}{\frac{1}{Z_X(s_1+s_2+s_3)}-\frac{1}{Z_s(s_1+s_2+s_3)}+2g_{m1}} \tag{3.63}$$

$$B_3(s_1,s_2,s_3)=\frac{(\frac{g''_{m7}}{6}+\frac{4}{3}g''_{m1})\alpha_0+(2g_{m1}+g_{m7})A_3(s_1,s_2,s_3)+g'_{m7}\alpha_1+\frac{g''_{m7}}{6}\beta 2+(g'_{m7}-4g'_{m1})\beta_0}{g_{m7}+\frac{1}{Z_Y(s_1+s_2+s_3)}} \tag{3.64}$$

$$C_3(s_1,s_2,s_3)=\frac{(\frac{g''_{m9}}{6}+\frac{4g''_{m1}}{3})\alpha_0+(2g_{m1}+g_{m9})A_3(s_1,s_2,s_3)+(g'_{m9}-4g'_{m1})\beta_0+g'_{m9}\lambda_0+\frac{g''_{m9}}{6}\lambda_1}{g_{m9}+\frac{1}{Z_Z(s_1+s_2+s_3)}} \tag{3.65}$$

Finally by using (3.58)–(3.65) and considering $g_{m5a}=g_{m5b}$, the first-order and third-order of Volterra series kernel at the output node, $D_1(s)$ and $D_3(s_1,s_2,s_3)$ are calculated as follows which are needed to calculated the IIP3 of the proposed circuit.

$$D_1(s)=\Big(A_1(s)g_{m3}+(B_1(s)+C_1(s))g_{m5a}\Big)\times Z_L \tag{3.66}$$

$$\begin{aligned}D_3(s_1,s_2,s_3)=&\Big[2\overline{A_1(s_1)A_2(s_2,s_3)}\frac{g'_{m3}}{2}+A_3(s_1,s_2,s_3)g_{m3}+\Big(B_3(s_1,s_2,s_3)+C_3(s_1,s_2,s_3)\Big)g_{m5a}\\&+\Big(B_1(s)^3+C_1(s)^3\Big)\frac{g''_{m5a}}{6}+A_1^3(s)\frac{g''_{m3}}{6}+g'_{m5a}\Big(\overline{B_1(s_1)B_2(s_2,s_3)}+\overline{C_1(s_1)C_2(s_2,s_3)}\Big)\Big]\times Z_L\end{aligned} \tag{3.67}$$

By applying (3.67) and (3.66), the A_{IP3} is calculated as:

$$A_{IP_3}(2\omega_b-\omega_a)=\sqrt{\frac{4}{3}\left|\frac{D_1(j\omega_a)}{D_3(j\omega_b,j\omega_b,-j\omega_a)}\right|} \tag{3.68}$$

then the IIP_3 is equal to:

$$\begin{aligned}IIP_3(2\omega_b-\omega_a)&=\frac{A_{IP_3}(2\omega_b-\omega_a)^2}{8\Re(Z_s(j\omega_a))}\\&=\frac{1}{6\Re(Z_s(j\omega_a))}\left|\frac{D_1(j\omega_a)}{D_3(j\omega_b,j\omega_b,-j\omega_a)}\right|\end{aligned} \tag{3.69}$$

As shown in (3.69), in order to improve the total IIP3 of the two-fold noise cancellation, the

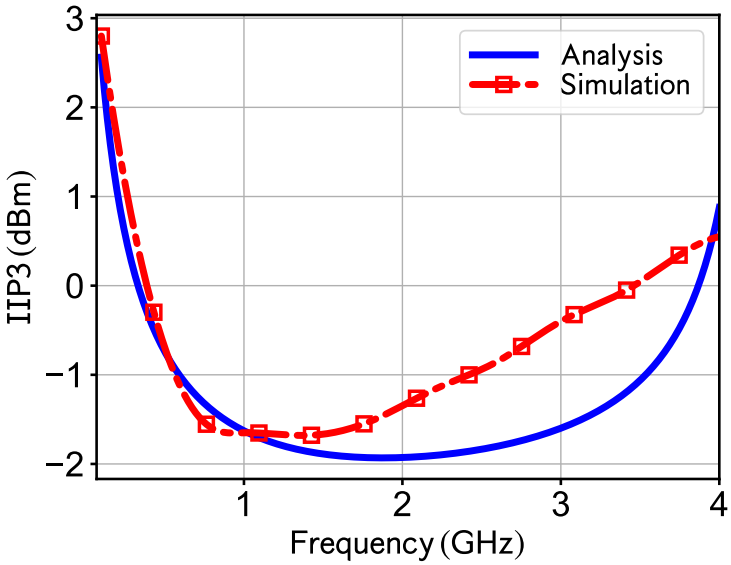


Figure 3.24: Simulated and calculated IIP3.

third Volterra series kernel of output voltage, $D_3(s_1, s_2, s_3)$, should decrease. The second and third terms in (3.67) are based on third-order non-linearity of M_1, M_7 and M_9. Thanks to the two-fold noise-cancellation technique it further cancels the third-order distortion of M_1 and M_7 and partially cancels the third-order distortion of M_9. By cancelling the non-linearity of first stage, the third-order non-linearity of M_3 and M_5 are dominated one which can be canceled or reduced by properly biasing of M_3 and M_5, which provides a different polarity for third-order non-linearity component of transistor, g_m''. The third-order cancellation criteria of M_3 and M_{5a} in low frequency are given in the following equation.

$$\frac{g_{m3}''}{g_{m5a}''} = -\frac{9}{16}(1 + \frac{2g_{m1}}{g_{m7}})^3 \tag{3.70}$$

Finally, the linearity performance of the presented LNA is illustrated by the IIP3 circuit simulation plots in Fig. 3.24 with superimposed analytical plots to verify the derived IIP3 equation derived in (3.69). The two-tone simulation is done by considering a 2.5 MHz spacing between the tones. The IIP3 simulations are firstly done for several frequencies; then the results are mathematically interpolated. The results prove that by properly setting the noise cancellation conditions and third-order non-linearity conditions, the linearity of the proposed two-fold LNA can be improved to IIP_3 of -1.6–+2.8 dBm.

3.4 Conclusion

Two novel novel wide band LN(T)As are proposed which are based on two-fold noise cancellation technique. The first design comprises three stages to achieve a low NF and to extend the high edge of bandwidth. The main idea is to cancel the channel thermal noise of the first noise-cancellation stage by using another cancellation stage, i.e. third LNA stage. The measurement results show that throughout the entire bandwidth a high gain is achieved and the input and output matching are well met, with very good noise and linearity performance.

Table 3.1: Summary and comparison with state-of-the-art wideband LNAs.

	This work	[85] JSSC'21	[68] TCASI'20	[70] TCASI'19	[71] TCASII'19	[72] TMTT'19	[74] TCASI'18	[75] TCASII'18	[91] MWCL'21	[80] MWCL'14
Noise cancel. used?	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No
Core drive ext. 50Ω?	Yes	Yes	No**	No**	Yes	No**	No**	No**	No**	No***
CMOS tech. [nm]	28	28	65	65	65	65	65	180	130	180
BW_{3-dB} [GHz]	0.02~2	0.02~4.5	0.05~1.3	0.05~1	0.4~2.2	0.3~4.4	0.2~2.7	2~5	0.1~1	0.025~1.4(#)
S_{11} [dB]	≤-15	≤-10	–	≤-10	–	–	–	–	<-10	-15
S_{21} [dB]	18.5	15.2	27.5	30	16.4	26.7	21.2	13	14	10
IIP3 [dBm]	+1.29~+4.25	-4.6~-3.53	-4~-1	-4~-1	-5	-14.2	-2	-9.5	+2	-1
IIP2 [dBm]	+19.6~+27.6	+3.49~+7.25	+10~+19.6	+10.7~+20.6	–	–	–	–	–	–
P-1dB [dBm]	-6.5	–	–	–	–	–	-22.2	-15	–	–
NF [dB]	2.5~3.5	2.09~3.2	2.3~3	2.3~3.3	2~2.5	3~4.4	3~3.5	6~8	4	5
VDD [V]	1	1	1	2.2	1.2	1	1.2	1.8	1.2	1.5
Power [mW]	4.1	4.5	5.7	19.8	29	13.7	0.96	1.8	2.7	7.5
Active area [mm^2]	0.022	0.03	0.046	0.0448	0.16	0.009	0.05	0.72	0.099	0.033
FoM_1	5.22	7.76	6.18	2.17	0.7	6.5	30.04	2.49	1.1	0.27
FoM_2	13.89	3.452	3.48	1.7	0.22	0.24	18.95	0.28	1.75	0.21
FoM_3	694	172.6	69.56	34.52	0.55	0.82	94.77	0.14	17.5	8.22

* Differential load is 100 Ω. ** Uses addt'l on-chip measurement buffer. *** Needs addt'l external measurement buffer.
# Estimated from plots.

Chapter

4

A High In/Out-of-Band Rejection Discrete-Time IIR Band-Pass Filter Using a Clock Phase Reusing Technique in 28-nm CMOS

Having covered the front-end part of the wireless receiver in the previous two chapters, we now move to the second part of the thesis which covers the analog back-end part of the receiver that conditions the signal just before feeding it to an ADC.

As discussed in Chapter 1, monolithic RF wireless receivers have been trending toward high intermediate frequency (IF) or superhetrodyne radios thanks to recent breakthroughs in silicon integration of band-pass channel-select filters [96–99]. The main motivation is to avoid the common issues in the currently predominant zero/low IF receivers, such as poor 2nd-order nonlinearity, sensitivity to $1/f$ (i.e. flicker) noise and time-variant dc offsets, especially in fine CMOS technology [17, 19, 46, 56, 100, 101]. To avoid interferers and blockers at the susceptible *image* frequencies that the high-IF entails, band-pass filters (BPF) with high quality (Q) factor components for sharp transfer-function transition characteristics are now required.

4.1 Introduction

N-path and charge-sharing (CS) discrete-time (DT) filters are two types of passive BPFs which have been explored recently to provide filtering at higher IF frequencies. They have been investigated as an alternative to the conventional continuous-time (CT) BPFs [102, 103]. A major disadvantage of the N-path filters, however, is that they cannot reject interferes/blockers at images that are located at odd harmonics of the sampling frequency, f_s, (equating there to the IF) because it inherently features replicas there.

To address the problem of replicas in the N-path filter and to provide IF tunability independent from f_s, full-rate switched-capacitor based CS DT infinite impulse response (IIR) filters were introduced in [96, 104]. They can operate in either voltage or current mode. The tunability feature offers greater freedom to change the IF frequency, for example, helping to dynamically avoid RX desensitization. Moreover, the scaled CMOS technology relies on switches, capacitors, and inverters, so the DT filters can keep on improving their performance due to the use of faster and smaller switching transistors, higher density capacitors and faster digital circuitry that consumes lower power. This makes the DT filters appealing in high-IF RX designs. Nonetheless, the Q-factor of these filters, defined as $Q = f_c/\text{BW}$, where f_c is the center frequency and BW is the bandwidth, is still quite low (e.g. Q≈0.5 for the 1st-order BPF reported in [105]), which makes it imperative to increase its order for sharper filtering. This was done by providing a higher number of clock phases, e.g. doubling their number to merely gain one order of filtering. This unfortunately adds significant complexity to the clock generation and distribution circuitry.

In this Chapater, we further improve the in-band and out-of-band filtering characteristics of a complex-signaling (i.e. using in-phase, I, and quadrature, Q, signal components) charge-sharing DT IIR filter by means of a proposed clock reusing technique. The main aim is to increase the order of the filter without increasing the number of clock phases, as required in the prior-art implementations. As such, this structure does not suffer from a reduction in duty cycle of the clock generator, which is a common issue in the prior-art complex IIR filters [96], and it is capable of running at high frequencies.

The intended application of the proposed DT complex-signaling BPF is shown in Fig. 4.1. The DT-receiver front-end path generally starts with a continuous-time (CT) low-noise transconductance amplifier (LNTA) [85] to amplify the antenna input and convert it to RF

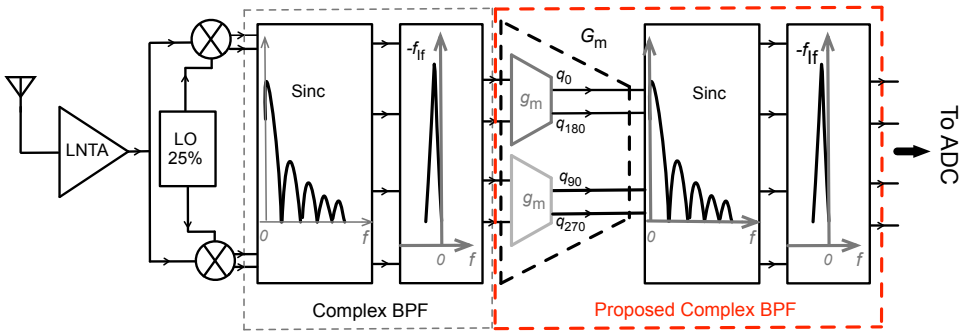


Figure 4.1: Example use of the proposed BPF in a DT superheterodyne receiver.

current. It is followed by a multi-phase (i.e. quadrature, but octal is also possible [96]) passive sampling mixer [106, 107] that preserves the DT nature of the signal. Thus generated IF signal feeds a multi-stage IF DT-filter [7, 96, 103] to perform channel selection and reject the IF images.

This Chapter is organized as follows. We start in Section 4.2 with reviewing the basic idea of charge-sharing complex band-pass filtering. We next introduce the clock reusing technique and describe the proposed BPF in detail. We then follow with an analysis of the filter's transfer function. In Section 4.3, we then describe the circuit implementation and follow with the simulation and measurement results in Section 4.4.

4.2 Band-Pass Filter Topology

4.2.1 Conventional 1st/2nd-Order Complex BPF

Prior-art discrete-time charge-sharing IIR filters [96, 104, 108] can improve their filtering performance mainly by means of increasing the order of filtering. Thus far, this has been achieved by increasing the number of charge-sharing phases, leading to a reduction in the duty cycle of a clock generator. The advent of new wideband applications, such as 5G cellular, necessitates high clock frequencies, which makes it impractical to decrease the duty cycle D beyond a certain point, dictated by the acceptable rise and fall edge timing in a given technology.

The conventional 1st-order band-pass IIR filter is illustrated in Fig. 4.2. It was synthesized in [108] from a 4th-order low-pass IIR filter with a single electrical node being shared by both the input (charge) and output (voltage). Here, the input is presented on four nodes as

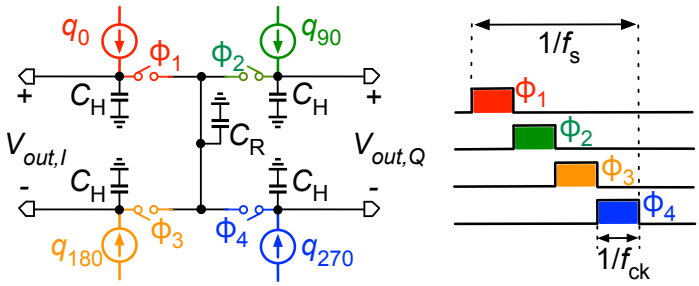


Figure 4.2: Conventional complex 1st-order DT IIR band-pass filter.

complex-valued charge packets consisting of the in-phase (q_0, q_{180}) and quadrature (q_{90}, q_{270}) differential components, which implies $q_0 = -q_{180}$ and $q_{90} = -q_{270}$ under ideal conditions. We can then encode the complex-valued input signal as $q_{in} = q_I + jq_Q = (q_0 - q_{180}) + j(q_{90} - q_{270}) \approx 2q_0 + j2q_{90}$. Similarly, $V_{out} = V_{out,I} + jV_{out,Q}$. During each phase of ϕ_1–ϕ_4, four charge packets of the input sample are accumulated into their respective history capacitors C_H. At the end of each phase, the rotating capacitor C_R containing a part of the charge "history" from the preceding phase is ready to be charge-shared with C_H containing the current input charge packet and the "history" charge. Therefore, in each phase, rotating capacitor C_R removes a charge proportional to $C_R/(C_H + C_R)$ from each C_H and then delivers most of it (i.e. $C_H/(C_H + C_R)$) to the next C_H. The band-pass characteristic is due to the periodical charge rotation among the four quadrature phases by means of the rotating capacitor C_R cycling through the the four history capacitors, C_H. The four quadrature outputs are read out as voltages from the same four physical nodes at the sampling rate of $f_s = 1/T_s = f_{\text{ck}}/4$.

The charge-sharing operation forms a complex filter with a transfer function derived as:

$$H^{(1)}(z) = \frac{V_{out}(z)}{q_{\text{in}}(z)} = \frac{k}{1 - a(1 + j(1-a))z^{-1}} \tag{4.1}$$

where $z = e^{j2\pi f/f_s}$, $k = 1/(C_H + C_R)$ and $a = C_H/(C_H + C_R)$, and superscript $^{(1)}$ denotes the filter's order. In accordance with Eq. (4.1), the charge-sharing process forms a complex 1st-order filter centered at

$$f_c^{(1)} = \frac{f_s}{2\pi} \arctan(1 - a) \tag{4.2}$$

Therefore, the center frequency f_c is adjustable by changing coefficient a and sampling frequency f_s. Compared to the N-path filter whose center frequency is exactly equal f_s, here

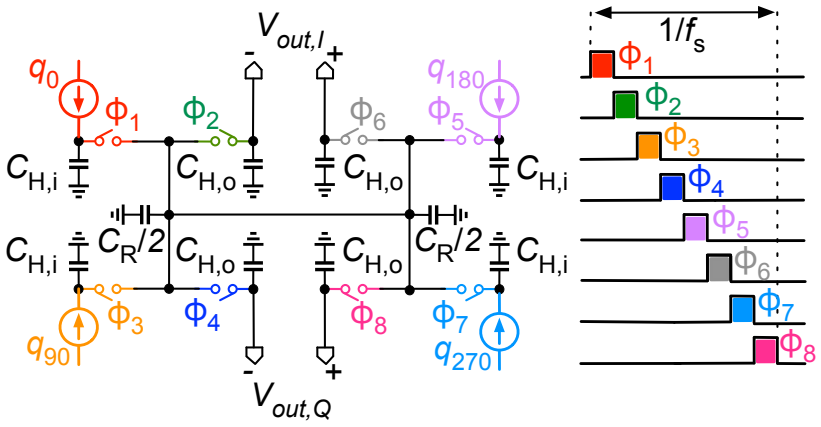


Figure 4.3: Conventional 2nd-order complex BPF built upon the 1st-order BPF of Fig. 4.2. For symmetry, C_R is redrawn in two halves, $C_R/2$.

f_c is slightly sensitive to the capacitance ratio mismatch, but this is not an issue in fine technology nodes and could be adjusted through calibration.

A key advantage of this structure, however, is that the I/Q charge-sharing BPF does not suffer from replicas and can provide robust filtering covering the entire range $-f_s/2$ to $f_s/2$ [108], especially when lower center frequencies are targeted (e.g. few tenths of MHz). It is worth mentioning that the N-path filter also has no replicas in the entire range $-f_s/2$ to $f_s/2$ from its center frequency f_c even up to $f_{max} < Nf_s/2$ [109]. However, as stressed in [96], there is a direct relationship between the sampling and center frequencies in the N-path filter (f_c=f_s). For instance, to achieve a lower value of f_c in the N-path filter (i.e f_c=10 MHz), f_s should be equal to 10 MHz which causes many replicas around $(2k+1)f_c, k = 1, 2, 3, ...$ However, in the complex charge-sharing BPF, f_s can be high enough (e.g. 250 MHz) while achieving low $f_c = 10$ MHz without having any replica problems in the entire range -125 MHz $< f <$ 125 MHz. Moreover, the asymmetric characteristic of the complex BPF provides more attenuation at the image frequency. As a result, this structure is suitable as a BPF centered at f_c and rejecting image signals located at (positive and negative) harmonics of f_c. Therefore, the effect of the unwanted image folding is less severe, in contrast to the N-path filters [108].

General bandwidth formula of the conventional 1st-order band-pass filter can be derived

as:

$$BW \simeq \frac{f_s}{2\pi}\left|\ln\left(\frac{C_S^2+C_H^2+2C_SC_H\cos(\theta)}{(C_S+C_H)^2}\right)\right| \tag{4.3}$$

where θ is $\pi/2$ for the filter with a quadrature input. By using (4.2) and (4.3), the quality factor of the first-order BPF is obtained as:

$$Q = \frac{f_c}{BW} \simeq \frac{\arctan(1-a)}{\left|\ln(a^2+(1-a)^2\right|} \tag{4.4}$$

However, (4.4) indicates that the first-order complex BPFs suffer from a low quality factor (e.g. for a=0.9, $Q \simeq$0.5).

Hence, to obtain stronger filtering, the order of this filter can be incremented by adding an additional charge-sharing phase to each of the four paths. An approach first introduced in [97] to increase the filtering order of a low-pass filter (LPF) by adding extra charge-sharing operations was employed in [96] for a BPF. Fig. 4.3 shows the resulting diagram of a 2nd-order BPF, which adds an extra set of four switched history capacitors $C_{H,o}$ to Fig. 4.2 in order to perform the additional charge-sharing operation and to provide a dedicated quadrature output, V_{out}. Contrary to [97], the output history capacitor $C_{H,o}$ also shares the charge with other phases through the rotating capacitor, just like the input history capacitor $C_{H,i}$ does, leading to a second complex pole. As a result, the output $C_{H,o}$ capacitors must have their own dedicated phases in order to avoid any C_R charge-sharing contention with the input $C_{H,i}$ capacitors. Hence, the number of phases and thus the complexity of the clock generation and distribution circuitry doubles while the duty cycle decreases from 25% to 12.5%.

To maintain the same sampling frequency f_s as in the 1st-order BPF, the 2-nd order BPF's input clock frequency f_{ck} needs to run at twice the rate, yielding $f_{\text{ck}} = 8f_s$. As a result, the pulse width halves, which makes it crucial to appropriately set the transistor switch sizes in Fig. 4.3 such that they stay "ON" long enough for sufficient settling during the charge sharing. By redefining $a_i = C_{H,i}/(C_{H,i}+C_R)$ and $a_o = C_{H,o}/(C_{H,o}+C_R)$, we can derive below the transfer function of this 2nd order BPF as

$$H^{(2)}(z) = \frac{k(1-a_o)z^{-1}}{(1-a_oz^{-1})(1-a_iz^{-1}) - j[(1-a_i)(1-a_o)z^{-2}]} \tag{4.5}$$

The order of this type of BPF can be arbitrarily extended by adding more phase slots along with more history capacitors between the existing input and output history capacitors [96]. In general, to have an M-order of quadrature complex DT BPF, $4 \times M$ number of clock phases are required, which can quickly inflate the complexity of the circuit design.

4.2.2 Proposed Complex BPF with Clock Reuse

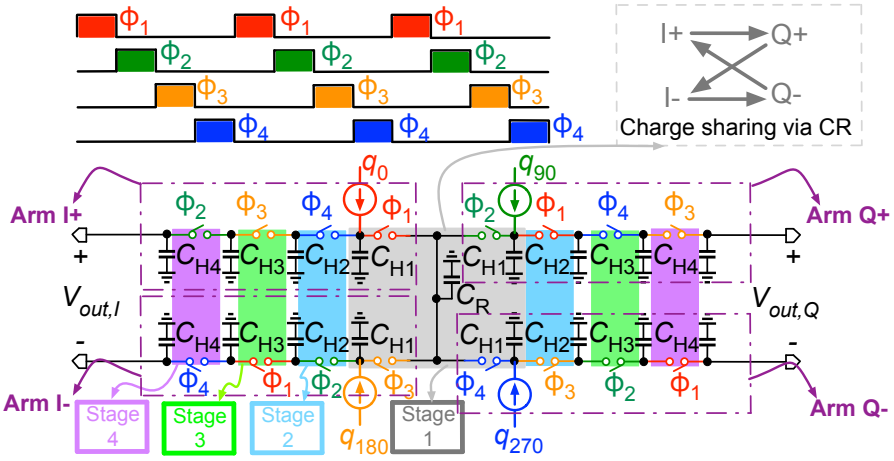


Figure 4.4: Proposed DT complex BPF with clock-phase reuse.

A new topology of the complex band-pass IIR filter that can substantially increase its order, yet without increasing the number of phases, is introduced in Fig. 4.4. This allows to beneficially reuse the simple I/Q clock generator from the 1st-order configuration in which $f_s = f_{\text{ck}}/4$.

Four different stages of the proposed band-pass filter are shown with different highlighted colors in Fig. 4.4. Just like in Fig. 4.2, the quadrature input charge packet components q_0–q_{270} are integrated on their respective history capacitors, C_{H1}, during respective phases ϕ_1–ϕ_4. During the first cycle, the input charge of each arm is shared between the history capacitors of the first stage (gray area) through the common rotating capacitor C_R. With ϕ_1 going active, in first stage, the input charge I+ (i.e. q_0) is shared between C_{H1} and C_R. Moreover, the residual of the previous charge stored in C_R (from Q-, i.e. q_{270}) is also shared with C_{H1}. Then, at ϕ_2 of the first cycle, the residual of the previous charge stored in C_R (from I+) and also the input charge of the second arm, Q+ (i.e. q_{90}), are shared between C_R and C_{H1}. By activating ϕ_3, now C_R shares the residual charge of the previous phase, Q+, with C_{H1} in the

third arm and also its input charge, I- (i.e.q_{180}), is shared between C_R and C_{H1}. Finally at ϕ_4, C_R shares the residual of the I- charge with C_{H1} of the 4th arm in addition of the charge sharing of Q- between C_R and C_{H1}.

By moving from the first cycle to the next, the 2nd/3rd/4th-stages (blue, green and purple areas in Fig. 4.4) are activated. Then, the charge stored in C_{H1} of the first stage in each arm is shared with its history capacitors, C_{H2}, C_{H3}, and C_{H4}, respectively. For instance, by considering "arm I+", before the phase ϕ_1 clock goes active in the 2nd cycle, at phase ϕ_4 of the 1st cycle, the previous charge of its history capacitor C_{H1} gets shared with the 2nd history capacitor C_{H2}. Then, at the 3rd cycle at phase ϕ_3, that shared charge is shared again with the 3rd history capacitor C_{H3}. Eventually, at the 4th cycle, the remaining charge is shared with the history capacitor at the output node, i.e. C_{H4}.

The proposed charge-sharing scheme happens during four cycles for each path, leading to a higher-order bandpass filtering. Consequently, without adding any extra phases, which would inadvertently narrow down the pulses (of duration $1/f_{\mathrm{ck}}$) under the constraint of the same sampling rate $f_s = f_{\mathrm{ck}}/4$, a much better filtering can be achieved. This leads to sharper transition bands, especially useful for in-band blockers in 4G/5G receivers.

Just like in the previous case of the conventional 1st-order BPF of Fig. 4.2, periodically sharing charges on all the 1st-stage history capacitors, C_{H1}, via the rotating capacitor, C_R, generates the *global* band-pass behavior in the proposed filter. Moreover, the 2nd/3rd/4th-stage of history capacitors, C_{H2}–C_{H4}, are charge-shared with their respective C_{H1} in each arm which creates a *local* low-pass filter. In other words, this 3-stage pipelined charge transfer and LPF filtering operate only on each individual component of the complex-valued quadrature signal where they all contribute to strengthening of the band-pass filtering and from the perspective of the overall transfer function, the band-pass filtering gets improved.

Schematic-level simulations of the frequency response of the proposed complex BPF of Fig. 4.4 are compared in Fig. 4.5 against the conventional 1st- and 2nd-order BPFs (Figs. 4.2 and 4.3, respectively). It is evident that the new method, under the constraint of the filter's identical sampling, f_s, and center, f_c, frequencies, significantly improves the in-band and out-of-band rejection compared to the 1st-order filter, all with the same occupied area. The new filter consumes the total history capacitance ($\sum C_H$) of 6 pF, the same as in the conventional 1st-order BPF.

For the conventional 2nd-order filter, on the other hand, the input and output history

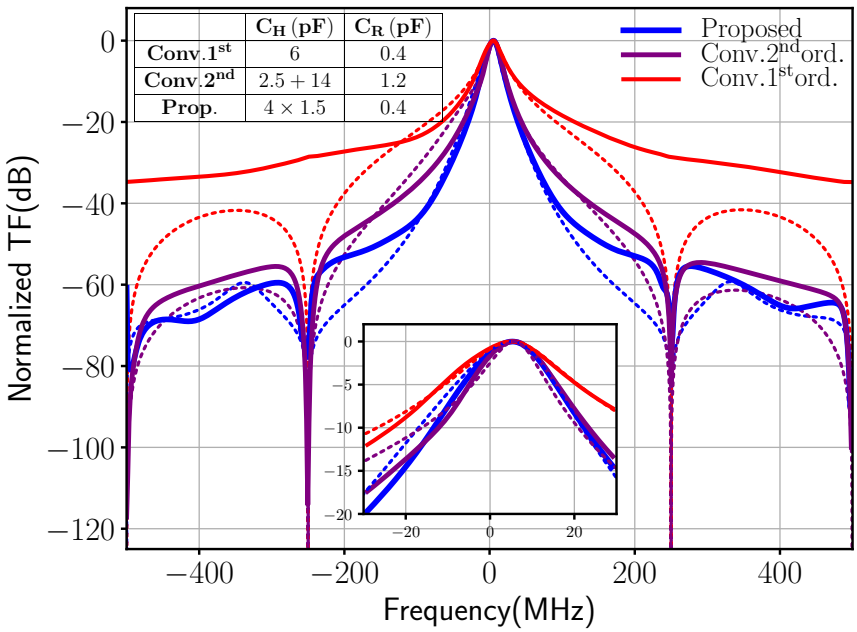


Figure 4.5: Simulated transfer functions of the conventional 1st/2nd-order BPF and the proposed BPF (dotted lines denote the corresponding analytical plots [i.e. Equations (4.1), (4.5), and (4.12)]. Constraints: sampling frequency f_s=250 MHz, center frequency f_c=6 MHz. Total history capacitance: $\sum C_H$=6 pF (1st-order), 16.5 pF (2nd-order), and 6 pF (proposed).

capacitance of 2.5 pF and 14 pF, respectively, is needed to maintain the same f_s and f_c. As another constraint, to keep the bandwidth of the 2nd-order filter similar to that of the proposed filter, its C_R has to increase to 1.2 pF, which is 3× of C_R of the proposed filter. This is expected since the pulse width must be narrowed by half just to keep the same f_s. Consequently, the total capacitance (thus, the occupied area) of history and rotating capacitors in the proposed BPF is less than half of that in the conventional 2nd-order BPF of similar in-band filtering characteristics, yet with better out-of-band filtering.

Figure 4.6 illustrates a similar comparison as in Fig. 4.5, but now the conventional 2nd-order architecture keeps its pulse width, $1/f_{ck}$, the same as in the proposed architecture, and its required input history capacitor is $C_{H,i}$= 4.8 pF (i.e. $C_{H,i} + C_{H,o}$= 6 pF). As discussed earlier,[1] f_c can be kept roughly constant when the sampling frequency, f_s, decreases by increasing the capacitor ratio, C_R/C_H (i.e. by decreasing C_H). As a result, if the pulse-width and f_c in the conventional 2nd-order architecture are maintained the same as in the conventional 1st-order one, the 2nd-order filtering is provided for the lower required history

[1]Later in Section 4.2.3, it will be shown that f_c of the proposed filter [derived as (4.14)] has a very similar relationship

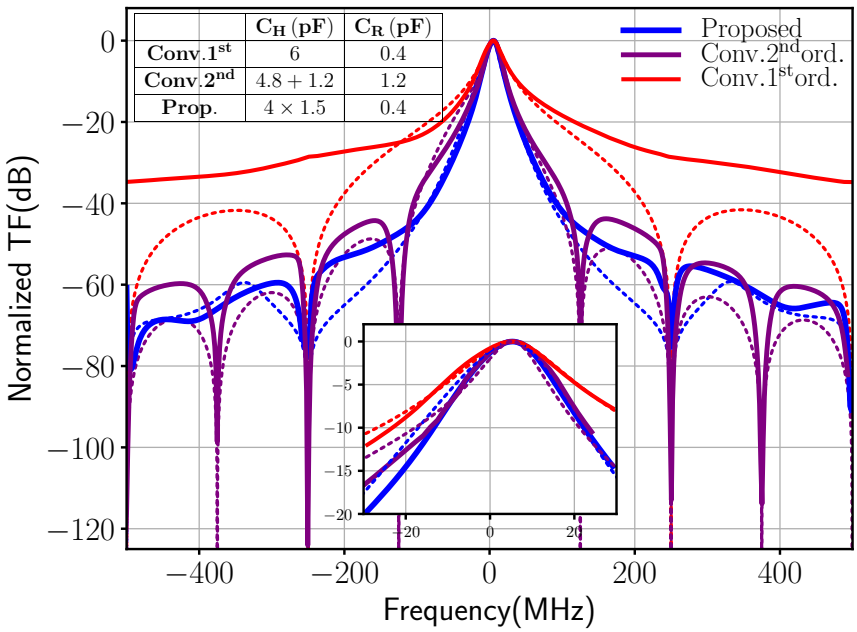


Figure 4.6: Simulated transfer functions as in Fig. 4.5 but with the conventional 2nd-order BPF decreasing its f_s to one-half. Total history capacitance: $\sum C_H = 6\,\text{pF}$ (1st-order), 6 pF (2nd-order), and 6 pF (proposed)

capacitance compared to Fig. 4.5, but at the expense of halving f_s, which would in turn possibly lead to pipelining just to be able to maintain the effective sampling rate, thus doubling the power consumption and area. The proposed clock-reuse filter still provides a comparable in-band/out-of-band filtering compared to this 2nd-order BPF operating at $f_s/2$=125 MHz. However, the out-of-band rejection of far-away frequencies and the aliasing at 125 MHz make the latter inferior.

4.2.3 Transfer Function Analysis

To help with deriving the transfer function (TF) of the proposed BPF, Fig. 4.4 is now redrawn in Fig. 4.7 with more details on the timing of the switches and charge sharing between the history and rotating capacitors. V_{11}, V_{21}, V_{31}, V_{41} designate the voltages on history capacitors C_{H1}, C_{H2}, C_{H3}, C_{H4}, respectively, in “arm I+".

After C_{H1} of “arm I+" gets disconnected from C_R at the end of ϕ_1, it gets charge-shared with C_{H2} during the next ϕ_4 phase. This local path operation gives rise to 1st-order low-pass filtering. Then, the charge on C_{H2} gets charge-shared with C_{H3} during the next ϕ_3 phase, also producing a local 1st-order low-pass filtering. The charge originally collected on C_{H1} moves

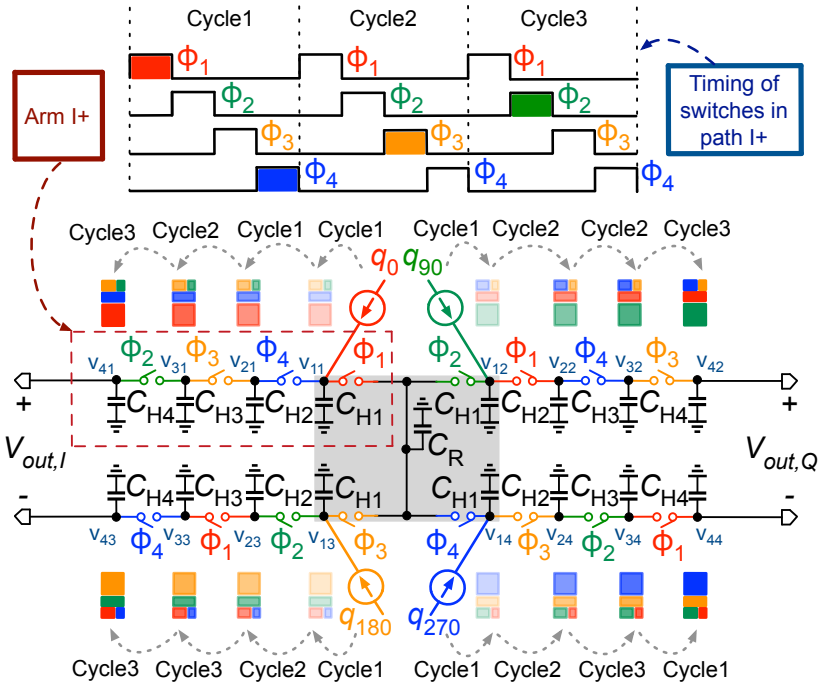


Figure 4.7: Charge-sharing operations in the proposed complex BPF.

in the direction from the input to output, experiencing a local 1st-order low-pass filtering at each stage. This charge-sharing operation eventually reaches the output when C_{H3} gets charge-shared with C_{H4} during the next ϕ_2 phase. Since the capacitors never get reset, the old history charge information also moves in the direction from the output to input (while experiencing the local low-pass filtering) to participate in the charge rotation among the quadrature paths, thus strengthening the band-pass filtering characteristic.

The timing diagram in Fig. 4.7 also reveals that this 3-stage directional charge-sharing path $C_{H1} \rightarrow C_{H4}$ is pipelined. For example, after C_{H1} gets charge-shared with C_{H2} during ϕ_4 so that the information can propagate towards the I+ output, a new "history" sample with the partial Q- information is available on the input capacitor, C_{H1}, for the same type of processing.

By concentrating on "arm I+" (see Fig. 4.7), the voltages on each node V_{11}–V_{41} are

calculated as:

$$
\begin{aligned}
@\phi_2 &: V_{41}[n-0] = \alpha_4 V_{41}[n-3] + (1-\alpha_4)V_{31}[n-1] \\
@\phi_3 &: V_{31}[n-1] = \alpha_3 V_{31}[n-3] + (1-\alpha_3)V_{21}[n-2] \\
@\phi_4 &: V_{21}[n-2] = \alpha_2 V_{21}[n-3] + (1-\alpha_2)V_{11}[n-3] \\
@\phi_1 &: V_{11}[n-3] = a_1 V_{11}[n-4] + a_1(1-a_1)V_{14}[n-4] + kq_0[n-3]
\end{aligned}
\tag{4.6}
$$

where α_{2-4}, a_1 and k are defined as:

$$
\begin{aligned}
\alpha_4 &= \frac{C_{\mathrm{H4}}}{C_{\mathrm{H4}}+C_{\mathrm{H3}}}, \quad \alpha_3 = \frac{C_{\mathrm{H3}}}{C_{\mathrm{H3}}+C_{\mathrm{H2}}} \\
\alpha_2 &= \frac{C_{\mathrm{H2}}}{C_{\mathrm{H2}}+C_{\mathrm{H1}}}, \quad a_1 = \frac{C_{\mathrm{H1}}}{C_{\mathrm{H1}}+C_R} \\
k &= \frac{1}{C_{\mathrm{H1}}+C_R}
\end{aligned}
\tag{4.7}
$$

z-domain equivalent of (4.6) is given as:

$$
\begin{aligned}
V_{41}(z) &= \alpha_4 z^{-3} V_{41}(z) + (1-\alpha_4) z^{-1} V_{31}(z) \\
V_{31}(z) &= \alpha_3 z^{-2} V_{31}(z) + (1-\alpha_3) z^{-1} V_{21}(z) \\
V_{21}(z) &= \alpha_2 z^{-1} V_{21}(z) + (1-\alpha_2) z^{-1} V_{11}(z) \\
V_{11}(z) &= a_1 z^{-1} V_{11}(z) + a_1(1-a_1) z^{-1} V_{14}(z) + kq_0(z)
\end{aligned}
\tag{4.8}
$$

As described in Section 4.2.1, the complex-valued input signal is defined as $q_{in} = (q_0 - q_{180}) + j(q_{90} - q_{270})$. Likewise, the complex-valued voltage developed in the first stage is defined as $V_1 = V_{1,I} + jV_{1,Q}$ where $V_{1,I} = V_{11} - V_{13}$ and $V_{1,Q} = V_{12} - V_{14}$. Moreover, according to Fig. 4.7, the relationship between the complex input and output of the first stage can be calculated as:

$$
\begin{aligned}
e^{0j\frac{\pi}{2}} \times \{V_{11} z^{-3}(1-a_1 z^{-1}) &= k z^{-3} q_0 + a_1(1-a_1) z^{-4} V_{14}\} \\
e^{1j\frac{\pi}{2}} \times \{V_{12} z^{-3}(1-a_1 z^{-1}) &= k z^{-3} q_{90} + a_1(1-a_1) z^{-4} V_{11}\} \\
e^{2j\frac{\pi}{2}} \times \{V_{13} z^{-3}(1-a_1 z^{-1}) &= k z^{-3} q_{180} + a_1(1-a_1) z^{-4} V_{12}\} \\
e^{3j\frac{\pi}{2}} \times \{V_{14} z^{-3}(1-a_1 z^{-1}) &= k z^{-3} q_{270} + a_1(1-a_1) z^{-4} V_{13}\}
\end{aligned}
\tag{4.9}
$$

By summing the terms on the left and right sides of (4.9), the complex transfer function

of the first stage (i.e the gray area shown in Fig. 4.7) is verified to agree with (4.1), where coefficient a is replaced with a_1.

By simplifying (4.8), the relation between V_{11} and V_{41} in "arm I+" is calculated as:

$$V_{41} = \frac{(1-\alpha_2)(1-\alpha_3)(1-\alpha_4)z^{-3}}{(1-\alpha_4 z^{-3})(1-\alpha_3 z^{-2})(1-\alpha_2 z^{-1})} V_{11} \tag{4.10}$$

Figure 4.7 illustrates that $V_{out,I} = V_{41} - V_{43}$ and $V_{out,Q} = V_{42} - V_{44}$, hence $V_{out} = V_{out,I} + jV_{out,Q}$. Since the amount of the old history charge information which moves from the output to the input is not high, the overall transfer function is a cascade of two transfer functions:

$$H(z) \approx \frac{V_{out}}{V_1} \times \frac{V_1}{q_{in}} \tag{4.11}$$

By using (4.1), (4.10) and (4.11), the transfer function of the proposed filter is derived as:

$$H(z) \approx \frac{V_{out}}{q_{in}} = \frac{(1-\alpha_4)(1-\alpha_3)(1-\alpha_2)kz^{-3}}{(1-\alpha_4 z^{-3})(1-\alpha_3 z^{-2})(1-\alpha_2 z^{-1})\left[1 - a_1 z^{-1} - ja_1(1-a_1)z^{-1}\right]} \tag{4.12}$$

$$H_{m,\varphi}(z) \approx \frac{k(1-\alpha)^{m-1} z^{-(m-1)}}{(1-\alpha z^{-(m-1)})(1-\alpha z^{-(m-2)}) \cdots (1-\alpha z^{-1}) \left[1 - a_1 z^{-1} - a_1(1-a_1) z^{-1} e^{j\frac{2\pi}{m}}\right]} \tag{4.13}$$

Calculating the center frequency for the proposed clock reusing technique is very complicated since there are other poles which influence f_c. By considering some simplifications, the center frequency is approximately defined as:

$$f_c \approx \frac{f_s}{2\pi} \arctan\left(\frac{(1-a_1)\cdot \sin(2\pi/4)}{1 + \cos(2\pi/4) - a_1 \cos(2\pi/4)}\right) \tag{4.14}$$

A significant attenuation could be introduced if there would be a charge loss due to a reset, like in a charge-sharing discrete-time LPF filter, such as [104]. There is no reset in the proposed charge-sharing discrete-time BPF. Charge sharing by itself does not result in any significant attenuation of the in-band transfer function, other than due to the constructive cancellation of charge by means of *indirect* charge sharing of positive/negative signal polarities

(i.e. I+ with I-, and Q+ with Q-). However, that is small in a properly designed DT BPF.

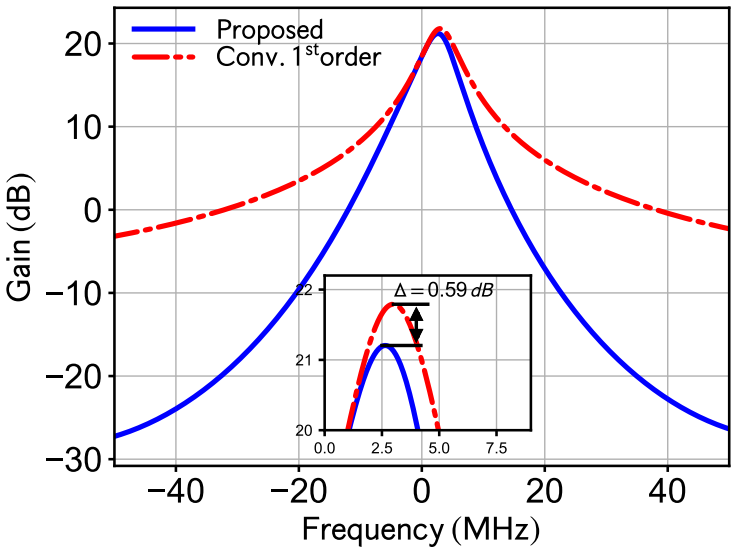


Figure 4.8: Analysis of the *non-normalized* gain based on (4.12) and (4.1) (conditions: $g_m = 1\,mS$, $\alpha_1 = 0.93$, $\alpha_2 = 0.5$, $\alpha_3 = 0.5$, $\alpha_4 = 0.5$, $k = 0.23(pF)^{-1}$, $f_s = 250\,MHz$)

To examine the gain difference between the proposed filter and the conventional first-order one (see Fig. 4.2), the absolute value of non-normalized gain, $A_v = (g_m T_s)^2 |H(z)|^2$, is shown in Fig. 4.8. To doing so, the value of the coefficients k and α_1 in (4.1) is considered the same as k and α in (4.12). The coefficients α_{2-4} are considered equal. According to Fig. 4.8, the gain difference between the conventional filter and the proposed one is less than 1 dB.

As a follow-up to the development in [96], which considered further extensions to the quadrature signaling system, such as octal, the generalized transfer function of the proposed filter for M elements, which gives the phase shift of $\varphi = 2\pi/M$ between neighboring paths, is calculated in (4.13). To keep the equation manageable, it considers all coefficients to be equal, $\alpha_2 = \cdots = \alpha_m = \alpha$.

The efficacy of the proposed clock-reuse technique of Fig. 4.7 is illustrated by superimposing the transfer-function SPICE circuit simulation plots of the three filters in Figs. 4.5–4.6 on the derived analytical plots: formulas (4.1), (4.5), and (4.12), respectively, for the conventional 1st- and 2nd-order and the proposed filter. The mismatch is less than 1 dB within 50 MHz offset frequency. Moreover, the stop-band rejection of the proposed filter improves more than 10 dB within 50 MHz offset compared to the 1st-order conventional BPF for the same total occupied silicon area (assuming the same capacitor density) and the same number of clock

phases.

The charge-sharing IIR filters are quite robust to the overlap between the clock phases [104, 107]. Simulation results show that for a 50 ps overlap between two successive phases, the filter characteristic (in-/out-of-band TF) does not change except for a 0.57 dB variation in the gain.

4.2.4 Noise Analysis

The noise analysis of the 1st-order complex charge-sharing BPF of Fig. 4.2 was discussed in detail in [108]. By further defining $b = (1 - a)$, while $a = C_H/(C_H + C_R)$, the power spectral density (PSD) of the differential output V_{out} noise is derived as:

$$\overline{V_{n,1}^2}(\omega) = \frac{2b^2\left[b\cos^2\left(\frac{\omega}{f_s}\right) - a\cos\left(\frac{\omega}{f_s}\right) + a^2\right]\cdot\frac{kT}{C_R f_s/2}}{(b^2+a^2)\cos^2\left(\frac{\omega}{f_s}\right) + (2b^3-4b^2+4b-2)\cos\left(\frac{\omega}{f_s}\right) + a^2\,(b^2+1)} \tag{4.15}$$

To calculate noise of the proposed filter, the input charge packets are assumed zero and the noise of each switch is considered as an uncorrelated voltage-noise source. The impact of each noise source is first individually considered at the output; then all calculated noise contributions are summed up at the output node. The noise of the first stage, calculated as $\overline{V_{n,1}^2}(\omega)$ in (4.15), will undergo the transfer function defined in (4.10) when reaching the output. The output noise PSD is therefore:

$$\overline{V_{out,n}^2} \approx \left[\frac{(1-\alpha_2)(1-\alpha_3)(1-\alpha_4)z^{-3}}{(1-\alpha_4 z^{-3})(1-\alpha_3 z^{-2})(1-\alpha_2 z^{-1})}\right]^2 \overline{V_{n,1}^2} \tag{4.16}$$

The noise statistics of the switches in the 2nd, 3rd, and 4th stages are the same in each path. Although all switches will contribute noise, the stages past C_{H1} will see large capacitance so their contributions will be much lower. Hence, the dominant noise at the output is the noise generated due to the switch of the first stage. Consequently, the total output noise PSD at the output is approximately equal to (4.16).

Figure 4.9 compares the output noise PSD of the proposed complex charge sharing BPF and the 1st-order complex BPF. The extra low pass filter due to the proposed clock reusing technique further suppresses the total noise of the proposed complex filter. By increasing the

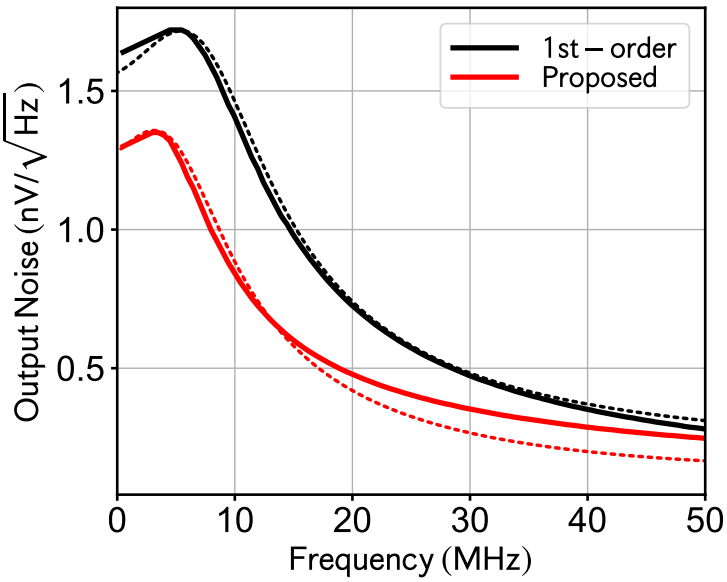


Figure 4.9: Simulated and calculated noise of the 1st-order and proposed BPF [dotted curves correspond to Eqs. (4.15) and (4.16), respectively]. Conditions: 1st-order BPF: $C_H = 18\,\text{pF}$, $C_R = 3\,\text{pF}$. Proposed BPF: $C_{H1} = 18\,\text{pF}$, $C_{H_{2-4}} = 1.5\text{pF}$, $C_R = 3\,\text{pF}$. $f_s = 1\,\text{GHz}$.

clock frequency, the peak gain is expected to drop, consequently, the noise performance will obviously deteriorate a bit at higher clock frequencies. However, the level of noise is still very low.

4.3 Circuit Implementation

The proposed high-order charge-sharing complex DT BPF is constructed using gm-stages, switches, capacitors and rail-to-rail clock waveform generator circuitry. It is, therefore, amenable to the digital deep nanoscale CMOS technology and each technology node advancement will improve the speed and reduce the area of these building blocks according to the Moore's law of scaling.

Figure 4.10 reveals the circuit diagram of the implemented design. The clock waveform generator receives an input signal CLK_{in} and generates the quadrature clock phases ϕ_1 through ϕ_4. They are used by the switched capacitor network to process the incoming quadrature signals converted to charge, q_0, q_{180}, q_{90}, q_{270}, according to the intended high-order complex band-pass filtering.

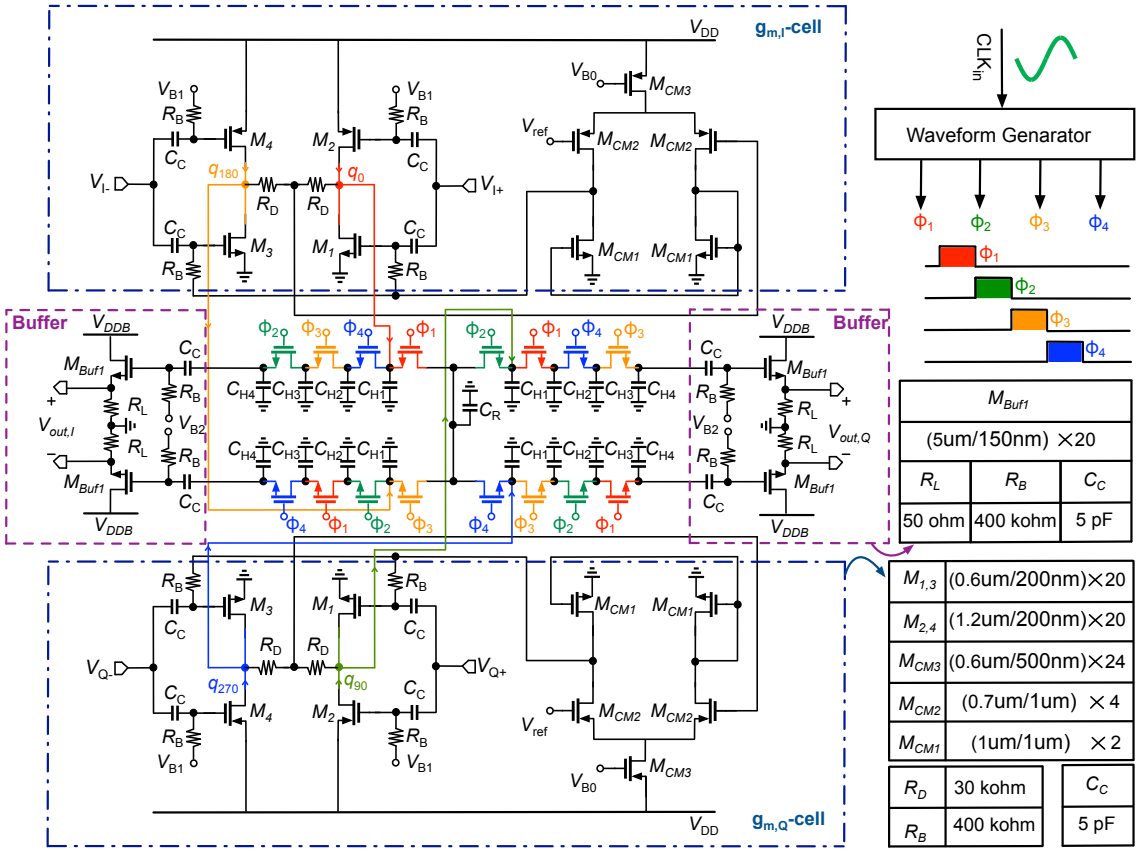


Figure 4.10: Architecture the proposed complex band-pass filter.

4.3.1 Filter

The filter's switches are implemented with NMOS-only transistors. Since they present lower parasitic capacitance at the gates compared to the transmission gate and bootstrap structures, their working frequency can be maximized. The size of NMOS transistors is chosen as a trade-off between the desire for low on-resistance, R_{on}, and the avoidance of charge injection and clock feedthrough. By increasing the size, we can achieve lower R_{on}, but the parasitic capacitance, i.e. gate-drain, C_{gd}, and gate-source, C_{gs}, increases. As a result, the clock feedthrough will increase. Moreover, as shown in [7], non-zero R_{on} resistance of the switches in switch- capacitor FIR and IIR filters has less impact on the overall TF. It slightly deteriorates the TF around the nulls (i.e. at nf_s, $n = 1, 2, \dots$). However, the transistor switches should be sized carefully to have sufficiently low R_{on} for fast settling on the sampling capacitors. Hence, they are chosen as low-V_T devices.

It is noteworthy that the parasitic capacitances slightly increase the size of C_H's and C_R,

consequently reducing the center frequency and bandwidth of the filter. These parasitics are much smaller than C_H's and C_R ($\ll 50\,fF$). However, this type of filter generally has the tunability feature (when it applies to RX), by changing the control bits of C_H's and C_R, any changes due to the parasitics in f_c can be compensated.

Metal-oxide-metal (MOM) capacitors are used for all the history and rotating capacitors. They use standard metal interconnect layers and can provide excellent matching. They are designed here based on a minimum capacitor unit cell of 100 fF. Moreover, they are implemented as two single-ended capacitors for differential path (in [110, 111] C_H is implemented differentially). Since the tuneability of a complex BPF has been already proven in [96, 108] and this design is pad limited, we only have one bit available to digitally change the C_H capacitance for the purpose of demonstrating the adjustability of center frequency. All C_{H1-4} values are the same and they are simultaneously controlled by one switch between 0.5 pF and 4.5 pF. We keep the value of C_R=0.5 pF fixed in this design since it helps to better maintain the gain, linearity, and noise in face of the changes in C_H.

4.3.2 Gm Stage

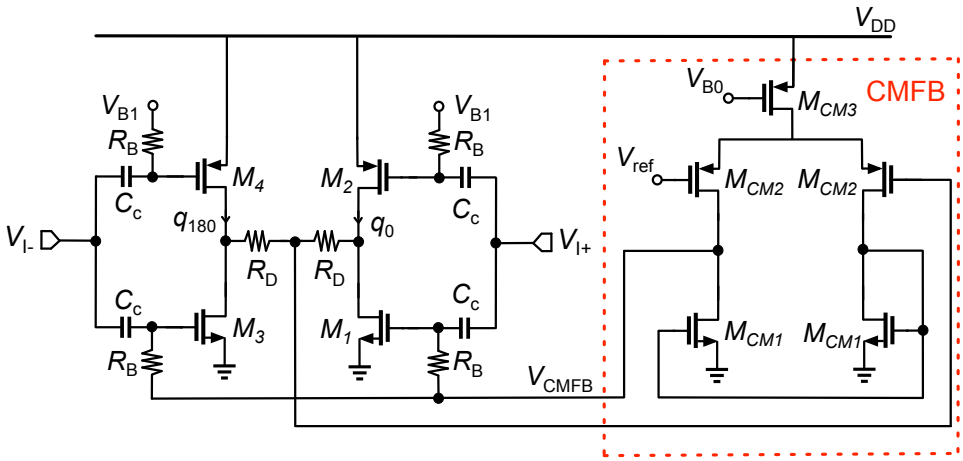


Figure 4.11: g_m cell.

As shown in Fig. 4.10, the differential I/Q input signals (V_I^+, V_I^-,V_Q^+, V_Q^-) are fed to the $g_{m_{I/Q}}$-cells which convert them to the charge domain as inputs q_0, q_{180}, q_{90} and q_{270}. The pseudo-differential g_m-cell compromises a pair of complementary long-channel thick-oxide PMOS/NMOS transistors to increase the transconductance linearity [58] and to make their

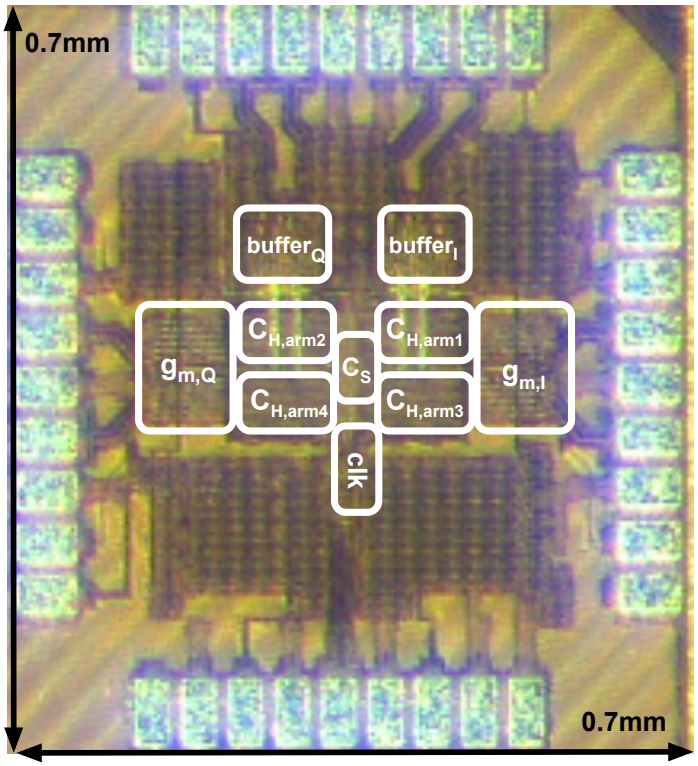


Figure 4.12: Microchip photograph.

behavior closer to the square-law model. A bias voltage V_{B1} to the PMOS transistors is supplied externally. A common-mode feedback (CMFB) ($M_{CM_{1-3}}$), shown in Fig. 4.11, sets the common-mode output voltage to $V_{DD}/2$ by adjusting the V_{CMFB} bias of the NMOS transistors. In the CMFB circuitry, the voltage at the output of the g_m-stage, M_1 and M_3 (M_2 and M_4) is sensed and compared with V_{ref}. Then through the feedback path, the bias voltage of M_1 and M_3 is set, accordingly. AC-coupling capacitors (C_c) and bias resistors (R_B) define a lower limit of the frequency response. By means of large C and R_B, the corner frequency of this high-pass filter (HPF) is well below the center frequency of the proposed BPF filter (i.e 500k kHz).

By properly sizing the NMOS and PMOS transistors (see Fig. 4.10), their second-order nonlinearities could be canceled out (although only partially in nanoscale CMOS), resulting in better linearity performance [85]. The output resistance of the g_m-cell should be at least 3× higher than $R_{eq} = 1/(2\pi f_s C_R)$ to ensure the integrity of the $q_{0,90,180,270}$ charge packet injection and to preserve the Q and bandwidth of the following CS-BPF.

4.3.3 Clock Generator

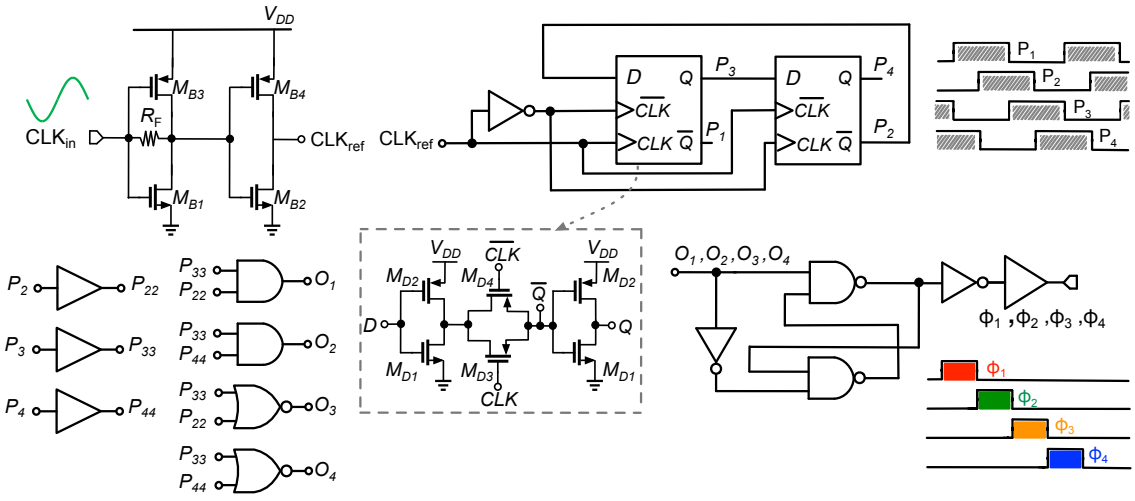


Figure 4.13: Clock generator circuitry.

Fig. 4.13 presents the clock generation circuitry employed to drive the BPF switches as $\phi_1 \sim \phi_4$ phases with 25% duty-cycle clocks. The external AC-coupled high-frequency (>1 GHz) sine-wave input signal is converted to a square-wave through the input buffer (i.e $M_{B_{1-4}}$). The input buffer consists of two stages of back-to-back inverters, where the first stage is self-biased with a fairly large feedback resistor R_F (50 kΩ). The transistor sizes in both stages are the same and are chosen by considering the trade-off between power consumption and the sufficient strength to load the parasitic capacitances of the loading stage (see Table 4.1).

The 50% duty-cycle square-wave CLK_{ref} and its inverted version, $\overline{\text{CLK}}_{\text{ref}}$, are sent to the ÷2 divider which consists of two D flip-flops (FF) arranged in the loop to generate the P_{1-4} clocks of 50% duty cycle with 25% delay between the adjacent edges. Since the proposed filter is capable of runing at high clock frequency CLK_{ref} (up to 4 GHz), the high-speed D-FFs are used in the divider stage, as shown in Fig. 4.13. Its transistor sizes are shown in Table 4.1. By means of the generated divider waveforms, $P_{2,3,4}$, and a few AND and NOR gates, the 25% duty-cycle waveforms O_{1-4} are constructed. The CS-BPF switches are driven by the ϕ_{1-4} clocks directly generated through the non-overlapping block, as illustrated in Fig. 4.13. It comprises NAND gates and the chain of inverters for proper driving of the load capacitance of NMOS switches.

It was demonstrated in [7] that a switch-capacitor structure is robust to non-idealities,

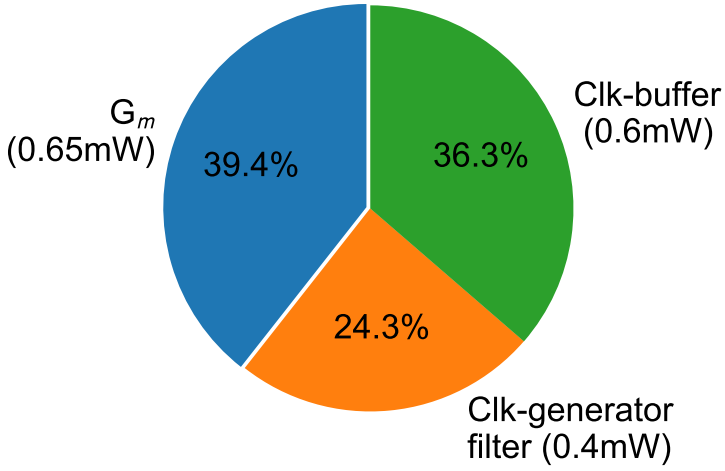


Figure 4.14: Power consumption break-down.

such as charge injection, nonzero rise/fall times of the clock, and clock jitter.

4.3.4 Test Buffer

Finally, an on-chip output test buffer is used to drive the 50 Ω load of the measurement equipment. As shown in Fig. 4.10, the output buffer is a pair of pseudo-differential source-follower amplifiers for both I and Q outputs, each having a R_L=50, Ω resistor at its source. The transistors are wide long-channel devices to provide minimum loss. Moreover, the AC-coupling capacitor, C_c, and bias resistor, R_B, create a high pass filter of 500 kHz cut-off frequency.

4.4 Measurement Results

The proposed I/Q BPF, whose chip micrograph is shown in Fig. 4.12, is fabricated in TSMC 28-nm LP CMOS. The design occupies merely 0.1 mm^2 of active area.Thanks to the proposed clock-reuse technique, it achieves remarkably high stop-band rejection in spite of

Table 4.1: Device dimensions of the input buffer and and D-FF of the clock generator.

$M_{B1,2}$	(0.6 μm/30 nm)×4	M_{D1}	(0.5μm/30 nm)×1
$M_{B3,4}$	(1μm/30 nm)×4	M_{D2}	(0.78 μm/30 nm)×1
R_F	50 kΩ	M_{D3}	(1.5μm/30 nm)×1
–	–	M_{D4}	(1μm/30 nm)×1

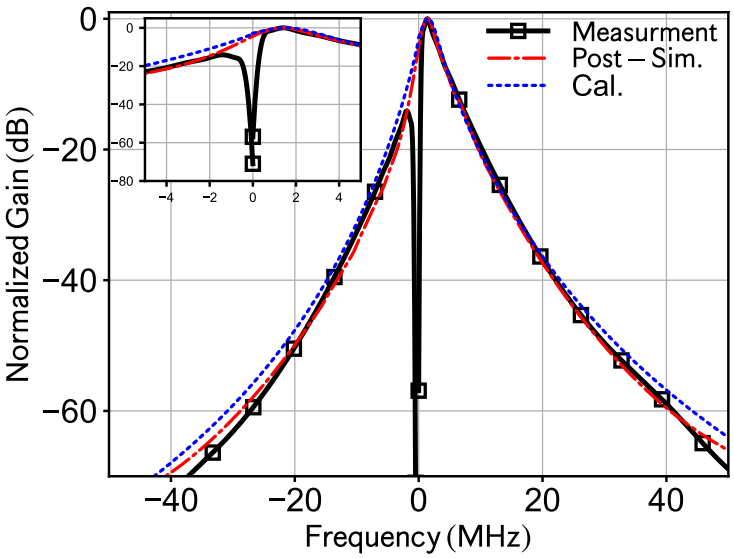


Figure 4.15: Measured TF for the maximum value of C_H with superimposed SPICE simulated and theoretical curves. The gain is 16 dB. Conditions: $C_{H_{1-4}}$= 4.5 pF, C_R= 0.5 pF, f_s= 500 MHz.

the conventional 25%-duty-cycle clocks.

The filter operates at 1 V and consumes 1.65 mW in total (excluding the test buffer, which consumes 9 mW). The power consumption breakdown is shown in Fig. 4.14 where the g_m-cells and waveform generator burn 0.65 mW and 1 mW, respectively. However, only 40% of the clock generator power consumption (i.e. 24.3% of the total) is used in the clock generator circuitry, the rest, i.e. 60% of it or 36.3% of the total) is due to the I/O functionality of its input buffer.[1]

To measure the proposed complex-valued filter, each single-ended I/Q input signal provided by a Keysight Waveform Generator 33600A is converted to differential through a wideband transformer on the printed circuit board (PCB), which is then terminated with a 50 Ω resistor. Moreover, the differential output of each I/Q arm is converted back to single-ended by another on-PCB transformer and the I/Q output signal is read via a Rohde & Schwarz FSM200 spectrum analyzer.

Figure 4.15 shows the measured normalized frequency response. The results are compared with post-layout simulation of the entire circuit including the input g_m stages and output buffers. Moreover, the ideal mathematical transfer function (4.12) is superimposed. The measurement actually indicates a few dB better filtering at higher frequency offsets than

[1] In the intended SoC application, the clock signal does not come through I/O pads and is rather generated internally.

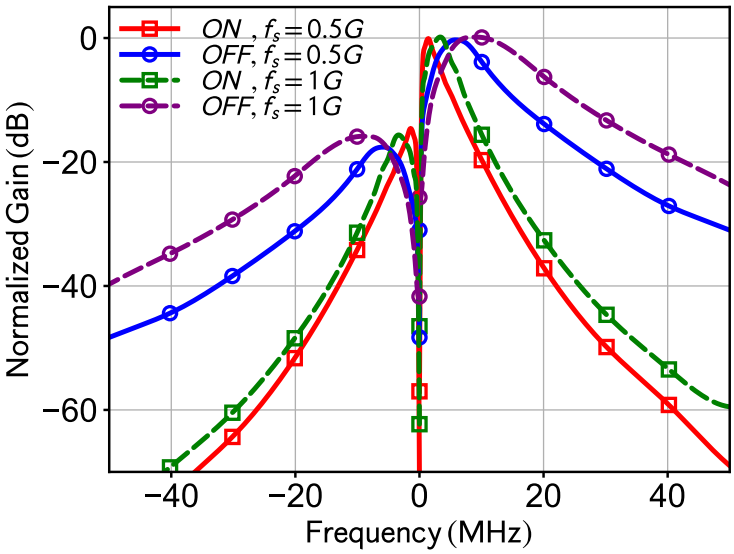


Figure 4.16: Measured TF for different center frequencies and bandwidths (ON mode: $C_{H_{1,4}}$=4.5 pF, C_R=0.5 pF. OFF mode: $C_{H_{1,4}}$=0.5 pF, C_R=0.5 pF).

predicted. The stop-band rejection is more than 70 dB for the highest history capacitor value at a 50 MHz offset (limited only by our current lab equipment) from its center frequency of 1.6 MHz. It is worth mentioning that the notch at dc is due to the high-pass characteristic of the dc-blocking capacitor, C_c in the g_m-cell (see Fig. 4.11).

To showcase the reconfigurability of the center frequency and bandwidth of the proposed BPF, the measured transfer function (TF) for different sampling frequencies f_s is illustrated in Fig. 4.16. As mentioned before, the clock frequency f_{clk} is 4× larger than the sampling frequency f_s, where f_s =1 GHz is achieved when f_{clk} runs at 4 GHz, which is the highest measured for this structure. Moreover, by changing the C_H/C_R ratio, the center frequency and BW can be tuned. As mentioned before, due to the pad/core-limitation, there is just one bit to show that the filter f_c and BW are tunable by changing C_H.

The noise of the filter is evaluated by the spectrum analyzer. For this measurement, the input of the filter is grounded and the output noise is measured. The input-referred noise of the proposed filter is illustrated in Fig. 4.17 for a 10 MHz bandwidth. The flicker noise and bias noise of the g_m-cell dominate at the lower frequencies, while at the higher frequencies the kT/C noise shaped by the filter's transfer function is dominant.

Shown in Fig. 4.18 is the out-of-band IIP3 measured by applying a two-tone test at the chip input. The out-of-band two-tone frequencies are at ∼50 MHz with a 2.5 MHz spacing

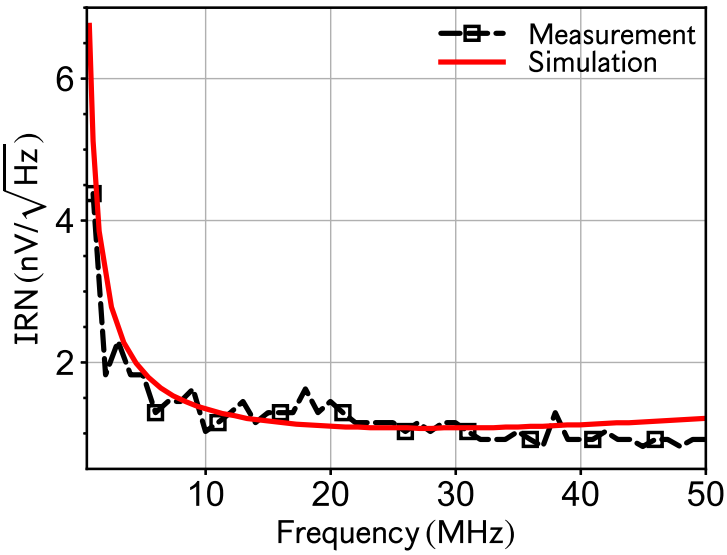


Figure 4.17: Measured noise with superimposed SPICE simulated curve.

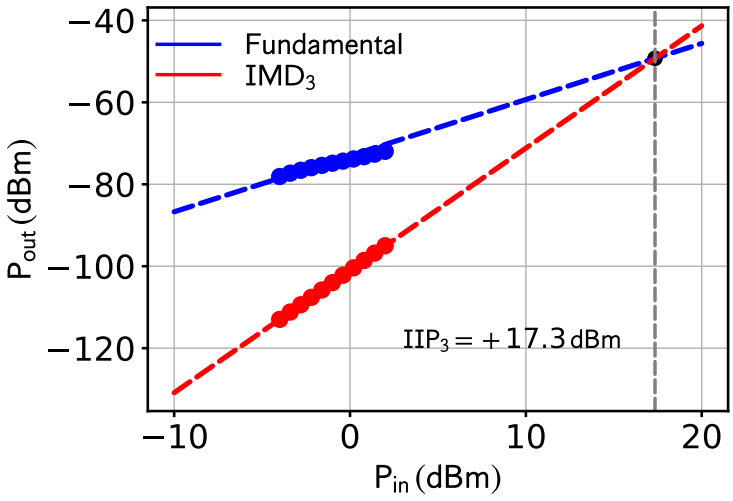


Figure 4.18: Measured out-of-band IIP3.

to have enough filtering at the output. The measured IIP3 is +17.34 dBm. Moreover, the in-band IIP3 is measured using a two-tone test at 2 MHz with 1 MHz spacing. According to Fig. 4.19, the in-band IIP3 of +2.46 dBm is achieved. It is worth mentioning that the linearity of the g_m-cell is the main limitation of IIP3. Notably, the charge-sharing part of the complex band pass filter achieves a much higher IIP3 value (i.e. +29.1 dBm per simulations).

Performance of the proposed band-pass filter is compared with prior-art architectures in Table 4.2 including six prior-art complex-valued BPFs and one LPF. Based on the reported measured filtering characteristics, Figure 4.20 summarizes the amount of stop-band rejection

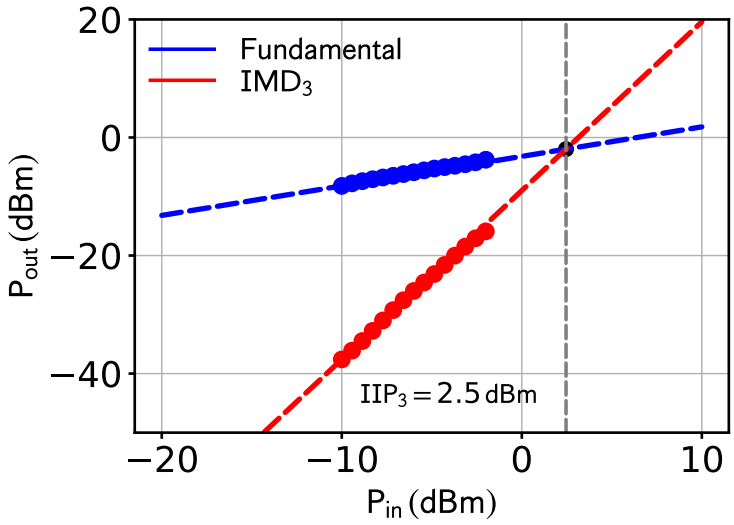


Figure 4.19: Measured in-band IIP3.

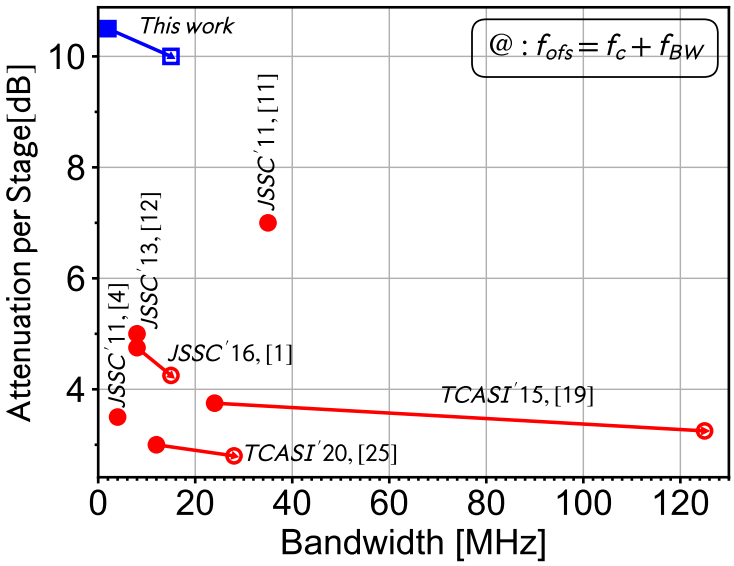


Figure 4.20: Extracted out-of-band rejection of reported BPFs at an offset frequency of one bandwidth, BW, away from center frequency, f_c, for minimum and maximum bandwidths. Note that in [99, 102, 103] the bandwidth is fixed.

per stage at an octave frequency offset with respect to the 3-dB (two-sided) bandwidth away from the center frequency (i.e $f_{\text{ofs}} = f_{\text{c}} + f_{\text{BW}}$). For the tunable filters, both the minimum and maximum BWs are reported in the plot and in Table 2.1. Our BPF shows the highest out-of-band rejection while offering the overall best-in-class performance at the lowest consumed power.

4.5 Conclusion

In this chapter, a band-pass complex IIR filter was proposed and experimentally verified in TSMC 28-nm LP CMOS. It takes advantage of a clock-reuse technique that facilitates its operation at high clock frequencies, while providing a high stop-band rejection, and bandwidth tunability. As a result, the proposed filter architecture is amenable for discrete-time receivers. Such receivers are typically difficult to design for applications that require relatively high performance filtering with high frequency clocks for generating multiple phases.

Table 4.2: Summary and comparison with state-of-the-art.

	CMOS [nm]	Type [-]	V_{DD} [V]	Power [mW]	IRN [nV/$\sqrt{\text{Hz}}$]	IB-IIP3 [dBm]	OB-IIP3 [dBm]	BW [MHz]	f_c [MHz]	Att. @BW [dB][(g)]	# stages [-]	IMR [dB]	Active area [mm^2]
This work	**28**	**Complex-IIR 4 phase**	**1**	**1.65[(a)]**	**1**	**+2.5**	**+17.3**	**2~15**	**1.8~8**	10.5~10	1	**18**	**0.1**
[112] JSSC'2020	22 nm FDSOI	LPF AFIR[(b)]	0.7	0.092	12	–	-3[(f)]	0.06~3.4	–	–	–	–	0.09
[113] TCASI'2020	65	Complex-IIR 4 phase	1.2	7.5	26.5~35.4	9.7~ 12.5	-	12~28	35~70	6~5.6[(e)]	2	–	0.17
[96] JSSC'2016	28	Complex-IIR 16 phase	0.9	9.1[(c)]	–	–	+14	8~15 [(e)]	10~90	9.5~8.5[(e)]	2	65	0.52
[108] TCASI'2015	65	Complex-IIR 4 phase	1.2	28	1.5	0	+9.5	24~125	20~100	7.5~6.5[(e)]	2	10[(e)]	0.19
[103] JSSC'13	65	N-path 8 phase	1.2	18~57	0.87~0.93[(h)]	-12	+26	8	100~1200	15[(e)]	3	–	0.27
[99] JSSC'2011	65	M-phase 8 phase	1.2/2.5	39[(d)]	0.87[(h)]	–	-8.4	4	110	7[(e)]	2	–	0.76
[102] JSSC'2011	65	N-path 4 phase	1.2	2~20	0.9~1.3[(h)]	–	+14	35	100~1000	7[(e)]	1	50	0.07

[(a)] Output buffer is not included. [(b)] Low pass filter [(c)] Total RX power consumption is 22 mW [(d)] Total RX
[(e)] Estimated from plots. [(f)] Calculated from reported OIP3 in dB as IIP3 = OIP3 − Gain.
[(g)] Calculated offset frequency as $f_{ofs} = f_c + f_{BW}$. [(h)] Calculated from reported NF as IRN = $\sqrt{4kTR_s(10^{(NF/10)}-1)}$.

Chapter

5

Charge-Sharing Low-Pass IIR Filter with Enhanced Anti-Aliasing Filtering due to a Linear Interpolation Technique

This chapter continues with the baseband filtering and introduces a new architecture of a discrete-time charge-rotating low-pass filter (LPF) which achieves a high-order of filtering and improves its stop-band rejection while maintaining a reasonable duty cycle of the main clock at 20%. Its key innovation is a linear interpolation within the charge-accumulation operation. Fabricated in 28-nm CMOS, the proposed IIR LPF demonstrates a 1–9.9 MHz bandwidth programmability and achieves a record-high 120 dB stop-band rejection at 100 MHz while consuming merely 0.92 mW. The in/out-of-band IIP3 is +18.6/+26.6 dBm.

5.1 Introduction

Integrated low-pass filters (LPF) with strong rejection of out-of-band frequency components are essential building blocks in a variety of applications, such as telecommunications,

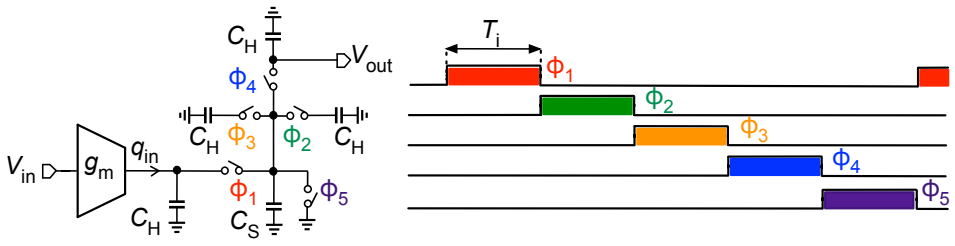


Figure 5.1: Conventional 4th-order charge-rotating IIR filter.

video signal processing, anti-aliasing filtering, etc. Attention is drawn toward structures featuring low noise, small area, high in-/out-of-band linearity performance, and low-power consumption. There are various techniques in building high-performance LPFs, including charge-rotating (CR) infinite-impulse response (IIR) [104, 114], analog finite-impulse response (AFIR) [112], filtering by aliasing (FBA) [115], and flipped/coupled source followers (FSF/CSF) [116], [117]. Among them, the discrete-time (DT) charge-rotating filters are becoming increasingly important since they rely on CMOS switches, inverters and capacitors, which all enjoy high process scalability [104]. They also offer hope in addressing one of the key remaining issues in advanced communication systems: the out-of-band rejection strength which is highly desired (e.g. in 5G wireless).

In the conventional charge-rotating IIR filtering, as illustrated in Fig. 5.1, the current is sampled over an integrating time window $T_i = 1/5f_s$. The resulting integrated charge is interpreted as a DT charge packet. The window integration acts like a zero-order hold (ZOH) on the charge, which forms a continuous-time (CT) $\mathrm{sinc}(\pi f/f_s)$ antialiasing filter. The DT charge samples are then low-pass filtered by a passive switched-capacitor circuit. By means of the sampling capacitor (C_S), the charge rotates between several history capacitors (C_H) leading to a high-order low-pass filtering. The order of filtering can be arbitrarily increased but at the cost of increasingly more clock phases and history capacitors [104].

Conceptually, if the ZOH is replaced with a first-order hold (FOH), whose frequency response is $\mathrm{sinc}^2(\pi f/f_s)$, its stop-band rejection will be substantially improved. This would lead to a better attenuation of unwanted signals folded from multiples of the sampling frequency, f_s. However, in practice, the realization of a linear interpolation is very challenging. In [118], a rectangular boxcar was convolved with itself to make a triangular response with a transfer function of $\mathrm{sinc}^2(\pi f/f_s)$. However, that technique requires another stage of the

charge sampling filter whose transconductance g_m-cell converts the voltage output of the first stage to the current and then integrates it into integrating capacitors for providing the second boxcar. This unfortunately leads to higher complexity and power consumption. Moreover, since the the number of sampling capacitors gets doubled, and they all need to be reset in both stages, the charge loss increase leads to a deterioration in signal-to-noise ratio (SNR).

In this chapter, we propose a new approach to implement the $\text{sinc}^2(\pi f/f_s)$ function by providing a *pseudo*-linear interpolation through an L-fold technique. Moreover, the history capacitor in each stage is dynamically changed to provide a higher-order of filtering. The proposed technique is applied to a 4th-order IIR LPF, leading to the highest out-of-band rejection among analog filters. The rest of the chapter is organized as follows. Section 5.2 describes the proposed low-pass filter. The circuit implementation is provided in Section 5.3. Finally, the measurement results are given in Sections 5.4.

5.2 Proposed Low-Pass Filter

An approximation to the triangular response is shown in Fig. 5.2(a). Instead of the integrating sampling capacitor C_S staying constant as in the conventional solutions, its capacitance gradually varies over time in discrete steps to approximate the linear response. The integrating phase ϕ_1 is split into five equal *sub*-phases to generate the three *active* sub-phases, ϕ_{IS1}, ϕ_{IS2}, and ϕ_{IS3}. The sampling capacitor, C_S, is split into 4 constituent capacitors, $C_S/3$,$C_S/6$, $C_S/6$ and $C_S/3$, as shown in Fig. 5.2. Enabling different combinations of the sampling capacitors during each of the sampling sub-phases allows varying the effective sampling capacitance over the integrating window, thus achieving the staircase approximation of a triangular sampling window. Moreover, the history capacitor also gradually increases in discrete steps. The capacitance change steps are carried out during the sub-phases $\phi_{\text{IH}_{1-3}}$ for the history capacitor and sub-phases $\phi_{\text{IS}_{1-3}}$ for sampling capacitor, all within the sampling period (T_s). The clocking scheme for enabling the constituent sampling capacitors is plotted in Fig. 5.3.

The new LPF in Fig. 5.3 is based on the conventional structure of Fig. 5.1 as a foundation for the proposed improvements. It replaces the fixed history and sampling capacitors in the conventional scheme with the dynamically variable C_H and C_S capacitors. Moreover, incrementally engaging the history capacitors $C_{\text{IH1}-3}$ during the sub-phases $\phi_{\text{IH}_{1-3}}$ further

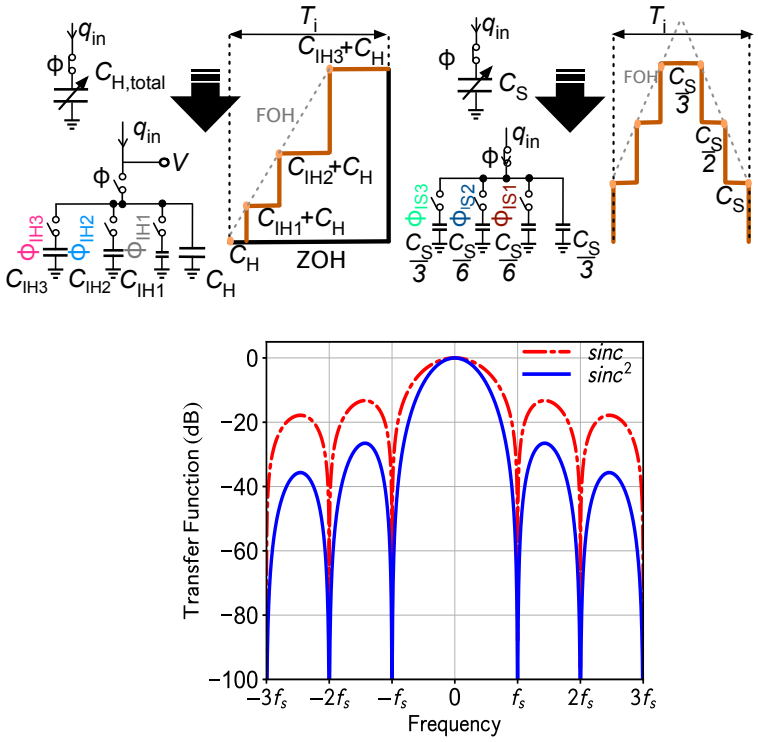


Figure 5.2: Idea of first-order-hold (FOH) and transfer function comparison of $\mathrm{sinc}(\pi f/f_s)$ and $\mathrm{sinc}^2(\pi f/f_s)$.

causes the charge to be dynamically shared between each C_H and its $C_{\mathrm{IH}_{1-3}}$, leading to a stronger filtering, specially at higher frequency offsets. However, the charge is not delivered to the output uniformly; it is conveyed in multiple steps (4-steps in this case) at a fraction of the sampling period, like in an L-fold linear interpolation [119]. Hence, the antialiasing transfer function is close to $\mathrm{sinc}^2(\pi f/f_s)$ for values of L above 2: as shown in Fig. 5.2, $\mathrm{sinc}^2(\pi f/f_s)$ improves the rejection at higher frequencies by around 20 dB as compared with just $\mathrm{sinc}(\pi f/f_s)$. It is worth mentioning that the sampling frequency is still beneficially maintained at f_s which is unchanged from the conventional 4th-order LPF. It should be noted that to improve the stop-band rejection in the conventional design, the order of filtering should increase by increasing the number of phases as well as increasing the sampling period, T_s (under the constraint of fixed duration of the individual phases).

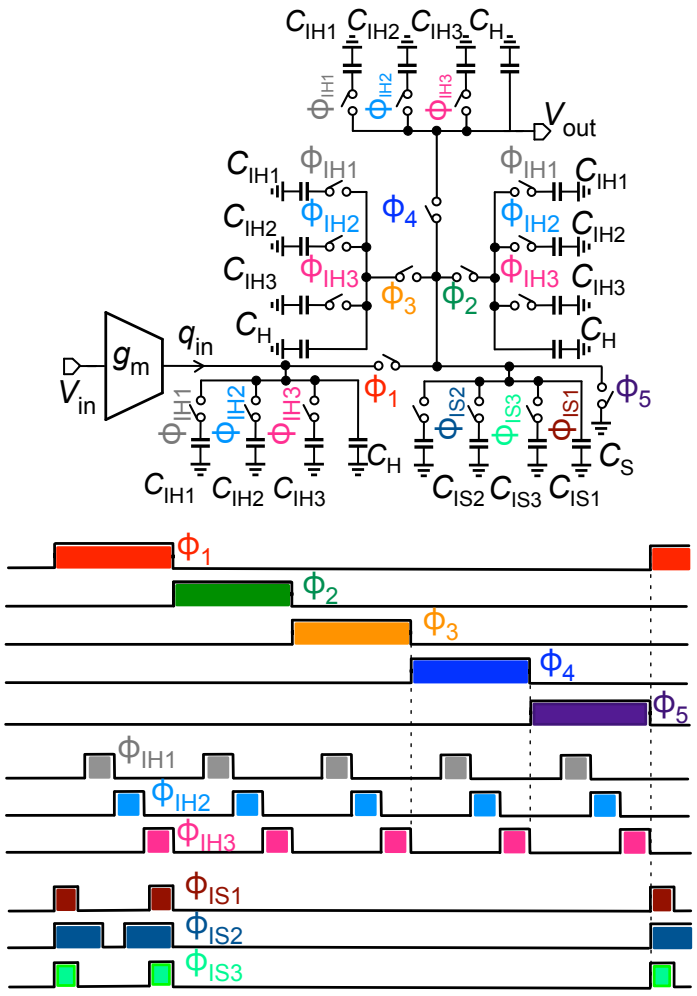


Figure 5.3: Proposed IIR filter with FOH, and its timing diagram.

5.3 Circuit Implementation

Implementation of the proposed 4th-order IIR filter is detailed in Fig. 5.4. The differential input V_I is converted to current by the pseudo-differential ac-coupled inverter-based g_m-cell. Its output dc voltage is set to $V_{\mathrm{DD}}/2$ by the common-mode feedback (CMFB) circuit. The current is integrated in the time-varying history capacitor, $C'_H = C_H + C_{IH1-3}$, and shared with the time-varying sampling capacitor, $C'_S = C_S + C_{IS1-3}$. Capacitor C_S samples the charge during the sampling phase of the IIR filter (i.e., ϕ_1) while its value changes during the sub-phases, as discussed in Section 5.2.

In each phase, C'_S shares the charge with other C'_H's. Finally, during the last phase, C_S is reset. Since this structure is reset just once per $1/f_s$ cycle, its noise degradation is kept at

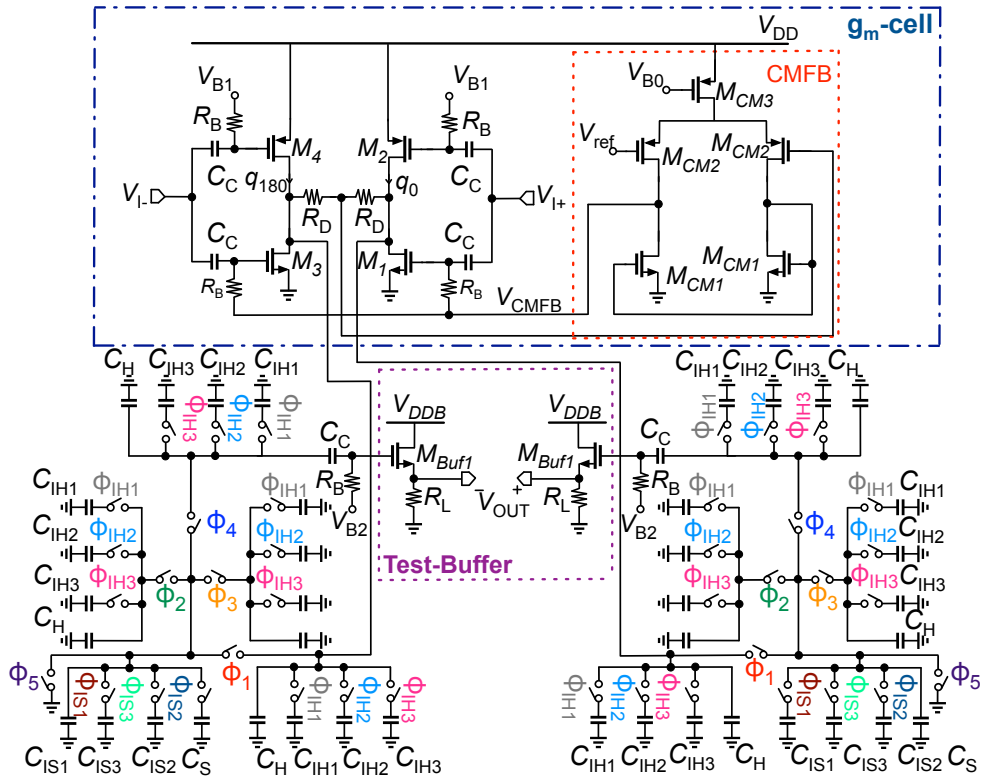


Figure 5.4: Full circuit implementation of the proposed low-pass filter. (The clock circuitry is shown in Fig. 5.5.)

minimum. During each main phase ϕ_{1-4}, the history capacitor is increased gradually with the additional capacitor bank of $C_{\mathrm{IH}1-3}$ during sub-phases $\phi_{\mathrm{IH}_{1-3}}$. This directly results in the improved out-of-band rejection compared to the prior art. Moreover, the bandwidth of the filter, defined by the ratio of C'_H/C'_S and f_s, is tunable.

Figure 5.5 illustrates the clock generator circuitry. The input sinewave signal at 2 GHz is injected to the waveform generator through an I/O buffer. The waveform generator produces three different clock phases including five main phases (i.e., ϕ_1, ϕ_2, ϕ_3, ϕ_4, ϕ_5) for the main functionality of the filter, three sub-phases for incrementally changing C'_H (i.e., ϕ_{IH1}, ϕ_{IH2}, ϕ_{IH3}), and three sub-phases to dynamically vary the value of C'_S (i.e., ϕ_{IS1}, ϕ_{IS2}, ϕ_{IS3}). It mainly consists of two sets of back-to-back circulating D-flip-flops, three in the first path and 20 in the second path. All required phases are generated through several gates.

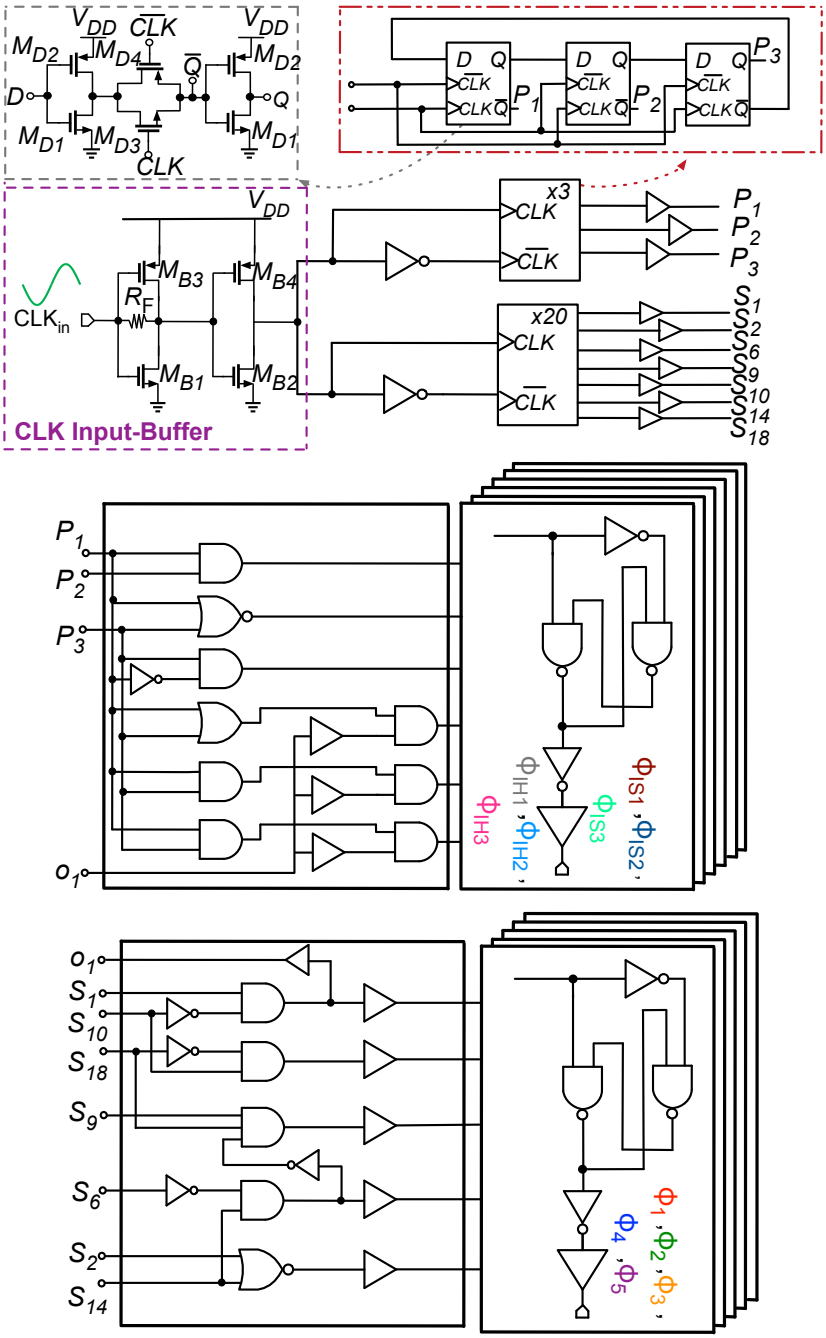


Figure 5.5: Circuit schematic of the clock generator circuitry.

5.4 Experimental Results

The proposed filter is realized in TSMC 28-nm LP CMOS. Fig. 5.6 shows the chip micrograph. The total chip area is 1.04 mm^2, with the active area occupying only 0.192 mm^2.

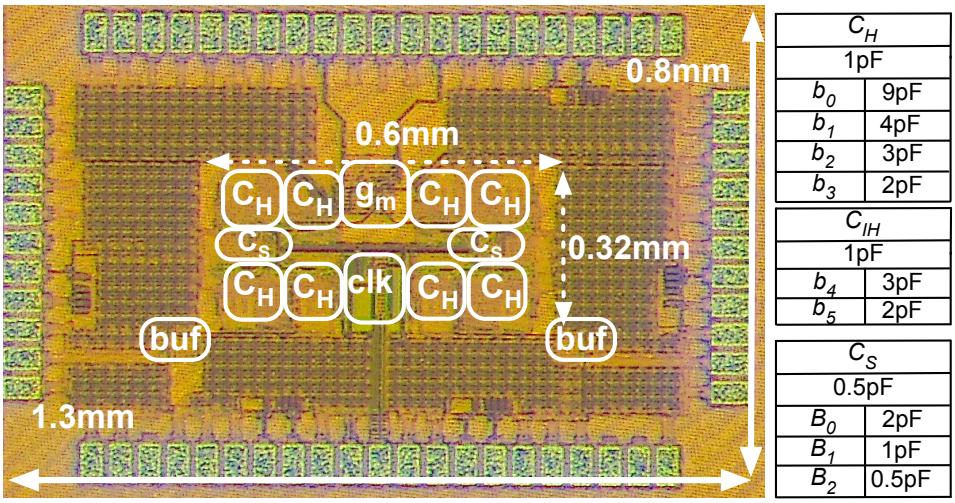


Figure 5.6: Chip micrograph.

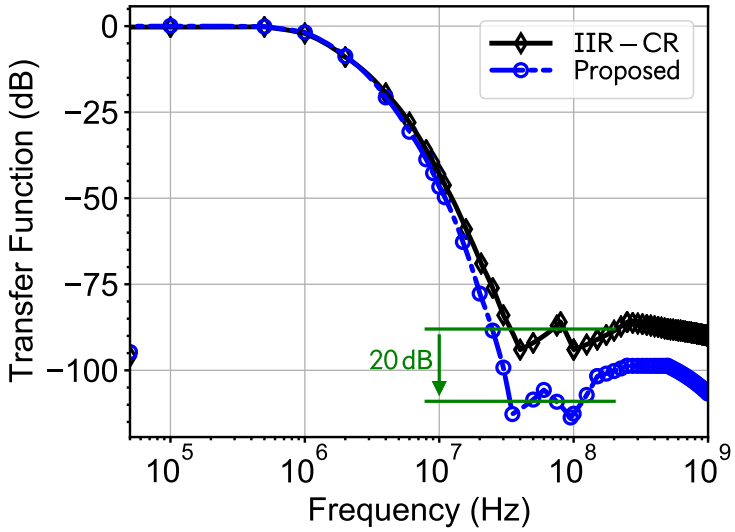


Figure 5.7: Measured normalized transfer functions in two filtering modes: conventional (see Fig. 5.1) and proposed, for the 3-dB bandwidth of 1 MHz.

All charge-rotating capacitors are implemented as binary-controlled MoM capacitors. To provide bandwidth tunability, sampling and history capacitors are digitally programmable by enabling/disabling the unit cells, with values listed in Fig. 5.6. The filter operates at 0.9 V and consumes 0.92 mW in total. The g_m-cell and 2-GHz waveform generator drain 0.32 mW and 0.60 mW, respectively. The power consumption of the external interface circuitry: input clock buffer and test output buffers is 1 mW and 7 mW, respectively.

Figure 5.7 shows the measured normalized transfer functions (TF) in the proposed and

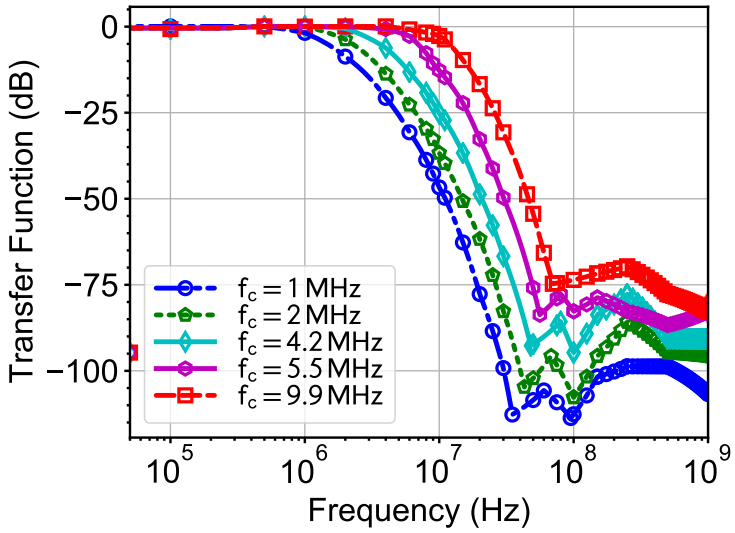


Figure 5.8: Measured normalized transfer functions: bandwidth programmability.

conventional modes. To keep the 3-dB bandwidth of both modes identical, the size of the history capacitors (C_H) in the conventional mode is chosen larger than the composite C'_H in the proposed mode. As shown, the out-of-band rejection improves by >20 dB. To demonstrate the filter's tunability, the TF was measured for different values of the history capacitor. Figure 5.8 shows the 3-dB bandwidth programmability of 1–9.9 MHz.

The in-band (out-of-band) IIP3 is measured in Fig. 5.9 using a two-tone test at 5 & 6 MHz (100 & 110 MHz). The achieved in-band (out-of-band) IIP3 is +18.6 dBm (+26.63 dBm).

Performance of the proposed filter is summarized in Table I and compared to state-of-the-art low-pass filters. It achieves the record-high stop-band rejection of 120 dB while providing best-in-class linearity and noise performance. The closest contender [104] achieved 100 dB stop-band attenuation by using a 7th-order filtering, but it requires more clock phases and consumes 2× the power. Besides featuring the best stop-band rejection, the proposed filter maintains better in-/out-of-band linearity, power consumption and noise performance compared to [115] and [120]. Although [112] achieves higher gain and lower power consumption using an analog finite-impulse response filtering technique (AFIR), its linearity and noise performances are significantly worse.

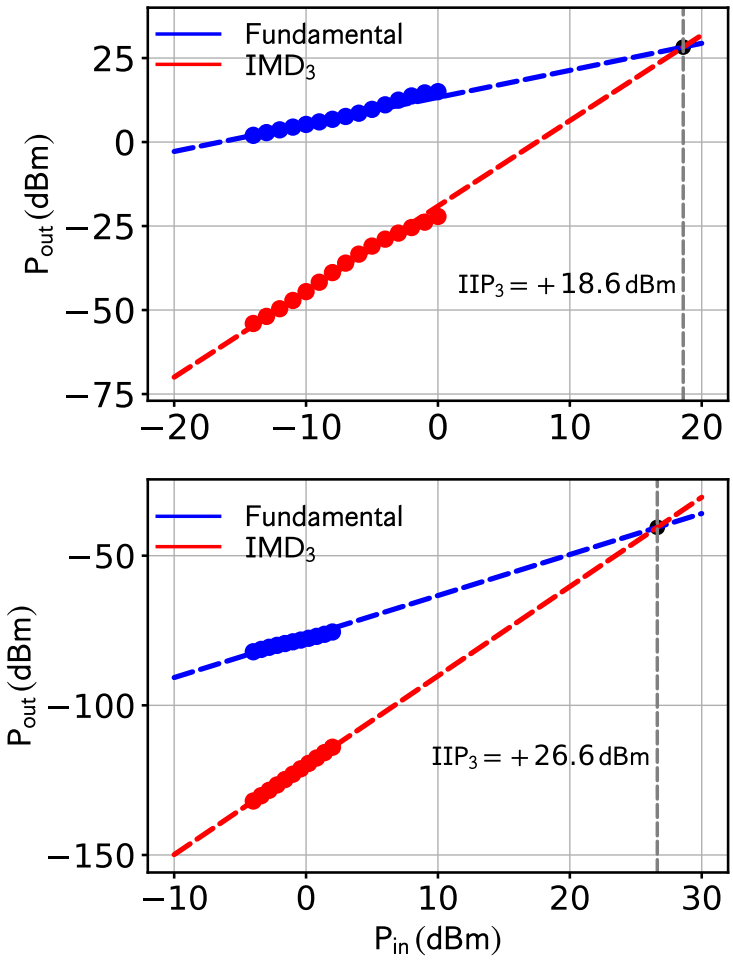


Figure 5.9: Measured IIP3: (top) in-band, and (bottom) out-of-band.

5.5 Conclusion

A new low-pass IIR filter was introduced and experimentally verified in 28-nm CMOS. It takes advantage of a new pseudo-linear interpolation technique that enhances the stop-band rejection while keeping the duty cycle of the clock the same as in the conventional CR-IIR filter. It also allows for an easy tunablity of the bandwidth. As a result, the proposed low-pass filter architecture appears a suitable candidate for various challenging applications, such as in discrete-time cellular receivers.

Table 5.1: Summary and comparison with state-of-the-art filters.

	This work	[104] JSSC'14	[115] ISSC'17	[114] VLSI'17	[116] ESSCIRC'18	[120] TCASI'18	[112] JSSC'20	[117] JSSC'20
Topology	CR-IIR	CR-IIR	FBA	CR-IIR	FSF	CR-IIR	AFIR	CSF
Technology [nm]	28 CMOS	65 CMOS	65 CMOS	130 CMOS	28 CMOS	180 CMOS	22 FDSOI	180 CMOS
Order	4th	7th	4th	3th	4th	4th	–	5th
BW [MHz]	1∼9.9	0.4∼30	2.5∼40	0.54	100	0.49∼13	0.06∼3.4	20
Max Stop-band Reject. [dB]	120	100	70	45**	60**	100	70**	80**
Gain [dB]	14.7	9.3	23	–	-2.6	17.6	31.5	0
IRN [nV/$\sqrt{\text{Hz}}$]	4.3	4.57	–	23.3	8***	6.54	12	15.3
IB IIP3 [dBm]	+18.6	+16	+8	–	+2.5∼+12.5	+11.1	–	+11.5∼+24.5
OB IIP3 [dBm]	+26.6	–	+21	+55.1	–	+15	-3.5*	–
VDD [V]	0.9	1.2	1.2	1.2	1	1.8	0.7	1.3
Power [mW]	0.92	1.96	76.8∼ 100.8	0.15	0.97	4.3	0.092	0.65
Active area [mm^2]	0.192	0.42	0.23	0.06	0.026	2.9	0.09	0.12

* Calculated from reported OIP3 in dB as IIP3 = OIP3 − Gain; ** Estimated from figure; *** Simulated result.

CHAPTER

6

Conclusion

In this dissertation, the design, analysis, modeling, and implementation of the *key* building blocks of a cellular receiver in the deep nano-scale CMOS process technology are discussed. Section 6.1 gives a short summary and repeats the accomplishments achieved. Since some parts of my research (the D/E-band all-digital transmitter and low-power Bluetooth discrete time receiver) are still undergoing measurements, Section 6.2 briefly mentions those. Finally, Section 6.3 proposes some suggestions for future work.

6.1 The Thesis Outcome

The superheterodyne receiver (RX) with resonant band-pass filters (BPFs) tuned at a fixed intermediate frequency (IF) was the architecture of choice over a period of several decades for wireless receivers constructed with external discrete components. With the invention of IC chip, the zero-IF architecture drew the RF designers' attention for making fully monolithic receivers due to its simplicity and cost reasons. The main advantage of the zero-IF architecture is that it does not require any bulky BPFs, which are needed in a

traditional superheterodyne RX for image rejection, and can instead rely on low-pass filters for channel selection, which are much easier to integrate in CMOS. However, that approach suffers from time-variant DC offset, limited IIP2, and a high flicker noise of devices.

On the other hand, since the superheterodyne architecture operates at high IF, it does not inherently suffer from the above problems. The main challenges towards a fully integrated superheterodyne receiver were the non-linearity of LNTA, especially in the FDD mode and the integration of IF bandpass filters. Both of them have been addressed in this work.

Moreover, while the transistor cutoff frequency (f_T) has improved dramatically with scaling, conventional RF/analog techniques, which were optimized for the older technology, do not effectively make use of the ultra-high speed of transistors of scaled CMOS to improve the system performance. In contrast, the DT RF/analog building blocks, such as a MOS switch, capacitor, gm-cell, and digital clock generator, benefit directly from scaling in terms of speed, power consumption and area. Therefore, an attempt was to use as much as possible the DT RF/analog or digital-like blocks throughout this dissertation. The DT implementation also reduces the performance sensitivity to the process variations.

In Chapter 2, a new noise reduction/cancellation technique is proposed to improve the noise figure (NF) of a broadband low-noise transconductance amplifier (LNTA) for 5G (sub-6 GHz) receivers. The LNTA combines a common-gate (CG) stage for wideband input matching and a common-source (CS) stage for canceling the noise and distortion of the CG stage. Yet another noise reduction is applied to reduce the channel thermal noise of the noise cancellation stage itself. The technique further exploits current reuse and increases transconductance of the CS transistor while keeping its power consumption low. Fabricated in 28-nm CMOS, the proposed LNTA is capable of driving an external 50 Ω load and achieves a NF of 2.09 dB to 3.2 dB and input return loss (S_{11}) better than –10 dB over the 3-dB bandwidth of 20 MHz to 4.5 GHz while consuming 4.5 mW from a single 1 V power supply. The achieved gain (S_{21}) and IIP3 are 15.2 dB and -4.6 dBm, respectively.

Chapter 3 discusses two wideband low-noise (transconductance) amplifiers (LN(T)A) where two novel two-fold noise cancellation schemes are proposed. Fine tuned for the advanced CMOS, the first proposed LNA architecture uses a common-gate input branch to provide wideband input matching. It is followed by two stages of the common-source structure which cancel the noise and distortion of the first and second stages and relax the design restriction on the first noise-cancellation stage. The provided circuit-level analysis is verified by simulations.

The proposed LNA is fabricated in 28-nm CMOS. It achieves a minimum noise figure (NF) of 2.5 dB and input return loss (S_{11}) < -15 dB over a 0.02–2 GHz bandwidth while consuming only 4.1 mW from a 1 V supply and driving an external 50-Ω load. The -3 dB power gain (S_{21}) is 18.5 dB and IIP3 is +4.15 dBm.

In the other design, the proposed LNTA employs a cross-coupled common-gate stage for wideband input matching. By applying a two-fold noise cancellation technique, the channel thermal noise of the first stage is removed, which improves its noise performance and linearity. We perform a detailed analysis of the transfer function, noise and linearity, which are then verified in simulations in TSMC 28-nm LP CMOS technology. The presented LNA achieves a power gain of 18.9–16 dB within 100 MHz up to 3.7 GHz and the input and output return loss of better than 10 dB. The IIP3 is +2.8 dBm and the noise figure (NF) ranges 1.58–2.4 dB over the band of interest with 24 mW DC power consumption.

In Chapter 4, we propose a novel clock-phase reuse technique for a discrete-time IIR complex-signaling band-pass filter (BPF). This leads to a deep improvement in filtering, especially the stop-band rejection, while maintaining the area, sampling frequency, number of clock phases and their pulse widths, but also the noise performance. Fabricated in 28-nm CMOS, the proposed BPF is highly tuneable and is capable of achieving a 70 dB stop-band rejection at 50 MHz offset with 25%-duty-cycle clocks, while consuming 1.65 mW. The achieved in/out-of-band IIP3 is +2.5 dB and +17.3 dBm, respectively, and the input-referred noise (IRN) is 1 nV/$\sqrt{\text{Hz}}$.

Finally, Chapter 5 introduces a new architecture of a discrete-time charge-rotating low-pass filter (LPF) which achieves a high-order of filtering and improves its stop-band rejection while maintaining a reasonable duty cycle of the main clock at 20%. Its key innovation is a linear interpolation within the charge-accumulation operation. Fabricated in 28-nm CMOS, the proposed IIR LPF demonstrates a 1–9.9 MHz bandwidth programmability and achieves a record-high 120 dB stop-band rejection at 100 MHz while consuming merely 0.92 mW. The in/out-of-band IIP3 is +18.6/+26.6 dBm.

6.2 Other Research in Progress

It is worth mentioning in passing that two novel DT Bluetooth receivers, one being an ultra low-power mixer-first receiver and another one being a high-performance low-power

receiver, have been designed and fabricated in 28-nm CMOS and are currently being measured in the lab. Besides the high-performance and low-power consumption features of these two designs, one of the key innovations is a new complex band-pass filter. Moreover, two novel high-frequency all-digitally assisted transmitter at 80 GHz and 150 GHz are designed and fabricated in 22-nm FDSOI which are under measurement. The key idea of these designs are mm-wave oscillators which could provide very low phase noise with minimum power consumption while transferring the maximum power. Finally, a novel first-ever reported D-band ADPLL based transmitter with an on-chip antenna has been designed and fabricated in 22-nm FDSOI, which is also under lab measurements.

6.3 Some Suggestions for Future Developments

After considerable improvements in the noise figure and linearity in the low noise (transconductance) amplifier [LN(T)A], new bottlenecks arise. The main suggestions for future research are briefly discussed as follows:

- Since the linearity of the noise-reduction LN(T)A is not optimized, the next challenge is to further improve its linearity. However, it is important not to sacrifice the noise, gain or power consumption performance.

- The proposed two-fold noise-canceling LNA is not suitable for the current-mode receiver since its output impedance is low. Hence, there is room for innovation there to make it amenable to work as a LNTA by keeping high linearity, low power consumption, and low noise figure.

Through this dissertation, it has been shown that the discrete-time (DT) signal processing will be the approach of choice for future development of commercial receivers in nanoscale CMOS.

- One recommendation is to integrate both the proposed LPF and BPF in a DT receiver and verify the overall RX improvement in noise, linearity, power consumption, and blocker tolerance.

- Since the proposed complex charge-sharing band-pass filter was pad limited, there is great room for research to provide a tuning bank and verify the bandwidth and center frequency tunabilty of the proposed clock reuse structure.

- Since a higher-order of filtering is achieved in both low-pass linear interpolation and complex charge-sharing band-pass filter without sacrificing the sampling frequency, by applying a pipeline technique, sharp filtering with high sampling frequency can be obtained that will be less sensitive to the folding effects due to sampling. Consequently, it would be more attractive for zero/low-IF receivers.

Bibliography

[1] C. Yue and S. Wong, "Scalability of RF CMOS," *2005 IEEE Radio Freq. Integr. Circuits Symp. - Dig. Pap.*, pp. 53–56, 2005.

[2] C. H. Diaz, D. D. Tang, and J. Y. C. Sun, "CMOS technology for MS/RF SoC," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 557–566, 2003.

[3] K. Muhammad, R. B. Staszewski, and D. Leipold, "Digital RF processing: Toward low-cost reconfigurable radios," *IEEE Commun. Mag.*, vol. 43, no. 8, pp. 105–113, 2005.

[4] M. Tohidian, I. Madadi, and R. B. Staszewski, "A 2mW 800MS/s 7th-order discrete-time IIR filter with 400kHz-to-30MHz BW and 100dB stop-band rejection in 65nm CMOS," in *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 56, 2013, pp. 174–175.

[5] M. Tohidian, S. Member, and I. Madadi, "Analysis and Design of a High-Order Discrete-Time Passive IIR Low-Pass Filter," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 0–30, 2014.

[6] I. Madadi, M. Tohidian, and R. B. Staszewski, "A 65nm CMOS high-IF superheterodyne receiver with a High-Q complex BPF," in *2013 IEEE Radio Freq. Integr. Circuits Symp.*, 2013, pp. 323–326. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6569594

[7] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. a. Abidi, "Analysis of first-order anti-aliasing integration sampler," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 10, pp. 2994–3005, 2008.

[8] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, 2011.

[9] R. B. Staszewski, K. Muhammad, D. Leipold, C. M. Hung, Y. C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. De-Obaldia, and P. T. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, 2004.

[10] K. Muhammad, Y.-c. Ho, T. L. Mayhugh, C.-m. Hung, T. Jung, I. Elahi, C. Lin, I. Y. Deng, C. Fernando, J. L. Wallberg, S. K. Vemulapalli, S. Larson, T. Murphy, D. Leipold, P. Cruise, J. Jaehnig, M.-c. Lee, R. B. Staszewski, S. Member, R. Staszewski, and K. Maggio, "The First Fully Integrated Quad-Band GSM / GPRS Receiver in a 90-nm Digital CMOS Process," *JSSC*, vol. 41, no. 8, pp. 1772–1783, 2006.

[11] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. A. Abidi, "An 800-MHz-6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2875, 2006.

[12] A. Geis, J. Ryckaert, L. Bos, G. Vandersteen, Y. Rolain, and J. Craninckx, "A 0.5 mm2 power-scalable 0.5-3.8-GHz CMOS DT-SDR receiver with second-order RF band-pass sampler," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2375–2387, 2010.

[13] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1097–1111, 2014.

[14] I. Madadi, M.Tohidian, and R. B. Staszewski, "A High IIP2 SAW-Less Superheterodyne Receiver with Multi-Stage Harmonic Rejection," under review with Minor Revision for Publication in IEEE Journal of Solid State Circuits.

[15] I. Madadi, M. Tohidian, and R. B. Staszewski, "A TDD/FDD SAW-Less superheterodyne receiver with blocker-resilient band-pass filter and multi-stage HR in 28nm CMOS," in *VLSI Circuits Digest of Technical Papers, 2015 Symposium on*, June 2015.

[16] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, 2nd ed., 2004.

[17] I. Fabiano, M. Sosio, A. Liscidini, and R. Castello, "SAW-Less analog front-end receivers for TDD and FDD," *IEEE J. of Solid-State Circuits*, vol. 48, no. 12, pp. 3067–3079, 2013.

[18] M. D. Tsai, C. F. Liao, C. Y. Wang, Y. B. Lee, B. Tzeng, and G. K. Dehng, "A multi-band inductor-less SAW-less 2G/3G-TD-SCDMA cellular receiver in 40nm CMOS," in *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 57, 2014, pp. 354–355.

[19] B. Van Liempd, J. Borremans, E. Martens, S. Cha, H. Suys, B. Verbruggen, and J. Craninckx, "A 0.9 V 0.4-6 GHz harmonic recombination SDR receiver in 28 nm CMOS with HR3/HR5 and IIP2 calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1815–1826, 2014.

[20] D. Murphy, A. Mirzaei, H. Darabi, M. C. F. Chang, and A. Abidi, "An LTV analysis of the frequency translational noise-cancelling receiver," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 1, pp. 266–279, 2014.

[21] D. Murphy, H. Darabi, A. Abidi, A. a. Hafez, A. Mirzaei, M. Mikhemar, and M. C. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, 2012.

[22] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, 2009.

[23] B. Razavi, *Fundamentals of Microelectronics*, 2008, vol. 13. [Online]. Available: http://www.amazon.com/dp/0471478466

[24] B. Van Liempd, J. Borremans, S. Cha, E. Martens, H. Suys, and J. Craninckx, "IIP2 and HR calibration for an 8-phase harmonic recombination receiver in 28nm," in *Proc. Cust. Integr. Circuits Conf.*, 2013, pp. 2–5.

[25] B. Debaillie, P. Van Wesemael, G. Vandersteen, and J. Craninckx, "Calibration of direct-conversion transceivers," *IEEE J. Sel. Top. Signal Process.*, vol. 3, no. 3, pp. 488–498, 2009.

[26] *Digital cellular telecommunications system (Phase 2+); Radio transmission and reception*, Std. (3GPP TS 45.005 version 11.2.0 Release 11), 2013.

[27] I. Fabiano, M. Sosio, A. Liscidini, and R. Castello, "SAW-less analog front-end receivers for TDD and FDD," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3067–3079, 2013.

[28] S. Chehrazi, A. Mirzaei, and A. Abidi, "Second-Order Intermodulation in Current-Commutating Passive FET Mixers," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 12, pp. 2556–2568, 2009.

[29] E. E. Bautista, B. Bastani, and J. Heck, "High IIP2 downconversion mixer using dynamic matching," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1934–1941, 2000.

[30] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "A +78 dBm IIP2 CMOS direct downconversion mixer for fully integrated UMTS receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 552–559, 2006.

[31] H. Darabi, H. J. K. H. J. Kim, J. Chiu, B. Ibrahim, and L. Serrano, "An IP2 Improvement Technique for Zero-IF Down-Converters," in *2006 IEEE Int. Solid State Circuits Conf. - Dig. Tech. Pap.*, vol. 38, 2006, pp. 171–174.

[32] I. Elahi and K. Muhammad, "IIP2 calibration by injecting DC offset at the mixer in a wireless receiver," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 12, pp. 1135–1139, 2007.

[33] K. Dufrene and R. Weigel, "A novel IP2 calibration method for low-voltage downconversion mixers," in *IEEE Radio Freq. Integr. Circuits Symp. 2006*, 2006.

[34] Q. Huang, J. Rogin, X. Chen, D. Tschopp, T. Burger, T. Christen, D. Papadopoulos, I. Kouchev, C. Martelli, and T. Dellsperger, "A tri-band SAW-less WCDMA/HSPA RF CMOS transceiver with on-chip DC-DC converter connectable to battery," in *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 53, 2010, pp. 60–61.

[35] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh, and P. Kinget, "A low-power low-noise direct-conversion front-end with digitally assisted IIP2 background self calibration," in *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 53, 2010, pp. 70–71.

[36] K. Dufrêne, Z. Boos, and R. Weigel, "A 0.13μm 1.5V CMOS I/Q downconverter with digital adaptive IIP2 calibration," in *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 2, 2007, pp. 80–82.

[37] K. Dufrene, Z. Boos, and R. Weigel, "Digital adaptive IIP2 calibration scheme for CMOS downconversion mixers," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2434–2445, 2008.

[38] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh, and P. R. Kinget, "Digitally assisted IIP2 calibration for CMOS direct-conversion receivers," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2253–2267, 2011.

[39] M. Chen, Y. Wu, and M. F. Chang, "Active 2nd-order intermodulation calibration for direct-conversion receivers," *IEEE Int. Solid State Circuits Conf. - Dig. Tech. Pap.*, vol. 38, no. 6, pp. 171–174, 2006.

[40] L. Longo, R. Halim, B.-R. H. B.-R. Horng, K. H. K. Hsu, and D. Shamlou, "A cellular analog front end with a 98 dB IF receiver," in *Proc. IEEE Int. Solid-State Circuits Conf. - ISSCC '94*, 1994, pp. 226–227.

[41] A. Hairapetian, "An 81-MHz IF receiver in CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1981–1986, 1996.

[42] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[43] R. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. Eliezer, E. de Obaldia, and P. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for

bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[44] K. Muhammad, Y. C. Ho, T. L. Mayhugh, C. M. Hung, T. Jung, I. Elahi, C. Lin, I. Deng, C. Fernando, J. L. Wallberg, S. K. Vemulapalli, S. Larson, T. Murphy, D. Leipold, P. Cruise, J. Jaehnig, M. C. Lee, R. B. Staszewski, R. Staszewski, and K. Maggio, "The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1772–1783, Aug. 2006.

[45] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. A. Abidi, "An 800-MHz–6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, Dec. 2006.

[46] A. Geis, J. Ryckaert, L. Bos, G. Vandersteen, Y. Rolain, and J. Craninckx, "A 0.5 $mm^{2\$}$ power-scalable 0.5–3.8-GHz CMOS DT-SDR receiver with second-order RF band-pass sampler," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2375–2387, Nov. 2010.

[47] Z. Ru, N. a. Moseley, E. a. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, 2009.

[48] X. Wang, J. Sturm, N. Yan, X. Tan, and H. Min, "0.6–3-GHz wideband receiver RF front-end with a feedforward noise and distortion cancellation resistive-feedback LNA," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 2, pp. 387–392, Feb 2012.

[49] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec 2004.

[50] Z. Z. Li, L. Chen, Z. Wang, C. Wu, J. Cao, M. Zhang, C. Wang, Y. Liu, and Z. Wang, "Low-noise and high-gain wideband lna with gm-boosting technique," *Electronics Letters*, vol. 49, no. 18, pp. 1126–1128, Aug 2013.

[51] H. Zhang, X. Fan, and E. S. Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 320–330, Feb 2009.

[52] K. C. He, M. T. Li, C. M. Li, and J. H. Tarng, "Parallel-RC feedback low-noise amplifier for UWB applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 8, pp. 582–586, Aug 2010.

[53] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "Design of a sub-mW 960-MHz UWB CMOS LNA," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2449–2456, Nov 2006.

[54] M. Moezzi and M. S. Bakhtiar, "Wideband LNA using active inductor with multiple feed-forward noise reduction paths," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 4, pp. 1069–1078, Apr 2012.

[55] F. Zhang and P. R. Kinget, "Low-power programmable gain CMOS distributed LNA," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1333–1343, Jun 2006.

[56] D. Murphy, A. Hafez, A. Mirzaei, M. Mikhhemar, H. Darabi, M. Chang, and A. Abidi, "A blocker-tolerant wideband noise-canceling receiver with a 2-dB noise figure," *2012 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 74–76, 2012.

[57] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, June 2008.

[58] H. Zhang and E. Sanchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 22–36, Jan 2011.

[59] P. Simitsakis, Y. Papananos, and E. S. Kytonaki, "Design of a low voltage-low power 3.1–10.6 GHz UWB RF front-end in a CMOS 65 nm technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 11, pp. 833–837, Nov 2011.

[60] Y. J. Lin, S. S. H. Hsu, J. D. Jin, and C. Y. Chan, "A 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 3, pp. 232–234, Mar 2007.

[61] R. M. Weng, C. Y. Liu, and P. C. Lin, "A low-power full-band low-noise amplifier for ultra-wideband receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 8, pp. 2077–2083, Aug 2010.

[62] A. Ansari and M. Yavari, "A very wideband low noise amplifier for cognitive radios," in *2011 18th IEEE International Conference on Electronics, Circuits, and Systems*, Dec 2012, pp. 623–626.

[63] I. Madadi, M. Tohidian, K. Cornelissens, P. Vandenameele, and R. B. Staszewski, "A high IIP2 SAW-less superheterodyne receiver with multistage harmonic rejection," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 332–347, Feb 2016.

[64] Y.-C. Ho, R. B. Staszewski, K. Muhammad, C.-M. Hung, D. Leipold, and K. Maggio, "Charge-Domain Signal Processing of Direct RF Sampling Mixer with Discrete-Time Filters in Bluetooth and GSM Receivers," *EURASIP Journal on Wireless Communications and Networking*, vol. 2006, no. 1, pp. 1–14, April 2006.

[65] C. F. Liao and S. I. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb 2007.

[66] B. Toole, C. Plett, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 2, pp. 319–328, Feb 2004.

[67] B. Razavi, *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*, 2nd ed. Prentice Hall Press, 2011.

[68] S. Kim and K. Kwon, "Broadband balun-LNA employing local feedback g_m-boosting technique and balanced loads for low-power low-voltage applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–10, 2020.

[69] H. Yu, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, "A 0.096-mm^2 1–20-GHz triple-path noise-canceling common-gate common-source LNA with dual complementary pMOS–nMOS configuration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 1, pp. 144–159, Jan 2020.

[70] S. Kim and K. Kwon, "A 50 MHz—1 GHz 2.3-dB NF noise-cancelling balun-LNA employing a modified current-bleeding technique and balanced loads," *IEEE Transactions on Circuits and Systems I*, vol. 66, no. 2, pp. 546–554, Feb 2019.

[71] S. S. Regulagadda, B. D. Sahoo, A. Dutta, K. Y. Varma, and V. S. Rao, "A packaged noise-canceling high-gain wideband low noise amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 1, pp. 11–15, 2019.

[72] J. Jang, H. Kim, G. Lee, and T. W. Kim, "Two-stage compact wideband flat gain low-noise amplifier using high-frequency feedforward active inductor," *Trans. on Microwave Theory and Tech.*, pp. 1–9, Aug 2019.

[73] H. Yu, Y. Chen, C. C. Boon, C. Li, P.-I. Mak, and R. P. Martins, "A 0.044-mm2 0.5-to-7-GHz resistor-plus-source-follower-feedback noise-cancelling LNA achieving a flat NF of 3.3±0.45 dB," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 1, pp. 71–75, Jan 2019.

[74] Z. Pan, C. Qin, Z. Ye, Y. Wang, and Z. Yu, "Wideband inductorless low-power LNAs with gm enhancement and noise-cancellation," *IEEE Transactions on Circuits and Systems I*, vol. 65, no. 1, pp. 26–38, Jan 2018.

[75] A. R. A. Kumar, B. D. Sahoo, and A. Dutta, "A wideband 2–5 GHz noise canceling subthreshold low noise amplifier," *IEEE Trans. on Circuits and Systems II*, vol. 65, no. 7, pp. 834–838, July 2018.

[76] B. Guo, J. Chen, L. Li, H. Jin, and G. Yang, "A wideband noise-canceling CMOS LNA with enhanced linearity by using complementary nMOS and pMOS configurations," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1331–1344, May 2017.

[77] M. Parvizi, K. Allidina, and M. N. El-Gamal, "Short channel output conductance enhancement through forward body biasing to realize a 0.5 v 250 μW 0.6 0.6–4.2 GHz

current-reuse CMOS LNA," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 574–586, March 2016.

[78] M. Parvizi and K. Allidina, "An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback," *IEEETransactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1843–1853, June 2016.

[79] S. Bagga, A. L. Mansano, W. A. Serdijn, J. R. Long, K. V. Hartingsveldt, and K. Philips, "A frequency-selective broadband low-noise amplifier with double-loop transformer feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1883–1891, Jun 2014.

[80] J. Y.-C. Liu, J.-S. Chen, C. Hsia, P.-Y. Yin, and C.-W. Lu, "A wideband inductorless single-to-differential LNA in 0.18 ¯m CMOS technology for digital TV receivers," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 7, pp. 472–474, July 2014.

[81] J. W. Park and B. Razavi, "A harmonic-rejecting CMOS LNA for broadband radios," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 1072–1084, Apr 2013.

[82] K. H. Chen and S. I. Liu, "Inductorless wideband cmos low-noise amplifiers using noise cancelling technique," *IEEE Transactions on Circuits and Systems I,*, vol. 59, no. 59, pp. 305–315, 2012.

[83] F. Belmas, F. Hameau, and J.-M. Fournier, "A low power inductorless LNA with double G_m enhancement in 130 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1094–1103, May 2012.

[84] W. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[85] A. Bozorg and R. B. Staszewski, "A 0.02-4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse," *IEEE Journal of Solid-State Circuits*, vol. 55, Sep. 2020.

[86] A. Parssinen, "System design for multi-standard radios," *IEEE Int of Solid-State Circuits Conf., Girafe Forum*, no. 2, Feb 2006.

[87] F. Bruccoleri, E. Klumperink, and B. Nauta, "Noise cancelling in wideband cmos lnas," *IEEE Int. of Solid-State Circuits Conf.*, Feb 2002.

[88] W. Chen1, G. Liu1, B. Zdravkow, and A. M. Niknejad1, "A highly linear broadband cmos lna employing noise and distortion cancellation," in *Radio Frequency Integrated Circuits Symposium. RFIC*, 2007.

[89] D. Im, I. Nam, H. Kim, and K. Lee, "A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner," *IEEE J. of Solid-State Circ.*, vol. 44, no. 3, pp. 686–698, Mar. 2009.

[90] A. Bozorg and R. B. Staszewski, "Two-fold noise-cancelling low-noise amplifier in 28-nm cmos," *Proc. of 17th IEEE International New Circuits and Systems Conf. (NEWCAS)*, June 2019.

[91] D. Kim, S. Jang, J. Lee, and D. Im, "A broadband PVT-insensitive all-nMOS noise-canceling balun-LNA for subgigahertz wireless communication applications," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 2, pp. 165–168, Feb. 2021.

[92] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 12, pp. 875–879, 2005.

[93] F. Bruccoleri, E. a. M. Klumperink, and B. Nauta, "Generating all two-MOS-transistor amplifiers leads to new wide-band LNAs," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1032–1040, 2001.

[94] M. Tohidian, I. Madadi, and R. B. Staszewski, "A Fully Integrated Discrete-Time Superheterodyne Receiver with +90 dBm Uncalibrated IIP2," submitted to IEEE Trans. Circuits Syst. I.

[95] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 571–581, Feb 2005.

[96] I. Madadi, M. Tohidian, K. Cornelissens, P. Vandenameele, and R. B. Staszewski, "A high IIP2 SAW-less superheterodyne receiver with multistage harmonic rejection," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 332–347, Feb 2016.

[97] M. Tohidian, I. Madadi, and R. B. Staszewski, "A fully integrated highly reconfigurable discrete-time superheterodyne receiver," *2014 IEEE Int. Solid-State Circuits (ISSCC)*, pp. 72–74, 2014.

[98] H. Wu, D. Murphy, and H. Darabi, "A harmonic-selective multi-band wireless receiver with digital harmonic rejection calibration," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 796–807, 2019.

[99] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, Dec. 2011.

[100] D. Kaczman and et al., "A single chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2," *IEEE J. of Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, Mar. 2009.

[101] D. Murphy, H. Darabi, and H. Xu, "A noise-cancelling receiver resilient to large harmonic blockers," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 6, pp. 1336–1350, June 2015.

[102] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-q n-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[103] M. Darvishi, R. van der Zee, and B. Nauta, "Design of Active N-Path Filters," *IEEE J. of Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, 2013.

[104] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2575–2587, Nov. 2014.

[105] I. Madadi, M. Tohidian, and R. B. Staszewski, "A fully integrated discrete-time superheterodyne receiver," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 2, pp. 635–647, Feb. 2017.

[106] Z. Ru, E. A. M. Klumperink, and B. Nauta, "Discrete-time mixing receiver architecture for RF-sampling software-defined radio," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1732–1745, Sep. 2010.

[107] A. Mirzaei, H. Darabi, J. C. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2678–2688, Oct. 2009.

[108] I. Madadi, M. Tohidian, and R. B. Staszewski, "Analysis and design of i/q charge-sharing band-pass-filter for superheterodyne receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 8, pp. 2114–2121, Aug. 2015.

[109] M. Tymchenko, D. Sounas, A. Nagulu, H. Krishnaswamy, and A. Alu, "Quasi-electrostatic wave propagation beyond the delay-bandwidth limitin switched networks," *phy.Rev. X*, vol. 9, p. 031015, July 2019.

[110] S. B. Ferreira, F. Kuo, M. Babaie, S. Bampi, and R. B. Staszewski, "System design of a 2.75-mW discrete-time superheterodyne receiver for bluetooth low energy," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 5, pp. 1904–1913, May 2017.

[111] F. Kuo, S. B. Ferreira, H. R. Chen, L. Cho, C. Jou, F. Hsueh, I. Madadi, M. Tohidian, M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, April 2017.

[112] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "Low-power highly selective channel filtering using a transconductor–capacitor analog FIR," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1785–1795, July 2020.

[113] Y. Xu, P. K. Venkatachala, Y. Hu, S. Leuenberger, G. C. Temes, and U.-K. Moon, "A charge-domain switched-gm-c band-pass filter using interleaved semi-passive charge-sharing technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 2, pp. 600–610, Feb. 2020.

[114] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A 150-μw 3rd-order butterworth passive-switched-capacitor filter with 92 dB SFDR," in *2017 Symposium on VLSI Circuits*, 2017, pp. C142–C143.

[115] S. Hameed and S. Pamarti, "24.6 a time-interleaved filtering-by-aliasing receiver front-end with >70db suppression at <4× bandwidth frequency offset," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017, pp. 418–419.

[116] F. Fary, M. De Matteis, T. Vergine, and A. Baschirotto, "A 28nm-CMOS 100mhz 1mw 12dbm-IIP3 4th-order flipped-source-follower analog filter," in *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, Sep. 2018, pp. 298–301.

[117] Y. Xu, H. Hu, J. Muhlestein, and U.-K. Moon, "A 77-dB-DR 0.65-mW 20-MHz 5th-order coupled source followers based low-pass filter," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 10, pp. 2810–2818, Oct. 2020.

[118] A. Mirzaei, R. Bagheri, S. Chehrazi, and A. A. Abidi, "A second-order anti-aliasing prefilter for an SDR receiver," *Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, 2005.*, pp. 629–632, Sep 2005.

[119] Yijun Zhou and Jiren Yuan, "An 8-bit 100-MHz CMOS linear interpolation DAC," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1758–1761, Oct. 2003.

[120] P. Payandehnia, H. Maghami, H. Mirzaie, M. Kareppagoudr, S. Dey, M. Tohidian, and G. C. Temes, "A 0.49–13.3 MHz tunable fourth-order LPF with complex poles achieving 28.7 dBm OIP3," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 8, pp. 2353–2364, Aug. 2018.

List of Publications

Book

- I. Madadi, M. Tohidian, **A. Bozorg**, and R. B. Staszewski, Wireless Discrete-Time Receivers, Cambridge University Press, in production.

Journal Papers

- **A. Bozorg** and R. B. Staszewski, "A 20 MHz–2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS," *IEEE Transaction on Circuit and System I (TCAS-I)*, vol. 99, iss. x, pp. 1–9, xxx. 2021.
  DOI: 10.1109/TCSI.2021.3092960. [IEEE Xplore link (Open Access)]

- **A. Bozorg** and R. B. Staszewski, "A Clock-Phase Reuse Technique for Discrete-Time Band-Pass Filters," *IEEE J. Solid-State Circuits (JSSC)*, vol. 99, iss. x, pp. 1–12, xxx. 2021.
  DOI: 10.1109/JSSC.2021.3086621 [IEEE Xplore link (Open Access)]

- **A. Bozorg** and R. B. Staszewski, "A 0.02–4.5-GHz LN(T)A in 28-nm CMOS for 5G exploiting noise reduction and current reuse," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 56, iss. 2, pp. 404–415, Feb. 2021.
  DOI: 10.1109/JSSC.2020.3018680. [IEEE Xplore link (Open Access)]

Conference Papers

- **A. Bozorg** and R. B. Staszewski, "A Charge-Rotating IIR Filter with Linear Interpolation and High Stop-Band Rejection," *Proc. of IEEE European Solid-State Circuits Conf. (ESSCIRC)*, sec. B2L-6, pp. 1–4, x Sept. 2021, Grenoble, France (remote). (Invited for JSSC Special Issue)

- **A. Bozorg** and R. B. Staszewski, "Two-Fold Noise-Cancelling Low-Noise Amplifier in 28-nm CMOS," *Proc. of 17th IEEE International New Circuits and Systems Conf. (NEWCAS)*, 26 Jun. 2019, ses. C2L-B2, pp. 1–4, Munich, Germany.
  DOI: 10.1109/NEWCAS44328.2019.8961224. [IEEE Xplore link]

Patents

- **A.Bozorg** and R. B. Staszewski "Multi-stage sub-THz frequency generator incorporating injection locking," Patent No. US 10,862,423, filed 2019-01-24, issued 2020-12-08.

- **A.Bozorg** and R. B. Staszewski "Discrete Time IIR Filter With High Stop Band Rejection," Patent No. US 10,840,890, filed 2019-01-03, issued 2020-11-17.

- **A.Bozorg** and R. B. Staszewski "Ultrawideband Very Low Noise Amplifier With Noise Reduction And Current Reuse," Patent No. US 10,903,798, filed 2019-01-03, issued, 2021-01-26.

- **A.Bozorg** and R. B. Staszewski, "Discrete Time Charge Sharing IIR Bandpass Filter Incorporating Clock Phase Reuse," Pub. No. US 20190229707 A1, just issued.

List of Figures

List of Tables

Acknowledgment

This has been a long journey to finally arrive at my PhD. I owe gratitude to so many people that have been involved in my study from the day I started my education. I would like to kindly acknowledge them here.

First and foremost, I would like to acknowledge my supervisor, Professor Bogdan Staszewski who has been a tower of strength to me on my journey to achieve my PhD. I bow to your superior knowledge in my field of study which has been of tremendous assistance to me. I can still feel how trilled I was when you gave me the opportunity to continue my scientific carrier under your wings as a PhD researcher by saying "Greetings from Graz," where you were for ESSCIRC conference. I felt like I was on top of the world. When I met you for the first time in your office, you told me "we will have lots of breakthroughs together! But be prepared for hard work" which I answered "I absolutely love challenges", that's how our non-stopped great works were started. I want to sincerely thank you for all trust you gave me and let me work in different research areas which thrived my knowledge and open different paths of success to me. You are my main inspiration and motivation in science, engineering and life in general. Having technical discussion with you always gives me the new thought and ideas. I have been so honored to know you and work with you and I will always be so proud of being part of your group.

My deepest appreciation is forwarded to my friend, Simon Factor from NovaUCD, who always inspires me to pursue my dream and dose his best to help me to achieve it. Thank you for all your technical and moral support and advice and I hope that I do my start-up in NovaUCD very soon!

I would like also to thank Helen McBreen from Atlantic Bridge, Eugene Heaney from

Ferfics, and Tony Donnelly from NovaUCD for all their given support in my difficult journey toward the start-up which helps me to get closer to my dream.

I have been very fortunate to meet two genius people, Dirk Leipold and Mike Asker, and began working with them on cryogenic circuits for quantum computing project. I really thank you for trusting me and involving me in this breathtaking project. I wish you the best of luck with your start-up, Equal1.

My appreciation is also extended to my Ph.D. committee members, Prof. Harald Pretl as the external Examiner, Dr. Deepu John as the internal Examiner and Dr. Teerachot Siriburanon as the chair of examination committee. Thank you for reviewing my PhD dissertation and providing insightful comments.

I would like to thank all my friends and former colleagues in Dialog semiconductor (former S3-semiconductor) specially Keven Fagan, Falvio Cali, Noel O'Riordan, Pamela Sutcliffe, and Aurelio Longhitano for all help and support they did during my collaboration with the company. It was a great chance for me to work with you for three years.

I also want to send my gratitude to Sunisa Staszewski not only for all the administrative support you did, but also for all thoughtful friendly life advice you give me which helps me to improve my judgment in general life matters. You always try to support me in any difficult situations and I really appreciate whatever you did for me.

From deep in my heart, I give my gratitude to my dear friends, Cagri and Pinar Cetintepe. I was very fortunate to meet you, Cagri, during my PhD. I remember that our friendship was started when the first time you were in UCD and got stuck behind the entrance door. You are one of the most talented people I know. We were a great team-mate who could overcome all problems. I always enjoyed of all fruitful technical discussions we had in different topics which most of the time they ended up with new ideas. I wish you success with your new carrier. I want to thank you, Pinar, as well for all your wise advises and support you did to me in my rainy days. Both of you are very supportive and as true F.R.I.E.N.D.S: "'*you are always there for me*".

During my PhD studies, I had the opportunities to have collaboration with my other colleges in several projects. Thank you ,Feng-wei Kuo, for your patient during our long meetings. I have also enjoyed working with you, Sandro Binsfeld and Filipe Baumgratz specifically during the brainstorming we had. I really appreciate your great sense of teamwork.

I must thank all my friends and colleagues in UCD. I always had great discussions with

Teerachot Siriburanon and Filippo Schembari. We did many tape-outs together and I really appreciate all support you did during those tight tape-out nights. Both of you have a bright future in the academia and industrial directions which you chose. Wish you both best in your carrier. I also thank all my friends in UCD along with Christos Hadjioannou, Aleksandar Stanic, Chiara Mauro, Rino Scarcelli, Arman Farhang, and Pierre Bisiaux.

My special thank to Mary Dunne and Philip Mortell who have helped me in last four years in different matters. Hence, I could fully concentrate on my research.

I want to convey my deepest gratitude going to my grandpa and grandma (Aghajoon and Aziz) for all the love they give to me. I wish you were with us today, grandpa, and you could read this letter. You were a notable man and always gave me fruitful lessons which I always apply in my personal and professional life. You taught me that no matter what I am doing in the moment, I should do it in the best way and should enjoy spending time on it. You always asked me never give up, like "John Nash" your favorite scientist, until I get to the point that "'*others leave their pen on my desk*". I promise you to get to that point. My lovely grandma, there is no exaggeration if I say I love you more than any one else in the world. Thank you for all your love give to me so far.

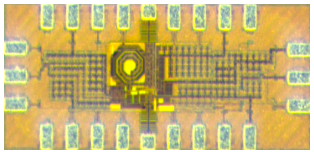
My little brother, Amin, you are one of the most intelligent persons I have ever seen who has a great sense of humor, and you are the only one who can make me laugh even when I am not in a good mood. Although you are very young, you are so supportive and you always do your best to help everyone in the family, specially myself. I want to thank you for being there and always making us have good times. You are not only a genius person, you are a very good example of a person who can handle all scientific works very well alongside your professional hobbies. I wish, one day, I could do "'*popping and locking*" as good as you!

Last, but not least, it is time to appreciate the great work you did for me, Mom and Dad. Mom, you are like a gold in my life as your name means (Zar). I know, there is no way to appreciate what you have done for me so far. From the beginning of my life, you sacrificed lots of opportunities in your career to spend enough time with me. You have been training me effortlessly during all these years. I still clearly remember how you taught me to read the clock when I was at age 3 or how you taught me geometry and simple math when I was at age 5. I can confidently say that it was all your effort which drew my attention towards science and mathematics from the beginning of my educational journey. Without your non-stop support I could not have achieved any success in my life.

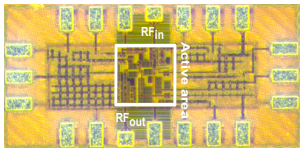
Dad, I wish I could have had even a small portion of your creativity. You are the main inspiration and role model in my life and I always wanted to be like you in so many matters. I have learned from you that it doesn't matter how big a problem is, I should always enjoy dealing with it. As you always say, if challenges are more difficult, the level of enjoyment is higher. You always encourage me to take risks in my life and discover any possible way to achieve success and never stop hard working until I get what I want. I still remember as clear as a crystal the day we fixed grandpa's old transistor radio and you gave me responsibilities which truly built my confident when I was so young. Or when you built a fully automated umbrella with very simple components like bike spikes, springs and so on, I learned the meaning of creativity for the first time in my life. When you gave me the "'*Science and Inventions of Leonardo da Vinci*" as a gift when I finished my primary school, I have been always thinking that you could have a book from your inventions as good as his one. I owe you for my entire life and all courage and creativity I have is just because of you.

— *Amir Bozorg*
Dublin, Ireland
May 2021

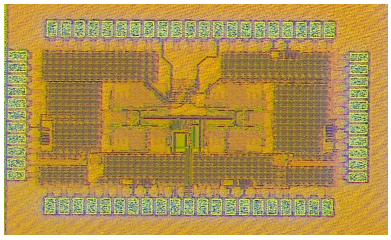
Chip Micrograph Gallery



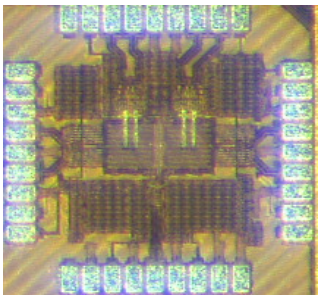
Wide band LNA with noise reduction in 28nm
[JSSC, 2020]



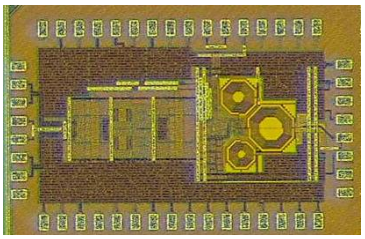
Two fold noise cancellation LNA in 28nm
[TCASI, 2021]



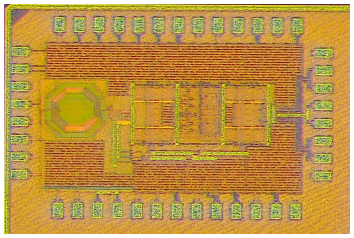
Charge rotating IIR LPF with linear
interpolation in 28nm [ESSCIRC, 2021]



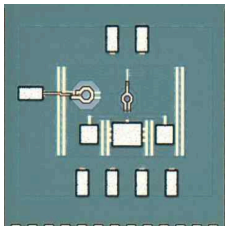
Clock-phase reuse complex charge sharing
BPF in 28nm [JSSC,2021]



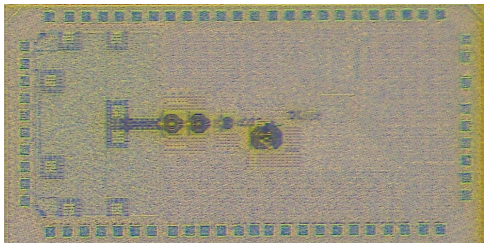
Low power DT BLE RX in 28nm
[Under measurement] (with S. Binsfeld)



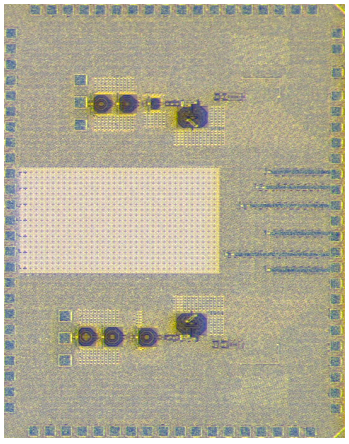
Ultra low power mixer first DT BLE RX in 28nm
[Under measurement] (with S. Binsfeld)



150GHz DCO in n16-TSMC
(with Feng-wei Kuo)



D-band all digital assisted TX with on chip antenna in 22nm-FDSOI
[Under measurement]



D-band all digital assisted TX in 22nm-FDSOI
E-band all digital assisted TX in 22nm-FDSOI

[Under measurement]

:

About the Author

Amir Bozorg was born in Tehran, Iran. Amir Bozorg received the M.Sc. degree (with Hons.) in Microelectronics from Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran in 2012. Since, 2016 he is pursuing the Ph.D. degree with University College Dublin (UCD), Ireland.

From 2016 to 2018, he was consulting for TSMC, Hsinchu, Taiwan, on a 16-nm ADPLL/RX for automotive radar applications. From 2017 to 2020 he was working as an R&D scientist at former S3 Semiconductor, now Dialog Semiconductor, Dublin, Ireland, where he was developing a K-band phased-array receiver.

He has also raised 210k€ venture capital from Atlantic Bridge Ventures, Dublin, Ireland, for commercializing a D/E-band ADPLL-based phased-array transmitter for automotive radars. Since 2020 he has been working with Equal1 Labs Ltd. in Dublin, Ireland as a Research Scientist

Mr. Bozorg has authored or coauthored several IEEE journal papers, an upcoming book on discrete-time receivers, and holds four issued U.S. patents in the field of RF-CMOS design. His research interests include millimeter-wave/RF transceivers, discrete-time receivers, ADPLLs, and oscillators.

Mr. Bozorg serves as a reviewer for the IEEE Journal of Solid-State Circuits, the

IEEE Transaction on Circuits and System I and IEEE Transaction on Circuits and System II.