PAMELA DATA ACQUISITION SYSTEM

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The PAMELA experiment is a satellite-borne apparatus devoted to the study of antiparticle component of cosmic rays. The instrument core is a permanent magnet surrounded by several instruments with different issues. Besides the TOF (Time-Of-Flight), spectrometer, calorimeter, an anticoincidence system and a neutron detector, the experiment has an on-board computer responsible of the whole acquisition and housekeeping. In this work we will show the Data Acquisition flux for PAMELA, explaining the read-out mechanism from the Front End and the data-storing trough the 2x2 GB Solid State Mass Memory and the Resurs VRL system toward the ground station.

1. Introduction

PAMELA (a Payload for Antimatter Matter Exploration and Light-nuclei Astrophysics) is a satellite-borne experiment designed to explore the charged particles in cosmic rays, with particular attention to the antimatter component.
The detector is a combination of different subdetectors which have different characteristics in order to identify, with high accuracy, particles within the experiment energy range (80 MeV - 190 s-GeV for antiprotons and 50 MeV - 270 GeV for protons). The telescope is based on a Magnetic Spectrometer, an Anticounter System, a Time-of-Flight System, an Electromagnetic Imaging Calorimeter, a bottom scintillator called S4 and a Neutron Detector [1].

The spectrometer is made of a permanent magnet (with a quasi-constant magnetic field in its cavity of 0.4 T) and a silicon tracker. The cavity is 445 mm tall and a cross-section of 132 mm * 162 mm which gives the geometric factor of the apparatus that is 20.5 cm^2×sr. The silicon tracker is made of six planes of double-layer, double-metal and AC coupled microstrip silicon detectors of 300 µm thickness and 25 µm strip pitch, with a total number of strips equal to 6144 per plane (total number of channel equal to 36864) [2].

The magnet is surrounded by the Anticounter System, needed to exclude particles that are out of the telescope geometric factor. It is made of 9 scintillator planes, read by phototubes [3].

The Time-of-Flight System provides the trigger to the experiment; is made by three scintillator planes and it will give information about the energy loss in

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the detector (*dE/dx*) and the absolute Z of the particles. These data, integrated with the trajectory, will give the velocity of the particle crossing and allows the rejection of albedo particles [4].

The Calorimeter is a 44 silicon planes detector, with 22 planes of tungsten in between to generate showers and measure the loss of energy. The structure is Si-x/W/Si-y (with a 380 μm thick and 2.4 mm wide strip in a 8×8 cm^2 ministrip silicon sensors arranged 3×3 in each plane, for 4416 total number of channels) in order to reconstruct the trace of the particles and their nature, is estimated that the protons (antiprotons) and positron (electrons) are distinguished at 95% retaining efficiency with a rejection factor of 10^4 [5].

S4 and the Neutron Detector are needed to extend Pamela energy range and to capture the showers that come out of the Calorimeter. The Neutron Detector, triggered by S4, will improve Pamela's capabilities of electron-proton discrimination up to higher energies (10^{11}-10^{13} eV).

Due to its orbital characteristics (elliptical and semi-polar, with an inclination of 70.4 and an altitude varying between 350 and 600 km) and its geometric factor (20.5 cm$^2\times$sr) it is expected an average trigger rate of 12 Hz. The amount of data for each event is roughly about 6 KB.

Redundancy has been used to avoid the most critical points of the experiment and to eliminate all the "single point failure". In the following paragraphs will be shown what the system is composed by and which is the data flux of any event in Pamela.

2. Event acquisition

The data acquisition is based on a data reduction philosophy, getting data from every subdetector starting from a single central unit (PSCU [6]: Pamela Storage and Control Unit).

As it is shown in picture n° 1, there is a chain of data collection points:

1) PSCU is the central unit which starts the data acquisition.
2) IDAQ multiplexes out all the PSCU commands to the Front-End electronics.
3) DSP boards are the first computational step in the data reduction.
4) Front-End boards are the analog to digital read-out boards.

All the data are stored in a 2+2 GB solid state mass memory in the PSCU and downloaded to the host satellite where there is a 30 GB unit for data storage (VRL: Very high speed Radio Link). The radio link towards the Data Downlink Station (near Moscow) is active 6 times a day and has a transmission window of 200 seconds at a speed of 153.6 Mbps. With these parameters has been designed

the Pamela Mass Memory in order to guarantee the maximum flux of data without any losses.
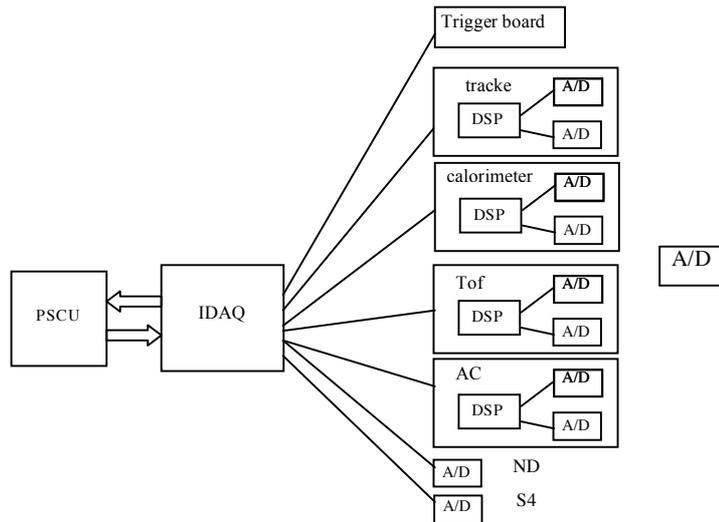

Figure 1. Electronic chain in the data reduction of Pamela.

The system has a global "busy" signal that is the only veto to the acquisition: if the IDAQ is busy (processing the event) no others triggers can be delivered. On the other hand, if the IDAQ is not busy, no commands can be sent to any subsystem. At startup the system is "busy", so that all the configuration settings can be done before starting acquiring data. The handshake protocol between PSCU and IDAQ allows setting a fixed number of "data acquisition commands queues" in the interface DMA, so that all the acquisitions have practically no cpu-time consuming.

The first command of each acquisition command queue is a "release busy" command to the IDAQ, which will wait, without acknowledging the next command, the first trigger; by this command the trigger system can start a trigger pulse as soon as the first particle generates the trigger mode defined (ex. S1 or S2 or S3) in the acquisition mode. All the subsystems will receive the trigger signal with different timing constraints, chosen considering the forming time of each dedicated readout electronics. As the trigger gets to the IDAQ the busy is set and a timeout of 3.5 ms starts to run on this board, in order to allow compression algorithms on the DSP boards; only after this time the

acknowledge to the pending command is sent back to the PSCU and all the commands start to reach every DSP board.

Once all the "read event" commands has got to every single subdetector and all the data are collected in the PSCU, the command queue starts again.

Monitoring the "busy" signal, the trigger board can calculate the "life-time" and "dead-time" of the experiment.

The Idaq protocol towards the CPU has a parallel link with a single handshake at a speed of 2 MB/s while the serial protocol towards the Dsp boards is a 10 Mbps link.

Once the packet is stored in the Mass Memory of the PSCU, there is a command from the host satellite to the Pamela system to download the data towards the data storage unit of the satellite itself. The interface unit that will handle the transmission between the PSCU and the satellite is called VRL adapter and which will guarantee a 12 MBps data link.

3. IDAQ

The Interface Data Acquisition board is an FPGA [7] based board, which has the major issues of commands redirection, protocol handling and trigger-busy managing in order to keep the acquisition going, secondly it is equipped with a DSP (Analog Device ADSP2187L), a RAM memory (CY62146V 4Mb Static RAM CYPRESS) and a FLASH memory (Am29LV800B 8Mb, AMD) in order to implement a second level trigger to cut out bad data from the acquisition if the trigger rate is too high and the "rubbish" data are too much (it is estimated that more then 80% of data will not be useful). The command queue needed to implement a second level trigger is different from the one used as default and this choice is written in the configuration parameters on the CPU software. All the software parameters can be set from the ground station and the same "second level trigger routine" can be loaded via the uplink.

All the communication links are LVDS based and the strobe-acknowledge protocol towards the PSCU gives to the Idaq the complete control of the data acquisition. Once the command queue is started there is no way to stop the acquisition unless a reset signal is sent to the system and the DMA is stopped.

In the other side, towards the DSP boards, it is implemented a serial protocol to reduce the number of connections and an hardware timeout of 2 µs to close the communication. The data-strobe protocol fulfills the requirements of speed and power consumption, moreover it fixes a standard interface between the different boards and makes the hardware development faster.

The RAM memory is used to collect data and allow any calculation wiht the DSP; there are two ram chips controlled by a dedicated FPGA (A54SX32A), which is demanded to implement a CRC protection on the data stored, so that any single bit error is corrected and a double one is recognized.

The same CRC encoding is implemented on the Flash chips which will contain the DSP programs and a backup of some configuration parameters (loaded from the PSCU).

The DSP is set in IDMA configuration and from the command queue point of view all the addressing overlays are handled by the controller which shows DSP memory as a linear 32 KWord (overlay equal to 1, 4 and 5).

In the Idaq architecture, the Main controller is master and all the peripherals (ram, flash, dsp and external links towards the dsp boards) are slaves and this "acquisition philosophy" has simplified radically both the hardware and the software organizations.

4. PSCU

The Pamela Storage and Control Unit, produced by Laben, is based on an ERC32 sparc V7 processor on which has been installed a real time operative system (RTEMS) and its structure is divided in five logical modules:

1) CPU module
2) Memory modules
3) PIF: Pamela Interface module
4) HKU: housekeeping unit
5) DC/DC: power supply

The CPU module hosts the processor, a SRAM 1Mb x 32 EDAC Protected, a Boot PROM, an EEPROM 256Kx32 EDAC Protected, a MIL-Std-1553 Bus Controller/Remote Terminal Function with its associated 64K x 16 RAM buffer, a Glue Logic ASIC including PCMCIA Bus Controller, Parallel System Bus interface (SBus90) called CRIMEA and developed by Laben.

The 1553 bus is the interface with the satellite and has a dedicated buffer memory to manage its commands which are the highest priority ones.

The Memory modules are organized to provide 16 Gbits storage capability, divided in eleven modules, independently monitored with a current absorption checker to avoid any latch-up faults. The ASIC designed to handle the access to the memory chips (SDRAM 8 MByte per unit), called DRAMMA (DRAM Manager ASIC), has a Reed-Salomon coding process and allow a maximum throughput of 750 Mbps.

The PIF unit is a dedicated interface board with three main issues:

1) Serving the communication with the Idaq through a DMA controller
2) handling the interface with the Mass Memory
3) providing the interface with the VRL adapter to download the data

Moreover it is implemented the interface with the PCMCIA bus to communicate with the processor. An FPGA (Actel RT54SX32S) is used to absolve its

functions and a memory unit (DRAM 256 Mb x 8) is used for buffering command and data paging.

Eventually the Housekeeping module has two serial links RS422 to communicate with the Kayser Housekeeping Board, which handles the connections with different subsystem (power supply control board, High Voltage control board, Tracker relays board, Idaq, S4 settings, Tracker sensors boards) to monitor the status of the system, plus a large number of ADC channel for analog monitoring (16 voltages, 16 sensors), contact closure inputs and differential bilevel inputs. This module is also equipped with 24 high level pulsed commands (26 V).

The DC/DC module is needed to provide all the voltages used inside the different modules. Is based on a push-pull topology and provides both common and differential mode. It is secured with latches for overloading and for output overvoltage, while has a non latching protection for input undervoltage. The module can be monitored with an analog output for the secondary voltage, a status bit and a thermistor.

5. Conclusions

The data acquisition system has been developed to fulfill requirements on the data handling and for its reliability. Moreover the housekeeping system and procedures will guarantee a full fault recovery.

Pamela will be launched at the beginning of 2006 and it will last for three years, acquiring a very large amount of data and enriching the whole scientific community with better results and maybe new aspects of our universe.

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