Level-2 Calorimeter Trigger Upgrade at CDF

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Abstract

The CDF RunII Level-2 calorimeter trigger is implemented in hardware and is based on a simple algorithm used in Run I. This system has worked well for RunII at low luminosity. However, as the Tevatron instantaneous luminosity increases, the limitation due to the simple algorithm starts to become clear. In this paper, we will present an upgrade path to the Level-2 calorimeter trigger system at CDF. This upgrade approach is based on the Pulsar board, a general purpose VME board developed at CDF and used for upgrading both the Level-2 tracking and the Level-2 global decision crate. This paper will describe the design, hardware and software implementation, as well as the advantages of this approach over the existing system.

I. Overview of CDF Trigger System

The goal of the trigger is to retain the most interesting events for physics analysis according with the bandwidth limitation of the CDF data acquisition system.

CDF RunII trigger is a three level trigger system [ref 1], as shown in Fig. 1. At Level-1 (L1), muon, track and calorimeter information is processed to produce the L1 decision. When an event is accepted at Level-1, all data is moved to one of four DAQ buffers in the front end electronics for all subsystems, and at the same time, subsets of detector information are sent to the Level-2 (L2) system where some limited event reconstruction is performed and a final L2 decision is made. Upon L2 accept, the full detector data is readout and sent to L3 processor farm for further processing. Only events accepted at L3 will be sent to mass storage. L1 is a synchronous 40 stages pipeline and is based on custom-designed hardware, while L2 is asynchronous and is based on a combination of custom hardware and commodity processor, Level-3 consists a processor farm. Each trigger stage has to reject a sufficient fraction of the events to allow processing at the next stage with minimal dead time. For the L2 trigger, this means that the processing speed should be fast enough (within ~ 20 microseconds) while the rejection power should be robust enough, which could be challenging at higher luminosity.

To prepare for higher luminosity running of Tevatron machine (1.8×10^{32} s^{-1} cm^{-2} already achieved while in the near future the peak is expected to be as high as 3.0×10^{32} s^{-1} cm^{-2}), many subsystems in the CDF trigger system have already been upgraded in the past few years (shown in pink in Figure 1). The L1 Track Trigger (XFT) is being upgraded to improve its trigger purity. The L2 SVT and Global decision subsystems have been upgraded to improve the processing speed. Both the Event Builder and L3 processor farm have been upgraded to increase the bandwidth downstream of L2. In this paper, we will describe an upgrade path for the L2 Calorimeter (L2CAL) subsystem to significantly improve its trigger rejection power (or purity) at higher luminosity and at the same time, improve its capability and flexibility in order to increase its trigger efficiency for important high Pt physics processes.

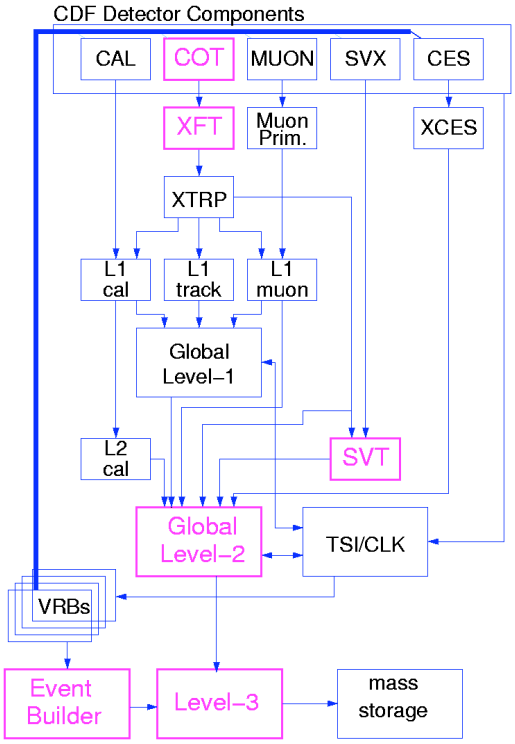

Figure 1: CDF RunII Trigger System. Boxes in pink are subsystems already upgraded in the past few years to prepare for the expected high luminosity. L2 Calorimeter (L2 CAL) and Global Level 2 are the subsystems involved in the upgrade stage described in this paper.

II. CDF Calorimeter Trigger

The goal of calorimeter trigger (both at L1 and L2) is to trigger on electrons, photons, jets, total event transverse energy (SumET) as well as missing transverse energy (MET). For CDF Run II, all calorimeter tower energy information,

including both Electromagnetic (EM) energy and Hadronic (HAD) energy, is digitized every 132 ns and the physical towers are summed into trigger towers, weighted to yield transverse energy. This results in a representation of the entire detector as a 24×24 map in the η-ϕ plane. The trigger tower energy data is then sent to both L1 and L2 calorimeter trigger system with 10-bit energy resolution, using a least significant count of 125 MeV resulting in a full scale Et of 128 GeV. At Level-1, the L1CAL only uses 8-bit trigger tower energy information for L1 processing, with the least significant and most significant bits dropped, giving a least count of 250 MeV and a full scale of 64 GeV.

As examples, electron and photon triggers are formed at L1CAL by simply applying energy thresholds to the EM energy of a trigger tower while jet triggers are formed using the total EM+HAD of a trigger tower. For electrons, tracks from the Level-1 track trigger (XFT) can be matched to the trigger towers while HAD energy can be used for rejection. L1CAL also calculates global transverse energy per event, Total Transverse Energy (SumET) and Missing Transverse Energy (MET), using the lower resolution 8-bit EM+HAD energy information. At Level-2, the L2CAL subsystem receives all 10-bit trigger tower energy information. However, the existing hardware-based L2CAL system does not re-calculate the event SumET and MET using the full resolution energy information available, rather, it still uses the SumET and MET information directly from L1CAL. This design feature limits its trigger selection capability for triggers requiring the global transverse energy. The main task of the existing L2CAL is to find clusters using the Energy Transverse (ET) of trigger towers. The cluster finding algorithm is based on a simple algorithm used for Run I, and is implemented in hardware. With the simple algorithm, the L2CAL hardware forms clusters by simply combining or linking contiguous regions of trigger towers with non-trivial energy. Each cluster starts with a tower above a "seed"

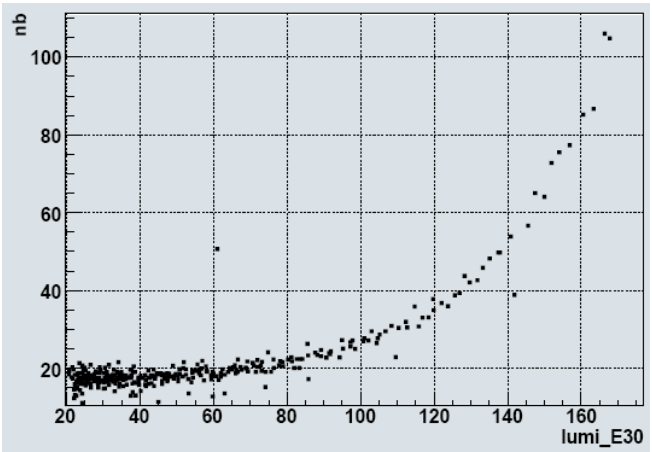

Figure 2: Rate of the jet trigger selection requiring jets above 40 GeV as a function of the instant luminosity (10^{30}cm^{-2}sec^{-1}).

threshold (typically a few GeV) and all towers above a second lower "shoulder" threshold that form a contiguous region with the seed tower are added to the cluster. The size of each cluster expands until no more shoulder towers adjacent to the cluster are found. The existing L2CAL trigger system has worked reasonably well at lower luminosity for Run II, however, as the luminosity increases (thus the occupancy in the calorimeter system), the simple algorithm based L2CAL system starts to lose its rejection power. In particular, at higher luminosity, the higher occupancy (largely due to multiple interactions per beam crossing) in calorimeter system has already produced large fake clusters with large fake ET in the L2CAL system (see figure 2a), resulting in high L2 accept rate saturating the bandwidth downstream of L2 (See Fig 2).

III. L2 Calorimeter Trigger Upgrade

The basic idea of the upgrade is making the full 10 bits resolution trigger towers energy information directly available to the Level-2 decision CPU running a new cluster finding and the Global Transverse Energy calculation. To do that we need to develop a new hardware path connecting the L1 CAL directly to the L2 decision CPU (See Figure 3). This new hardware path is based on the Pulsar boards [2], a general purpose VME board developed at CDF and used for upgrading both the Level-2 global decision crate [3] and the Level-2 silicon vertex tracking (SVT) subsystem [4]. With a such new system the full resolution calorimeter trigger tower data are received, preprocessed and merged by a set of Pulsar boards before being sent to the Level-2 decision CPU running a new *fixed-cone* cluster finding. Since the actual clustering finding is done inside the CPU, it is much more flexible.

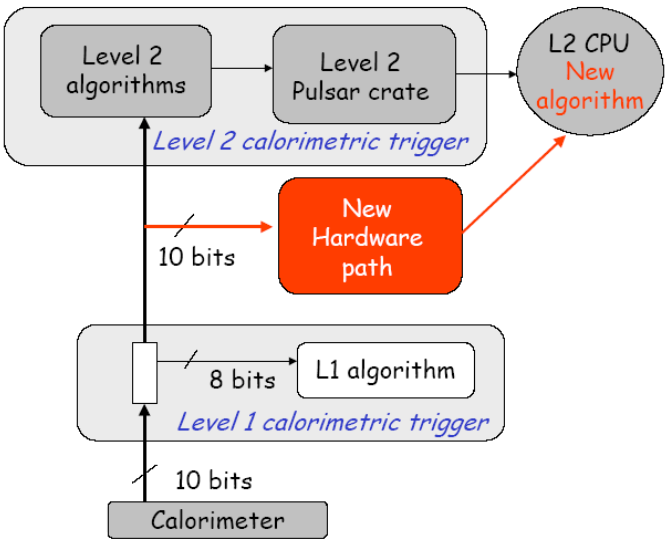

Figure 3: Hardware configuration for the L2 Trigger upgrade. The red path is the new hardware path that makes available the full 10 bit resolution trigger towers to the L2 decision CPU.

The fixed cone algorithm performs the following steps: (a) it finds and orders the seed trigger towers in ET, (b) it clusters ET in a fixed cone around the largest seed (no iteration is allowed), (c) it flags towers as used (d) it repeats until seeds are all used, (e) it orders the found clusters, (f) finally the cluster η and ϕ are weighted by ET. Offline precision can be reached if adapted clustering parameters are

chosen. The new clustering algorithm is more robust against increasing luminosity (thus occupancy in the calorimeter system).

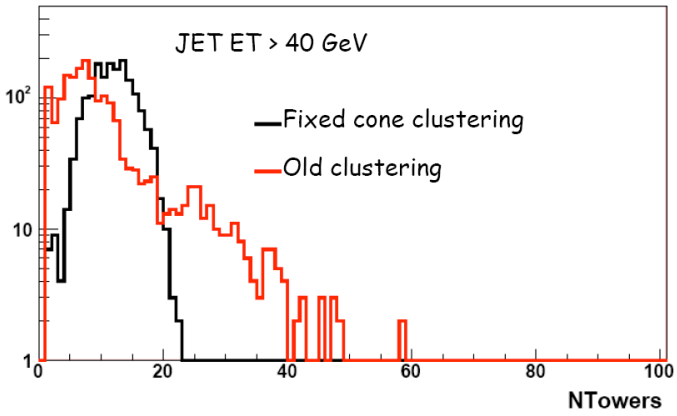

Figure 2a: The number of towers in the online reconstructed jets by the old clustering (red line) and the proposed algorithm (black line) for jets above 40 GeV. The seed and shoulder thresholds are respectively set to 3 and 1 GeV. The bump above 20 towers, in the red curve, shows that the frequency of these strange jets is quite large. The figure shows also that the fixed-cone algorithm fixes this problem.

In addition, the event SumET and MET can be re-calculated using the full resolution 10-bit trigger tower energy information available to L2. As an example, to show the impact of using the full 10-bit resolution trigger tower information for MET calculation, Figure 3 shows the difference in the efficiency turn-on curve for MET trigger using different resolution of trigger tower energy. The slow turn-on of the black and red efficiency curves, convoluted with a steeply falling background spectrum, produces a large Level 2 rate and a low purity sample.

The turn-on shown by the blue curve in fig 4 allows a better purity for the selected sample and a much smaller rate if applied with a threshold that provides the same signal efficiency of the black-red lines.

The challenges of this upgrade is to keep the clustering algorithm processing latency within ~ 20 microseconds, and have minimal impact on the experiment data taking during commissioning.

IV. Hardware Configuration

The basic idea of Pulsar is to use a motherboard (with powerful Altera FPGAs and RAMs) to interface any user data with any industrial standard link (for example, CERN S-LINK or Gigabit Ethernet) through the use of custom mezzanine cards. The key devices on the Pulsar board are three FPGAs (APEX 20K400BC-652-1XV [5]): two DataIO FPGAs and one Control FPGA. Each DataIO FPGA is connected to the Control FPGA. Both DataIO FPGAs provides interfaces to two mezzanine cards each and the connections are bidirectional.

In the current system one L2CAL board receives four Low Voltage Differential Signals (LVDS) input cables from L1CAL system, corresponding to 8 trigger towers energy information (both EM and HAD) at the CDF clock frequency (132 ns period). In the new system (see Figure 5), one new LVDS mezzanine card will receive the same amount of input data a L1CAL board is receiving now. With four mezzanine cards per Pulsar board, a first set 18 Pulsars will be able to receive all the input data. Then the 3 FPGAs process data, merge them and convert them into SLINK format. A second set of SLINK Merger Pulsars, already used in the previous L2 upgrade, receives the 18 SLINK data information, merge them and send to the L2 CPU. A highly integrated PCI interface, FILAR (Four Input Links Atlas Readout) move data from the SLINK channel to a 32-bit PCI bus running at 33 MHz.

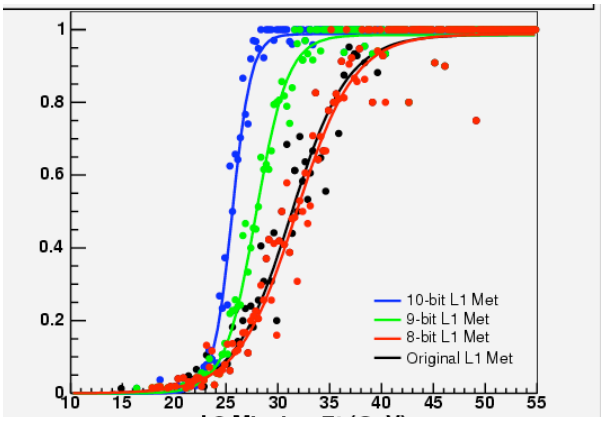

Figure 4: MET efficiency turn-on curves, using different resolution of trigger tower energy information. The black line is the current system performance at both L1 and L2. The red, green and blue curves are obtained simulating on data the MET algorithm with respectively 8 (red), 9 (green) and 10 (blue) bit resolution for trigger tower information.

Unlike other L2 path, the data for the new system will be available before the L1 decision is made. From the L1 decision arrival to the clustering about 20 us are available. Because the Pulsar can work up to 100 Mhz frequency and the firmware is very simple at each stage of the pulsar cluster, the main hardware contribution to the timing is due to the SLINK transfer (32-bit at the frequency of 40 Mhz). We expect that the latency due to the data transfer will be on average within 10 us.

Figure 6 shows a simplified top view of the mezzanine card. 4 logical blocks receive the input data from 4 80-pin Honda connectors. Each connector receives 40 LVDS signals at CDF clock frequency. Each input block includes 10 LVDS/TTL receiver chips. An Altera Apex device (EP20K160E) controls the flux of data from the Mezzanines to the DataIO Pulsar. The FPGA receives the TTL signals and simply store them into four registers at the CDF clock frequency. A multiplexer selects among the four sets of data

to be sent to the Pulsar at the frequency of 4xCDF clock frequency.

The firmware inside Pulsar selects only events confirmed by the L1 and trigger towers with non-trivial energy, finally converts to SLINK format.

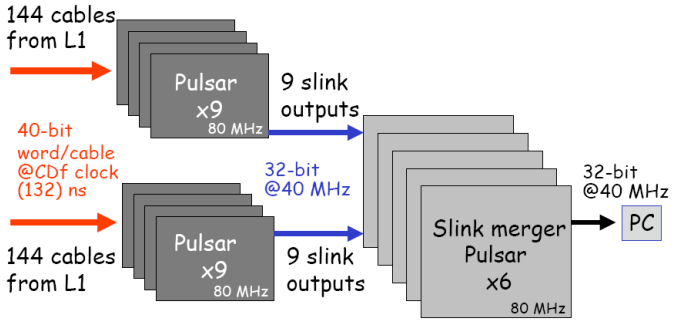

Figure 5: Pulsar Cluster used to make trigger tower energy information directly available to L2 CPU.

V. Algorithm Timing Study

In this section we present the status of the timing studies for the proposed Level-2 clustering and MET algorithm. In principle the proposed clustering and MET calculation could be done separately. However, it is something natural to merge MET calculation in the clustering algorithm since the inclusion is straightforward and makes use of some of the clustering code already exists. We assume as input for the algorithm all the non-zero energy towers. For each trigger tower, HAD and EM energy information are provided. The algorithm performs the following tasks: (1) Sum EM and HAD energy for each tower, selecting the seeds and shoulders according to corresponding threshold. (2) MET calculation. This operation can be done while looping over all the input towers for the previous item. (3) Sort the seed list in decreasing Et. (4) Cluster generation: beginning with the first seed. Sum the Et of all the towers above the shoulder threshold in a fixed size cone of the seed. The shoulders around the seed are directly addressed by using a look-up table (to speed up the algorithm). Mark all towers used in the current cluster as "used" and then move to the next seed tower in the list that is not marked as "used" and repeat. When seed tower list is exhausted return a list of the clusters. (5) Sort the clusters list in decreasing order.

Other important algorithms are not yet included in this study, but we expect that we will run them in the L2 decision CPU as well and we expect the extra CPU time taken to be negligible since they are simpler than the cluster finding. The algorithm timing, shown in Figure 7 is assessed running over a data set of 300 events firing the L2 trigger. The timing performance has been measured running on the L2 CPU (Dual AMD Opteron 2.4 GHz). On average the timing is about 5 microseconds with tail up to 10 microseconds.

VI. Commissioning Strategy

In order to minimize the impact on the operation of the CDF experiment during the commissioning phase, we will make a copy of the LVDS input signals available to the new system, while the original system continues to drive the data acquisition. In order to do that, we use the LVDS "multi-drop" property. The standard and suggested LVDS multi-drop configuration consists of one transmitter (L1CAL boards) and multiple receivers (actual and new L2CAL boards). The driver is restricted to be located at one end of the cable and only the other end is terminated. In this standard configuration the signal splitting is done replacing the L1CAL-L2CAL connecting LVDS cable with a longer one having a drop (without termination) on the new LVDS mezzanine receiver.

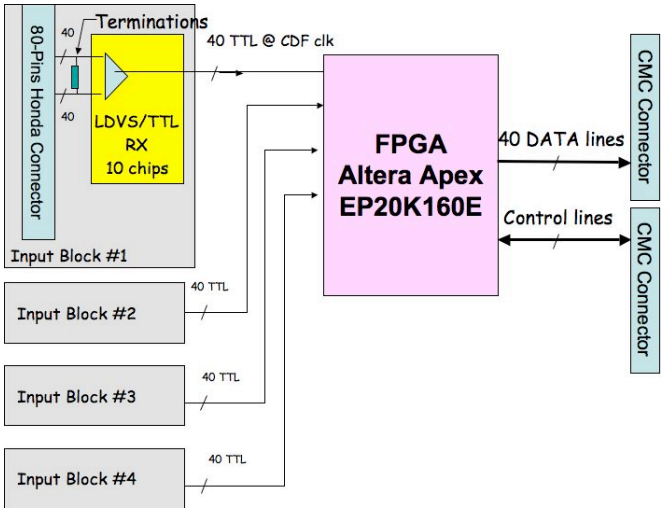

Figure 6: Simplified top diagram of the mezzanine card.

A non-standard multi-drop configuration, instead, consists of one transmitter (L1CAL boards) and double receivers (L2CAL and new L2CAL), both of them with terminations. Recent measures demonstrate that even using double termination, the voltage level of the differential signal is

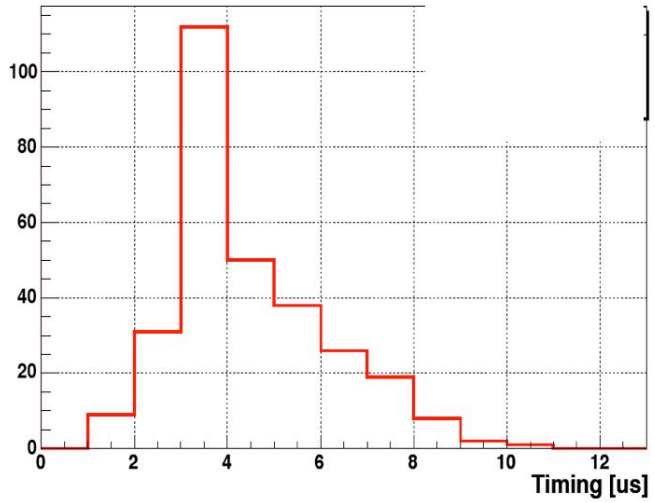

Figure 7: Timing for clustering and MET calculation.

acceptable and the reflections do not affect the TTL signal. The advantages of this non-standard configuration are multiple: first we don't affect the timing signals arrival for the

actual L2CAL during commissioning, because we can maintain the same cable length, second, at the end, we only have to disconnect the previous path without redressing cables and third the don't need to wait the end of the commissioning to sold the terminations on the Mezzanines. We run in this setup with beam for a long time, monitoring that the L1CAL-L2CAL connection doesn't introduce errors in the running system and signals received by the new L2CAL are fine.

The universality of the Pulsar board design allows us to test each data path, hardware as well as firmware, in a test stand using additional Pulsars configured in transmitter mode. In addition, during the production of the new LVDS receiver mezzanine cards, we are able to test the path from the DATAIO FPGAs of the LVDS receiver Pulsar to the L2 PC, for a subset of the input signals (a vertical slice of the system) simply loading fakes input data into the transmitter Pulsar RAM and replacing the LVDS link under construction with an available Hotlink. As soon as the first prototypes of the Mezzanines will be ready we simply have to add them to the already tested system in a test stand and quickly we can move to the running system.

VII. SUMMARY

The proposed L2CAL upgrade for CDF is providing to the L2 decision CPU the full 10-bit resolution trigger tower information to improve the resolution of the calorimetric level 2 algorithms. A fast, flexible fixed-cone jet clustering provides a much better jet resolution and background rejection. The missing transverse energy calculation reaches the level 3 resolution and rejection capability. The purity of the selected samples will be strongly increased. This is a big step forward to improve the CDF triggering capability at Level-2.

VIII. ACKNOWLEDGMENTS

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IX. REFERENCES

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