A fast and low noise charge sensitive preamplifier in 90 nm CMOS technology

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ABSTRACT: A fast charge sensitive preamplifier was designed and built in a 90 nm CMOS technology. The work is part of the R&D effort towards the read out of pixel or small strip sensors in next generation HEP experiments. The preamplifier features outstanding noise performance given its wide bandwidth, with a ENC (equivalent noise charge) of about 350 electrons RMS with a detector of 1 pF capacitance. With proper filtering, the ENC drops to less than 200 electrons RMS. Power consumption is 5 mW for one channel, and the closed loop bandwith is about 180 MHz, for a rise-time down to 2 ns in the fastest operation mode. Thanks to some freedom left to the user in setting the open loop gain, detectors with larger source capacitance can be read out without significant loss in bandwidth, being the rise time still 5.5 ns for a 5.6 pF detector. The output can drive a 50 Ω terminated transmission line.

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Contents

1 Introduction

Several next generation experiments in the field of high energy physics will exploit deep submicron technologies to readout small pixel and strip sensors near the interaction vertex [1]. The main reasons for choosing deep submicron processes are the higher density that can be achieved with increased scaling, and their intrinsic radiation hardness [2, 3]. Pixels sensors are characterized in general by a small capacitance, less than 1 pF, while small strip sensors have a larger capacitance, of the order of 5 pF. In any case these detectors can take advantage of short shaping time contants without a large increase of series noise. Short shaping is also forced by the high interaction rate in order to prevent pile-up.

An integrated charge sensitive preamplifier (CSP) was realized in a 90 nm CMOS technology from TSMC, as a test bench to explore the capability of this technology to fulfill the requirements of the readout of pixel and strip sensors. The CSP is composed of a single-ended inverting gain block, and a feedback capacitor and resistor.

2 Preamplifier schematic

The schematic of the charge sensitive preamplifier is presented in figure 1. A structure made of three gain stages in series was designed. To reduce power consumption, a single ended amplifier was preferred over a differential structure.

The input transistor M_1 is a N-channel MOS, which gives a lower series white noise with respect to the P-channel counterpart, due to its higher transconductance. The current source at its drain is made with the P-channel MOS M_6 with smaller transconductance, in order to make its noise contribution negligible. The input transistor is thus the main source of series noise. The second stage M_2 is the Miller stage, providing gain and the dominant pole of the gain structure with the capacitance C_c. The small resistor R_c, whose value is close to the inverse transconductance of M_2, is used to suppress direct transmission through C_c at high frequency [4].
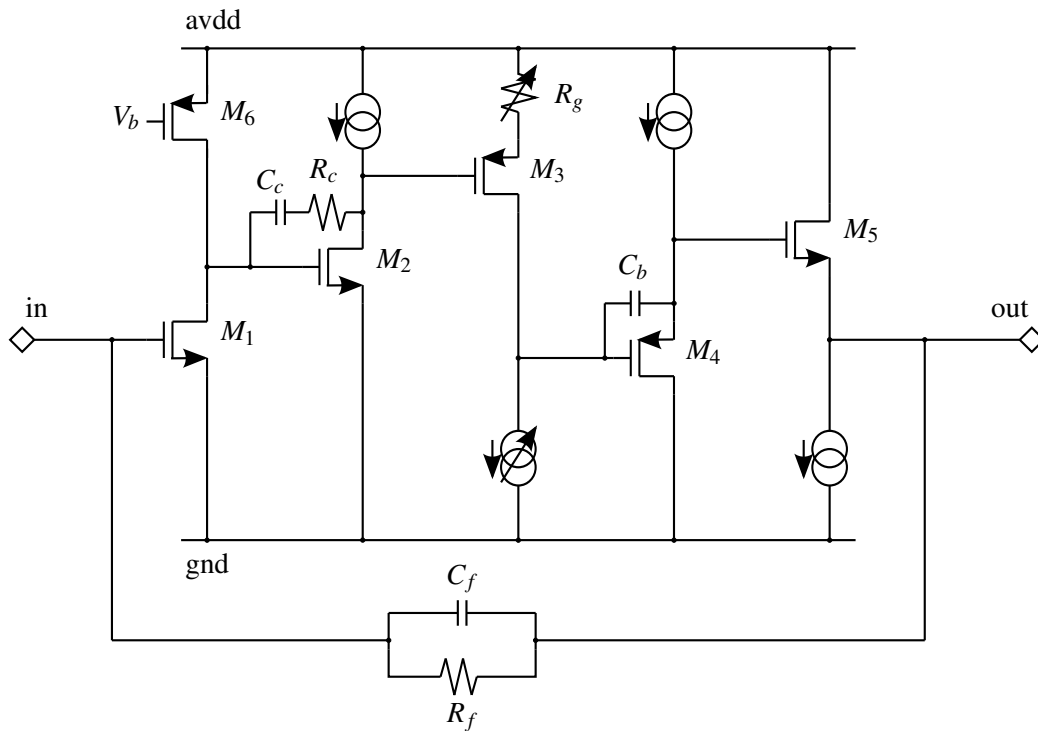
Figure 1. Equivalent schematic of the charge sensitive preamplifier.

The third gain stage M_3 is needed for two reasons: first, it makes the overall gain of the structure negative (making it possible to apply negative feedback with passive feedback components), and second, it can be tuned by means of the variable resistor R_g in order to change the open loop gain. The effect of changing R_g is depicted in figure 2. This degree of freedom allows to tune the open loop gain in order to match the bandwidth upper limit with the closed loop gain C_d/C_f, where C_d is the detector capacitance. This makes possible to readout detectors with different source capacitances without virtually any change in bandwidth.

The fourth stage M_4 is a voltage follower with a feedthrough capacitor C_b. Its only effect is to shift the DC voltage up before the last stage M_5, and is biased with a very small current, in order to keep its output impedance high. At signal frequencies, this stage is equivalent to a passive AC coupling stage, as all signal passes through C_b. The last stage M_5 is the output stage; the preamplifier is optimized for negative charge pulses (electrons) at the input, so the output pulse is positive, and a N-channel transistor is more suitable to drive the output.

The feedback loop is made of a capacitor C_f and a resistor R_f. The purpose of the resistor is to stabilize the working point of the preamplifier with a DC feedback loop, and to discharge the capacitor with time constant $C_f R_f$ after each pulse. The resistor R_f is the main source of parallel noise.

There is a drawback to this design, due to the presence of high frequency poles at the second, third and last stage. These poles determine the upper bandwidth limit of the preamplifier, which gives the rise time of the output pulse. The first stage, whose output is a current into the Miller capacitor, and the fourth, which is bypassed with a feed-through capacitor, do not contribute to the
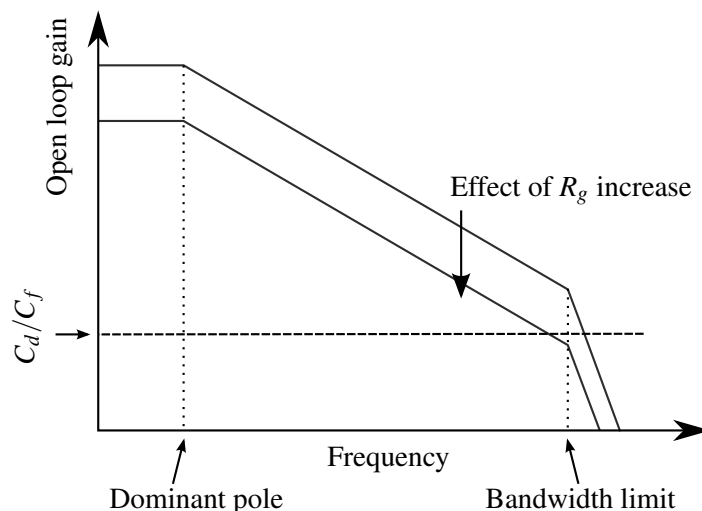
Figure 2. Effect of a change in R_g on the open loop gain.

bandwidth limit. The need to push the parasitic poles at higher frequency sets a lower limit on the power dissipation of this circuit. If each stage has high transconductance and relatively low output impedance, as in a 90 nm CMOS technology, the parasitic poles sit at very high frequency, enough to allow the amplifier to operate at high frequency without ringing or instability.

3 Implementation in a 90 nm CMOS technology

This preamplifier schematic was implemented in a 90 nm CMOS technology from TSMC, which features MOS transistors with very high transconductance and relatively low output impedance. The transconductance of the input transistor was easily obtained to be as high as 10 mA/V, which gives a white noise contribution of about $1 \, \text{nV}/\sqrt{\text{Hz}}$ at the input. The capacitance of the input transistor is 300 fF. The feedback components C_f and R_f were chosen to be 200 fF (including parasitics) and 300 kΩ respectively.

The tuning of R_g, whose purpose was described in the preceding section, was achieved by means of a switch implemented with a P-channel mos, not shown in figure 1. This allowed to choose the value of R_g between 100 Ω and 0 Ω (a short). In addition to this, the bias current for the third stage could be adjusted independently from the bias current of the rest of the preamplifier by changing the value of an external bias resistor, allowing to change the transconductance and output impedance of M_3.

With the exception of the fourth stage, which is biased with a negligible current, the others are operated at the fairly high current of about 1 mA to keep transconductance high. Being the power supply voltage set at 1.2 V the total power consumption is about 5 mW for the whole preamplifier.

The test circuit is shown in figure 3. A voltage step was applied at the input through a test capacitor, simulating an input charge of 15 kiloelectrons. The preamplifier was tested with source capacitance values of 1 pF and 5.6 pF. The output was acquired with a fast oscilloscope at the far end of an AC coupled 50 Ω transmission line.
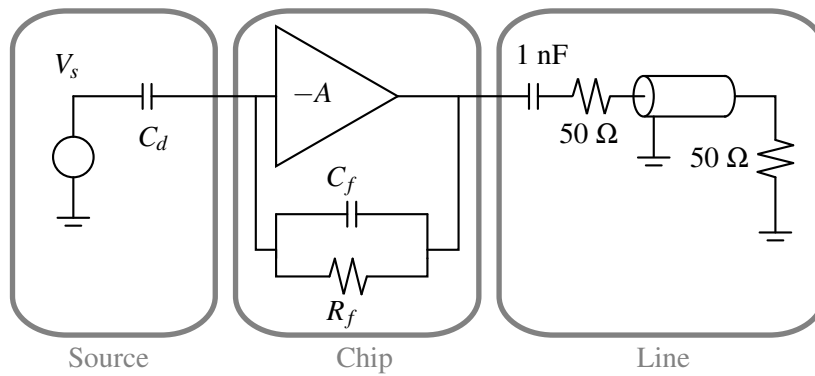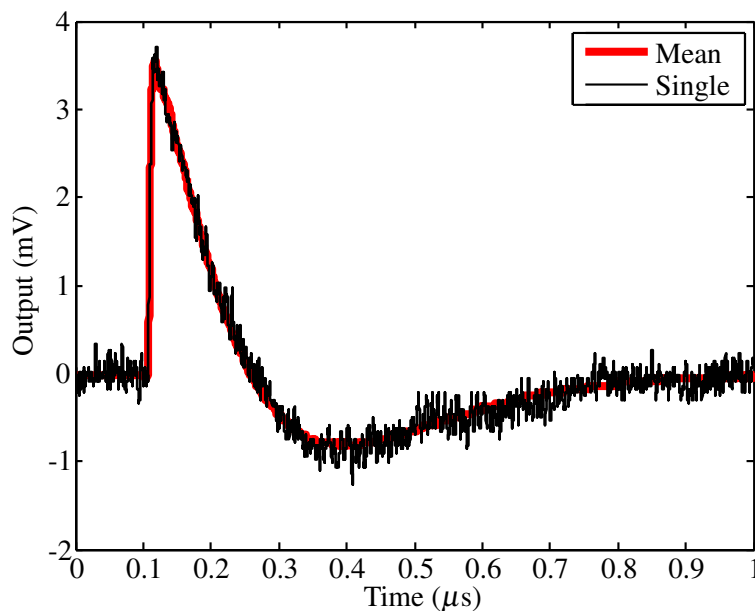
Figure 3. Test circuit.

Figure 4. Response to pulses of 15 kiloelectrons with a 1 pF source.

3.1 Signals and noise with a 1 pF source

Figure 4 shows the output of the preamplifier in response to charge pulses of 15 kiloelectrons from a 1 pF source. The fall time of the signal is about 150 ns, set by C_f and R_f. The undershoot is due to the AC coupling at the output, shown in figure 3. The rise time depends on the bandwidth setting; by tuning the third stage, it can be lowered to 1.95 ns (10% to 90%), as shown in figure 5, where some ringing starts to show, revealing the closed loop bandwidth limit of 180 MHz. Summing together the capacitance of the source, of the input transistor, and a parasitic contribution of about 250 fF from the input pad and the interconnects, we can estimate the total capacitance at the input node to be 1.5 pF. The gain bandwidth product of the preamplifier is thus close to 1.35 GHz in this configuration, and it is stable at a closed loop gain of 7.5.
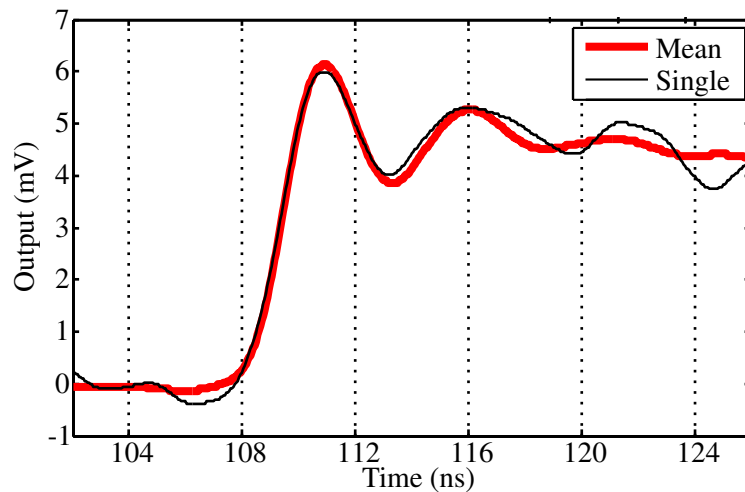
Figure 5. Fastest risetime with a 1 pF source.

The noise was measured as the RMS baseline fluctuation of the output signal divided by the charge gain. In this way, the input noise is expressed in terms of the RMS Equivalent Noise Charge (ENC) [5]. For the signal in figure 4, the ENC is 377 electrons RMS over the full preamplifier bandwidth, before any shaping. This value is due to the parallel noise of the feedback resistor and to the series noise of the input transistor, almost in equal weights. This result matches the expected noise from simulations.

A set of simple low-pass (RC) filters was applied offline in order to improve the noise performance of the preamplifier. The low-pass time constant was set to 10 ns, 20 ns, 50 ns and 100 ns. The resulting waveforms are shown in figure 6. In the latter case of 100 ns, the preamplifier fall time combines with the filter time constant, giving a nearly CR-RC shaping. The effect of the filter is to eliminate the series white noise contribution from the ENC. The parallel noise is unaffected, since no high pass filter is applied, and so is the $1/f$ constribution, which anyway is negligible for this value of input capacitance. The resulting values for the ENC are 226, 206, 196, 186 electrons RMS respectively.

3.2   Signals and noise with a 5.6 pF source

The preamplifier was also tested with a source of 5.6 pF capacitance. If the gain-bandwidth product of the preamplifier were fixed, a bandwidth reduction of a factor of five would come with the increased input capacitance, resulting in a rise time of nearly 10 ns. By adjusting the third gain stage, the gain-bandwidth product could be increased to 2 GHz, gaining a factor of two from the previous setting. Since the closed loop gain is now about 30, the closed loop bandwidth is 65 MHz, and the 10% to 90% rise time of the output pulse is 5.5 ns, as shown in figure 7.

The ENC of the unshaped signal is 588 electrons RMS. The value is larger than in the previous case, due to the larger source capacitance, which makes the contribution from the series noise dominate over the parallel noise of the feedback resistor. Also in this case, there is a good match with the expected noise from simulations. Again a set of RC filters with different time constants
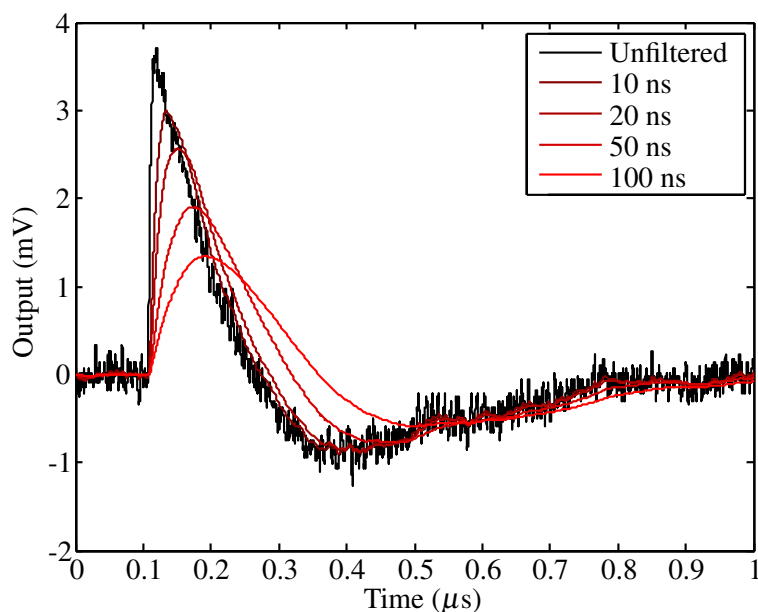
Figure 6. Response to pulses of 15 kiloelectrons with a 1 pF source, low-pass filtered.
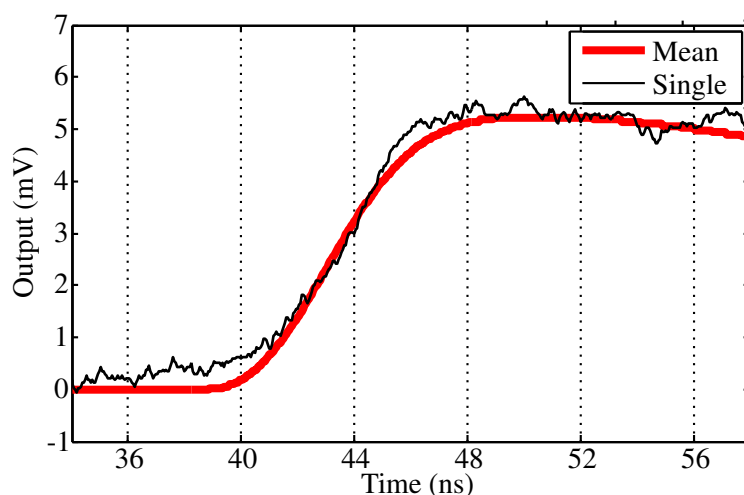

Figure 7. Risetime with a 5.6 pF source.

were applied offline; the resulting waveforms are shown in figure 8. The resulting values for the ENC are 503, 398, 300 and 260 electrons RMS for filters at 10 ns, 20 ns, 50 ns and 100 ns respectively. The low-pass filter reduces the weight of the series white noise to negligible amounts. At 100 ns filtering, noise is larger than in the previous case because the $1/f$ series contribution, which is proportional to the input capacitance, adds to the parallel noise of the feedback resistor.

The noise performance here presented is of the same order of magnitude of existing integrated charge sensitive preamplifiers, which however have a smaller bandwidth (see, for example, [6]).
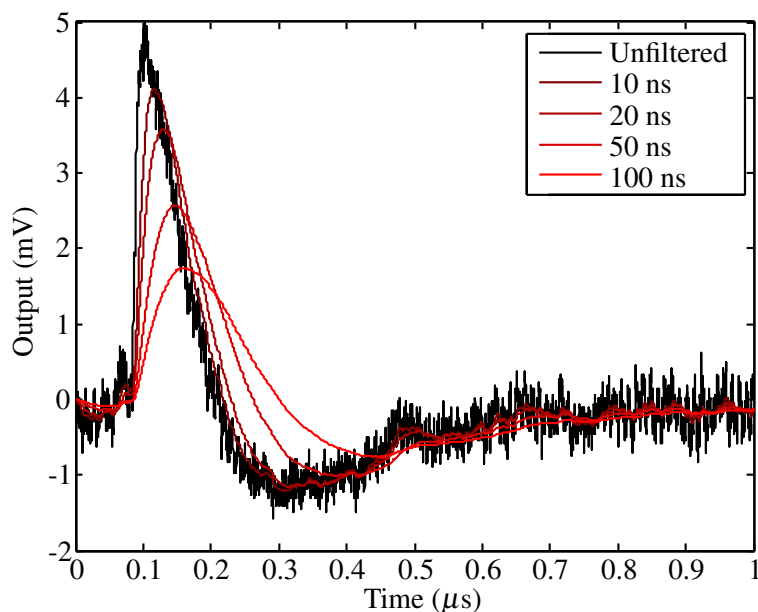
Figure 8. Response to pulses of 15 kiloelectrons with a 5.6 pF source, low-pass filtered.

Faster circuits with a bandwidth close to the circuit presented in this paper usually exhibit a higher noise (see, for example, [7]).

3.3 Jitter

The time jitter was measured with large signals, in the hundred of kiloelectrons range. This charge corresponds to the single photoelectron response of a photomultiplier such as a photomultiplier tube (PMT) or a microchannel plate (MCP). The MCPs in particular are known to offer an outstanding time resolution, of the order of 100 ps and below, and are good candidates for time of flight (TOF) applications, requiring low jitter from the front-end electronics. The measured jitter for the CSP prototype coupled to a 1 pF source is 56 ps RMS and 47 ps RMS for pulses of 150 and 300 kiloelectrons respectively. Even if this value is not at the cutting edge of timing performance, it was obtained with a preamplifier consuming relatively low power (5 mW) compared to usual electronics for TOF applications.

4 Conclusions

The charge sensitive preamplifier performs well in terms of bandwidth and noise, meeting the design specifications. The adopted 90 nm CMOS technology allows to achieve very high transconductance thanks to increased scaling: low series noise can be obtained, although at the price of fairly high power consumption in the first stage. About 20% of the total power can be saved if the 50 Ω line drive capability by the output stage is not required. Furthermore, an optimization of the second and third stages could be tried in order to reduce the biasing current. This may be necessary in order to prevent excessive power dissipation and heat in closely packed pixel arrays. The feedback resistor could be replaced with a MOS switch to reduce the parallel noise contribution.

Acknowledgments

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