



The analog signal processing board for the HEAT telescopes

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ABSTRACT

The aim of the Pierre Auger Observatory is to measure with high statistics the flux, the arrival directions and the mass composition of cosmic rays at the highest energies. Since 2009, the Auger Collaboration has added three new High Elevation Auger Telescopes (HEAT) along with a new 25 km² infill array in the field of view of the new telescopes. These enhancements have lowered the energy threshold of the Observatory by about an order of magnitude. In combination with the existing telescopes in Caihueco the vertical field of view is extended to about 60°, allowing the measurement of nearby air showers arising from primaries with energies as low as 2×10^{17} eV.

In this paper we describe the new front-end analog board developed to process the signals generated by the photomultipliers of the HEAT telescopes. Eighty analog boards have been produced, fully characterized and tested. The main characteristics of the electronic circuits and the circuit parameters are illustrated.

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1. Introduction

The Pierre Auger Observatory [1] measures ultrahigh energy cosmic rays using an array of surface detectors and fluorescence telescopes. It combines surface and fluorescence detection techniques in a hybrid design which improves the accuracy of shower reconstruction and provides energy measurements independent from hadronic interaction models.

The surface detector (SD) [2,3] covers 3000 km² of area and consists of 1660 water Cherenkov detectors, arranged on a triangular grid with a distance of 1.5 km between each other. The fluorescence detector (FD) [4] is composed of 24 fluorescence telescopes located in four sites around the perimeter of SD array. Each FD site has six telescopes with a Schmidt optical system that covers a field of view of 30° in azimuth and 30° in elevation towards the SD array. In this configuration, the Observatory is fully efficient above 10¹⁸ eV.

The Pierre Auger Observatory has expanded its energy range down to 10¹⁷ eV by a nested surface array with reduced spacing and additional muon detection capabilities (AMIGA, Auger muons and infill for the ground array [5]) overviewed by three additional fluorescence telescopes (HEAT) with an elevated field of view from 30° to 60° above the horizon [6,7].

The HEAT telescopes have been built at a distance of about 180 m from one of the existing FD buildings (named Caihueco)

and few meters (about 6 m) below its horizon in three separate shelters grouped together. HEAT and Caihueco together can be treated as an FD site with nine telescopes covering an elevation range from the horizon to about 60°, in order to measure the complete shower profile (including depth of shower maximum, X_{\max}) without a bias from geometry. Most of the HEAT hardware is the same as in the other 24 telescopes, including the optical system and the mechanics.

In each telescope, light is collected by a camera [8] composed of 440 pixels, arranged in a matrix of 22 rows and 20 columns located on the focal surface of the telescope. An extensive air shower (EAS) initiated by a primary cosmic ray is imaged on the camera as a sequence of activated pixels. Each pixel is a hexagonal photomultiplier tube (PMT) (XP3062 manufactured by Photonic [9]).

A characteristic PMT signal can be modeled with a trapezoidal current pulse whose width varies from hundreds of nanoseconds to tens of microseconds, depending from the shower distance [10,11]; whereas the rise and fall times are about 1/3 the pulse width at the base because of the relative size of the spot size and the PMT window (see Fig. 1). The amplitude is highly variable and depends on the shower distance, its energy and on the atmospheric light attenuation.

Every PMT is physically connected to an electronic unit, called the head electronics (HE) [12]. The signals generated by the PMTs of a camera are fed to one front-end sub-rack composed of 20 analog boards (ABs) [10] each connected to one first level trigger (FLT) board that in the 24 telescopes of the original design digitizes the signals at a 10 MHz sampling rate with 12-bit

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resolution. The FLTs also forward the information on triggered pixels to one second level trigger (SLT) board per telescope which is housed in the same sub-rack and implements a track finding algorithm in FPGA firmware [13,14]. When an event passes the first two hardware trigger levels, it is read out and analyzed by a third level trigger (TLT) [15], a software trigger based on track length and space/time requirements.

In the low energy range relevant for HEAT the emission of fluorescence photons is faint, for this reason such showers can be properly detected only at closer distances. Such showers remain in the field of view of each PMT for a shorter time than the showers at greater distances. For this reason improved temporal resolution is

required. To fulfill this request the front-end electronics design has been modified with respect to the existing one. In particular, to increase the trigger efficiency the time resolution has been enhanced from 100 ns to 50 ns, therefore the sampling rate has been increased from 10 MHz to 20 MHz on the FLT. In addition the dynamic range has been enlarged by a factor of about 1.5.

From the point of view of the analog signal conditioning, some upgrades have been made. We describe the improvements of the new AB developed in the next sections.

2. Analog board features and architecture

Although maintaining the same physical size, channel count and features of the originals, the new AB developed for the HEAT telescopes adds a variety of new and improved features, such as enlarged bandwidth, increased dynamic range, enhanced signal-to-noise ratio and differential drivers for the new differential FADCs placed on the new FLT boards.

The AB is a multi-channel system and, as shown in the schematic diagram of Fig. 2, is composed of 22 channels and receives AC-coupled signals from the 22 PMTs of a single camera column. At a typical gain (~ 30 V/V), each channel has an input voltage range of 70 mV. In the rare case of very high-energy air showers, very close to the FD site, there is the possibility that one or more acquisition channels saturate. In the design of the AB we have accounted for this possibility, in the same way it was accounted in the ABs of the other 24 telescopes. In fact, the 22

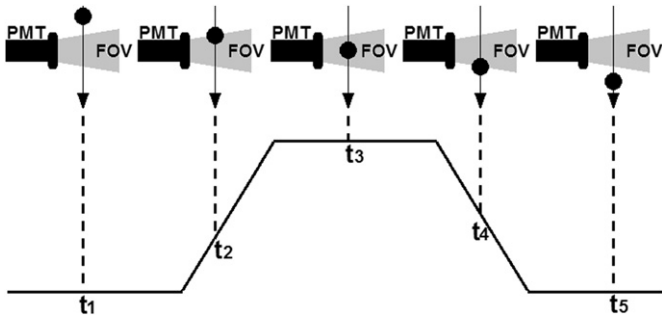


Fig. 1. Schematic diagram illustrating an EAS (the black spot) passing through the field of view (FOV) of one PMT and the trapezoidal current pulse at the PMT output.

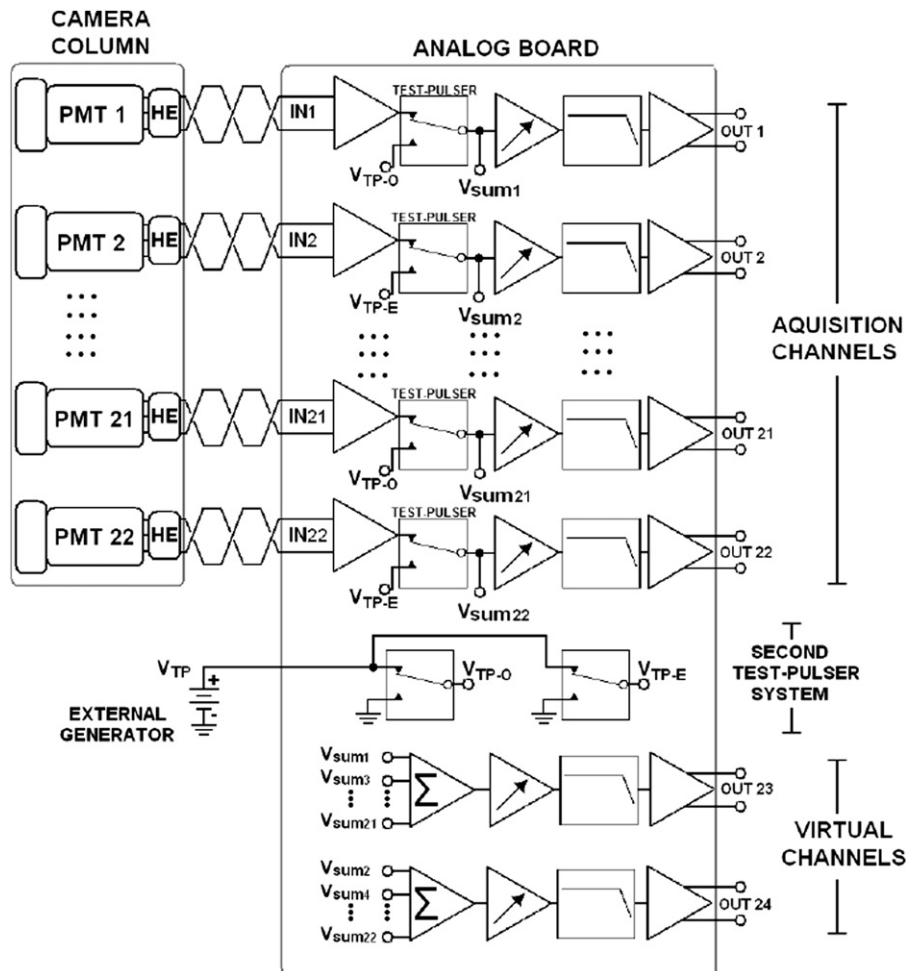


Fig. 2. Circuit block diagram of an analog board connected to a single camera column.

readout channels are optioned with two special additional channels set at a lower gain (~ 1.5 V/V) called “virtual channels” that permit to manage signals up to 2 V. The virtual channel solution is based on the fact that signals generated by different pixels in the camera are shifted in time and, generally, occupy only one of the 11 non-adjacent channels of the same column. To exploit this characteristic we consider the two groups formed with the odd and even channels. Signals from each group are added, properly conditioned and provide an extra virtual channel for the digitization at the FLT. These special channels are taken into account by the analysis only if one or more signals of the group of 11 are saturated.

3. Analog channel features and architecture

An analog channel provides signal conditioning for the analog signal generated by one PMT in such a way that it fulfills the requirements of the FLT board: the signal is amplified in order to exploit the voltage range required by the FADC on the FLT and filtered to satisfy the Nyquist sampling theorem.

As shown in the block diagram in Fig. 3, an analog channel can be divided into five stages:

- input stage;
- test-pulser;
- variable gain amplifier (VGA);
- anti-aliasing filter;
- output stage.

In the next subsections we will discuss the basic operations and the circuit details of above five stages.

3.1. Input stage

As it is well known, impedance matching is important to reduce reflections and preserve signal shape; when we have high signal frequencies the proper termination leads to a good signal reproduction. Furthermore, since the first stage gives the dominant contribution to the total noise of the readout channel, noise optimization has been the most critical step in the design procedure and in the choice of the operational amplifiers and the gain. Since we did not find an inexpensive differential receiver that met our noise requirements, we preferred a custom configuration in order to increase the performance/price ratio. We used the operational amplifiers LT6232 because of very low noise and large gain bandwidth product. The scheme employed is shown in Fig. 4, where the three op-amp configuration has been used for the highest precision and performance; the resistor tolerances are of 0.1% in order to maximize the common-mode rejection ratio. In addition, we have connected the non-inverting inputs of the first two op-amps before the R_G resistors because this peculiar configuration leads to a noise reduction, provided that the resistors values are selected properly.

The HE provides a fully differential configuration that drives a twisted pair cable that brings the signal to a single channel of the AB. The signal driver of the HE is based on a Maxim 4147 ESD, the input has a symmetrical network [10] and receives the PMT signal only through the leg connected to the PMT anode, whereas the second leg, identical to the first one, is not connected to the PMT. For this reason the HE generates a differential signal that is not symmetric (Fig. 5): the negative going pulse has a gain of 1.5, whereas the positive going pulse has a gain of 0.5. In addition the driver is DC biased at 1.5 V, with this configuration the negative pulse has more room before reaching the non-linear region. This

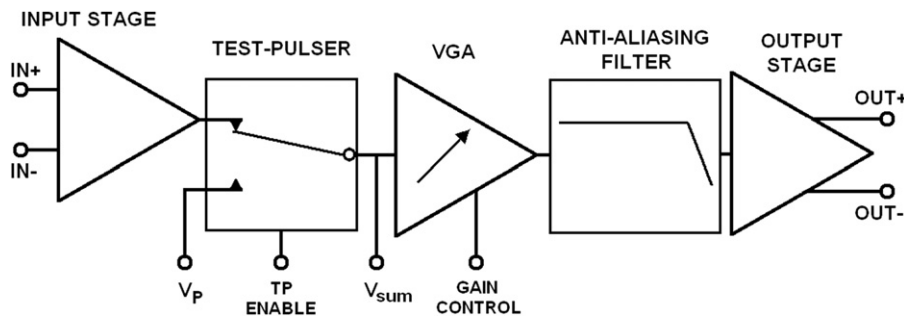


Fig. 3. Block diagram of a single analog channel.

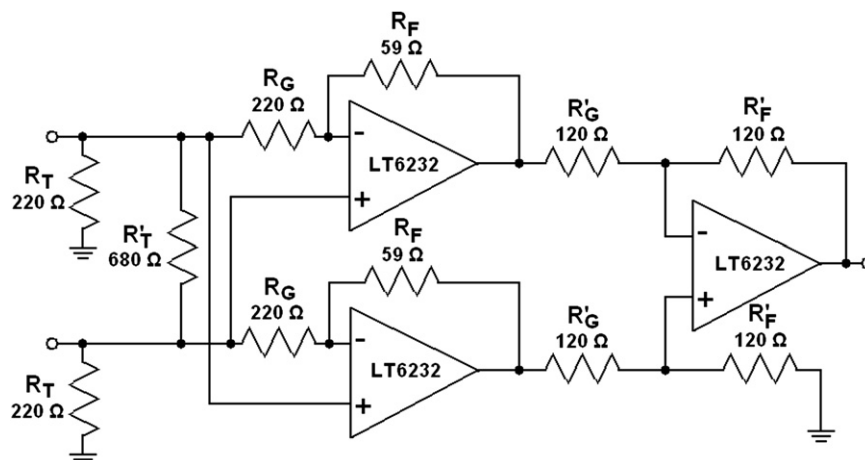


Fig. 4. Differential-to-single-ended receiver specifically designed for receiving the signals from the HE electronics over twisted pair cable.

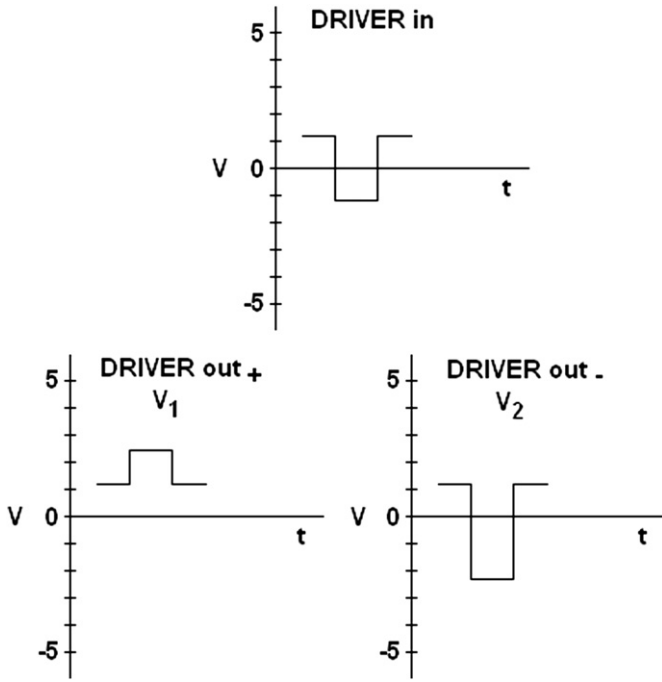


Fig. 5. Signal at the input and at both outputs of the HE driver.

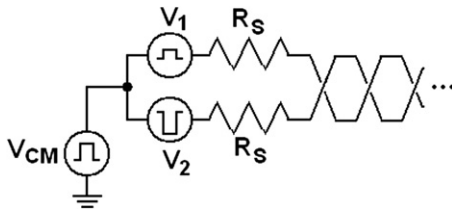


Fig. 6. Simplified scheme of the voltages generated on the twisted pair by the HE electronics: V_1 and V_2 form the differential signal and V_{CM} is the common-mode voltage.

asymmetry implies that the common-mode signal (V_{CM}) across the twisted pair is not zero, consequently it appears on both lines in phase and with equal amplitudes (Fig. 6). For that reason, it is very important to perform impedance matching for both differential signals and common-mode signals.

With the assumption that the operational amplifiers are ideal and using the virtual-gnd concept, looking at the input of the differential receiver (Fig. 4) we can express the input impedance Z_{diff} seen by the differential signal as

$$Z_{diff} = 2R_T \parallel R'_T \parallel R_G = 120 \Omega \quad (1)$$

while the input impedance seen from the common-mode signal is given by

$$Z_{cm} = R_T \parallel R_T = 110 \Omega. \quad (2)$$

The gain of the input stage (G_{in}) is determined by the equation

$$G_{in} = \frac{R'_F}{R'_G} \left(1 + 2 \frac{R_F}{R_G} \right) = 1.54 \quad (3.75 \text{ dB}). \quad (3)$$

This gain is the highest possible value that avoids non-linearities for input signals up to 2 V.

3.2. Test-pulser systems

The AB has two test-pulser systems that allow the injection of pulses with programmable width and amplitude in order to test

the analog blocks after the differential receiver and the digital functions of the FLT and SLT boards.

The first test-pulser system is placed on each acquisition channel after the differential receiver, as shown in Fig. 3. The repetition rate and the pulse width are digitally controlled by the FLT board, while the pulse amplitude is determined by an external voltage V_{TP} common to all the channels and generated by a DAC at the SLT (see Fig. 2). The basic element of this test-pulser is a digitally controlled analog switch, and the choice of the specific switch was mainly based on the transition times and the internal parasitic capacitance. We tested and compared the performances of some analog switches and choose the NLAS4599 (produced by On Semiconductor) that better fitted our application. The circuit configuration is shown in Fig. 7, and the basic concept of operation is as follows: the signal present at the input in_1 will be transferred to the output when the logic level (generated by the FLT board) present on the SELECT input is low, under this condition the channel works in normal acquisition. If the PMT is disabled, the voltage present at in_1 is zero; on the second input in_2 a constant voltage V_{TP} is present. If now we apply a signal on the SELECT input that commutes from low to high and then back to the low state, persisting a time t_w on the high state, at the output of the switch a pulse with an amplitude of V_{TP} and a width of t_w is generated.

A second test-pulser system (Fig. 2) digitally controlled by the FLT is implemented in the AB. It is composed by two analog switches (AD8170, from Analog Devices) with outstanding performances: the turn-on/turn-off times for these devices produce very fast rise/fall times. The first switch allows pulses to be injected in the odd channels and the second one in the even channels. The pulses generated by this second system (Fig. 8) are injected in the selected channel if the switch after the differential receiver is constantly switched on the pin “ in_2 ”.

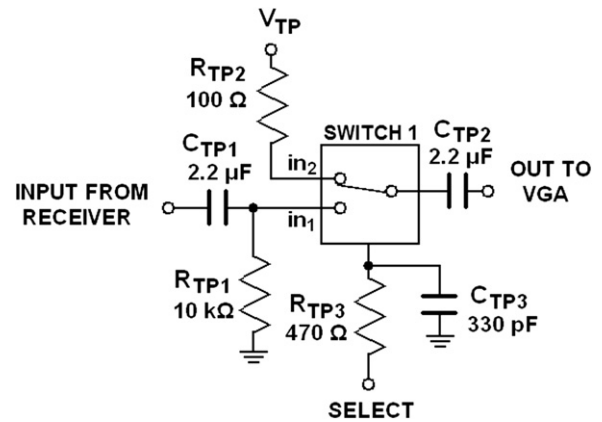


Fig. 7. The first test-pulser system placed after the differential receiver.

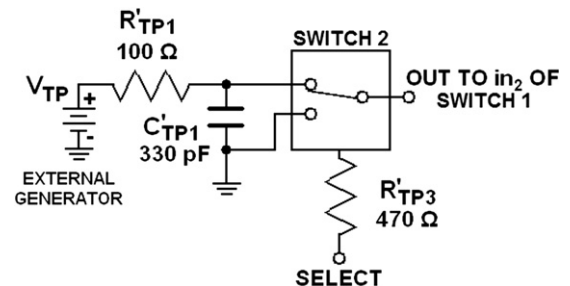


Fig. 8. The second test-pulser system.

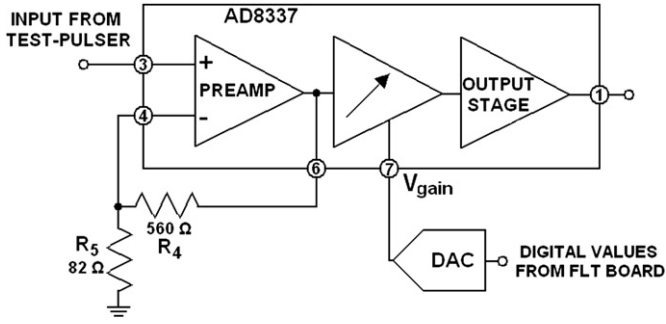


Fig. 9. Functional block diagram of AD8337 and circuit configuration.

3.3. Variable gain amplifier

A variable gain amplifier (VGA) is used to balance the gain spread of the PMTs. The VGA (see Fig. 9) is digitally controlled by the FLT board, and its total gain can change in steps of 0.006 dB from 12 dB to 36 dB, covering the whole expected range.

We selected the AD8337 for its wide bandwidth characterized by an excellent uniformity across the entire gain range (the -3 dB bandwidth is 280 MHz and it is flat in the range from 0 to 100 MHz), and good low noise characteristics.

The preamplifier stage of AD8337 is an operational amplifier whose gain is set by an external resistor network. We have configured it as a non-inverting amplifier with the gain (G_{pre}) established by fixed external resistors R_4 and R_5 :

$$G_{pre} = 1 + R_4/R_5 = 7.8 \quad (18 \text{ dB}). \quad (4)$$

With this configuration, the output is in phase with the input.

The second stage is a variable attenuator with a gain ranging from -24 dB to 0 dB. The voltage V_{gain} applied to pin 7 determines the gain of the stage, and the gain response, G_{att} , is linear-in-dB with respect to V_{gain} in the range from -0.6 V to $+0.6$ V. The voltage V_{gain} is set by adjusting the digital inputs (generated by the FLT board) of the 12-bit DAC.

The third stage is a Class AB, voltage-feedback, complementary emitter-follower with a fixed gain (G_{os}) of 18 dB.

The total gain of the VGA (G_{VGA}) is given by

$$G_{VGA} = G_{pre}G_{att}G_{os} = 61.96 \cdot G_{att} \quad (5)$$

or, transforming to decibels,

$$G_{VGA}(\text{dB}) = 35.84 \text{ dB} + G_{att}(\text{dB}) \quad (6)$$

with $-24 \text{ dB} \leq G_{att}(\text{dB}) \leq 0 \text{ dB}$.

3.4. Anti-aliasing filter

The purpose of the low-pass filter is to significantly attenuate the aliasing distortion due to the sampling process performed by the FADC placed on the FLT board.

To preserve the shape of the signals we designed a linear phase filter. In particular, a filter whose phase shift varies linearly with frequency is equivalent to a constant time delay for signals within the passband, consequently the shape of the signals is weakly distorted. A filter that optimizes this characteristic is the Bessel filter.

We have designed a fifth-order low-pass Bessel filter with a cutoff frequency of $f_c = 6.8$ MHz. One way to implement a filter with these characteristics is to cascade 1-pole Bessel low-pass filters to two 2-pole Bessel low-pass filters. The desired transfer function $H(s)$ of the filter can be written as follows:

$$H(s) = H_1(s)H_2(s)H_3(s) \quad (7)$$

Table 1

The coefficients for the fifth-order Bessel low-pass filter.

Filter	$a_i(s)$	$b_i(s^2)$
1	0.6656	0
2	1.1402	0.4128
3	0.6216	0.3245

where H_1 is a first-order transfer function, H_2 and H_3 are second-order transfer functions. In particular, the three transfer functions can be written as

$$H_1(s) = \frac{A_1}{1 + a_1s} \quad (8)$$

$$H_2(s) = \frac{A_2}{1 + a_2s + b_2s^2} \quad (9)$$

$$H_3(s) = \frac{A_3}{1 + a_3s + b_3s^2} \quad (10)$$

where $A = A_1A_2A_3$ is the passband gain, s is the complex frequency, and a_i and b_i are the Bessel filter coefficients reported in Table 1 [16].

In order to minimize the signal-to-noise ratio, the first stage is the one with the highest gain. In particular, A_1 is given by relation (5), and successive stages have unitary gain ($A_2 = A_3 = 1$).

The first section of the filter is placed between the analog switch and the VGA (Section 1 of Fig. 10). The operational amplifier of the preamplifier stage of the VGA is used as part of the filter. The transfer function of the circuit is given by

$$H_1(s) = \frac{A_1}{1 + R_3C_1s}. \quad (11)$$

The coefficient comparison between this transfer function, Eqs. (5) and (8) yields

$$A_1 = G_{VGA} \quad (12)$$

and

$$a_1 = R_3C_1. \quad (13)$$

Once the filter cutoff frequency f_c , the gain A_1 , and the capacitor C_1 are chosen, we solved for resistors R_3 and R_4 .

The second section of the filter (Section 2 of Fig. 10) uses the MBF (multiple feedback) topology and the transfer function of the circuit is ($R_8 = R_6$):

$$H_2(s) = \frac{-1}{1 + C_4(R_6 + 2R_7)s + C_4C_3R_6R_7s^2} \quad (14)$$

through coefficient comparison with Eq. (9) we obtain the relations

$$A_2 = -R_8/R_6 \quad (15)$$

$$a_2 = C_4(R_8 + R_7 + R_8R_7/R_6) \quad (16)$$

$$b_2 = C_4C_3R_8R_7. \quad (17)$$

The resistances R_6 , R_7 , and R_8 are found from Eqs. (15)–(17) after fixing C_3 , C_4 and A_2 .

The third section of the filter (Section 3 of Fig. 10) uses the MBF topology and the transfer function is ($R_{10} = R_{14} = R_{12} = R_{16}$, $R_{11} = R_{15}$ and $C_9 = C_{10}$)

$$H_3(s) = \frac{R_{12}/R_{10}}{1 + C_9(R_{11} + R_{12} + R_{11}R_{12}/R_{10})s + (2C_6)C_9R_{11}R_{12}s^2} \quad (18)$$

through coefficient comparison with Eq. (10) we obtain the relations

$$A_3 = R_{16}/R_{14} \quad (19)$$

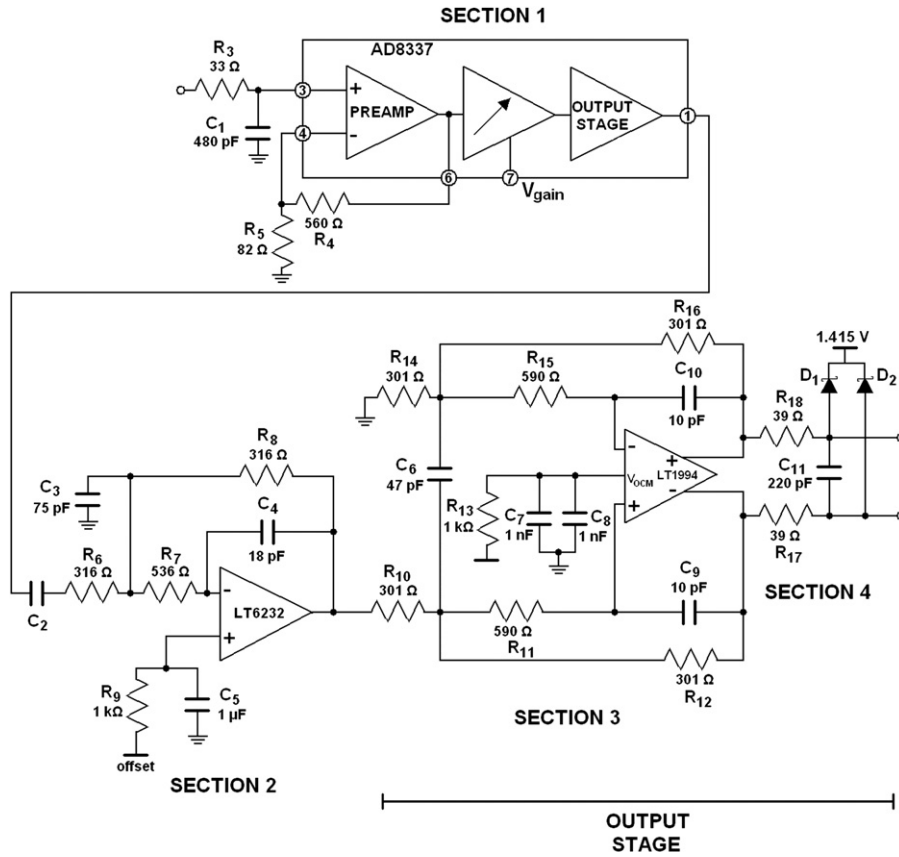


Fig. 10. The 5-pole Bessel low-pass filter using the AD8337, LT6232 and LT1994, and the output stage.

and

$$a_3 = C_9(R_{11} + R_{12} + R_{11}R_{12}/R_{10}) \quad (20)$$

$$b_3 = (2C_6)C_9R_{11}R_{12}. \quad (21)$$

Tolerance of components (resistors, capacitors and op-amps) imposes to take precaution; furthermore there are problems that can only be determined after PCB layout. After the production of the first prototypes, full characterization was made to check the full functionality. A small spurious oscillation between the first and second section of the filter was detected, as well as a somewhat unsatisfactory alignment of the cutoff frequencies and quality factors of the filter sections. For these reasons the actual values of a few resistors and capacitors of the filter were slightly modified and the cutoff frequency of the RC filter (Section 4 of Fig. 10) was lowered as explained in the next subsection. Acting in this way we have departed slightly from the expected response of the Bessel filter, but achieved a high stability.

3.5. Output stage

The op-amp employed for the output stage (Fig. 10, Section 3) is a fully differential input/output amplifier optimized to drive differential input FADCs.

Section 4 of the output stage is an RC low-pass filter and it was used for two reasons.

First, as we mentioned at the end of the last subsection, the anti-aliasing filter departs slightly from the expected response from the Bessel filter. For this reason the RC filter of Section 4 is employed to optimize the transient response. The transfer

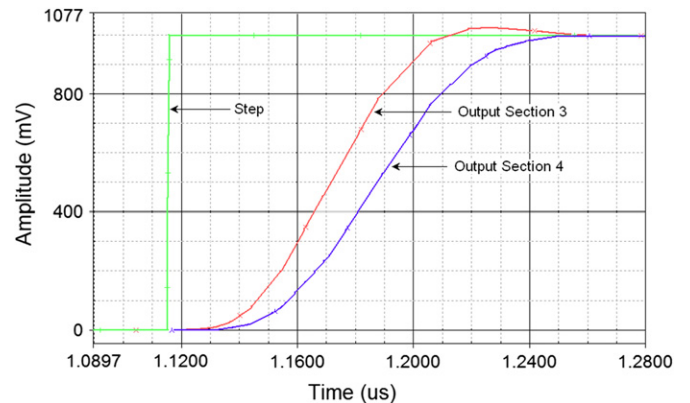


Fig. 11. Simulated step response at the output of Sections 3 and 4.

function of this RC low-pass filter is

$$H_4(s) = \frac{1}{\tau_{rc}s + 1} \quad (22)$$

and the cutoff frequency $f_{rc} (= 1/(2\pi\tau_{rc}))$ is given by

$$f_{rc} = \frac{1}{2\pi(R_{18} + R_{17})C_{11}} = 9.3 \text{ MHz}. \quad (23)$$

Figs. 11 and 12 show the simulated step and frequency responses at the output of Sections 3 and 4, respectively. From simulation we know that the cutoff frequency of the whole acquisition channel is about 5.5 MHz, and the rise time is about 63.8 ns.

Second, the FADC analog input circuit presents a finite complex (real and reactive components) input impedance which is

connected to the output stage of the analog channel, that adds transient currents coming from the switching action of the sample-and-hold function in the FADC. To minimize these transients we used the balanced RC filter, formed by R_{17} , R_{18} and C_{11} (Section 4 in Fig. 10), to assist the output stage in driving the load presented at the input stage of the FADC.

Finally, the circuit (Section 4 in Fig. 10) formed by the Schottky diodes D_1 and D_2 (model BAT54C), limits the signals to about 1.6 V peak-to-peak to prevent excessive voltage that could damage the FADC.

The gain of this stage is given by

$$G_{out} = R_{12}/R_{10} = 1 \quad (0 \text{ dB}). \tag{24}$$

3.6. Total gain of the readout channel

The gains of the main stages are given by the sum of Eqs. (3), (6), (24) resulting in the total gain of

$$G(\text{dB}) = G_{in} + G_{VGA} + G_{out} = 39.6 \text{ dB} + G_{att} \tag{25}$$

with $-24 \text{ dB} \leq G_{att} \leq 0 \text{ dB}$. In the end, the total gain can vary from 15.6 dB to 39.6 dB, with linear-in-dB characteristics.

4. Virtual channels architecture and features

Two virtual channels (those with number 23 and 24 in Fig. 2) allow to extend the range of the input signals up to 2 V. The structure of one virtual channel of the AB is shown in Fig. 13. The differences between a virtual channel and an ordinary channel are the input stage, the absence of the test-pulsar system, the preamplifier configuration of the VGA, and the different gain range required to match the input signals with greater amplitude to the FADC.

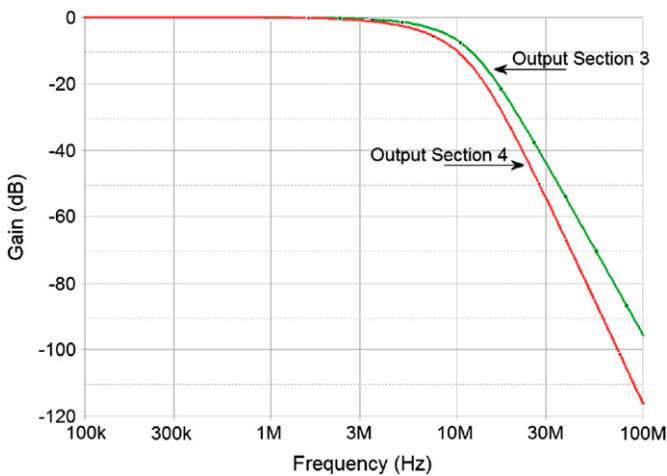


Fig. 12. Simulated frequency response at the output of Sections 3 and 4.

4.1. Analog adder

The first stage of the virtual channel is an analog adder. The virtual channel 23 sums the 11 voltages of the odd input signals, while the analog adder connected to channel 24 sums the 11 voltages of the even inputs. The 11 signals are taken from the output of the test-pulsers, as shown in Fig. 2.

In Fig. 14 the circuit configuration of the input stage of channel 23 is given. Since $R_{S1} = R_{S3} = \dots = R_{S21} = R_S$, we have that the output voltage V_S is given by

$$V_S = -\frac{R_{Sf}}{R_S}(V_{sum1} + V_{sum3} + \dots + V_{sum21}). \tag{26}$$

The gain of this circuit (G_{add}) is determined by the ratio of the resistors $R_{Sf} = 220 \Omega$ and $R_S = 4 \text{ k}\Omega$

$$G_{add} = -R_{Sf}/R_S = -0.055 \quad (-25.19 \text{ dB}). \tag{27}$$

With this configuration the output is out of phase with respect to the input.

Input signals from each of the 11 channels to the adder can be very large (even in excess of 3 V), the sum is surely greater, for this reason the adder attenuates the sum in order to not saturate

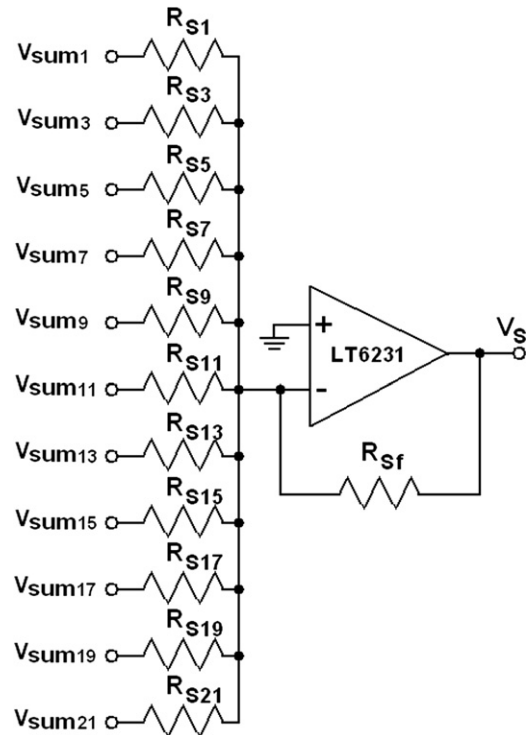


Fig. 14. Analog adder corresponding to the channel 23.

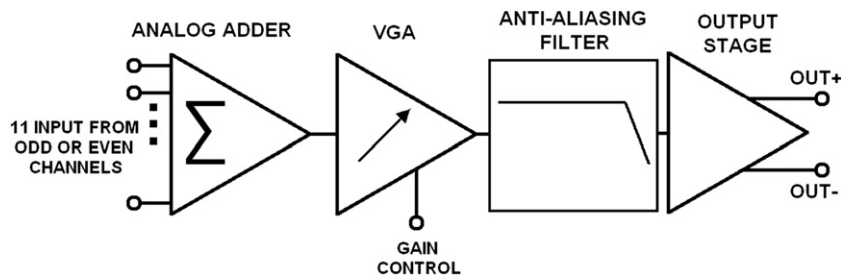


Fig. 13. Block diagram of the virtual channel.

the subsequent stages, in particular the preamplifier stage of the VGA. On the other hand for such big pulses noise is not an important issue.

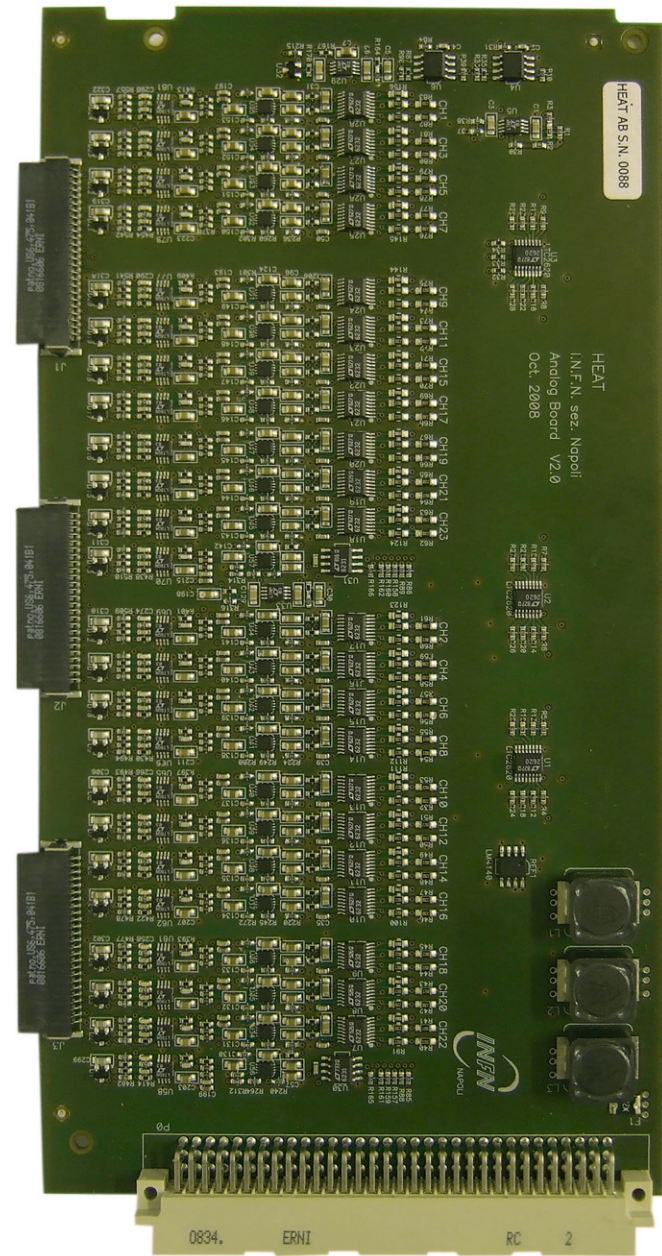


Fig. 15. Top view of one of the AB.

4.2. Total gain of the virtual channel

The preamplifier of the VGA is configured as an inverting gain amplifier in order to recover the original signal polarity, because the signal has been reversed by the previous stage. For this reason the gain of the first stage (G_{pre-vc}) of the VGA is given by

$$G_{pre-vc} = -R_4/R_5 = -6.8 \quad (16.7 \text{ dB}) \quad (28)$$

and the output is out of phase with respect to the input. The other two stages maintain the same gain configuration of a normal channel, so the total gain, G_{VGA-VC} , of the VGA is

$$G_{VGA-VC} = G_{pre-vc} + G_{att} + G_{att} = 34.6 \text{ dB}. \quad (29)$$

The gains of the main stages of a virtual channel are the sum of Eqs. (3), (27), (29), (24):

$$G_{vc}(\text{dB}) = G_{in} + G_{add} + G_{VGA-VC} + G_{out} = 13.2 \text{ dB} + G_{att} \quad (30)$$

with $-24 \text{ dB} \leq G_{att} \leq 0 \text{ dB}$. Finally, the total gain can vary from -11 dB to 13 dB , with linear-in-dB characteristics.

5. Tests and characterization

After production, all the 80 ABs were tested in our laboratory. One of them is shown in Fig. 15. In this section we describe the measurements made to characterize each readout channel of each AB.

As sketched in Fig. 16, the electronics test system was composed of a distribution board, the AB, the FLT board, a PC-controlled signals generator and an acquisition PC. The distribution board provides routing for signals and power supplies; the AB is the device under test; the FLT board digitizes the signals with 12-bit resolution and 20 MHz sampling rate, and transmits data to the acquisition PC.

On all the analog channels (for a total number of 1920) the following measurements have been systematically and automatically performed:

- linearity;
- frequency response;
- gain as a function of value set to the DAC controlling the VGA;
- common-mode rejection ratio (CMRR);
- equivalent input voltage noise;
- test pulsing functionality.

5.1. Linearity

Linearity is a desirable characteristic of all systems where an output response is required to be a faithful reproduction (except for a constant scale factor, the gain of the system) of one or more inputs.

We characterized the linear response of each acquisition channel injecting pulse signals of known shape. A typical response is shown in Fig. 17. We determined the integral non-linearity of whole system (AB+FLT board) and typical values are better than

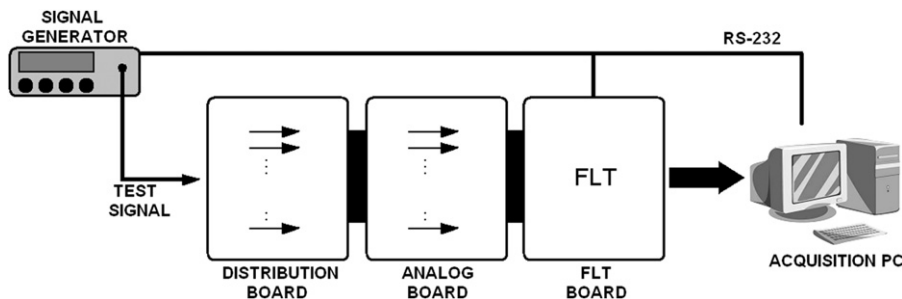


Fig. 16. Test setup.

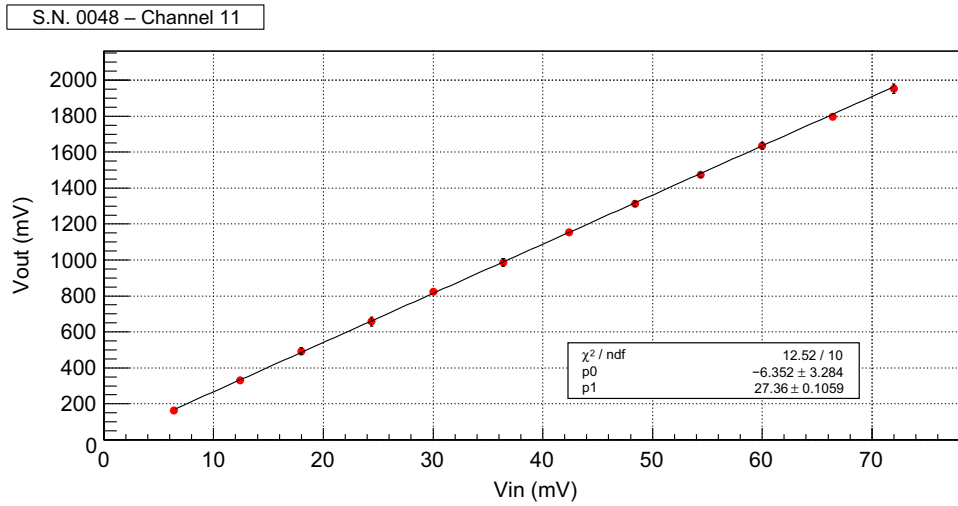


Fig. 17. Typical linear response of an acquisition channel.

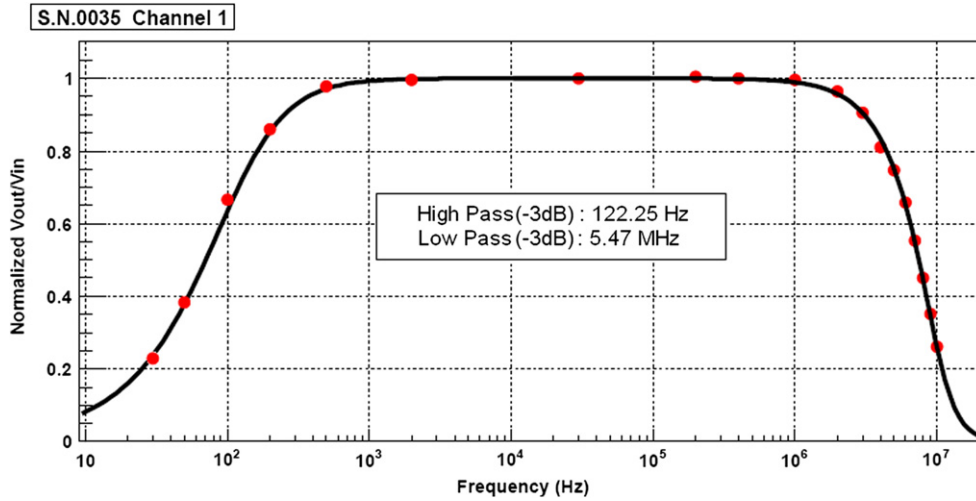


Fig. 18. Typical filter characteristic.

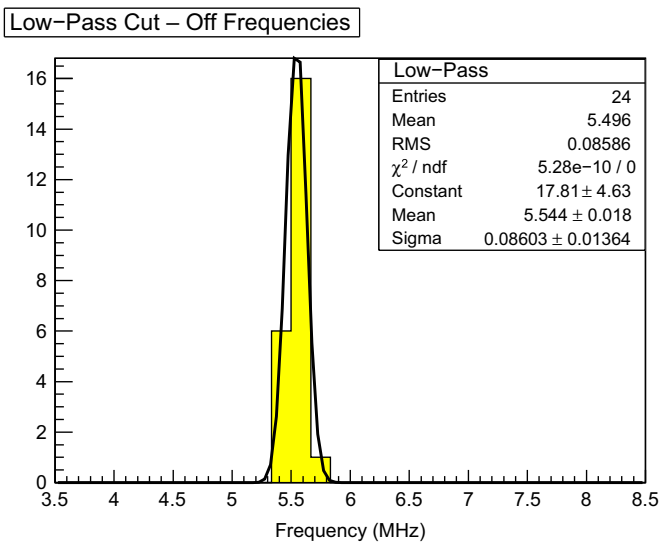


Fig. 19. Distribution of the low-pass cutoff frequencies of a single AB.

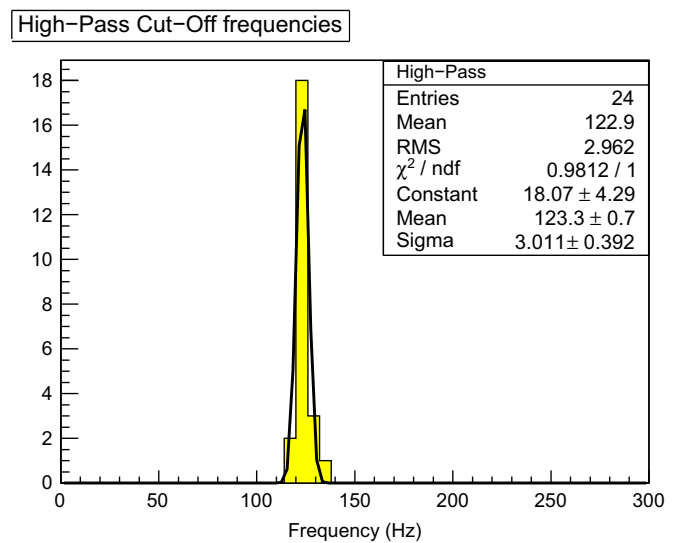


Fig. 20. Distribution of the high-pass cutoff frequencies of a single AB.

0.6%. In addition, we measured the departure from the linearity of the analog channel at the maximum of the dynamics: fitting all points but the last and measuring the residual of the last point from the fit. We found that typical deviations are within 0.1%.

5.2. Frequency response

The frequency response of each channel was measured sweeping a constant-amplitude sinusoidal signal through the bandwidth of interest and measuring the amplitude of the signals at the outputs of the channels.

The experimental points of the frequency response at frequencies higher than 200 kHz were fitted with the function

$$G_H(\omega) = |H(s)| = |H_1(s)| \cdot |H_2(s)| \cdot |H_3(s)| \cdot |H_4(s)| \tag{31}$$

where $H_1(s)$, $H_2(s)$, $H_3(s)$ and $H_4(s)$ are given by Eqs. (11), (14), (18) and (22), respectively.

In the low frequency range the experimental data were interpolated with the amplitude response $G_L(\omega)$ given by

$$G_L(\omega) = \frac{1}{\sqrt{1+(\omega_L/\omega)^2}} \tag{32}$$

Typical frequency response of a single channel is shown in Fig. 18. Figs. 19 and 20 show typical distributions of the low-pass and high-pass cutoff frequencies of the 24 channels of a single AB, respectively. In Fig. 21 the step response of an analog channel is shown, and the measured rise time is 63.5 ns.

5.3. Gain as function of digital values generated by the FLT board

The total gain of the readout channels was measured injecting a signal with constant parameters and by varying the digital values generated by the FLT board from 0 to 4080 in steps of 204 to set the VGA. Typical linear-in-dB responses of a single acquisition channel and a virtual channel are reported in Figs. 22 and 23,

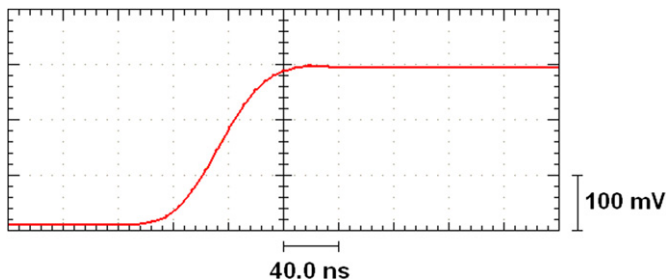


Fig. 21. Typical step response of an analog channel. This measurement has been performed using an oscilloscope.

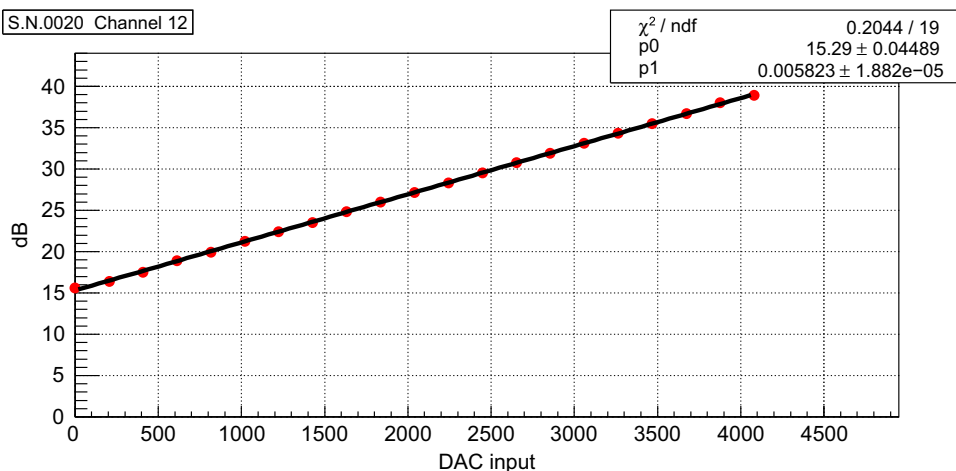


Fig. 22. The measured linear-in-dB relationship between channel gain and digital values generated by the FLT.

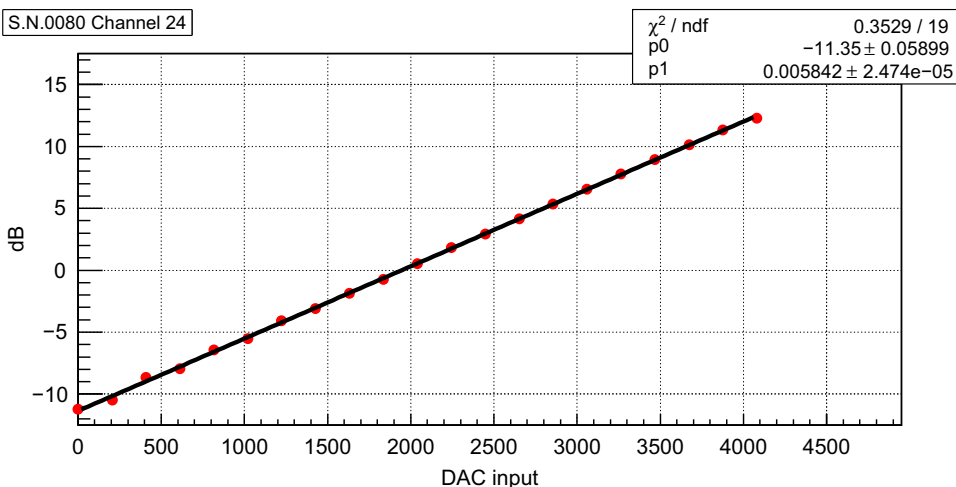


Fig. 23. The measured linear-in-dB relationship between virtual channel gain and digital values generated by the FLT.

respectively. We evaluated the integral non-linearity and typical values are better than 0.46%.

5.4. Common-mode rejection ratio

The output signal of a readout channel can be expressed as

$$v_{out} = A_d v_d + A_{cm} v_{cm} \tag{33}$$

where A_d is the differential-mode gain and A_{cm} the common-mode gain, v_d the difference between input signals (v_+ and v_-) and $v_{cm} = 1/2(v_+ + v_-)$ the common-mode input signal. The common-mode rejection ratio (CMRR) is defined as the ratio of the differential-mode gain A_d to common-mode gain A_{cm} :

$$CMRR = 20 \log(A_d/A_{cm}). \tag{34}$$

To evaluate the CMRR as a function of the frequency we feed the differential inputs with the same sinusoidal signal ($v_+ = v_- = A \sin[\omega + \phi_0]$, varying ω in the desired range). First we set the gain to the typical value of 30 and then measured the output and the input voltages, from which we calculated A_{cm} as the ratio of the output voltage and common-mode input voltage. The differential-mode gain was measured injecting two sinusoidal signals with the following characteristics: $v_+ = A \sin[\omega + \phi_1]$ and $v_- = A \sin[\omega + \phi_2]$, with $\phi_1 - \phi_2 = \pi$, and varying ω as in the previous measures. Then we measured the output signal, from

which we calculated A_d . In the end, we evaluated the CMRR defined by Eq. (34).

Typical common-mode gain and CMRR at operational differential gain are reported in Figs. 24 and 25, respectively.

5.5. Equivalent input voltage noise

From the characteristics of the selected components the expected equivalent input voltage noise of each stage has been estimated as reported in Table 2.

The total equivalent input voltage noise (e_n) of a readout channel at a typical gain ($G \sim 30$) has been estimated by adding the squares of the sources introduced by the main blocks of the

Table 2

Equivalent input voltage noise estimated for the five stages. The gain of the channel is fixed at 30.

Input stage, e_{n1} (nV/ $\sqrt{\text{Hz}}$)	Test-pulser, e_{n2} (nV/ $\sqrt{\text{Hz}}$)	VGA+ filter (first pole), e_{n3} (nV/ $\sqrt{\text{Hz}}$)	Filter (two 2-pole)+ output stage, e_{n4} (nV/ $\sqrt{\text{Hz}}$)
3.2	0	3.0	10.3

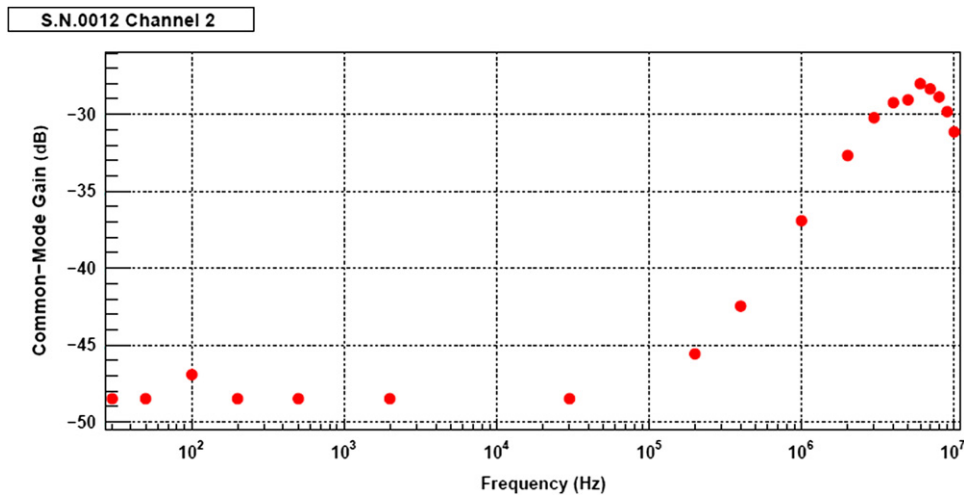


Fig. 24. Typical common-mode gain in dB vs. frequency.

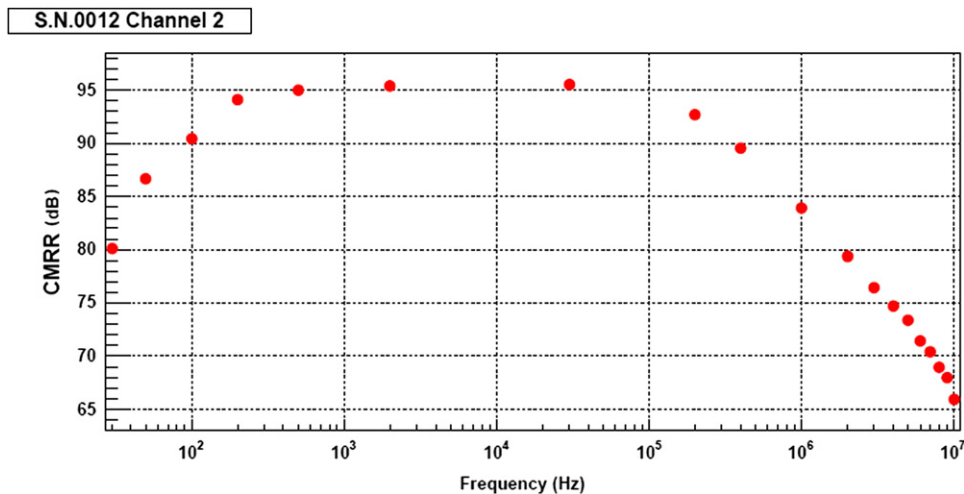


Fig. 25. CMRR at typical differential gain (~ 30) vs. frequency.

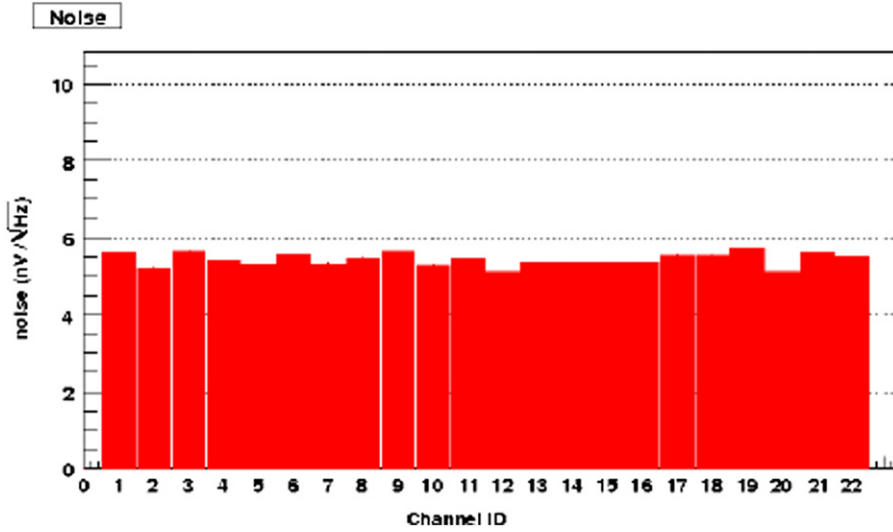


Fig. 26. Equivalent input voltage noise at working gain.

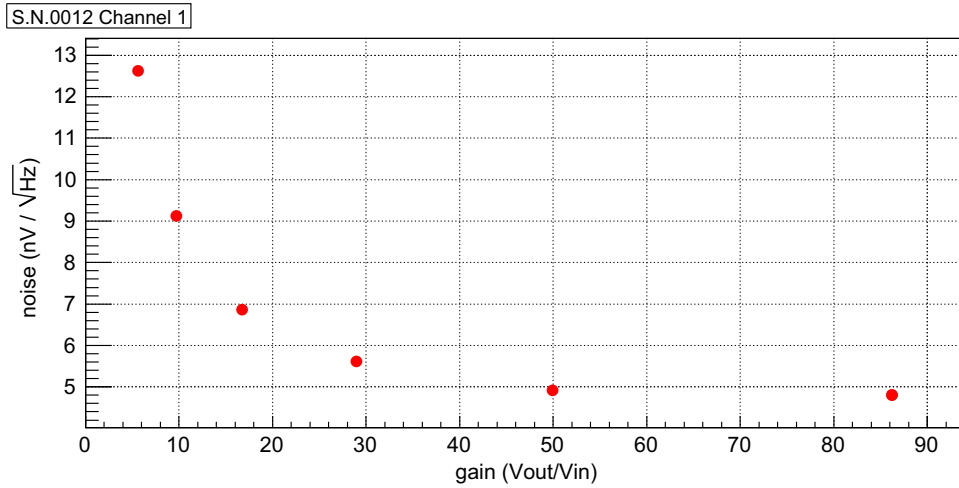


Fig. 27. Equivalent input voltage noise as function of gain.

channel (all sources obviously uncorrelated):

$$e_n = \frac{G_{out} \sqrt{\left[G_{VGA} \sqrt{(e_{n1} \cdot G_{in})^2 + e_{n3}^2} \right]^2 + e_{n4}^2}}{G} \approx 4 \text{ nV}/\sqrt{\text{Hz}}. \quad (35)$$

This is much lower than the expected sky background (about $40 \text{ nV}/\sqrt{\text{Hz}}$ during the darkest nights).

The equivalent input voltage noise has been measured for each channel. Typical channel spread and dependence on gain setting are reported in Figs. 26 and 27, respectively. The measured noise is slightly higher than the expected value calculated in Eq. (35) because the noise introduced by the distribution board was not taken into account (see Fig. 16).

The virtual channels present a different equivalent input voltage noise because they add the noise of 11 differential receivers, and the equivalent input voltage noise introduced by the adder circuit (about $5.1 \text{ nV}/\sqrt{\text{Hz}}$) must be taken into account. Furthermore, since the gain is lower, the noise introduced by the ADC is not negligible as in the case of normal channels. The measured equivalent input voltage noise of a virtual channel is

about $80 \text{ nV}/\sqrt{\text{Hz}}$. Again the measured noise is much lower than the expected sky background.

6. Conclusions

We have developed the new analog board for the High Elevation Auger Telescopes. The AB is a multi-channel system: 22 channels receive the signals from 22 PMTs of a single camera column, and each channel provides signal conditioning for the analog signal generated by one PMT; two virtual channels allow recovery of signals with a high voltage range. The main goals of the new design are enlarged bandwidth, increased dynamic range and improved signal-to-noise ratio. In particular, although the bandwidth has been doubled with respect to the analog boards of the other 24 telescopes the electronic noise at each channel is reduced at least by a factor 3.

Our production tests showed that the main circuit parameters of all readout channels comply with the requirements of the new front-end electronics developed to increase the trigger efficiency of the new fluorescence telescopes.

The complete system has been installed at the Auger South Observatory in Argentina, and since the end of 2009 is used to detect EAS in the desired energy range.

Glossary

AB	analog board
AMIGA	Auger muons and infill for the ground array
DAC	digital-to-analog converter
EAS	extensive air shower
FADC	flash analog-to-digital converter
FD	fluorescence detector
FLT	first level trigger
FPGA	field programmable gate array
HE	head electronics
HEAT	high elevation Auger telescopes
MBF	multiple feedback
PCB	printed circuit board
PMT	photomultiplier tube
SD	surface detector
SLT	second level trigger
TLT	third level trigger
VGA	variable gain amplifier

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