Received 24 May 2021; revised 15 July 2021 and 2 August 2021; accepted 30 August 2021. Date of publication 6 September 2021; date of current version 22 September 2021.

Digital Object Identifier 10.1109/OJSSCS.2021.3110461

Design Considerations for a Sub-mW Receiver Front-End for Internet-of-Things

EHSAN KARGARAN, DANILO MANSTRETTA (Member, IEEE), AND RINALDO CASTELLO (Life Fellow, IEEE)

(Invited Paper)

Microelectronic Group, University of Pavia, 27100 Pavia, Italy

CORRESPONDING AUTHOR: E. KARGARAN (e-mail: ehsan.kargaran01@universitadipavia.it)

ABSTRACT Internet-of-Things (IoT) and Wireless sensor networks (WSNs) require very low power transceivers. This paper presents techniques for minimizing power consumption of receiver (RX) frontends for short range wireless links. Two key approaches, i.e., current reuse and supply voltage reduction are compared. Different RX architectures such as direct-conversion, low-IF, sliding IF as well as phase-tracking RX, are compared, emphasizing their potential and limitations when targeting sub-mW RX power dissipation. Low-power design techniques for LNA, frequency generation blocks and baseband amplifiers are presented. As a case study, an efficient low-IF RX front-end for IoT is described in detail. In 28 nm CMOS, such a receiver occupies an active area of 0.1 mm^2 and consumes only 350 μW from a 0.9 V supply while showing a minimum in band NF of 6.2 dB. The achieved performance is very competitive with state-of-the-art ultra-low-power receivers, while consuming the lowest power.

INDEX TERMS Ultra low-power (ULP), current reuse, gm-boosting, complex filter, IoT, ultra-low-voltage (ULV).

I. INTRODUCTION

THE EXPLODING demand for ubiquitous communications has created significant attention toward the development of wireless sensor networks (WSNs) and Internet-of-Things (IoT) for both sub-GHz and 2.4 GHz ISM band. While sub-GHz wireless systems show longer operation range and are better suited for wide area network communications, the 2.4 GHz ISM band has become very popular for short-range communications, based on widely used standards like Bluetooth Low Energy (BLE) or ZigBee [1]–[2] on which this paper is focused. In many applications such as WSNs, continuous communication is not required. Thus, to further lower the average power dissipation, the main receiver is kept off for most of the time and a Wake-UP receiver (WuRX) with extremely low power dissipation is used to detect the signal and turn-on the main RX. Recently reported WuRXs dissipate sub-μW power [3]–[7]. This gives an energy consumption which is equal or smaller than the one of the main receiver even for a 0.1% duty cycle. Even though we focus here on the active power of the main RX, its sleep power is also very important. Achieving nW-range sleep power without affecting the active performance is not trivial and is an important research subject [9]. Therefore, the major challenge in these applications is designing low-cost RF transceivers with ultra-low power (ULP) consumption while meeting the required performance level. For instance, BLE requires a minimum sensitivity of −70 dBm, i.e., a noise figure (NF) of 29 dB for a typical signal-to-noise ratio (SNR) of 15 dB [8], 21 dB image rejection and better than −35 dBm IIP3 [1]. Owing to the very relaxed BLE specifications, it is highly desirable to reduce the cost and power consumption in short-range communication devices. Most RF transceivers for BLE trade-off power consumption with sensitivity (i.e., receiver NF). As an example, state-of-the-art BLE transceivers [9]–[14] with sub-mW power consumption have a NF above 10 dB [9]–[10], while they consume over 1.5 mW for a NF below 6.5 dB [11]–[14]. This paper is a review of design techniques for ULP receiver (RX). Power optimization is a complex task, involving the choice of the architecture, the design of the building blocks as well as their co-optimization. Depending on the available supply voltage, different architectures and circuit solutions are more

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

appropriate. In Section II, current reuse and supply voltage reduction as two common approaches for minimizing power consumption are compared. The pros and cons of 4 different RX architectures targeting ULP applications are studied in Section III. In Section IV, the fundamental limitations in term of power consumption for each building block of a sub-mW RX are discussed. Then, Section V gives measurement results for the case study described in [15] which has the lowest power consumption with a very competitive NF among all prior sub-mW RX. Finally, a broad comparison among state-of-the-art ULP RX is given in Section VI while some general conclusions are drawn in Section VII.

II. CURRENT REUSE VS ULTRA-LOW SUPPLY VOLTAGE

Power minimization demands a careful choice of the receiver architecture and of the circuit topologies. Depending on the application and the available power supply, different design approaches are adopted. In systems relying on energy harvesting, the extremely low (down to 0.2−0.3 V) and varying supply voltage is a fundamental challenge [16]. Low-voltage boost converters require external bulky inductors and capacitors and have poor efficiency [17]. An attractive approach is to lower the supply voltage of the radio [11]. so that it can be connected directly to the harvester. The power dissipation of the receiver scales down with the supply but the use of a drastically reduced supply voltage makes designing ULP receivers even more challenging. It prevents stacking of devices, limiting the achievable reverse isolation and the maximum available gain in amplifiers. The RX in [11] has a minimum supply voltage of 0.3 V, it adopts forward body biasing to lower the active devices threshold voltage and transformer coupling to avoid transistor stacking. It achieves a sensitivity of −91.5dBm (i.e., 6.1 dB NF), dissipating 1.6 mW but the chip area is large (2.5 mm^2) due to many transformers used between stages. The implementation of key circuits such as frequency dividers is prohibitive at very low supply voltages, imposing to the choice of unconventional architectures. The lowest voltage frequency divider reported in the literature, to the best of our knowledge, is [72], working at 0.5 V. Thus, at very low supply voltages, a lossy quadrature splitter should be employed in the signal path, either after LNA [9] or before LNA [10], thus degrading the NF. Even though it is plausible to raise the internal supply by CP [9], this increases chip area and power dissipation. The receiver in [9] pushes the supply down to 0.18 V, achieving a power dissipation of only 382 μW. The classical flip-flop-based quadrature frequency dividers are eliminated using a carrier-frequency VCO with passive quadrature splitter in the RF path. This lowers the power, but it lowers the gain and increases the noise of the RF path. Transistor stacking is avoided in the LNA, relying on inductors and transformers, while integrated switched-capacitor charge pumps (CPs) are used to supply blocks that need higher voltages, such as the baseband amplifiers. The NF is 11.3 dB and the IIP3 is −12 dBm, greatly exceeding the BLE specifications. However, a large chip area of 1.65 mm^2 results due to CPs, inductors, and transformers. Moreover, running the VCO at the carrier frequency increases the risk of VCO pulling.

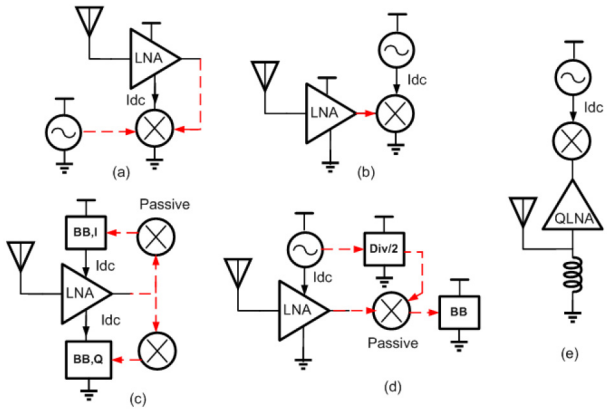

FIGURE 1. Current reuse receiver configurations: (a) Low noise converter [20] (b) Self-oscillating mixer [21], (c) Stacked LNA-BB [19], (d) Stacked LNA-VCO [36], (e) QLMV [10].

Portable devices are typically powered by a single cell battery ranging from 1 to 1.8 V. The natural approach to save power is current reusing [10], [18]–[22]. This can be done within a single block (e.g., the LNA in [23] reuses the same current in four transistors that work effectively in parallel) or by stacking different receiver building blocks. Combining the LNA and the downconverter, the so-called low-noise converter is obtained, as shown in Fig. 1 (a) [20]. This configuration can achieve an adequate down-conversion gain but typically has a relatively poor noise figure (NF). Combining oscillator and mixer [21] into a self-oscillating mixer (SOM) represents another current-reuse possibility, as shown in Fig. 1 (b). SOM typically have poor down-conversion gain and NF, creating the need for a low-noise pre-amplifier. Amplifying both RF and down-converted signal in the same block is a possibility proposed in [18] for the so-called "recursive receiver". On the other hand, processing RF and IF signals with the same device can increase distortion and care is required to prevent noise degradation. In [18] the RX draws 2.6 mA from 1.2 V with a NF of 8.2 dB. The extra generated distortion leads to an IIP3 of −41 dBm which is often too low. Another reuse approach is to recycle the current in different blocks. In [19], as shown in Fig. 1(c), the first stage of the baseband amplifier reuses the LNA bias current. An excellent OOB-IIP3 of 6 dBm is reported while drawing 2.4 mA from a 1.8 V supply. Still the power consumption exceeds the desirable 1 mW limit for IoT applications. In [10] (shown in Fig. 1 (e)), LNA, mixer, VCO and baseband input stage are stacked to recycle 530 μA from a 0.8 V supply. The interactions between stacked blocks generally leads to higher noise (NF is 15 dB in [10]) and makes the VCO more vulnerable to pulling from large blockers.

This section introduced pros and cons of a drastically reduced supply voltage versus recycling the bias current within two or more different circuits while using a higher

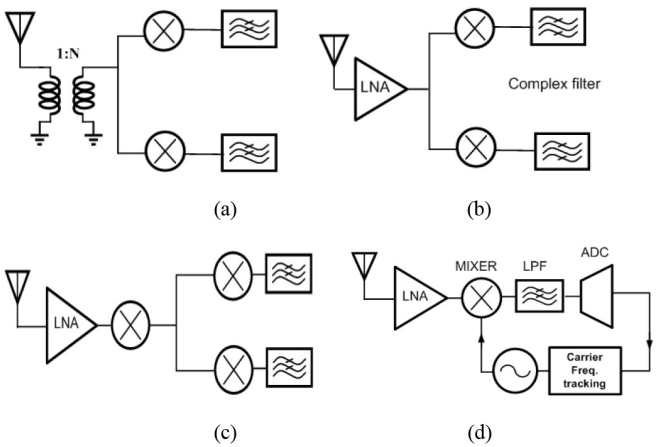

FIGURE 2. Example of RX architecture, (a) DCR RX [51], (b) Low-IF RX [10], (c) Sliding IF [30], (d) Phase-tracking RX [32].

supply voltage as two common approaches found in the literature to reduce power consumption. Often system supply voltage is much higher than the minimum supply-voltage required for sub-circuits. Lower supplies can be generated power efficiently using charge pumps with inductors, but this takes significant extra chip area. It may then be both power and area efficient to stack circuits while re-using supply current. In fact, no on-chip CPs are required to supply baseband amplifiers and frequency dividers , thus improving power efficiency and reducing chip area. Besides, complementary LNAs without inductive loads can be used, which greatly reduces the chip area. For instance, in [24] a 60 μW LNA that uses inverter-based amplifiers achieves a NF of 5.3 dB. In [23] two LNAs both consuming 30 μW, one based on current reuse and the other with a 0.18 V supply, are compared. The former has smaller area and lower noise.

III. ULP RECEIVER ARCHITECTURES

ULP receivers use different architectures, as shown in Fig. 2, with none clearly emerging as the best one. In this section, the pros and cons of recently reported architectures are examined.

A. DIRECT CONVERSION RX (DCR)

The main advantage of a DCR architecture is the drastic reduction of the image rejection required since it has a self-image with the same strength as the desired signal [25]. Thanks to current reuse, the DCR in [26] has a NF of 5.2 dB (i.e., sensitivity of −95.1 dBm) burning 1 mW. Power consumption cannot be easily lowered without degrading NF or exploiting advanced CMOS technology. For instance, the sub−600μW DCR in [27] that uses translational positive feedback from BB to RF to perform input matching and improve linearity has an OOB IIP3 of 3.3 dBm and a 12 dB NF. For narrowband systems such as BLE, flicker noise is an additional issue in DCR.

B. LOW-IF RX

Low-IF, shown in Fig. 2(b), may be the most appealing architecture to eliminate the DCR issues. Image rejection and channel selection can be implemented with complex filters, but care is required to minimize power dissipation. Image rejection requirements are very relaxed for BLE if the intermediate frequency (IF) is chosen carefully. An IF of 1 MHz or less demands very high selectivity to filter out flicker noise and DC offsets, while an IF of 3 MHz requires more selectivity to filter out blockers at higher frequencies. An IF of 2 MHz is often chosen as a compromise. By exploiting current-reuse and complex filter the low-IF RX reported in [10] has a NF of 15 dB consuming 600 μW. The RX in [28] burns 2.7 mW and has a NF of 9 dB.

C. SLIDING-IF RX

The sliding-IF (SIF) architecture, shown in Fig. 2(c) saves power in the mixer driver thanks to the reduced frequency of the quadrature LO [29]–[31]. Image filtering, however, is its main issue. For $f_{IF} = f_{RF}/n$ and $f_{LO} = f_{RF}(n-1)/n$, a smaller n, i.e., a higher IF, relaxes the image filtering at the cost of more LO power. A popular choice is $n = 5$. An LC filter is usually added at the LNA output, providing 31−35 dB image rejection ýý. The LC filter, however, by loading the current-switching passive mixer reduces the baseband driving impedance which increases noise. A 2nd LNA stage or an active mixer can be used instead, but this leads to higher power and noise. The SIF RX in [30] employs an LNA with an image filtering followed by an all-passive voltage-mode mixer, where the switches impedance is larger than their driving impedance. Switch size must be carefully chosen to avoid linearity and noise degradation. Excluding VCO and relying on off-chip matching, the RX consumes only 640 μW with a NF of 6.5 dB.

D. PHASE TRACKING RX (PTRX)

Thanks to its constant-envelop modulation, the BLE RX can use a phase-demodulation loop. In its simplest implementation the RX signal is down-converted by a mixer, acting as a phase detector, directly driven by the VCO, which is part of the phase-tracking loop (Fig. 2(d)). Power consumption can be reduced since there is no need for quadrature LO and baseband circuits [32]. This basic architecture, however, is prone to VCO pulling by strong interferers, mandating power-hungry LO buffers. Different solutions have been developed to address this issue. Reference [33] describes a PTRX based on a SIF architecture. The frequency dividers generate a 16-phase IF clock signal and the feedback loop is closed in digital, acting on the IF clock phase selection. Noise shaping is used to further reduce phase quantization error. Like cartesian SIF receivers, this solution suffers from the image problem and the high-speed digital circuitry requires considerably power consumption. In phase tracking DCR an efficient way to address phase pulling from both on chip coupling and strong interference is to use a sub-harmonic oscillator followed by a frequency doubler [34]. Thanks to techniques like current reuse, low supply, forward body bias and the use of an LO with no quadrature, such an RX consumes 750 μW with a NF of 7.1 dB. Finally, since

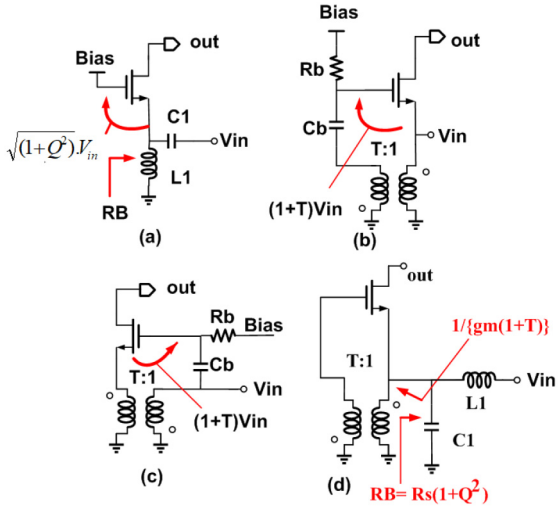

FIGURE 3. Impedance matching network in CG topology using (a) L-match network, (b) passive gate boosting network [39], (c) power efficient passive source boosting in [40], (d) Proposed input matching in [15].

in PTRX LNA and VCO may dissipate over 2/3 of the power [32]–[33], it is promising to stack LNA and VCO to reduce power. For instance, the stacked LNA-VCO, shown in Fig. 1 (d), requires only 72μW from a sub-1V supply with performance sufficient for the application [36].

IV. LOW POWER RX BUILDING BLOCKS DESIGN

A. LNA

The first block of the RF frontend is the LNA, which performs input matching and low noise amplification. Source impedance boosting, active feedback and inductive source degeneration are common approaches to lower its power. The noise-power tradeoff for those LNA topologies is explored in [23]. Among these topologies, inductive source degeneration is the most popular one. It can be designed to substantially lower power consumption while adding little noise at the cost of using a big inductor at the gate terminal. This inductor it is generally placed off-chip leading to excellent noise but also to higher cost and board complexity [23]. In [37] inductive source degeneration is used for a pn structure to lower power consumption with the inductors placed on-chip. For such an LNTA an IIP3 of −7.5 dBm while consuming 170 μW from a 0.7V supply voltage is reported. However, the chip area is large due the presence of three integrated inductors [37]. On the other hand, low power Common Gate (CG) LNA using novel re-use techniques have good potential to reduce the active area while preserving good noise and linearity [15], [38]. In the following, the noise-power tradeoff for CG LNA topologies will be initially examined. This leads to the ULP CG LNA with performance sufficient for the BLE applications to be discussed shortly [15].

For a standard CG LNTAs, input matching defines the device transconductance (gm), making it unsuitable for ULP applications. Scaling up the source impedance using an L-matched network (Fig. 3a) lowers power consumption

TABLE 1. The comparison between different input impedance matching networks for CG topology.

	Device gm	Noise Factor	Gm
L-Match network	$g_m = \frac{1}{R_s(1+Q^2)}$	$F \geq 1+\gamma$	$G_m = \frac{1}{\sqrt{(1+Q^2)}.R_s}$
Gate boosting	$g_m = \frac{1}{R_s(1+T)}$	$F \geq 1+\frac{\gamma}{(1+T)}$	$G_m = \frac{1}{R_s}$
Source Boosting	$g_m = \frac{1}{R_s T(1+T)}$	$F \geq 1+\frac{T.\gamma}{(1+T)}$	$G_m = \frac{1}{R_s T}$
Combined L-Match & Gate boosting	$g_m = \frac{1}{R_s(1+T)(1+Q^2)}$	$F \geq 1+\frac{\gamma}{(1+T)}$	$G_m = \frac{1}{\sqrt{(1+Q^2)}.R_s}$

while preserving matching. However, excessive scaling-up can be a problem since it lowers the LNTA transconductance gain (Gm), making the noise of the following stages more important, it increases sensitivity to parasitic, degrades the NF due to losses in the input network and it degrades linearity because of the amplified input voltage. Passive gain boosting using a transformer with a turn ratio T to boost the gate (Fig. 3b) or the source (Fig. 3c) also lowers the power needed for input matching [39] in addition to reducing noise. The required gm is reduced by (1 + T) compared to the simple CG. Ideally increasing T increases the boosting factor, further lowering the noise of the active device and the dissipated power. However, increasing T increases transformer loss, which at some point may result in a larger NF. In practice it is difficult to have on chip transformers with T larger than 3. In Fig. 3d [15], the input matching network combines an L-match circuit (with a given Q) with passive gate boosting. The input signal is first amplified by the L-match network. This increases the driving impedance by $1 + Q^2$ and correspondingly lowers the power required for matching by the same value. In addition, passive gain boosting is employed to amplify the gate to source voltage. The circuit is simulated using ideal passives to evaluate the minimum achievable NF and required device gm versus T and Q. From Table 1 and Fig. 4a, for a given T increasing Q, lowers the required device gm (i.e., lowers power) at the cost of a lower LNA Gm with the same NF. For instance, for T = 1 and Q of either 1 or 1.7, the device gm is 1/(4Rs) or 1/(8Rs) while the Gm is $\sqrt{2}$/(2Rs) or 1/(2Rs) respectively with a NF of $1+\gamma/2$. On the other hand, for a given Q, increasing T lowers the required gm (i.e., power) and improves the NF while the Gm does not change. For example, for Q = 1 and T of either 1 or 2 the device gm is 1/(4Rs) or 1/(6Rs), and the NF is $1+\gamma/2$ or $1+\gamma/3$ respectively while the Gm is 1/($\sqrt{2}$Rs). In [15] we choose Q = 1 and T = 2 to lower the power and NF to a sufficiently small value without excessive Gm degradation. Compared to a simple CG, the new topology has 6x lower power consumption and 3x lower noise of the active device at the cost of 30% lower Gm. Notice that even though other authors [23], [40] have showed the same power efficiency (1/(6Rs) for T = 2 with the topology of Fig. 3c, our solution has higher Gm and

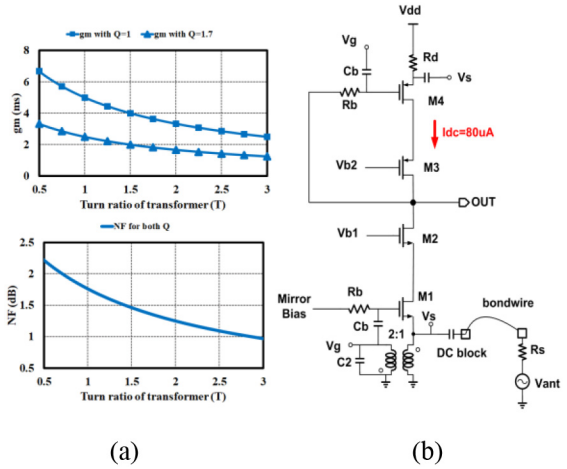

FIGURE 4. (a) Simulated the required device gm and NF versus turn ratio of transformer at matching condition, (b) Schematic of the ULP LNTA in [15].

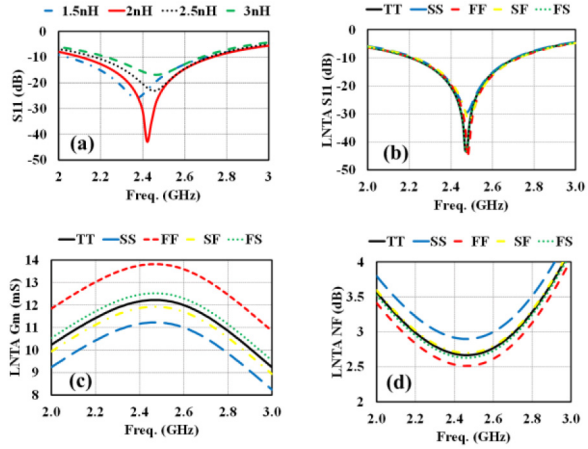

FIGURE 5. (a) Bond-wire effect on S11, LNTA simulation results in all corner process by considering bond-wire of 2nH (b) S11, (c) Gm, (d) NF.

lower NF. The required device gm, NF and Gm for different CG based LNA topologies are listed in Table 1. An additional factor of 2 in power saving is obtained using P-N structures.

The complete LNTA is shown in Fig. 4b. In this design we have re-used the transformer of [23], that has a Q of 9 and 14 at the primary and secondary respectively, with k $\approx$ 0.8. Notice that, for k less than 1, the transformer can be modeled adding a parallel inductance at the secondary and a series inductance at its primary [41]. Moving C_1 from primary to secondary, the series inductance forms an L-match that increases the transformer voltage boosting factor from 2 to 2.5. This reduces the required value of the inductance L_1, making it feasible to implement it with a bond-wire, which saves area. Moreover, the high Q of the bond-wire (around 50), improves NF. The bond-wire inductance varies from 1.5 to 3 nH depending on its length, which affects s_{11}. Nonetheless, when including such a variation, according to simulation the s_{11} is always better than -10 dB from 2.2 to 2.7 GHz, as shown in Fig. 5a. The NF of this LNTA is:

$$F = 1 + \frac{\gamma}{1+T} + \frac{(1+Q^2)R_S}{R_{loss}} + \frac{(1+Q^2)R_S}{R_d} \qquad (1)$$

where γ is the MOS noise factor, T is the transformer turns ratio (equal 2), R_{loss} is the transformer parallel loss resistance at the secondary, and Rd is the biasing resistor. Simulated in different process corners, as a stand-alone block loaded with a linear impedance equal to the up-converted baseband impedance, the LNTA shows good robustness to process variation (see Fig. 5). For a bond wire of 2 nH NF = 2.7 dB, Gm = 12 mS and IIP3 is -8 dBm. This is comparable with the cascoded LNTA used in [42], that shows NF = 3.3dB, Gm = 9mS and IIP3 = -6dBm. Notice that both LNTAs draw only 80 μA. On the other hand, re-simulating the inductive source degeneration complementary p-n LNTA that uses 3 on-chip inductor with a Q = 10 [37] results in a NF = 3.3dB a Gm = 14mS and an IIP3 = $-$ 7.5dBm while drawing 150 μA from 0.8 V supply. We see that the similar performance to the CG LNTA discussed above [15], [42] are achieved but for a larger power consumption and bigger active area. LNTA gain variation over PVT could be reduced by adopting a proper biasing strategy which, however, is not, explored here. It should be pointed out that although no gain programmability was implemented in the LNTA in [15], this can be done by steering the current from the cascode devices or using a reconfigurable topology [43] to balance the NF and linearity for different signal-blocker combinations.

In some architectures, the LNA is removed to lower power consumption and improve linearity. This approach is called mixer-first RX (MFRX) [44]–[48]. The MFRX has good blocker tolerance due to the lack of RF amplification. However, in MFRX the impedance driving the BB transimpedance amplifier (TIA) is reduced, causing a significant increase of its noise. Therefore, higher power is consumed in the TIA for equal RX NF [49]. The MFRX in [44]–[47] has a NF>15 dB burning less than 1 mW. Larger switches are also required in the mixer for impedance matching, leading to higher LO drive power [50]–[51]. On the other hand, scaling up the source impedance, often using an external balun, can improve NF below 10 dB while still consuming sub-mW power [48]. Removing external SAW filters can significantly reduce board complexity and cost. SAW-less RX architectures were already explored in [49] and will not be discussed extensively here. Recently, passive voltage mode boosting using capacitive stacking is emerging as an interesting way to make low NF MFRX with high linearity while consuming sub-mW power [52]–[53]. For instance, [52] shows an outstanding OOB-IIP3 of 25dBm while consuming 600 μW at 1GHz carrier frequency. This is a very promising result, even though the chip does not include neither VCO nor BB stage and it is expected that, when implementing the entire RX chain, to preserve low noise and high linearity, a significant power dissipation will be required in the BB stage. More recently the same idea was reported in [71], which includes the BB stage, and achieves 20$-$24 dBm OOB IIP3 while

burning only 1.7−2.5 mW in the 1.8−2.8 GHz frequency range. Another example of capacitive stacking MFRX is reported in [53]. It shows NF of 5.7dB with OOB-IIP3 of 10 dBm. Here, to reduce chip area and to lower power consumption below 140 μW, a ring oscillator was used instead of an LC VCO. The drawback of this choice is that the NF will be substantially degraded in the presence of blockers due to the higher phase noise of the ring oscillator [53].

B. LO GENERATION

There are two common approaches to generate quadrature LO signals, i.e., by a quadrature oscillator and with a single VCO operating at twice the frequency followed by a frequency divider. Quadrature VCOs running at the carrier frequency have large area since they require at least two inductors in the VCO tank and are potentially subject to injection locking due to crosstalk between VCO and RF circuits. In addition, care must be taken in the way the two tanks are coupled to avoid degrading the Figure of Merit (FOM) of the overall oscillator. As an alternative, to reduce chip area, an IQ splitter can be introduced in the signal path either before [10] or after the LNA [9]. This, however, does not eliminate the risk of VCO pulling and introduces losses that degrade NF (e.g., NF>11 dB for sub-mW RX [9]–[10]). Divider-based solutions solve this problem and require only one smaller inductor since the VCO operates at twice the LO frequency. A comprehensive comparison between different divider topologies targeting low power consumption is given in [37]. The digital frequency divider is a natural choice for the smallest possible area and is often implemented by current mode logic (CML) to obtain high speed. Due to the resistive load and the constant supply current this is not the most power efficient approach. Dynamic dividers are more power efficient as they only draw current during transitions and their power is given by $P_{diss} = C_L V_{dd}^2 f_o$, where V_{dd} is the supply voltage, f_o the carrier frequency and C_L the load capacitance [54]. Lowering the supply and using advanced CMOS technologies is key to reduce power. A frequency divider-by-2 typically converts an input differential clock operating at $2f_{LO}$ to 50% duty-cycle quadrature clocks operating at f_{LO}. Then, 25% duty-cycle non-overlapping quadrature clocks can be generated by ANDing these 50% duty-cycle quadrature clocks with each other, as shown in Fig. 6 (a). Equal rise and fall time in LO are required to make the same driving capability. Equalizing rise and fall time in old CMOS process requires to choose pMOS devices to be typically 3X bigger than nMOS devices. This leads to large input capacitance, for instance, for a minimum gate length of L, Cin = $4W_nL$ for an inverter. However, in advanced CMOS process like 28nm, to have equal driving capability, the pMOS needs to be roughly 20% bigger than the nMOS. This reduces Cin by almost a factor of 2 which lowers power consumption. In Stacked D-flipflop (DFF), shown in Fig. 6(c), the ON/OFF switch resistance at the output is high due to the series combination of inverter stage and LO switch functionality

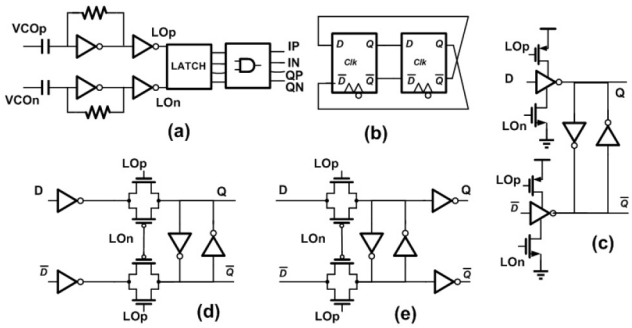

FIGURE 6. (a) 25% LO generation chain, (b) Latch, (c) Stacked DFF [12], [52], (d) Conventional DFF [35], (d) Modified Latch implemented in [15].

between supply rails. Additionally, the total parasitic capacitance at the output is that of 4 inverters, one from the driving stage, two from the cross coupled inverters and one from the next DFF, plus the load capacitance of the ANDing stage. So, it is expected to give the slowest transient response as shown in Fig. 7 (b). In conventional dynamic latch as shown in Fig. 6 (d), the outputs are taken after the cross coupled inverters, the parasitic capacitance at this node is slightly higher than the one in Fig. 6(c), and includes two cross coupled inverters, pass-gate and the inverter of the next stage, plus the load capacitance of the ANDing stage, but the ON/OFF switch is nearly half due to folding the pass-gate. This switch resistance affects the clock sharpness, which defines the phase noise. In the modified latch, shown in Fig. 6 (e), the output is taken after the inverter, which leads to smaller parasitic capacitance. The total parasitic capacitance at this node is due to inverter and pass-gate of the next stage, plus the load capacitance of the ANDing stage. Therefore, an ON/OFF switch resistance similar to that of Fig. 6 (d) is expected but with lower parasitic capacitance, which increase the clock sharpness improving phase noise. To quantify the above observations, 3 different latches (Fig. 6(c–e)) are designed with identical size, i.e., pMOS = 240nm/30nm and nMOS = 200nm/30nm using ULVt devices in 28nm CMOS process. The supply voltage is 0.8V and each latch is loaded with $C_L = 3$ and 5fF. According to the simulation shown in Fig. (7) and reported in Table 2, for the given C_L, the modified latch (Fig. 6(e)) shows 2.5dB and 5.5dB better phase noise at 1MHz offset compared with a conventional latch (Fig. 6(d)) and a stacked one (Fig. 6(c)), respectively. Besides, it also draws 25% lower current from the supply. Notice that, due to the use of very small devices to lower power consumption for all 3 configurations, a small glitch can be observed in Fig. 7 (b) for the modified latch. This, however, does not have an impact on its performance as it will be suppressed by the following ANDing stage that generates the 25% duty-cycle non-overlapping quadrature clocks. The LO generation chain, shown in Fig. 6a, is simulated with a supply voltage of 0.8V to estimate the current consumption of each block for different mixer switch size.

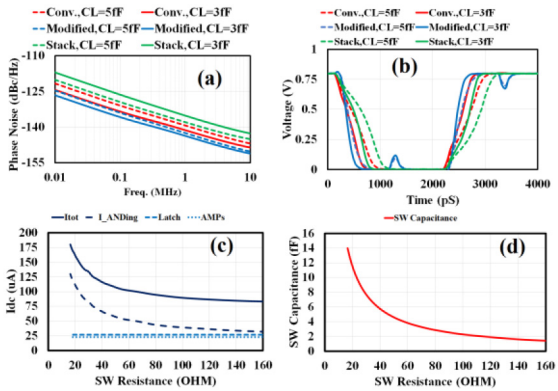

FIGURE 7. Comparison between latches (a) Phase noise, (b) latch output waveform for different C_L , (c) Idc vs SW resistance, (d) SW capacitance vs SW resistance.

TABLE 2. Comparison between three different Latch.

	C_L(fF)	Idc(uA)	PN(dBc/Hz) @1M	Slope (GV/s)
Fig.6(c)	3	57	-138	12.8
Fig.6(c)	5	90	-135.2	8.7
Fig.6(d)	3	60	-141.3	14.55
Fig.6(d)	5	85	-139.4	10.1
Fig.6(e)	3	45	143.7	25.2
Fig.6(e)	5	60	142.5	16.7

As can be seen in Fig. 7 (d), as the SW resistance increases from 16Ω to 160Ω, i.e., the SW size is reduced, the corresponding parasitic capacitance is reduced from 14 fF to below 2fF. This has direct impact on reducing the power consumption of the LO chain. As shown in Fig. 7(c), the current consumption of latch and pre-amplifiers is independent of the SW size and is about 25μA. On the other hand, the ANDing stage, which needs to drive the mixer SW, is the most power-hungry block of the LO chain, especially when the SW becomes bigger. Notice that, if a low supply voltage is not available, charge- reusing can be adopted [13] to lower power by stacking LO buffers.

C. VCO

The VCO is another key building block of RF frontend. There are two conditions that define the minimum power consumption of a VCO. First, to satisfy the Barkhausen oscillation criteria to ensure start-up. Second, to meet the required phase noise. In both cases power is reduced if the tank Q is increased. However, while the power required to sustain oscillation is inversely proportional to the tank inductance (for a given Q), phase-noise constrained power minimization requires a specific inductance value. Moreover, while the phase noise limited power is sensitive to both current and voltage efficiency, the minimum start-up power depends only on current efficiency. In general, in ULP applications phase noise requirements are very relaxed and the limiting factor is oscillation start-up. For example, for BLE, the SNRmin is 12 dB + 3dB implementation margin, i.e., a SNR of 15 dB [44]. For 1 MHz signal BW the reciprocal mixing noise power spectral density (PSD) should be $-15 - 60 = -75$ dBc/Hz. For a 27 dBm interferer at 3 MHz offset [1] the required phase noise is -102 dBc/Hz at 2.5 MHz offset frequency from a 2.4 GHz carrier [1], [44]. For a Q of 10, the theoretical maximum oscillator figure of merit (FOM) is 196.8 dBc/Hz. Assuming an excess noise factor (ENF) of 6 dB, which is reasonable for a class-C VCO [55], the required phase noise is achieved dissipating only 1.2 μW and with an inductance around 100 nH. Practical on-chip inductances are much smaller, which forces to use a larger current to ensure startup yielding a lower phase noise. It follows that the limiting factor is start-up. Therefore, optimum VCO design involves maximizing tank impedance (acting on the tank Q and the inductor value) and current efficiency, while voltage efficiency can be ignored. From the point of view of the VCO topology, the biggest gain comes from complementary p-n topologies that double current efficiency [56] (shown in Fig. 8 (a)). Among different architectures the most promising should be class-C, that has the best current efficiency although with of a relatively low voltage efficiency. The VCO tank should give the highest impedance level at resonance, i.e., the inductance should be increased up to the maximum acceptable value from the area point of view and before the Q starts to decrease. As an example, for a class B n-only topology and assuming $g_m/I_D = 20\ V^{-1}$, the minimum bias current required to sustain oscillation at 4.8GHz for a 5nH inductance with Q of 16 is 85 μA. A $\pi/2$ reduction can be obtained using a class-C oscillator thanks to its higher current efficiency [55]. Using a p-n structure the required current is further reduced by a factor of 2 bringing the minimum bias current down to about 27μA. However, in practice, 2-3 times higher current is needed to ensure robust start-up. Reducing the supply voltage for the same bias current is a possible strategy to ensure start-up while saving power. This also increases the ratio of output swing to supply voltage, i.e., voltage efficiency, which improves phase noise. For instance, a class-D [9] and a Class-C [57] 2.4 GHz VCO consume 152 μW and 114 μW from 0.18V and 0.2V with a phase noise of -106 and -104 dBc/Hz at 1MHz offset, respectively. In both cases, a starter circuit ensures fast start up. On the other hand, a complementary class-C VCO, shown in Fig. 8 (b), has an even better FOM. Operating at 4.8GHz, it dissipates only 137 μW under a 0.55V supply with a phase noise of -107.7 dBc/Hz at 1MHz offset after frequency division by two [38]. Similarly, to the other blocks, current reuse VCOs have been proposed. This was done stacking more devices on both sides of the inductor and flowing a single current through them [48], [58] as presented in Fig. 8(c). This solution doubles current efficiency but halves (at least) voltage efficiency, producing no improvement in the FOM. On

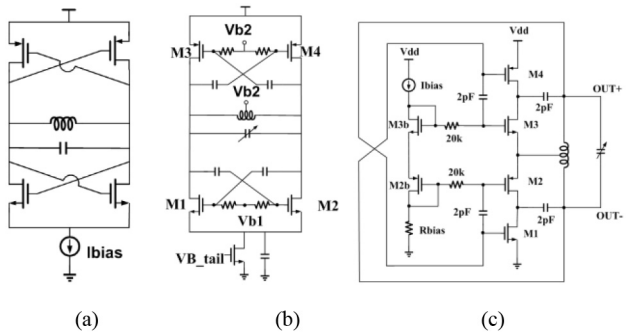

FIGURE 8. (a) Standard pn Class-B VCO, (b) Complementary pn Class-C VCO (c) Current reuse Class-C VCO [42], [58].

the other hand, the minimum power consumption to sustain oscillation for a given thank is reduced. As an example, using a single 0.8V supply for the entire front-end gives 90 μW power consumption with -106 dBc/Hz phase noise at 1 MHz [42], [48], [58] at 2.4 GHz oscillation frequency. To quantify the above observations, several VCO topologies are simulated in 28nm CMOS using RF devices models and the results are given in Table 3. All topologies, operate at 4.8 GHz, from a 0.8 V supply and use a 4.3nH tank inductance with a Q of 18 (taken from the PDK). For robust startup, a bias current at least 2x higher than the minimum value that satisfies the Barkhausen criteria is used. From Table 3, the complementary PN Class-B VCO requires half the bias compared with the class-B N-only VCO with similar phase noise. On the other hand, as expected, the complementary PN Class-C VCO requires a bias current nearly 30% lower than that of a class-B with similar phase noise. Flowing a single dc current through all devices as shown in Fig. 8(c), is another possibility. Notice that in this case, care is required to avoid amplitude unbalance for differential outputs [59].

D. BASEBAND FILTERING

The transimpedance amplifier (TIA) is an essential part of an RX. It acts as a current buffer and simultaneously as mixer load, converting current to voltage and filtering OOB blockers. The TIA should provide a low input impedance from base band frequency to the harmonics of the clock to ensure mixer linearity. Dynamic range requirements in ULP applications are quite relaxed. For instance, a spurious-free dynamic range (SDFR) of 50 dB greatly exceeds the minimum requirements of BLE. For a simple low pass filter with a filter figure of merit (FOM_{FLT}) of 0.05 fJ as in [60], the power-per-pole of a channel-select filter following the TIA will be in the order of 12 μW. Opamp with RC feedback and CG are two widely used structures. In CG, the input devices need a bias current that gives a sufficiently low input impedance. For example, considering g_m/I_d of 20 V^{-1}, 1 mA is required to create around 50 Ω at its input. The large bias current increases the noise of the resistive load (due to voltage head-room limitations) and makes

TABLE 3. Comparison between different VCO operating at 4.8GHz.

	Idc(uA)	PN(dBc/Hz) @1M	FoM
Class-B only N	180	-108	-190
Class-B PN	91	-106.8	-191.8
Class-C PN	70	-105.6	-192
Class-C PN Current Reuse	65	-104	-190.4

CG TIAs not attractive for low power applications. An active gm-boosted CG can have an acceptably low input impedance while consuming only 20 μA [26]. On the other hand, an opamp based design eliminates the IQ crosstalk [61] present with CG TIAs. A simple inverter-based amplifier shows low noise and low power. However, a single stage amplifier has poor linearity due to its low gain, especially at low supply voltage. As an example, a one stage inverter-based amplifier with about 20 dB gain dissipates 50 μW from 0.85 V [48] and 17 μW from 0.55 V [38]. In both cases, an RX IIP3 of -30dBm at low offset frequency is reported, which is limited by the OTA. To improve linearity, a second stage can be added to give higher loop gain at the signal frequency. This comes at the cost of higher power dissipation and the risk of common-mode (CM) instability due to the CM positive feedback created when two simple inverters are cascaded. Another interesting way to improve selectivity is to exploit a transconductor-capacitor analog FIR low-pass filter [62]. 60 dB rejection at >2 channels offset is obtained while consuming only 92 μW from 0.7 V. This filter is intended for a DCR architecture. However, many ULP communication standards use narrow bandwidth. As an example, in Bluetooth 99% of the signal power lays between dc to 430 kHz and transmitted center frequency offset can be as large as 100 kHz in one time slot. Due to this, a significant SNR degradation might be expected due to flicker noise and dc offset when using DCR [63] especially in worst case condition considering the very large variability of the flicker noise observed in deeply scaled technologies.

Given the relaxed image rejection (IRR) generally required (e.g., for BLE only 21 dB [1], [10]), a low-IF architecture with a BB complex filter can overcome these issues. In Low-IF receivers BB complex filters provide simultaneous channel selection and image rejection. Active-RC and gm-C complex filters can be used [64]–[67] as shown in Fig. 9. While active-RC filters are placed directly after the passive mixer, gm-C are normally placed after a TIA.

E. GM-C COMPLEX FILTERS

Complex poles are obtained shifting by $\Delta\omega$ along the imaginary axis the real poles of a low pass filter to create a complex band-pass (BP) transfer function centered around the IF frequency $\Delta\omega$. Starting from a pair of real low-pass filters with bandwidth $\omega_P = g_{mRE}/C$ equal to

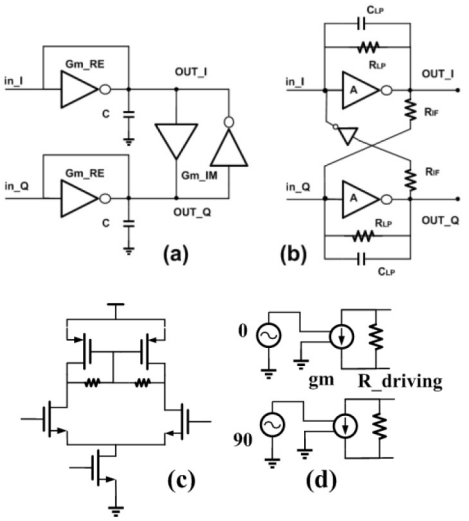

FIGURE 9. Complex filter: (a) gm-c, (b) active RC filter (the -1 amplifier is implemented by swapping the wires in differential implementations), (c) Using 3 cascaded CS amplifier with active load to implement A, (d) Quadrature generation testbench to drive BB stage.

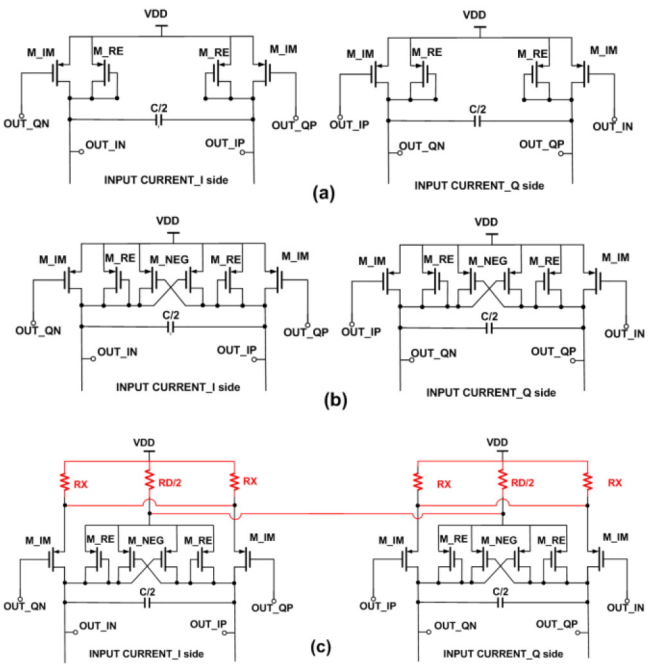

FIGURE 10. Complex pole (a) in [28], (b) in [10], (c) proposed in [15].

half the desired passband and adding two transconductances cross-coupled between the I and Q paths (transistors M_{IM} in Fig. 10(a)) creates a pole at $s_P = -\omega_P + j\Delta\omega$, with $\Delta\omega = g_{mIM}/C$ (Fig. 9(a)). In [28] the current of an LNA/active mixer (Blixer) is re-used in a Gm-C pseudo-differential loads that implements the complex filter. In this way low power consumption is achieved, but the topology includes a CM positive feedback (formed by the cross-coupled Gm-C integrators) with a CM loop gain Q^2, where $Q = g_{mIM}/g_{mRE}\Delta\omega/\omega_P$. If the IF frequency is greater than

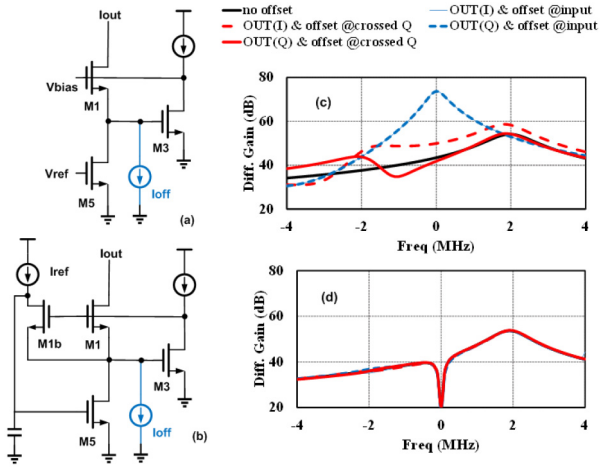

FIGURE 11. (a) Simple current mirror (b) proposed insensitive CG biasing (c) using a simple mirror bias without Rd, Rx and (d) with the proposed topology insensitive to offsets.

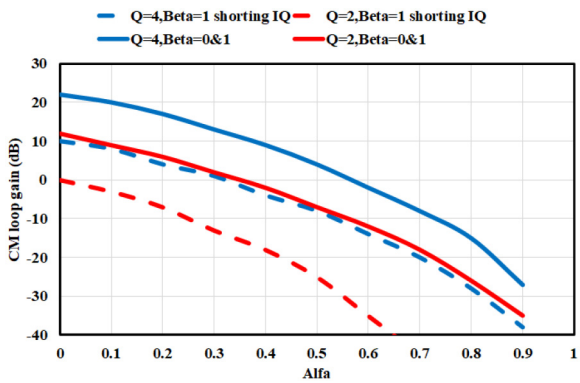

FIGURE 12. DC CM loop gain as a function of α with ($\beta = 1$) and without ($\beta = 0$) degeneration resistors.

half the passband the Q is greater than 1 and CM instability can occur. This problem is addressed in [10] where the complex filter loads a BB CS amplifier located after the TIA whose extra gain lowers noise. Adding cross-coupled transistors (M_{NEG} in Fig. 10(b)) results in a differential-mode negative resistance and a CM positive one that lowers the CM and increases the differential gain. The complex pole s_P is given by (2) and the CM gain is inversely proportional to $\alpha = g_{mNEG}/g_{mRE}$ [60].

$$s_P = \frac{(gm_{RE} - gm_{NEG})}{C} + j\frac{gm_{IM}}{C} \tag{2}$$

The DC CM loop gain versus α for $Q = 2$ and $Q = 4$ is reported in Fig. 12 (continuous lines), showing the α that makes the loop gain smaller than 1. For 1 MHz bandwidth centered at 2 MHz ($Q = 4$) for $\alpha = 0.7$ the CM loop gain is well below 1, ensuring stability. However, increasing α degrades noise, and the circuit is more sensitive to the problem of mismatches and offsets as explained below.

Assuming that, due to mismatch, there is a small offset voltage between the cross coupled transistors of the Q path (M_IM) this changes the bias current of transistors

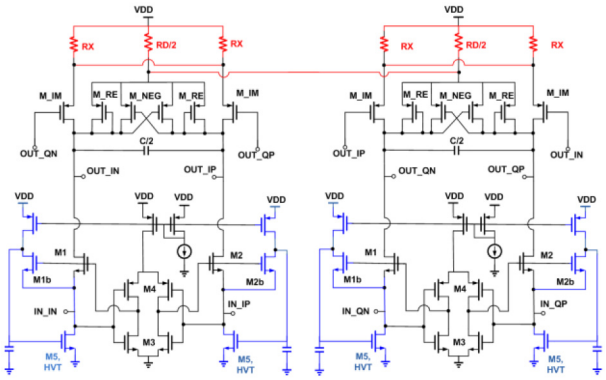

FIGURE 13. Gm boosted CG amplifier with complex load insensitive to offsets [15].

M_IM in the I path. Since the current injected from the input transistors in the complex load is fixed, the diode connected transistor (M_RE) and the negative resistance (M_NEG) experience an opposite variation. As a result, transistors M _IM in the Q path are affected as well. In summary, due to an offset on one side (I or Q), the transfer function becomes *unbalanced* between the two sides. However, for a bias current sufficiently large this effect can be tolerated. In [15] noise is reduced by reducing the current in the complex load. Low input impedance is preserved using a Gm-boosted CG stage. The small bias current, however, exacerbate the problem of the offset at the input and of the mismatch on the load. To cope with this, various techniques are proposed. The Gm-boosted CG BB stage is placed between the passive mixer and the complex Gm-C load, as shown in Fig. 13. The BB input impedance is:

$$Z_{in} = \frac{1}{g_{m1}(1 + ((g_{m3} + g_{m4}).(r_{o3} \| r_{o4}))} \tag{3}$$

with r_o and g_m being the transistors output resistance and transconductance respectively. Low input impedance and low noise are achieved by allocating most of the current in the boosting amplifier (M3−4) as opposed to the CG (M1−2). This, however, causes lower linearity and earlier compression. As in [10], cross-coupled transistors M_{NEG} boost differential and reduce CM load but with much less additional noise thanks to the reduced current. Degenerating the load transistors (as shown in red in Fig. 10(c)) reduces the CM loop gain. Cross-coupled transistors (M_IM) are degenerated with $R_X = \beta/g_{mIM}$ and the rest with $R_D = \beta/(g_{mRE}+g_{mNEG})$. Notice that resistors R_D in the I and Q side are connected to each other, while R_X are not. In this way the CM transconductance of the cross-coupled transistors is lowered but the CM load impedance stays the same. This reduces the CM loop gain, without affecting the differential transfer function. Consequently, a smaller α (lower g_{mNEG}) is required to ensure stability. This is beneficial for noise and reduces the effect of offset within the load. Fig. 12 reports the loop gain as a function of α for Q = 2 and 4 with ($\beta = 1$) and without ($\beta = 0$) degeneration resistors. For $\alpha = 0$ the loop is unstable. Increasing α the loop gain decreases. Inserting degeneration resistors R_X and R_D and shortening the source of M_RE and M_NEG from the I to the Q side (as shown in Fig. 10(c)) decrease the CM loop gain for a given α. In [15] the bias current of the CG and auxiliary amplifiers are 1.6 μA and 14 μA, respectively. The transistors gate length are 3 times the minimum to reduce mismatches since when biased with a such a low current, the standard boosted CG shown in Fig. 11a is very sensitive to mismatches. Any offset voltage at the CG input (due to the passive mixer switched-capacitor effect) is converted to an offset current, resulting in unequal currents in the two complex loads. From simulations 5-mV input offset generates 400 nA offset current at the CG input, which is sufficient to completely upset the transfer function, as shown by the blue curve in Fig. 11(a). To make the bias current equal in both branches even in the presence of an input offset, the negative feedback shown in blue in Fig. 13 (repeated in a simplified form in Fig. 11(b)) is introduced. In the new circuit, the offset current is absorbed by M5 and does not affect the rest of the circuit. In fact, as long as M_{1b} remains in saturation, which is ensured by making M5 a high threshold device, the current through M1 is a scaled copy of I_{ref}. Since this feedback loop high pass filters the signal, an 8 pF capacitor is added at the gate of M5 to make the loop stable and its bandwidth sufficiently small not to affect the useful signal (above 1.5MHz). Robustness against process variations is proved by simulation (shown in Fig. 14). The ratio between differential mode (DM) and CM loop gain is more than 40 dB in all corners.

TABLE 4. Comparison between gm-boosted CG and Active RC for 1st order complex filtering.

	CG-gm boosted	Active RC(1)	Active RC (2)
Idc (μA)	20	20	80
IRN (μV)*	1	2.2	1.2
NF (dB)	6.8	13.6	8.7
IIP3(dBm)^	-34	-31	-15
SFDR (dB)	35.8	33.3	47.3
Gain (dB)	54	55	55
IRR (dB)	15	15	15
FoM (fJ)#	1.98	3.53	0.26

*Integrated input referred noise in 1MHz BW, ^ 2 tones at 5,8 MHz, # Using FoM in [45].

F. ACTIVE-RC COMPLEX FILTERS

Active-RC filters can be used instead of gm-C, as shown in Fig. 9 (b). The integrator is the basic frequency-dependent element in the filter. To convert a 1st order active-RC LPF with cutoff frequency ω_{LP} to a complex 1st order BPF filter centered at ω_{IF}, a complex feedback loop is added as

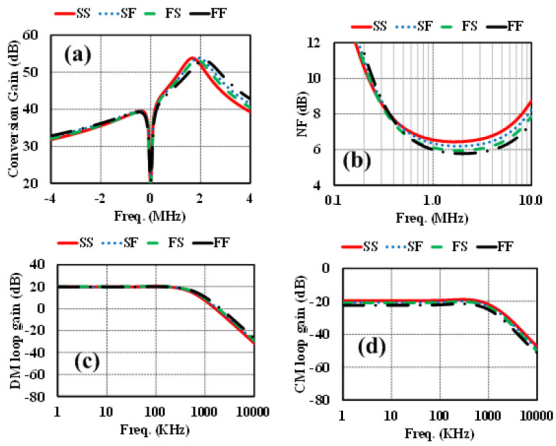

FIGURE 14. Simulation results in all corner process, (a) transfer function, (b) NF, (c) DM, (d) CM.

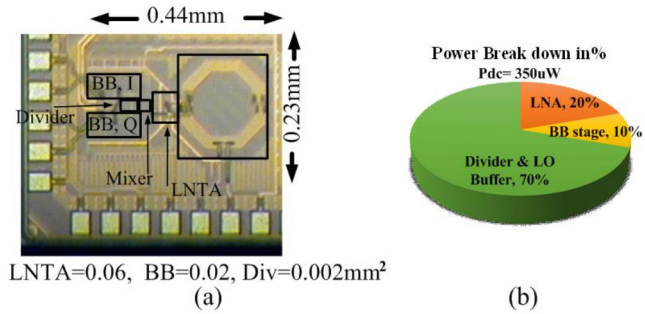

FIGURE 15. (a) Chip micrograph (b) and power dissipation breakdown.

shown conceptually in Fig. 9(b). The corresponding complex pole is $s_P = -\omega_{LP} + j\omega_{IF}$, with $\omega_{IF} = 1/R_{IF}C_{LP}$ and $\omega_{LP} = 1/R_{LP}C_{LP}$. For instance, to select 1 MHz bandwidth centered at 2 MHz, R_{IF} should be equal to 4 R_{LP}. Active-RC filters offer better linearity compared to gm-C at the cost of extra power [64]. Active RC filter requires an OTA with high enough gain-bandwidth to give high linearity since it is the amount of loop gain at the signal frequency that suppress the OTA distortion. Two-stage OTAs are often used instead of single-stage to increase the overall loop gain at the cost of extra power. With a single OTA complex 2nd order filters can be implemented as in [65]. For instance, a 4th order active-RC filter cantered at 1.65 MHz with a bandwidth of 0.9MHz has IB-IIP3 of −9.5dBm (tone at 1.8, 2MHz). Although linearity is good, it dissipates 350 μW from 0.7 V, which is excessive for ULP RX. For the 3rd order active-RC filter of [66], consumption is reduced using a single stage inverter-based amplifier with a negative transconductance at its virtual ground (to counter the low voltage gain). Only two stacked devices are used with a 0.4V supply. The filter has a 1MHz bandwidth cantered at 2MHz over 34 dB image rejection and 1.5dBm OOB-IIP3 (tones at 4 and 6 MHz) burning only 65 μW [66]. However, its 216 μV input noise requires an amplifier in front of it.

Let us compare a gm-boosted CG with an active RC filter implementing a 1-order complex filtering. The testbench is shown in Fig. 9 (d) where the driving impedance is 5kΩ (equal to the down-converted impedance at the mixer output), and the transconductance is 2.5mS (equal to the down converted RF transconductance). Each gm-boosted CG complex filter, shown in Fig. 13, burns 20μA to select 1MHz signal centered at 2MHz. As can be seen in Table 4, the peak gain and image rejection ratio (IRR) is 54dB and 15 dB respectively. The integrated input referred noise within a 1MHz BW is 1μV, however this comes at the cost of lower linearity. IIP3 is −34dBm for two tones placed at 5 and 8MHz (as done in [10]). On the other hand, for the active RC filter, the single stage does not provide enough gain, so a three-stage amplifier is used by cascading 3 CS with an active load as shown in Fig. 9 (c). The feedback and the crossing resistors are chosen to have a similar gain as the gm-boosted CG amplifier. Two cases are considered. First, the same current as the gm-boosted CG (i.e., 20μA) is used where the current distribution between stages is as follows 4, 2, 4μA. Higher noise is expected due to the low current of the first stage but better linearity having a current at the output stage twice that in the load of gm-boosted CG. Second, 4 times more current (i.e., 80μA) is used. In this case −15dBm IIP3 is achieved thanks to the high loop gain at the signal frequency and also the higher current in the output stage. Additionally, the integrated input referred noise decreases to 1.2μV due to the extra current in the input stage. We conclude that for the same power budget, the gm-boosted CG loaded with a complex pole shows better NF than the active RC filter. On the other hand, much better linearity can be obtained by consuming more power in the active RC filter.

V. MEASURED RESULTS OF CASE STUDY [15]

A prototype ULP receiver front-end operating at 2.4 − 2.5 GHz was implemented in a standard 28 nm CMOS technology. The receiver has a low-IF architecture with 2 MHz IF frequency. The CG LNA combines L-match and gate boosting, as in Fig. 4(b). The baseband complex filter is a Gm-boosted CG amplifier with complex load insensitive to offsets (Fig. 13). The chip micrograph is shown in Fig. 15a and has an active area of 0.1 mm^2. The front-end consumes only 350 μW from a 0.9 V, excluding the VCO (Fig. 15(b)). For BLE, owing to the relaxed phase noise requirements, the VCO power can be quite low, e.g., only 65 μW [58]. The RX has 53.3 dB conversion gain at the 2 MHz IF frequency with 15.3 dB image rejection (IR) as shown in Fig. 16(a). Additional IR can be obtained by cascading a second complex filter (with only 40 μW additional power [60]) or adding a passive polyphase filter. In both cases no NF degradation would result because of the significant gain in front. The minimum NF around the IF frequency is 6.2 dB and is 6.5 dB integrating over a 1 MHz band. Fig. 16(d) shows s_{11} in the 2.4 − 2.5 GHz band while Fig. 16(c) shows IIP3/2 versus LO offset when the intermodulation product is at 2MHz. OOB-IIP3 is −8 dBm for two tones at 100 and 198 MHz away from the LO while

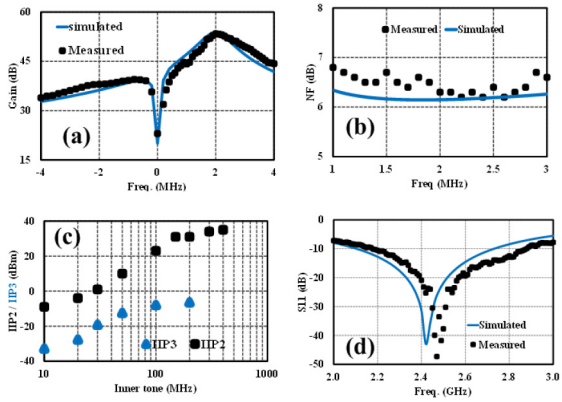

FIGURE 16. Measured results: (a) Conversion gain, (b) NF, (c) IIP3/2, (d) S11.

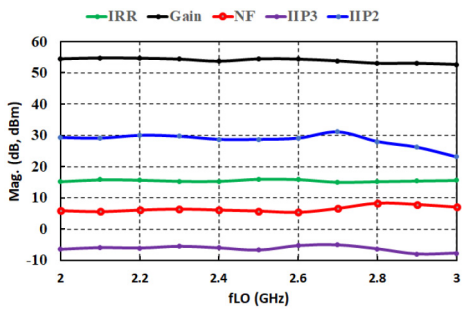

FIGURE 17. RX performance versus LO frequency.

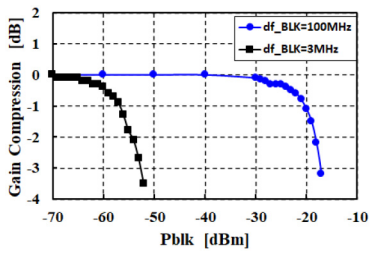

FIGURE 18. Normalized gain compression vs blocker power.

OOB-IIP2 is 30 dBm for two tones 200MHz and 202MHz away from the LO. At lower offset frequencies both IIP3 and IIP2 degrade. At 8 MHz offset from the channel IIP3 is −32 dBm and in-band it is marginally below BLE specs (i.e., −35 dBm for basic sensitivity [1]), limited by the complex filters. This can be improved increasing the current of the CG transistors. Simulations shows that 10 μA additional current in CG results in 10 dB in-band IIP3 improvement with less than 1 dB NF degradation. RX performance versus LO frequency is shown in Fig. 15. The gain and NF are 54 dB (+/−1 dB) and 6 dB (+/−0.6 dB) respectively in the 2−3 GHz interval. With two tone at LO+100MHz and LO+198 MHz and sweeping LO, the OOB-IIP3 is measured to be −7dBm (+/−1 dB) while the OOB-IIP2 is around 29 dBm with two tones at 150 MHz and 152 MHz from LO. Fig. 18 shows the normalized gain compression for in-band and OOB blockers. The 1-dB gain compression for

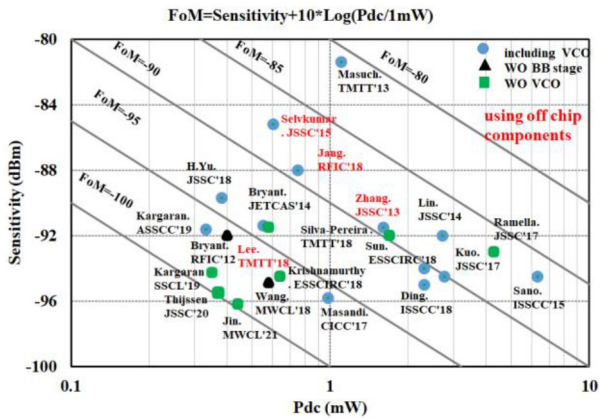

FIGURE 19. Sensitivity versus power consumption.

a blocker at 3 MHz is −56 dBm limited by the complex filter, while for a blocker at 100MHz it is −20 dBm. For BLE the strongest OOB blocker is −30 dBm [1] and our RX withstand this level of blocker power without any gain drop. Finally, RX performance shows good robustness to process variation as shown in Fig. 14. The NF varies less than 1dB across corners. The most sensitive element is the base band complex filter, which needs tuning of both CM and DM loops to achieve the desired band and center frequency. In this simulation, without bias adjustment we see around 300 kHz frequency shift of the peak gain in SS/FF corners. Changing the supply by +/−100mV has a small effect on gain (±1dB), NF(±0.2dB) and IB-IIP3(±2dBm) but power consumption goes from 270μW with 0.8V to 450μW with 1V, since the most power-hungry block is the frequency divider.

VI. STATE-OF-THE-ART SURVEY

An overview of state-of-the-art ULP receiver front-ends is given in Table 5. The RX in [38] consumes the lowest power with moderate NF but has poor in-band linearity, which makes it compliant with ZigBee but not with BLE. [11], [26] have low NF and better IIP3 but power dissipation and area are much higher. Sub-mW RX have a NF at least 5 dB higher [9]–[10] or low in-band IIP3 [15], [48], [68]. DCR solutions with strong BB filtering [9], [37] tend to have very good IIP3 and low power, at the price of increased sensitivity to flicker noise. To compare different solutions two figure-of-merit (FoM) are typically used. The first [69], whose definition is reported in Fig. 19, includes sensitivity and power dissipation. Here sensitivity is obtained integrating the noise across the desired channel (1MHz for all cases to have a fair comparison) and considering SNR = 13 dB [70]. State-of-the-art solutions [15], [37], [67] achieve a FoM of −99, when the power consumption of the VCO is not considered. The best solutions that include the VCO [26], [38] achieve a FoM of −96. The power dissipation of several building blocks in the receiver chain is limited by linearity considerations. To capture this aspect, another FoM is typically used that normalizes the spurious-free dynamic

TABLE 5. Performances summary and comparison with state-of-the-art receivers.

	[15]*	[11]	[10]	[38]	[30]*	[32]	[68]	[9]	[37]*	[48]	[26]
Tech (nm)	28	65	130	22	28	40	28	28	22	65	40
Architecture	Low IF				SIF	PTRX		DCR			
EX Matching	No	Yes	Yes	No	Yes	No	Yes	No	No	No	No
Vdd (V)	0.9	0.3	0.8	0.55	0.8	0.85	0.7 / 0.22	0.18	0.7	0.85	1
Chip Pdc (μW)	350	1600	600	330	640	1550	900	382	370	550	980
Pdc (μW) w/o VCO	350	1000	530	193	640	1050	400	230	370	455	700
NF (dB)	6.5	6.1	15.8	9.4	6.5	6	6	11.3	5.5	9.6	5.2
Gain (dB)	53.3	83	55	32.3	65	86	60	34.5	61	41	47-72
IIP3 IB (dBm)	-32	-20.6	-17	-30	-20	-35^	-43	-12.5	-7.5	-30	-20#
IIP3 OOB (dBm)	-8	-NA	NA	-8	-1	NA	-16	-17^	-7.5	-3	NA
IRR (dB)	15.3	NA	30	27.7	31	No Image	No Image	26.2	NA	NA	NA
Chip Area [mm^2]	0.1	2.5	0.25	0.15	0.25	0.3	0.48	1.65	0.5	0.15	0.7
Area ** [mm^2]	0.1	~1.8	~0.15	~0.1	0.25	~0.12	~0.16	~1	0.5	~0.1	~0.5
FoM 1	-99	-90	-87.5	-96.5	-96.5	-93.4	-95.5	-94	-99.8	-94	-96
FoM 2	43	42	44	42.5	47	34	30.8	52	58	38.6	47

*excluding VCO (VCO power can be as low as 65 μW [58]), ^ LNA IIP3, # Measured IIP3 at low gain, ** excluding other blocks (estimated from the chip photos)

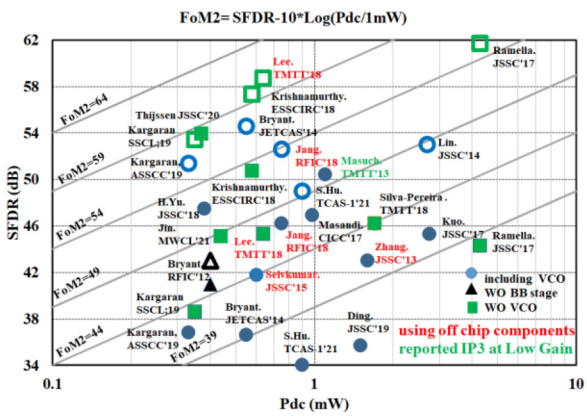

FIGURE 20. SFDR versus power consumption, Solid symbol for close-in offset and empty symbol for far-out offset.

range (SFDR) to power dissipation. The SFDR is defined as 2/3 (IIP3 - NF – 10log10 (BW) + 174). Its definition is reported in Fig. 20 as FoM_2. The available data from the literatures was limited and, in some cases, IIP3 was reported at different offsets or even at a single frequency, this makes it hard to capture the full picture for having a fair comparison! Therefore, to calculate SFDR, we have chosen two points for the IIP3, at the close-in offset frequency (i.e., <10MHz as shown in Fig. 20 by solid symbol) and also far-out offset frequency (i.e., >100MHz, represented by empty symbol in Fig. 20) reported in the literatures to have a qualitative comparison. The highest FoM_2 is 58 dB in [37], which does not include the VCO, and 52 dB in [9], which includes the VCO. Both use a DCR architecture, which benefits from stronger baseband filtering compared to low-IF, thus improving OOB IIP3 while reducing power dissipation in the BB blocks. LNA linearity is also important for OOB IIP3. Both these RX use LNAs with large passives: two 3.6 nH inductors for the inductive-degenerated LNA in [37] and a 1:1 transformer with 5.4 nH inductance in the gate-boosted LNA in [9]. These topologies can give an IIP3 better than −10 dBm with less than 200 μW power dissipation and moderate NF. Even lower power could be achieved adopting current-reuse. Combining current-reuse with transformer-based passive gate or source-boosting, the LNA in [15] and [38] achieve −8 dBm IIP3 while dissipating 72 μW and 25 μW, respectively.

VII. CONCLUSION

IoT and WSN demand ULP wireless receivers. Despite the fact that IoT and WSNs receivers have fairly relaxed noise and linearity requirements, it is still very challenging to design a sub-mW wireless radios since the power consumption does not directly scale down with SFDR. Different RX architectures were examined for BLE with none clearly emerging as the best one. In fact, by choosing one architecture, some challenges can be exchanged with respect to others. DCR can potentially offer better BB filtering leading to the higher SFDR while consuming lower power compared with Low-IF and SIF RX. On the other hand, it is very challenging to deal with the flicker noise and DC offset for the specified 1 MHz channel bandwidth. The main disadvantage of low-IF is the higher power dissipation of the complex baseband band-pass filter with respect to the low-pass filter of the DCR. Several design techniques to lower power dissipation in the key receiver building blocks have been presented and the inherent design trade-offs have been carefully analyzed. Low-power design techniques for complex baseband filters have been thoroughly analyzed. Finally, a 2.4 GHz Low-IF RX front-end suitable for ULP IoT applications was reported as a case study to compare with other state-of-the-art ULP receivers using the two most common FoMs.

REFERENCES

[1] Bluetooth SIG, Inc., Group. (Sep. 2013). *Bluetooth Core Specification V4.0*. [Online]. Available: https://www.bluetooth.org/en-us/specification/adopted-specifications, visited2013-09-15

[2] R. Cavallari, F. Martelli, R. Rosini, C. Buratti, and R. Verdone, "A survey on wireless body area networks: Technologies and design challenges," *IEEE Commun. Surveys Tuts.*, vol. 16, no. 3, pp. 1635–1657, 3rd Quart., 2014.

[3] K. R. Sadagopan, J. Kang, S. Jain, Y. Ramadass, and A. Natarajan, "A 365nW −61.5 dBm sensitivity, 1.875 cm^2 2.4 GHz wake-up receiver with rectifier-antenna co-design for passive gain," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Honolulu, HI, USA, 2017, pp. 180–183.

[4] N. E. Roberts *et al.*, "26.8 A 236nW −56.5dBm-sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2016, pp. 450–451.

[5] P. -H. P. Wang and P. P. Mercier, "A dual-mode Wi-Fi/BLE wake-up receiver," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1288–1298, Apr. 2021.

[6] V. Mangal and P. R. Kinget, "Sub-nW wake-up receivers with gate-biased self-mixers and time-encoded signal processing," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3513–3524, Dec. 2019.

[7] C. Jeon and J. -Y. Sim, "A 2.5-nW radio platform with an internal wake-up receiver for smart contact lens using a single loop antenna," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2668–2679, Sep. 2021, doi: 10.1109/JSSC.2021.3071300.

[8] S. B. Ferreira, F.-W. Kuo, M. Babaie, S. Bampi, and R. B. Staszewski, "System design of a 2.75-mW discrete-time superheterodyne receiver for Bluetooth low energy," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1904–1913, May 2017.

[9] H. Yi, W.-H. Yu, P.-I. Mak, J. Yin, and R. P. Martins, "A 0.18-V 382-μW Bluetooth low-energy receiver front-end with 1.33-nW sleep power for energy-harvesting applications in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1618–1627, Jun. 2018.

[10] A. Selvakumar, M. Zargham, and A. Liscidini, "Sub-mW current re-use receiver front-end for wireless sensor network applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2965–2974, Dec. 2015.

[11] F. Zhang, Y. Miyahara, and B. P. Otis, "Design of a 300-mV 2.4-GHz receiver using transformer-coupled techniques," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

[12] F.-W. Kuo *et al.*, "A Bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.

[13] J. Prummel *et al.*, "A 10 mW Bluetooth low-energy transceiver with on-chip matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.

[14] M. Ding *et al.*, "A 0.8V 0.8mm^2 bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS," in *Proc. ISSCC*, San Francisco, CA, USA, 2018, pp. 446–448.

[15] E. Kargaran, B. Guo, D. Manstretta, and R. Castello, "A sub-1-V, 350- μW, 6.5-dB integrated NF low-IF receiver front-end for IoT in 28-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 2, pp. 29–32, 2019.

[16] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.

[17] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, Feb. 2015.

[18] R. Srinivasan, W.-G. Ho, T. Forbes, and R. Gharpurey, "A 2-stage recursive receiver optimized for low flicker noise corner," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig.*, Tampa, FL, USA, Jun. 2014, pp. 47–50.

[19] M. Ramella, I. Fabiano, D. Manstretta, and R. Castello, "A SAW-less 2.4-GHz receiver front-end with 2.4-mA battery current for SoC coexistence," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2292–2305, Sep. 2017.

[20] M. A. Abdelghany, R. K. Pokharel, H. Kanaya, and K. Yoshida, "Low-voltage low-power combined LNA-single gate mixer for 5GHz wireless systems," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Baltimore, MD, USA, Jun. 2011, pp. 199–202.

[21] T.-P. Wang *et al.*, "A low-power oscillator mixer in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 88–95, Jan. 2006.

[22] L. Zhicheng, P.-I. Mak, and R. P. Martins, "A sub-GHz multi-ISM-band ZigBee receiver using function-reuse and gain-boosted N-path techniques for IoT applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2990–3004, Dec. 2014.

[23] E. Kargaran, D. Manstretta, and R. Castello, "Design and analysis of 2.4 GHz 30μW CMOS LNAs for wearable WSN applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 3, pp. 891–903, Mar. 2018.

[24] T. Taris, J. B. Begueret, and Y. Deval, "A 60μW LNA for 2.4 GHz wireless sensors network applications," in *Proc. IEEE RFIC Symp.*, Baltimore, MD, USA, 2011, pp. 1–4.

[25] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ, USA: Prentice-Hall, 2012.

[26] A. H. M. Shirazi, H. M. Lavasani, M. Sharifzadeh, Y. Rajavi, S. Mirabbasi, and M. Taghivand, "An ultralow-power current-reused direct-conversion Bluetooth-low-energy receiver front-end in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 5, pp. 2697–2711, May 2021.

[27] S. Krishnamurthy, F. Maksimovic, and A. M. Niknejad, "580μW 2.2-2.4GHz receiver with +3.3dBm out-of-band IIP3 for IoT applications," in *Proc. IEEE ESSCIRC*, Dresden, Germany, 2018, pp. 106–109.

[28] Z. Lin, P.-I. Mak, and R. P. Martins, "A 2.4 GHz ZigBee receiver exploiting an RF-to-BB-current-reuse Blixer + hybrid filter topology in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1333–1344, Jun. 2014.

[29] Y.-H. Liu *et al.*, "A 1.9nJ/b 2.4GHz multistandard (Bluetooth low energy/ZigBee/IEEE802.15.6) transceiver for personal/body-area networks," in *ISSCC Dig. Tech Papers*, San Francisco, CA, USA, Feb. 2013, pp. 446–447.

[30] S. Lee, D. Jeong, and B. Kim, "Ultralow-power 2.4-GHz receiver with all passive sliding-IF mixer," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 5, pp. 2356–2362, May 2018.

[31] H.-G. Seok, O.-Y. Jung, A. Dissanayake, and S.-G. Lee. "A 2.4GHz, −102dBm-sensitivity, 25kb/s, 0.466mW interference resistant BFSK multi-channel sliding-IF ULP receiver," in *Proc. IEEE Symp. VLSI Circuits*, Kyoto, Japan, 2017, pp. 319–320.

[32] Y. Liu, V. K. Purushothaman, C. Bachmann, and R. B. Staszewski, "Design and analysis of a DCO-based phase-tracking RF receiver for IoT applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 785–795, Mar. 2019.

[33] Y.-H. Liu, A. Ba, J. H. C. van den Heuvel, K. Philips, G. Dolmans, and H. de Groot, "A 1.2 nJ/bit 2.4 GHz receiver with a sliding-IF phase-to-digital converter for wireless personal/body area networks," *IEEE J. Solid-State Circuits.*, vol. 49, no. 12, pp. 3005–3017, Dec. 2014.

[34] B. Jiang and H. C. Luong, "A 750μW −88dBm-sensitivity CMOS sub-harmonic phase-tracking receiver," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Philadelphia, PA, USA, 2018, pp. 296–299.

[35] B. van Liempd *et al.*, "A 0.9 V 0.4–6 GHz harmonic recombination SDR receiver in 28 nm CMOS with HR3/HR5 and IIP2 calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1815–1826, Aug. 2014.

[36] E. Kargaran, D. Manstretta, and R. Castello, "A sub-1V, 72 μW stacked LNA-VCO for wireless sensor network applications," in *Proc. IEEE Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Prague, Czech Republic, 2018, pp. 185–188.

[37] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "2.4-GHz highly selective IoT receiver front end with power optimized LNTA, frequency divider, and baseband analog FIR filter," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2007–2017, Jul. 2021, doi: 10.1109/JSSC.2020.3031493.

[38] E. Kargaran, C. Bryant, D. Manstretta, J. Strange, and R. Castello, "A sub-0.6V, 330 μW, 0.15mm^2 receiver front-end for bluetooth low energy (BLE) in 22 nm FD-SOI with zero external components," in *Proc. IEEE Asian Solid-State Conf. (ASSCC)*, Macau, Macao, 2019, pp. 169–172.

[39] X. Li, S. Shekar, and D. J. Allstot, "G/sub m/-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-/spl mu/m CMOS" *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2618, Dec. 2005.

[40] E. Kargaran, D. Manstretta, and R. Castello, "A 30μW, 3.3dB NF CMOS LNA for wearable WSN applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Baltimore, MD, USA, 2017, pp. 1–4.

[41] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[42] E. Kargaran, D. Manstretta, and R. Castello, "A sub-1V, 220 μW receiver frontend for wearable wireless sensor network applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Florence, Italy, 2018, pp. 1–5.

[43] M. Tamura *et al.*, "A 0.5-V BLE transceiver with a 1.9-mW RX achieving −96.4-dBm sensitivity and −27-dBm tolerance for intermodulation from interferers at 6- and 12-MHz offsets," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3376–3386, Dec. 2020

[44] J. Masuch and M. Delgado-Restituto, "A 1.1-mW-RX—81.4 -dBm sensitivity CMOS transceiver for Bluetooth low energy," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1660–1673, Apr. 2013.

[45] S. Lee, I. Choi, H. Kim, and B. Kim, "A sub-mW fully integrated wide-band receiver for wireless sensor network," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 5, pp. 319–321, May 2015.

[46] O. Elsayed, M. Abouzied, V. Vaidya, K. Ravichandran, and E. Sánchez-Sinencio, "An ultralow-power RF wireless receiver with RF blocker energy recycling for IoT applications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4927–4942, Nov. 2018.

[47] J. Im, H.-S. Kim, and D. D. Wentzloff, "A 217μW-82dBm IEEE 802.11 Wi-Fi LP-WUR using a 3rd-harmonic passive mixer," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Philadelphia, PA, USA, 2018, pp. 172–175.

[48] C. Bryant and H. Sjöland, "A 0.55 mW SAW-less receiver front-end for Bluetooth low energy applications," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 262–272, Sep. 2014, doi: 10.1109/JETCAS.2014.2337153.

[49] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly integrated and tunable RF front ends for reconfigurable multiband transceivers: A tutorial," *IEEE Trans. Circuit Syst. I, Reg. Papers*, vol. 58, no. 9, pp. 2038–2050, Sep. 2011.

[50] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.

[51] A. Homayoun and B. Razavi, "A low-power CMOS receiver for 5 GHz WLAN," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 630–643, Mar. 2015.

[52] V. K. Purushothaman, E. A. M. Klumperink, B. T. Clavera, and B. Nauta, "A fully passive RF front end with 13-dB gain exploiting implicit capacitive stacking in a bottom-plate N-path filter/mixer," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1139–1150, May 2020.

[53] A. Mohammadpour, D. Manstretta, and R. castello, "a 140μw front-end with 5.7-db nf and +10-dbm OOB-IIP3 using voltage-mode boosting mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 729–732, Jun. 2021, doi: 10.1109/LMWC.2021.3066420.

[54] R. Dutta, E. Klumperink, X. Gao, Z. Ru, R. van der Zee, and B. Nauta, "Flip-flops for accurate multiphase clocking: Transmission gate versus current mode logic," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 7, pp. 422–426, Jul. 2013.

[55] M. Garampazzi *et al.*, "An intuitive analysis of phase noise fundamental limits suitable for benchmarking LC oscillators," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 635–645, Mar. 2014.

[56] M. Garampazzi, P. M. Mendes, N. Codega, D. Manstretta, and R. Castello, "Analysis and design of a 195.6 dBc/Hz peak FoM P-N class-B oscillator with transformer-based tail filtering," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1657–1668, Jul. 2015.

[57] K. Okada, Y. Nomiyama, R. Murakami, and A. Matsuzawa, "A 0.114-mW dual-conduction class-C CMOS VCO with 0.2-V power supply," in *Proc. IEEE Symp. VLSI Circuits*, Kyoto, Japan, 2009, pp. 228–229.

[58] C. Bryant and H. Sjöland, "A 2.45GHz ultra-low power quadrature front-end in 65nm CMOS," in *Proc. IEEE RFIC Symp.*, Montreal, QC, Canada, 2012, pp. 247–250.

[59] T. Siriburanon, W. Deng, K. Okada, and A. Matsuzawa, "A current-reuse class-C LC-VCO with an adaptive bias scheme," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Seattle, WA, USA, 2013, pp. 35–38.

[60] A. Selvakumar and A. Liscidini, "Current-recycling complex filter for Bluetooth-low-energy applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 4, pp. 332–336, Apr. 2015.

[61] A. Mirzaei, H. Darabi, J. C. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and optimization of current-driven passive mixers in narrow-band direct-conversion receivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2678–2688, Oct. 2009.

[62] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "Low-power highly selective channel filtering using a transconductor–capacitor analog FIR," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1785–1795, Jul. 2020.

[63] A. A. Emira and E. Sanchez-Sinencio, "A pseudo differential complex filter for Bluetooth with frequency tuning," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 10, pp. 742–754, Oct. 2003.

[64] A. Balankutty, S.-A. Yu, Y. Feng, and P. R. Kinget, "A 0.6-V zero-IF/low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 538–553, Mar. 2010.

[65] Z. Xie, J. Wu, and C. Chen, "A compact low-power biquad for active-*RC* complex filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 6, pp. 709–713, Jun. 2018.

[66] L. Compassi-Severo and W. Van Noije, "A 0.4-V 10.9-μW/pole third-order complex BPF for low energy RF receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 6, pp. 2017–2026, Jun. 2019

[67] J. Jin, J. Wu, R. Castello, and D. Manstretta, "A 4.8dB NF, 440 μW Bluetooth receiver front-end with a cascode noise canceling LNTA," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 5, pp. 489–492, May 2021, doi: 10.1109/LMWC.2021.3062901.

[68] S. Hu, P. Chen, P. Quinlan, and R. B. Staszewski, "A 0.7-V sub-mW type-II phase-tracking Bluetooth low energy receiver in 28-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 6, pp. 2317–2328, Jun. 2021, doi: 10.1109/TCSI.2021.3070782.

[69] D. D. Wentzloff, *Low Power Radio Survey*. [Online]. Available: https://wics.engin.umich.edu/ultra-low-power-radio-survey/

[70] Y. Zhang, A. Atac, L. Liao, and S. Heinen, "A low-power high-efficiency demodulator in bluetooth low energy receiver," in *Proc. PRIME 8th Conf. Ph.D. Res. Microelectron. Electron.*, Aachen, Germany, 2012, pp. 1–4.

[71] V. K. Purushothaman, E. A. M. Klumperink, R. Plompen, and B. Nauta, "Low-power high-linearity mixer-first receiver using implicit capacitive stacking with 3x voltage gain," *IEEE J. Solid-State Circuits*, early access, Jul. 7, 2021, doi: 10.1109/JSSC.2021.3091942.

[72] H. Zheng and H. C. Luong, "Ultra-low-voltage 20-GHz frequency dividers using transformer feedback in 0.18μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2293–2302, Oct. 2008.

EHSAN KARGARAN was born in Abarkouh, Iran, in 1984. He received the B.S. and M.Sc. degrees in electronic engineering from the Sadjad University of Technology, Mashhad, Iran, in 2007 and 2011, respectively, and the Ph.D. degree from the University of Pavia, Pavia, Italy, in 2017. From 2011 to 2014, he was a Lecturer with the Electronic Engineering Department, Sadjad University of Technology. From 2015 to 2016, he was an Intern with Marvell Semiconductor, Pavia. He was also an RF Intern at MediaTek, U.K., where he was involved in the design of ultra-low power (ULP) RX for BTLE in 2017. He was also a Postdoctoral Fellow of the University of Pavia in 2018. His current research interests include high performance and ULP RF integrated-circuit designs. He was chosen as the Best Student for Research Work by the Dean of the Sadjad University of Technology in 2011. He serves as the Reviewer of many scientific journals, including IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.

DANILO MANSTRETTA (Member, IEEE) received the Laurea (*summa cum laude*) and Ph.D. degrees in electrical engineering and computer science from the University of Pavia in 1998 and 2002, respectively. During his studies, he worked on CMOS RF front-end circuits for direct-conversion wireless applications. From 2001 to 2003, he was with Agere Systems as a member of Technical Staff, working on WLAN transceivers and linear power amplifiers for base stations. From 2003 to 2005, he was with Broadcom Corporation, Irvine, CA, USA, working on RF tuners for TV applications. In 2005, he joined the University of Pavia, where he is currently an Associate Professor. His research interests are in the field of analog, RF, optical and millimeter-wave integrated circuit design. He was a co-recipient of the 2003 *IEEE Journal of Solid-State Circuits* Best Paper Award. He was a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS May 2017 Special Section dedicated to the 2016 RFIC Symposium and a Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES June 2018 Mini Special Issue dedicated to the 2017 RFIC Symposium. He has been a member of the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium since 2006 and the Steering Committee for RFIC since 2017.

RINALDO CASTELLO (Life Fellow, IEEE) received the graduate degree (*summa cum laude*) from the University of Genova in 1977, and the M.S. and the Ph.D. degrees from the University of California at Berkeley, Berkeley, in 1981 and 1984, where he was a Visiting Assistant Professor from 1983 to 1985. In 1987, he joined the University of Pavia, where he is currently a Full Professor. He consulted for ST-Microelectronics, Milan, Italy, up to 2005, in 1998 he started a joint research center between the University of Pavia and ST and was its Scientific Director up to 2005. He promoted the establishing of several design center from multinational IC companies around Pavia, among them Marvell for which he was a consultant from 2005 to 2016. He is currently consulting for Huawei. He was a Technical Chairman of ESSCIRC 1991, a General Chairman of ESSCIRC 2002, an Associate Editor for Europe of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1994 to 1996, and a Guest Editor of its July 1992 special issue. From 2000 to 2007, he has been a Distinguished Lecturer of the IEEE Solid State Circuit Society. He was named one of the outstanding contributors for the first 50 and 60 years of ISSCC and a co-recipient of the Best Paper Award at the 2005 Symposium on VLSI of the Best Invited Paper Award at the 2011 CICC and the Best Evening Panel Award at ISSCC 2012 and 2015. He was one of the two European representatives at the Plenary Distinguished Panel of ISSCC 2013 and the Summer 2014 Issue of the *IEEE Solid State Circuit Magazine* was devoted to him. He has been a member of the TPC of the European Solid-State Circuit Conference (ESSCIRC) from 1987 to 2016 and the International Solid-State Circuit Conference (ISSCC) from 1992 to 2004.