

Low-noise, low drift, high precision linear bipolar (± 10 V) voltage supply/reference for cryogenic front-end apparatus

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(Received 21 December 1998; accepted for publication 27 April 1999)

A very simple linear bipolar (± 10 V) voltage supply/reference (VS/R) featuring very low noise has been implemented. The noise is about $1 \mu\text{Vpp}$ in a 0.1–10 Hz bandwidth, becoming, for the -10 V supply only, $1.3 \mu\text{Vpp}$ at 1.5 A. The VS/R is based on commercial devices and has been designed to face the stringent requirement of very low drift systems. It features very good line regulation, less than 10 mV over 10 V at 1.5 A supply current, and very low drift, between 3 and 8 ppm/ $^{\circ}\text{C}$; it also shows large power supply rejection ratio (PSRR), >120 dB. The VS/R presented includes also safety circuits, to protect itself and the electronic equipment to be supplied in an actual experimental condition. It is protected against inversion of polarity and against under and over voltage at its inputs, and has a foldback current limiting circuit which shuts down the whole system if the current absorption lasts for some time. These protecting circuits acts on both outputs (± 10 V), to maintain always the symmetry. From an analysis made on the data extracted from the measured noise spectra, it was possible to measure the dynamic output impedance, found mainly inductive, with a value of the order of 1 mH. The dc PSRR has been improved by about 20 dB with respect to the performances of the devices used, thanks to a very simple circuit solution. © 1999 American Institute of Physics. [S0034-6748(99)02408-9]

I. INTRODUCTION

The front-end electronics for cryogenic bolometric detectors needs to be very accurate not only for what concerns the noise performances, but also for precision and low drift. The preamplifiers which readout the detector signals are realized using hybrid solutions, where discrete and monolithic devices share a common substrate.¹ Low drift systems are obtained if the direct current (dc) voltages and currents of the working points are very precise and show low noise, especially at low frequencies. These tasks can certainly be obtained, saving space occupation, if the voltage supplies used for the preamplifiers and the subsequent stages can be used at the same time also as very precise reference voltages with low noise and low drift. This way a detector having a large number of channels^{2,3} can be equipped with a few such voltage supplies, located near a suitable number of readout channels.

In this article, a linear voltage supply designed and realized for this purpose is described. In the following sections, the basic diagram of the voltage supply will be introduced. In Sec. III, the part of the circuit devoted to the protection against wrong input connections and under/over voltage will be described. Finally, in Secs. IV and V, the schematic circuit and the current limiting protection circuit and the experimental results will be shown.

II. THE SUPPLY VOLTAGE SYSTEM

The front-end electronics for bolometric detectors has to be very stable against ambient temperature variation. Very often the very front-end preamplifier is realized with an hybrid circuit consisting of discrete and monolithic devices,

which may need an accurate reference current or voltage, common to the whole network, to get an overall stable and precise working point. In these cases, it is a difficult task to realize very precise voltage references, as can be done with a monolithic circuit,⁴ but it is possible to use monolithic commercial band-gap voltage references, or zener based references, which exhibit very low drift. Unfortunately, these circuits show also large noise, and this can be very critical because noise can be added to the circuit, unless it is filtered using very large capacitance values.

For this reason, we decided to design a voltage supply that is able to be at the same time also a very precise and low-noise voltage reference. Since we intend to use it with a detector with a large number of channels, the design was aimed at obtaining a very robust circuit, capable of driving a large current and also equipped with circuits that protect it against undesired situations frequently present in an experimental environment.

In Fig. 1, the schematic diagram of the system is shown. The unregulated dc input voltages, V_{IN1} and V_{IN2} , are checked for their correct connection to the system. After being filtered, a “decision” network assures the rest of the circuit against possible under or over voltage failures. The resulting pair of bipolar sources, V_{PAS+} and V_{PAS-} , are the ones that will be regulated to generate the final ± 10 V linear voltage supply/reference, VS/R. To maintain symmetry under all situations a protecting circuit, which acts on both output voltages at the same time, is also included.

III. INPUT SAFE PROTECTION CIRCUITS

Experience shows that it is not so difficult to confuse the connections of the voltages applied to the circuit, in an ex-

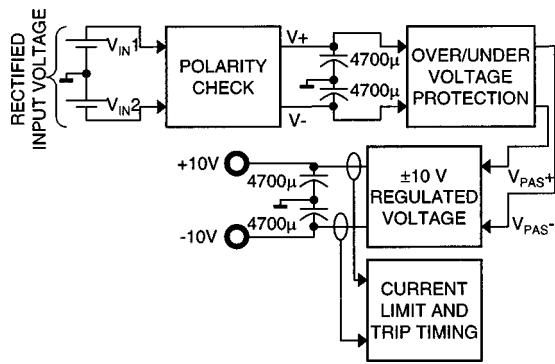


FIG. 1. Schematic diagram of the voltage supply.

perimental condition. A protection against any possible error has been implemented. The supply voltages can be connected to the circuit with either polarity, the circuit itself is able to select the corrected output combination. For any other wrong input combination, nothing is transmitted. The behavior of the network is similar to that of the four diodes bridge rectifier, but with a much smaller voltage drop across it. The implementation has been realized in a simple form, using metal-oxide-semiconductor (MOS) transistors as switches. In Fig. 2, the schematic diagram is shown. The MOS transistors used in this network have been operated as shown in the inset of Fig. 2, connected with the source and the drain interchanged, to avoid the effects of the substrate diode D_i . With this connection when the MOS is reverse biased, D_i is reverse biased too, while when the MOS is forward biased, the low voltage drop between the source (S') and the drain (D') is very small, and D_i has anyway no effect. As a consequence, each MOS behaves as a true switch that autoselects itself in a manner explained below. Consider the input voltages with the polarity A of Fig. 2, with V_{IN1} positive and V_{IN2} negative. The MOS transistors with the label A are in this case all ON. As such, the P-MOS pass transistor Q_{15} (in ON state), sets the output $V+$ positive. The N-MOS Q_{20} forces to be zero the voltage drop between the drain D' and the gate G' of the P-MOS pass transistor Q_{14} , putting it in the OFF condition. The same consideration applies to the N-MOS pass transistor Q_{24} , that copy V_{IN2} to the negative output $V-$, while Q_{23} is put OFF by Q_{22} . If now the input polarity is B, with V_{IN1} negative and V_{IN2} positive, the transistors in the ON state become all those with the label B. Q_{14}

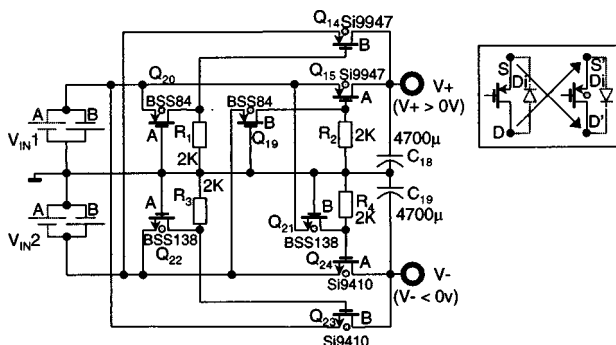


FIG. 2. Decision circuit for the correct polarity connection of the input voltage to the circuit.

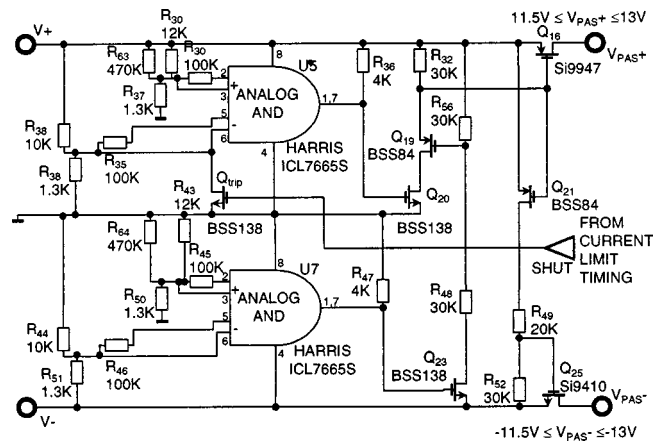


FIG. 3. Under/over voltage protection circuit.

is the P-MOS that put $V+$ positive, while now Q_{15} is set OFF by Q_{19} . The output $V-$ is forced negative by Q_{23} , while Q_{24} is put OFF by Q_{21} .

The pass transistors used have been selected for their low value of the ON resistance, about 25 m Ω . When the load current is ± 1.8 A, the maximum handled by the circuit, the voltage drop across this decision network is only about 0.1 V, to be compared to a value of at least 1 V, which is obtained when using a classical four Schottky diodes bridge.

Another frequent situation happens when the inputs are forced to an over or under voltage condition. This situation occurs especially when the line is filtered with inductances and capacitances. To protect against failures, a pair of window comparators has been used in this design.

Some commercial monolithic "detectors" circuits are able to do this job. We have chosen the ICL7665 (by Harris) that has two inputs, with hysteresis, and two open collector outputs. The inputs, amplified with opposite sign, are both compared with a trip voltage of 1.3 V. To realize the voltage window we need, the circuit of Fig. 3 has been implemented. Two ICL7665 have been employed, U5 and U7, to sense the value of $V+$ and $V-$, respectively. The voltage window and hysteresis have been realized with the resistances connected to pins 2 and 3, and to 5 and 6 of both U5 and U7.

The two open collector outputs of each detector (pins 1 and 7) are connected together. In this way each ICL7665 behaves as an analog AND discriminator: only if the input voltage is within the window, the output will be in its high state. For the present solution, the two window voltages were set to: (11.5 V, 13 V) and (-13 V, -11.5 V), with an hysteresis of about 1 V. This choice is a compromise between a minimal and maximal drop across the output power transistor.

If $V+$ lies in its window, U5 puts in the ON state the N-MOS switch Q_{20} . If $V-$ lies in its window, U7 puts in the ON state the P-MOS switch Q_{19} , using the N-MOS Q_{23} . Switch transistors Q_{19} and Q_{20} are connected in series: only when both are ON the pass MOS transistors Q_{16} and Q_{25} are put in their ON state (note that Q_{25} is driven by the inverter Q_{21}). Therefore, the under/over voltage protection circuit operates in such a way that if and only if both inputs $V+$ and $V-$ are within their own windows, both the outputs V_{PAS+}

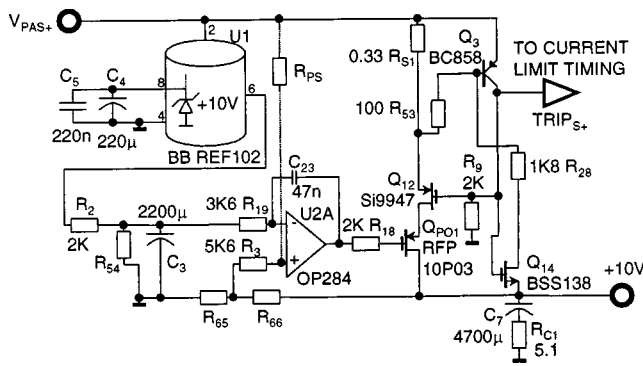


FIG. 4. Schematic diagram of the +10 V voltage supply.

and V_{PAS-} are connected to the rest of the circuit. In Fig. 3, an input called SHUT is also present. It is driven high when an over current absorption lasts for some time (see Sec. IV C). When SHUT is high, the N-MOS Q_{TRIP} puts low the input of the Analog AND U5, simulating an under voltage state, that, in turn, shuts down the voltages V_{PAS+} and V_{PAS-} .

IV. THE BIPOLAR ± 10 V VOLTAGE SUPPLY/ REFERENCE

A. +10 V voltage supply/reference

Generation of currents and voltages for proper system operation with low drift and low noise is a very critical step in a circuit realization that is based on discrete and monolithic devices. Also very critical is to obtain very large power supply rejection ratio (PSRR). In a system with a large number of channels, the voltage supplies must feed circuits distributed over a large area. Consequently, possible crosstalks can be present if the impedance of the connecting cables is not sufficiently low. In this situation, a better solution is to use several voltage supplies, each one dedicated to a few number of channels. Their realization must occupy the smallest volume, as space is always limited. Our choice was therefore to make a voltage supply capable at the same time to be also a voltage reference having low drift and low noise, as required with bolometer applications.

The adopted approach for the circuit design is based on the use of a very precise and stable monolithic voltage reference, filtered to lower the noise, and then buffered to drive a large current. The schematic diagram of the circuit is shown in Fig. 4. The monolithic circuit U1 is the BB REF102, a very precise +10 V voltage reference with a very low drift, <2.5 ppm/ $^{\circ}$ C over -25 to 85 $^{\circ}$ C temperature range. Although it is one of the lowest noise voltage references commercially available, 5 μ Vpp in a 0.1 – 10 Hz bandwidth, our aim was to improve the overall noise performance further. Its output was therefore heavily low pass filtered by means of R_2 and C_3 . To obtain a low dropout, the buffering of the voltage present on C_3 was realized with one of the dual operational amplifier (OpAm) OP284, which has low noise and rail-to-rail input/output capability. The output driver is the power P-MOS Q_{PO1} . The chosen configuration for the OpAm- Q_{PO1} buffer exploits the negative excursion

of the OpAm output, when Q_{PO1} will increase its gate to source voltage to drive large currents.

If needed, the output voltage can be selected to be less than the +10 V nominal value, by proper setting the resistor R_{54} , or larger, by setting R_{65} and R_{66} . The nominal output value of +10 V is obtained when $R_{54}=R_{65}=\text{open}$ and $R_{66}=0$ Ω .

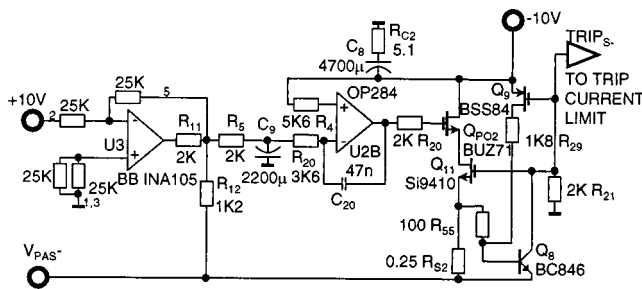
A foldback current limit is included in the VS/R. If the current absorption of the load does not exceed 1.8 A transistor Q_3 is off, since the voltage drop on R_{51} is not enough to forward bias its base-emitter junction, V_{B3} . In this condition, Q_{12} is ON and Q_{14} OFF: the network is in its normal mode of operation. If there is a current overload, Q_3 starts to conduct, limiting the current absorption by putting Q_{12} in its linear mode of operation, and putting Q_{14} in its ON state. The OpAm- Q_{PO1} buffer feedback loop stops to operate and the output of U2A saturates towards the negative voltage supply. A foldback effect is also included, realized by using only resistor R_{28} , in series with the switch Q_{14} , and resistor R_{53} . When there is an overload the current limit circuit lowers the output voltage from its nominal value. The consequent flow of current into R_{28} establishes an increase of the voltage drop on R_{53} . The sum of the voltage drop, V.D., on R_{53} and R_{51} determines V_{BE3} . Since the latter is rather constant, the increase of the V.D. of R_{53} forces the V.D. of R_{51} to become smaller, decreasing the limit current. If, during the overload, current absorption increases, the output voltage lowers, and the foldback limits the current to smaller and smaller values. As an extreme situation, if a short circuit at the output is present the current is limited only to about 80 mA, maintaining low the power dissipation on Q_{12} . The limiting circuit breaks the buffer feedback loop OpAm- Q_{PO1} , and is realized with a loop configuration consisting of only two transistors, Q_3 and Q_{12} , with a good margin of stability. The presence of the switch Q_{14} allows to minimize the latchup to the lower limiting current, otherwise fired by the foldback circuit at the startup, or after there has been, for the first time, an overload.

A further protecting circuit is present. When the overload is established, the $TRIP_{S+}$ node goes high, starting a tripping timer (see Sec. IV C) which shuts down all the system if the overload lasts for more than about 2 s.

Resistors R_{19} and R_3 have the purpose to limit the current into the OpAm inputs when it is forced to saturate towards the negative voltage supply, under current overload conditions. Resistors R_3 , R_{19} , and R_2 are symmetrically connected at the two OpAm inputs to compensate the drift of the OpAm input bias current. This pair of resistors serves also, together with R_{PS} , for the optimization of the dc power supply rejection ratio of the system, as will be explained in Sec. V.

B. -10 V voltage supply/reference

The circuit of the negative, -10 V, voltage supply is very similar to that of the positive voltage supply. In Fig. 5, the schematic diagram is shown. The input to the network is the regulated +10 V. This voltage is amplified by -1 with the instrumentation amplifier U3, a BB INA105. The

FIG. 5. Schematic diagram of the -10 V voltage supply.

INA105 is especially designed to have unity gain with very low drift and offset. Since the U3 output is not able to reach the negative supply, resistors R_{11} and R_{12} have been added to offset the output of U3 to a few volts above the regulated negative voltage supply. The voltage present at the U3 output, -10 V, is again heavily low pass filtered with R_5 and C_9 , to eliminate any residual noise present at the output of the INA105. A structure complementary to the one shown in the previous subsection has then been implemented. The second OpAm of the dual chip OP284, U2B, and the driver N-MOS Q_{PO2} form the buffer stage. The current limiting network is composed of transistors Q_8 , Q_9 , and Q_{11} (Q_8 and Q_9 OFF, Q_{11} ON in normal mode of operation) and resistors R_{S2} , R_{21} , R_{29} , R_{55} , complementary to those employed for the $+10$ V voltage supply. Even in this case when any overload in current absorption occurs, the $TRIP_{S-}$ changes state, starting the timing circuit described in the next subsection.

C. Timing limiting circuit for overload current absorption

A current overload is considered a fault situation accepted only for a transient. As such, if it lasts too long, all supplies are shut down until the normal condition is reached again. This specification has been implemented with the circuit of Fig. 6. The timer U6, a TL7702A, is fired when one or both of the two signals $TRIP_{S+}$ and $TRIP_{S-}$ change state. In particular, since $TRIP_{S-}$ changes from zero to the negative voltage, switches Q_{17} and Q_{22} and resistors R_{33} , R_{39} and R_{40} are introduced to translate it into the right positive logic value. The TL7702A is generally used as a startup circuit: when the input increases above its internal reference voltage, it starts to charge capacitor C_{16} until its voltage drop exceeds the same reference voltage, a condition which fires the output to change state. If the input returns to the lower state

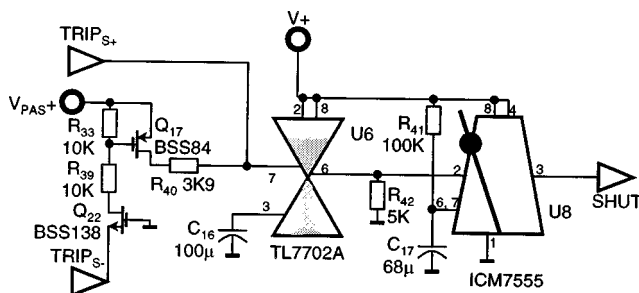
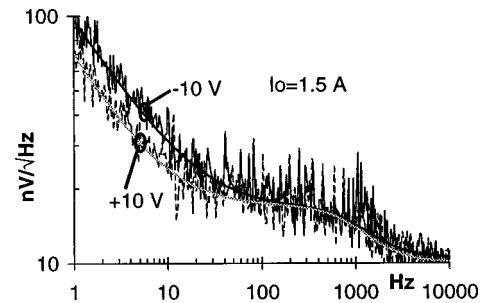


FIG. 6. Schematic diagram of the current overload timing circuit.

FIG. 7. Noise spectra of the two voltages supply, $+10$ and -10 V, at 1.5 A driving current.

within the charging interval, the output does not change state. It is then evident how U6 is used in the present application. A current overload will start U6 to charge C_{16} . If the overload lasts for more than the charging interval, about 2 s, the output of U6 changes to the high state. When this situation happens, the monostable ICM7555 U8, (a CMOS version of the NE555) puts the SHUT node to the high state for about 2 s. The high state of SHUT shuts down both the $+10$ and -10 V regulated voltages, by closing the switch Q_{TRIP} of Fig. 3.

The shut down will persist until the overload condition is present, forcing to a negligible value the power dissipated by the output MOS transistors.

V. EXPERIMENTAL RESULTS

As shown above, the presented ± 10 V VS/R has been designed to fulfill several specifications. Firstly, consider the one concerning the noise performance. Noise has been measured at different levels of load current absorption, for both the $+10$ and -10 V. It was found that noise is quite independent from the current absorption from the load, increasing slightly at the largest currents. At low frequency, the noise spectrum was found to follow a $1/f$ law. For the $+10$ V supply, it resulted to be about 70 nV/ $\sqrt{\text{Hz}}$ at 1 Hz. In the frequency band 0.1 – 10 Hz (usually used as a parameter of comparison in the data sheets), the peak-to-peak noise is less than 1 μVpp , up to 1.5 A load current. The same behavior has been measured also for the -10 V supply, except for the current of 1.5 A, where it increases to about 1.3 μVpp , with the noise at 1 Hz of 95 nV/ $\sqrt{\text{Hz}}$. This behavior can be interpreted by considering the different sources of the parallel noise of the OpAms, U2A and U2B, with their common mode input voltage. The common mode input capability of the OP284 is obtained by using two long tail pairs at the input, one *nnp* and the other *pnnp*. At the positive larger common mode input only the *nnp* pair is operating, while for the negative common mode only the *pnnp* pair is active. The two pairs absorb the same amount of current, when active. For the largest currents the circuit board heats up by about 20 – 30 $^{\circ}\text{C}$ with respect to room temperature, for the presence of the sensing resistances R_{S1} and R_{S2} of Figs. 4 and 5. It seems that the low frequency parallel noise of the *pnnp* pair increases with temperature more than that of the *nnp* pair.

Noise spectra for the worst case of 1.5 A load current are shown in Fig. 7, for both the $+10$ and -10 V supplies. A slightly larger noise at low frequencies for the negative volt-

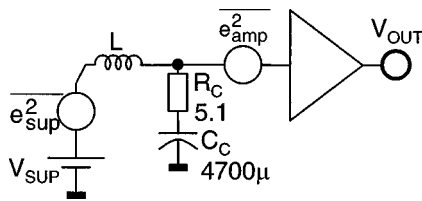


FIG. 8. Circuit model used in the determination of the output impedance of the voltage supply/reference.

age supply can be noted. It must be remarked that the figure of noise measured is very low compared with that of the commercial monolithic voltages reference, about 5 μ Vpp for frequencies in 0.1–10 Hz range.

As can be observed in Fig. 7, the shape of the noise spectrum is not flat at high frequencies, two plateaus being present, one of which for frequencies larger than about 1 kHz. This behavior is attributed to the output impedance of the VS/R. At dc the output impedance is a few m Ω , but at larger frequencies it shows an inductive component. As can be seen in Fig. 4 at the output of the network a capacitance of 4700 μ F, having in series a resistance of 5.1 Ω , is connected. At large frequencies, a partition between the output impedance of the VS/R and this network is present, that reduces the amplitude of the noise. The residual measured noise is that of the reading preamplifier. In Fig. 8 the circuit model for the described behavior is illustrated. The output impedance of the VS/R is represented by the inductance L . The generator e_{amp}^2 represents the series input noise of the amplifier, while the noise of the VS/R is the voltage generator e_{sup}^2 . At the preamplifier input we expect the noise given by the following transfer function ($s = j\omega$):

$$\overline{V_{OUT}^2} = \left| \frac{1 + sR_C C_C}{s^2 C_C L + s C_C R_C + 1} \right|^2 \overline{e_{sup}^2} + \overline{e_{amp}^2} \quad (1)$$

The noise generators were considered to show the following frequency behavior:

$$\overline{e_{sup}^2} = \frac{A_f}{f^\alpha} + \overline{e_{wsup}^2}; \quad \overline{e_{amp}^2} = \frac{A_{fam}}{f^\alpha} + \overline{e_{wsup}^2} \approx \overline{e_{wamp}^2}; \quad (2)$$

$$A_{fam} \ll A_f.$$

The χ^2 method has been used to fit the curves of the measured noise with the model of Eqs. (1) and (2), with free parameters A_f , α , e_{wsup}^2 , e_{wamp}^2 and L . In Fig. 7, the fits for the two noise spectra are superimposed on the curves. The found inductances are 1.9, 1, and 0.8 mH, respectively. A similar result has also been found for the negative voltage supply, with slightly smaller values for the inductance. The results obtained are consistent, once it is considered that the open loop gain of the buffer voltage increases at large currents, due to the transconductance increase of the power output MOS transistor, Q_{P0} , and that the output impedance of the VS/R is inversely proportional to the open loop gain of the OpAmp- Q_{P0} buffer.

The use of a very low drift monolithic reference voltage, along with the strict symmetry adopted in the construction of the buffer voltage, allowed a very low drift system to be obtained, as required by the application. The temperature

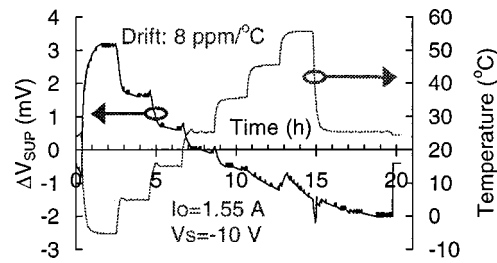


FIG. 9. Thermal drift of the -10 V in -10 $^{\circ}$ C, 50 $^{\circ}$ C.

drift has been measured by putting the VS/R inside a climatic room, a VT7004 by Vötsch, varying the temperature from about -10 to 50 $^{\circ}$ C, a large interval around room temperature, well beyond the required specifications. Figure 9 shows the behavior of the -10 V supply at 1.5 A load current. As can be seen, the drift resulted very low. Maximum deviation in the temperature range was less than 7 mV, corresponding to 8 ppm/ $^{\circ}$ C. A close result was obtained also for the +10 V supply with 1.5 A load current, Fig. 10, which gave about one half of the drift of the -10 V, or 3 mV, corresponding to 3.6 ppm/ $^{\circ}$ C.

A last important requirement is to have a large dc PSRR, of at least 100 dB. From Figs. 4 and 5, it is evident that the dc PSRR of the system is limited to the smaller value between the monolithic voltage reference BB REF102, about \approx 150 dB, the OpAm OP284, \approx 90 dB and the INA105, \approx 110 dB. We succeeded to improve the dc PSRR by at least 20 dB with a very simple circuit solution that will be illustrated with a practical example. Suppose that in the circuit of Fig. 4 an increase of the voltage V_{PAS+} gives origin to a decrease of the output voltage of the positive VS/R with an absolute gain of -86 dB, or -31.6 μ V/V. We can compensate this by simply adding a resistor, R_{PS} , connected between V_{PAS+} and the non inverting input terminal of the OpAm- Q_{P01} buffer. The value of the resistor being such that the inverse of its ratio with the corresponding resistor, 5.6 k Ω , connected to the OpAm input equals 31.6 μ V/V. In the example considered, the value of such a resistor would be 177 M Ω . The increase of the dc PSRR is related to the precision of the added resistor. For a minimum 10% accuracy, we expect about 20 dB of improvement.

This technique was applied to the circuit boards realized. The measurement of the residual dc PSRR after correction has required an accurate procedure, since a sensitivity of the order of less than 1 μ V over 10 V was needed. The output voltage of the VS/R under test was attenuated a factor of 2 and sent to one input of a differential amplifier having a

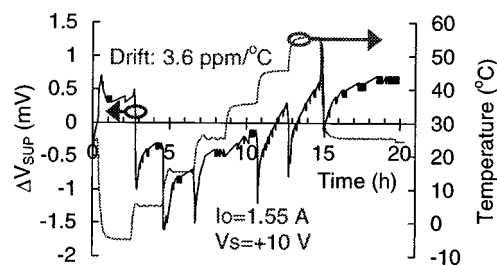


FIG. 10. Thermal drift of the +10 V in -10 $^{\circ}$ C, 50 $^{\circ}$ C.

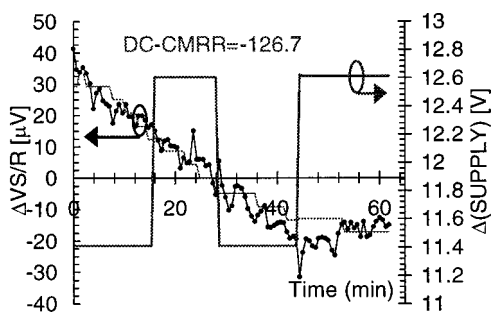


FIG. 11. DC power supply rejection ratio of the VS/R after rejection correction. The square wave is the supply voltage excitation, the curve with the dots is the measured VS/R response, the continuous curve is the simulation of the VS/R response which accounts also of the ambient temperature variation.

voltage gain of 130. At the other input of the amplifier a voltage reference given by a similar VS/R was connected, to null the offset. The dc output of the amplifier was readout with a HP3572 digital multimeter and stored. The changes in the supply voltage of the VS/R under test and the ambient temperature were also acquired, the latter with a platinum Pt100 resistor. Very good accuracy in the measurement were achieved by taking into account the correlation between the ambient temperature and amplifier output voltage: it has to be remarked that $10 \text{ ppm}/^\circ\text{C}$ means $100 \text{ } \mu\text{V}/^\circ\text{C}$ of absolute drift for the VS/R. The obtained result is shown in Fig. 11. The square wave is the supply voltage excitation, the curve

with the dots is the measured voltage response of the VS/R. As can be observed the result is very good, since apparently the VS/R output voltage does not depend on its supply voltage. The continuous curve of Fig. 11 is the fitting of the VS/R. The fitting was calculated with the χ^2 method, assuming a linear dependence of the amplifier output voltage with the measured temperature (changed about half $^\circ\text{C}$ over the measurement time), and assuming also a square response superimposed on the VS/R due to the excitation. The interpolation of Fig. 11 has found a peak-to-peak square wave of $0.54 \text{ } \mu\text{Vpp}$ superimposed on the drift, in response to the 1.2 Vpp input. This corresponds to about 126 dB. The initial dc PSRR for this circuit board was slightly less than 86 dB, and a $100 \text{ M}\Omega$ resistor was used for compensation.

ACKNOWLEDGMENT

The authors thank M. Perego for layout realization and measurements.

- ¹A. Alessandrello, C. Brofferio, C. Bucci, D. V. Camin, O. Cremonesi, A. Giuliani, A. Nucciotti, M. Pavan, G. Pessina, and E. Previtali, *IEEE Trans. Nucl. Sci.* **44**, 416 (1997).
- ²A. Alessandrello, C. Brofferio, C. Bucci, D. V. Camin, O. Cremonesi, E. Fiorini, A. Giuliani, A. Nucciotti, M. Pavan, G. Pessina, S. Pirro, E. Previtali, and L. Zanotti, *Phys. Lett. B* **433**, 156 (1998).
- ³A. Alessandrello, J. W. Beeman, C. Brofferio, C. Bucci, O. Cremonesi, E. Fiorini, A. Giuliani, E. E. Haller, A. Monfardini, A. Nucciotti, M. Pavan, G. Pessina, E. Previtali, and L. Zanotti, *Phys. Rev. Lett.* **82**, 513 (1999).
- ⁴R. J. Widlar, *IEEE J. Solid-State Circuits* **SC-6**, 2 (1971).