CMOS monolithic sensors in a homogeneous 3D process for low energy particle imaging

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***Abstract*— A 3D, through silicon via microelectronic process, capable of face-to-face assembling two 130 nm CMOS tiers in a single bi-layer wafer, has been exploited for the design of monolithic active pixels (MAPS), featuring a deep N-well (DNW) collecting electrode. They are expected to improve on planar CMOS DNW MAPS in terms of charge collection efficiency since most of the PMOS transistors in the front-end electronics, with their N-wells, can be moved to a different layer from that of the DNW sensor. The vertical integration process also requires that one of the two CMOS tiers be thinned down to a mere 6 μm to expose the through silicon vias and contact the sandwiched circuits. In this work, results from device simulations of 3D MAPS will be presented. The aim is to evaluate the potential of such a thin sensitive substrate in the detection of low energy particles (in the tens of keV range), in view of possible applications to biomedical imaging.**

I. Introduction

DEEP N-well CMOS monolithic active pixel sensors (DNW-MAPS) were proposed a few years ago to satisfy the requirements of the experiments at the future high luminosity machines, like the SuperB Factory and the International Linear Collider. They have the potential for incorporating both the low-material budget features of standard 3-transistor MAPS and the pixel-level sparsification capabilities of hybrid detectors [1], [2]. The driving idea in the design of a DNW-MAPS sensor is that of using a relatively large electrode (as compared to conventional MAPS), taking up a substantial fraction of the pixel area, to collect the charge released in the substrate. This notwithstanding, the area of the elementary cell remains almost fully available for the readout electronics, as NMOS devices can be integrated inside the collecting electrode, which is laid out with a deep N-well structure. The large dimensions of the DNW sensor make it possible to include also PMOS devices in the pixel level processing electronics, as long as the region covered by P-type transistors and their N-wells is negligible with respect to the area of the collecting electrode. The full power of complementary MOS technology being available, high gain analog stages, performing continuous time filtering, and low power, high speed digital blocks can be packed inside each elementary cell of the detector, enhancing local intelligence and autonomy with respect to peripheral readout electronics. Recently, vertical integration, or 3D, processes have been taken into consideration for the design of 3D DNW MAPS [3]. Three dimensional circuit manufacturing involves the independent fabrication of two or more planar circuits on different wafers, which are subsequently bonded together after precise alignment and thinning [4]. Vertical integration technologies have already become quite popular among IC designers, as they can alleviate some important performance limitations correlated with CMOS feature size scaling [5]. They are already widely used in the design of high density storage devices and promise to provide a means to overcome the bandwidth bottleneck in modern microprocessors by vertically integrating processor and memory subsystems in a single chip [6], [7].

This paper is devoted to discussing the potential of vertically integrated deep N-well MAPS in the detection of low energy beta particles, of particular interest in autoradiography applications. After a short review of the state of the art in the field of solid state devices for autoradiography, a description of the fabrication technology, of the MAPS device and of the submitted test structures is provided. Results from simulations performed with Monte Carlo and finite element methods are also presented and discussed.

II. Silicon microsensors for β-imaging applications

Film emulsion and phosphor imaging plates are still the most widespread devices for the detection of low energy β particles from weak sources in radioactive labeling applications. Although they may suffer from relatively poor detection efficiency and linearity, films offer yet unmatched granularity (in the order of 1 μm) while covering a dynamic range of a few orders of magnitude [8]. Phosphor imaging plates are more sensitive but feature a worse resolution [9]. Recently, performance limitations in the above mentioned devices have motivated many feasibility studies and developments based on solid state microelectronic technologies. In this field, while spatial resolution and effective area coverage are still constrained by the features of fabrication processes and by the physical mechanisms underlying device operation (e.g. charge diffusion), extremely good results in terms of sensitivity and

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linearity can be achieved, not to mention the built-in advantages of direct digital image acquisition. Following is a list (not meant to be exhaustive) of the different approaches that have been proposed in the past years as far as silicon microtechnologies are concerned.

A. Hybrid pixels

Hybrid pixels take advantage of high resistivity, high quality silicon substrates coupled with low power, VLSI ASIC chips for precise particle tracking in modern high energy physics experiments. Many research teams have been working to adapt hybrid pixel technology to biomedical applications such as X-ray radiography or protein crystallography [10]. Among them, the Medipix collaboration has developed three generations of readout chips for pixel detectors with single photon counting characteristics and large dynamic range [11]. The Medipix2, a 256×256 channel, 55 μm pitch readout chip featuring a 13-bit counter in each channel has been tested in autoradiography applications after bump bonding with a 300 μm thick pixel detector [12]. With a threshold of 6 keV, the system was able to obtain real time images of various sources (^{3}H, ^{14}C, ^{125}I) from autoradiographic microscales. A limited spatial resolution (about 80 μm) and a minimum detectable activity from ^{3}H of 0.32 Bq were achieved. The Medipix1 chip has also been used in autoradiography tests with less interesting results [13].

B. CCDs

The features of charge coupled devices have been exploited in digital autoradiography tests both in a direct irradiation configuration [14] and as part of more complex systems including a gaseous or a solid scintillation detector and an intensifier tube [15]. As far as direct irradiation is concerned, room temperature operation requires using fixed pattern noise correction techniques to compensate for interpixel and interframe variations in dark current. Good linearity performance has been obtained with a matrix of 22.5 μm pitch, 1152×826 pixels operated with a 15 s integration time in tests with ^{14}C and ^{35}S marked samples and standard microscales. CCD beta imaging systems based on scintillators may have some advantages in terms of area coverage, which can be made as large as 20×25 cm^2. Depending on the scintillator detector type, a resolution down to 15 μm can be obtained. Minimum detectable activity is generally significantly higher than in hybrid pixel detectors both in the direct and the indirect methods.

C. DEPFET

The DEPleted Field Effect Transistor, integrating the front-end device of the analog processor directly in each pixel cell, was proven to feature an outstanding noise performance, in the range of a few rms electrons [16], [17]. Its characteristics are exploited in several applications, from X-ray astronomy to particle physics. The properties of the DEPFET as an imaging device for tritium autoradiography applications have been experimentally evaluated by means of a couple of dedicated CMOS ASICs performing parallel readout of a 64×64 matrix of hexagonal pixels [18]. The thin entrance window makes it possible to detect low-energy emitters, like ^{3}H. The detector was found to feature excellent spatial resolution (a few microns for energies ranging from a few keV to a few tens of keV) when suitable offline recostruction algorithms are applied. Energy resolution is sufficient to separate different radiolables in the same specimen, for example ^{3}H and ^{14}C. The relatively high current dissipation of DEPFETs might be an issue when a larger area has to be covered.

D. CMOS MAPS

CMOS monolithic active pixel sensors (MAPS) have been developed and are widely used for imaging applications in the visible range of the electromagnetic spectrum (like digital still photography and high definition television). They take advantage of VLSI technology to integrate both the sensing element and the readout electronics in the same substrate [19]. In the last decade they have been proposed as particle tracking detectors, since they may offer some desirable features, such as high point and momentum resolution, which can be exploited in the next generation of high energy physics experiments [20], [21], [2]. The first tritium autoradiography ever taken with a monolithic sensor [22], [23] was obtained with a CMOS MAPS of the MIMOSA series [24]. The sensor is a high resolution (17 μm pitch), back-illuminated, megapixel imager with 3T analog front-end, capable of detecting β-particles with energies ranging from 4 keV to 30 keV. Sensitivity to such low energies was achieved by thinning the substrate down to the epitaxial layer and reducing the entrance window to about 160 nm. Sequential readout of the entire detector requires a few milliseconds. This, together with the time taken by off-chip data sparsification procedures limits the effective availability of the device to about 25% of the operating time. Subpixel resolution has been obtained with a 512×512 matrix of 25 μm pitch 3T monolithic pixels through off-line, dual-thresholding techniques [25]. In this case, a column-parallel readout with a 12-bit ADC for each four columns has been implemented, resulting in a processing speed not exceeding 100 frames/s.

III. Tezzaron/Globalfoundries vertical integration technology

Among the available three dimensional integration processes and techniques, the one provided by Tezzaron Semiconductor was chosen for the fabrication of the first 3D DNW-MAPS. The devices are being fabricated in the framework of the first 3D multiproject wafer, managed by the 3DIC consortium [26]. Tezzaron 3D technology relies upon the vertical integration of two (or more) 130 nm CMOS wafers produced by Chartered Semiconductor (now part of Globalfoundries), which adopts a via middle strategy for through silicon via (TSV) fabrication (holes for TSVs are dug after device formation and before metal layers and intermetal oxide deposition). A cross-section of the Tezzaron/Globalfoundries process is shown in Fig. 1. Wafers

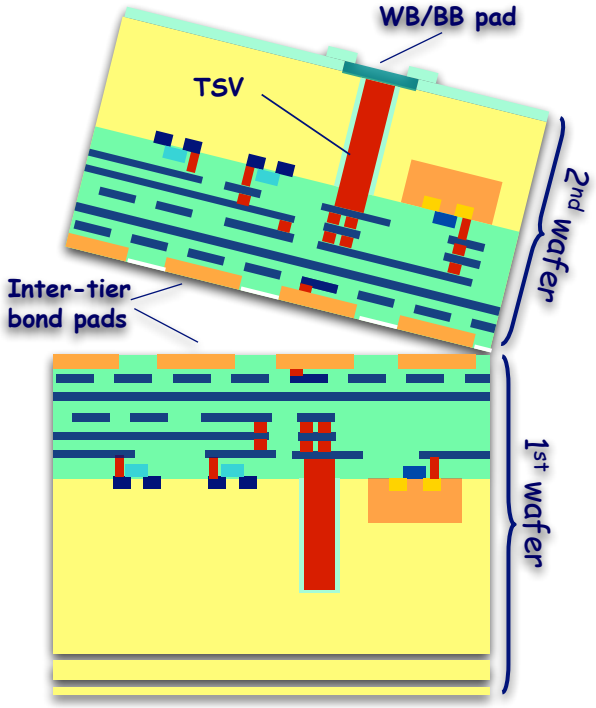

Fig. 1. Cross-sectional view of a double-layer 3D process.

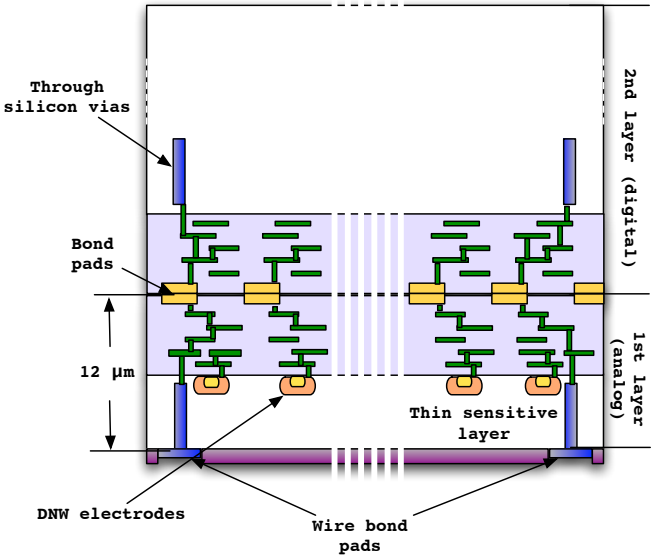

Fig. 2. Cross-sectional view of a 3D DNW MAPS detector with thin sensitive volume.

are face-to-face bonded by means of thermo-compression techniques. Bond pads on each wafer are laid out on the copper top metal layer and provide the electrical contacts between devices integrated in the two layers. The top tier is thinned down to about 12 µm to expose the through silicon vias, therefore making connection to the buried circuits possible. Among the options available in the Chartered technology, the low power (1.5 V supply voltage) transistor option was chosen. The technology also provides 6 metal layers (including two top, thick metals), dual gate option (3.3 V I/O transistors) and N- and P-channel devices with multiple threshold voltages.

IV. 3D DNW MAPS FOR β PARTICLE DETECTION

In a three dimensional DNW MAPS, the analog layer includes the DNW sensor, the charge preamplifier (a shaperless version of the optimum channel for capacitive detectors) and the NMOS differential pair of a threshold discriminator. The PMOS mirrored load of the discriminator, which, for matching purposes, needs to feature quite a large area, is integrated in the digital tier together with all of the logic blocks, to reduce parasitic collection by N-wells and improve the charge collection efficiency of the sensor. The set of logic functions performed by the top tier electronics includes token management for sparsified readout, control of global buses for data output and double hit and time stamp storage. A thorough description of the 3D DNW MAPS structure and of the front-end and readout electronics can be found in a previously published paper [3]. A number of small test structures (including single pixel elements and small matrices) and a large detector, comprised of 240 $\times$ 256, 20 µm pitch DNW MAPS pixels, have been designed for fabrication in a single production batch. For this purpose, the analog and the digital layers of the 3D structures have been laid out side by side in a subreticle replicated 28 times on each of the 25 wafers of the batch (three of them actually being used for the fabrication of planar test structures). By flipping one wafer on top of the other and suitably aligning them, two identical versions for each structure are obtained, one having the collecting electrode (and the analog front-end electronics) on the top wafer, the other on the bottom one. Since one of the two wafers has to be thinned down to about 12 µm (including the substrate and the metal and intermetal dielectric layers) to expose the TSVs and contact the external, backmetal bond pads, in each pair of 3D structures, one will feature a thick substrate under the DNW sensor, the other one will have a 6 µm thick sensitive volume. This latter case is depicted in Fig. 2, showing the technology cross-sectional view for vertically integrated MAPS sensors with thin substrate. The aim of this work is to characterize 3D DNW-MAPS sensors with thin substrate in view of applications where sensitivity to low energy particles, with a penetration depth of a few micron in silicon, is needed. Since MAPS operation is based on the collection of charge diffusing in the substrate, a small thickness (together with back-side illumination) is a mandatory requirement for the sensor to gather enough signal. Also, passive entrance window needs to be minimized in order for the particle not to loose a significant amount of energy in an insensitive device layer [27]. As already mentioned in section II, thinned CMOS MAPS have actually already been proposed for beta autoradiography in tritium radiolabeled biological specimens [22]. It is worth remarking here that the sparsified architecture implemented in the 3D deep N-well MAPS may provide some advantages in

terms of readout bandwidth with respect to standard MAPS devices.

V. Simulation Results

Bi-dimensional device simulations have been performed on the thin 3D DNW MAPS sensor to study its charge collection properties. Fig. 3 shows the section of a DNW MAPS structure simulated with the TCAD tools provided by Synopsys (former ISE-TCAD). In the figure, the charge cloud (about 1000 electrons) released in a very small range (as expected for low energy electrons impinging on silicon) at the bottom of the substrate can be noticed. As shown in Fig. 4, the charge is almost entirely collected by the sensor in about 10 ns. The fast collection time is justified by the very short path electrons have to cover to reach the deep N-well. A very small fraction of the released charge escape collection due to lateral spreading. However, it is worth noticing here that the simulated structure in Fig. 3 does not take into account the parasitic collection action of N-well diffusions used in the sensor layer to integrate PMOS devices. Fig. 5 shows the charge collected by the DNW electrode in DNW MAPS structures like the one in Fig. 3 but with substrate thickness varying from 6 to 10 µm. This simulation was perfomed to take into account possible changes in the technology step related to substrate etching for through silicon via exposure and systematic variation of the substrate thickness in the chip depending on TSV density. At the largest thickness among those considered in Fig. 5, the collected charge is reduced by about 20%. Variation in the amount of collected charge with the substrate thickness is due to charge diffusing in the substrate. As a matter of fact, in the case of a thicker substrate, a larger fraction of the charge manages to avoid being collected by the overlaying pixel due to lateral spreading. Escaping electron may be collected, at least partially, by neighboring pixels.

The above data have been obtained using a 2D TCAD simulation tool. Better founded results are expected with the use of a three-dimensional model, where more details of the device and accurate field modeling can be included. On the other hand, 3D device simulations may require extremely long computational times, depending on the granularity of the mesh. As a fair trade off, some three-dimensional Monte Carlo device simulations have been performed on sensor matrices with 6 µm thick substrate. Fig. 6 shows the charge collected by each cell in a 3×3, 20 µm pitch sensor matrix when a point-like charge amounting to 1000 electrons is released at the center of the detector backside. The figure also shows how the DNW collecting electrode (larger rectangles) and the competitive N-wells for PMOS (smaller rectangles) are arranged in each cell. Charge spreading among the pixels is almost negligible, a major part of the released charge being collected by the central element. Fig. 7 shows the charge collected by three pixels in a 5×5, 20 µm pitch MAPS matrix as a function of the hit

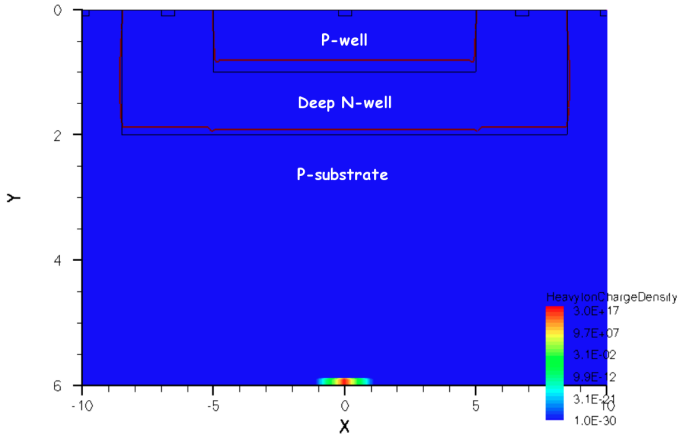

Fig. 3. Cross-section of the simulated thin DNW MAPS structure, emphasizing the internal and external junctions of the deep N-well sensor and the charge cloud released at the bottom of the substrate.

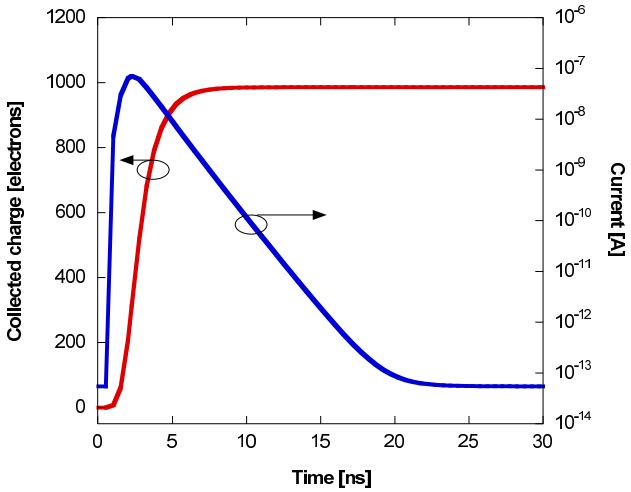

Fig. 4. Charge collected by and current flowing through the junction in the simulated DNW MAPS structure of Fig. 3.

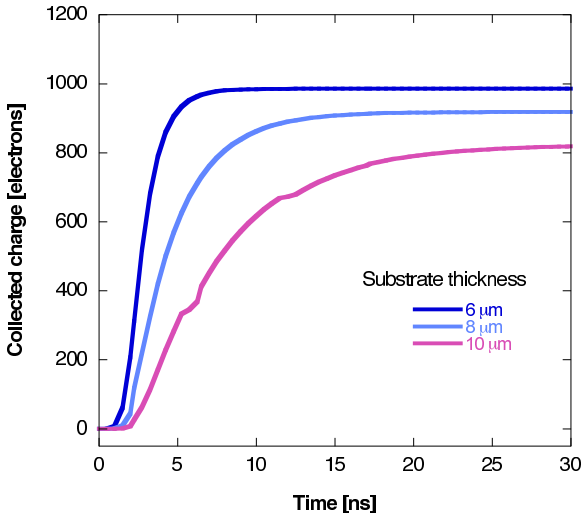

Fig. 5. Charge collected by the DNW electrode in simulated DNW MAPS structures like the one in Fig. 3 but with varying substrate thickness.

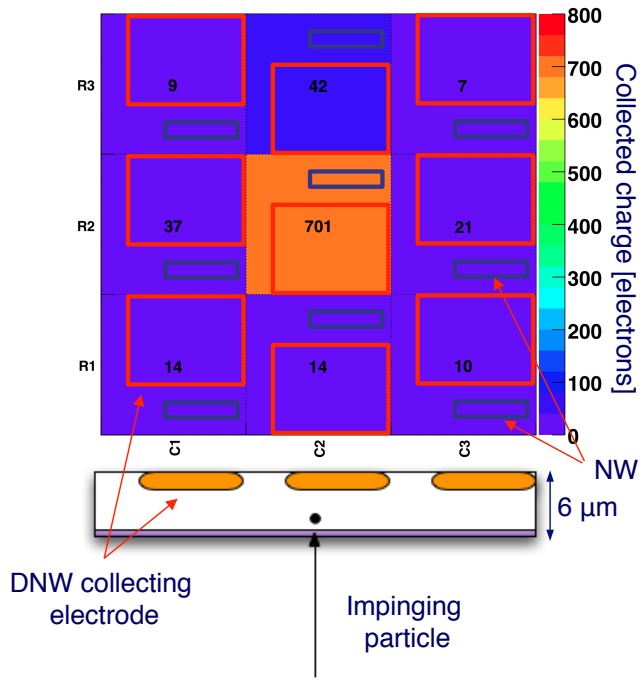

Fig. 6. Charge collected (in electrons) in a 3×3 matrix of 3D deep N-well MAPS with a 6 µm thick substrate resulting from a device Monte Carlo simulation. A point-like charge cloud of 1000 electrons released at the center of the detector backside is assumed. Collected charge for each cell is indicated both through the color scale and the number of collected electrons.

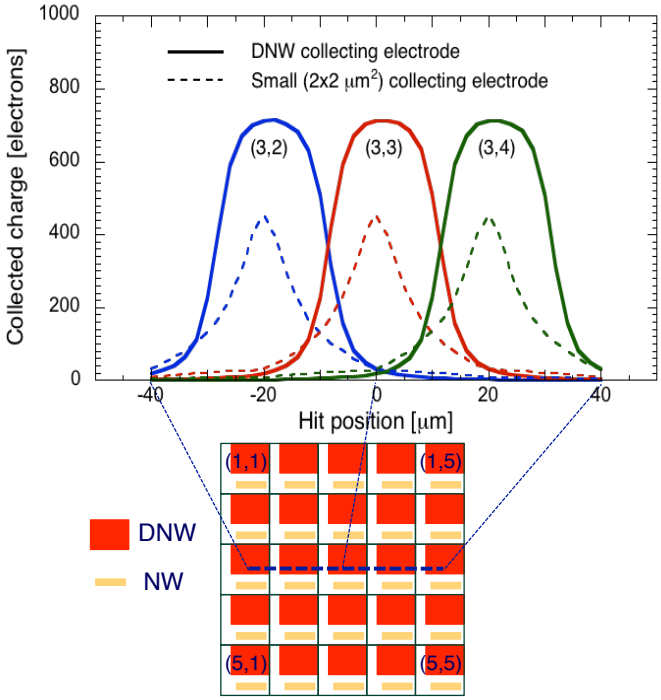

Fig. 7. Charge collected by 3 pixels in a 5×5 matrix (the position is given by means of the (row,column) coordinates), as a function of the hit position on the sensor backside (along the trajectory shown in the figure). Comparison with the expected performance of a monolithic detector with standard, small area sensor, is also provided.

position. Again the charge is released as a point-like clump of 1000 electrons at the backside of the detector. The arrangement of the DNW electrode and of the parasitic N-wells in each cell is described in the picture. As shown in the figure, when the hit is close to the border between two adjacent pixels, the expected signal to noise ratio is about 10, the noise from the analog electronics being of the order of 35 rms electrons. Actually, some room is still left for improving the signal-to-noise ratio through optimization of the geometry and area (and corresponding capacitance) of the collecting electrode. As compared to the results shown in Fig. 4, obtained with two-dimensional finite element simulations, the peak charge in Fig. 7 is about 30% smaller. On the one hand, in Monte Carlo simulations, the effect of N-wells in the sensor tier, stealing charge from the DNW sensor, has been taken into account. On the other hand, the same Monte Carlo simulations may underestimate the real potential of the detector, as they do not take into account any possible effect due to residual, though weak, fields extending into the substrate from the sensor junction, which might be non negligible in the case of very thin substrates. Fig. 7 also provides a comparison with the performance of a monolithic sensor with standard, small area collecting electrode (2×2 µm^2 in area and located in the exact center of the cell). The advantage offered, in terms of collected charge, by the use of a large area diffusion is apparent.

VI. Conclusion

Use of 3D DNW MAPS for low energy particle imaging has been briefly discussed. With respect to previous attempts, the implementation of an in-pixel sparsified architecture may provide some advantages in terms of readout speed and detection/readout duty cycle. Promising results have been obtained from device simulations. Confirmation and support to simulation data need to be found in the next-to-start prototype characterization. Experimental tests are also expected to provide valuable information about the possible need for entrance window optimization and the presence of charge trapping and recombination phenomena at the substrate/oxide interface. Moreover, the design of a different readout architecture, of the counting type, will be considered in a new 3D multi project wafer submission, the present architecture specifically targeting charged particle tracking for vertex reconstruction.

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