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The JEM-EUSO time synchronization system

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Abstract: The JEM-EUSO instrument is a wide-angle refractive telescope in near-ultraviolet wavelength region being proposed for attachment to the Japanese Experiment Module, Kibo, onboard ISS. The instrument consists of high transmittance optical Fresnel lenses with a diameter of 2.5m, a focal surface covered by 4932 MAPMTs of 64 pixels, frontend readout, trigger and system electronics. The tracks generated by the Extensive Air Showers produced by UHE primaries propagating in the atmosphere, are reconstructed on the focal surface by registering in a cyclic memory, every 2.5 microseconds, the data coming from the 315648 pixels and by selectively retrieving only the interesting ones on the occurrence of a second level trigger. The second level trigger has a latency of the order of 10 ms and it is asserted from one or more of the 18 CCB units looking at different zones of the focal surface. In order to guarantee the correct time alignment of the events and to measure the arrival time of the event with a precision of few microseconds a clock distribution and time synchronization system for the focal surface electronics has been developed. We will discuss the status and the technical solutions adopted so far.

Keywords: Extreme High Energy Cosmic ray, electronics for space environment.

1. Introduction

JEM-EUSO (Extreme Universe Space Observatory on Japanese Experiment Module) is a project for a new type of observatory that uses the whole Earth as a detector[1]. The sensor is a super wide-field telescope that detects transient luminous phenomena taking place in the Earth atmosphere caused by particles coming from Space.
The main objective of JEM-EUSO is to investigate the nature and origin of the Extreme Energy Cosmic Rays, EECRs ($E > 5\times10^{19}$ eV), which constitute the most energetic component of the cosmic radiation. [2]
This remote-sensing instrument orbits around the Earth every ~90 minutes on board of the International Space Station at the altitude of 300-400 km. The instrument is planned to be attached to JEM/EF of ISS and will be launched by H2B rocket and conveyed to ISS by HTV (H-II transfer Vehicle).

2. The JEM EUSO apparatus

The instrument consists of high transmittance optical Fresnel lenses with a diameter of 2.5m, a focal surface covered by 4932 MAPMTs of 64 pixels, focal surface electronics and system electronics. A LIDAR and an IR camera assembly will also be provided for atmosphere sounding, which is an important complement for the main data analysis.
The telescope has to be capable to detect fluorescence and Cherenkov photons from the Extensive Air Showers (EAS) and to observe space-time development from 430 km altitude above sea level.
The fluorescence and Cherenkov photons coming from EAS are converted to electric charge by 64 pixel MAPMTs. The signals from the MAPMT are discriminated from electrical noise and digitalized by a front-end ASIC [3]. The ASIC counts the number of photoelectrons produced in a fixed time window for each pixel. The recorded amount of light is nearly proportional to the shower size at the various depths in the atmosphere. By imaging the motion of the streak every few microseconds, it allows to determine the arrival direction of the primary EECR. The integral of light recorded is correlated to the energy of the primary EECR
Since the total number of pixels in the array is very large ($\sim 3\times10^{5}$), a multi-level trigger scheme was developed [4]. This trigger scheme relies on the partitioning of the Focal Surface in subsections, named PDM (Photo Detector Module), which are large enough to contain a substantial part of the imaged track under investigation. The general JEM-EUSO trigger philosophy asks for a System Trigger organized into two main trigger-levels. The two levels of trigger work on the statistical properties of the incoming photon flux in order to detect the physical

events hindered in the background, basing on their position and time correlation. In Figure 1 a scheme of the FS electronics and trigger flow diagram is reported. The First-level trigger is implemented in a dedicated board (PDM board) [5]. Each PDM board is connected to 9 pieces of ECs (36 MAPMTs), handling 2304 channels in total. The output from each 8 PDM board is transmitted to one of 21 Cluster Control Boards (CCB) [6], then CCBs in turn transmit pixel information which passed the fine trigger conditions via Intermediate Data Acquisition Board to the main CPU.

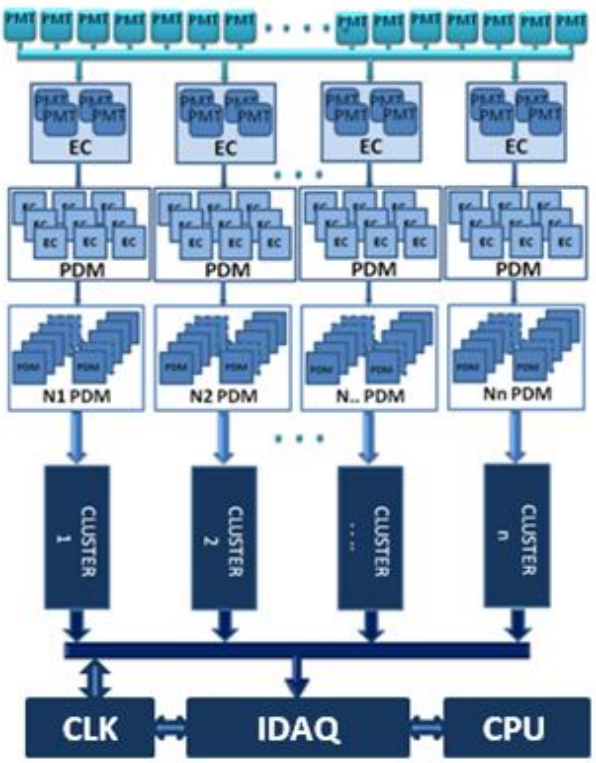

Figure 1. Focal Surface electronics hierarchical scheme

The data acquisition is based on the same hierarchical architecture designed to reduce the amount of data at each level of trigger. All the signals produced by MAPMTs are registered and stored in cyclic buffer waiting for the trigger signal before to be transmitted to the next level for further analysis. The two trigger levels have different latencies in particular the second level trigger has a latency of the order of 10 ms. The data has to be stored for such a long period before to be rejected of acquired. The apparatus is segmented in various zones and in each of these zones different units process independently different sets of data. In order to correctly assign to an event all its own data sets (distributed in space and time) and in order to keep under control the dead time of the apparatus (at level of PDM) is mandatory to perfectly synchronize the whole system and to tag properly the data sets. The role of manage the synchronization of the system is performed by a dedicated board (CLK board) which will be described in the next sections.

3. The clock board

3.1 Requirements

The clock and time synchronization board (CLK board) is mainly devoted to generate and to distribute the system clock and the synchronization signal (GTU clock) to all the devices of the Focal Surface (FS) electronics. However, in order to provide the time synchronization of the events, further and more complex functionality has to be added to the board. The board generates or receives all the signals needed to control the timing of data acquisition. These same signals can be used for measuring the absolute arrival time of the events with a precision of few microseconds if the board is interfaced with the GPS system of the apparatus.
The requirements for CLK board are:

- Generating and distributing system clock (40 MHz) and GTU clock (400 KHz)
- Time synchronization of the event
- Interfacing with the JEM EUSO GPS system
- Interfacing with the Time provided by ISS/JEM (to be used in case of failure of GPS system)
- Receiving the CCB 2nd level trigger signals and registering the trigger pattern
- Live-time and dead-time measurements

A block diagram of the CLK board is shown in Figure 2.

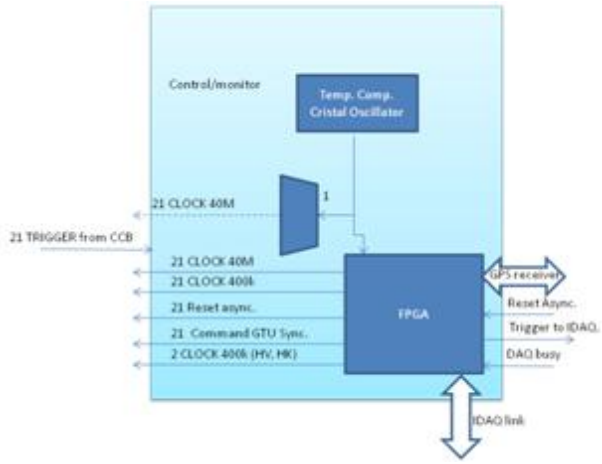

Figure 2. Clock board block diagram.

3.2 Clock signals

The main function of the CLK-board is the generation and distribution of the system clock and the GTU clock to all the devices of the Focal Surface (FS) electronics.
The distribution of these signals through the chain CCB-PDM-FE is considered the baseline design.
According to this scheme the clock signals go through three levels of boards before reaching, for example, the FE-ASIC. The responsibility of the signal integrity, as well as the total power budget, is shared among the three

levels. Prescriptions shall be imposed at each level to keep the total jitter and the total skew inside the requirements.

The master clock is generated by a space qualified crystal oscillator. Frequency stability of +/-0.1 ppm is easily achievable making use of TCXO, Temperature Compensated Crystal Oscillator. Better performance could be guaranteed by using space qualified OCXO, Oven Controlled Crystal Oscillator, with the frequency stability of +/-5 ppb.

An FPGA (Xilinx Virtex4/5 or ACTEL) will be used to fan out the signals. The system clock signals and the GTU clock signals are sent to the CCB boards.

Differential LVDS as output protocol and point to point connections will be used.

The static power dissipation is 10 mW/line for 2.5 V typical driver plus 145 microW/MHz of dynamic power. Cables of equalized length and system blocks like PLL, DLL or clock network of the Virtex family shall be used on the CLK, CCB and PDM boards in order to minimize the total skew of the clocks.

An alternative approach in which the CLK-board generates and distributes only the GTU clock and each CCB and PDM board has an own 40 MHz crystal oscillator will be carefully studied. In this case the synchronization between the two clocks signal will be performed by using double latches technique or PLL system block of the Xilinx Virtex devices.

3.3 Synchronization with GPS system and Time system from ISS/JEM

The measurements of the arrival time of the particles on a scale of few microseconds by our instrument may be possible if each trigger correlated with a detected cosmic particle, acquires a precise time stamp provided by a spatial GPS receiver or, in case of failure of the GPS system, with less precision, by the Time reference provided by the ISS/JEM. The time stamp will be also used to calibrate the internal clocks of the experiment. The slow signal PPS (1 Hz) will be used to open a communication gate to get the UTC time. This time, associated with the internal clock, will provide a stamp of a physical event. In order to associate to each 2nd level trigger the appropriate time stamp, the 2nd level trigger signals coming from the CCB board shall be sent to the CLK-board. On each 2nd level trigger the CLK-board stores in a register the trigger configuration and send a trigger signal to the IDAQ board. The timing of this last operation should be carefully defined in order to take into account the L2 trigger latency. The information on the trigger pattern could be used by the IDAQ board in order to start different data acquisition procedures.

3.4 Event synchronization

Events which trigger simultaneously two CCBs can be correctly reconstructed only if the time information on the development of the event is present in the data structure and it is synchronized with a precision of one GTU.

A possible way to obtain such a time synchronization on all the CCB cards at level of one GTU is to implement GTU counters on the CCB boards and on the CLK board. If a trigger rate of 0.1 Hz is assumed, the CCB and Clock board counters should have ≥ 24 bits to avoid over flow between two consecutive triggers.

In this scheme the 2nd level (L2) trigger lines from all CCB boards are connected to the CLK-board.

After receiving the appropriate command, the CLK board initializes all the GTU counters (Time-sync signal) and starts to count the GTUs.

On the occurrence of each 1st level trigger, the PDM transfers a block of data. The CCB latches the GTU number present in its own GTU counter and associates this information to the data packet. In case of an L2 trigger the content of GTU counter of the CLK board is latched. In such a way the difference in the arrival time of different L2 trigger signals can be measured. Furthermore the CLK board can associate to each L2 trigger a time stamp with UTC time obtained from the GPS receiver. The arrival time of the event will be reconstructed, with the time accuracy of the GTU clock, by adding to the UTC time the appropriate number of GTUs as evaluated from the GTU number relative to the L1 and L2 triggers and from the position of the GTU relative to the L1 trigger in the transferred data from a PDM. In this regard it is worthwhile to note that the PDM data block, in the baseline design, contains a fixed number of consecutive GTUs acquired half before and half after the GTU relative to the trigger. However, in case of slow events, it could be useful to transfer data relative to non consecutive GTUs, for example a data every 10, 100 GTUs. To address this situation and to improve the flexibility of the system, additional information on the number of GTU transferred, on the position inside the transferred block of the GTU relative to the L1 trigger and on the sampling rate will be added to the header of the data block.

A *Time-sync* signal, synchronous with the GTU clock, will be distributed to each CCB to initialize all the GTU counters and restart the acquisition after the data transfer from CCB to IDAQ –CPU.

3.5 Live/dead time counters

The main CPU measures the time length of the run with a precision of the order of 1 ms.

To measure a flux is necessary to know the live-time T_{live} of the apparatus during all the period of data taking. If we measure, for each event, the time between event and event t_{ev} and the time needed to acquire the data relative to the event (dead-time) t_m then the total live time of a run can be evaluated by:

$$T_{life}^{(1)} = T_{CPU} - \sum_{i=1}^{N} t_m^{(i)}$$

Where N is the total number of events or by

$$T_{life}^{(2)} = \sum_{i=1}^{N} t_{ev}^{(i)}$$

The possibility of measuring two different ways T_{live} on the entire run allows controlling and possibly correcting off-line, any drift in the clock of the board. The verification can be done by checking that:

$$T_{CPU} = \sum_{i=1}^{N} (t_{ev}^{(i)} + t_m^{(i)})$$

The dead time of an event and the time between two events can be easily measured with a couple of counters implemented on the clock board. The start-stop logic is driven by the trigger signal sent to the IDAQ board and by the busy signal received in response to this signal from the CPU

A 18 bit counter clocked by a 100 KHz signal guarantees an error on the single measure of dead time $\Delta t_m = 10^{-5}$ s with overflow reached after 2.62 s (typical dead times of the order of tens of milliseconds).

The time between two events can be measured by a 18 bits counter clocked at lower frequency (400 kHz clock divided by a factor 128 (3.125 KHz) . The error on the single measurement of live time is in this case: $\Delta t_{ev} = 3.2\ 10^{-4}$ s with overflow reached after 83.9 s (expected trigger rate 0.1 Hz).

The approach just described is valid in cases where the whole apparatus is stopped at the arrival of each trigger. If it is decided to acquire only the CCB that has triggered leaving the rest of the apparatus in operation, the live time and the dead time should be measured separately for each CCB.

4. Prototype board and test

The CLK board laboratory prototype, currently tested at INFN Section of Naples, is implemented in a Virtex-5 FPGA (XC5VLX50T, package FFG1136) hosted on a Virtex®-5 LXT ML505 development board. The device is not space qualified so this prototype board is used mainly to develop and test interfaces to other devices.

In order to measure the jitter and the skew of clock and GTU signals along the chain of three board (CLK board, CCB board and PDM board), the setup shown in Figure 3 has been used. The CCB board has been simulated by using a Virtex-4 FPGA (XC4VFX20, package FF672) mounted on a Virtex®-4 ML405 development board. The PDM board has been simulated by using a M1A3P1000L-FGG484 ACTEL FPGA mounted on an ACTEL M1A3PL development board. Obviously this configuration allow us to test only the solution in which all the clock signals are transmitted and received on the I/O pins of the FPGA without use of any LVDS buffer. More realistic test will be performed when the maximum length of cables will be better known.

The interface with the GPS system is simulated by using a Vincotech A1080-A SiRFStar III-based GPS receiver.

The device supports a subset of the NMEA-0183 standard for interfacing marine electronic devices as defined by the National Marine Electronics Association (NMEA).

A bi-directional serial interface with Vincotech's GPS module has been implemented by use of the full duplex UART (Universal Asynchronous Receiver Transmitter) interface of the GPS processor.

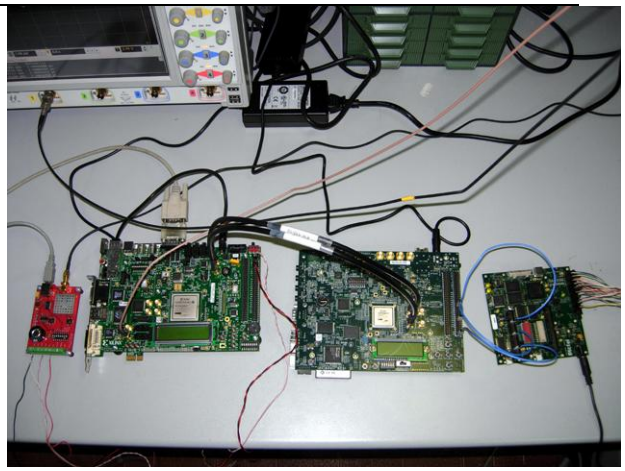

Figura 3. The setup used to test the CLK board.

This interface allows to acquire the output of the GPS modules (NMEA sentences, etc.) roughly 300 ms after the PPS pulse and store in a memory the relevant information (UTC time, longitude, latitude, number of satellites, etc), on the other side the UART interface is used to send commands to Vincotech's GPS modules.

The communication link between CLK board and IDAQ board is based on a serial protocol developed according the Spacewire standard but tailored for the specific characteristics and constraints of the PAMELA mission.

5. Conclusions

The time synchronization system for the JEM-EUSO project has been discussed in this paper. The system distributes the clock signals to the FS electronics and manages all the signal needed to take correctly aligned in time the data packets produced in different parts of the apparatus at different time. The system, for each event, provides the measurement of the arrival time with a precision of few microseconds, the measurement of the time elapsed since the previous event (live time) as well as the time needed to acquire the previous event (dead time). The CLK board described in this paper is now under development, and it will be further tested in laboratory in this year.

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