Characterization of a front-end electronics for the monitoring and control of hadrontherapy beams

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Abstract

An integrated 64-channel device for the read-out of parallel plate pixel and strip ionization detectors has been developed by the INFN and University of Torino. The detectors will be used for the monitoring and control of hadrontherapy beams. The ASIC has been designed in CMOS 0.8 μm technology and it is based on a current-to-frequency converter followed by a synchronous counter. In this paper, we present a detailed characterization of the device done with 113 chips.
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1. Introduction

The main goal of the radiotherapy is the local control of the tumor and of the surrounding diffusion path. In order to reach this goal, one must deliver to the tumor a sufficiently high dose to destroy it, while sparing the surrounding healthy tissues so that they do not undergo serious or even irreversible damage or complications. Taking advantage of the Bragg peak, hadron therapy maximizes the dose delivered to the tumor sparing the surrounding healthy tissue. The result is an increase of complication-free tumor cure in comparison to conventional radiotherapy [1,2].

At the moment, approximately 45,000 patients worldwide have been treated with proton or ion beam therapy and there are excellent follow-up results for selected treatment sites. The number of patients treated each year with proton and carbon ion beams continues to increase and the opening of new dedicated facilities, several of which are hospital based, may increase dramatically [3].

In the near future, Centro Nazionale di Adroterapia Oncologica (CNAO) will be the first hospital-based hadrontherapy facility in Italy. Nowadays, CNAO is in the building phase in Pavia. The main part of the center consists of a synchrotron accelerator. The beam extracted from the accelerator has a narrow energy spectrum and narrow spatial profile. These characteristics have to be adapted to the tumor volume to deliver the prescribed dose to the appropriate site. The design of CNAO is oriented toward the active spread-out system due to its performance in shaping the dose to the treated volume and reducing the beam impurities caused by nuclear fragmentation. To cover the target volume, the pencil beam is steered by means of two scanning magnets and modulated in energy in order to penetrate different depths.

Fondazione CNAO, in cooperation with the INFN and University of Torino are developing the beam monitor

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system. The detectors are based on the architecture of a parallel-plate ionization chamber with one of the electrodes subdivided in strips or pixels [4,5]. The *strip detectors* are composed by two anode layers oriented in two orthogonal directions, where each anode is segmented into 128 strips over a $(21 \times 21)\,cm^2$ surface. The *pixel detectors* consist of 1024 pixels covering the same area [6]. Such a number of channels on a relatively small area make preferable a solution with a dedicated front-end electronics read-out.

For this reason, an Application Specific Integrated Circuit (ASIC) has been developed from INFN and University of Torino. The ASIC, named Tera06, has been designed in CMOS $0.8\,\mu m$ technology and has been developed to independently read out the current from up to 64 pixels or strips and convert it to frequency. The design and the characterization of the first few prototypes are described in [7,8].

In this paper, we present the results of the tests performed to characterize the performance of the circuit studied on 113 ASICs, which will equip the whole parallel plate pixel and strip ionization detectors that will be used at CNAO to perform measurement of position and intensity of the therapeutic beams.

2. Brief description of the integrated circuit

The INFN and University of Torino developed in the last years a family of multipurpose chips to read out in parallel the current from up to 64 channels and measure the corresponding charge by converting it into counts. The conversion is based on the recycling integrator principle. The ASIC implementation and the circuitry overall architecture have been studied and documented in several papers [7,8]. The subject of this paper is a 64-channel ASIC designed in CMOS $0.8\,\mu m$ technology encapsulated in a PGA 144 package.

To have a large dynamic range, the ASIC architecture is based on a current-to-frequency converter, followed by a digital counter. Using this architecture, the charge can be measured by counting the number of pulses coming out from the converter in a given time.

Fig. 1 shows the current-to-frequency converter, which has been implemented with the charge balancing integration technique [9]. The input current is integrated over a capacitor (C_{int}) of 600 fF via an operational transconductance amplifier (OTA). The integration output (V_A) is a voltage ramp that is compared with a threshold voltage (V_{th}) by a synchronous comparator. When $V_A > V_{th}$, a fixed amount of charge (that is called charge quantum, Q_c) is subtracted from the capacitor C_{int}. This results in sharp decrease of the voltage across C_{int}, which is proportional to the charge injected by the subtraction circuit. After this charge subtraction, the output of the OTA (V_A) ramps up again, and the process is repeated. For each charge subtraction a pulse is also sent to the digital counter.

Therefore, the frequency of the pulse is proportional to the input current, according to the following relation:
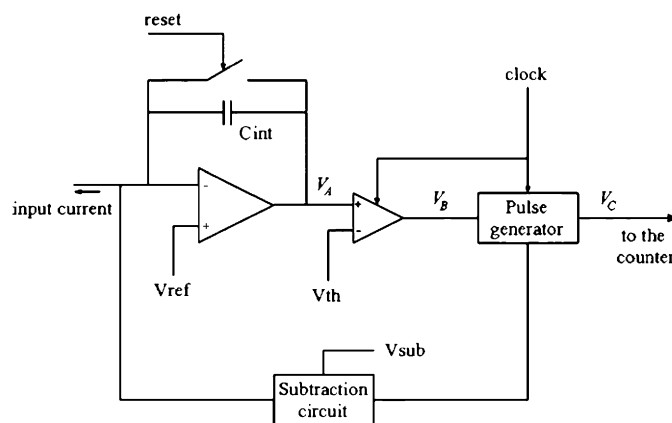

Fig. 1. Current-to-frequency converter scheme [8].

$f = I_{in}/Q_c$ (where I_{in} is the input current and Q_c is the charge quantum).

Therefore, the number of pulses generated in the measurement time multiplied by the charge quantum gives the total charge read-out from the input.

The charge quantum is obtained by sending a voltage pulse from the Pulse generator (see Fig. 1) to the 200 fF capacitor (called subtraction capacitor, C_{sub}) included in the Subtraction circuit block.

Therefore, the charge quantum is defined by the relation $Q_c = C_{sub}V_{sub}$, where V_{sub} is defined as the difference between two reference voltages (V_{pulse+} and V_{pulse-}), which are set externally in a range between 0.5 and 4.5 V.

A voltage variation V_{sub} across the subtraction capacitor C_{sub} corresponding to a voltage variation of $\Delta V = V_{sub}C_{sub}/C_{int}$ across the integration capacitor C_{int}.

The voltage variation ΔV is applied at the input of the comparator, and must be able to reduce the output of the OTA resetting the status of the comparator. The minimum charge quantum is set by the resolution of the comparator and is limited in the present design to 100 fC [8].

The overall schematic of the ASIC is shown in Fig. 2. The following signals can be externally set and are common to all channels: OTA reference voltage (V_{ref}), comparator thresholds (V_{th}), V_{pulse+} and V_{pulse-}.

The counters can be zeroed via a common asynchronous digital input, *reset.* The read-out of the counters can be done independently with respect to any other operations. Asserting the *latch,* the actual bit configuration of each 16-bit counter is stored in a 16-bit register. This operation is done in parallel for all the 64 channels. Any given channel can be acquired by addressing it via the six digital inputs (*Channel select* lines). The appropriate register is multiplexed to the 16-bit output bus signal through *MUX*.

It is worth mentioning the following: (a) the latch operation is done at the same time for all the channels, the counters are copied to the registers when the counting transitions are completed; (b) though the acquisition has to be done channel by channel, the counters are latched to the registers at the same time thus, data refer to the same instant; and (c) the acquisition being independent of the
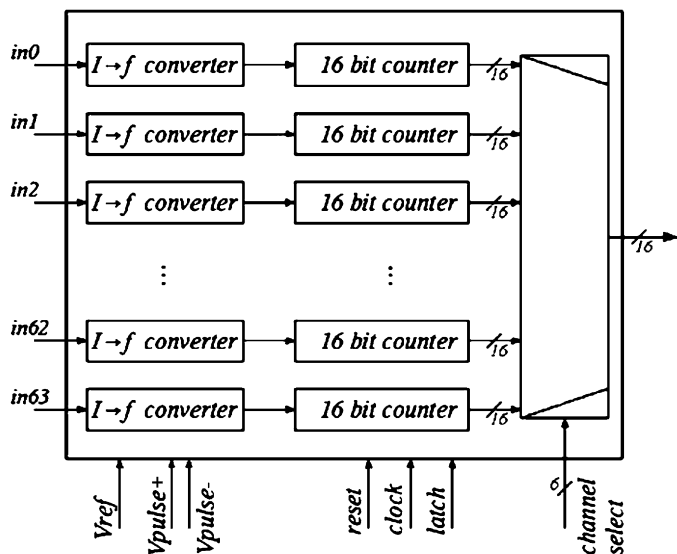
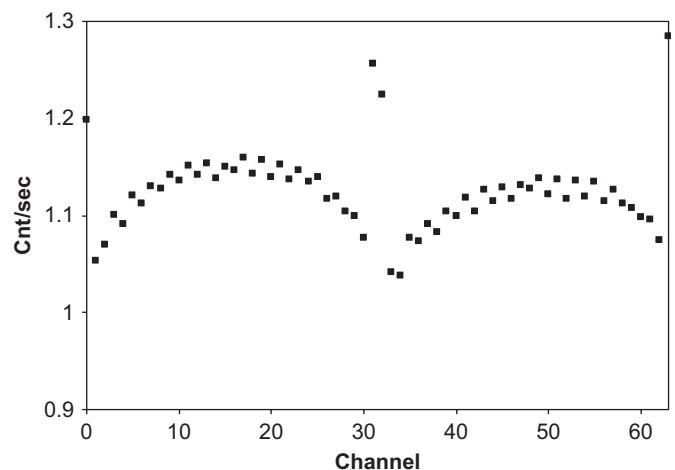Fig. 2. Architecture of the 64-channel charge measurement ASIC [8].

Fig. 3. Distribution of the average background counts per second as function of the channel. The average has been computed over the 113 chips.
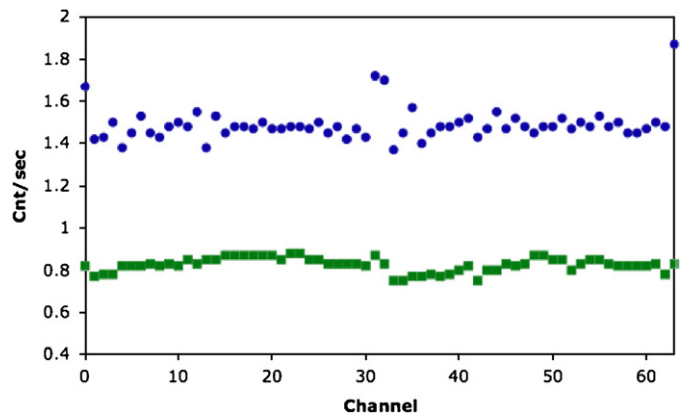

Fig. 4. Background counts distribution on three different chips: the highest (●) and the lowest (■) number of counts per second.

pulse counting, the data acquisition does not stop the counter activity, thus there is no dead time due to read-out.

The chip works with a clock frequency of 20 MHz and the maximum frequency of the counters is one fourth of the clock frequency corresponding to 5 MHz.

3. Test results

The experimental setup, which has been used to characterize the chip, is based on a National Instrument PCI DAQ card and LabVIEW software [10,11].

For most of the tests, we need to inject a precise constant current into a given channel. This was done using a Keithley 2400 V generator connected to the chip input via a large resistor (10 MΩ). The voltage generator provides a precise voltage source in the range between 1 μV and 211 V, which corresponds to a current from 0.1 pA to 21 μA, which is measured by the instrument itself with a 0.012% accuracy.

The performance of 113 chips has been studied, with a fixed charge quantum of 200 fC (charge quantum value that will be used with the detector), by measuring:

1. background currents,
2. charge quantum;
3. linearity of current-to-frequency converter,
4. stability of the charge quantum,
5. temperature dependence of the background counts and the charge quantum.

3.1. Background current

Fig. 3 shows the number of counts per second when no current is injected. In this configuration, the inputs are left open in order to measure the background current of each channel. The values plotted have been obtained by averaging the frequencies measured for the corresponding

channels over the 113 chips. Fig. 4 shows the results obtained from two chips corresponding to the highest and the lowest.

Setting a theoretical charge quantum of 200 fQ, we have measured that the mean value of the background current is 194 fA. It is worth mentioning that this value is more than 6 orders of magnitude smaller than the typical current, that is the detector current for a standard setup at beam intensity used in hadrontherapy.

From Fig. 3, it is possible to recognize a pattern of the background, which is related to the layout design where the channels 0, 31, 32, and 63 are housed on the corners of the chip detecting more charge than the other channels.

3.2. Charge quantum value

The charge quantum has been measured by injecting a fixed current to all channels of the 113 chips. The spread of the charge quantum over the channels of the 113 chips has been measured. Fig. 5 shows the results for charge
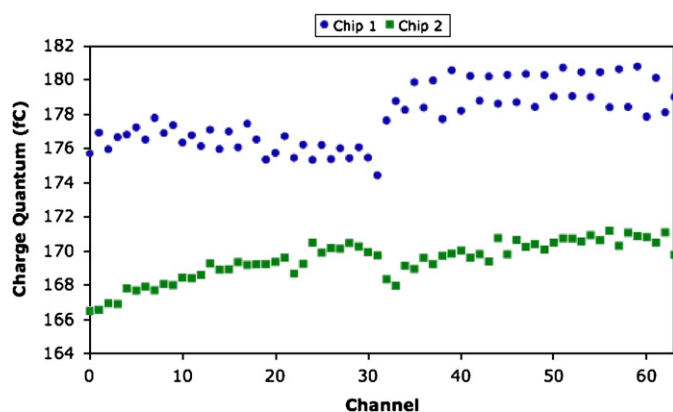
Fig. 5. Charge quantum distribution of two chips for fixed input current for a theoretical charge quantum of 200 fC as function of the channel.
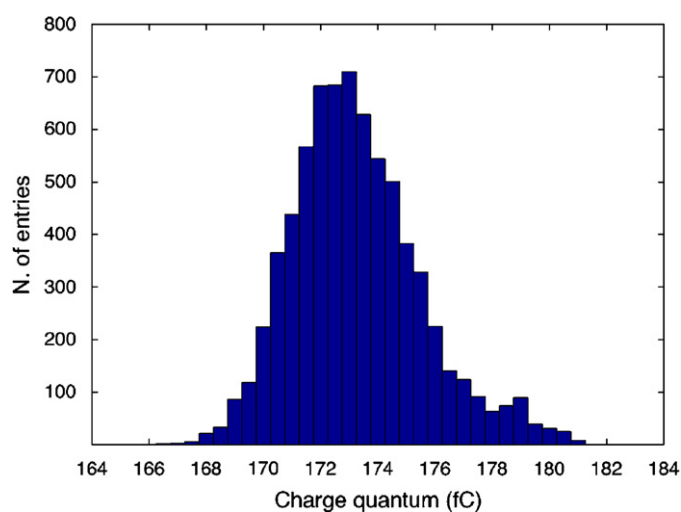

Fig. 6. Distribution of charge quanta of the 113 tested chips, for fixed input current for a theoretical charge quantum of 200 fC.
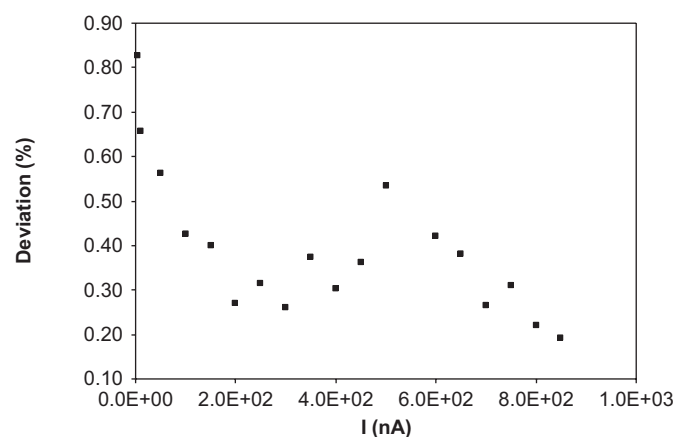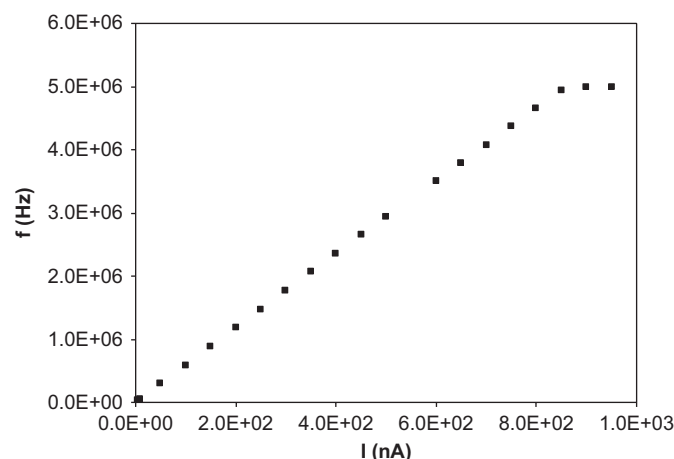

Fig. 7. (top) Frequency as a function of an input current for a theoretical charge quantum of 200 fC. (bottom) Deviation from linearity as a function of an input current for a charge quantum of 200 fC.

quantum of 200 fC. The upper (circles) and the lower (squares) points represent the 64 channels of the chips with the highest and the lowest charge quantum in the series.

Fig. 6 shows the charge quantum distribution over 113 chips. We observe that the mean value is 173 fC and the r.m.s. spread is 2.3 fC, or 1.3%.

The difference between the nominal value of 200 fC and the measured 173 fC is mainly due to the tolerance of the integrator capacitor and to the parasitic capacitor in the Subtraction circuit block (see Fig. 1). It is worth mentioning that this kind of difference arises after the front-end electronics calibration.

3.3. Linearity of current-to-frequency converter

Fig. 7 shows the linearity of current-to-frequency converter of a typical channel for a charge quantum of 200 fC. In the same figure, the relative deviation from the linearity as a function of the input current is shown. The maximum deviation is less than 1% over a dynamic range of 10^3.

3.4. Stability of the charge quantum value

To check the stability of the charge quantum, the same measurements in the same conditions described in Section 3.2 have been done twice, three weeks apart, where the charge quantum has been measured by injecting a fixed current. From the measurements made on two selected chips, we have obtained, respectively, the charge quantum and the standard deviation reported in Table 1.

Fig. 8 shows the results obtained from measurements made on two selected chips. The relative deviation is below 0.12%.

3.5. Temperature dependence of the background counts and the charge quantum value

An important parameter is the stability of the background and the charge quantum value with temperature variations. We have studied this in a range of temperature between 15° and 30°.

Fig. 9 shows the variation of the background versus the temperature of a typical channel for a charge quantum of 200 fC. From the measurements done, it is possible to note the variation is less than 0.1 Hz per °C.

Table 1
Charge quantum and the standard deviation of the measurements made on two selected chips, to check the stability of the charge quantum

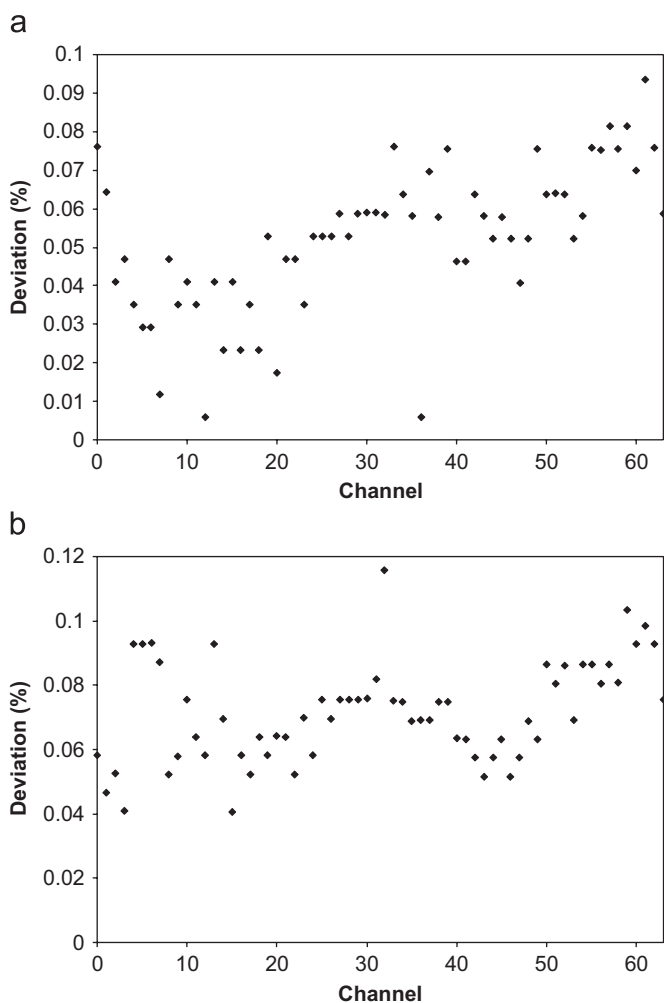|	Charge quantum (fC)	Standard deviation (fC)
Serie 1	171.4	0.9
Serie 2	171.3	0.8
Serie 1	172.9	0.9
Serie 2	171.8	0.9

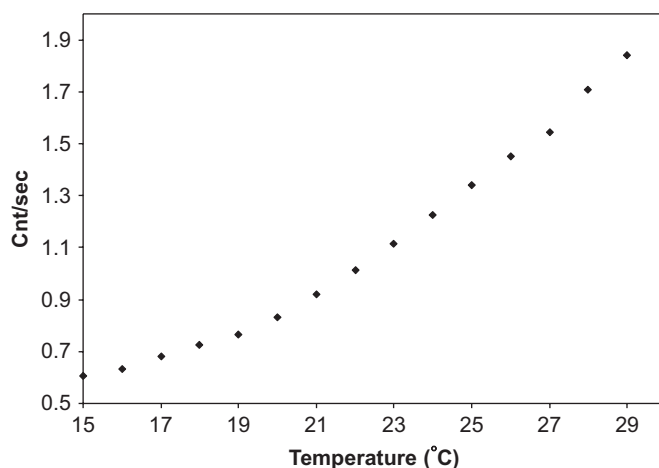Fig. 8. Stability of the charge quantum value of two Tera06 chips (a, b).

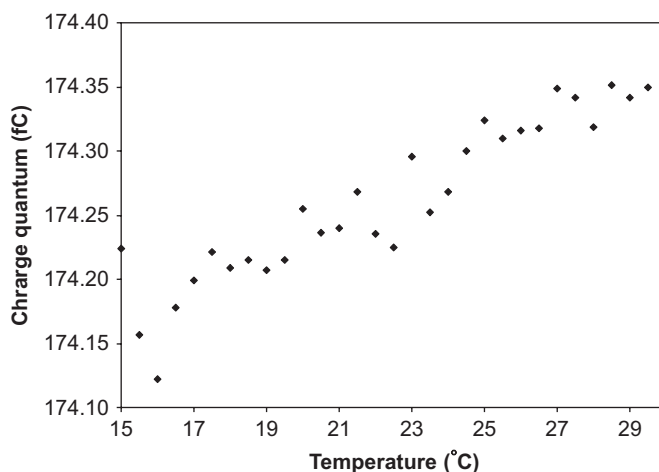Fig. 9. Variation of the background counts versus the temperature of a typical channel for a charge quantum of 200 fC.

Fig. 10. Variation of the charge quantum versus the temperature of a typical channel for a charge quantum of 200 fC.

Fig. 10 shows the variation of the charge quantum versus the temperature of a typical channel for a charge quantum of 200 fC. The variation of the charge quantum per °C is <0.01%. This variation is completely negligible for the practical use of the chip.

It is worth mentioning that the ASICs will be used in a room where the temperature will be controlled to be around 22–23 °C.

4. Conclusions

An integrated 64-channel device in CMOS $0.8\,\mu m$ technology has been developed by INFN and University of Torino. Each channel contains a current-to-frequency converter based on a charge balancing principle and followed by a 16-bit synchronous counter.

The background current is less than 230 fA with a mean value of 194 fA, while the spread of the charge quantum (r.m.s.) is 1.3% for a charge quantum of 200 fC. The variation of the charge quantum versus the temperature is <0.01% per °C.

The deviation of the response from linearity for negative currents over a current input dynamic range of 10^3 is <1%.

The ASICs will be used for the read-out of parallel plate pixel and strip ionization detectors that will be used at CNAO to perform measurement of position and intensity of the therapeutic beams.

Acknowledgements

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