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NUCLEAR
INSTRUMENTS
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RESEARCH
Section A

MICA: a multichannel integrated charge amplifier for the read-out of multielectrode detectors

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A 16 channel, fully parallel, CMOS integrated circuit including a preamplifier, a shaper and a discriminator, has been designed and succesfully tested in the laboratory and on the detector. It combines fast shaping (28 ns peaking time) with good noise performance (600 + 18/pF electrons ENC). The shaper can be tailored for both delta and tail currents with positive or negative polarity. The discriminator has an ECL compatible output with a threshold sensitivity of ±5000 electrons. It seems well suited for the read-out of 1-D and 2-D microstrip gas chambers as well as for silicon microstrip detectors or other multielectrode detectors with parallel digital read-out and moderate sampling pitch.

1. Introduction

Highly subdivided detectors (wire chambers, pad chambers, segmented calorimeters, etc. · · ·) with multielectrode read-out have become since many years, the most widely used instruments for doing high-energy physics research at existing particle accelerators. This process has been dramatically speeded-up in the last few years by the emerging of new detection technologies (silicon microstrip detectors, microstrip gas chambers) with a read-out pitch in the sub-millimeter range and by the requirements set by the new high luminosity colliders (LHC. SSC, B factories, etc. · · ·) which will be put in operation in the present decade. The high channel density (~ 100 channels per cm of detector), the 2-D read-out capability, the limited available transmission bandwidth and the mandatory fast processing and acquisition time, all point towards the need of highly parallel, integrated, low-noise, low-power consumption electronics to be mounted as close as possible to the detector itself.

In a previous paper [1] we have presented the design and test of a multichannel integrated circuit with both analog and TTL digital output, specifically designed for the read-out of the microstrip gas chamber [2]. It combined very high sensitivity (9 mV/1000 electrons) and fast shaping (25 ns peaking time), with good noise performance (700 electrons ENC for 5 pF input capacity). The main limitations of this design were the digital threshold which could not be lower than 30000 electrons, the unipolar operation (only positive signals were accepted) and the relatively low channel density (8 channels/chip). To overcome these limits and to make it useful also for a wider (faster) class of detectors, a new version of this chip with the following goals has been designed:

- provide 16 fully parallel channels/chip,
- lower the digital threshold to 5000 electrons,
- modify the front-end preamplifier so that it will accept bipolar input currents without significant distortion,
- provide a differential analog output to reduce the cross-talk between channels,
- provide a differential analog output current in order to drive a coaxial cable and to adjust the output stage gain by means of external resistors,
- reduce the discriminator logic swing by providing an ECL digital output in order to limit the capacitive coupling between output and input pads,
- reduce the overall gain to alleviate oscillation problems,

A new feature has also been added that allows the tail cancellation network to be disabled and therefore pro-

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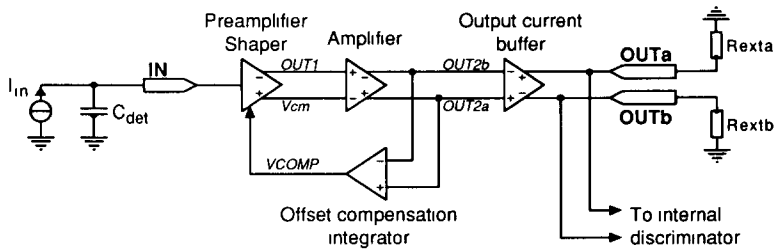

Fig. 1. Charge sensitive amplifier and shaper circuit principle.

vides a very fast shaping for fast current input (such as the one delivered by a microstrip silicon detector).

The new chip has been named MICA for Multi-channel Integrated Charge Amplifier.

2. The charge sensitive amplifier and shaper

2.1. Principle

The charge sensitive amplifier and shaper principle is described in fig. 1. The first block corresponds to the preamplifier combined with the shaper, the second block provides additional voltage gain ($A_{DC} \approx 5$) and single-ended to differential conversion. An additional feedback amplifier had to be introduced in order to compensate for the offset voltage produced by the preamplifier. The DC offset voltage at the amplifier output (OUT2a, OUT2b) is sensed, integrated and applied to the VCOMP auxiliary input to cancel the output offset. The final block is simply a transconductance stage that provides the differential output current to the external loads or to the input of the discriminator circuit.

2.2. The preamplifier

The circuit principle of the preamplifier/shaper is presented in fig. 2. The transconductor g_{m2} and the voltage followers ($\times 1$ blocks) that appeared in the previous design (cf. fig. 5 of ref. [1]) have been removed in order to provide bipolar operation capability and to reduce the power consumption. However, the general principle of operation is approximately the same. Considering small-signal operation, the transimpedance of the preamplifier presented in fig. 3 is given by:

$$Z_m(s) = \frac{R_m}{1+s\tau_{in}} \quad \frac{1+s\tau_{tc}}{1+bs+cs^2}, \tag{1}$$

where

$$R_m = \frac{1}{g_{m3}(1+g_{m4}R_{tc})}, \tag{2}$$

$$\tau_{in} = \frac{C_{det}+C_{in}}{g_{msl}}, \tag{3}$$

$$b = \frac{\tau_4+\tau_{tc}}{1+g_{m4}R_{tc}}, \tag{4}$$

$$\tau_4 = C_4/g_{m3}, \tag{5}$$

$$c = \frac{\tau_4\tau_{tc}}{1+g_{m4}R_{tc}}, \tag{6}$$

$$\tau_{tc} = R_{tc}C_3. \tag{7}$$

Assuming $\tau_{tc} \gg \tau_4$ and $g_{m4}\ R_{tc} \gg 1$, leads to:

$$Z_m(s) = \frac{R_m}{1+s\tau_{in}} \quad \frac{1+s\tau_{tc}}{1+s\frac{\tau_s}{Q}+(s\tau_s)^2}, \tag{8}$$

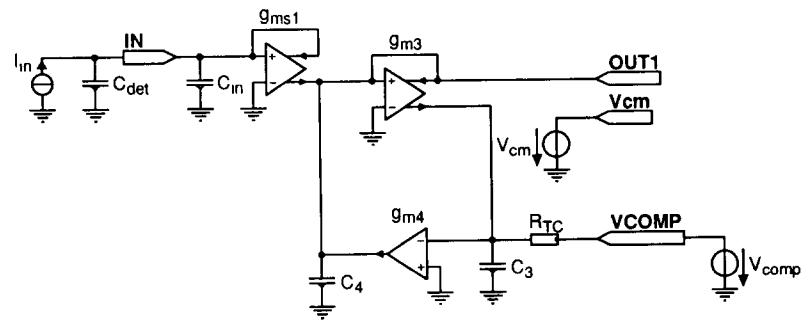

Fig. 2. Preamplifier/shaper circuit principle.

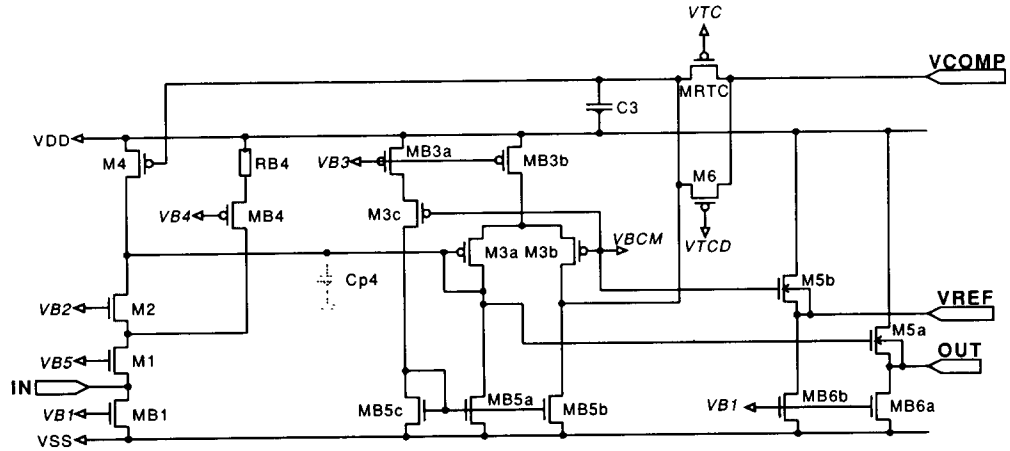

Fig. 3. Preamplifier/shaper circuit schematic.

where

$$R_m \cong \frac{1}{g_{m3}g_{m4}R_{tc}}, \tag{9}$$

$$\tau_3 = \frac{C_3}{g_{m4}}, \tag{10}$$

$$\tau_s \cong \sqrt{\tau_3\tau_4} = \sqrt{\frac{C_3C_4}{g_{m3}g_{m4}}}, \tag{11}$$

$$Q = \frac{\tau_s}{\tau_3} = \sqrt{\frac{g_{m4}C_4}{g_{m3}C_3}}. \tag{12}$$

The shaping time τ_s depends on the product of g_{m3} and g_{m4}, while the quality Q factor depends on the ratio of g_{m3} and g_{m4}. The nominal values of g_{m3} and g_{m4} are fixed by integrated resistors and they can be tuned by adding some external resistors.

The preamplifier can also be used with much shorter input current pulses (delta input current) by disabling the tail cancellation setting VTCD to VSS. This is equivalent to set R_{tc} to zero. In this case the transimpedance becomes:

$$Z_m(s) = \frac{1}{g_{m3}} \frac{1}{(1+s\tau_{in})(1+s\tau_4)}. \tag{13}$$

2.3. The 2nd stage amplifier

The 2nd stage amplifier shown in fig. 4 is a simple g_mR gain stage that also provides single-ended to differential conversion. To obtain a global gain of 25 [mV/fC], the additional gain has been set to 5. The transconductor formed by differential pair M1a–M1b has been cascoded to reduce the output parasitic capacitance in order to increase the amplifier speed.

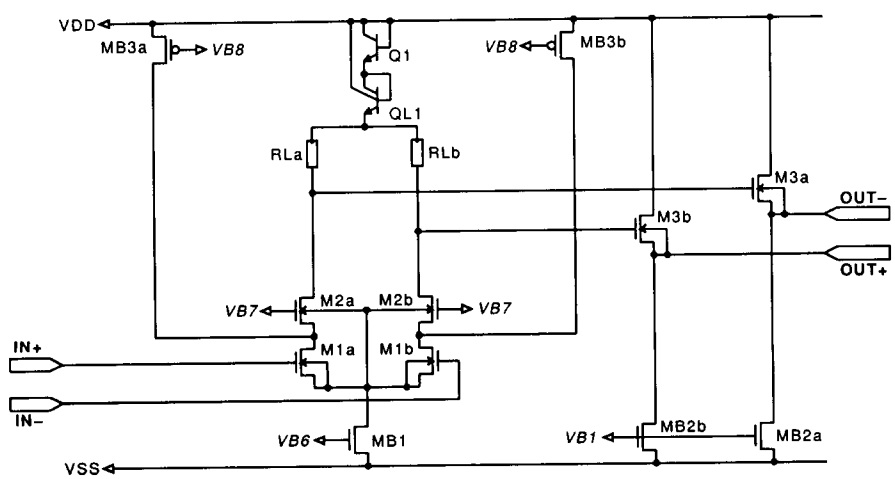

Fig. 4. Amplifier circuit schematic.

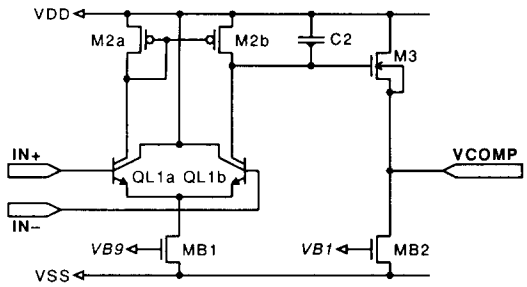

Fig. 5. Offset compensation amplifier circuit schematic.

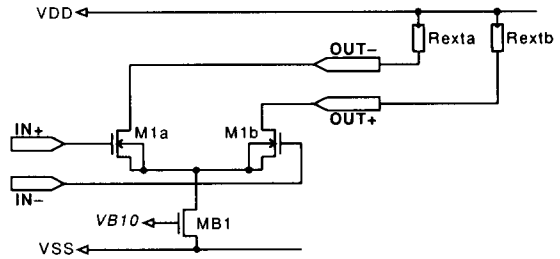

Fig. 6. Current output buffer circuit schematic.

2.4. The offset compensation block

The offset voltage appearing at the output of each channel has mainly two constituents: a systematic (purely deterministic) and a random component. The systematic offset, which is common to every channel, would not be troublesome if it did not introduce an asymmetry between positive and negative signals. The random offset generated in the preamplier stage and amplified at the channel output, is due to mismatches between two paired devices of one channel and between devices of different channels. It has the same effect than the systematic offset but is different for each channel.

To avoid any external offset compensation system, both offset component are cancelled at the amplifier output of each channel by means of the circuit presented in fig. 5. This circuit senses the DC voltage at the output of the amplifier, integrates this error and feeds a correction voltage at the preamplifier VCOMP input that compensates for any offset introduced between the preamplifier and the amplifier output. The input differential pair has been implemented using Compatible Lateral Bipolar Transistors (CLBT) [3] in order to minimize the input offset of the compensation integrator. Furthermore, the integration time has been chosen much larger than the tail cancellation time constant ($\tau_{comp} \approx 250\tau_{tc} \approx 50$ μs).

2.5. The output current buffer

In order to drive a coaxial cable of reasonable length and to adjust the gain externally by means of two external resistors, the output signal is driven by a differential current. The transconductance of the output buffer shown in fig. 6 is approximately equal to 1 [mA/V]. The gain is then equal to unity if both external resistors are equal to 1 kΩ. To reduce the effect of the load capacitance, it is recommended to precede the load resistors by two current followers (common base configuration) having a transconductance of the order of a few [mA/V].

3. The discriminator

The circuit schematic of the discriminator is presented in fig. 7. It is a cascade of 3 low-gain differential amplifier stages. The output current of the charge amplifier buffer is fed to resistors R_{L1a} and R_{L1b} by two current followers. The adjustable threshold is im-

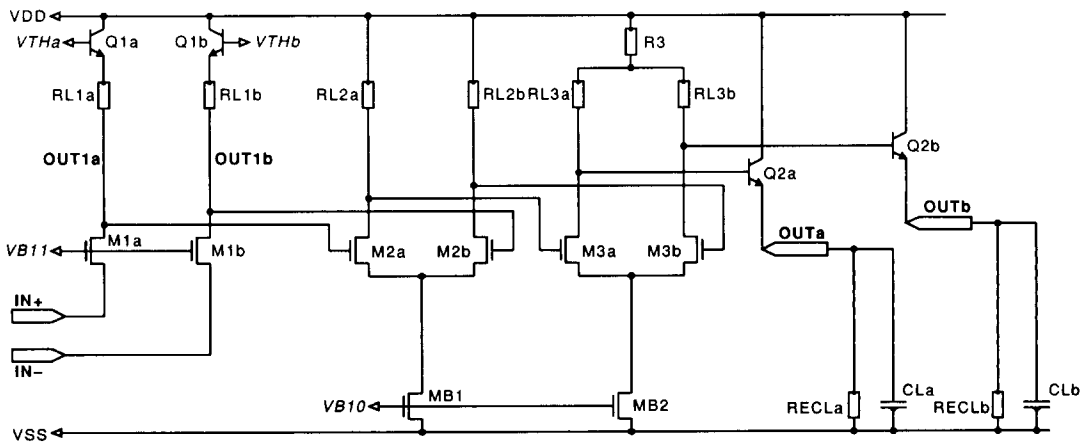

Fig. 7. Discriminator circuit schematic.

plemented by two bipolar voltage followers. A threshold corresponding to positive (negative) injected charges is imposed by biasing VTHa (VTHb) at voltage lower than VDD keeping VTHb (vTHa) connected to VDD.

The gain of the first stage is equal to 5. The peak amplitude of the differential voltage between nodes OUT1a and OUT1b for $Q_{in\infty} = +250\,000$ electrons ($Q_{ineff} \approx 0.1$ or $Q_{in\infty} = 25\,000$ electrons) and $\tau_t = 200$ ns is approximately 500 mV. A difference between VTHa and VTHb voltage of 100 mV corresponds thus to an effective injected charge $Q_{ineff} = 5000$ electrons.

In order to reduce the coupling of the discriminator output to the input of the charge amplifier an ECL compatible output has been chosen for its balanced voltages and for its low voltage swing. The output stage

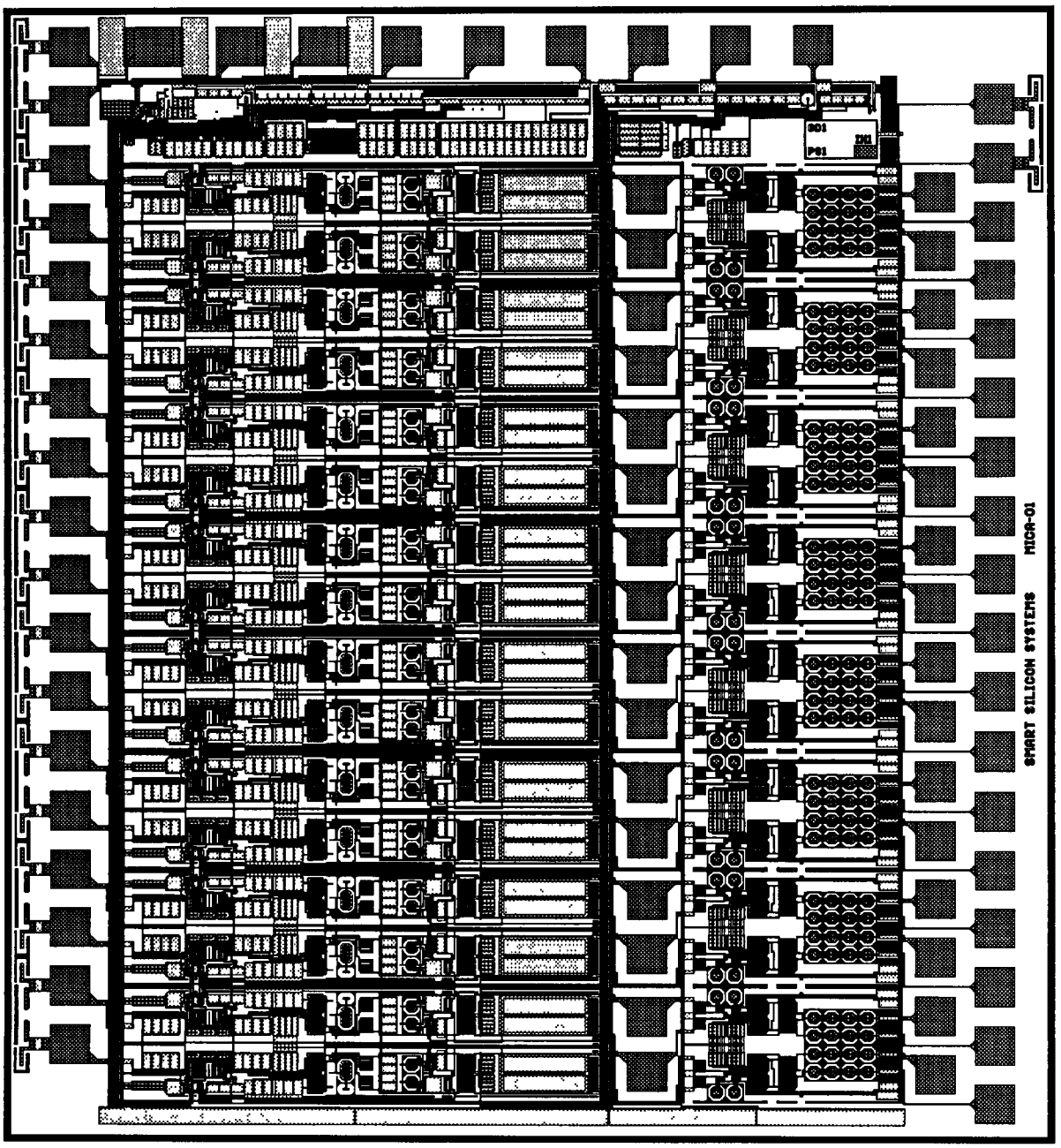

Fig. 8. Layout of MICA.

is again a current buffer stage that should be loaded by two external resistors R_{ECLa} and R_{ECLb}. To be fully compatible with an ECL gate [4], the circuit should be biased with VDD connected to ground (VDD = 0) and VSS = −5 V. In such biasing conditions with $R_{ECLa} \approx$ 4.1 kΩ, the output voltage are set to the ECL logic voltages −0.9 V and −1.7 V.

4. The bias

The bias circuit provides all the bias voltages V_{B1} to V_{B11} that impose all the quiescent currents.

Except for the threshold voltages which have to be provided externally, all the circuit is selfbiased for nominal operating conditions. However, some parameters can be adjusted independently within ±20% around their nominal values, by means of external resistors. These include the peaking time constant τ_s, the quality factor Q and the preamplifier current follower speed corresponding to τ_{in}. Note that this allows the circuit to be adapted for detectors having a capacitance larger than 5 pF.

5. The layout

The dies are supposed to be glued on the same substrate then the detector, allowing the chip input pads to be directly bonded to the detectors. This imposes that the height of the die should stay smaller than 16 times the pitch of the detector chosen to be 200 μm. The die size after sawing should thus be smaller than 3.2 mm. For this reason the circuit height has been set to 3 mm leaving some free space for the border. In order to have some place for the biasing circuit on top of the 16 channels, the channel height and pitch has been set to 150 μm. A plot of the layout is shown on fig. 8. The core of the circuit is composed of 8 rows containing each 2 channels that are mirrored in order to share the same power and bias buses. All outputs of the charge amplifier are directly connected to the input of the discriminator and 1 channel among 2 is connected to intermediate pads giving access to the analog signal coming from the charge amplifier and to the input of the discriminator. Since the top pads will not be usable when the dies will be glued side by side, all the indispensable pads have been put on the left and the right side of the chip. Those include the input pads, the differential output pads, the power pads, the peaking time biasing pad, the tail cancellation pad and the threshold voltage pads.

6. Simulation results

Simulation have been performed using ESACAP simulation program [5]. The detector has been modeled by a current source $I_{in}(t)$ injecting a positive entering current defined by:

$$I_{in}(t) = \frac{Q_{in\infty}}{\tau_t} \exp\left(-\frac{t}{\tau_t}\right) \tag{14}$$

in parallel with a capacitor $C_{det} = 5$ pF.

All the simulation have been made with each analog output loaded with a resistor $R_{Lext} = 1$ kΩ in parallel with a capacitor $C_L = 5$ pF.

Fig. 9 shows the differential voltage at the output of the charge amplifier for the nominal signal $Q_{in\infty} = +250\,000$ electrons and $\tau_t = 200$ ns. The peaking time is found to be about 30 ns, the FWHM is 51 ns, the rise time is 22 ns and the fall time is 52 ns. The peak

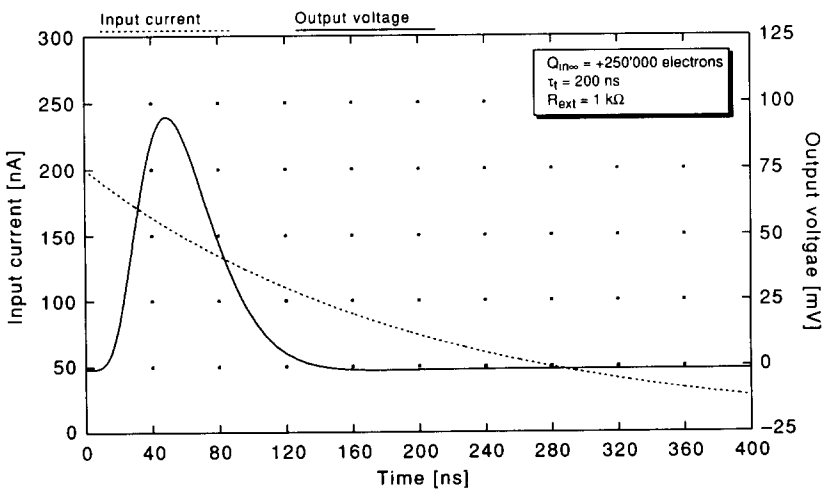

Fig. 9. Differential output voltage with tail cancellation enabled.

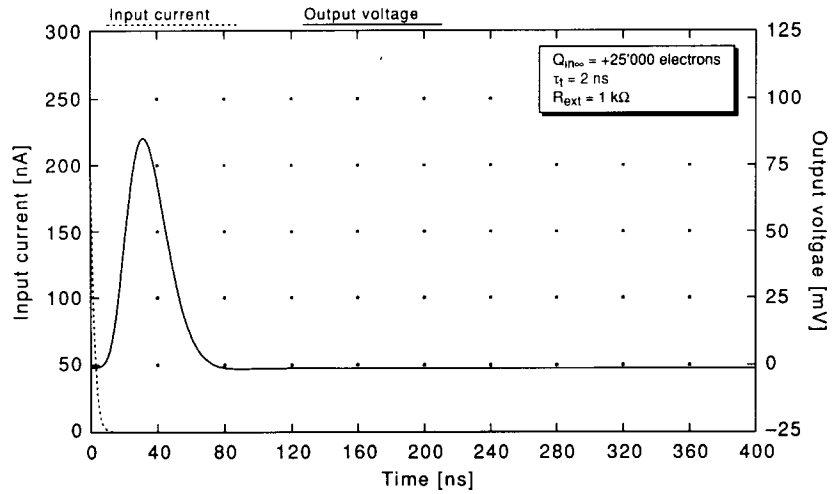

Fig. 10. Differential output voltage with tail cancellation disabled.

amplitude is 96 mV. If the gain is defined by the ratio of this peak amplitude to an effective input charge $Q_{in\text{-}eff}$ corresponding to 10% of the total injected charge delivered after about 20 ns, the gain can be estimated to 3.84 mV/1000 electrons or 24 mV/fC.

Fig. 10 shows the output voltage with the tail cancellation disabled for a positive effective input charge of 25 000 electrons with $\tau_t = 2$ ns (delta current response).

Figs. 11 and 12 show the output of the discriminator for a threshold voltage $V_{th} = 100$ mV for different effective input charges $Q_{in\text{-}eff}$ (5000 and 50 000 electrons respectively) and with $\tau_t = 200$ ns. In order to have ECL compatible output voltages, the VDD and VSS power supplies have respectively been set to 0 and -5 V. The external load is composed of a 4.1 kΩ resistor in parallel with a 5 pF capacitor.

Fig. 11 shows that the two ECL output voltages (ECL+ and ECL−) just reach the -1.3 V ECL threshold voltage, which confirms that 100 mV threshold correspond approximately to an effective charge of 5000 electrons.

7. Experimental results

Several non encapsulated dies were mounted on a printed circuit board developed in house and extensively measured in the laboratory. Fig. 13 shows the averaged delta current response of one of the comple-

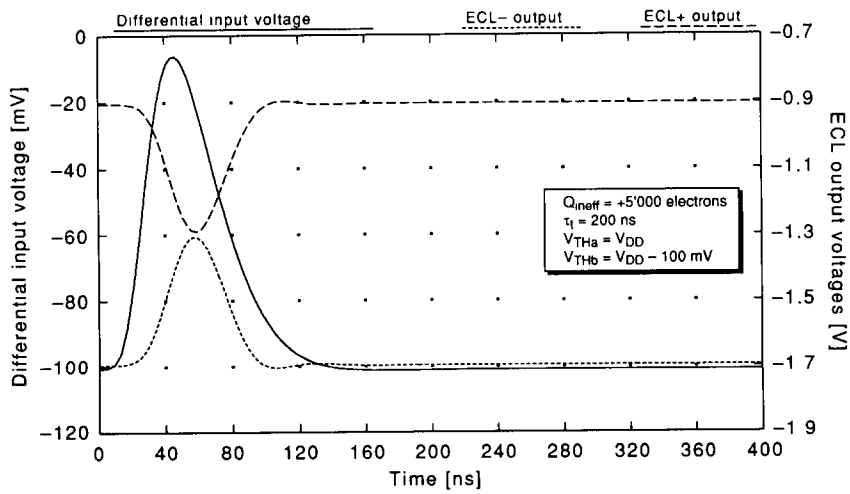

Fig. 11. Discriminator ECL output voltages.

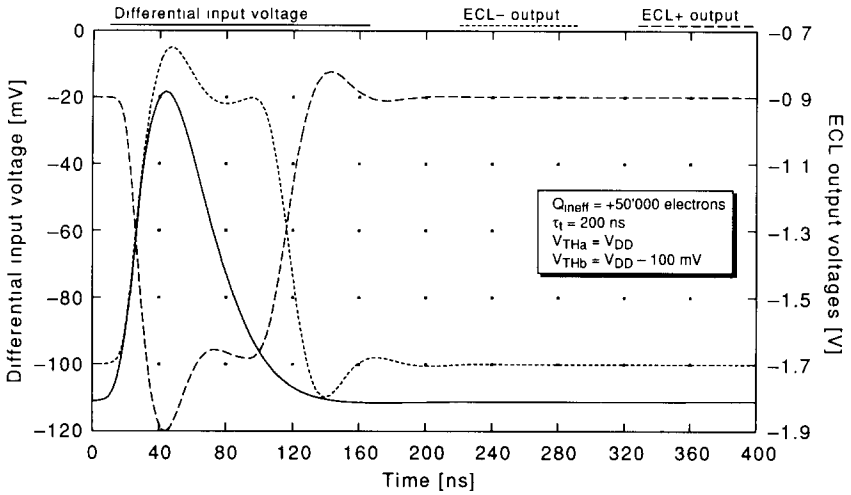

Fig. 12. Discriminator ECL output voltages.

mentary analog output to an injected charge of 27000 electrons as observed on a digital oscilloscope (Tektronix 2440). To study the response to a delta current the tail cancellation network was disabled connecting VTCD to VSS. Note that if the tail cancellation is enabled for the same delta current input, the output voltage has a bipolar shape. This is due to the shaper quality factor which is approximately equal to 0.6. The observed signal rise time is 18 ns, the fall time is 43 ns, the peaking time is 28 ns, the full width at half maximum (FWHM) is 37 ns and the peak amplitude is 100 mV. The measured overall gain of the analog chain is therefore 3.7 mV/1000 electrons or 23 mV/fC. The symmetric operation of the amplifier with both positive and negative currents is demonstrated in fig. 14 which shows the response to a rectangular wave injecting positive and negative charges into the input stage of the preamplifier. The amplifier linear range corresponds roughly to an effective input charge between -50000 and $+50000$ electrons.

To model the tail of the detector ion current, the passive network of fig. 15 was connected to the channel input. The step response of this network is an exponentially decaying pulse with ~ 200 ns time constant. The upper trace of fig. 16 shows the analog output when the tail cancellation circuit is disabled, while the lower trace shows the corresponding analog output when the cancellation circuit is enabled. The fall time of the signal is reduced from 500 ns to 50 ns. The shapes of these signals are very close to those obtained with the simulation, indicating that the tail cancellation circuit works as expected and the good reliability of the simulation procedure.

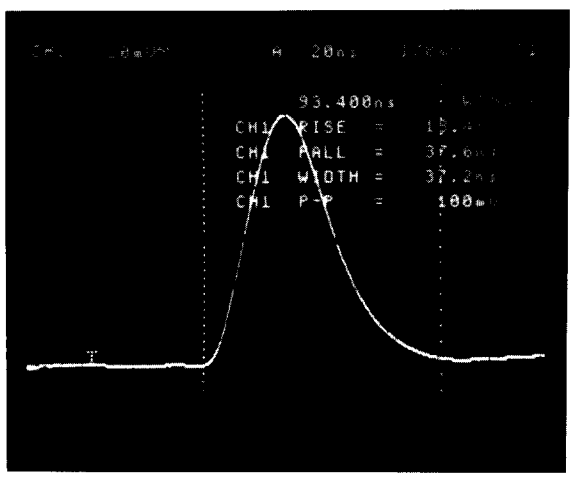

Fig. 13. Measured delta current response at the analog output ($Q_{in\text{-}eff} = 27000$ electrons,).

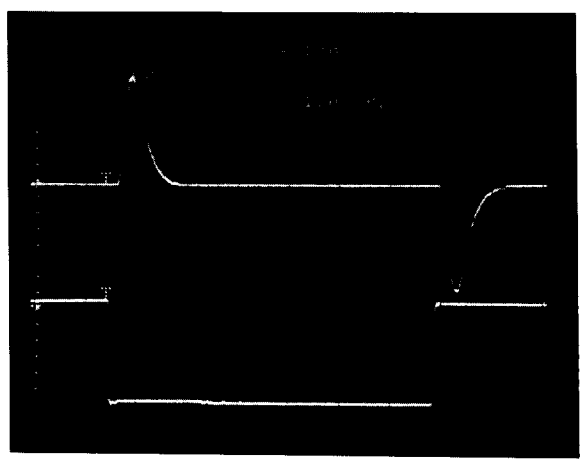

Fig. 14. Measured delta current response to positive and negative currents.

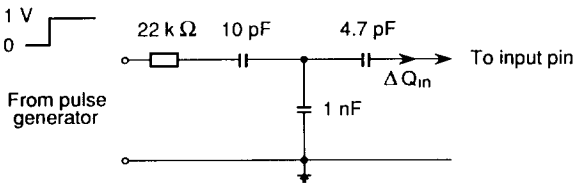

Fig. 15. The passive network used to inject an exponential current into the input stage of the preamplifier.

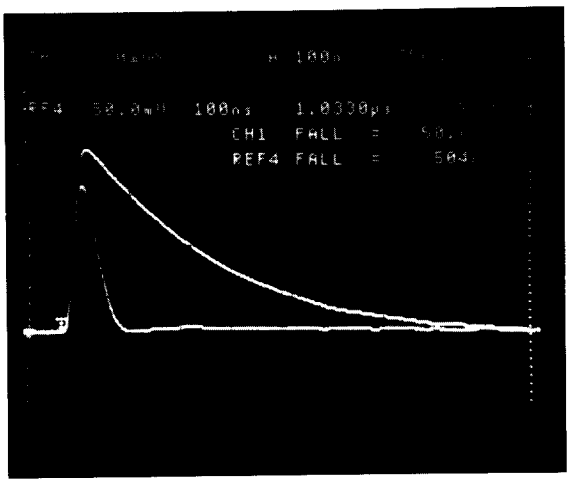

Fig. 16. Measured analog output response to an exponential current when the tail cancellation is disabled (upper trace) and when is enabled (lower trace).

The noise performance of the circuit has been studied utilizing the measuring capability of the digital oscilloscope connected to a personal computer. The RMS voltage of the analog output when nothing was connected to the input ($C_{det} = 0$) has been measured to be 2.1 mV, corresponding to a ENC of 570 electrons. The dependence of the noise on the input capacitance has been obtained by repeating the previous measurement but with several calibrated capacitors connected between the input pad and the ground. A sensitivity of 18 electrons/pF has been measured (see fig. 17).

For our purposes, the most important characteristic of the digital section is the minimum threshold. This feature is shown in fig. 18. The upper bipolar trace is the analog response to a rectangular wave injecting, ±5000 electrons, while the middle and lower trace are the corresponding ECL complementary digital outputs for the same input pulse. In this case the threshold was set to trigger on the negative going pulse. The analog positive going pulse wich do not fire the discriminator is completely unaffected by the digital section, while the analog triggering signal shows a small shoulder due to some capacitive coupling of the digital pulse to the amplifier input. We believe that this small residual coupling could be furtherly reduced when removing the large analog output pads, as expected for a fully digital operation. Below a digital threshold of ±5000

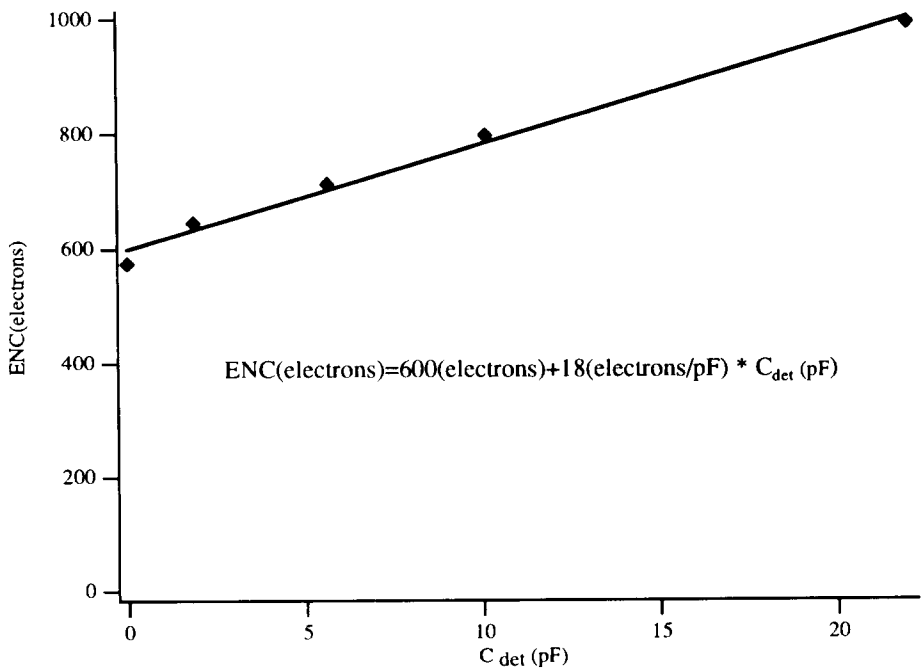

Fig. 17. Measured sensitivity of noise on input capacitance.

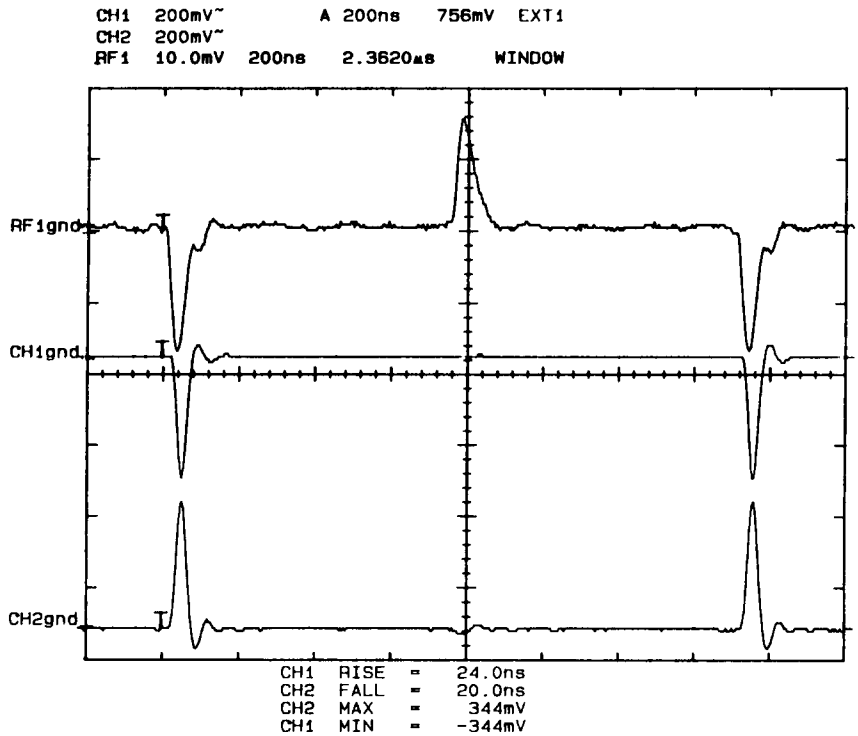

Fig. 18. Measured analog response to ±5000 electrons (upper trace); corresponding complementary digital outputs (middle and lower trace).

electrons the circuit shows some instability which makes it prone to oscillate.

After the bench test, a non encapsulated die was mounted on a microstrip gas chamber. Sixteen anode strips were AC connected to 16 input pads of the amplifier with a ultrasound bonding technique. The analog outputs were connected to a fast line driver (LH0002) to reduce the capacitive load and to observe the signals on a remote analog oscilloscope. Fig. 19 shows the complementary analog output signals when the detector was illuminated by the 8 keV photons from a X-ray tube. In this particular case the tail cancellation circuit was disabled. The main performance based on the previous measurements are summarized in table 1.

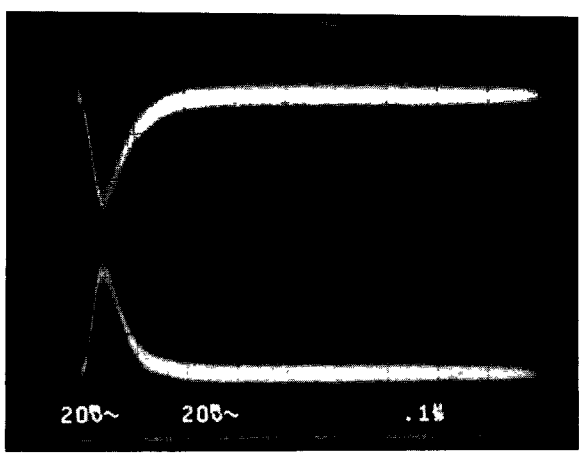

Fig. 19. Analog output signal observed from one microstrip when the detector is illuminated with 8 keV photons.

Table 1
Measured performance

Charge amplifier	
Gain	3.7 mV/1000 electrons (23 mV/fC)
Peaking time	28 ns
FWHM	37 ns
Rise time	18 ns
Fall time	37 ns
Noise	600 + 18/pF electrons rms
Chip power consumption	
Charge amplifier (1 chan.)	850 µA
Discriminator (1 chan.)	1.6 mA (+1.8 mA on R_{ext})
Bias	1.2 mA
Total current consumption	40 mA (+29 mA on R_{ext})
Power consumption	200 mW (+145 mW on R_{ext})
(@$V_{DD} - V_{SS} = 5$ V)	12.5 mW/chan. (+9 mW on R_{ext})

8. Conclusion

A 16 channels, fully parallel, CMOS, integrated circuit including a preamplifier, a shaper and a discriminator has been designed and succesfully tested in the laboratory and on the detector. It combines fast shaping (28 ns peaking time) with good noise performance (600 + 18/pF electrons ENC). The shaper can be tailored for both delta and tail currents with positive or negative polarity. The discriminator has an ECL compatible output with a threshold sensitivity of ± 5000 electrons. It seems well suited for the read-out of 1-D and 2-D microstrip gas chambers as well for silicon microstrip detectors or other multielectrode detectors with parallel digital read-out and moderate sampling pitch (≥ 100 μm).

Acknowledgements

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