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Performance Enhancement of Large Crossbar Resistive Memories with Complementary and 1D1R-1R1D RRAM Structures

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***Abstract*— The paper proposes novel solutions to improve the signal and thermal integrity of crossbar arrays of Resistive Random-Access Memories, that are among the most promising technologies for the 3D monolithic integration. These structures suffer from electrothermal issues, due to the heat generated by the power dissipation during the write process. This paper explores novel solutions based on new architectures and materials, for managing the issues related to the voltage drop along the interconnects and to thermal crosstalk between memory cells. The analyzed memristor is the 1 Diode - 1 Resistor memory. The two architectural solutions are given by a reverse architecture and a complementary resistive switching one. Compared to conventional architectures, both of them are also reducing the number of layers where the bias is applied. The electrothermal performance of these new structures is compared to that of the reference one, for a case-study given by a 4×4×4 array. To this end, a full-3D numerical Multiphysics model is implemented and successfully compared against other models in literature. The possibility of changing the interconnect materials is also analyzed. The results of this performance analysis clearly show the benefits of moving to these novel architectures, together with the choice of new materials.**

***Index Terms*— 3-D crossbar RRAM, 1D1R-1R1D, CRS, signal integrity, thermal integrity.**

I. Introduction

High demands for big data storage, high-performance computing, and deep learning are driving intense research efforts on next-generation memories [1]-[4]. Among these, binary oxide Resistive Random-Access Memories (RRAMs) are emerging as promising beyond CMOS technology to substitute FLASHs, thanks to their excellent nano-downscaling potential for increased storage density, high operating speed, low power operation, high energy efficiency, and long data retention [4]-[8]. In fact, RRAM electrical resistivity state can switch between Low Resistance State (LRS) and High Resistance State (HRS). A common implementation of this cell structure is to separate two electrodes by a metal oxide, being one of the electrodes active (for instance, made by nickel, Ni). Under suitable conditions involving voltage and/or temperature, ions are emitted from the active electrodes and may form a Conducting Filament (CF) between these electrodes, leading to the LRS (SET). Other conditions can instead lead to the CF breakdown, putting the memory into the HRS (RESET), as discussed later. Several technological solutions have been so far proposed to realize the elementary RRAM cell [9]-[10], and different oxides have been investigated, such as hafnium, titanium, aluminum, silicon, and vanadium oxide [10]-[20]. In addition, this structure is usually augmented by a series diode (e.g., $Pt/TiO_2/Ti$), to avoid the effects of sneaky currents during read/write, leading to the so-called 1 Diode – 1 Resistor (1D1R) RRAM cell.

As pointed out in literature [4]-[5], and [17], these elementary memory cells are suitable for monolithic integration, being arranged in a large number in 3D stacked arrays such as the 1D-1R crossbar structures proposed in [21]-[22]. However, the implementation of RRAMs in monolithic integration and neuromorphic applications faced significant reliability issues; for instance, the unwanted leakage currents and read/write disturbances in the crossbar array [23]-[28]. These issues are worsened by the downscaling of the structures: high-density 3-D stackable crossbar structures which introduce additional latency and power consumption, causing voltage IR drop along the bias delivery interconnects.

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For these reasons, the bias voltage level can be increased to and/or the delivery bias schemes can be adapted to mitigate IR voltage drop and therefore ensuring that each cell is supplied with the threshold voltage level for its correct operation with the loss of bit/information. Nevertheless, the increase of bias voltage for supplying the RRAM cells in a high-density integrated structure leads to thermal integrity issues related to the heat production by Joule dissipation. In turns, the huge increase of temperature inside the cells may lead to reliability issues, including performance degradation, due for instance to unwanted switching, [29]-[30].

Several solutions have been so far proposed to address the above signal and thermal integrity issues, including the use of novel bias schemes [31], novel heat management strategies, as the one in [32] based on "thermal houses", and novel materials, such as the carbon nanotubes proposed by the Authors in [33]-[34], to realize the conducting bars.

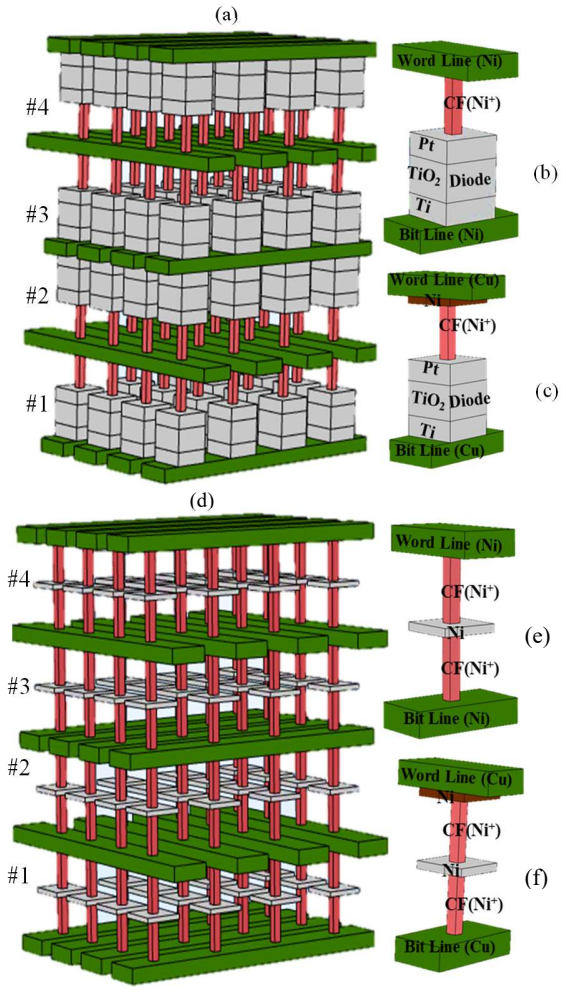

Fig.1. The novel proposed architectures for realizing a 4×4×4 RRAM array: a) 1D1R-1R1D reverse architecture; b) 1D-1R cell, with Ni bars; c) 1D-1R cell, with Cu bars and thin Ni layers; d) CRS architecture; e) CRS single cell, with Ni bars; f) CRS single cell, with Cu bars and thin Ni layers.

The main scope of this paper is to propose two novel architectures, namely a reverse and a complementary resistive switching, for realizing large arrays of RRAMs, comparing their performance in terms of signal and thermal integrity, to the conventional 1D-1R crossbar structure. For all the considered architectures, the elementary memory unit (also denoted as the "X-point") is the 1D-1R cell depicted in Fig.1b, made by the series of a Ni / HfO_2 / Pt resistor and a Pt / TiO_2 / Ti diode. The reference crossbar structure (see for instance [34]) is obtained by sandwiching planar arrays of 1D-1R between two sets of conducting bars, denoted as Word Lines (WL) and Bit Lines (BL). In the reference structures, these lines are made by Ni, so to realize the active electrode and to create a Ni conductive filament (see Fig.1b).

The two novel architectures proposed in this paper are depicted in Fig.1, referring to a 4×4×4 array. The first one (Fig.1a), is based on reversing the 1D-1R cell from one layer to another one. Hereafter, it will be denoted as the "reverse architecture". The second one (Fig.1d) is based on an elementary cell without the diode (Fig.1e): two memory cells are integrated into the array in such a way to realize two anti-serial resistive elements (Complementary Resistive Switching, CRS) sharing a thin common electrode [8]-[9]. This structure will be hereafter denoted as CRS architecture. For all the considered architectures, we assume the whole 3D structure to be surrounded by Hafnium dioxide (HfO_2) which is not shown in Fig.1.

Besides investigating these new structures, this paper also analyzes the advantages of using new materials and new biasing schemes. Specifically, it is proposed to realize the WL and BL bars by using Copper (Cu) instead of Nickel (Ni). In this case, a thin Ni layer is lying on the copper WLs (see Fig.1c and Fig.1f), so that the CF is still realized by Ni ions, as for the reference structure, as done in [34]. Finally, bi-lateral biasing schemes are also investigated.

The paper is organized as it follows. Section II presents the fully coupled multiphysics model that has been implemented in order to study the electrical and thermal responses of the proposed structures. In particular, an accurate modelling of the resistive switching mechanism is provided, leading to a suitable definition of the equivalent conductivity to be assigned to the CF of each cell. The results of the Multiphysics model of the single cell proposed here are successfully compared to those available in the literature.

In Section III, the two proposed architectures are investigated by means of the above model, along with novel materials and/or biasing schemes. Specifically, the voltage drop along the bars and the temperature distributions inside the structures are derived, so that the signal and thermal performance are evaluated and compared. The analysis is carried out during a RESET switching. Indeed, this is the most current-demanding operating condition, hence representing the worst case for signal and thermal integrity.

The conclusions, drawn in Section IV, highlight a significant improvement of the performance coming from the novel layouts, the use of new materials, and new biasing schemes for monolithic RRAMs.

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II. RRAM Cell and Multiphysics Model

A. 1D-1R cell and the SET and RESET process

As pointed out in the introduction, the starting point of our analysis is the 1D-1R cell given in Fig.1b. In order to introduce the multiphysics model and its parameters, it is needed to provide here a short description of the physical mechanisms leading to the destruction of the conducting filament (CF), hence to the switching from LRS to HRS (i.e., RESET).

In the considered cell, the formation/dissolution of the CF is a complex mechanism dictated by thermochemical reactions, including localized redox processes [35]-[36], and ion migration. The SET and RESET mechanisms may be described through defect migration (e.g., excess hafnium and oxygen vacancies) induced by the local values of electric field and temperature [37]. During the SET process, the ions are emitted from the active electrode and migrate through the oxide, under the action of a voltage bias applied to the active electrode (anode, positive top electrode, TE), whereas the bottom electrode, BE, is grounded (cathode). The LRS state reached by the cells after the CF is formed is also responsible for Joule heating that greatly increases its temperature, and provides the thermal energy necessary to facilitate ion migration. In the RESET process, the filament rupture is a consequence of a thermal effect: it ends up breaking due to the high temperature and the device turns back to HRS. The actual conditions that determine the rupture may significantly change from one RRAM to another one, for instance, due to a different metal oxide [38]-[41]. If the temperature increases as a consequence of the cell's self-heating, these conditions can be achieved by applying a minimum voltage level, typically V_{RESET} = 0.53 V [42]-[44]. However, the conditions for resetting a single cell can also be reached in absence of any voltage applied to that cell, as a consequence of a thermal exchange from the nearby cells. In this case, an unwanted RESET occurs, and hence the thermal crosstalk leads to the device failure.

Since the final goal of the paper is to compare different architectural arrangements of cells, rather than to study the single cell, a simplified model for the single cell has been here used. As detailed in the next paragraph, the formation/dissolution of the CF is simply described by an equivalent CF conductivity, that models the gradual and smooth transition between LRS and HRS occurring during the reset, following a non-linear law with respect to temperature. The V-I characteristic curve of such devices is known to be highly non-linear. In our simplified model, a linear approximation is used for the LRS and HRS, that can be adopted if we limit our analysis to the branch of the V-I curve that refers to the reset operation, as shown in [44]. With the above-mentioned limitations, this simple model is suitable for our purposes for perform the signal and thermal integrity analysis.

B. Electrothermal model and its validation

The electrothermal model is given by the following set of coupled thermal and electrical equations based on a finite element analysis simulation and implemented in COMSOL [45]. This involves the electric field, **E**, the electrical potential, V, the current density **J**, and the temperature distribution, T:

$$\nabla \cdot \mathbf{J} = 0 \quad ; \quad \mathbf{J} = \sigma(\mathrm{T})\mathbf{E} \quad ; \quad \mathbf{E} = -\nabla \mathrm{V}, \tag{3}$$

$$\rho(\mathrm{T})\, \mathrm{C_P}(\mathrm{T}) \frac{\partial \mathrm{T(t)}}{\partial \mathrm{t}} - \nabla \kappa(\mathrm{T}) \nabla \mathrm{T(t)} = \mathrm{Q_s}, \tag{4}$$

$$\mathrm{Q_s} = \mathbf{J} \cdot \mathbf{E}\,. \tag{5}$$

The electrical problem is described by the current continuity equation, Ohm's law, and the relation between the electric field and potential (3). The thermal one is formulated through the Fourier heat equation (4). The two problems are coupled by means of the Joule heat production term Q_s.

The parameters of the model, $\sigma(T)$, $\kappa(T)$, $\rho(T)$, and $C_P(T)$, are the electrical conductivity, thermal conductivity, mass density, and specific heat. They are in principle dependent on temperature, even though this dependence may be neglected for some of the materials adopted here. The values assumed for such parameters for realizing a single 1D-1R cell are listed in Table I. As shown, the cell dimensions are 80×80×250 nm, where this latter value is given by two lines of heigth 30 nm each, one resistor of heigth 80 nm and one diode of heigth 110 nm. Table I provides the temperature-independent parameters' values.

A crucial temperature-dependent parameter is given by the equivalent electrical conductivity to be associated to the CF in the oxide. Compared to previous works done by the Authors [33]-[34], and [42], here the CF conducivity model is improved, to properly account for the variation of the conductivity while the RESET switching is in progress. To this end, the conductivity of the CF is formulated as:

$$\sigma(\mathrm{T}) = \sigma_1 \left(1 - \frac{1}{1+\left(\exp\left(-B(T-T_{CRIT})\right)\right)}\right) + \sigma_2, \tag{6}$$

This equation describes a smooth transition from high (σ_1) to low (σ_2) conductive states (see Fig.2). The parameters appearing in (6) strongly depend on the CF status, as for instance the filament actual geometry and the local doping. In the following, we assume the values $\sigma_1 = 3.3 \cdot 10^5\ \Omega^{-1}m^{-1}$ and $\sigma_2 = 10^3\ \Omega^{-1}m^{-1}$, corresponding to a typical dopant density of the CF [35], [47], and the value of the critical temperature T_{CRIT} = 550K taken from [42]-[44]. This parameter is the mean value of the temperature range where the transition occurs. In this way, we can take into account a statistical distribution of the reset, that can actually take place for different temperature values around T_{CRIT}. Here, a uniform distribution is assumed in the range $T_{CRIT} \pm 20\%$, obtained by putting $\mathrm{B} = 0.153$ in (6).

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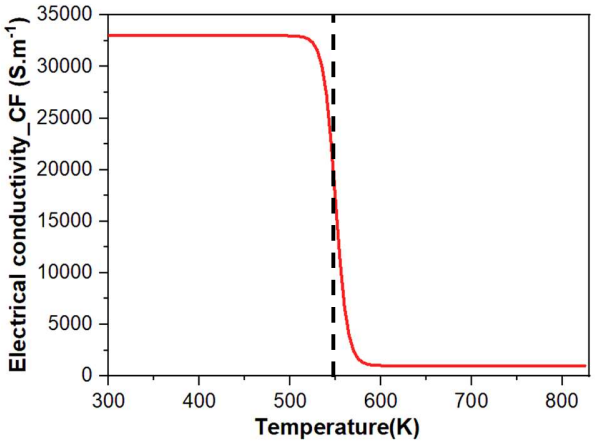

Fig.2. Temperature-dependent electrical conductivity of the conductive filament (Ni).

TABLE I: RRAM GEOMETRY AND PARAMETER VALUES AT T=300 K

Material	CF	Diode			BL/WL		HfO_2
		TiO_2	Pt	Ti	Ni	Cu	
Width (nm)	16	80			80		80
Height (nm)	80	50	30	30	30		80
κ $Wm^{-1}K^{-1}$	23	33.8	8.31	21.9	22	390	Eq.(9)
C_P $Jkg^{-1}K^{-1}$	445	133	710	523	455	400	445
σ_0 ($S.m^{-1}$)	Eq.(6)	3.07k (ON) 50m (OFF)	9.65M	2.5M	0.12M	33.5M	Eq.(7)
α (K^{-1})	-----	--------			2.7 m (Cu)		0.01
ρ ($kg.m^{-3}$)	8.9m	19.8 k	4.2 k	4.5 k	8.9k	8.9k	9.7k

The electrical conductivity of the metal oxide HfO_2, is assumed to be thermally activated by Arrhenius equation [46]:

$$\sigma(T) = \sigma_2 \exp\left(-\frac{E_{AC}}{k_B T}\right), \quad (7)$$

where σ_2 is a pre-exponential factor, $E_{AC} = 0.05$ eV is the activation energy for insulating conduction, k_B is Boltzmann's constant, and T is the local temperature.

The temperature-dependent electrical conductivity of the conductors to be used in this paper for realizing the word and bit lines (Cu and Ni) can be formulated by the classical law:

$$\sigma(T) = \frac{\sigma_0}{1 + \alpha(T - T_0)} \quad (8)$$

where σ_0 is the electrical conductivity at the reference temperature T_0 (here assumed as 300K) and α is the temperature coefficient. For Cu wire with the size dimension adopted here (30 nm), we can assume $\sigma_{Cu0} = 33.5\ MS \cdot m^{-1}$ and $\alpha_{Cu} = 2.7\ mK^{-1}$, [48]. For the nickel wire, it can be assumed $\sigma_{Ni0} = 0.12\ MS \cdot m^{-1}$, neglecting the temperature dependence.

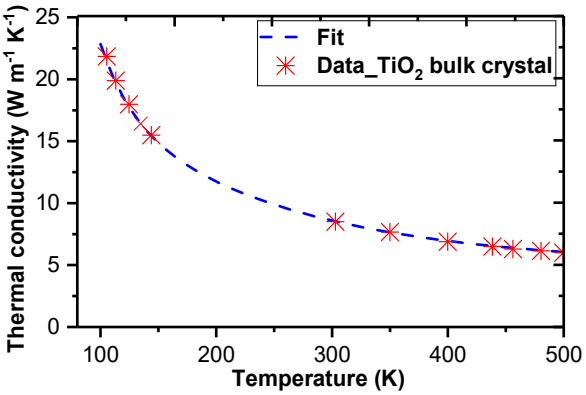

Fig. 3. Thermal conductivity of TiO_2 as function of temperature [35].

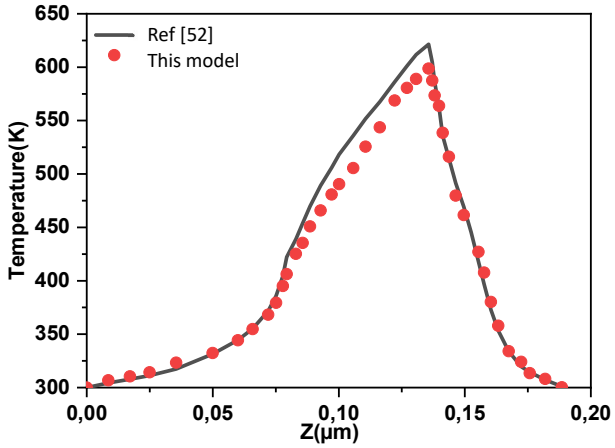

Fig. 4. Model comparison: temperature values computed at the center of a RRAM 1D-1R cell along the vertical axis (z-axis), by means of our model (red dots) and compared to the results in [52] (black line).

Next, the thermal conductivity of the surrounding medium HfO_2 is here modeled as in [49],

$$k_{HfO} = k_{HfO0}(1 + \lambda(T - T_0)), \quad (9)$$

where k_{HfO0} is the value at $T_0 = 300\ K$, and $\lambda = 10\ mK^{-1}$, is the linear thermal coefficient.

In the temperature range of interest for this work (300 K – 1500 K), the thermal conductivity of the CF can be assumed to be constant, with the value provided in Table I [50]. Note that this value may change slightly from metal to metal.

As for the TiO_2 metal oxide film, an experimental characterization of $\kappa(T)$ is provided in [51], and can be fitted as follows, see Fig.3 [34]:

$$k(T) = a_1 \exp(-b_1 T) + a_2 \exp(-b_2 T) + c, \quad (10)$$

with $a_1 = 230.2\ W\,m^{-1}K^{-1}$, $a_2 = 22.3\ W\,m^{-1}k^{-1}$, $b_1 = 0.037\ Wm^{-1}K^{-1}$, $b_2 = 6.5\ Wm^{-1}K^{-1}$, $c = 5.1\ Wm^{-1}K^{-1}$.

After defining the model parameters, proper boundary conditions have been set for both the electrical and thermal problem. Note that in our model the heat is exchanged not only through the conductors but also through the surrounding medium (HfO_2), as in [44]. In addition, the heat is also

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exchanged with an external heatsink, connected to both the top and bottom layers of the 3D structure. The thermal problem is therefore closed with a Dirichlet boundary condition ($T = 300\ K$) at the interfaces with the heatsink, and with adiabatic or Neumann conditions at the other boundaries. As for the electrical conditions, the WL electrode is assumed to be connected to the bias source, from one side or both sides. This means that a known voltage waveform (bias voltage) is imposed on one (or two) bar edge surfaces. The bottom electrodes (bit lines) are grounded. All the other boundary surfaces of the device are given perfect electrical insulating conditions.

Nevertheless, an adaptive tetrahedral mesh is used to implement the numerical model. A proper mesh assessment has been carried out for each simulation, by refining step by step the mesh element size in order to ensure good convergence. The finally adopted mesh has been chosen so to provide a relative error on the estimated maximum temperature less than 0.3%.

In order to compare the Multiphysics model proposed here to the results available in the literature, the 1D-1R RRAM cell studied in [52] was implemented, where the details of geometry and material parameters can be found. The results obtained with the proposed model are successfully compared to those provided in [52], as reported in Fig.4. In details, Fig.4 plots the steady-state temperature at the center of the structure, along the vertical axis of the device (z-axis), after a RESET signal of voltage 1.6V.

III. Signal and Thermal Integrity Analysis on the Novel Architectures

Before analyzing the performance improvement obtained by means of the novel RRAM architectures proposed in this paper, we have first studied the conventional architecture so far proposed in the literature to realize a 4×4×4 crossbar array of 1D-1R cells [29],[30]. The conventional way to arrange 4 layers of 1D-1R memory cells in a vertical stack is that of placing the cells with the same polarity at each layer, and alternating a layer of word lines and a layer of bit lines. The WL bars are biased and connected to the reference electrode of each cell, whereas those of the bit lines are grounded, and connected to the reference electrode of each cell.

This structure has been, for instance, studied in [21] and [22], where the promising features in terms of monolithic integration are highlighted, along with the potential issues related to the crosstalk noise. The Authors have already proposed in [33]-[34] some possible solutions to mitigate these problems, based on replacing the conducting materials of the WL and BL bars. Specifically, modelling results obtained by assuming both conventional conductors (like copper) or novel conducting materials (such as carbon nanotubes [53]) are suggesting the possibility to improve the structure's performance. As pointed out in the introduction, this paper proposes to solve the signal and thermal integrity issues by moving to two alternative architectures, but also considering the possibility of replacing the Ni bars with Cu ones, as done in [33] and [34].

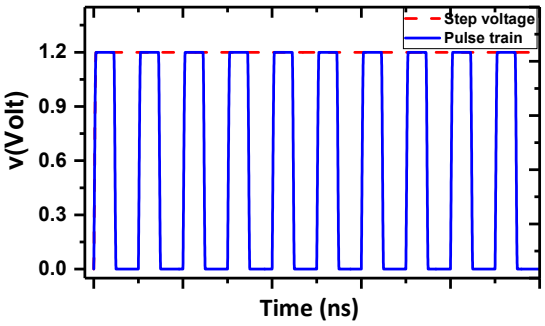

Fig. 5. Time-domain voltage applied to the RRAM cell during the reset switching: actual signal (pulse train, blue) and equivalent signal (voltage step, red).

As already pointed out, the operating condition under examination is a RESET switching that is the most demanding in terms of electrical currents, since it occurs when the cell is in its low-resistance state. The signal to be applied for resetting the targeted memory cells is the train of voltage pulses plotted in Fig.5. It is worth noting that it has been shown that this signal can be replaced by an equivalent step voltage, [34]. The minimum voltage level to ensure the RESET with a reasonable margin is here assumed to be 0.7V. As for the temperature, taking into account the model described in Section II, we assume here $T \geq T_{CRIT} = 550\text{K}$.

The results of the analysis on this reference structure are given in Figs. 6 and 7, and refer to the distributions of the electrical potential and temperature at the steady state, for the case of Ni wires (Fig.6) and Cu wires (Fig.7).

The results in Fig.6 were obtained by considering a bias voltage of 1.4V, applied from one side of two WLs, which means that layers #1 and #3 are active (therefore they are supposed to RESET), whereas layers #2 and #4 are passive and thus they should maintain the SET state. The reason for a so high bias value is that of compensating the huge voltage drop along the Ni wires, which makes the voltage in the cells far from the bias point much lower than that of the nearest ones. Indeed, a bias of 1.4V is necessary to guarantee the minimum level of 0.7 V across the filaments of each cell, as reported in Table II. This bias, however, leads to thermal integrity issues, since the cell temperature reaches values such as all the cells are resetting, including those in the passive layers, as shown in Fig.6b and reported in Table III.

As pointed out, a way to mitigate this issue is to replace the WL and BL nickel bars with copper ones, leaving a small layer of Ni at the top of each cell to provide the active electrode. Moving to Cu bars, the bias needed to provide the minimum reset voltage to all cells may be lowered to 0.9V, as shown in Table II. Indeed, Fig.6a shows an excellent degree of uniformity in the voltage distribution over the Cu crossbar lines when compared to Ni interconnects. As for the thermal response, Figs. 6b and 7b show a clear decrease in terms of maximum temperature when using Cu compared to Ni bars. This solves the problems of unwanted RESET in layer #4 but not in layer #2, where the temperature is about 729 K, still higher than the critical value.

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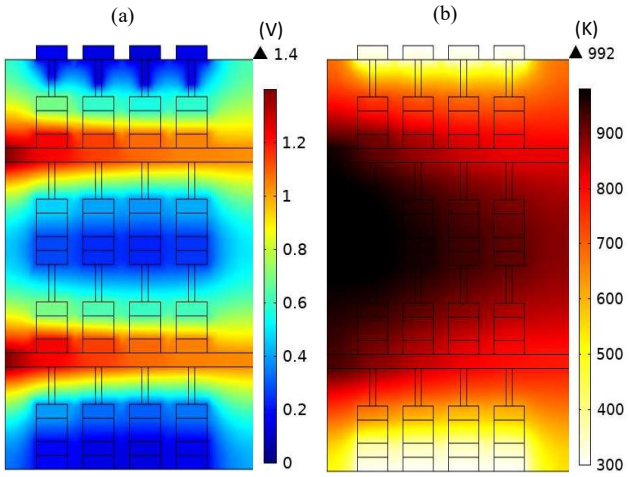

Fig. 6. Reference architecture with Ni wires at the steady state: a) electrical potential distribution; b) temperature distribution.

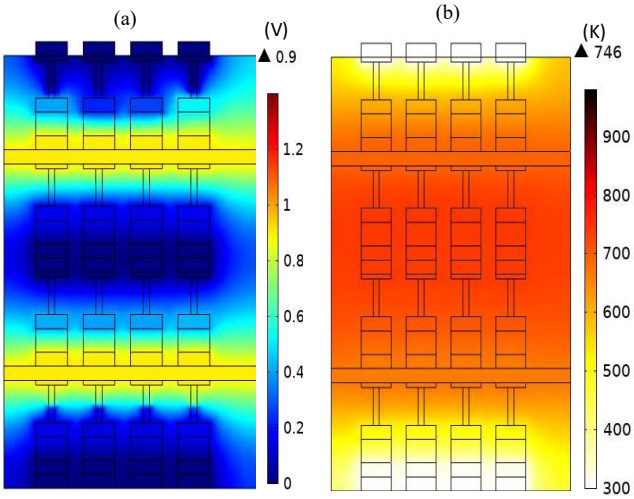

Fig. 7. Reference architecture with Cu wires at the steady state: a) electrical potential distribution; b) temperature distribution.

To summarize, in this conventional reference structure, the heat generation induced by the active layers can change the state of the victim RRAM cells, as an effect of thermal crosstalk, which leads to unwanted RESET operations.

The same kind of analysis has been carried out on the two alternative architectures depicted in Fig.1. To compare the performance in the same conditions, we assume here again a biasing condition leading to two active layers and two passive ones. Note that in the reverse architecture (Fig1a), in order to switch two layers, it is sufficient to apply the bias to only one WL. In other words, the first main advantage of this solution is the possibility to double the number of cells that can be driven by a single biased interconnect layer. Given this consideration, now the active layers are #1 and #2, and the passive ones are #3 and #4.

The electrical potential and the temperature distributions of the 1D1R-1R1D reverse architecture are given in Figs.8 and 9 for Ni and Cu bars, respectively. In the case of Ni bars, the voltage drop requires the application of minimum bias voltage of 1.2V at both sides of the WL, see Table II.

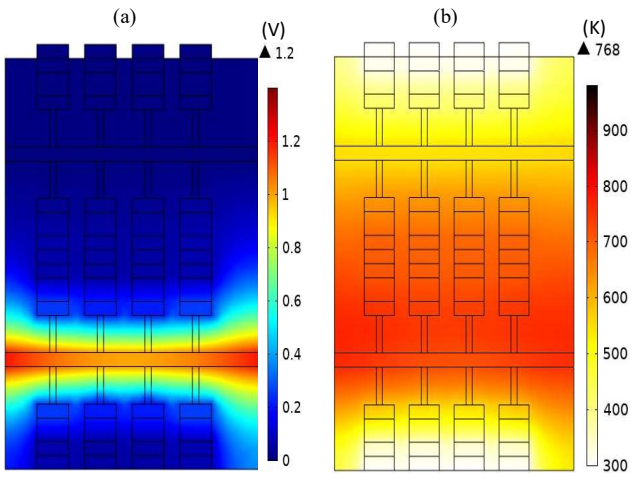

Fig. 8. Reverse architecture with Ni wires at the steady state: a) electrical potential distribution; b) temperature distribution.

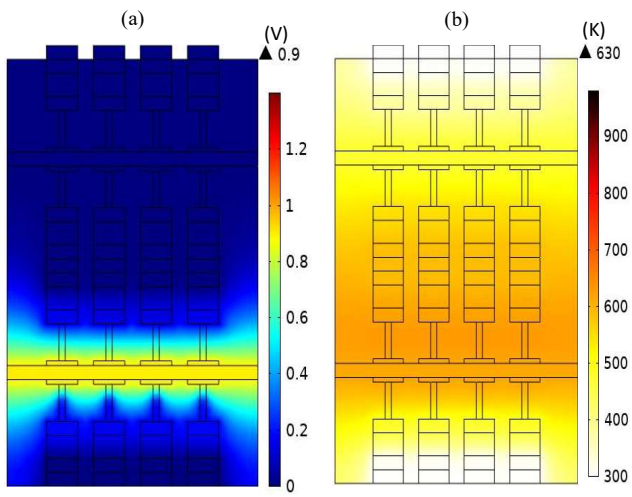

Fig. 9. Reverse architecture with Cu wires at the steady state: a) electrical potential distribution; b) temperature distribution.

Instead, the use of Cu in this reverse structure has advantages in terms of bias, since it can be applied from one WL side only, with a lower level (0.9V), then improving the energy efficiency with respect to the Ni case, see Table II. As for the thermal distributions in Figs. 8b and 9b, once again the use of Cu reduces the temperature inside the structure, and in particular inside the cells of the passive layers. As for the reference case, it is evident that the steady-state temperature rise follows the increase of the voltage level. The high voltage level required on the Ni wires reduces the energy efficiency and increases the Joule power dissipated into the conductors, leading to unwanted RESET switching. Table III clearly shows that the reverse architecture with Ni still has thermal crosstalk problems (cells of layer #3), whereas they are completely solved with the Cu bars.

The second architecture proposed here is the complementary one (CRS), see Fig.1d, presented in the introduction, where two anti-serial memristive elements share a common electrode. When the voltage is applied to the WL of the upper cell and to the ground of the BL of the lower one, both cells are activated. This offers an interesting

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perspective for solving the problem of the sneak path, without the introduction of any selector element, like the diode seen in the cells so far studied. The CRS cell presents a high overall resistance once, storing bit data, it effectively limits the leakage current in crossbar structures.

The results obtained for such a structure are given in Figs. 10 and 11, for Ni and Cu bars, respectively. Note that the active layers and the passive ones are the same as with the reverse structure.

Table II shows that for the two materials a bias level of 1.3V (for Ni) and 0.8 V (for Cu) is enough to guarantee the switching level to the cells. The results of the thermal analysis are plotted in Figs. 10b and 11b and reported in Table III provide a similar outcome as for the reverse structure, with a thermal crosstalk problem only partially solved for the Ni case (cells in layer #3 have still unwanted RESET) and completely solved for the Cu case.

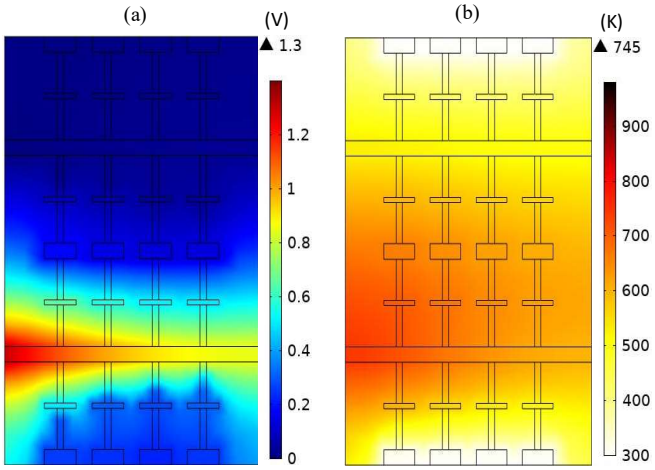

Fig. 10. CRS architecture with Ni wires at the steady state: a) electrical potential distribution; b) temperature distribution.

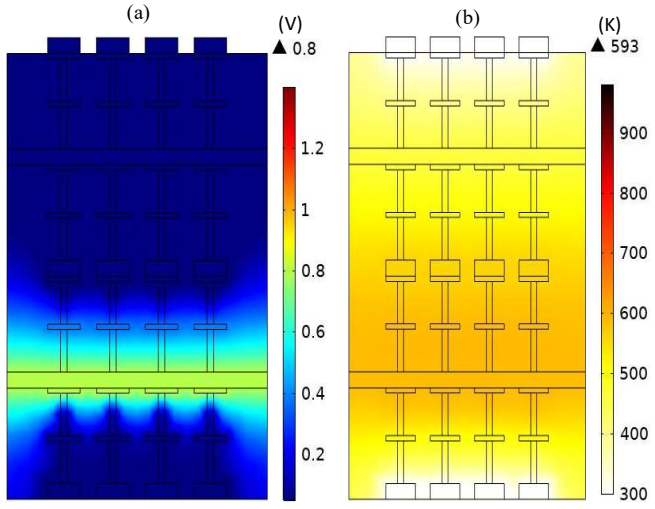

Fig. 11. CRS architecture with Cu wires at the steady state: a) electrical potential distribution; b) temperature distribution.

TABLE II: VOLTAGE LEVELS (V) ACROSS THE CF OF THE CELLS ALONG A BAR, FOR ALL THE CONSIDERED CASES

Architectures		Reference	Reverse	CRS
Ni	**Bias**	**1.4V**	**1.2V (both sides)**	**1.3 V**
	Cell1	0.80	0.73	1.02
	Cell2	0.79	0.71	0.89
	Cell3	0.76	0.71	0.81
	Cell4	0.70	0.70	0.75
Cu	**Bias**	**0.9 V**	**0.9V**	**0.8V**
	Cell1	0.75	0.72	0.79
	Cell2	0.76	0.73	0.79
	Cell3	0.76	0.73	0.79
	Cell4	0.74	0.72	0.78

TABLE III: MAXIMUM TEMPERATURE (K) OF THE CFS FOR ALL THE CONSIDERED CASES.

	Layer state	Reference	Reverse	CRS
Ni	**Bias**	**1.4V**	**1.2V (both sides)**	**1.3 V**
	Layer #1	802.81	675.76	685.29
	Layer #2	972.74	757.22	737.11
	Layer #3	960.04	592.01	573.10
	Layer #4	581.00	488.30	487.91
Cu	**Bias**	**0.9 V**	**0.9V**	**0.8V**
	Layer #1	619.21	571.59	569.70
	Layer #2	729.12	626.35	591.76
	Layer #3	728.47	510.23	489.39
	Layer #4	489.48	430.00	431.63

TABLE IV. MAXIMUM TEMPERATURE (K) IN THE TWO VICTIM CELLS OF LAYER #1 OF THE 1D1R-1R1D STRUCTURE FOR DIFFERENT CELL SPACING

Layer #1	2nd victim cell	4th victim cell
Ni (2 F)	596.79 K	539.12 K
Ni (2.25 F)	576.37 K	530.12 K
Cu (2 F)	521.91 K	487.72 K
Cu (2.25 F)	501.78 K	473.78 K

From the thermal distribution seen in Fig. 10, we note that the maximum temperature decrease compared to the conventional structure (Table III), following the decrease of the applied bias. However, when compared with the 1D1R1-1R1D integration (Fig.7 and Fig.8) we took attention that this maximum is declined to a value less than the critical temperature in the two victim layers (about 430K) and then can serve to limit the effect of thermal crosstalk problems. Furthermore, we can confirm this through the results in Table III for the maximum temperature for each layer.

Finally, it can be pointed out that the residual thermal crosstalk issue that is found in the two proposed architectures can be solved in an alternative way, without replacing the Ni bars with the Cu ones. Indeed, the crosstalk can be mitigated by following the classical rule of widening the cell separation. Let us for instance refer to the reverse 1D1R-1R1D architecture, considering only one layer (layer #1) and assuming that only cells 1 and 3 are biased, whereas 2 and 4 are passive. In the previous cases, the horizontal distance between the cells has been assumed to be equal to 2F, being

F the size of the feature cell. Table IV shows the decrease of the temperature obtained in the two passive cells, by increasing the cell separation, for both Ni and Cu interconnects. A significant decrease in thermal crosstalk is noted when the active cells are spaced away from the victim cells, so that this issue can be completely solved with a proper increase of spacing. Of course, this solution avoids the change of the bar material, but decreases the density of memory for a given volume.

IV. Conclusions

This paper demonstrates the possibility of mitigating or even solving some of the major electrothermal issues suffered by 3D stacked arrays of 1D-1R RRAMs. Two novel architectures are proposed to stack these memories, one based on a reverse arrangement (reverse) and the other one based on a complementary structure (CRS). Both of them are shown to optimize the bias management, whereas the latter one (CRS) provides the additional benefit to avoid the use of diodes. A comparative analysis has been carried out with reference to the RESET process. Compared to the reference architecture, both of the novel architectures are able to drive the RESET with almost the same values of the bias voltage. This level can be strongly reduced if the electrical interconnects of the array are realized with copper instead of nickel. Indeed, this is a way to solve the problem of the significant voltage drop along the interconnects introduced by the high resistivity of Ni wires.

The new architectures are also demonstrated to strongly mitigate or even solve the problem of the unwanted RESET switching associated with the thermal crosstalk between adjacent cells. Indeed, once moving to these architectures, this problem can be solved by replacing Ni wires with Cu ones, or by increasing the spacing between cells.

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